1. Description

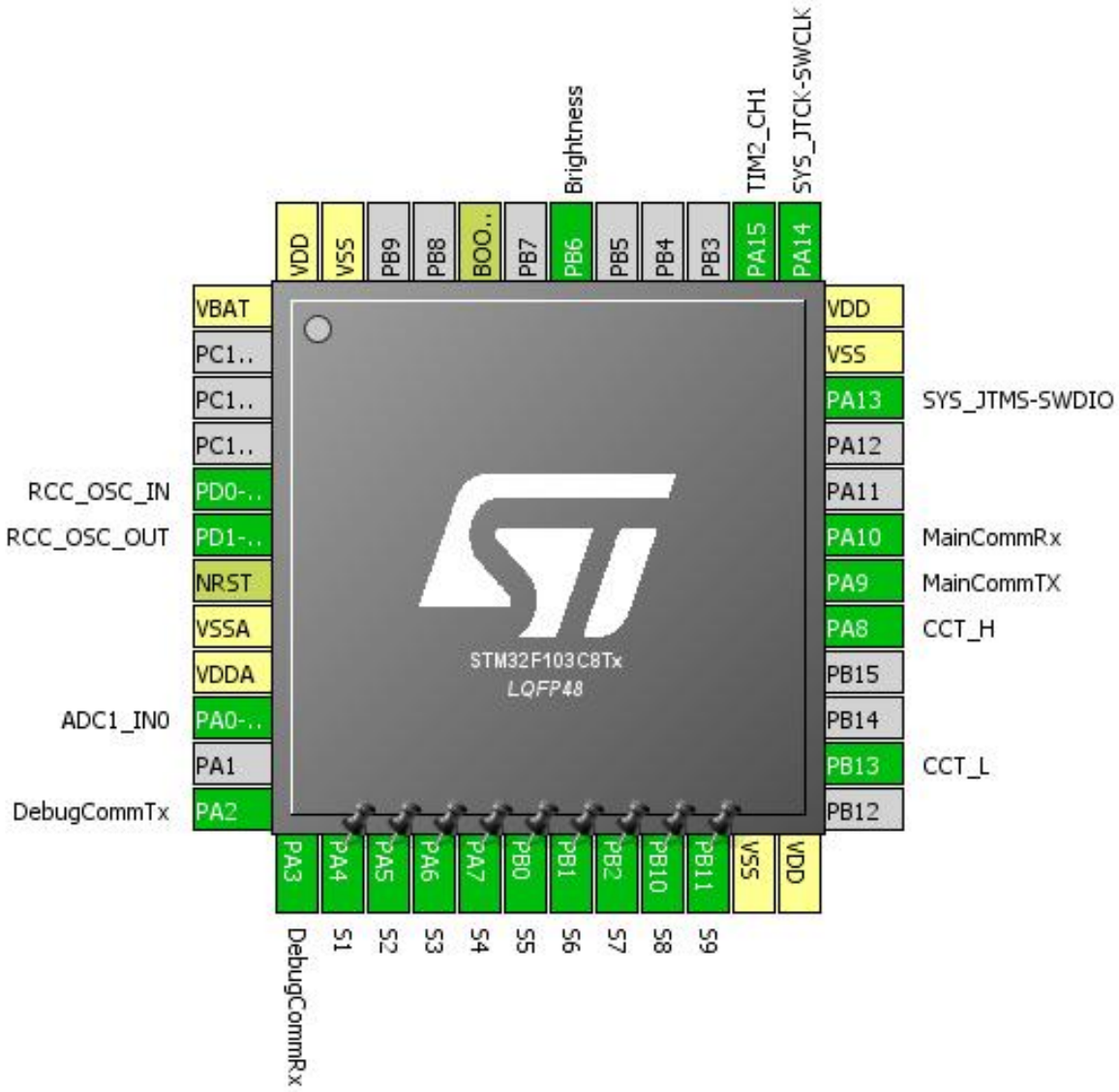
1.1. Project

Project Name	CCT_App
Board Name	CCT_App
Generated with:	STM32CubeMX 4.19.0
Date	06/07/2018

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F103
MCU name	STM32F103C8Tx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration

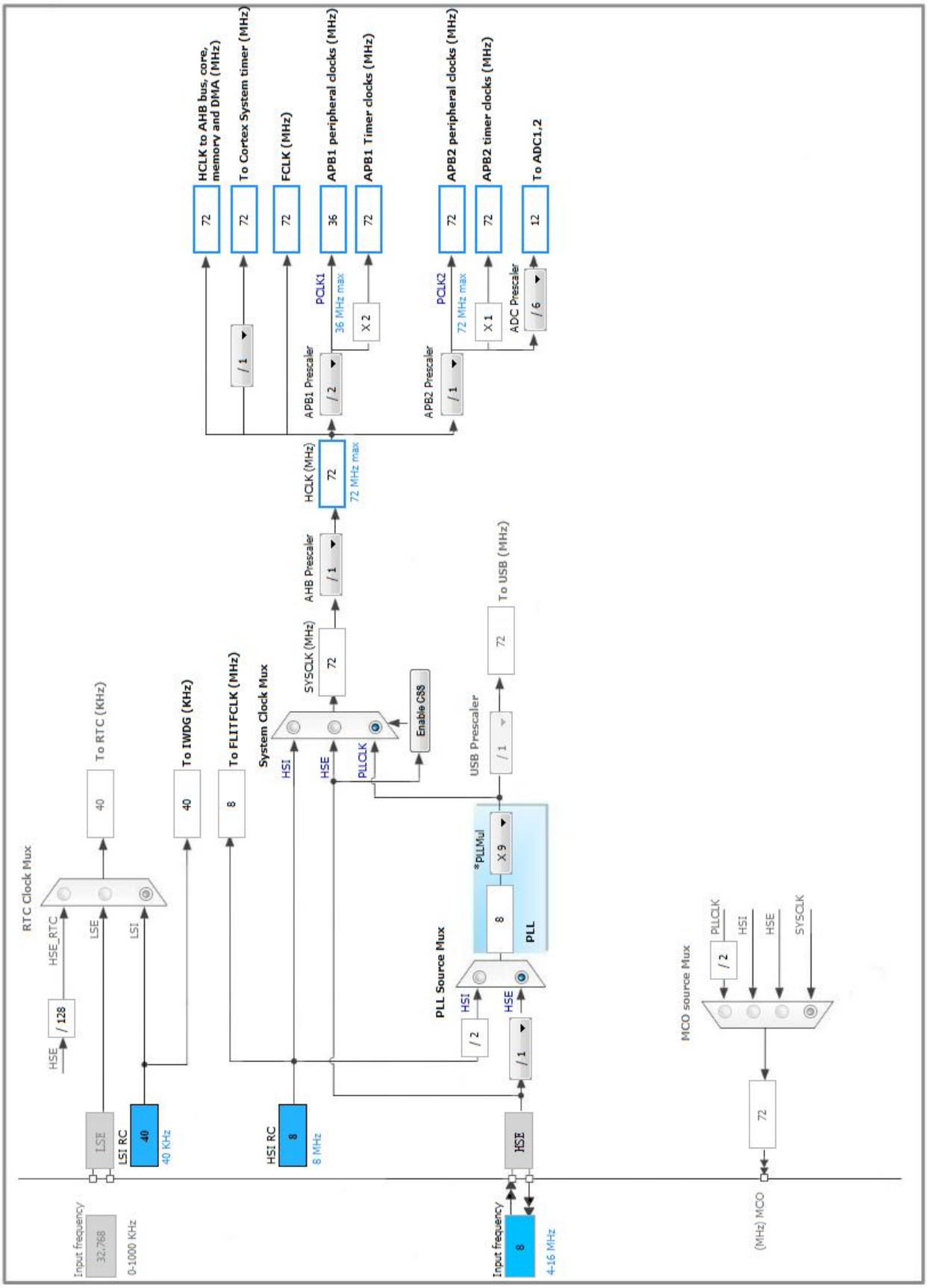


3. Pins Configuration

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PD0-OSC_IN	I/O	RCC_OSC_IN	
6	PD1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA	Power		
9	VDDA	Power		
10	PA0-WKUP	I/O	ADC1_IN0	
12	PA2	I/O	USART2_TX	DebugCommTx
13	PA3	I/O	USART2_RX	DebugCommRx
14	PA4 *	I/O	GPIO_Input	S1
15	PA5 *	I/O	GPIO_Input	S2
16	PA6 *	I/O	GPIO_Input	S3
17	PA7 *	I/O	GPIO_Input	S4
18	PB0 *	I/O	GPIO_Input	S5
19	PB1 *	I/O	GPIO_Input	S6
20	PB2 *	I/O	GPIO_Input	S7
21	PB10 *	I/O	GPIO_Input	S8
22	PB11 *	I/O	GPIO_Input	S9
23	VSS	Power		
24	VDD	Power		
26	PB13	I/O	TIM1_CH1N	CCT_L
29	PA8	I/O	TIM1_CH1	CCT_H
30	PA9	I/O	USART1_TX	MainCommTX
31	PA10	I/O	USART1_RX	MainCommRx
34	PA13	I/O	SYS_JTMS-SWDIO	
35	VSS	Power		
36	VDD	Power		
37	PA14	I/O	SYS_JTCK-SWCLK	
38	PA15	I/O	TIM2_CH1	
42	PB6	I/O	TIM4_CH1	Brightness
44	BOOT0	Boot		
47	VSS	Power		
48	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. IPs and Middleware Configuration

5.1. ADC1

mode: IN0

5.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 0
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

5.2. IWDG

mode: Activated

5.2.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

5.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

5.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Prefetch Buffer	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

5.4. SYS

Debug: Serial Wire

Timebase Source: SysTick

5.5. TIM1

Clock Source : Internal Clock

Channel1: Output Compare CH1 CH1N

5.5.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off
Dead Time	0

Output Compare Channel 1 and 1N:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High
CHN Polarity	High
CH Idle State	Reset
CHN Idle State	Reset

5.6. TIM2

Clock Source : Internal Clock

Channel1: Input Capture direct mode

5.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

5.7. TIM4

mode: Clock Source

Channel1: Output Compare CH1

5.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	0
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode	Disable (no sync between this TIM (Master) and its Slaves
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Output Compare Channel 1:

Mode	Frozen (used for Timing base)
Pulse (16 bits value)	0
CH Polarity	High

5.8. USART1

Mode: Asynchronous

5.8.1. Parameter Settings:

Basic Parameters:

Baud Rate	**9600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

5.9. USART2

Mode: Asynchronous

5.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

6. System Configuration

6.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0-WKUP	ADC1_IN0	Analog mode	n/a	n/a	
RCC	PD0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PD1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PB13	TIM1_CH1N	Alternate Function Push Pull	n/a	Low	CCT_L
	PA8	TIM1_CH1	Alternate Function Push Pull	n/a	Low	CCT_H
TIM2	PA15	TIM2_CH1	Input mode	No pull-up and no pull-down	n/a	
TIM4	PB6	TIM4_CH1	Alternate Function Push Pull	n/a	Low	Brightness
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	MainCommTX
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	MainCommRx
USART2	PA2	USART2_TX	Alternate Function Push Pull	n/a	**High ***	DebugCommTx
	PA3	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	DebugCommRx
GPIO	PA4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S1
	PA5	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S2
	PA6	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S3
	PA7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S4
	PB0	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S5
	PB1	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S6
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S7
	PB10	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S8
	PB11	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	S9

6.2. DMA configuration

nothing configured in DMA service

6.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM1 break interrupt	unused		
TIM1 update interrupt	unused		
TIM1 trigger and commutation interrupts	unused		
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM4 global interrupt	unused		
USART2 global interrupt	unused		

*** User modified value**

7. Power Consumption Calculator report

7.1. Microcontroller Selection

Series	STM32F1
Line	STM32F103
MCU	STM32F103C8Tx
Datasheet	13587_Rev17

7.2. Parameter Selection

Temperature	25
Vdd	3.3

8. Software Project

8.1. Project Settings

Name	Value
Project Name	CCT_App
Project Folder	F:\CCT_Workspace\CCT_App\CCT_App
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F1 V1.4.0

8.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No