Lecture 10: MOSFET

VE311 Electronic Circuits

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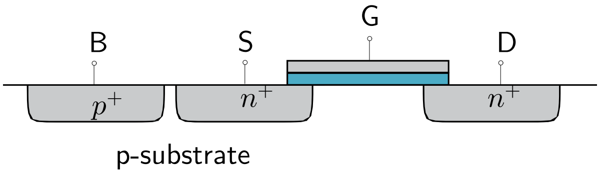
Recap of Last Lecture

- BJT Circuits

Topics to Be Covered

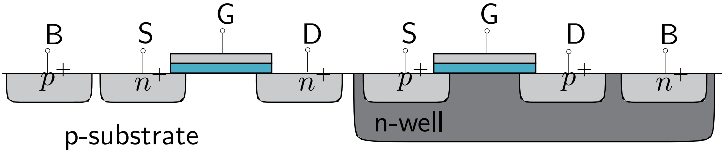
- MOSFET

NMOS FET



- MOS = Metal-Oxide-Semiconductor
- FET = Field effect Transistor
- CMOS Technology keeps on reducing t_{ox} and L_{eff} (Moore’s Law).
- Substrate (Body) of NMOS is generally connected to ground.
- See Chapter 17 for the introduction of CMOS fabrication technology.

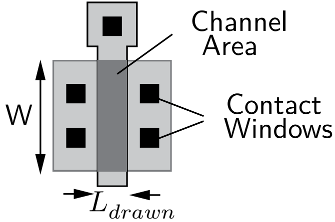
CMOS



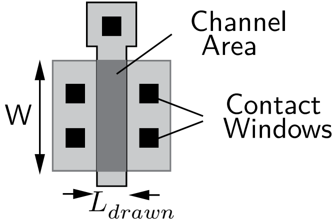
- CMOS = Complementary MOS
- Substrate (Body) of NMOS is generally connected to ground.
- N-well (Body) of PMOS is generally connected to V_{DD}.

Layout

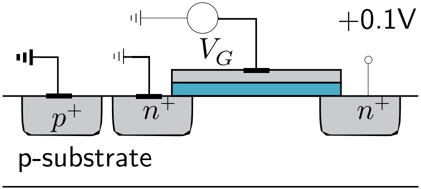
NMOS

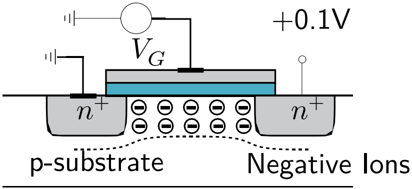


PMOS



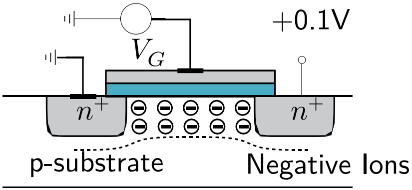
Threshold Voltage (V_{TH}) for NMOS





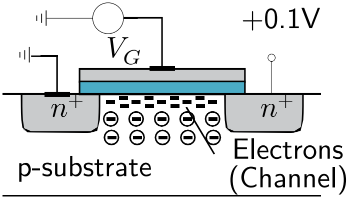
- $V_G = 0V$
- No current flow
- As VG increases from zero, holes in p-substrate are repelled, leaving negative ions (ionized boron dopants) behind to form a **depletion region**.
- Positive charges are mirrored at the gate.

Threshold Voltage (V_{TH}) for NMOS



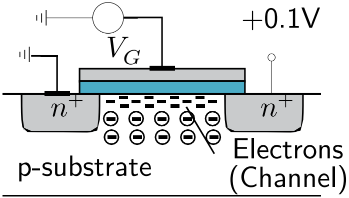
- No charge carriers (electrons or holes) in the channel, so no current flow.
- Higher V_G further increases the width of the **depletion region**.

Threshold Voltage (V_{TH}) for NMOS



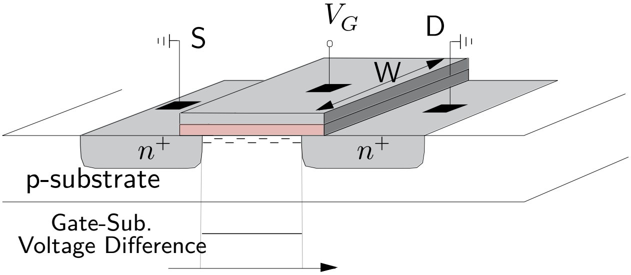
- When V_G reaches a sufficiently positive value, a channel of electrons (**inversion layer**) is formed beneath the gate oxide.
- Electrons flow from "source" to "drain". Equivalently, current flows from "drain" to "source".
- The value of V_G at which the inversion layer forms is the **threshold voltage (V_{TH})**.

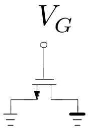
Threshold Voltage (V_{TH}) for NMOS



- If V_G rises further, the charges in the depletion region remain relatively constant, whereas the charges in the inversion layer increase rapidly.

NMOS I-V Characteristics (Triode)





NMOS I-V Characteristics (Triode)

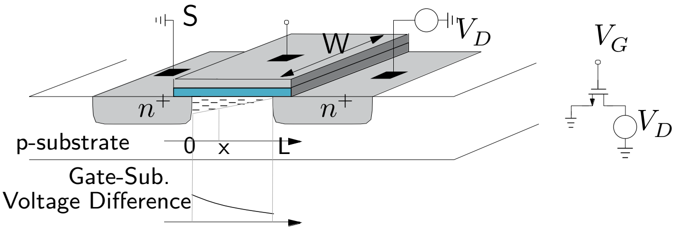
For $V_{GS} \geq V_{TH}$

$$Q = -WL_{eff}C_{ox}(V_{GS} - V_{TH})(\text{unit: coulomb}) \quad (1)$$

$$Q_d = -WC_{ox}(V_{GS} - V_{TH})(\text{unit: coulomb} \cdot m^{-1}) \quad (2)$$

$$\begin{aligned} &C_{ox}(\text{gate oxide capacitance per unit area}) \\ &= \epsilon_{\text{silicon oxide}} / t_{ox} \\ &= \left[8.85 \times 10^{-12}(F/m) \times 3.9\right] / t_{ox} \end{aligned} \quad (3)$$

NMOS I-V Characteristics (Triode)



NMOS I-V Characteristics (Triode)

$$I_D = Q_d \times V = Q_d \times (\mu_n \varepsilon) = -WC_{ox}\left[V_{GS} - V_{TH} - V(x)\right] \times (\mu_n \varepsilon) \quad \varepsilon = -dV(x)/dx$$

$$= W_{ox}\left[V_{GS} - V_{TH} - V(x)\right] \times \mu_n \times \frac{dV(x)}{dx} \tag{4}$$

$$\int_{x=0}^{x=L_{\text{eff}}} I_D \cdot dx = \int_{V(0)=0}^{V(L)=V_{DS}} \mu_n C_{ox} W\left[V_{GS} - V_{TH} - V(x)\right] \cdot dV(x) \tag{5}$$

$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}}\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}{V_{DS}}^2\right] \quad I_D : \text{constant along channel} \tag{6}$$

NMOS I-V Characteristics (Triode)

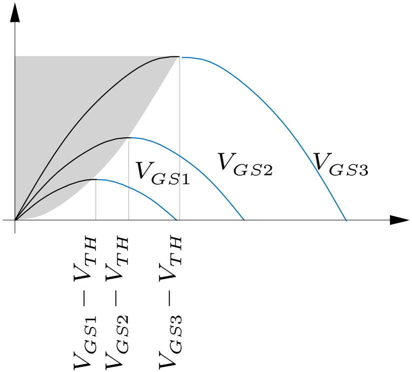
$$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \tag{7}$$

$$I_{D,\ \mathsf{max}} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \quad V_{DS} = V_{GS} - V_{TH} \tag{8}$$

NMOS I-V Characteristics (Triode)

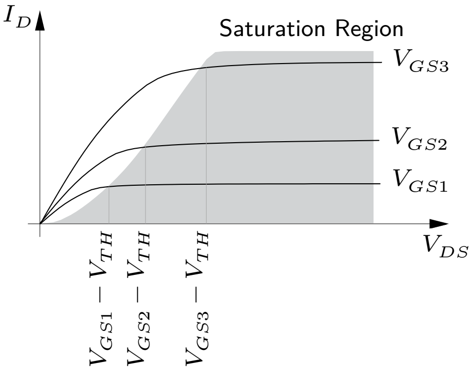
Deep triode region

$$R_{on} = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right)_{\text{eff}} (V_{GS} - V_{TH})} \tag{9}$$



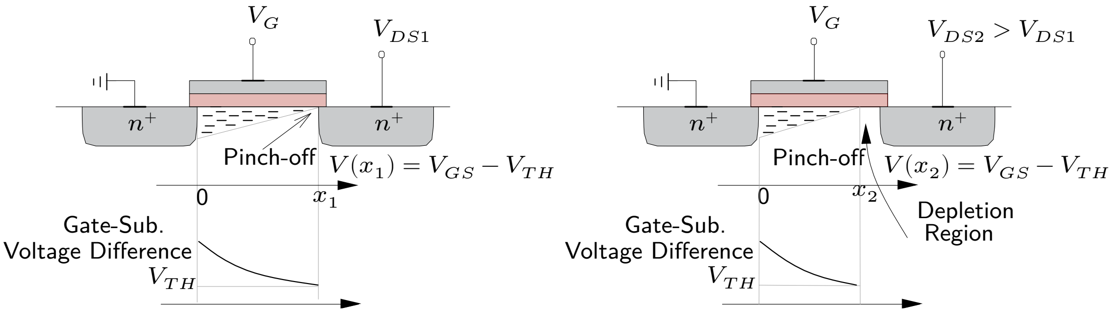
- For digital circuit, MOSFET, as a switch, usually operates in deep triode region.
- This is why reducing t_{ox} and L_{eff} can improve speed.

Saturation Region



- For $V_{DS} > V_{GS} - V_{TH}$, I_D becomes relatively constant.
- $V_{DS} = V_{GS} - V_{TH}$ is the minimum value for the NMOS to operate in saturation region.

Saturation Region



Saturation Region

$$\int_{x=0}^{x=L'} I_D \cdot dx = \int_{V(0)=0}^{V(L')=V_{GS}-V_{TH}} \mu_n C_{ox} W \left[V_{GS} - V_{TH} - V(x)\right] \cdot dV(x) \qquad (10)$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}\left(V_{GS} - V_{TH}\right)^2 \quad (11)$$

I_D: constant along channel
L': the point at which Q_d drops to zero
$V_{GS} - V_{TH}$: the overdrive voltage

- Electron velocity ($v = I_D/Q_d$) becomes tremendously high at the pinch off point ($Q_d \to 0$), such that electrons shoot through the depletion region and arrive at the drain terminal.

Channel-Length Modulation

$$\begin{cases} I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L'}\left(V_{GS} - V_{TH}\right)^2 \\ L' = L_{eff} - \Delta L \\ \frac{1}{L'} = \frac{1}{L_{eff} - \Delta L} = \frac{1}{L_{eff}} \cdot \frac{1}{1 - \frac{\Delta L}{L_{eff}}} \approx \frac{1}{L_{eff}} \cdot \left(1 + \frac{\Delta L}{L_{eff}}\right) \end{cases} \tag{12}$$

$$\begin{aligned} I_D &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}\left(V_{GS} - V_{TH}\right)^2\left(1 + \frac{\Delta L}{L_{eff}}\right) \\ &= \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right) \end{aligned} \tag{13}$$

Channel-Length Modulation

$$r_o = \frac{\partial V_{DS}}{\partial I_D} = 1/\frac{\partial I_D}{\partial V_{DS}} \tag{14}$$

$$= \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \cdot \lambda} \tag{15}$$

$$\approx \frac{1}{I_D \cdot \lambda} \tag{16}$$

Body Effect

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|2\Phi_F + V_{SB}|} - \sqrt{|2\Phi_F|}) \tag{17}$$

$$\Phi_F = \frac{kT}{q} \ln \frac{N_{sub}}{n_i} \tag{18}$$

$$\gamma = \frac{\sqrt{2q\epsilon_{Si} N_{sub}}}{C_{ox}} \tag{19}$$

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L'} \left(V_{GS} - V_{TH}\right)^2 \tag{20}$$

Body Effect

$$\begin{aligned} gm_b &= \frac{\partial I_D}{\partial V_{SB}} = \frac{\partial I_D}{\partial V_{TH}} \cdot \frac{\partial V_{TH}}{\partial V_{SB}} \\ &= -\mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH}) \cdot \frac{\partial V_{TH}}{\partial V_{SB}} \\ &= -\mu_n C_{ox} \frac{W}{L'} (V_{GS} - V_{TH}) \cdot \frac{\gamma}{2} \frac{1}{\sqrt{|2\Phi_F + V_{SB}|}} \\ &= -gm \cdot \eta \end{aligned} \tag{21}$$

Body Effect

- V_{GS} increases, I_D increases.
- V_{SB} increases, V_{TH} increases and thus I_D decreases.

Spice Models

NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

Spice Models

- Simulators such as SPICE and Cadence need accurate models for each device.
- Above is the simplest MOS SPICE model, known as "Level 1," and provide typical values for each parameter corresponding to 0.5-μm technology.

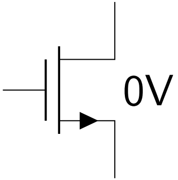
Spice Models

VTO : threshold voltage with zero V_{SB} (unit : V)
GAMMA : body effect coefficient (unit : $V^{1/2}$)
PHI : $2\Phi_F$ (unit : V)
TOX : gate oxide thickness (unit : m)
NSUB : substrate doping (unit : cm^{-3})
LD : source/drain side diffusion (unit : m)
UO : channel mobility (unit : $cm^2/V/s$)
LAMBDA : channel-length modulation coefficient (unit : V^{-1})

Spice Models

CJ : source/drain bottom-plate junction capacitance per unit area (unit : F/m^2)
CJSW : source/drain sidewall junction capacitance per unit length (unit : F/m)
PB : source / drain junction built-in potential (unit : V)
MJ : exponent in CJ equation (unitless)
MJSW : exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit : F/m)
CGSO : gate-source overlap capacitance per unit width (unit : F/m)
JS : source/drain leakage current per unit area (unit : A/m^2)

Body Effect Example



$$\left(\frac{W_{drawn}}{L_{drawn}}\right) = \frac{10\mu m}{2\mu m} \tag{22}$$

$$V_{th} = 0.7 + 0.45(\sqrt{0.9+1} - \sqrt{0.9}) \tag{23}$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{Gs} - V_{th})^2(1 + \lambda V_{DS}) \tag{24}$$