VE311 Electronic Circuit Homework 4

Due: **July 4th**

Note:

1) Please use A4 size paper or page.

2) Please clearly state out your final result for each question.

3) Please attach the screenshot of Pspice simulation result if necessary.

Question 1. MOSFET DC Biasing

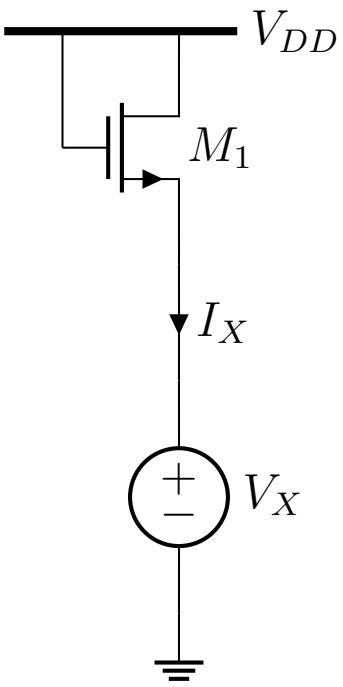
Use the drain current equations below. Don't consider channel-length modulation and body effect. Assuming $\mu_n = 350 \times 10^{-4} m^2/V/s$, $\mu_p = 350 \times 10^{-4} m^2/V/s$, $V_{TH} = 0.7V$ (NMOS), $V_{TH} = -0.8V$ (PMOS), $W_{drawn}/L_{drawn} = 20\mu m/2\mu m$, $t_{ox} = 9 \times 10^{-9} m$, $L_D = 0.08\mu m$, sketch I_X of M_1 as a function of V_X increasing from 0V to $V_{DD} = 5V$.

(1) $$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \text{ (NMOS in triode region)}$$

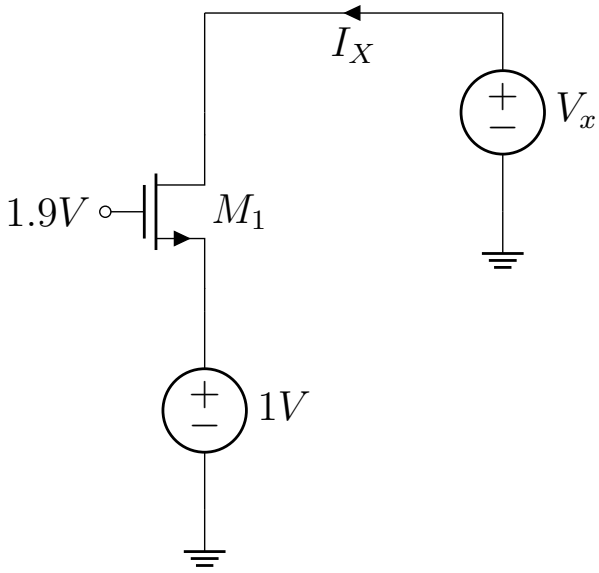
(2) $$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 \text{ (NMOS in saturation region)}$$

(3) $$I_D = \mu_p C_{ox} \frac{W}{L_{eff}} \left[(V_{SG} - |V_{TH}|) V_{SD} - \frac{1}{2} V_{SD}^2 \right] \text{ (PMOS in triode region)}$$

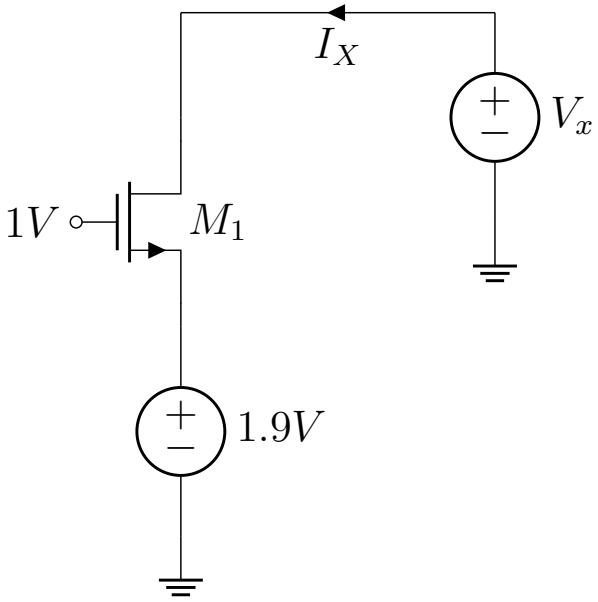
(4) $$I_D = \mu_p C_{ox} \frac{W}{L_{eff}} (V_{SG} - |V_{TH}|)^2 \text{ (PMOS in saturation region)}$$



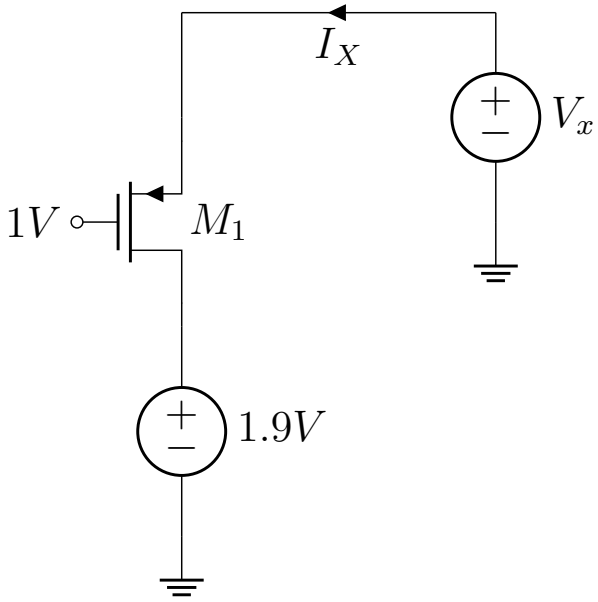
(A)



(B)



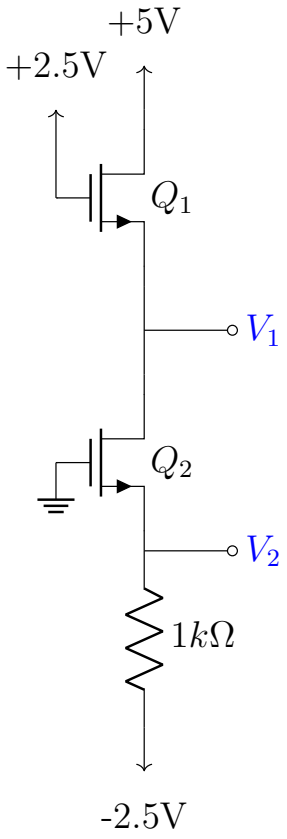
(C)



(D)

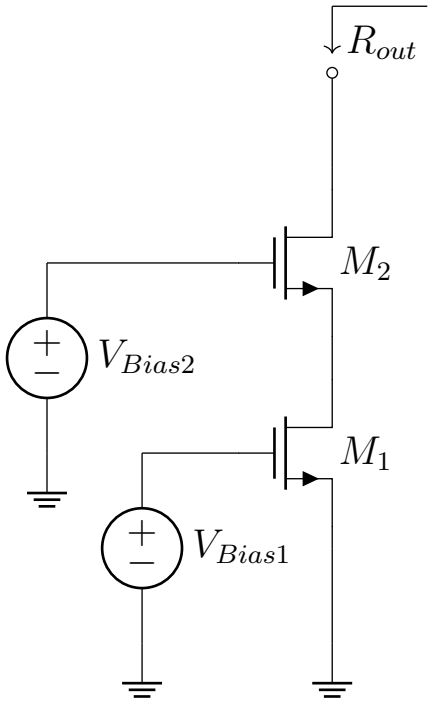
Question 2. Combination of MOSFET

For the circuit below, find the labeled node voltages. The NMOS transistor has $V_{TH} = 0.9V$, $k_n = \mu_n C_{ox}(W/L) = 1.5mA/V^2$.

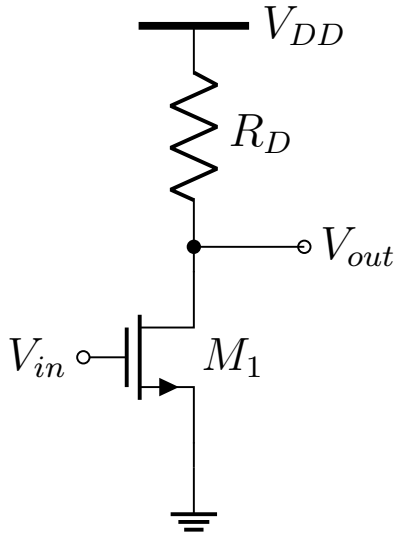


Question 3. Small Signal of of MOSFET

The circuit shown below is a MOSFET cascode amplifier. Draw the small signal model and derive R_{out} for the amplifier. Assume transistors M_1 and M_2 are in saturation and include r_O in your calculation.



Question 4. Common-Source with Resistive Load
Assume $\lambda = 0$ and $\gamma = 0$. For $V_{DD} = 5V$, V_{in} = 0.9 V + small signal, $R_D = 15k\Omega$ and $L_{drawn} = 2\mu m$, find out the value W_{drawn} to obtain a voltage gain $|A_v| > 10$ and V_{OUT} (the DC biasing voltage at the output) close to 2.5 V as much as possible.



NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

VTO : threshold voltage with zero V_{SB} (unit : V)
GAMMA : body effect coefficient (unit : $V^{1/2}$)
PHI : $2\Phi_F$ (unit : V)
TOX : gate oxide thickness (unit : m)
NSUB : substrate doping (unit : cm^{-3})
LD : source/drain side diffusion (unit : m)
UO : channel mobility (unit : $cm^2/V/s$)
LAMBDA : channel-length modulation coefficient (unit : V^{-1})
CJ : source/drain bottom-plate junction capacitance per unit area (unit : F/m^2)
CJSW : source/drain sidewall junction capacitance per unit length (unit : F/m)
PB : source / drain junction built-in potential (unit : V)

MJ : exponent in CJ equation (unitless)
MJSW : exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit : F/m)
CGSO : gate-source overlap capacitance per unit width (unit : F/m)
JS : source/drain leakage current per unit area (unit A/m^2)
Vacuum permittivity (ϵ_o) = 8.85×10^{-12}(F/m)
Silicon oxide dielectric constant (ϵ_r) = 3.9