VE311 Electronic Circuit Homework 4

Due: **July 4th**

Note:

1) *Please use A4 size paper or page.*
2) *Please clearly state out your final result for each question.*
3) *Please attach the screenshot of Pspice simulation result if necessary.*

Question 1. MOSFET DC Biasing

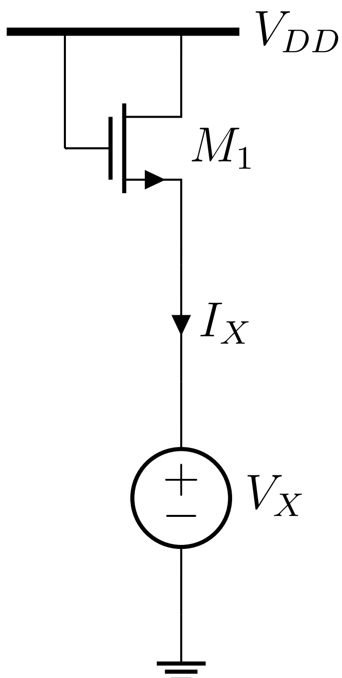
Use the drain current equations below. Don't consider channel-length modulation and body effect. Assuming $\mu_n = 350 \times 10^{-4} m^2/V/s$, $\mu_p = 350 \times 10^{-4} m^2/V/s$, $V_{TH} = 0.7V$ (NMOS), $V_{TH} = -0.8V$ (PMOS), $W_{drawn}/L_{drawn} = 20\mu m/2\mu m$, $t_{ox} = 9 \times 10^{-9} m$, $L_D = 0.08\mu m$, sketch I_X of M_1 as a function of V_X increasing from 0V to $V_{DD} = 5V$.

(1) $$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left[\left(V_{GS} - V_{TH}\right) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \text{(NMOS in triode region)}$$

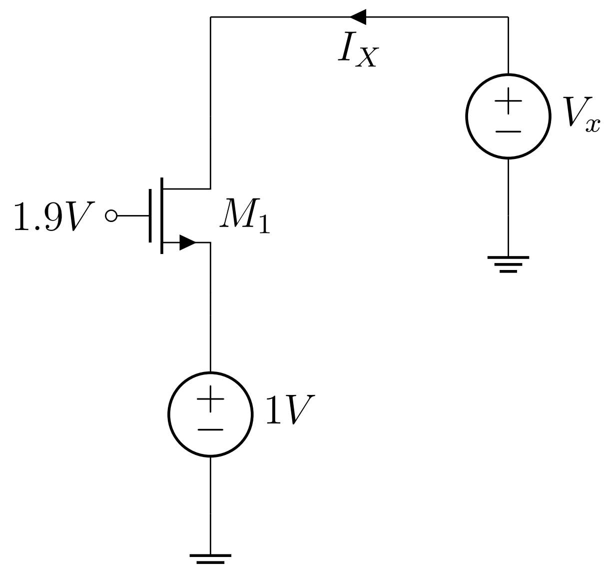
(2) $$I_D = \mu_n C_{ox} \frac{W}{L_{eff}} \left(V_{GS} - V_{TH}\right)^2 \text{(NMOS in saturation region)}$$

(3) $$I_D = \mu_p C_{ox} \frac{W}{L_{eff}} \left[\left(V_{SG} - |V_{TH}|\right) V_{SD} - \frac{1}{2} V_{SD}^2 \right] \text{(PMOS in triode region)}$$

(4) $$I_D = \mu_p C_{ox} \frac{W}{L_{eff}} \left(V_{SG} - |V_{TH}|\right)^2 \text{(PMOS in saturation region)}$$



(A)



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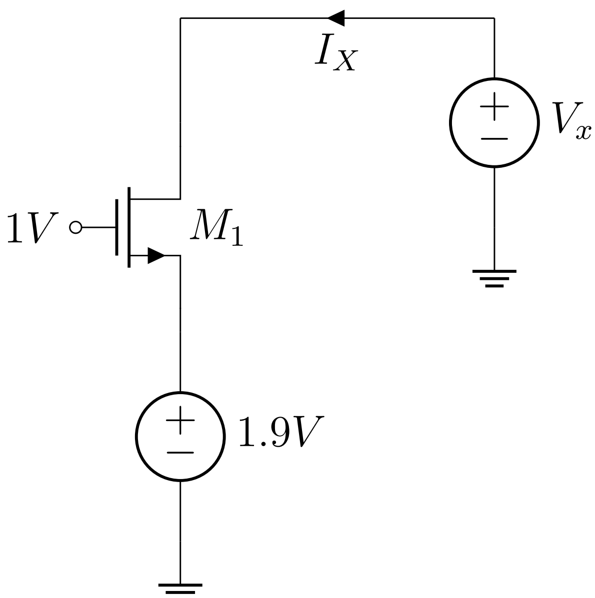

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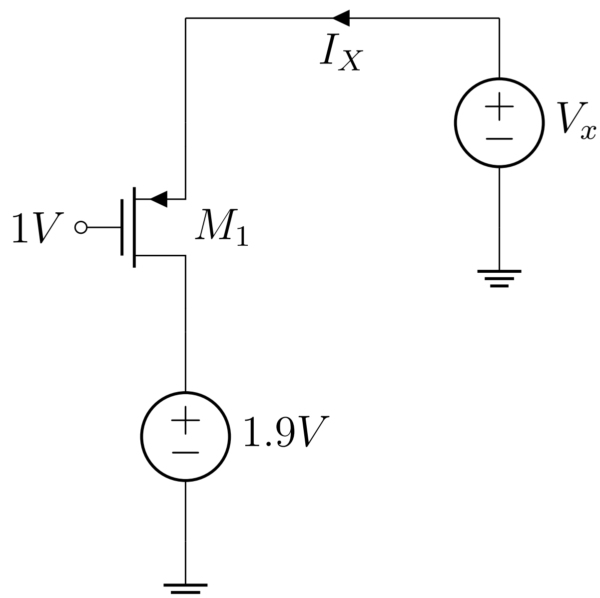


(D)

Q1:

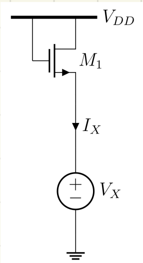
Already know: $\mu_n = 350\times10^{-4}\ m^2/V/s$, $\mu_p = 350\times10^{-4}\ m^2/V/s$, $V_{TH} = 0.7V$ (NMOS)

$V_{TH} = -0.8V$ (PMOS) , $\frac{W_{drawn}}{L_{drawn}} = \frac{20\mu m}{2\mu m}$, $t_{ox} = 9\times10^{-9}m$, $L_D = 0.08\mu m$, $V_{DD} = 5V$

$\Rightarrow L_{eff} = L_{drawn} - 2L_D = 2-2\times0.08 = 1.84\ \mu m \Rightarrow \frac{W}{L_{eff}} = \frac{20}{1.84} = \frac{250}{23}$

$\varepsilon_{ox} = 3.9\,\varepsilon_0 = 3.45\times10^{-11}\ F/m \Rightarrow C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 3.83\times10^{-3}\ F/m^2$

(A)



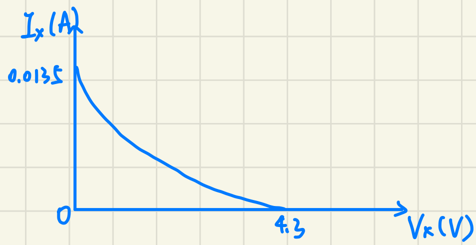
From the graph, we know it's a NMOS. $\Rightarrow V_{TH} = 0.7V$, $V_{DS} = \overset{5-x}{\overset{\parallel}{V_{DD} - V_x}} = V_{GS}$

$\Rightarrow V_{DS} \geq V_{GS} - V_{TH} = V_{DS} - 0.7 \Rightarrow$ it's in saturation region

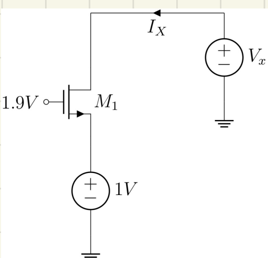
$V_{GS} \leq V_{TH} \Leftrightarrow 5 - V_x \leq 0.7 \Leftrightarrow V_x \geq 4.3V \Rightarrow$ it's in cut off region $I_x = 0A$

$V_x \leq 4.3V$: $= \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2 = \frac{1}{2}\cdot350\times10^{-4}\cdot3.83\times10^{-3}\cdot\frac{250}{23}(4.3-V_x)^2$

$\Rightarrow I_x = 7.285\times10^{-4}\times(V_x-4.3)^2$



(B)



From the graph, we know it's a NMOS. $\Rightarrow V_{TH} = 0.7V$

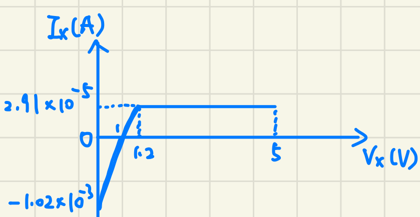
$V_{GS} = 0.9V > V_{TH}$, $V_{DS} = V_x - 1 \Rightarrow V_{GS} - V_{TH} = 0.2V$

① $V_{DS} < 0.2V \Leftrightarrow V_x < 1.2V \Rightarrow$ Triode Region

$I_D = \mu_n C_{ox}\frac{W}{L_{eff}}[(V_{GS}-V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2] = -7.285\times10^{-4}\cdot[(V_x-1.2)^2 - \frac{1}{25}]$

② $V_{DS} \geq 0.2V \Leftrightarrow V_x \geq 1.2V \Rightarrow$ saturation Region

$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}-V_{TH})^2 = 2.91\times10^{-5}A$



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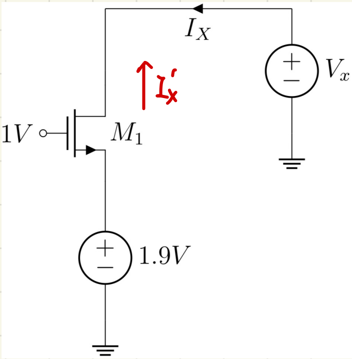


From the graph, we know it's a NMOS. $\Rightarrow V_{TH} = 0.7V$

$V_{GS} = -0.9V < V_{TH}$. $V_{DS} = V_x - 1.9$

$V_x > 1.9V \Rightarrow$ cut off region $I_x = 0\,A$

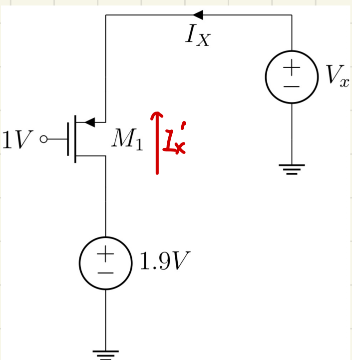
$V_x < 1.9V \Rightarrow$ change drain & source terminal

$\Rightarrow V_{GS}' = 1 - V_x$ $\quad V_x \geq 0.3V \Rightarrow V_{GS}' \leq V_{TH}$. cutoff region

$V_x < 0.3V \Rightarrow V_{DS} = 1.9 - V_x > V_{GS}' - V_{TH} = 0.3 - V_x \Rightarrow$ saturation

$I_x' = \frac{1}{2}\mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS}' - V_{TH})^2 \Rightarrow I_x = -7.285\times10^{-4}\cdot(V_x - 0.3)^2$

(D)



From the graph, we know it's a NMOS. $\Rightarrow V_{TH} = -0.8\,V$

$V_{GS} = 1 - V_x$, $V_{DS} = 1.9 - V_x$

① $V_x \leq 1.9\,V \Rightarrow$ change drain & source

$V_{GS} = -0.9V$, $V_{DS} = V_x - 1.9$

i) $V_{GS} - V_{TH} \leq V_{DS}$ triode region

$\Rightarrow -0.9 + 0.8 \leq V_x - 1.9 \Rightarrow V_x \geq 1.8V$

$I_x' = \mu_p C_{ox}\frac{W}{L_{eff}}[(V_{SG} - |V_{TH}|)V_{SD} - \frac{1}{2}V_{SD}^2]$

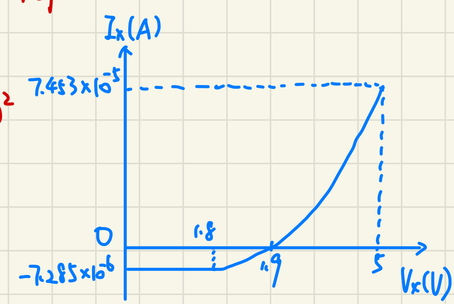
$= -7.285\times10^{-4}(V_x - 1.7)(V_x - 1.9)$

ii) $V_{GS} - V_{TH} > V_{DS}$ saturation region

$\Rightarrow V_x < 1.8V$

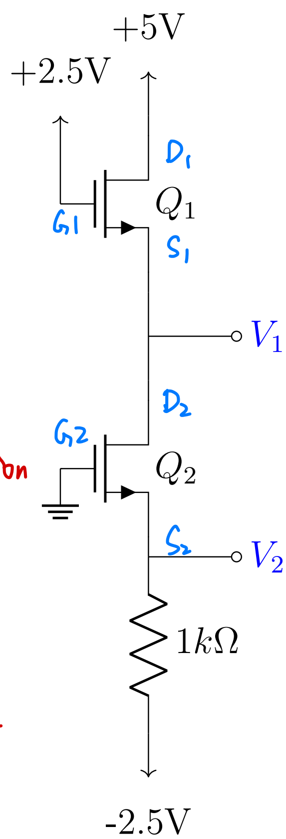
$I_x' = \frac{1}{2}\mu_p C_{ox}\frac{W}{L_{eff}}(V_{SG} - |V_{TH}|)^2$

$= 7.285\times10^{-6}\,A$



Question 2. Combination of MOSFET

For the circuit below, find the labeled node voltages. The NMOS transistor has $V_{TH} = 0.9V$, $k_n = \mu_n C_{ox}(W/L) = 1.5mA/V^2$.



$V_{GS1} = 2.5 - V_1$, $V_{DS1} = 5 - V_1$

$\Rightarrow V_{GS1} - V_{TH} = 1.6 - V_1 < V_{DS1}$

$\Rightarrow$ M_1 in saturation ($V_1 \leq 1.6V$)

$V_{GS2} = -V_2$, $V_{DS2} = V_1 - V_2$

$\Rightarrow V_{GS2} - V_{TH} = -V_2 - 0.9$

Assume M_2 also in saturation region

$V_{GS2} \geq 0.9V \Rightarrow V_2 \leq -0.9V$

$\Rightarrow I_1 = I_2 \Leftrightarrow \frac{1}{2}\mu_N C_{ox}\frac{W}{L_{eff}}(V_{GS1} - V_{TH})^2$

$= \frac{1}{2}\mu_N C_{ox}\frac{W}{L_{eff}}(V_{GS2} - V_{TH})^2$

$\Rightarrow |V_{GS1} - 0.9| = |V_{GS2} - 0.9|$

$\Leftrightarrow |1.6 - V_1| = |V_2 + 0.9| \Rightarrow V_1 - V_2 = 2.5V$

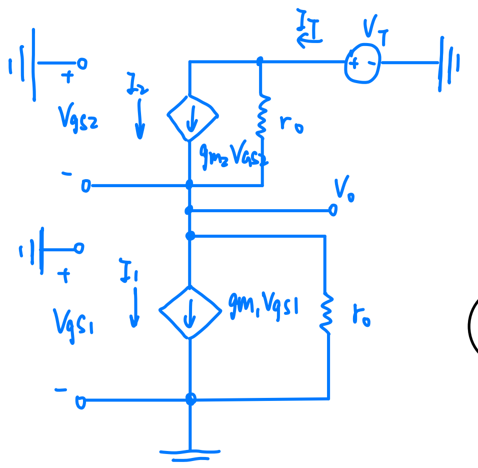
Meanwhile . $V_2 = -2.5 + 10^3 I_2 \Rightarrow I_2 = \frac{1}{2}\mu_N C_{ox}\frac{W}{L_{eff}}(-V_2 - V_{TH})^2 = \frac{1}{2} \times 1.5 \times 10^{-3}(2.5 - 10^3 I_2 - 0.9)^2$

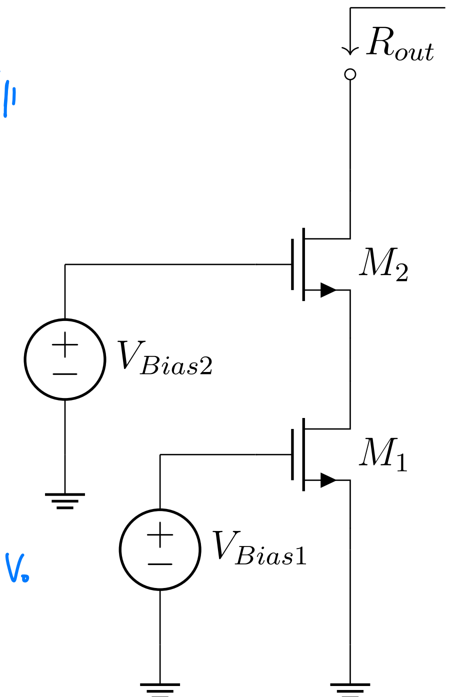
$\Rightarrow I_2 = 6.857 \times 10^{-4}$ A

$\Rightarrow \begin{cases} V_1 = 0.66\ V \\ V_2 = -1.84\ V \end{cases}$ ($\Rightarrow V_{GS2} - V_{TH} = 0.94V < V_{DS2} = 2.5V \Rightarrow$ assumption is correct)

Question 3. Small Signal of of MOSFET

The circuit shown below is a MOSFET cascode amplifier. Draw the small signal model and derive R_{out} for the amplifier. Assume transistors M_1 and M_2 are in saturation and include r_O in your calculation.





$$I_2 = g_{m2}V_{gs2} = g_{m2}(0 - V_o) = -g_{m2}V_o$$

$$I_1 = g_{m1}V_{gs1} = g_{m1} \cdot 0 = 0$$

$$\frac{V_T - V_o}{r_o} + I_2 = \frac{V_o}{r_o}$$

$$\Rightarrow V_o = \frac{V_T}{r_o} \cdot \frac{1}{\frac{2}{r_o} + g_{m2}}$$

$$\Rightarrow I_T = \frac{V_o}{r_o} = \frac{V_T}{r_o} \cdot \frac{1}{2 + g_{m2}r_o} \quad \Rightarrow R_{out} = \frac{V_T}{I_T} = r_o(2 + g_{m2}r_o)$$

Question 4. Common-Source with Resistive Load

Assume $\lambda = 0$ and $\gamma = 0$. For $V_{DD} = 5V$, $V_{in} = 0.9$ V + small signal, $R_D = 15k\Omega$ and $L_{drawn} = 2\mu m$, find out the value W_{drawn} to obtain a voltage gain $|A_v| > 10$ and V_{OUT} (the DC biasing voltage at the output) close to 2.5 V as much as possible.

$|A_v| = g_m R_D = k_n' \frac{W}{L_{eff}} (V_{GS} - V_{TH}) R_D > 10$

$\Rightarrow k_n' \frac{W}{L_{eff}} > \frac{1}{300}$

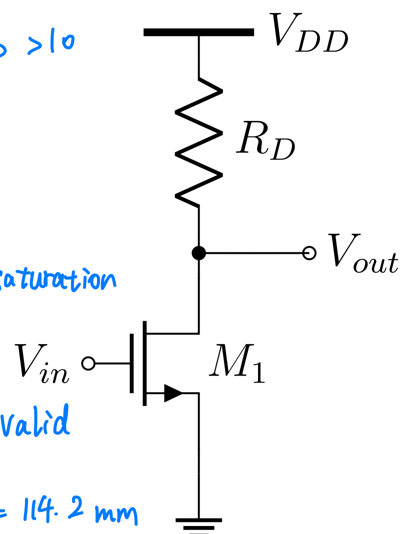
$V_{out} \approx 2.5V \Rightarrow I_D = \frac{V_{DD} - V_{out}}{R_D} = \frac{1}{6000} A$

$\Rightarrow V_{DS} = 2.5V > V_{GS} - V_{TH} = 0.2V \Rightarrow$ saturation

$\Rightarrow I_D = \frac{1}{2} k_n' \frac{W}{L_{eff}} (V_{GS} - V_{TH})^2 = \frac{1}{6000} A$

$\Rightarrow k_n' \frac{W}{L_{eff}} = \frac{1}{6000} \times 2 \times \frac{1}{0.2^2} > \frac{1}{300}$ valid

$\Rightarrow W = \frac{1}{120} \cdot \frac{L_{eff}}{k_n'} = \frac{1}{120} \cdot \frac{L_{drawn} - 2L_D}{\mu_n C_{ox}} = 114.2$ mm



NMOS Model			
LEVEL=1	VTO=0.7	GAMMA=0.45	PHI=0.9
NSUB=9e+14	LD=0.08e-6	UO=350	LAMBDA=0.1
TOX=9e-9	PB=0.9	CJ=0.56e-3	CJSW=0.35e-11
MJ=0.45	MJSW=0.2	CGDO=0.4e-9	JS=1.0e-8
PMOS Model			
LEVEL=1	VTO=-0.8	GAMMA=0.4	PHI=0.8
NSUB=5e+14	LD=0.09e-6	UO=100	LAMBDA=0.2
TOX=9e-9	PB=0.9	CJ=0.94e-3	CJSW=0.32e-11
MJ=0.5	MJSW=0.3	CGDO=0.3e-9	JS=0.5e-8

VTO : threshold voltage with zero V_{SB} (unit : V)
GAMMA : body effect coefficient (unit : $V^{1/2}$)
PHI : $2\Phi_F$ (unit : V)
TOX : gate oxide thickness (unit : m)
NSUB : substrate doping (unit : cm^{-3})
LD : source/drain side diffusion (unit : m)
UO : channel mobility (unit : $cm^2/V/s$)
LAMBDA : channel-length modulation coefficient (unit : V^{-1})
CJ : source/drain bottom-plate junction capacitance per unit area (unit : F/m^2)
CJSW : source/drain sidewall junction capacitance per unit length (unit : F/m)
PB : source / drain junction built-in potential (unit : V)

MJ : exponent in CJ equation (unitless)
MJSW : exponent in CJSW equation (unitless)
CGDO: gate-drain overlap capacitance per unit width (unit : F/m)
CGSO : gate-source overlap capacitance per unit width (unit : F/m)
JS : source/drain leakage current per unit area (unit A/m^2)
Vacuum permittivity (ϵ_o) = 8.85×10^{-12}(F/m)
Silicon oxide dielectric constant (ϵ_r) = 3.9