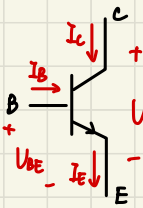
BJT

U_{BE}	发射极与基极电压
I_B	基极电流
I_C	集电极电流
U_{CE}	管压降



① 放大电路概述

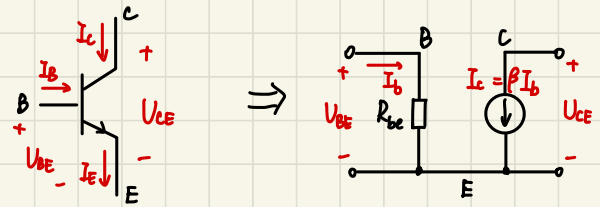
* 静态分析：直流通路（电容当断路）求静态工作点 Q：U_{BE}、I_B、I_C、U_{CE}

其中：硅管 $|U_{BE}| = 0.7V$，锗管 $|U_{BE}| = 0.3V$

* 动态分析：交流通路（电容短路，去掉直流独立电源）求动态性能指标：A_u、R_i、R_o
  + 微变等效电路模型

A_u	放大倍数	← $\frac{U_o}{U_i}$
R_i	输入电阻	← $\frac{U_i}{I_i}$
R_0	输出电阻	← 去源，R_L 开路，$= \frac{U_o}{I_o}$

② 微变等效电路模型



- BE 之间连一个等效电阻 R_{be}
- CE 之间连一个电流源 $I_C = \beta I_b$
- $R_{be} = R_{bb'} + (1+\beta)\frac{26(mV)}{I_E(mA)}$

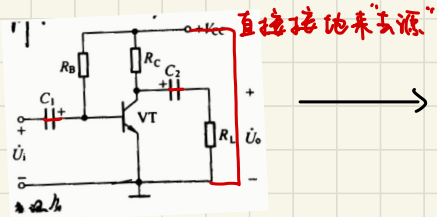
$R_{bb'}$：基区体电阻（题目会给 $R_{bb'}$）

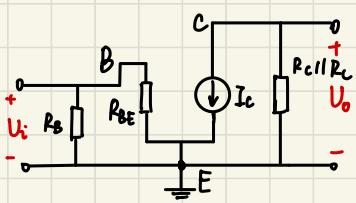
③ 当三极管在放大区时

$$\begin{cases} I_C = \beta I_b \\ I_e = (1+\beta) I_b \\ I_e = I_b + I_C \end{cases}$$

④ 画微变等效电路

电容看做短路，直流电源作"去源"处理，擦去三极管并用等效电路替换

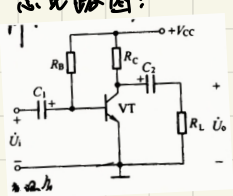




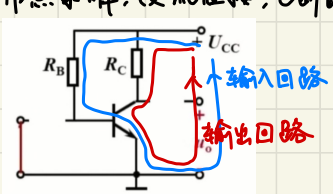
⑤ BJT 双极型三极管的共射放大电路

共射电路：基电极 B 输入，集电极 C 输出

总电路图：



静态工作点求解：（交流短接，C 断路）



step 1 求 I_B：$I_B R_B + U_{BE} - U_{CC} = 0$

step 2 求 I_C：$I_C = \beta I_B$

step 3 求 U_{CE}：$I_C R_C + U_{CE} - U_{CC} = 0$

$L_{eff} = L_{drawn} - 2L_D$

输入电压 v_{GS} 会由直流的 V_{GS} 和交流的 v_{gs} 组成（$v_{GS} = V_{GS} + v_{gs}$）

对于直流部分，我们可以用直流电路来求出 I_D = 先比 V_{DS} 是否 > $V_{GS} - V_{TH}$ 来判断是否饱和；再看是否需要考虑 channel-length modulation

（例子：公式均为 NMOS 管）

对于 I_D：① 不饱和（triode region）→ $V_{GS} - V_{TN} \geq V_{DS} > 0$

$$I_D = \underbrace{\mu_n C_{ox}}_{k_n'} \left(\frac{W}{L_{eff}}\right)\left[(V_{GS} - V_{TH})V_{DS} - \frac{1}{2}V_{DS}^2\right]$$

k_n

② 饱和并且考虑 channel-length modulation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}) \text{ 或 } I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff} - \Delta L}\right)(V_{GS} - V_{TH})^2$$

③ 饱和但不考虑 channel-length modulation

$$I_D = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{TH})^2$$

Body effect：

$$\gamma = \frac{\sqrt{2q\varepsilon_{Si}N_{sub}}}{C_{ox}}$$

不考虑时 $V_{TH} = V_{TH0}$

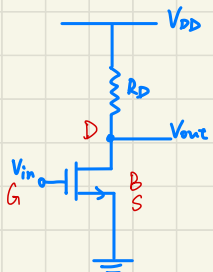
考虑时 $V_{TH} = V_{TH0} + \gamma\left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}\right)$

求完 I_D 之后才能进 small signal 分析：

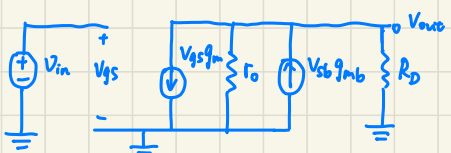
$$g_m = \begin{cases} \dfrac{2I_D}{V_{GS} - V_{TH}} = \sqrt{2\mu_n C_{ox}\dfrac{W}{L_{eff} - \Delta L}I_D} = \mu_n C_{ox}\dfrac{W}{L_{eff} - \Delta L}(V_{GS} - V_{TH}) & \text{不考虑 channel} \\ \sqrt{2\mu_n C_{ox}\left(\dfrac{W}{L}\right)I_D(1 + \lambda V_{DS})} = \mu_n C_{ox}\dfrac{W}{L}(V_{GS} - V_{TH})(1 + \lambda V_{DS}) & \text{考虑 channel} \end{cases}$$

$$r_o = \begin{cases} 0 & \text{不考虑 channel} \\ \dfrac{1}{\frac{1}{2}\mu_n C_{ox}\dfrac{W}{L_{eff} - \Delta L}(V_{GS} - V_{TH})^2 \cdot \lambda} = \dfrac{1}{I_D \cdot \lambda} & \text{考虑 channel} \end{cases}$$

$$g_{mb} = \begin{cases} 0 & \text{不考虑 body effect} \\ g_m \cdot \dfrac{\gamma}{2\sqrt{2\phi_F + V_{SB}}} = \eta g_m & \text{考虑 body effect} \end{cases}$$



微变电路

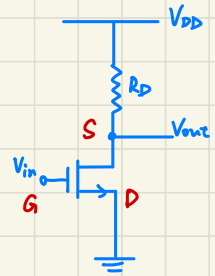


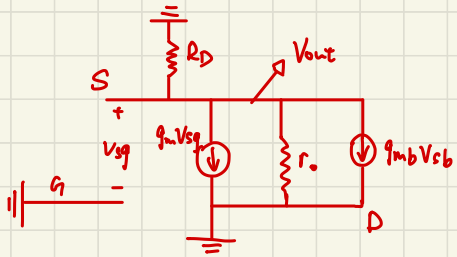
Gate：栅极

Source：源极

Drain：漏极

（ps：PMOS 管公式加绝对值就行）





PMOS Formula Table

NMOS Transistor Mathematical Model Summary
The following equations represent the complete model for the $i-v$ behavior of the NMOS transistor.
For all regions,

$$K_p = K_p'\frac{W}{L} \quad K_p' = \mu_p C_{ox}'' \quad i_G = 0 \quad i_B = 0 \tag{15}$$

Cut off region,

$$i_D = 0 \quad \text{for } V_{GS} \geq V_{TP} \tag{16}$$

Triode region,

$$i_D = K_p\left(v_{GS} - V_{TP} - \frac{v_{DS}}{2}\right)v_{DS} \quad \text{for } 0 \leq |v_{DS}| \leq |v_{GS} - V_{TP}| \tag{17}$$

PMOS Formula Table

Saturation region,

$$i_D = \frac{K_p}{2}(v_{GS} - V_{TP})^2(1 + \lambda|v_{DS}|) \quad \text{for } |v_{DS}| \geq |v_{GS} - V_{TP}| \geq 0 \tag{18}$$

Threshold voltage,

$$V_{TP} = V_{TO} + \gamma\left(\sqrt{v_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \tag{19}$$

For the enhancement-mode PMOS transistor, $V_{TP} < 0$. Depletion-mode PMOS devices can also be fabricated; $I_{TP} \geq 0$ for these devices.

Body effect（体效应），也称作substrate effect（底座效应），是指在MOSFET（金属氧化物半导体场效应晶体管）中，由于栅极和底座（substrate）之间的电压差异，导致晶体管特性发生变化的现象。

MOSFET是由P型或N型的底座（衬底）和两个与之电性相反的源极（Source）和漏极（Drain）组成。栅极（Gate）位于底座上，通过控制栅极电压可以控制源极和漏极之间的电流。在MOSFET中，底座与源极之间的电压差会影响晶体管的工作特性，这就是体效应。

具体来说，当在MOSFET的底座与源极之间施加反向偏置（对于N型MOSFET是正向偏置），底座的电势会影响通道区域的形成，从而影响源极和漏极之间的电流。这是因为底座与通道之间的电势差会改变通道中的载流子浓度。底座与源极电压之间的这种关系可以通过MOSFET的参数之一，称为阈值电压（Threshold Voltage），来表示。

在集成电路设计和应用中，需要考虑体效应，尤其是在高度集成的CMOS电路中。通过了解体效应的影响，工程师可以更好地优化MOSFET的特性，以确保电路的性能和可靠性。

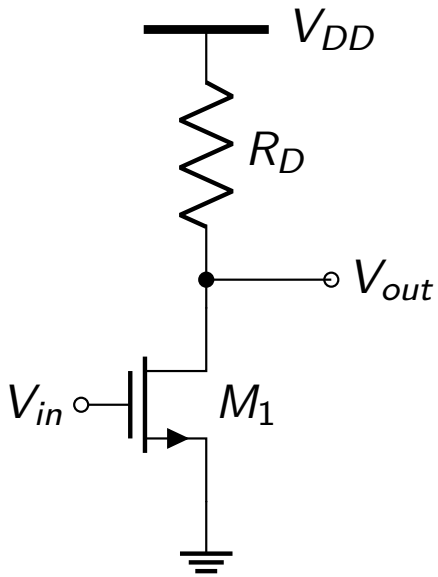
Channel-Length Modulation（沟道长度调制）是指在MOSFET（金属氧化物半导体场效应晶体管）中，当沟道长度发生变化时，晶体管的特性也会相应地改变的现象。

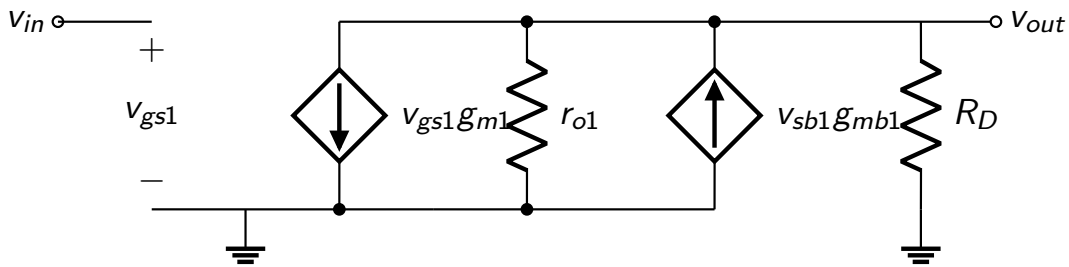
MOSFET的沟道长度指的是源极和漏极之间形成的通道区域的长度。当MOSFET处于饱和区（Saturation Region）时，沟道长度的变化会导致漏极电流（ID）发生调制，即漏极电流与漏极电压（VDS）之间的关系不再是简单的线性关系。

具体来说，当VDS增大时，沟道长度会因为底座与源极之间的电场而增加。由于沟道长度的增加，通道中的电荷载流子数量增多，从而导致漏极电流ID增加。这种现象就是沟道长度调制。

在高电压或高电流的工作条件下，沟道长度调制会成为一个显著影响MOSFET工作的因素。这可以导致MOSFET的输出电流不再是一个固定的值，而是与VDS有关。为了准确建模和设计MOSFET电路，工程师需要考虑沟道长度调制效应，特别是在高性能和高精度的电路应用中。

CS with Resistive Load





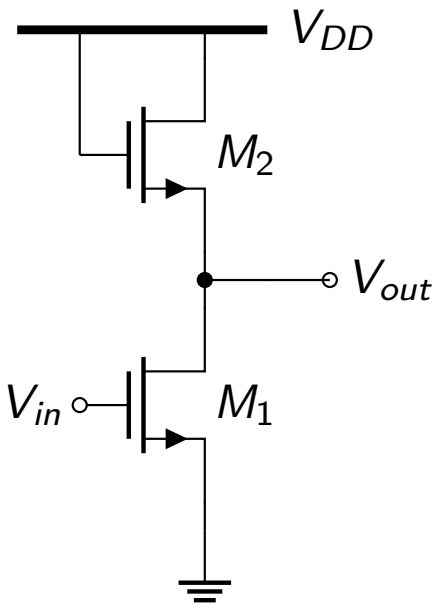
If no channel-length and body effect:

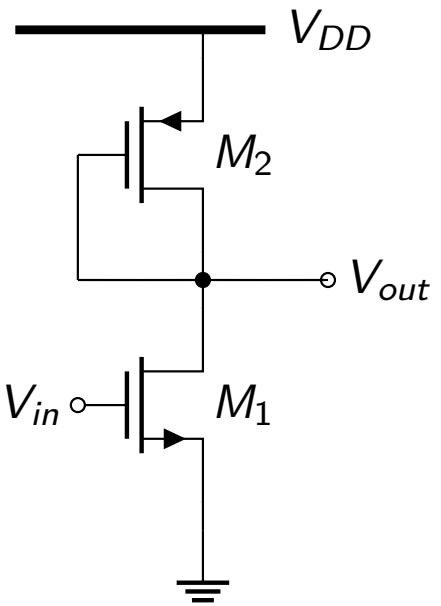
$$A_v = \frac{v_{out}}{v_{in}} = -g_{m1}R_D \tag{1}$$

No body effect:

$$A_v = -g_{m1}(R_D \parallel r_{o1}) \tag{2}$$

CS with Diode-connected Load





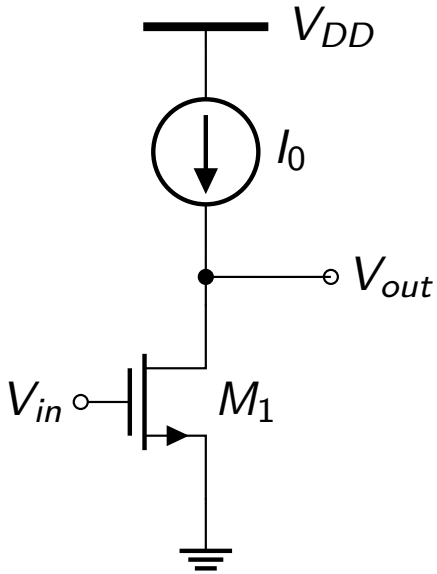
NMOS:

$$A_{\mathrm{v}} = -\sqrt{\frac{(W/L)_1}{(W/L)_2}}\frac{1}{1+\eta} \qquad \eta = g_{\mathrm{mb2}}/g_{\mathrm{m2}} \tag{3}$$

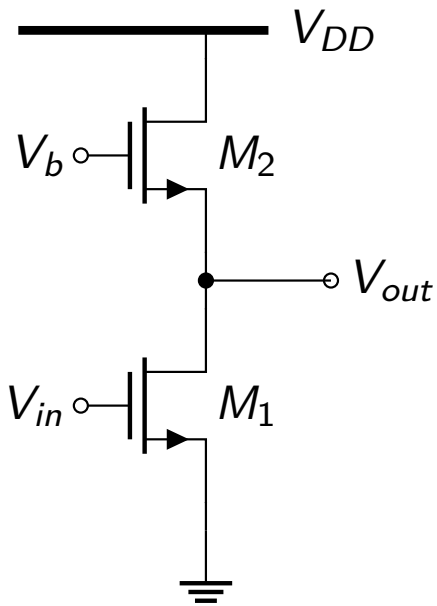
PMOS:

$$A_{\mathrm{v}} = -\sqrt{\frac{\mu_{\mathrm{n}}(W/L)_1}{\mu_{\mathrm{p}}(W/L)_2}} \tag{4}$$

CS with Current Source Load

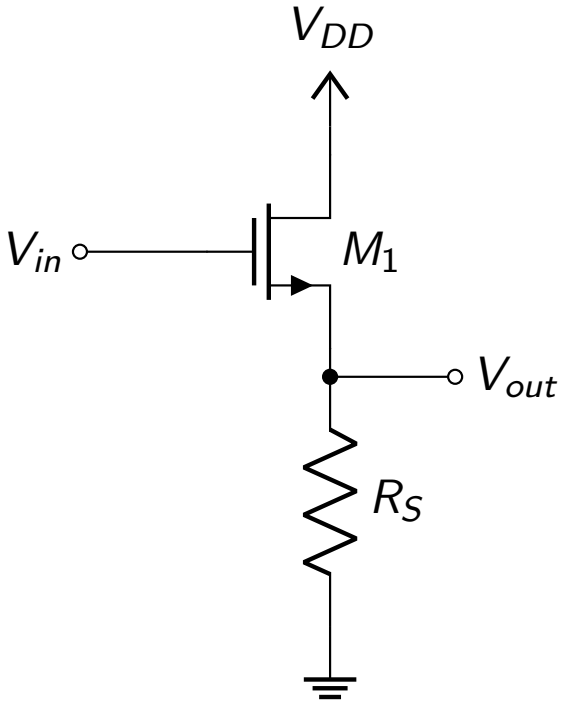


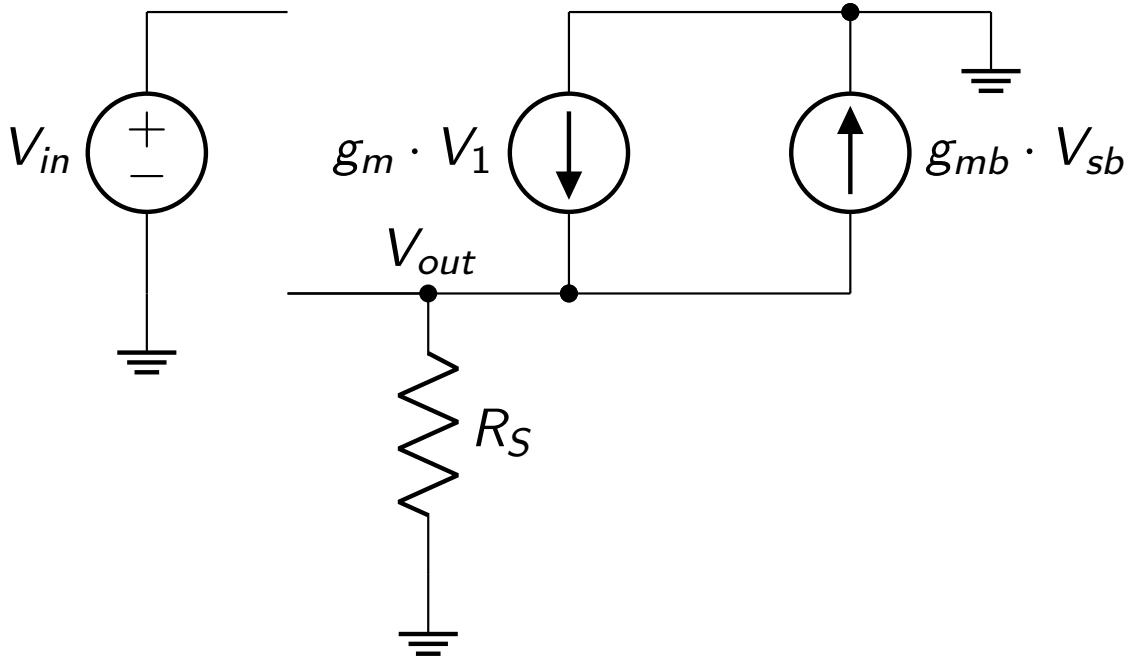
or



$$A_v = -g_{m1}(r_{o2} \parallel r_{o1}) \tag{5}$$

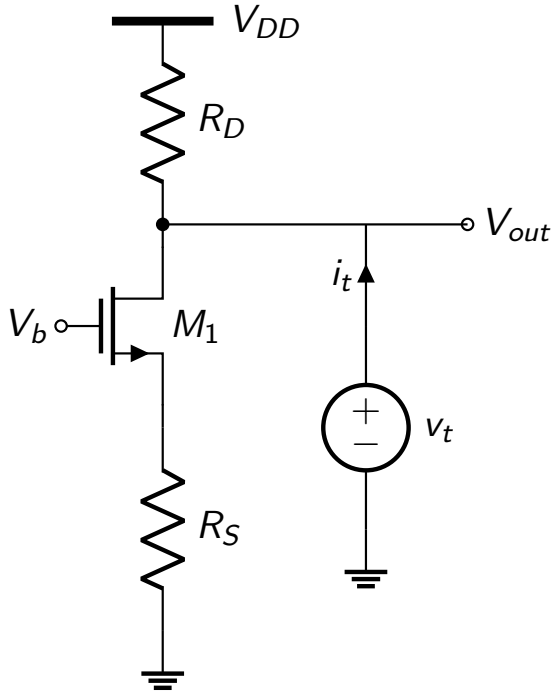
Source Follower

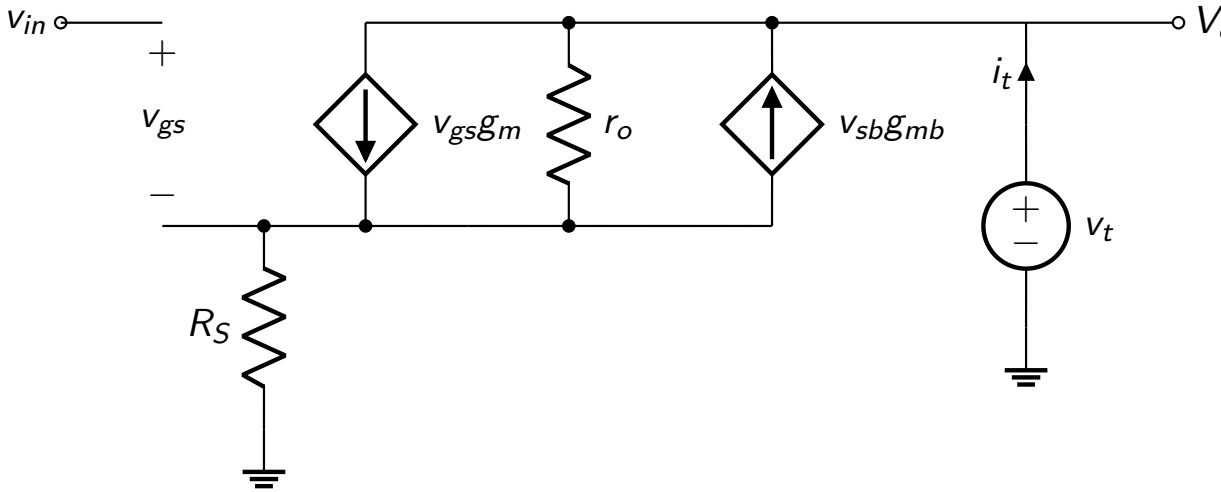




$$A_v = \frac{g_m R_S}{1 + g_m R_S(1+\eta)} = \frac{g_m R_S}{1 + (g_m + g_{mb})R_S} \approx \frac{1}{1+\eta} \qquad (6)$$

Common Gate

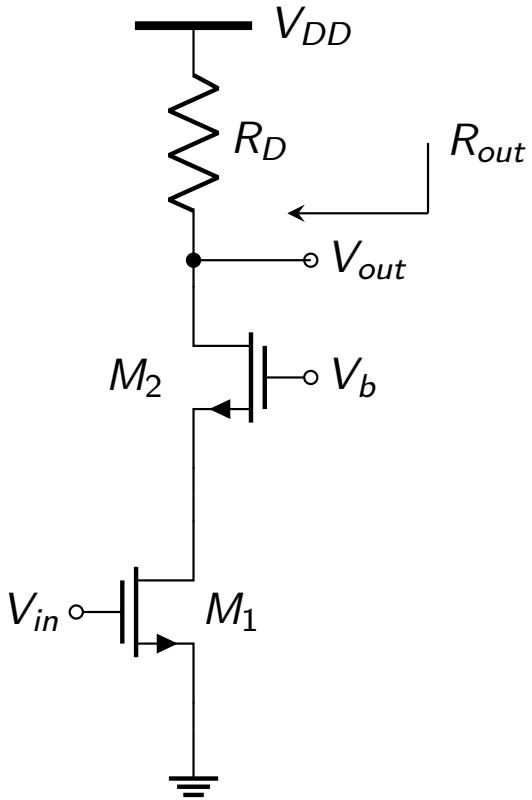




$$R_{in} = \frac{R_D + r_o}{1 + (g_m + g_{mb})r_o} \begin{cases} \text{If } R_D = 0 & R_{in} = r_o \parallel \frac{1}{g_m} \parallel \frac{1}{g_{mb}} \\ \text{If } R_D = \infty & R_{in} = \infty \end{cases} \quad (7)$$

$$R_{out} = [R_S + r_{o1} + (g_{m1} + g_{mb1})r_{o1}R_S] \parallel R_D \quad (8)$$

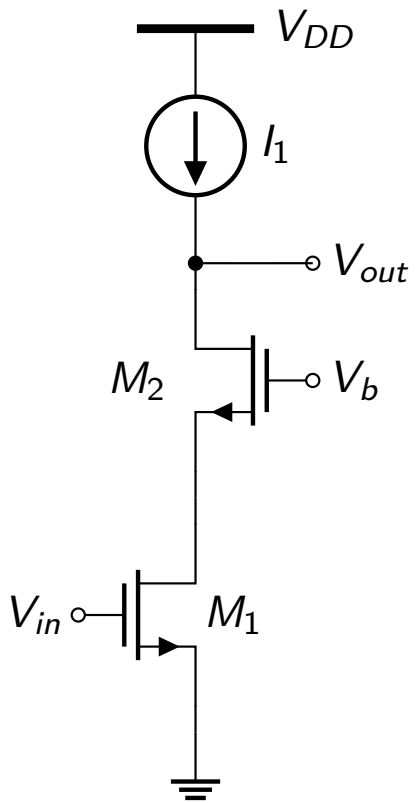
Cascode



$$G_m = -g_{m1} \frac{r_{o1}}{r_{o1} + \left(r_{o2} \parallel \frac{1}{g_{m2}+g_{mb2}} \right)} \quad (9)$$

$$R_{out} = [r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o2} r_{o1}] \parallel R_D \quad (10)$$

Cascode

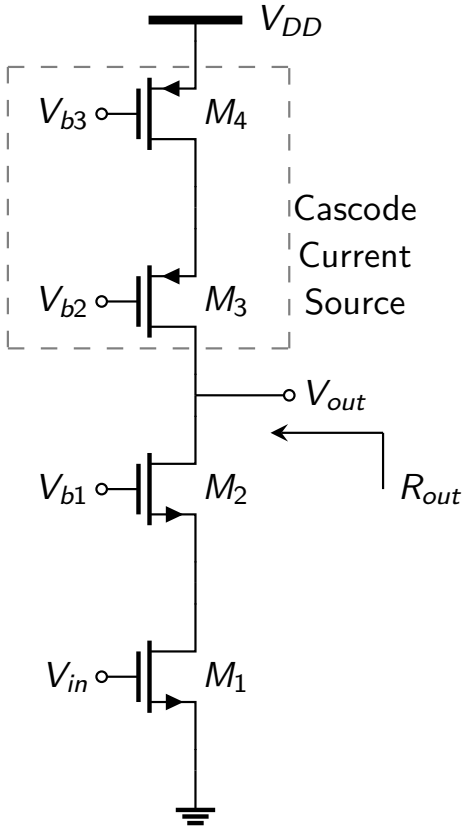


$$G_m = -g_{m1} \frac{r_{o1}}{r_{o1} + \left(r_{o2} \parallel \frac{1}{g_{m2}+g_{mb2}} \right)} \tag{11}$$

$$R_{out} = r_{o1} + r_{o2} + (g_{m2} + g_{mb2}) r_{o2} r_{o1} \tag{12}$$

$$A_v = G_m R_{out} \tag{13}$$

Cascode

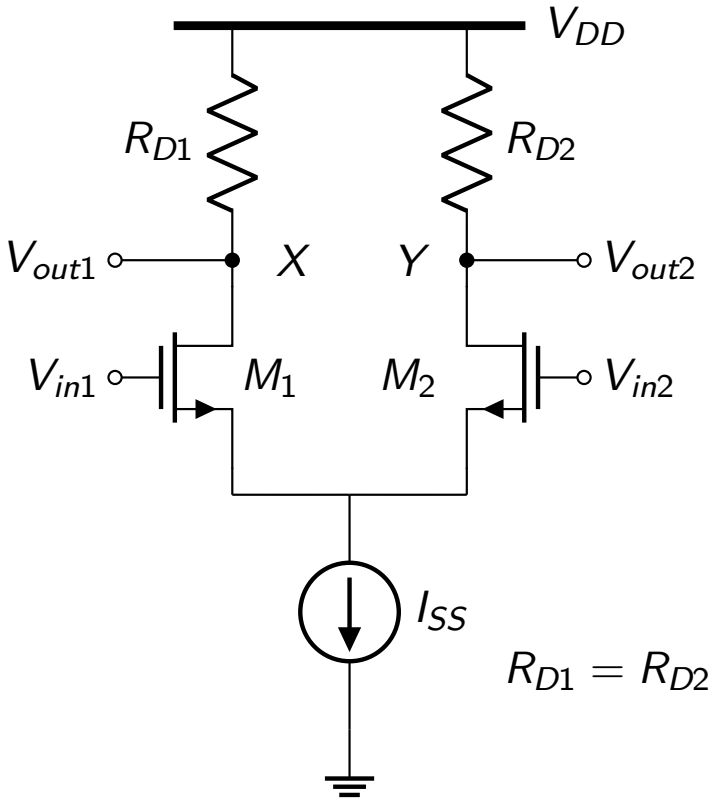


$$G_m = -g_{m1}\frac{r_{o1}}{r_{o1} + (r_{o2} \parallel \frac{1}{g_{m2}g_{mb2}})} \quad (14)$$

$$R_{out} = [r_{o1} + r_{o2} + (g_{m2} + g_{mb2})r_{o2}r_{o1}] \parallel [r_{o3} + r_{o4} + (g_{m3} + g_{mb3})r_{o3}r_{o4}] \quad (15)$$

$$A_v = G_m R_{out} \quad (16)$$

Differential Pair



$$R_{D1} = R_{D2} = R_D$$

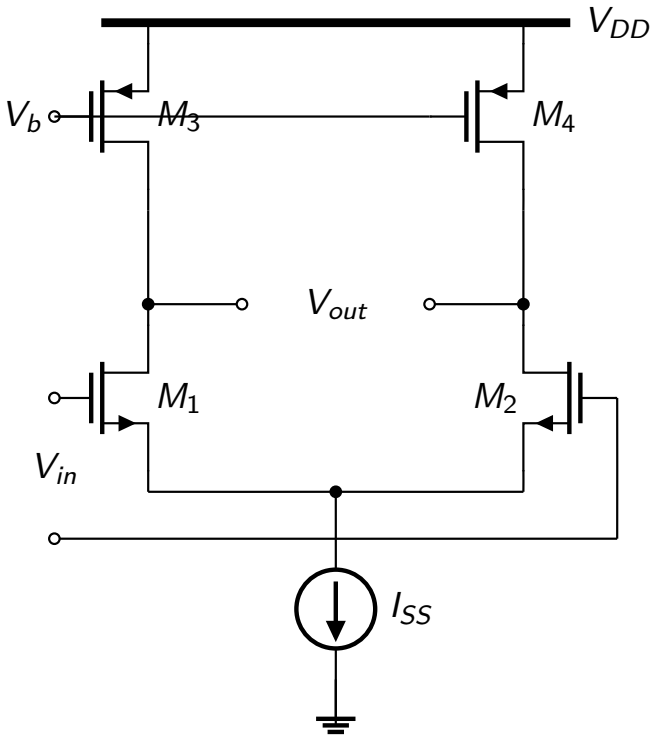
$$A_{DM} = \frac{V_{out1} - V_{out2}}{v_d} = -g_m(R_D \parallel r_o) \quad (17)$$

If the circuit is fully symmetric,

$$A_{CM-DM} = \frac{V_{out1} - V_{out2}}{v_{in,CM}} = 0 \quad (18)$$

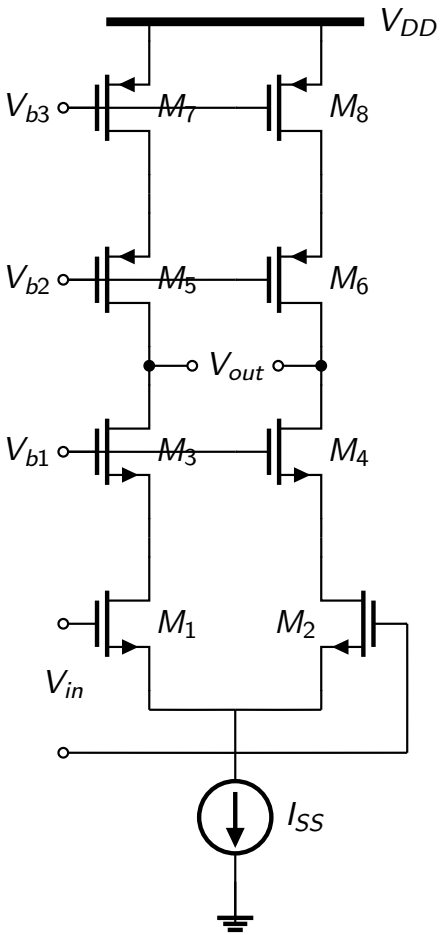
$$CMRR = \left| \frac{A_{DM}}{A_{CM-DM}} \right| = \infty \quad (19)$$

Differential Pair with MOS Loads



$$A_{DM} = -g_{m1,2}(r_{o1,2} \parallel r_{o3,4}) \qquad (20)$$

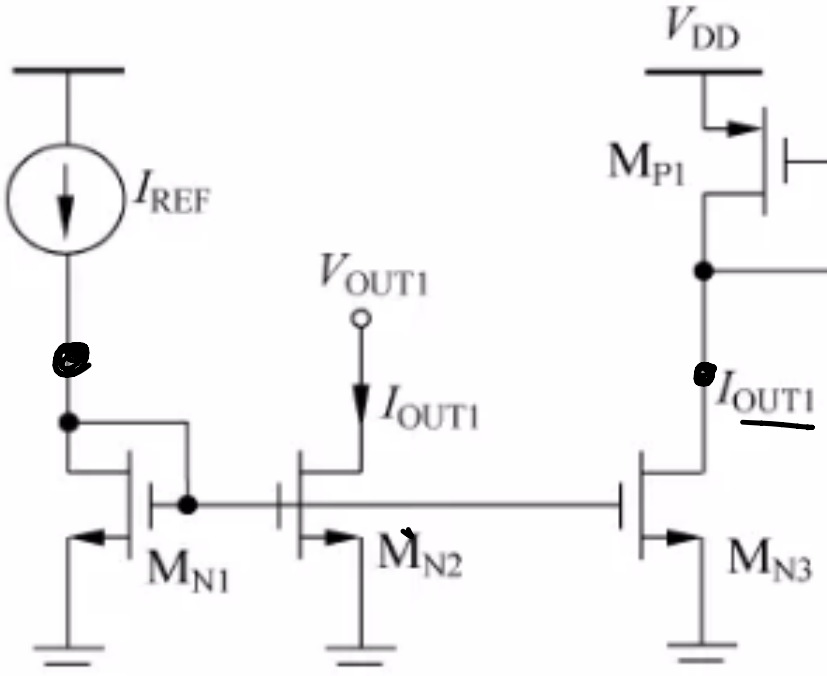
Differential Pair with Cascode Loads

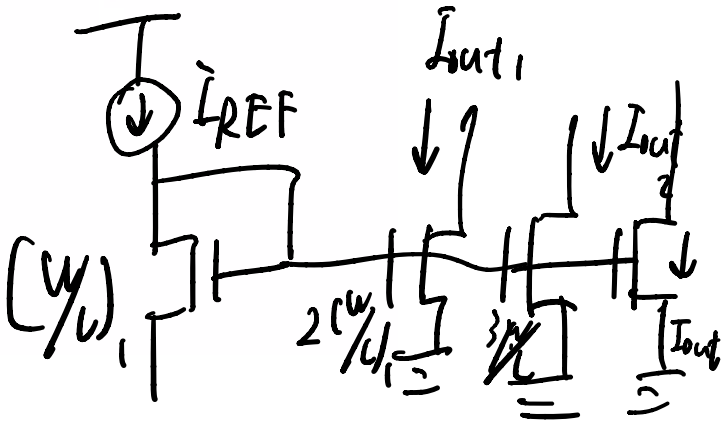


$$A_{DM} \cong -g_{m1,2}[(g_{m3,4} + gmb_{3,4})r_{o3,4}r_{o1,2} \parallel (g_{m5,6} + g_{mb5,6})r_{o5,6}r_{o7,8}] \tag{21}$$

Current Mirror

at most 4 MOSFET





$$I_{OUT1} = \frac{(W/L)_{N2}}{(W/L)_{N1}} I_{REF}$$

$$I_{OUT2} = \frac{(W/L)_{N3}}{(W/L)_{N1}} \frac{(W/L)_{P2}}{(W/L)_{P1}} I_{REF}$$

$I_{out1} = 2 I_{REF}$

$I_{out2} = 3 I_{REF}$