# VE311 Electronic Circuits

# Summer 2023 — Lab 4

## Instructor: Dr. Xuyang Lu

## Due: 11:59 pm, July 29, 2023 (Saturday)

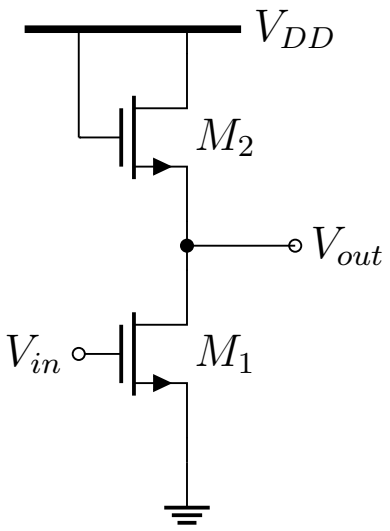
Note:

1. Please use A4 size papers.
2. The lab report should be submitted online individually.
3. Use Proteus 8.10 for simulation before the lab session. In the Proteus library, you should be able to find all the components used in the schematics. The lab report must include both the simulation and measurement results.

## Exercise 4.1

[Common-Source with NMOS Diode-Connected Load]

1. [20%] Design and build a common-source with diode-connected load amplifier using NMOS (VN0104). Plot $V_{OUT}$ vs $V_{IN}$. What is the voltage gain $A_v$ ? (Hint: Perform DC sweep of $V_{IN}$ from 0 V to 3 V. Choose a $V_{IN}$ at which both transistors are in the saturation region. The voltage gain is the slope of the DC sweep curve at the chosen $V_{IN}$.) Caution: the transistors could become very hot with high drain current. Don't touch with bare hands before they fully cool down.
2. [15%] Following (a), now put two common-source NMOS in parallel. Plot $V_{OUT}$ vs $V_{IN}$ again. At the $V_{IN}$ chosen in (a), does the voltage gain $A_v$ double? Briefly explain the reason. (Note: Make sure all NMOS remain in the saturation region.)
3. [15%] Following (b), for $V_{in} = V_{IN} + 0.01 \sin(2\pi 10^2 \cdot \text{time})$, plot $V_{out} = V_{OUT} + v_{out}$ vs time. Confirm that the amplitude of $v_{out}$ is close to $0.01 \times A_v$.



# Exercise 4.2

[Common-Source with PMOS Diode-Connected Load]

1. [20%] Design and build a common-source with diode-connected load amplifier using NMOS (VN0104) and PMOS (VP0104). Plot $V_{\mathrm{OUT}}$ vs $\mathrm{V_{IN}}$. What is the voltage gain $\mathrm{A_v}$ ? (Hint: Perform DC sweep of $V_{IN}$ from 0 V to 3 V. Choose a $V_{IN}$ at which both transistors are in the saturation region. The voltage gain is the slope of the DC sweep curve at the chosen $V_{IN}$.) Caution: the transistors could become very hot with high drain current. Don't touch with bare hands before they fully cool down.

2. [15%] Following (a), now put two PMOS diode-connected loads in parallel. Plot $V_{\mathrm{OUT}}$ vs $V_{\mathrm{IN}}$ again. At the $V_{\mathrm{IN}}$ chosen in (a), how does the voltage gain $\mathrm{A}_v$ change? Briefly explain the reason. (Note: Make sure all NMOS and PMOS remain in the saturation region.)

3. [15%] Following (b), for $V_{\mathrm{in}} = V_{IN} + 0.01 \sin(2\pi 10^2 \cdot \text{ time})$, plot $V_{\mathrm{out}} = V_{\mathrm{OUT}} + v_{\mathrm{out}}$ vs time. Confirm that the amplitude of $v_{\mathrm{out}}$ is close to $0.01 \times \mathrm{A}_v$.