UM–SJTU Joint Institute
Electronic Circuits Summer (ECE3110J)

Lab4 Report

Common-Source with NMOS and PMOS Diode-Connected Load

Instructed by

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1 Exercise 4.1.1

Since Proteus does not allow connecting the source directly to ground, I add a resistor of 1ω to the drain as shown in Figure 1. The obtained values thus may vary slightly from real theoretical values.

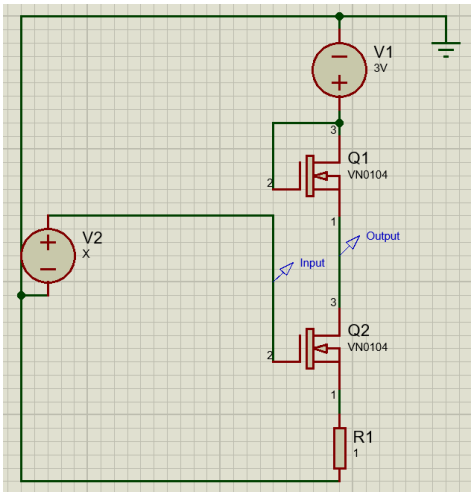

Figure 1: Circuit of 4.1.1

The resulting graph of V_{OUT}vs.V_{IN} is shown in Figure 2. From the curve, when V_{IN} = 0.99V, V_{OUT} = 2.01V and when V_{IN} = 1.01V, V_{OUT} = 1.98V. Thus, at V_{IN} = 1V, the slope is,

$$\left|\frac{2.01 - 1.98}{0.99 - 1.01}\right| = -1.5 \tag{1}$$

So when V_{IN} = 1V , A_V = -1.5. At this time, V_{OUT} ¿ V_{IN} - V_{TH} and 3 - V_{OUT} ¿ V_{TH} so the NMOSes are both on and in saturation region.

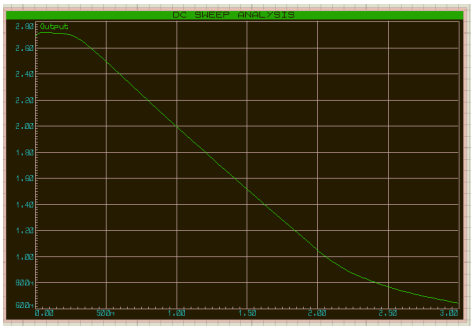

Figure 2: DC sweep of 4.1.1

2 Exercise 4.1.2

According to Figure 3, when V_{IN} = 0.99V , V_{OUT} = 1.97V and when V_{IN} = 1.01V , V_{OUT} = 1.94V . Thus, at V_{IN} = 1V , the slope is,

$$\left|\frac{1.97 - 1.94}{0.99 - 1.01}\right| = -1.5 \tag{2}$$

So when V_{IN} = 1V , A_V = -1.5. At this time, three NMOSes are in saturation region. Comparing the value of A_V with that in 4.1.1, we can conclude it does not double.

This is because in (a),

$$A_V = -gm_1(\frac{1}{gm_2}||r_{01}||r_{02}||\frac{1}{gmb_2}), \tag{3}$$

while in (b),

$$A_V = -(gm_1 + gm_3)(\frac{1}{gm_2}||r_{01}||r_{02}||r_{03||}\frac{1}{gmb_2}), \tag{4}$$

Hence, the relation between two A_V s is not double or half.

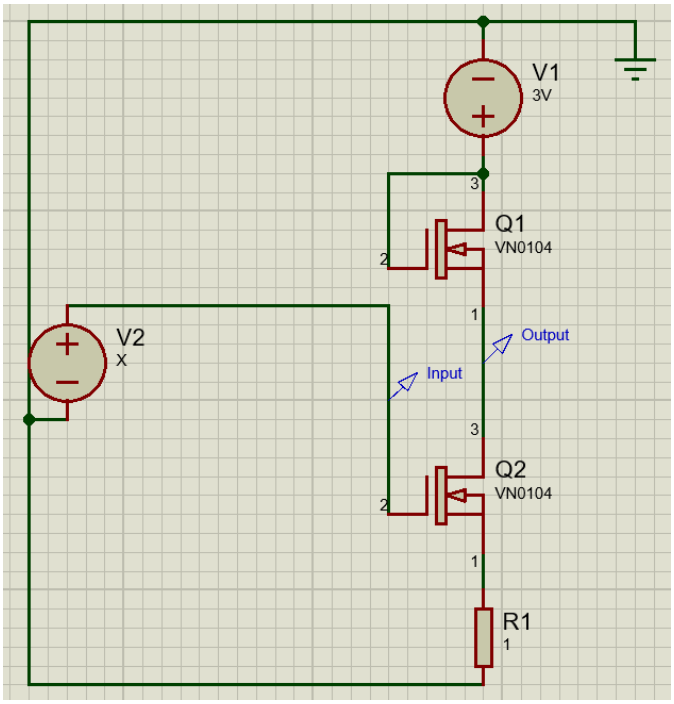

Figure 3: Circuit of 4.1.2

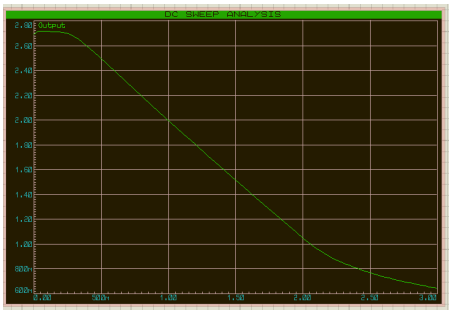

Figure 4: DC sweep of 4.1.2

3 Exercise 4.1.3

According to Figure 5, the amplitude of V_{OUT} is

$$\left|\frac{14m + 14m}{2}\right| = 0.014 \tag{5}$$

This value is quite close to $0.01|A_V| = 0.015$.

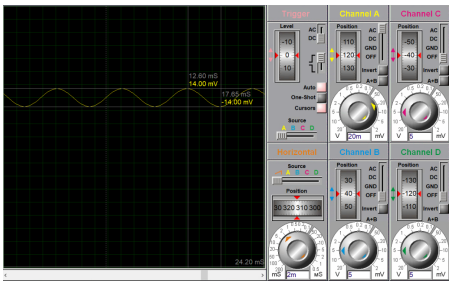

Figure 5: Simulation of 4.1.3

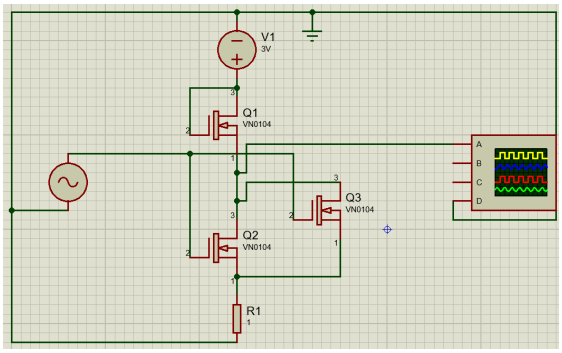

Figure 6: Circuit of 4.1.3

The experimental result is shown below:

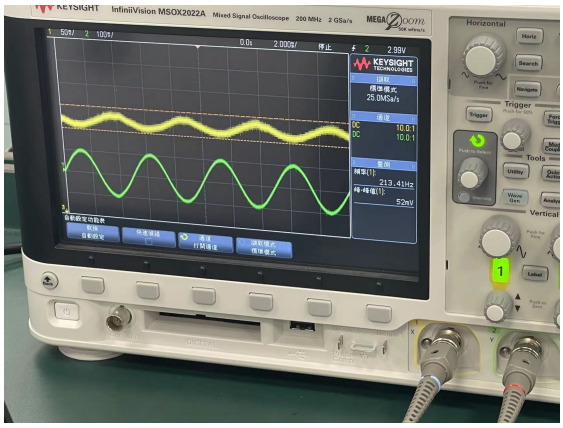

Figure 7: Lab result of 4.1.3

4 Exercise 4.2.1

In this part, I add a resistor of 10ω to the source of NMOS as shown in Figure 8.

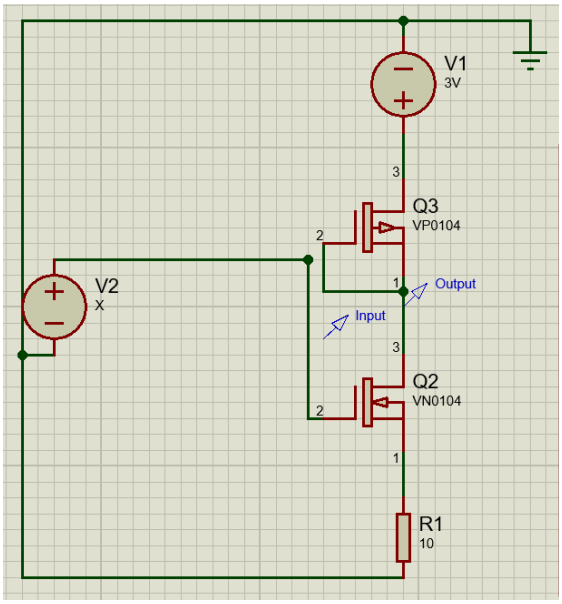

Figure 8: Circuit of 4.2.1

The resulting graph of V_{OUT}vs.V_{IN} is shown in Figure 9. From the curve, when V_{IN} = 0.79V , V_{OUT} = 2.51V and when V_{IN} = 0.81V , V_{OUT} = 2.49V . Thus, at V_{IN} = 0.8V , the slope is,

$$\frac{2.51 - 2.49}{0.79 - 0.81} = -1 \tag{6}$$

So when V_{IN} = 0.8V , A_V = -1. At this time, The NMOS and PMOS are both in saturation region.

5 Exercise 4.2.2

According to Figure 9, when V_{IN} = 0.79V , V_{OUT} = 2.53V and when V_{IN} = 0.81V , V_{OUT} = 2.51V . Thus, at V_{IN} = 0.8V , the slope,

Figure 9: Simulation of 4.2.2

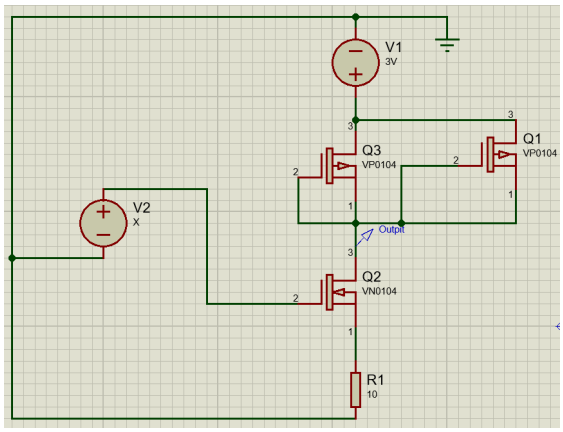

Figure 10: Circuit of 4.2.2

6 Exercise 4.2.3

According to Figure 11, the amplitude of V_{out} is

$$\frac{6.25m + 6.25m}{2} = 0.000625 \tag{7}$$

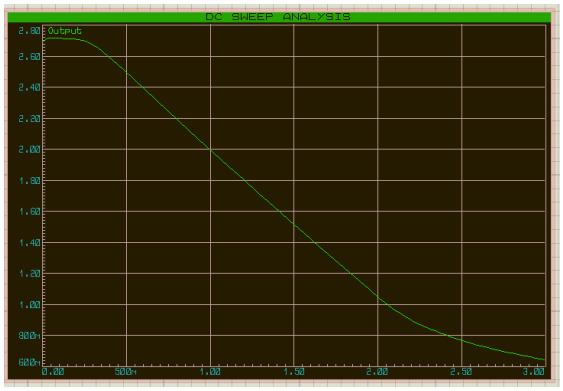

Figure 11: Simulation of 4.2.3

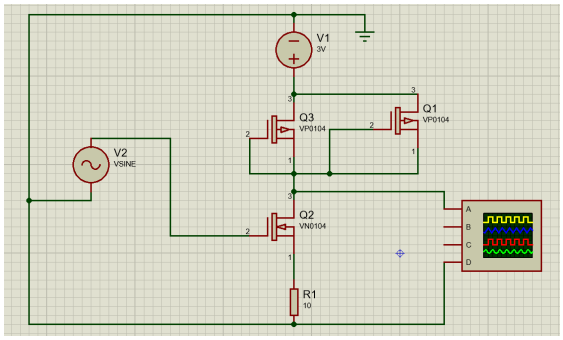

Figure 12: Circuit of 4.2.3

This value is somehow close to $0.01A_V = 0.001$. The reason why it's not quite close may be the source degeneration caused by the resistor.

The experimental result is shown below:

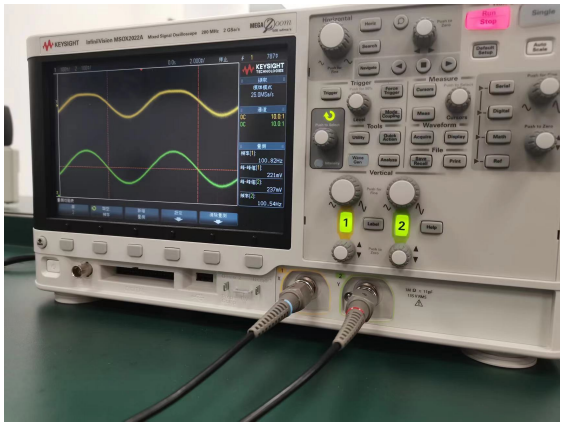

Figure 13: Lab result of 4.2.3