Lecture 6

VE 311 Analog Circuits

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2023 Summer

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Recap of Last Lecture

- Diode Circuits
- Op-amps

Topic to be covered

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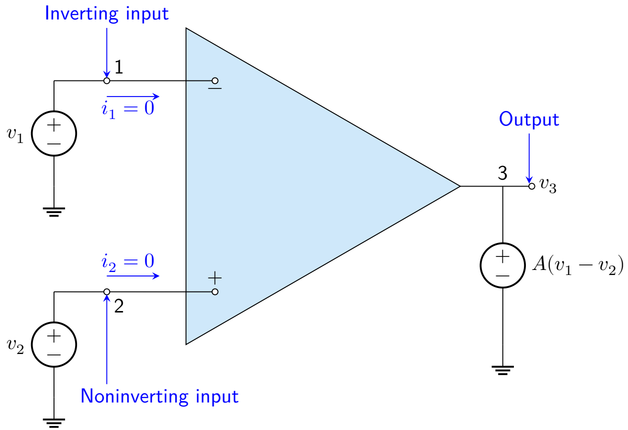
- Op-amps

Ideal Op-amps



Non-Ideal Op-amps

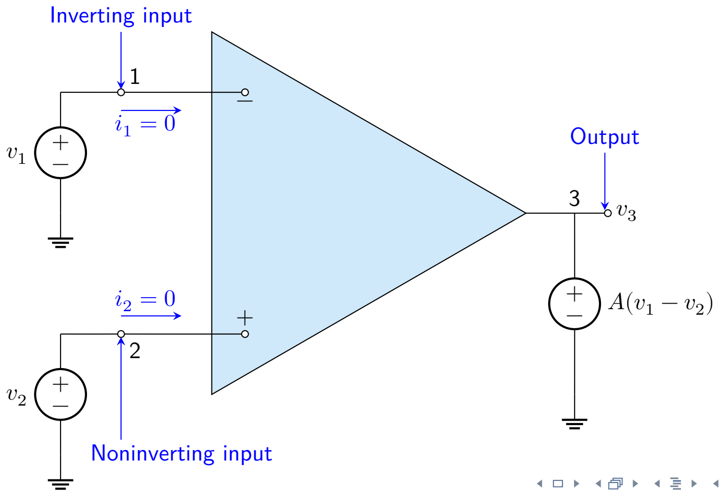
- Ideal op-amp approximation is usually very good and gives us values that are close to non-ideal behavior, in some cases.
- Ideal op-amp analysis is easier to perform and give us a good approximation.

Parameters of Interest

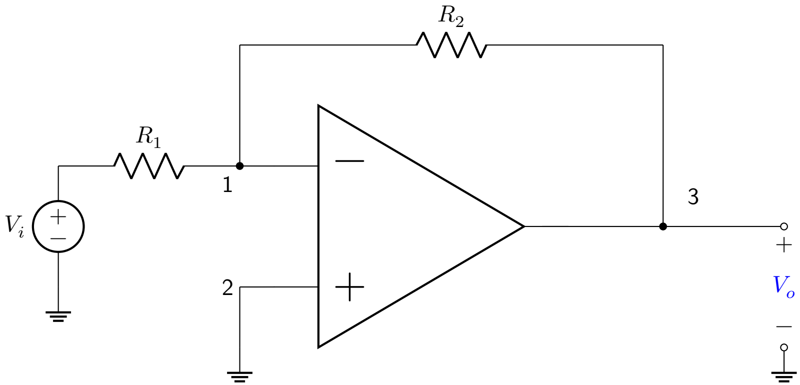
- Gain
- Rout
- Rin
- CMRR

- Offset voltage
- Clipping
- Bandwidth
- Slew Rate

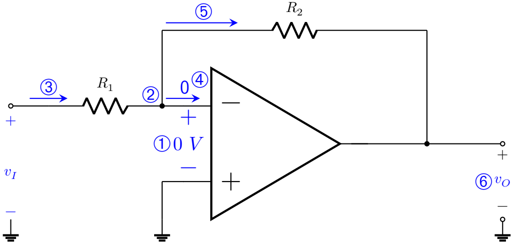
Finite Gain


Inverting input
1
$i_1 = 0$
v_1
Output
3
v_3
$A(v_1 - v_2)$
$i_2 = 0$
2
v_2
Noninverting input

Inverting Amplifier Gain



Virtual Ground



②: (Virtual ground)

$$v_+ = V_- = 0 \tag{1}$$

③:

$$i_1 = \frac{V_i}{R_1} \tag{2}$$

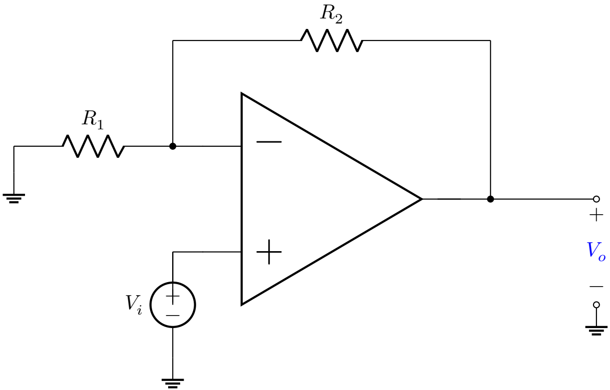
⑤:

$$i_2 = i_1 = \frac{V_i}{R_1} \tag{3}$$

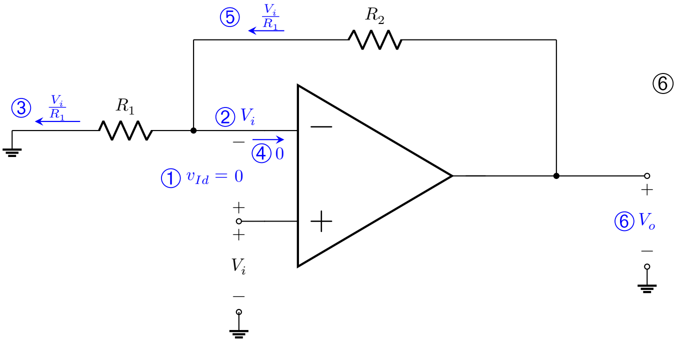
⑥:

$$V_o = 0 - \frac{V_i}{R_1} R_2 = -\frac{R_2}{R_1} V_i \tag{4}$$

Non-Inverting Amplifier



Non-Inverting Amplifier

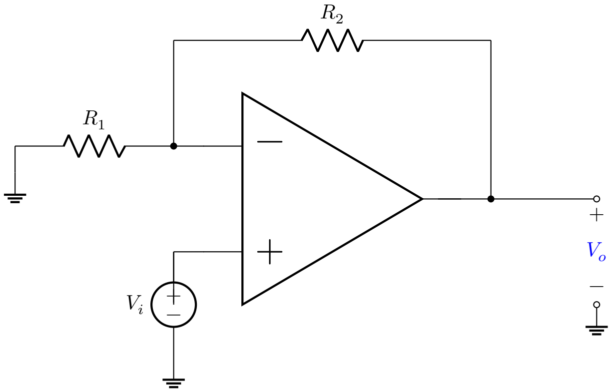


⑥:

$$V_o = V_i + \frac{V_i}{R_1} R_2 \tag{5}$$

$$= V_i \left(1 + \frac{R_2}{R_1}\right) \tag{6}$$

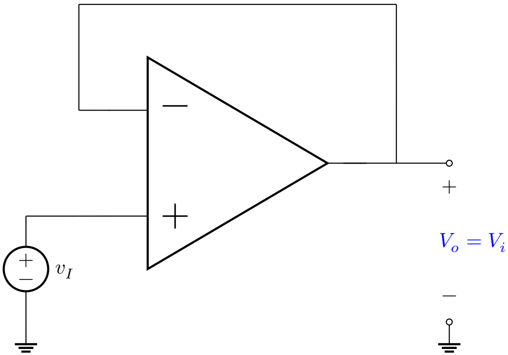
Feedback Factor



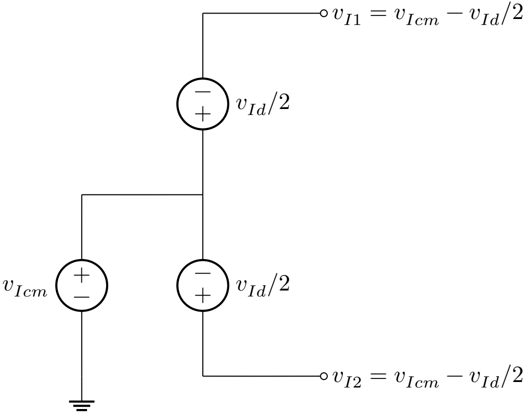
- fraction of V_o gets fed back to $V\_$ of Opamp terminal.

$$\frac{V_-}{V_o} = \frac{R_1}{R1 + R_2} = \beta \qquad (7)$$

Unity Gain Buffer (Voltage Follower)



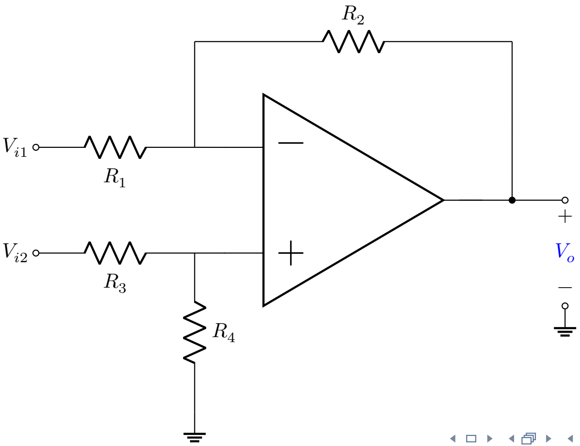
Common and Differential Signal



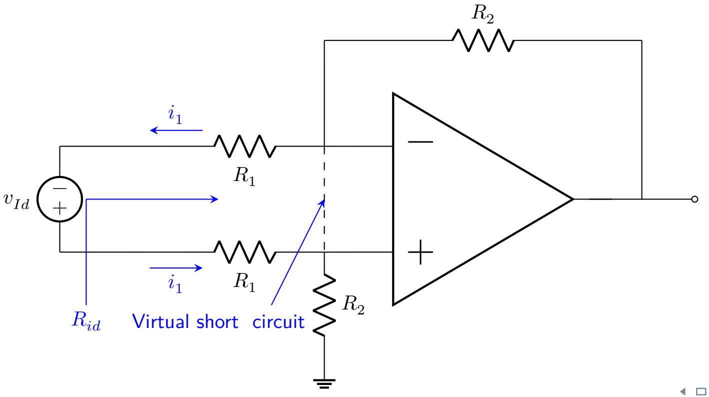
$$V_{id} = V_{i2} - V_{i1} \tag{8}$$

$$V_{icm} = \frac{1}{2}\left(V_{i1} + V_{i2}\right) \tag{9}$$

Difference Amplifier ($\frac{R_2}{R_1} = \frac{R_4}{R_3}$)



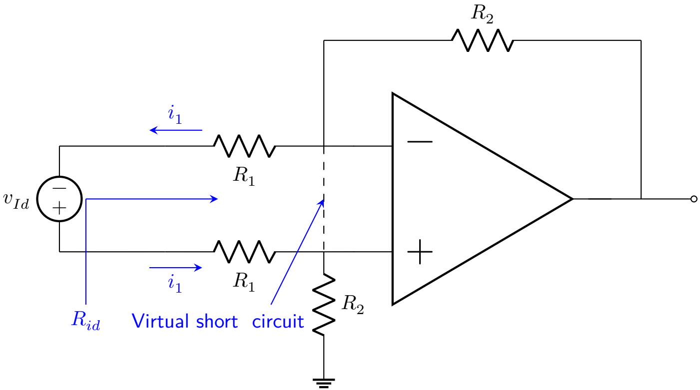
Input Impedance of a Difference Amplifier



Find the input impedance of op-amp, assume that

- $R_3 = R_1$
- $R_4 = R_2$

Input Impedance of a Difference Amplifier

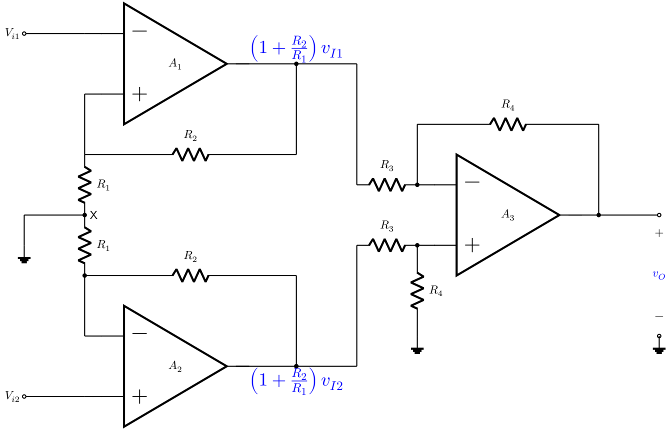


$$R_{id} = \frac{V_{id}}{i_i} \qquad (10)$$

$$V_{id} = R_1 i_I + R_1 i_i \qquad (11)$$

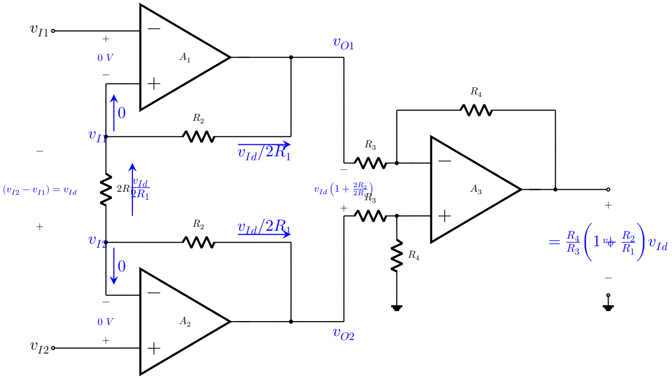
$$R_{id} = 2R_1 \qquad (12)$$

Instrumentation Amplifier



- Possible op amps saturation
- Mismatch between branches

Instrumentation Amplifier



$$A_d = \frac{V_o}{V_{id}} \tag{13}$$

$$= \frac{R_4}{R_3}\left(1+\frac{R_2}{R_1}\right) \tag{14}$$

- Common mode first stage gain $= 1$

Finite Op-Amp Gain

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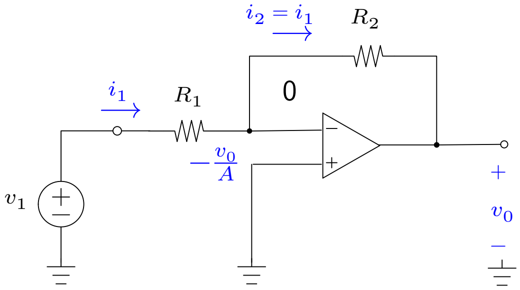
Now let's consider what happens to the gain expressions we just derived with an ideal op-amp having an infinite gain, when the op-amp gain is finite, although still very large.

- Consider the following three circuits
  - Inverting Amplifier
  - Non-Inverting Amplifier
  - Unity Gain Buffer
- Op-Amp Gain = A = not infinite, but still very large

Inverting Amplifier - Finite Gain

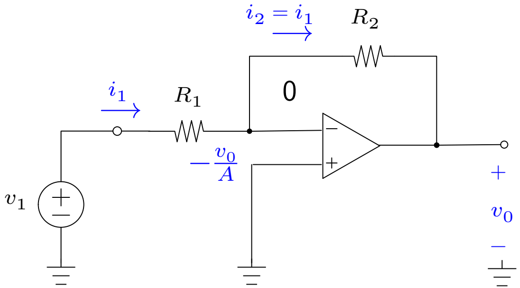


$$V_- - V_+ = -\frac{V_o}{A} \qquad (15)$$

$$i_1 = \frac{V_i - (-V_o/A)}{R_1} \qquad (16)$$

$$= \frac{V_i + V_o/A}{R_1} \qquad (17)$$

Inverting Amplifier –Finite Gain



$$V_- - V_+ = -\frac{V_o}{A} \quad (18)$$

$$V_o = -\frac{V_o}{A} - i_1 R_2 \quad (19)$$

$$= -\frac{V_o}{A} - \left(\frac{V_i + V_o/A}{R_1}\right) R_2 \quad (20)$$

Finite Gain Example

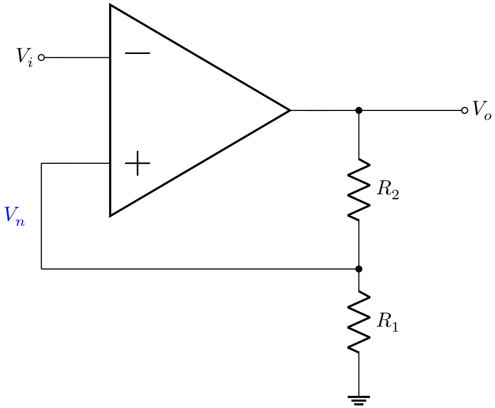
$R_1 = R_2$, $A = 1000$, what is the gain?

$$G = \frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A} \tag{21}$$

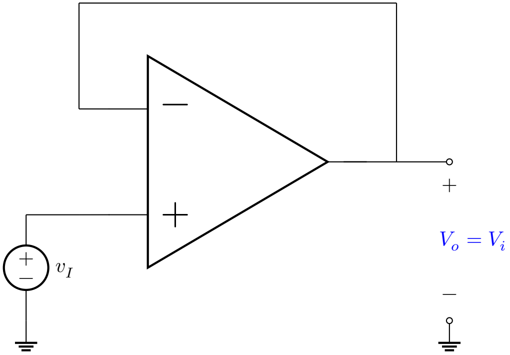
This can also be expressed in terms of feedback factor β

$$G = -\frac{R_2}{k_1}\left(\frac{\beta A}{1 + AA}\right) \tag{22}$$

Non-Inverting (Finite Gain)



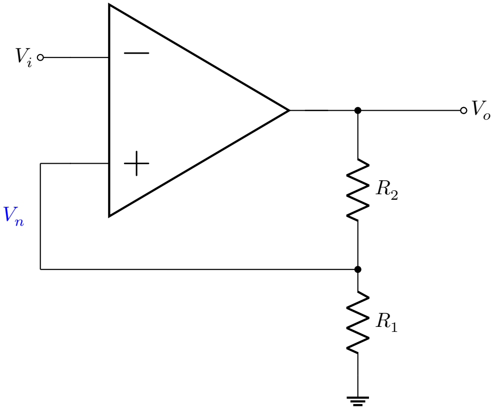
Unity Gain Buffer with Finite Gain



Op-Amp Output Resistance > 0

- Non-Inverting Amplifier
  - Effect on overall gain
- Unity Gain Buffer
  - Effect on overall gain
  - Effect on overall output resistance

Non-Inverting, Finite Gain, Rout >0



Earlier with $R_{out} = 0$

$$\frac{V_o}{V_i} = \frac{A}{1 + \beta A} \tag{23}$$

Non-Inverting, Finite Gain, Rout >0

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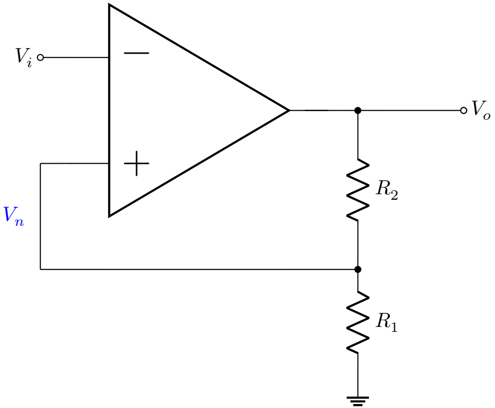


R_{out} reduces effective gain

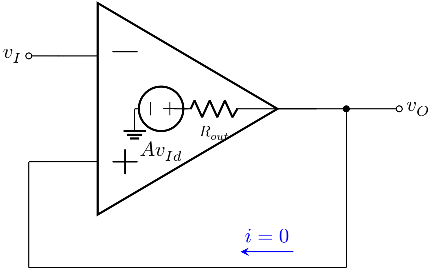
$$v_{eff} = Av_{Ia}\frac{R_1 + R_2}{R_1 + R_2 + R_{out}} \tag{24}$$

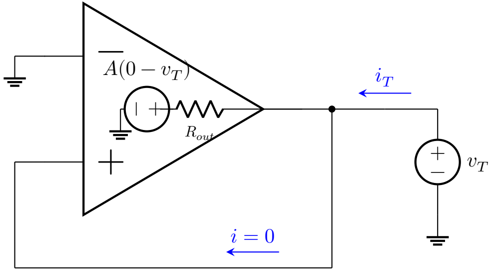
$$A_{eff} = A\frac{R_1 + R_2}{R_{out} + R_1 + R_2} \tag{25}$$

Close loop gain:

$$\frac{V_o}{V_i} = \frac{A_{eff}}{1 + \beta A_{eff}} \tag{26}$$

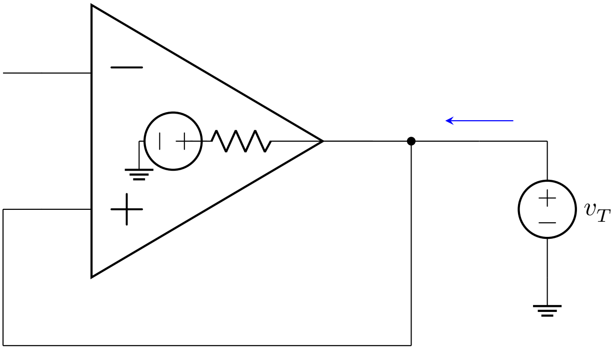
Non-Inverting, Finite Gain, Rout >0





- How to find out the output impedance?

Non-Inverting, Finite Gain, Rout >0



$R_{out} = 100\ \Omega$
A $= 1000{,}000$

Summary

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- Finite op-amp open-loop gain causes an error in the closed-loop gain of the amplifier.
- The error is related to the finite open-loop gain A of the op-amp.
- The finite output resistance of the op-amp reduces the effective gain.
- However, when used in a closed-loop circuit, the output resistance of the closed-loop amplifier is still reasonably low because of the large gain of the open-loop op-amp.

Common and Differential Mode

Read: Sedra & Smith 2.4

- Assume two signals, one is 1001 V, and the other is 999 V volts.
- To amplify the difference of these two signals, that is 1001 - 999 = 2 V.
- But if you feed these signals to the two inputs of an op-amp-based amplifier, then each op-amp input will see the large voltages, not just the difference.
- The op-amp has a non-ideality in that it would amplify a portion of the large voltage.

Common and Differential Mode

- The two signals can be thought of as being 1 volt above or below an average value of 1000 V. That is :

$$V_1 = 1001V = 1000 + 1V = V_{common-mode} + V_{id/2} \tag{27}$$

$$V_2 = 999V = 1000 - 1V = V_{common-mode} - V_{id/2} \tag{28}$$

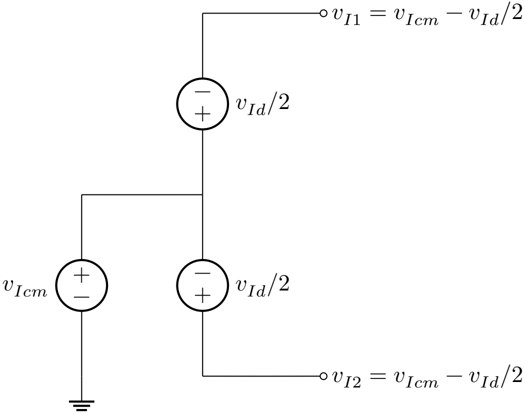
Where:

$$V_{common-mode} = V_M = (V_1 + V_2)/2 = (1001 + 999)/2 = 1000V \tag{29}$$

and

$$V_{id} = (V_1 - V_2) = (1001 - 999) = 2V \tag{30}$$

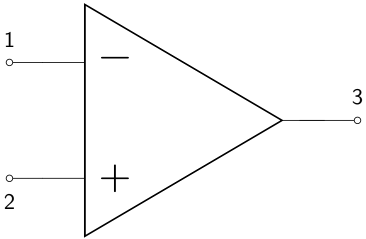
Common and Differential Mode



$$v_{Id} = v_{I2} - v_{I1} \tag{31}$$

$$v_{Icm} = \frac{1}{2}\left(v_{I1} + v_{I2}\right) \tag{32}$$

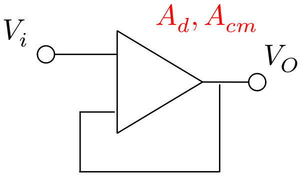
Common and Differential Mode



$$V_o = A_d V_{Id} + A_{cm} V_{IC} \quad (33)$$

$$CMRR = 20\ log \frac{|A_d|}{|A_{CM}|} \quad (34)$$

Unity Gain Buffer (Finite A_d, $A_c = 0$)



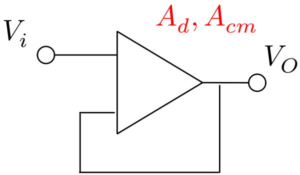
$$V_o = \frac{A_d}{1 + A_d} V_i \quad (35)$$

$$V_o = A_d V_{Id} + A_{CM} V_{IC} \quad (36)$$

$$V_{Id} = V_i - V_o \quad (37)$$

$$V_{IC} = \frac{V_i + V_o}{2} \quad (38)$$

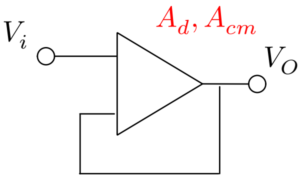
Unity Gain Buffer (Finite A_d, Finite A_c)



$$V_o = A_d V_{Id} + \frac{A_d}{CMRR} V_{IC} \tag{39}$$

$$V_o = A_d \left(V_{Id} + \frac{V_{IC}}{CMRR} \right) \tag{40}$$

Unity Gain Buffer



$$V_o = A_d\left(V_{I_D} + \frac{1}{CMRR}V_{IC}\right) \tag{41}$$

$$= A_d\left(V_i - V_o + \frac{1}{CMRR}\cdot\frac{V_i + V_o}{2}\right) \tag{42}$$

$$\frac{V_o}{V_i} = \frac{A_d\left(1 + \frac{1}{2CMRR}\right)}{1 + A_d\left(1 - \frac{1}{2CMRR}\right)} \tag{43}$$

Summary

- If the signal is carried across two wires, we typically have two components to an input signal, the common-mode component and the differential mode component.
- We want to amplify the differential-mode component, therefore we want the amplifier to have a common-mode gain that is as close to zero as possible, and a differential-mode gain as large as possible.
- The ratio of the magnitude of the differential-mode gain to common-mode gain is called the common-mode rejection ratio (CMRR) and is often described in dB.

Non-Ideal Opamps

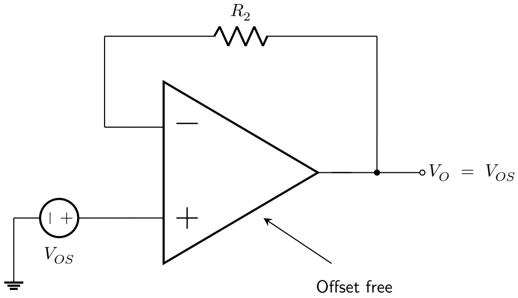
- So far we have assumed that the output voltage of the op-amp will be zero when the input is zero, and that it can be any amplitude, and that it can change as fast as we want it to change.
- In reality that is of course not the case, there are limitations on how large or fast the output voltage can change and what the output voltage is when there is no input.
- Let's discuss offset voltage first.

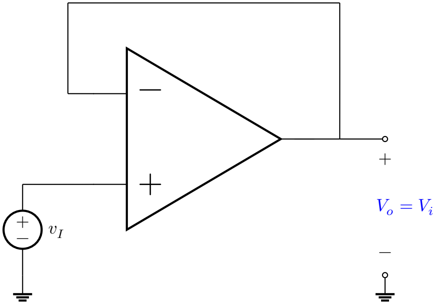
Offset Voltage (S&S 2.6)

Real op-amp transfer curve:

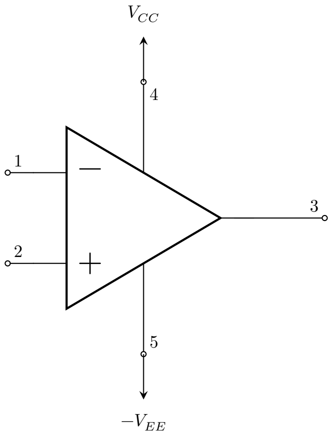
- non-zero output for zero in
- Output is limited (saturates) beyond some voltage)

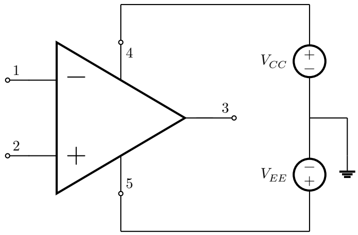
Measurement of the Offset Voltage (S&S 2.6)



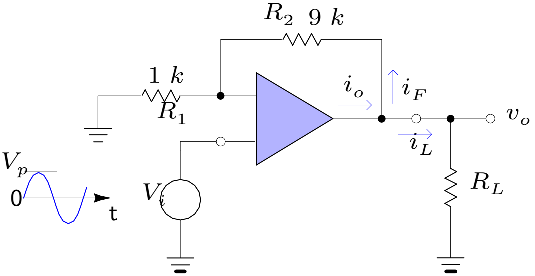


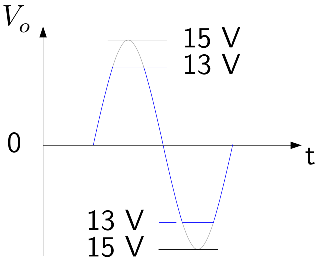
Transfer Characteristics





Clipping (Output Saturation)





- Due to limited power supply voltage and internal circuit limitations

Clipping in Closed-Loop Amplifier

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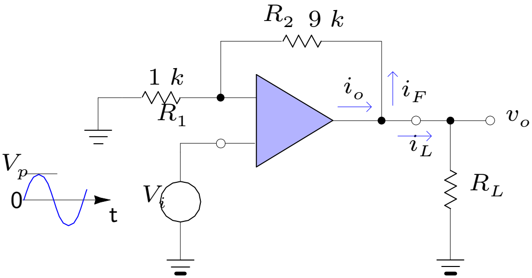

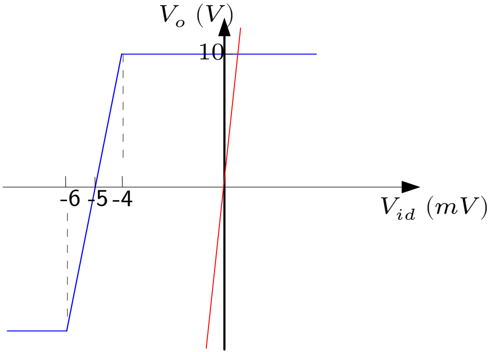

Op-amp Summary

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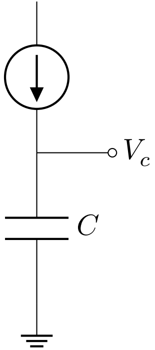
- Op-amps have an offset voltage which causes the output to be non-zero when the input is zero;
- Offset voltage is typically < 1mV, and can be random;
- Offset voltage can be trimmed, meaning it can be reduced through specific internal circuit techniques, or using external circuits;
- Maximum output voltage of an o-amp is also limited. The limits are sometimes referred to as saturation voltages, meaning the voltage value at which the output of the o—amp does not change and saturates at a specific fixed value;
- The saturation voltage is typically about 1-2 V below the supply voltage;
- Because of this saturation voltage, the waveforms at the output of a circuit utilizing an op-amp could be clipped.

Slew Rate

Sedra and Smith: Slewing, Section 2.8

- Charging capacitances within the Op-Amp limits how fast the output can change.
- it takes time to charge and discharge a capacitor.
- If you want to charge a capacitor using a constant current source, the voltage of the capacitor can only increase linearly with time.

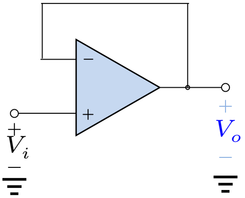


Slew Rate

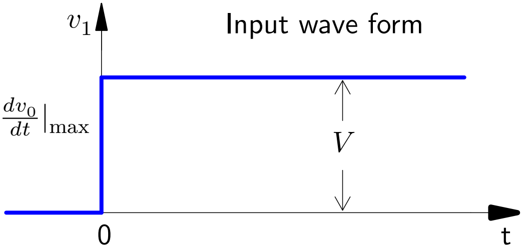
Sedra and Smith: Slewing, Section 2.8

- The slew-rate of the op-amp, simple states the maximum rate the output of the op-amp can change in time, i.e., $SR = dv_0/dt$.
- This is a large-signal effect.
- SR is usually provided in V/μsec, for example 10 V/μsec.
- This means the op-amp output voltage cannot change more than 10V in 1 μsec.

Slew Rate



$$\mathrm{SR} = \frac{dv_0}{dt}\Big|_{\max}$$



Slew Rate

- How does the output waveform look like?

$$v_i = \hat{V}_i \sin \omega t$$

- What happens for a square wave input or a sine wave input.

Slew Rate