

Final RC

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9.1 The Schottky Barrier Diode

Work function (Φ): energy difference between the vacuum energy level and the Fermi level (depend on doping concentration, not an intrinsic characteristic)

Electron affinity: energy difference between the vacuum energy level and conduction band bottom edge

(Note: here, the notation ‘m’ means metal and ‘s’ means semiconductor)

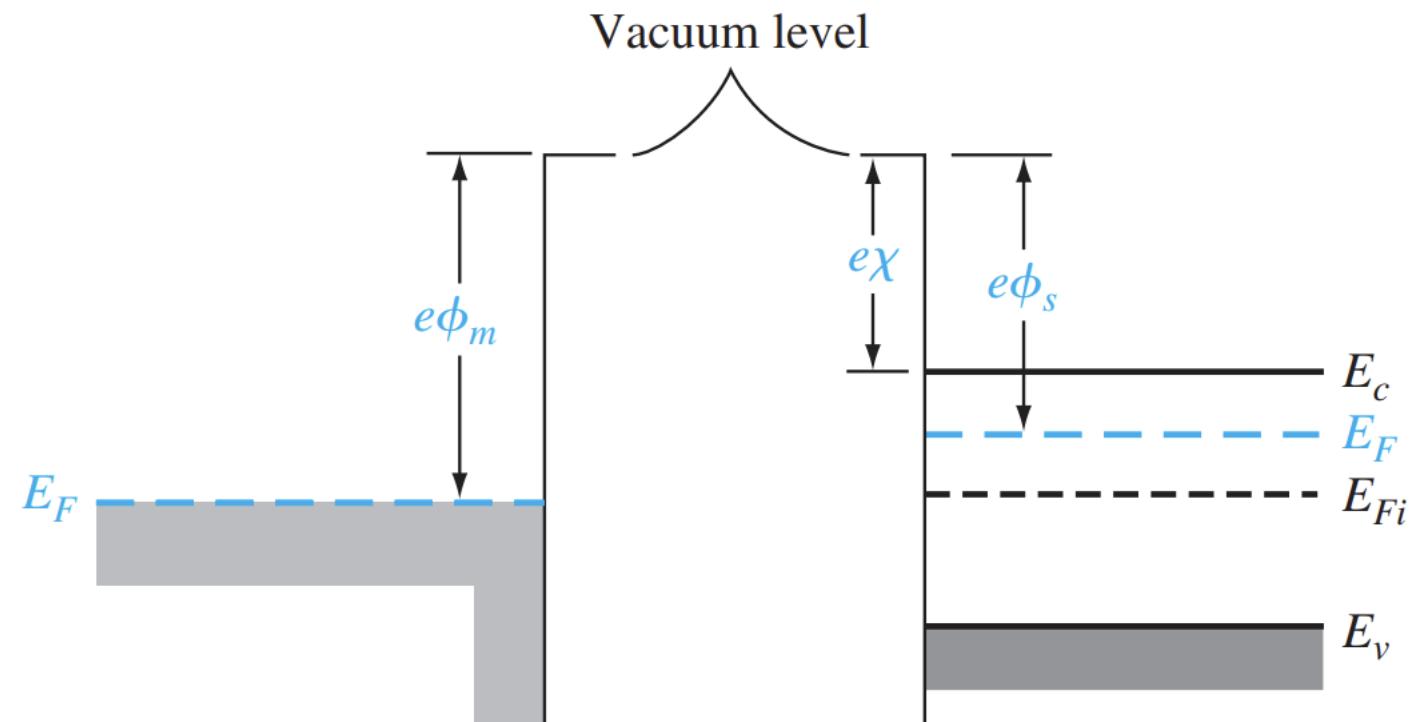


Figure. Energy-band diagram of a metal and semiconductor before contact

9.1 The Schottky Barrier Diode

The parameter ϕ_{B0} is the ideal barrier height of the semiconductor contact, the potential barrier seen by electrons in the metal trying to move into the semiconductor. This barrier is known as the *Schottky barrier* and is given, ideally, by

$$\phi_{B0} = (\phi_m - \chi)$$

On the semiconductor side, V_{bi} is the built-in potential barrier. This barrier, similar to the case of the pn junction, is the barrier seen by electrons in the conduction band trying to move into the metal. The built-in potential barrier is given by

$$V_{bi} = \phi_{B0} - \phi_n$$

which makes V_{bi} a slight function of the semiconductor doping, as is the case in a pn junction.

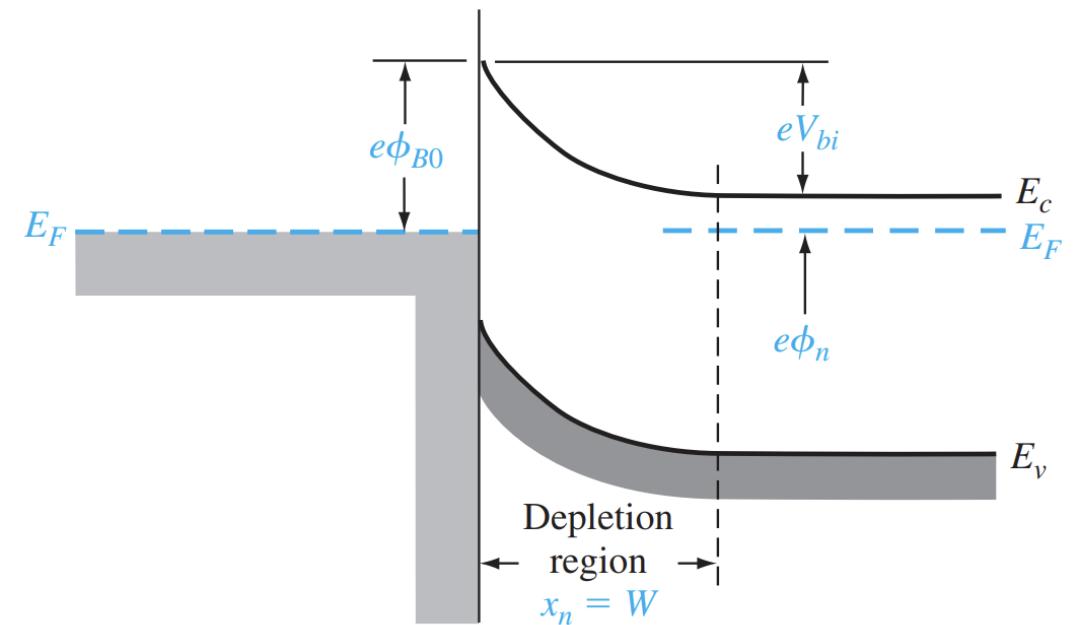


Figure. Ideal energy-band diagram of a metal-n-semiconductor for $\Phi_m > \Phi_s$

9.1 The Schottky Barrier Diode

How to draw the energy-band diagram?

- First, draw the metal and semiconductor part separately.
- Then, in thermal equilibrium, the fermi energy level should be flat. Align the fermi levels in the metal and semiconductor. You may have to bend the conduction and valence band in the semiconductor.

9.1 The Schottky Barrier Diode

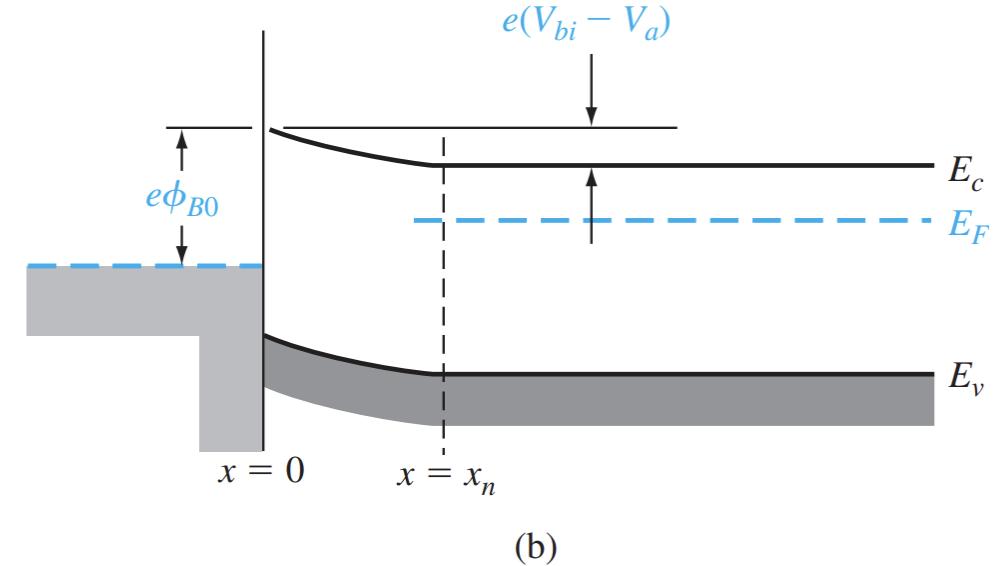
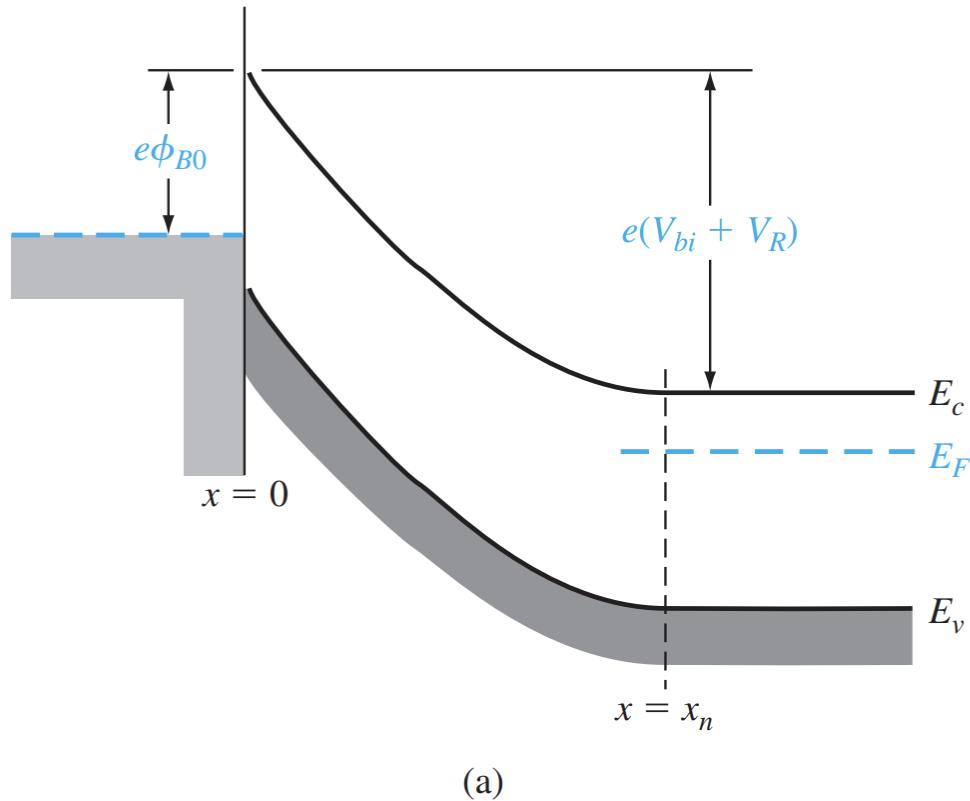


Figure. Ideal energy-band diagram of a metal–semiconductor junction (a) under reverse bias and (b) under forward bias.

9.1 The Schottky Barrier Diode

Ideal Junction Properties

- Electric Field:

$$E = -\frac{eN_d}{\epsilon_s}(x_n - x)$$

- Space Charge Region Width:

$$W = x_n = \left[\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d} \right]^{1/2}$$

(The results are similar to the one-sided p+n junction.)

9.1 The Schottky Barrier Diode

Junction Capacitance

$$C' = eN_d \frac{dx_n}{dV_R} = \left[\frac{e\epsilon_s N_d}{2(V_{bi} + V_R)} \right]^{1/2}$$

$$\left(\frac{1}{C'} \right)^2 = \frac{2(V_{bi} + V_R)}{e\epsilon_s N_d}$$

Here, C' is the capacitance per unit area.

9.1 The Schottky Barrier Diode

- Current voltage relationship

$$J = J_{sT} \left[\exp \left(\frac{eV_a}{kT} \right) - 1 \right]$$

- Reverse saturation current density

$$J_{sT} = A^* T^2 \exp \left(\frac{-e\phi_{Bn}}{kT} \right)$$

- Richardson constant

$$A^* \equiv \frac{4\pi e m_n^* k^2}{h^3}$$

9.2 Metal Semiconductor Ohmic contacts

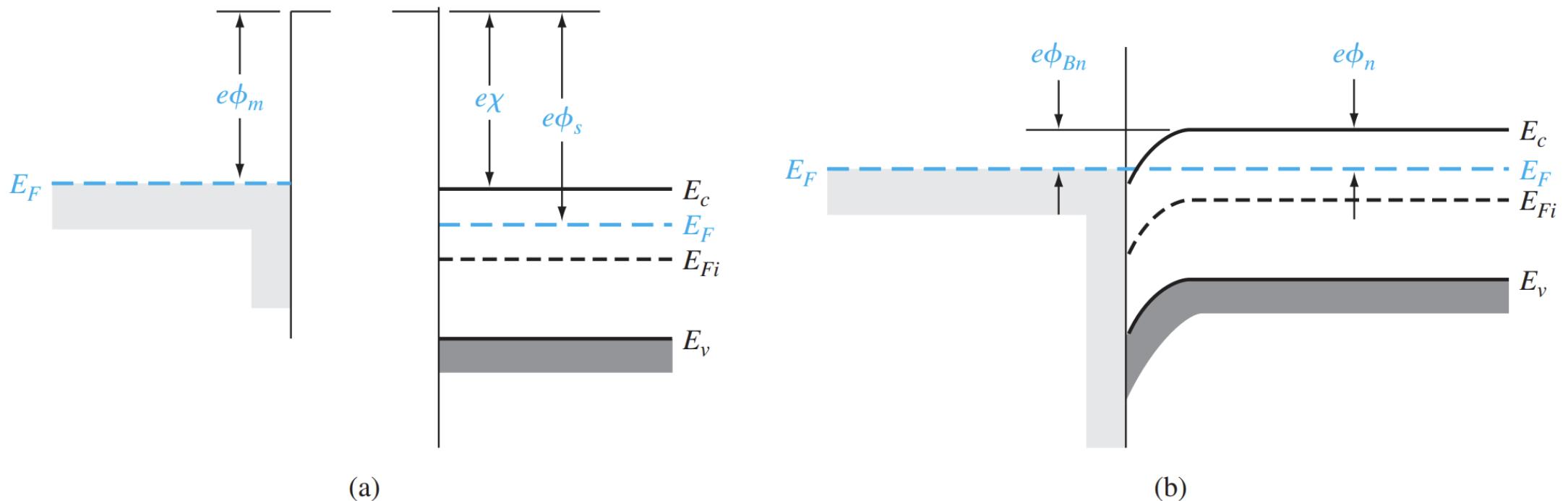


Figure. Ideal energy-band diagram (a) before contact and (b) after contact for a metal-n-type semiconductor junction for $\Phi_m < \Phi_s$

9.2 Metal Semiconductor Ohmic contacts

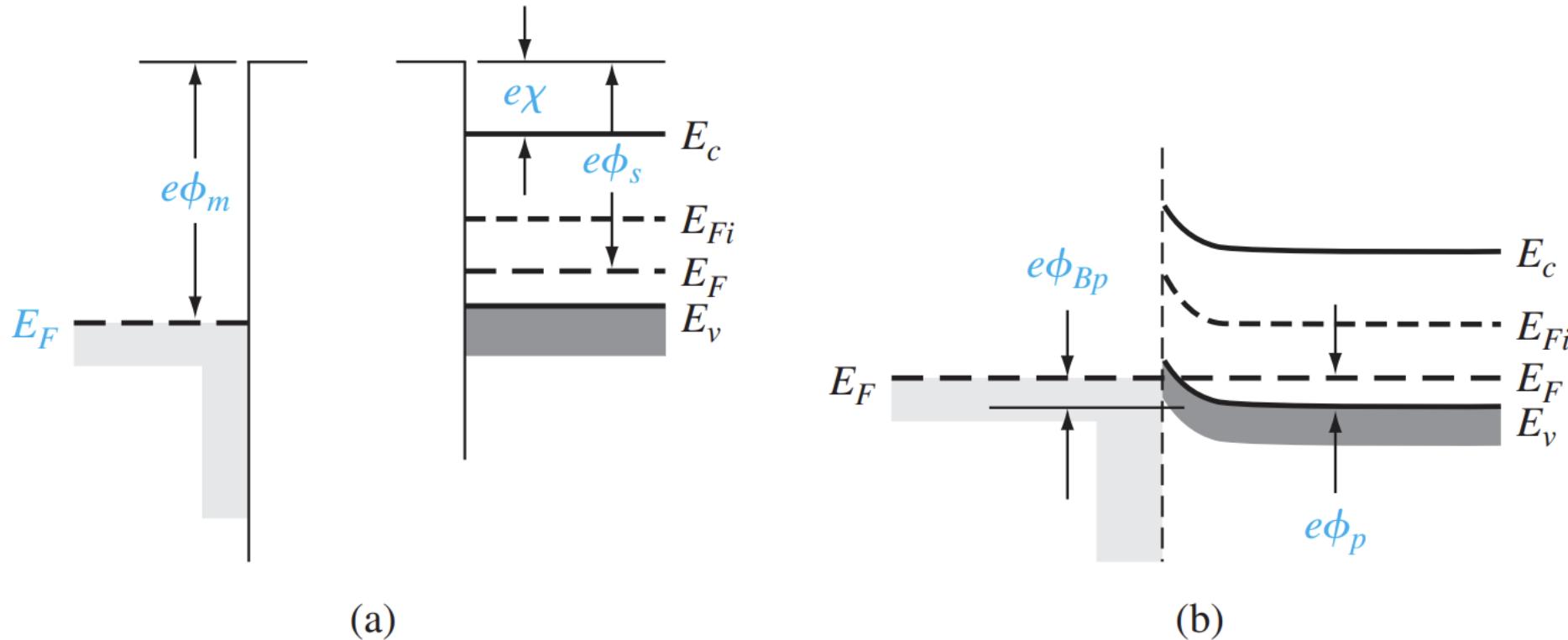
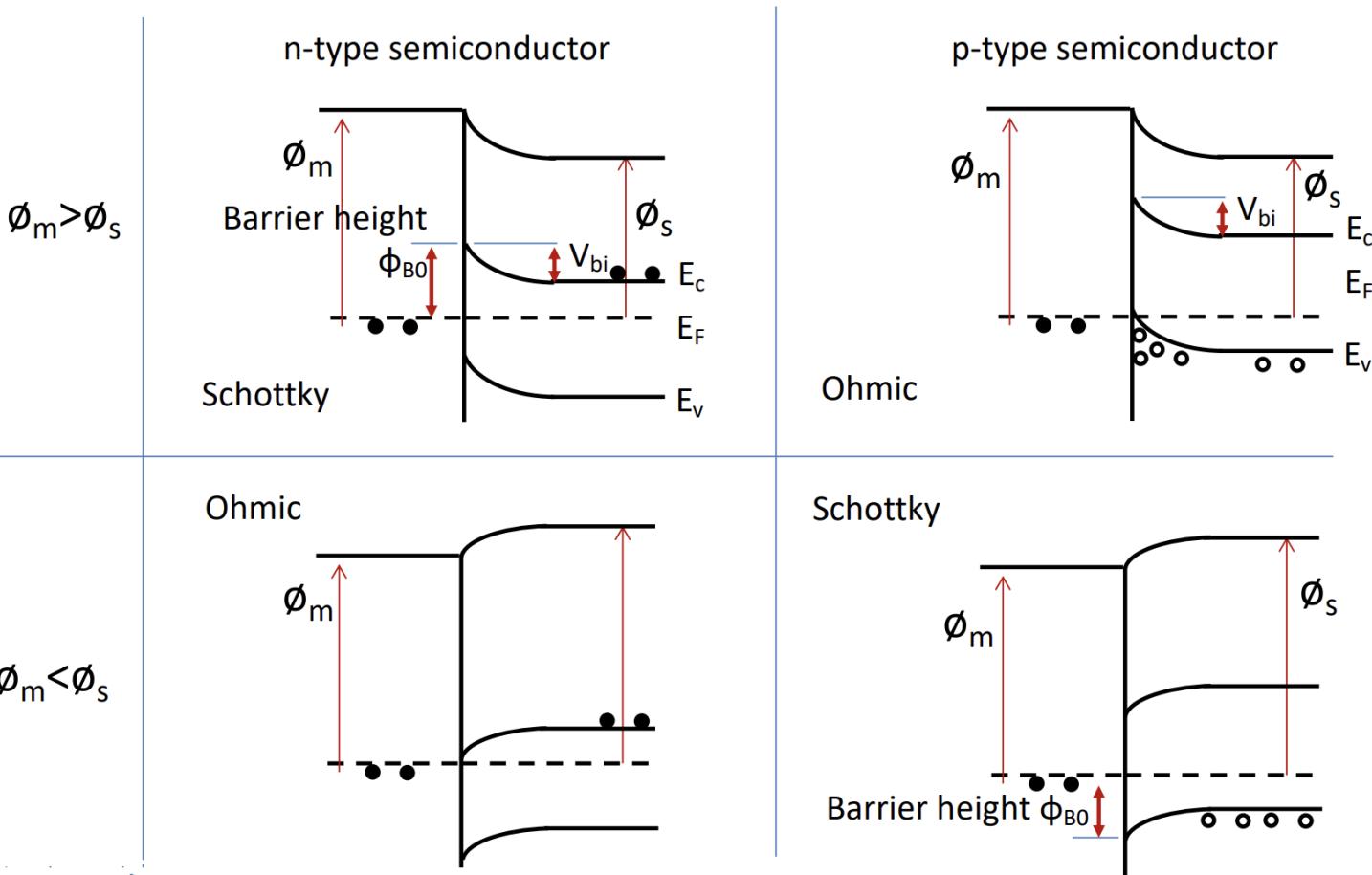


Figure. Ideal energy-band diagram (a) before contact and (b) after contact for a metal-p-type semiconductor junction for $\Phi_m > \Phi_s$

9.2 Metal Semiconductor Ohmic contacts



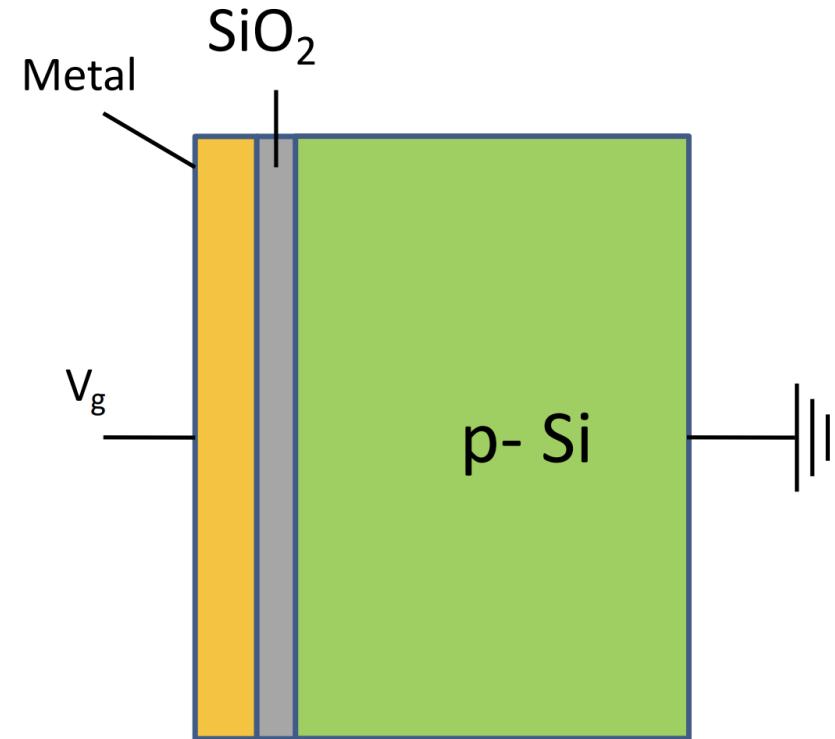
10.1 The two-terminal MOS structure

Take p-type semiconductor as an example:

V_g is the gate voltage, which is applied on the metal side.

The semiconductor side is usually grounded.

The MOS capacitor model is different from the Schottky diode model since it has an oxide layer between the metal and semiconductor.



Metal-insulator-semiconductor (MIS)

10.1 The two-terminal MOS structure

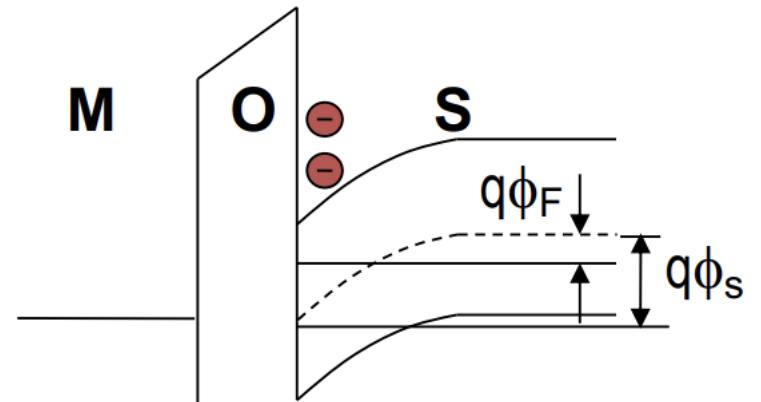
Some Important Terminologies:

- Surface potential (difference between the intrinsic fermi level of the bulk and surface):

$$\phi_s = \frac{1}{q} [E_i(\text{bulk}) - E_i(\text{surface})]$$

- Potential difference (between fermi level and intrinsic fermi level):

$$\phi_{fp} = V_t \ln \left(\frac{N_a}{n_i} \right) \quad \phi_{fn} = V_t \ln \left(\frac{N_d}{n_i} \right)$$



10.1 The two-terminal MOS structure

$V_g < 0$ (Accumulation Mode)

Negative charges will exist on the metal plate due to the negative applied voltage

An electric field will then be induced

This induced electric field will make the holes in semiconductor move towards the oxide-semiconductor interface

Positive charges are accumulated at the interface, so this is called the accumulation mode

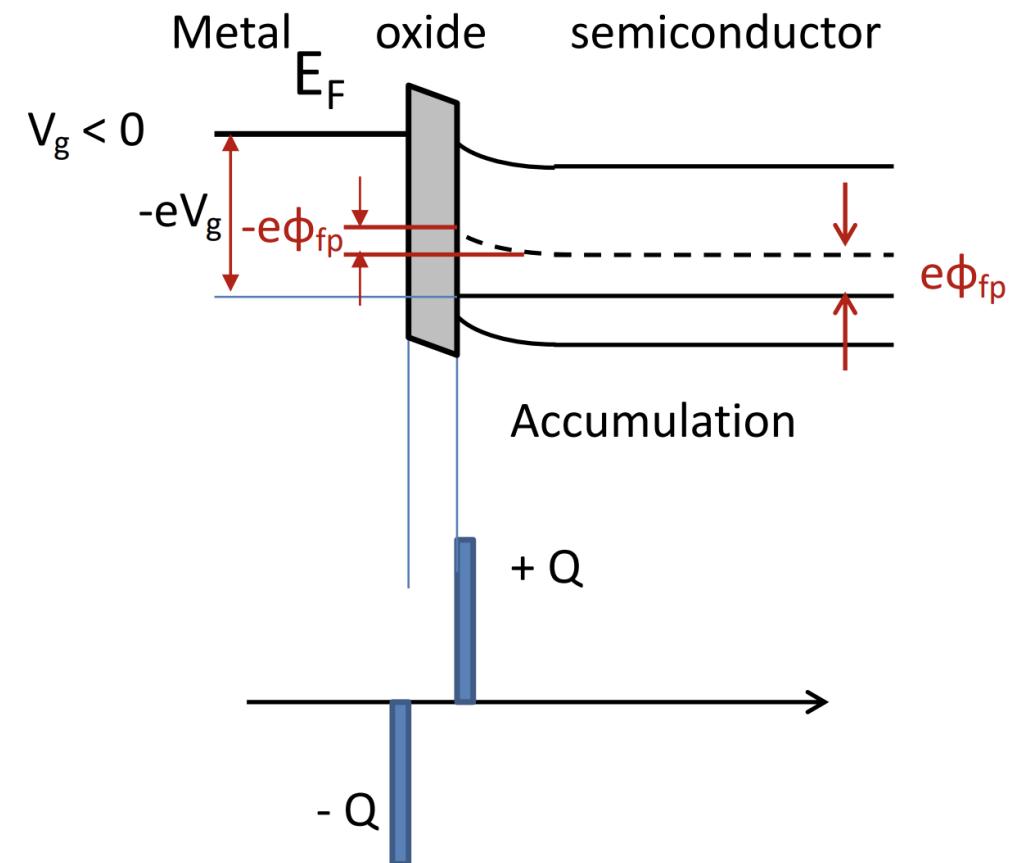


Figure. Energy-band diagram and charge distribution in accumulation mode

10.1 The two-terminal MOS structure

$V_g > 0$ (Depletion Mode)

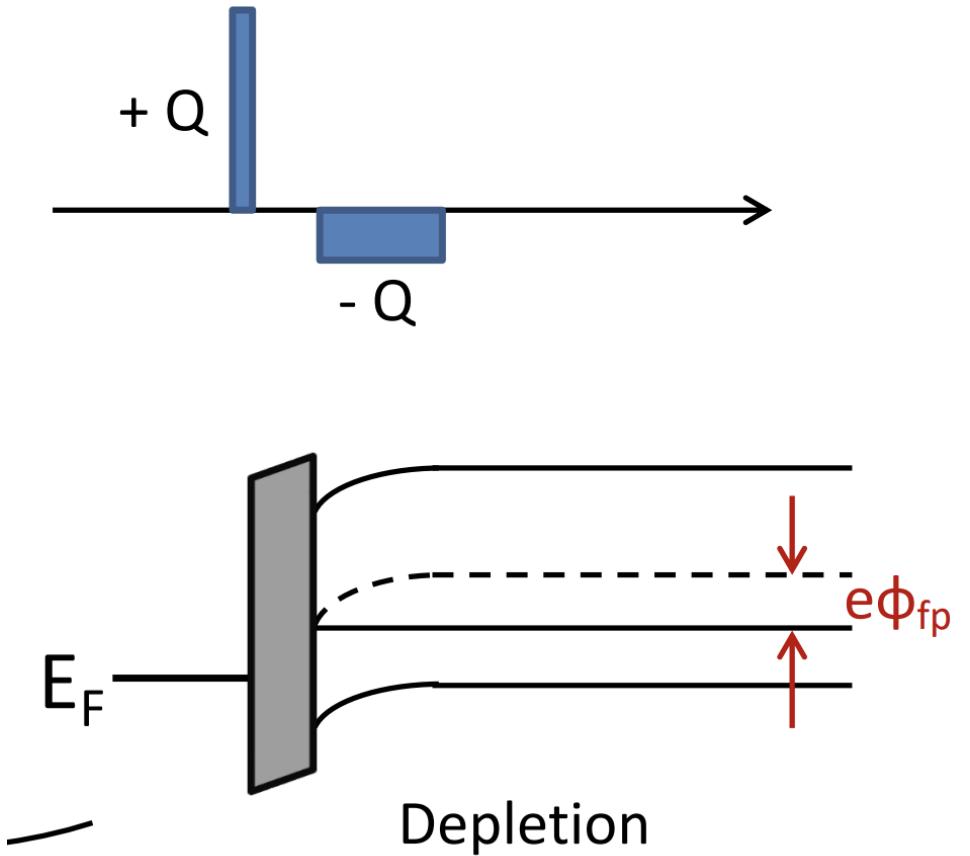
Positive charges exist on the metal plate

The induced electric field is reversed

Holes in the semiconductor are pushed away from the interface

A negative space charge region is created

Thus, this is called the depletion mode



10

Figure. Energy-band diagram and charge distribution in the depletion mode

10.1 The two-terminal MOS structure

$V_g > 0 (\Phi_f < \Phi_s < 2\Phi_f)$ Weak Inversion

The induced electric field still increases

The larger negative charge in MOS

capacitor implies a larger induced space
charge region and more band bending

The intrinsic fermi level at the surface is
below the fermi level

The surface close to the interface turns into
n-type!

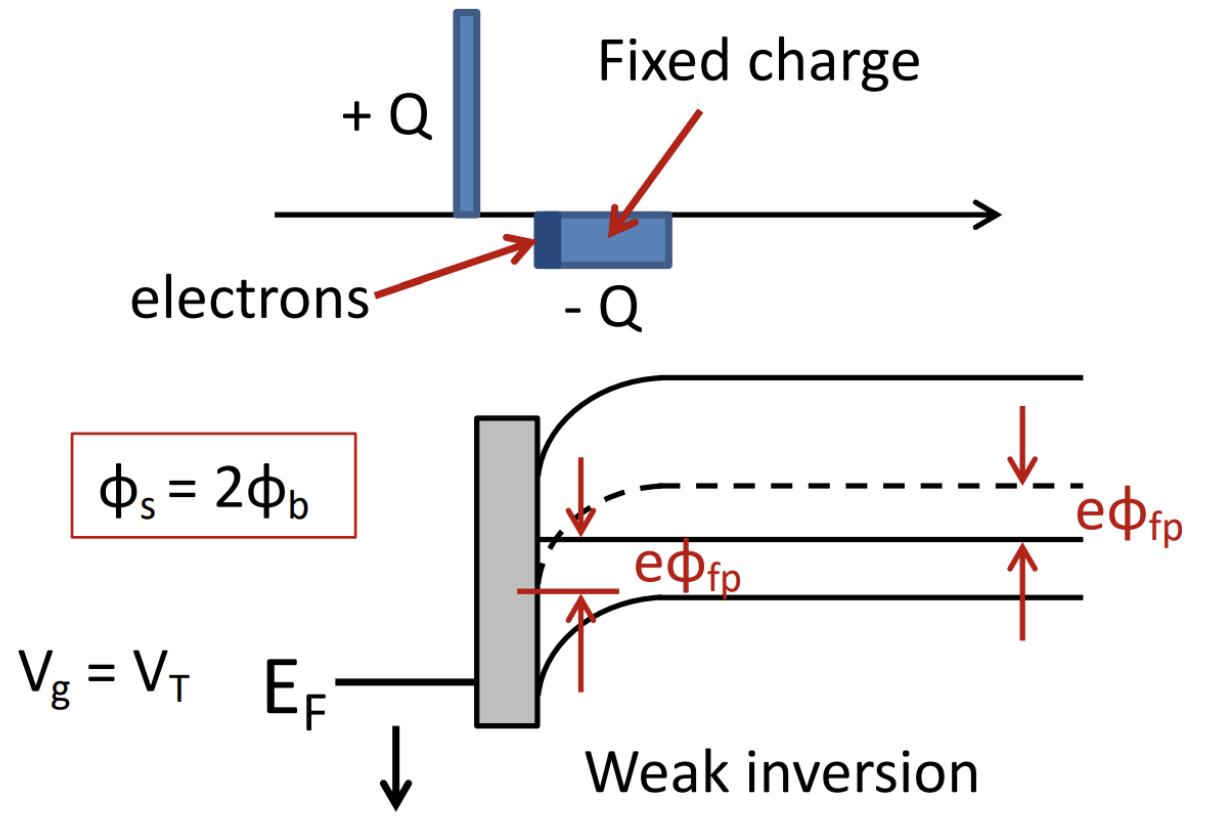


Figure. Energy-band diagram and charge distribution in the weak inversion mode

10.1 The two-terminal MOS structure

$$V_g = V_t \ (\Phi_s = 2 \Phi_f) \text{ Threshold}$$

The electron concentration at the surface is the same as the hole concentration in the bulk material.

If $V_g > V_t$, the conduction band will bend slightly closer to the Fermi level, but the change in the conduction band at the surface is now only a slight function of gate voltage. The electron concentration at the surface, however, is an exponential function of the surface potential. The surface potential may increase by a few (kT/e) volts, which will change the electron concentration by orders of magnitude, but the space charge width changes only slightly. In this case, then, the space charge region has essentially reached a maximum width.

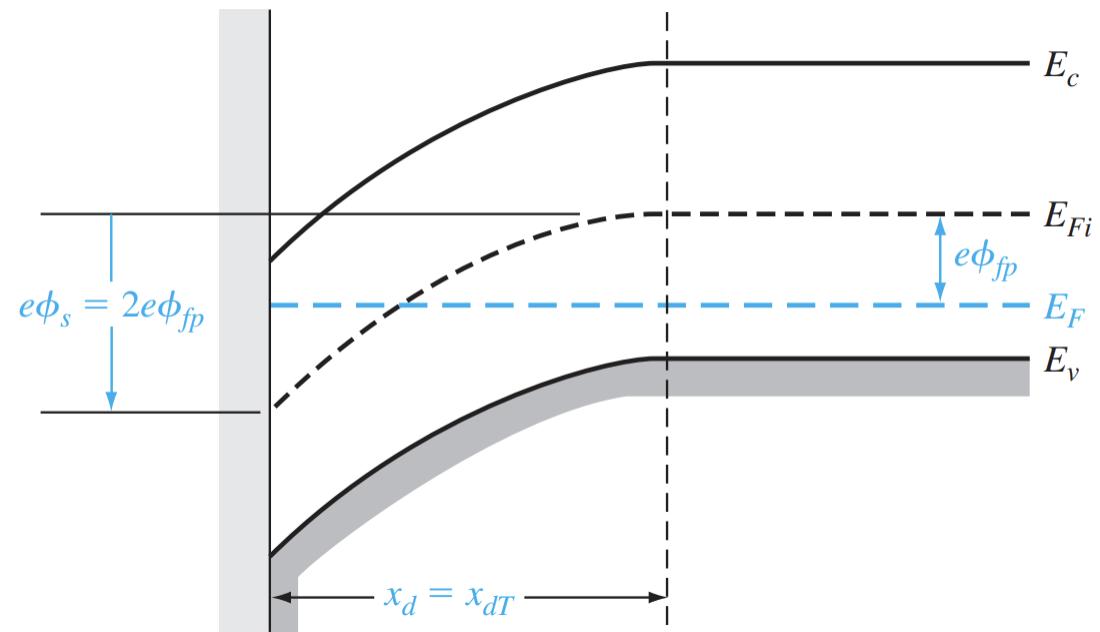


Figure. Energy-band diagram under the threshold voltage

10.1 The two-terminal MOS structure

- Space charge region width

$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a} \right)^{1/2}$$

- Maximum depletion width:

Since threshold inversion point is $\phi_s = 2\phi_F$

Then, maximum depletion layer is

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a} \right)^{1/2}$$

10.1 The two-terminal MOS structure

$$V_g > V_t \ (\Phi_s > 2\Phi_f \text{ Strong Inversion})$$

The electric concentration at the surface is greater than the hole concentration in the bulk material

So, this is called strong inversion

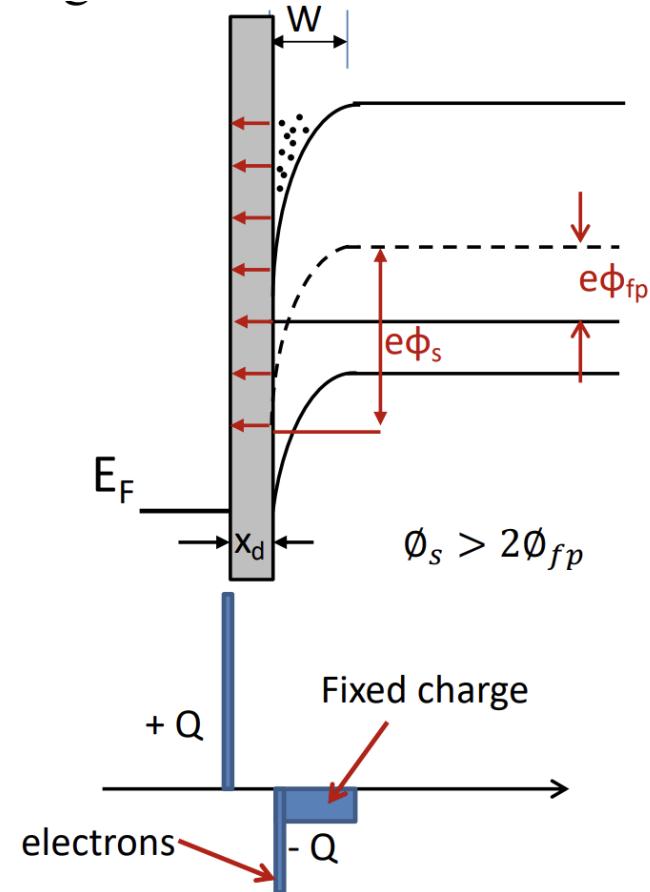
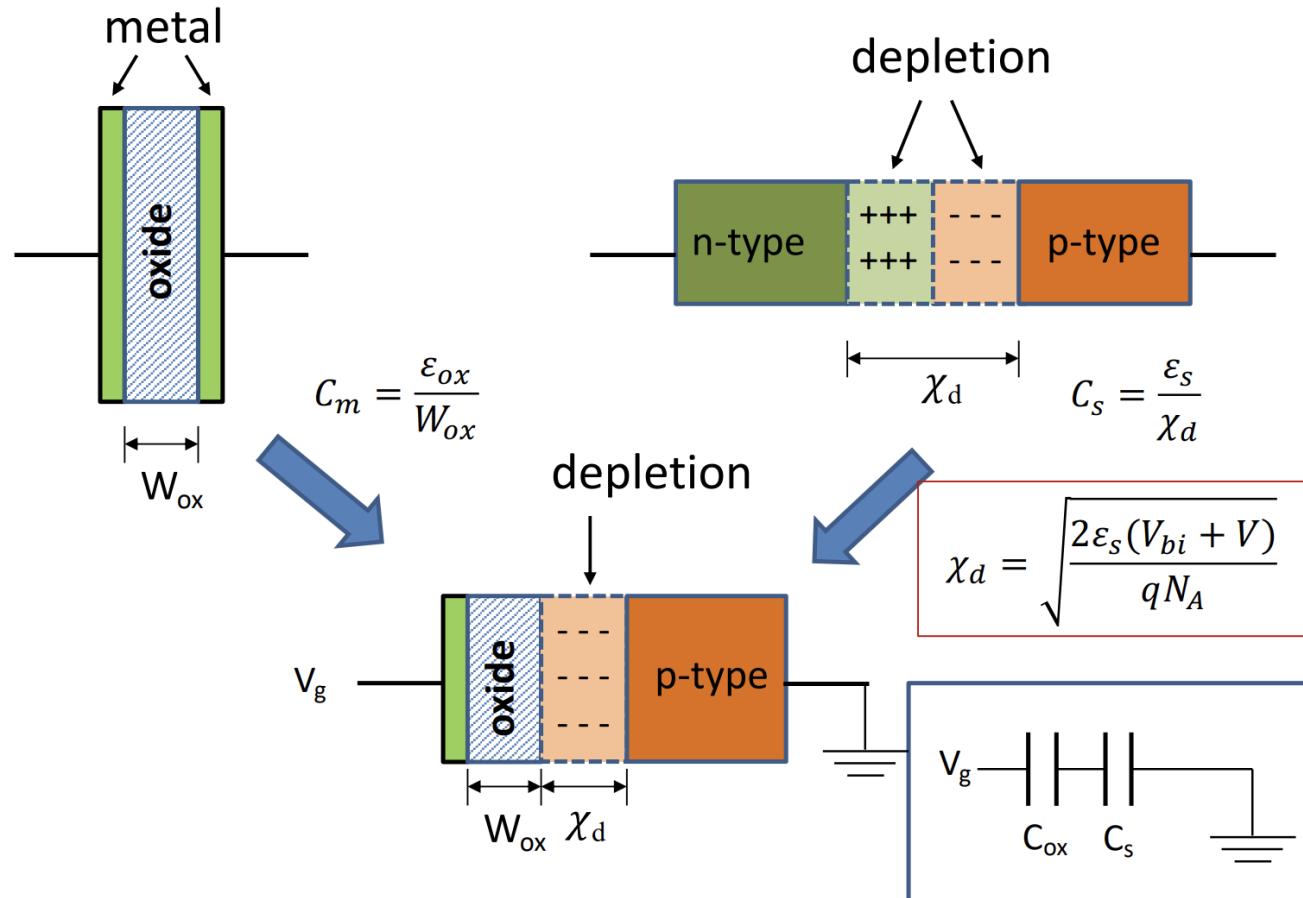


Figure. Energy-band diagram and charge distribution

10.2 Capacitance-voltage characteristics

MOS capacitance structure is composed of two parts: the oxide capacitance and semiconductor capacitance (caused by depletion region). The two capacitances are in series.



10.2 Capacitance-voltage characteristics

Accumulation:

C_s is almost infinite.

A small change in V_g will cause a differential change in charge on the metal side and also hole accumulation charge. So the total capacitance is just C_{ox} .

$$C'(acc) = C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

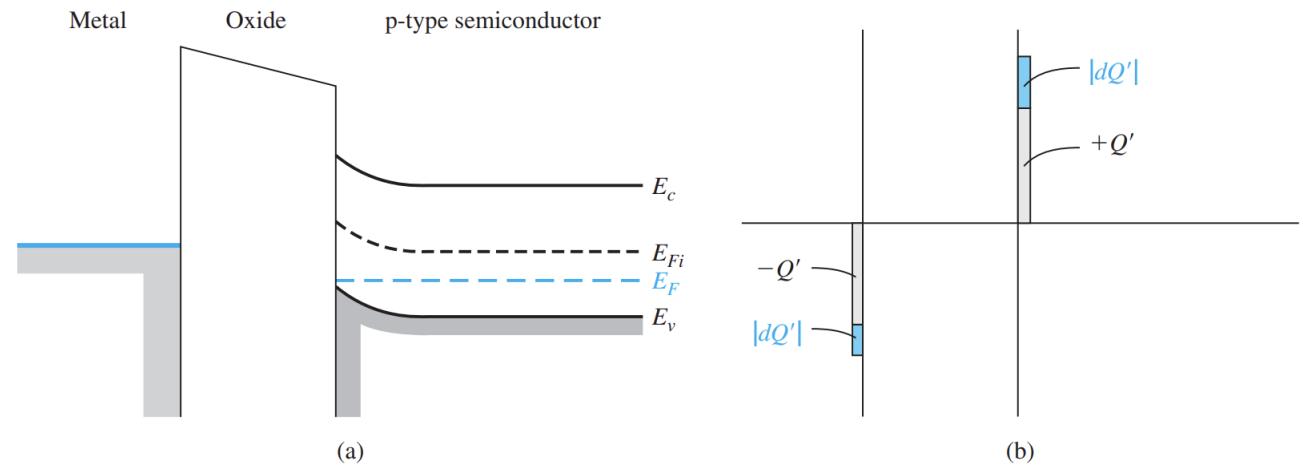


Figure. (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gain voltage

10.2 Capacitance-voltage characteristics

Depletion and weak inversion:
 C_s and C_{ox} are in series.

$$C'(\text{depl}) = \frac{C_{ox} C'_{SD}}{C_{ox} + C'_{SD}}$$

And since $C_{ox} = \epsilon_{ox}/t_{ox}$ and $C'_{SD} = \epsilon_s/x_d$,

We have $C'(\text{depl}) = \frac{C_{ox}}{1 + \frac{C_{ox}}{C'_{SD}}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_d}$

Obviously, when x_d increases, total capacitance decreases. Thus, when the space charge width reaches its maximum, capacitance will reach its minimum.

$$C'_{\min} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) x_{dT}}$$

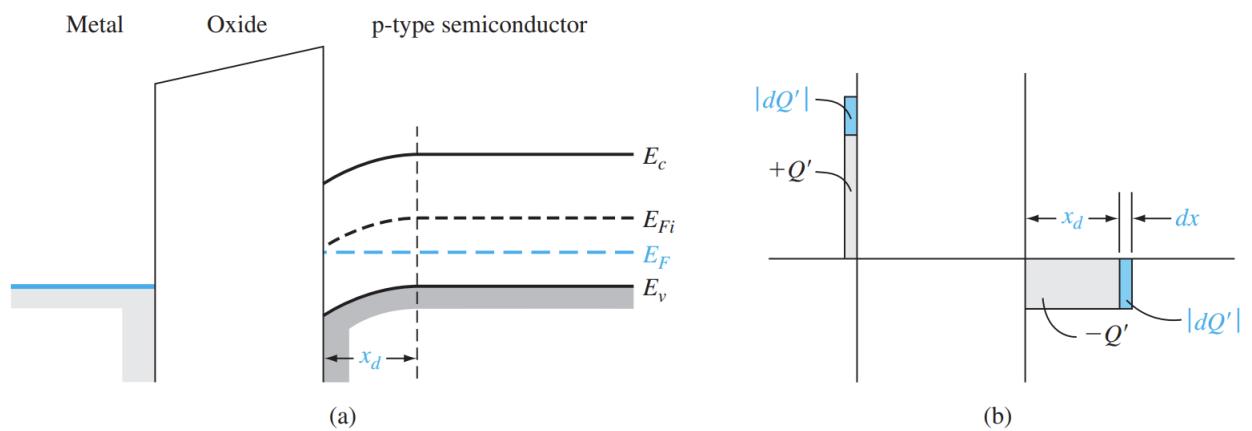


Figure. (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

10.2 Capacitance-voltage characteristics

Strong inversion:

A small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density. The space charge width does not change.

As a result, the capacitance will be the oxide capacitance.

$$C'(\text{inv}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

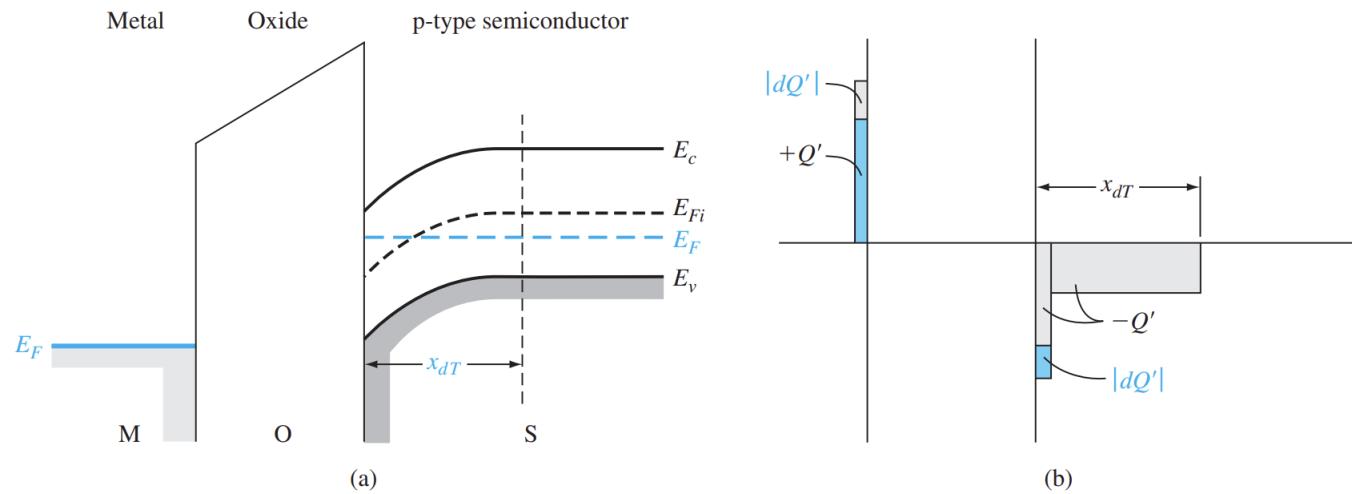


Figure. (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

10.2 Capacitance-voltage characteristics

Here:

Moderate inversion: the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.

Flat band condition: happens between the accumulation and depletion mode.

Capacitance at flat band:

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right) \sqrt{\left(\frac{kT}{e}\right) \left(\frac{\epsilon_s}{eN_a}\right)}}$$

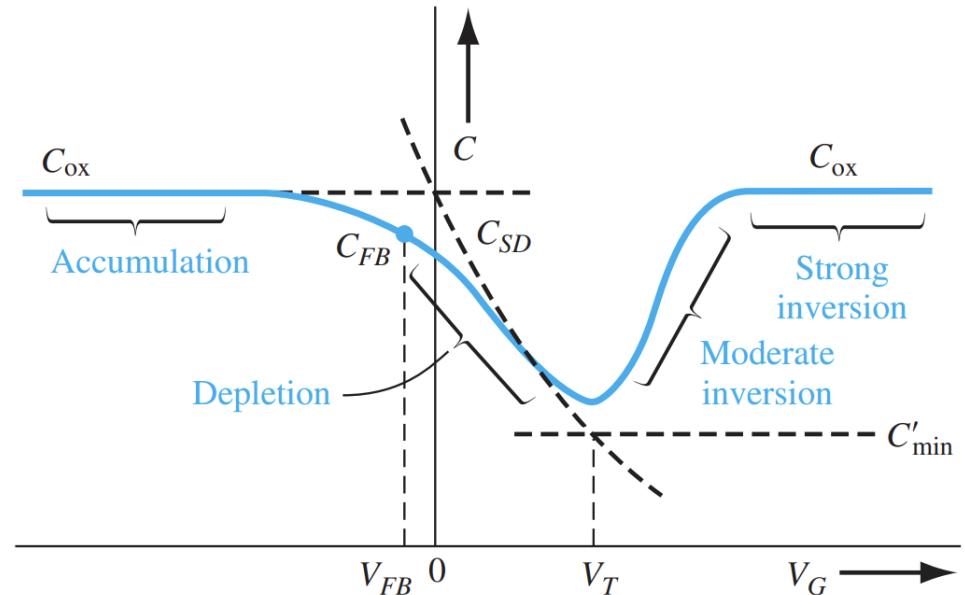


Figure. Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate

10.2 Capacitance-voltage characteristics

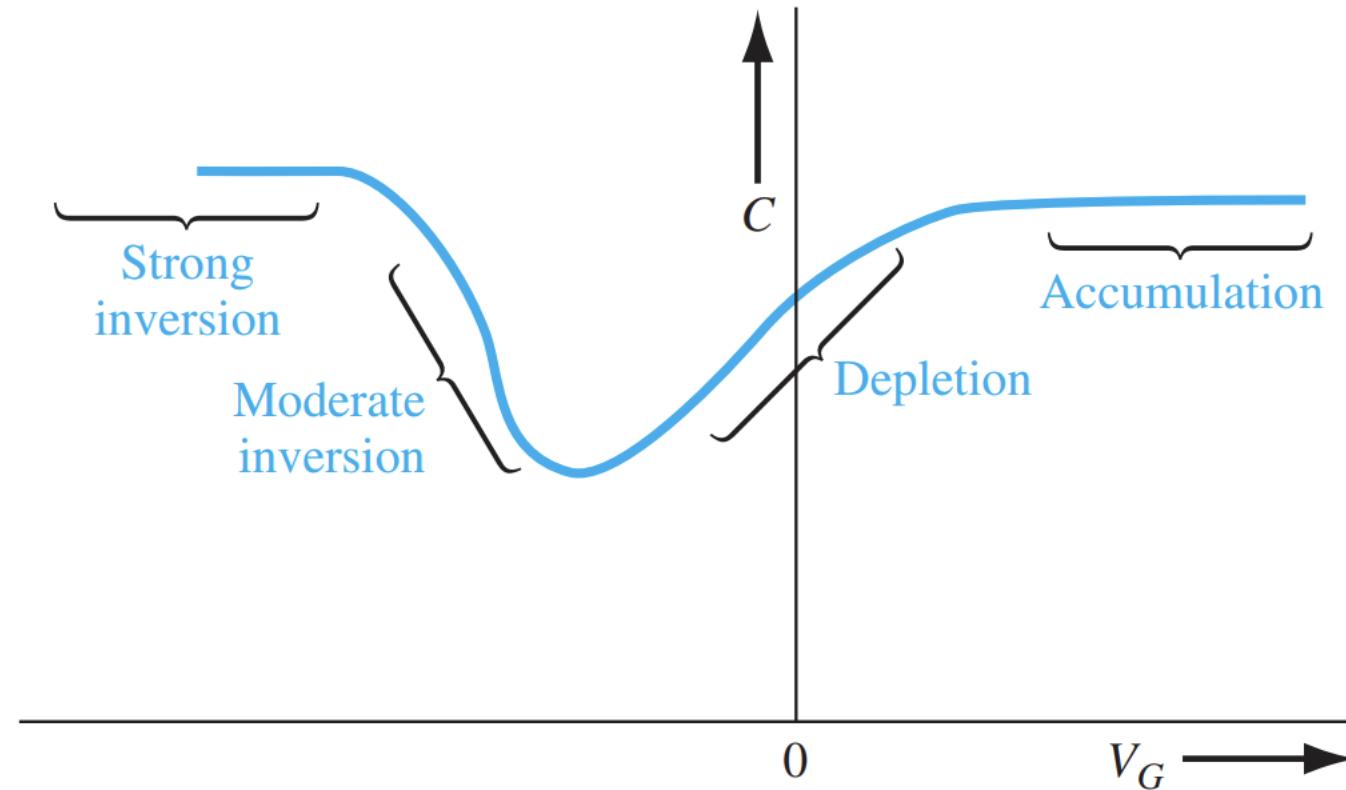


Figure. Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n-type substrate.

10.2 Capacitance-voltage characteristics

The threshold voltage should be sum of the voltage across the semiconductor and the oxide.

$$V_T = V_s + V_{ox}$$

At threshold, voltage across the semiconductor should be $V_s = 2\phi_{fp}$

For voltage across the oxide,

$$V_{ox} = \frac{Q_{ox}}{C_{ox}} = \frac{ex_{dT}N_a}{C_{ox}} = \frac{2\sqrt{e\varepsilon_s N_a \phi_{fp}}}{C_{ox}}$$

Therefore,

$$V_T = 2\phi_{fp} + \frac{2\sqrt{e\varepsilon_s N_a \phi_{fp}}}{C_{ox}}$$

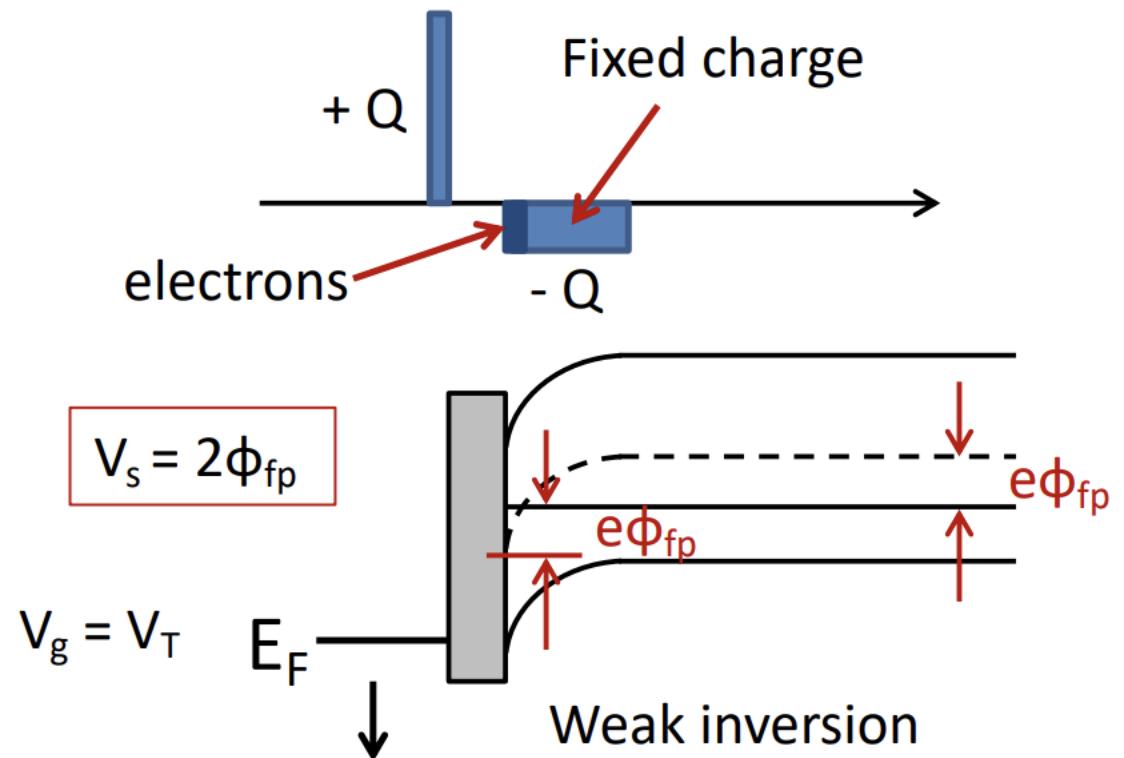


Figure. Energy-band diagram and charge distribution at the threshold voltage

10.2 Capacitance-voltage characteristics

Two sources of electrons (in the inversion layer):

1. Diffusion of minority carrier electrons
2. Thermal generation of electron-hole pairs within the space charge region.

Frequency effects: electron concentration in the inversion layer cannot change rapidly. In the limit of a high frequency, the inversion layer charge will not respond to a differential change in capacitor voltage.

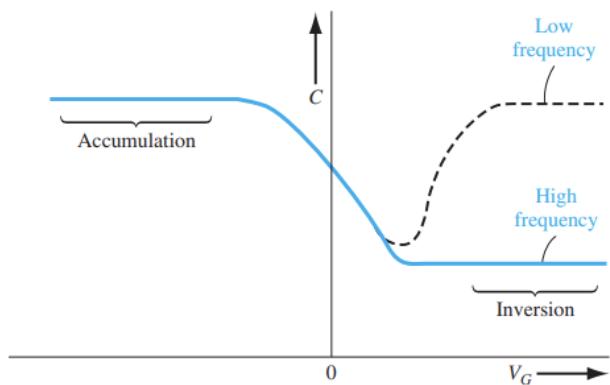
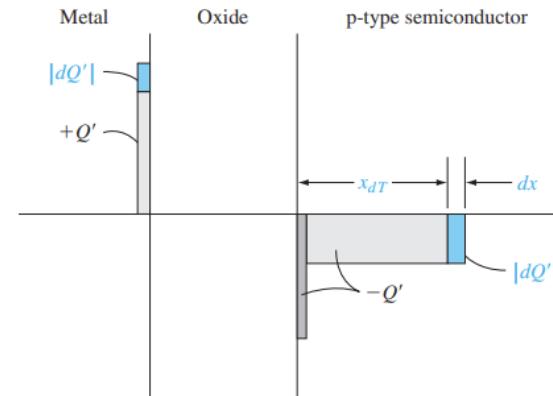


Figure. Charge distribution and low-freq and high-freq capacitance vs gate voltage. (p-type substrate)

10.3 Non-ideal effects

Metal-semiconductor work function difference:

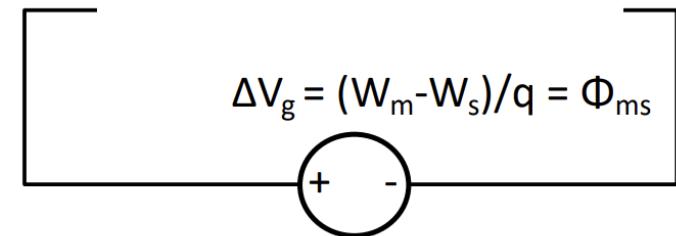
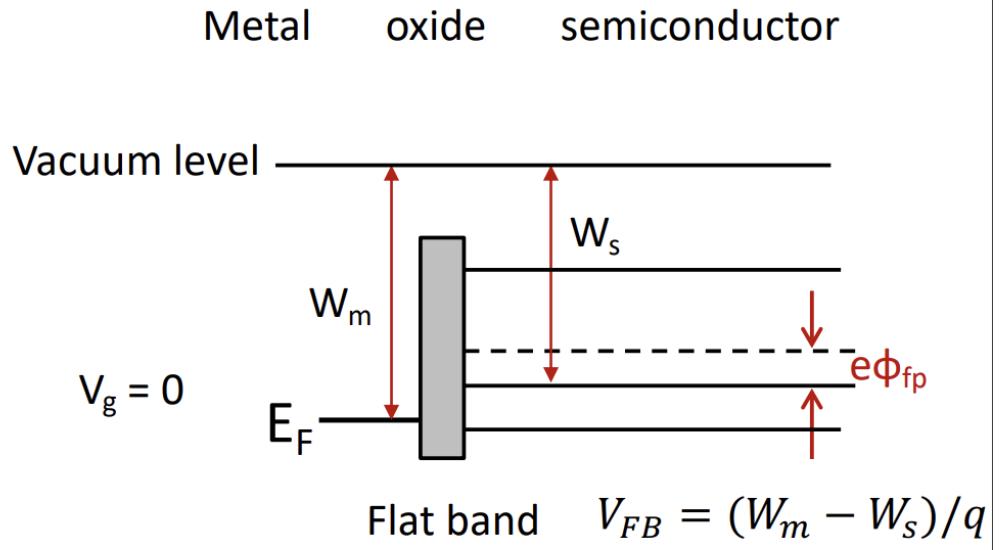
$$\phi_{ms} = \phi_m - \phi_s$$

Here, flat band voltage $V_{FB} = \phi_{ms}$

Thus, the threshold voltage

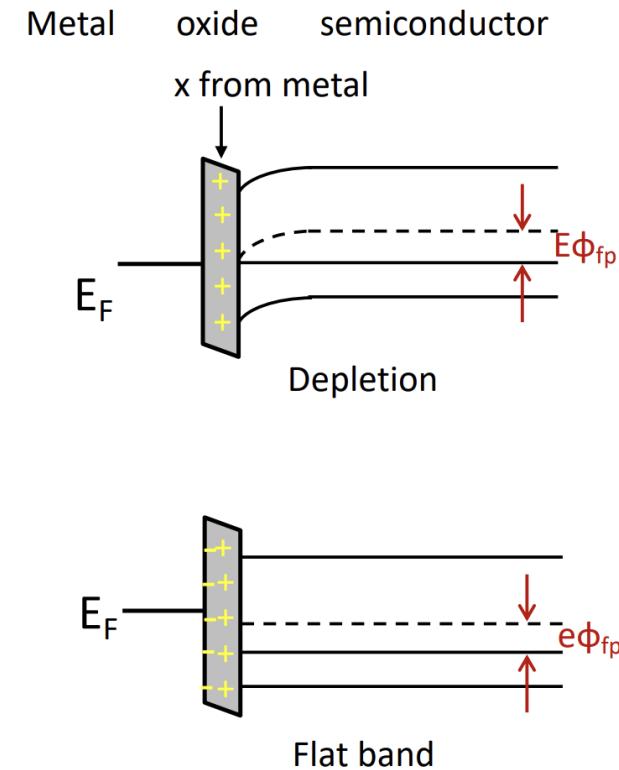
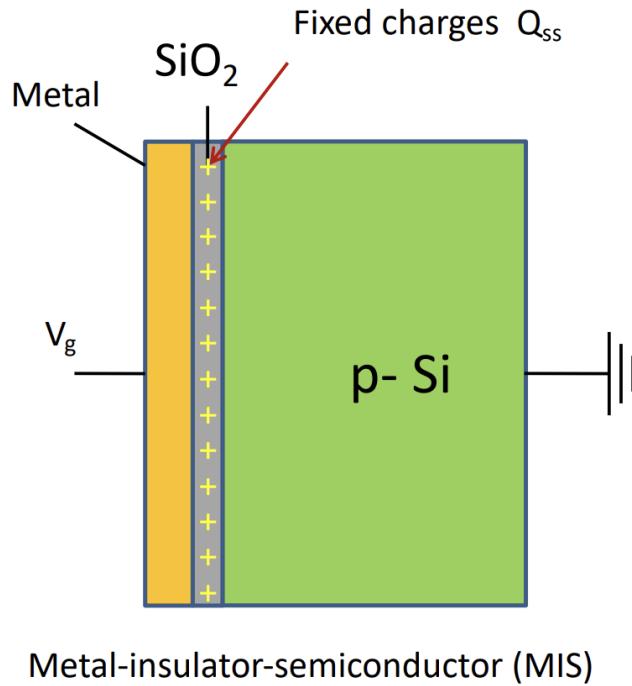
$$V_T = 2\phi_{fp} + t_{ox} \sqrt{\frac{4eN_a \epsilon_{Si} \phi_{fp}}{\epsilon_{ox}^2}} + V_{FB}$$

$$= 2\phi_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \phi_{ms}$$



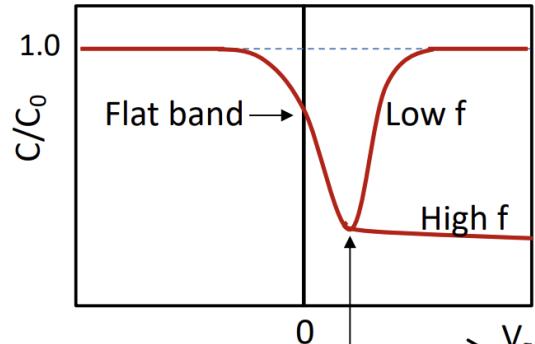
10.3 Non-ideal effects

Fixed charges

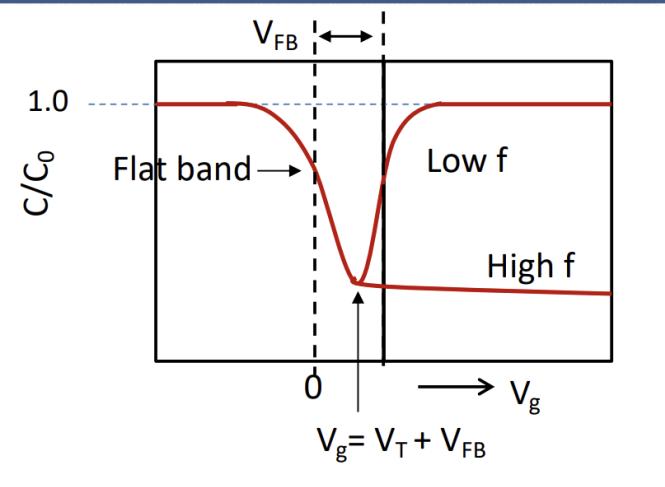
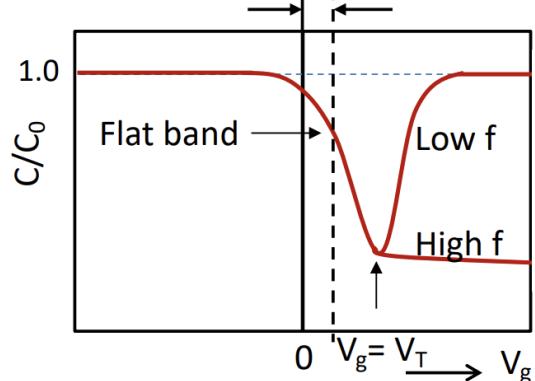


10.3 Non-ideal effects

Fixed charges



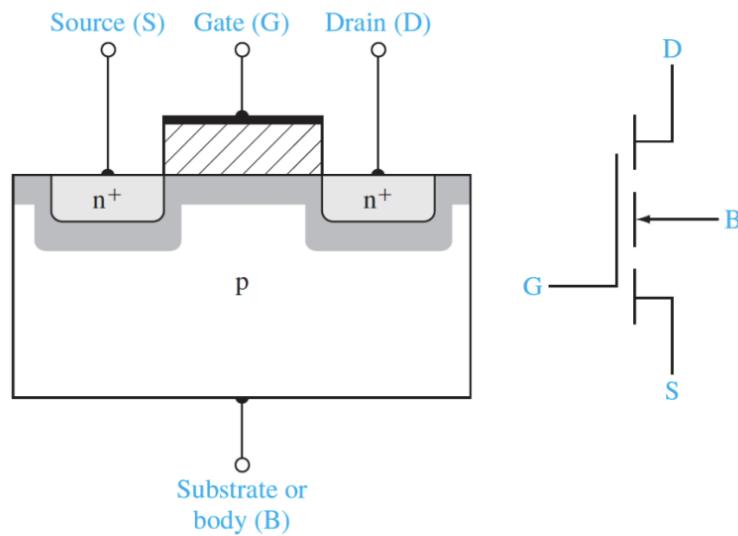
$$\Delta V_g = (W_m - W_s)/q$$



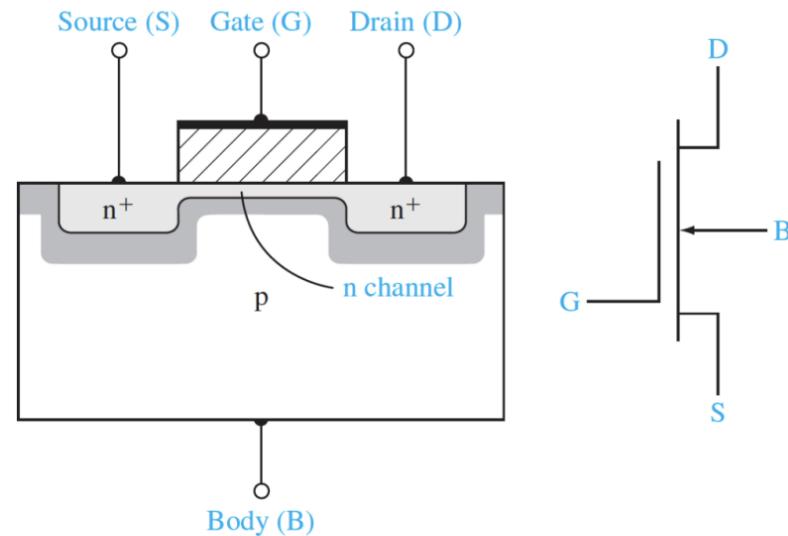
$$\begin{aligned} V_T &= 2\phi_{fp} + t_{ox} \sqrt{\frac{4eN_a\epsilon_{Si}\phi_{fp}}{\epsilon_{ox}^2}} + V_{FB} \\ &= 2\phi_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \end{aligned}$$

10.4 The basic MOSFET operation

MOSFET structures



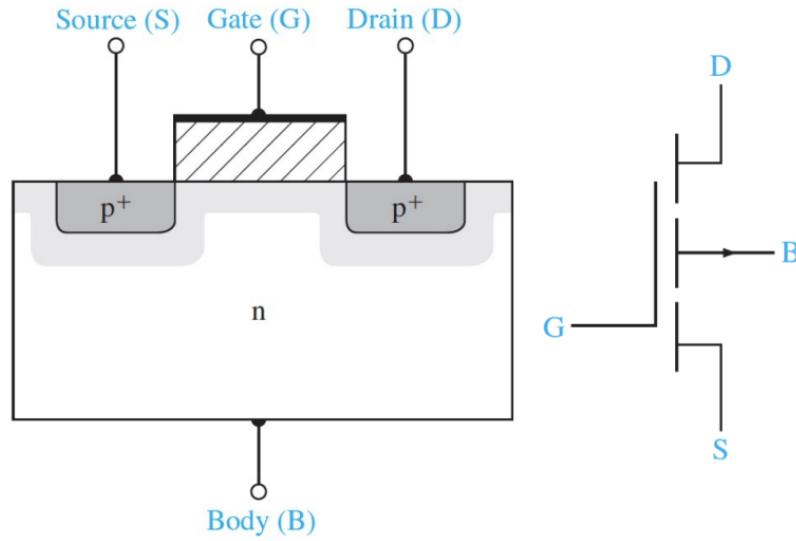
NMOS Enhancement mode



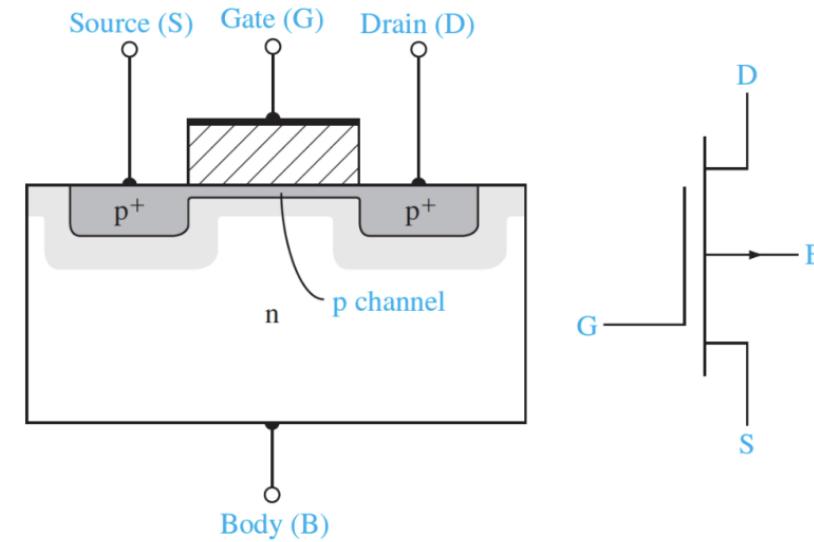
NMOS Depletion mode

10.4 The basic MOSFET operation

MOSFET structures



PMOS Enhancement mode



PMOS Depletion mode

10.4 The basic MOSFET operation

Source and substrate are grounded.

In (a), $V_{GS} < V_T$. There is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero.

In (b), $V_{GS} > V_T$. The drain voltage is small. An electron inversion layer is created. Electrons flow from the source to the drain, so the current direction is from the drain to the source.

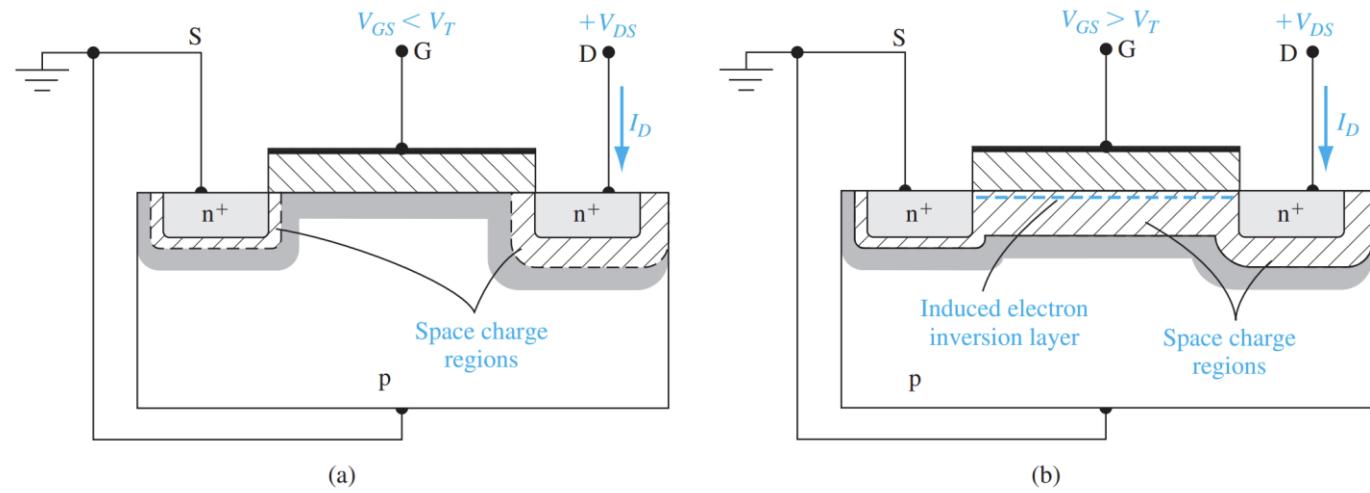


Figure. The n-channel enhancement mode MOSFET (a) with an applied gate voltage $V_{GS} < V_T$ and (b) with an applied gate voltage $V_{GS} > V_T$.

10.4 The basic MOSFET operation

In (a), the thickness of the inversion channel layer qualitatively indicates the relative charge density. It is constant through the entire channel for this case.

In (b), when the drain voltage increases, the voltage drop across the oxide decreases. Thus, the induced inversion charge density decreases.

In (c), the drain voltage continues to increase. It reaches the point when the voltage across the oxide at the drain is exactly V_T . $V_{DS(sat)} = V_{GS} - V_T$.

In (d), $V_{DS} > V_{DS(sat)}$, electrons enter the channel from the source, travel through the channel towards the drain and are swept by the electric field when they reach the point where inversion electron density is zero.

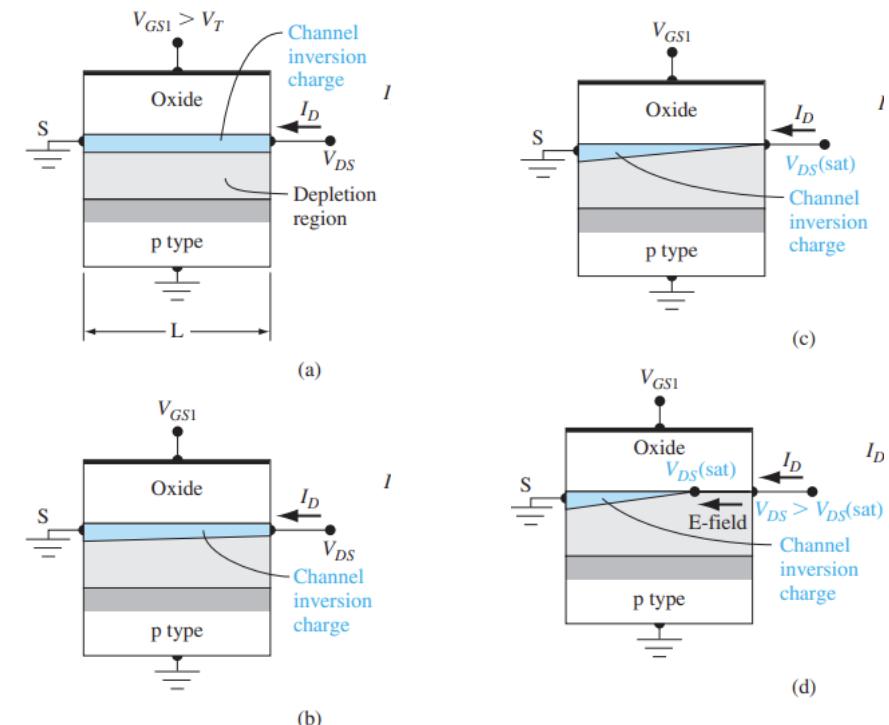


Figure. Cross section when $V_{GS} > V_T$ for (a) a small V_{DS} value; (b) a larger V_{DS} value; (c) a value of $V_{DS} = V_{DS(sat)}$; (d) a value of $V_{DS} > V_{DS(sat)}$

10.4 The basic MOSFET operation

I_D vs. V_{DS} Characteristics

The MOSFET I_D - V_{DS} curve consists of two regions:

1) Resistive or “Triode” Region: $0 < V_{DS} < V_{GS} - V_T$

$$I_D = k'_n \frac{W}{L} \left[V_{GS} - V_T - \frac{V_{DS}}{2} \right] V_{DS}$$

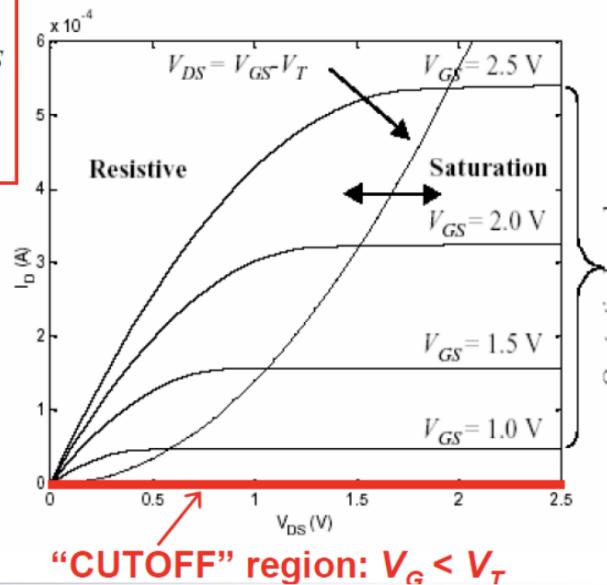
where $k'_n = \mu_n C_{ox}$
process transconductance parameter

2) Saturation Region:

$$V_{DS} > V_{GS} - V_T$$

$$I_{DSAT} = \frac{k'_n}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

where $k'_n = \mu_n C_{ox}$



10.4 The basic MOSFET operation

$$I_D = \frac{W\mu_n C_{\text{ox}}}{L} (V_{GS} - V_T)V_{DS}$$

$$\sqrt{I_D(\text{sat})} = \sqrt{\frac{W\mu_n C_{\text{ox}}}{2L}}(V_{GS} - V_T)$$

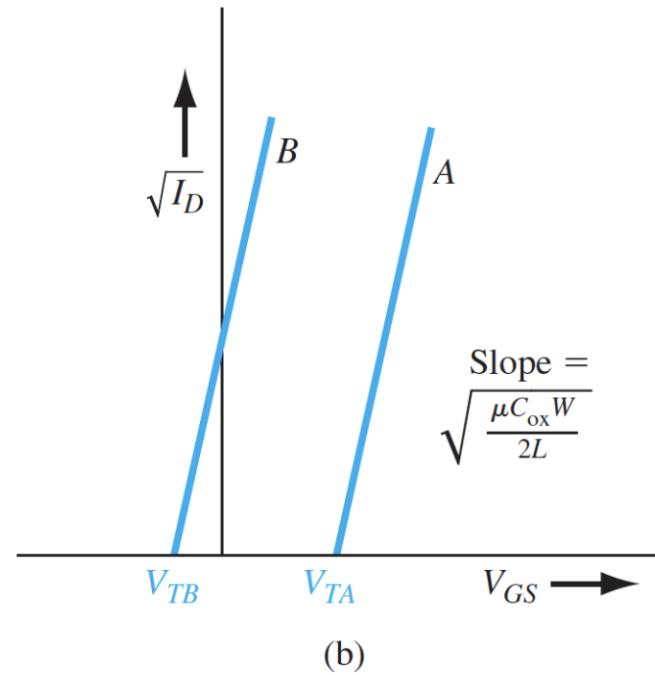
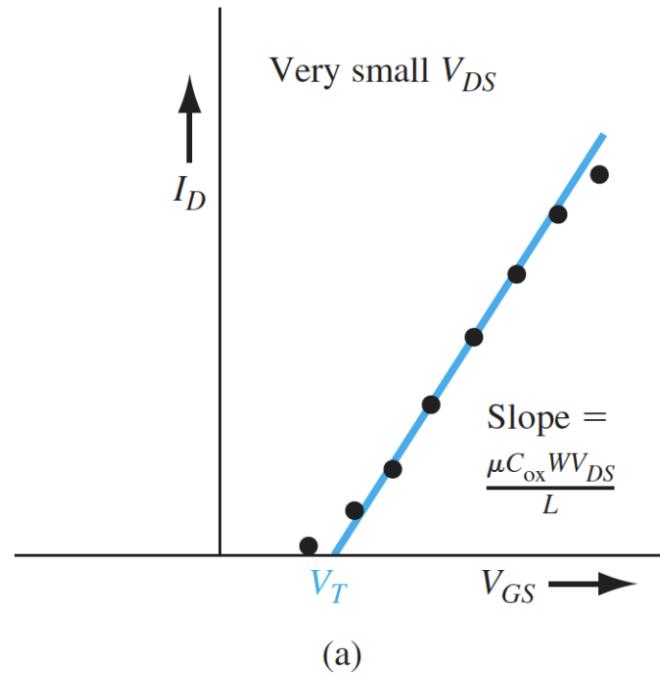
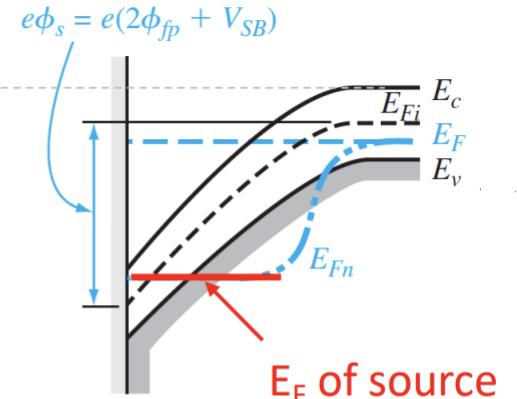
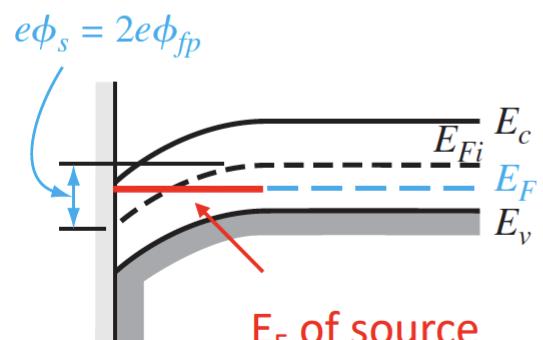
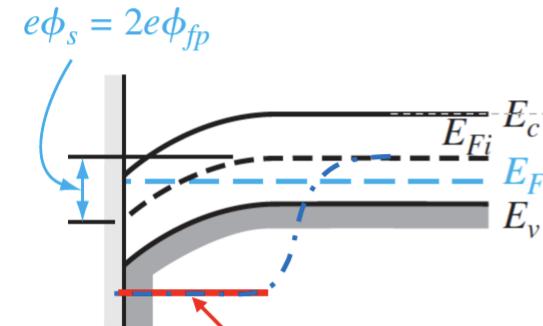
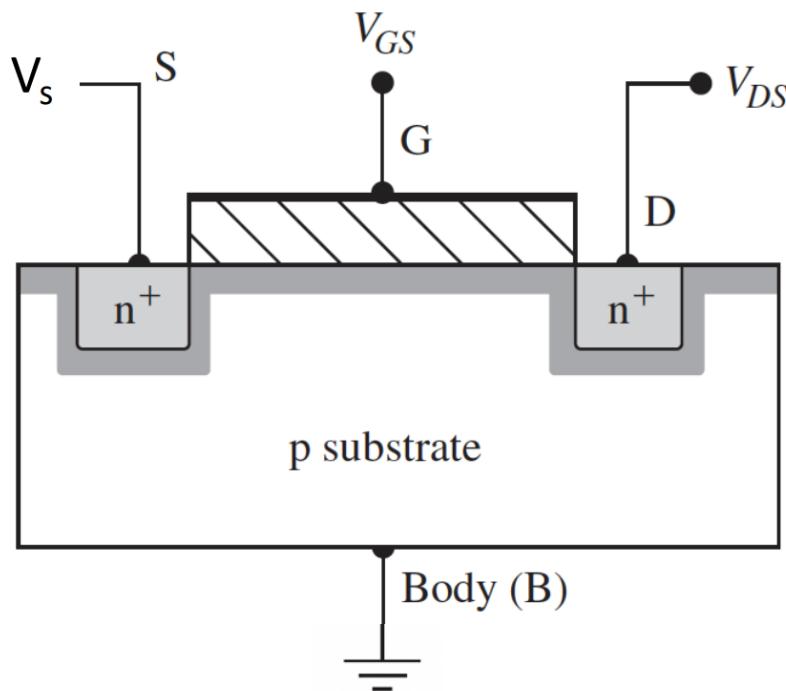


Figure. (a) I_D vs V_{GS} (for small V_{DS}) for enhancement model MOSFET. (b) Ideal $\sqrt{I_D}$ vs V_{GS} in saturation region for enhancement mode (curve A) and depletion mode (curve B) n-channel MOSFET.

10.4 The basic MOSFET operation

Substrate bias effect



10.4 The basic MOSFET operation

When $V_{SB} = 0$, we had

$$Q'_{SD} (\text{max}) = -eN_a x_{dT} = -\sqrt{2e\epsilon_s N_a (2\phi_{fp})}$$

When $V_{SB} > 0$, the space charge width increases and we now have

$$Q'_{SD} = -eN_a x_d = -\sqrt{2e\epsilon_s N_a (2\phi_{fp} + V_{SB})}$$

The change in the space charge density is then

$$\Delta Q'_{SD} = -\sqrt{2e\epsilon_s N_a} [\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}]$$

To reach the threshold condition, the applied gate voltage must be increased. The change in threshold voltage can be written as

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} [\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}]$$

10.4 The basic MOSFET operation

Body effect coefficient

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$$

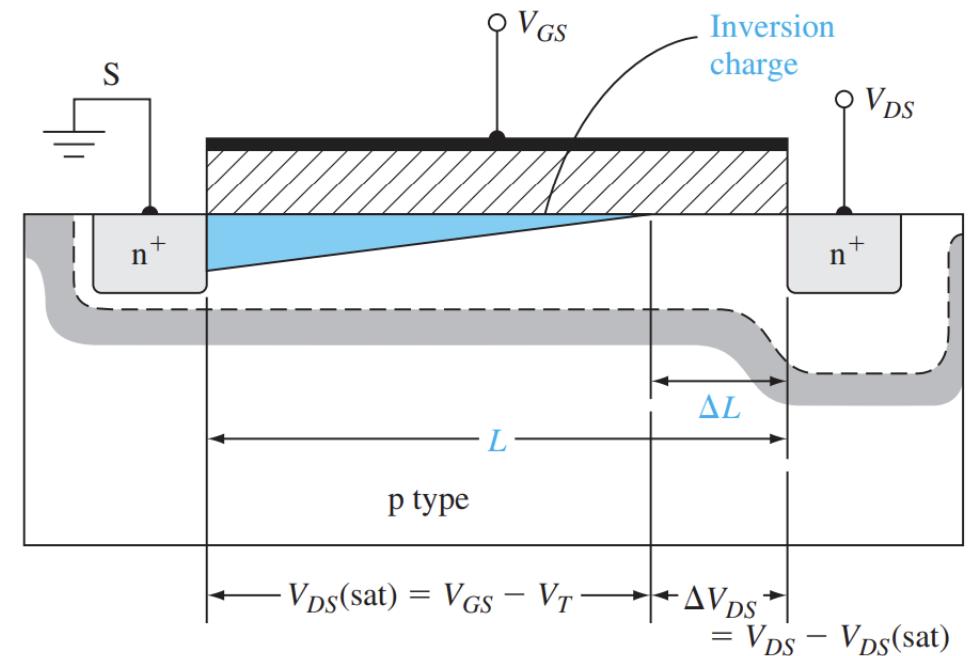
The equation can be rewritten as

$$\Delta V_T = \gamma [\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}]$$

11.1 Channel length modulation

- Assume that the channel length L is a constant
- However, in saturation region, the depletion region at the drain extends into channel
- Thus, the effective channel length is reduced

$$I_D = \begin{cases} 0 & V_{GS} - V_T < 0 \\ \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) & 0 \leq V_{GS} - V_T < V_{DS} \\ \mu_n C_{ox} \frac{W}{L} [(V_{GS} - V_T)V_{DS} - \frac{1}{2} V_{DS}^2] & V_{GS} - V_T \geq V_{DS} \end{cases}$$



11.1 Channel length modulation

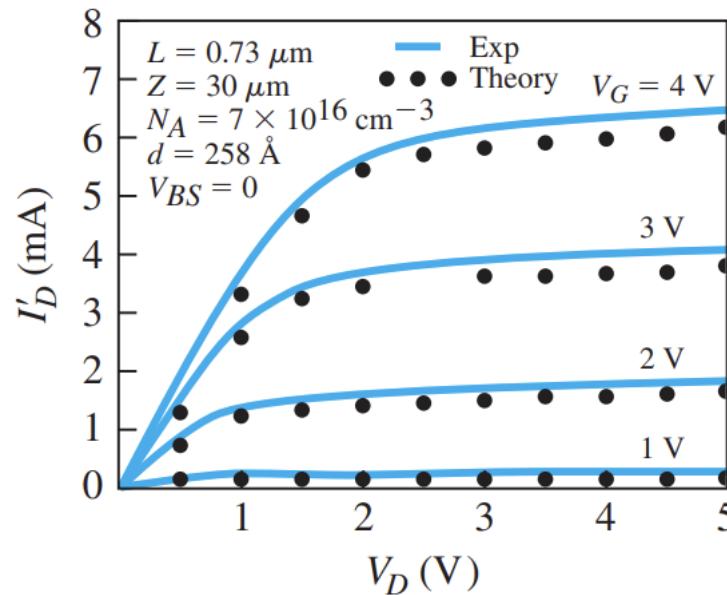


Figure. Current–voltage characteristics of a MOSFET showing short-channel effects.

11.2 Conductance and transconductance

- Transconductance

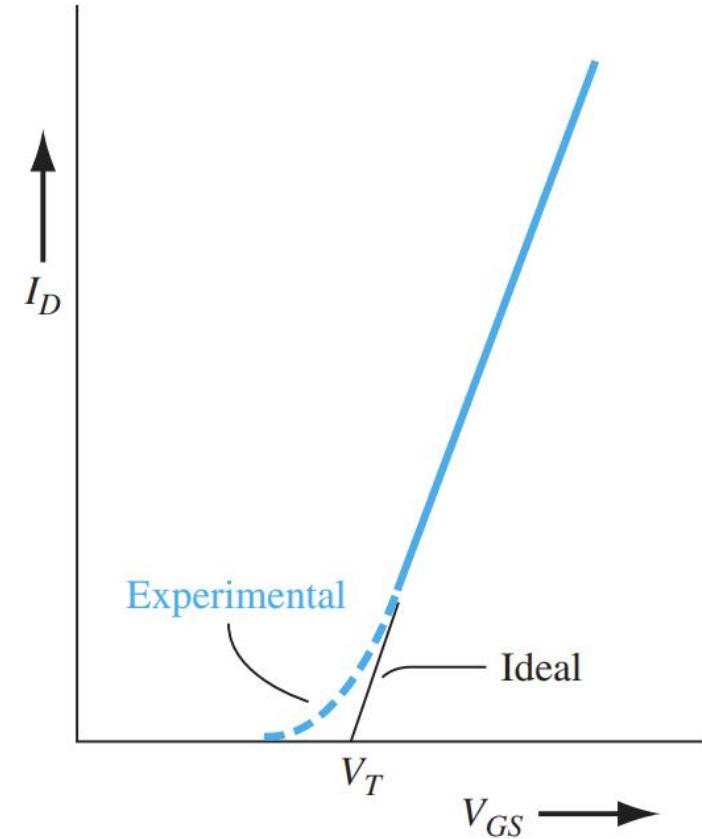
$$g_m = \frac{\partial I_D}{\partial V_{GS}}$$
$$= \begin{cases} \mu_n C_{ox} \frac{W}{L} V_{DS}, & 0 < V_{DS} < V_{GS} - V_T \\ \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T), & V_{DS} > V_{GS} - V_T \end{cases}$$

- Output conductance

$$\bullet g_D = \frac{\partial I_{DS}}{\partial V_{DS}} = \begin{cases} \frac{W}{L} \mu_n C_{ox} (V_{GS} - V_T - V_{DS}) & (0 < V_{DS} < V_{GS} - V_T) \\ 0 & (V_{DS} > V_{GS} - V_T) \end{cases}$$

11.3 Subthreshold conduction

- For NMOS, ideally, we assume drain current to be zero under threshold
- But experimentally, there is threshold current
- Under weak inversion, E_F is closer to E_C at the surface so the surface becomes a lightly-doped n-type material.
- There will be some conduction between source and drain via this weakly inverted channel



11.3 Subthreshold conduction

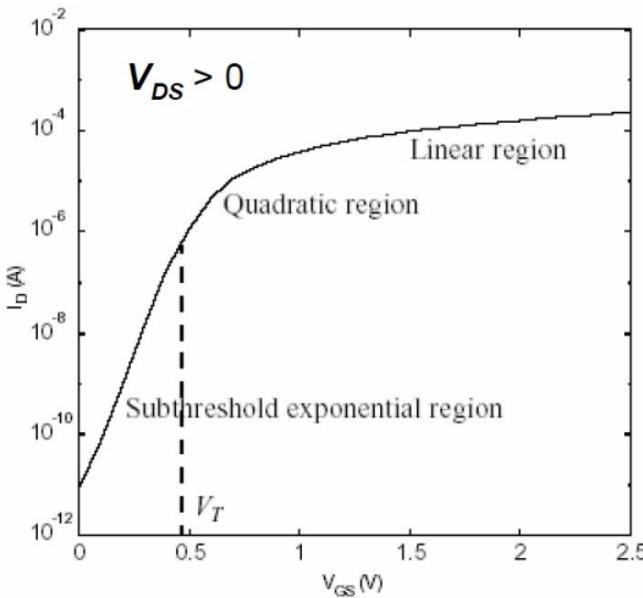
Subthreshold Conduction (Leakage Current)

- The transition from the ON state to the OFF state is gradual. This can be seen more clearly when I_D is plotted on a logarithmic scale:

- In the subthreshold ($V_{GS} < V_T$) region,

$$I_D \propto \exp\left(\frac{qV_{GS}}{nkT}\right)$$

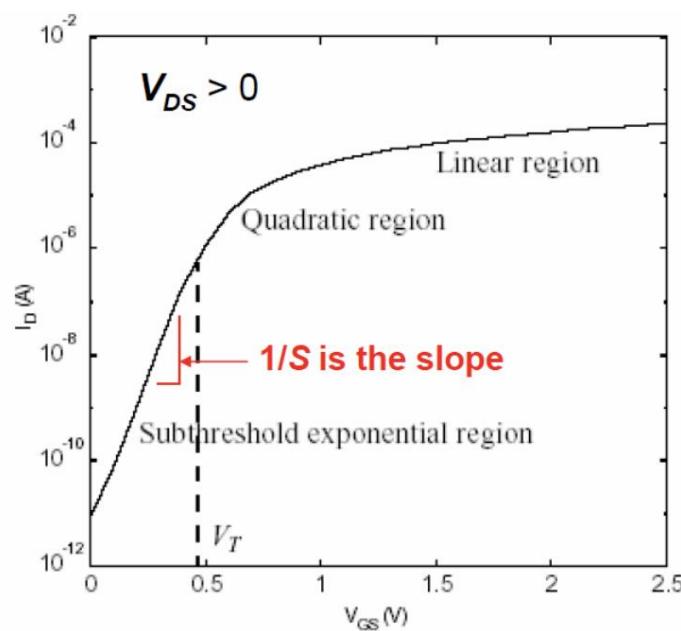
This is essentially the channel-source pn junction current.
(Some electrons diffuse from the source into the channel, if this pn junction is forward biased.)



11.3 Subthreshold conduction

Slope Factor (or Subthreshold Swing) S

- S is defined to be the inverse slope of the log (I_D) vs. V_{GS} characteristic in the subthreshold region:



$$S \equiv n \left(\frac{kT}{q} \right) \ln(10)$$

Units: Volts per decade

Note that $S \geq 60$ mV/dec
at room temperature:

$$\left(\frac{kT}{q} \right) \ln(10) = 60 \text{ mV}$$

11.4 Velocity saturation

$$v_d \rightarrow v_{th}$$

As the transistor size scales down,
the electric field intensity E increases.

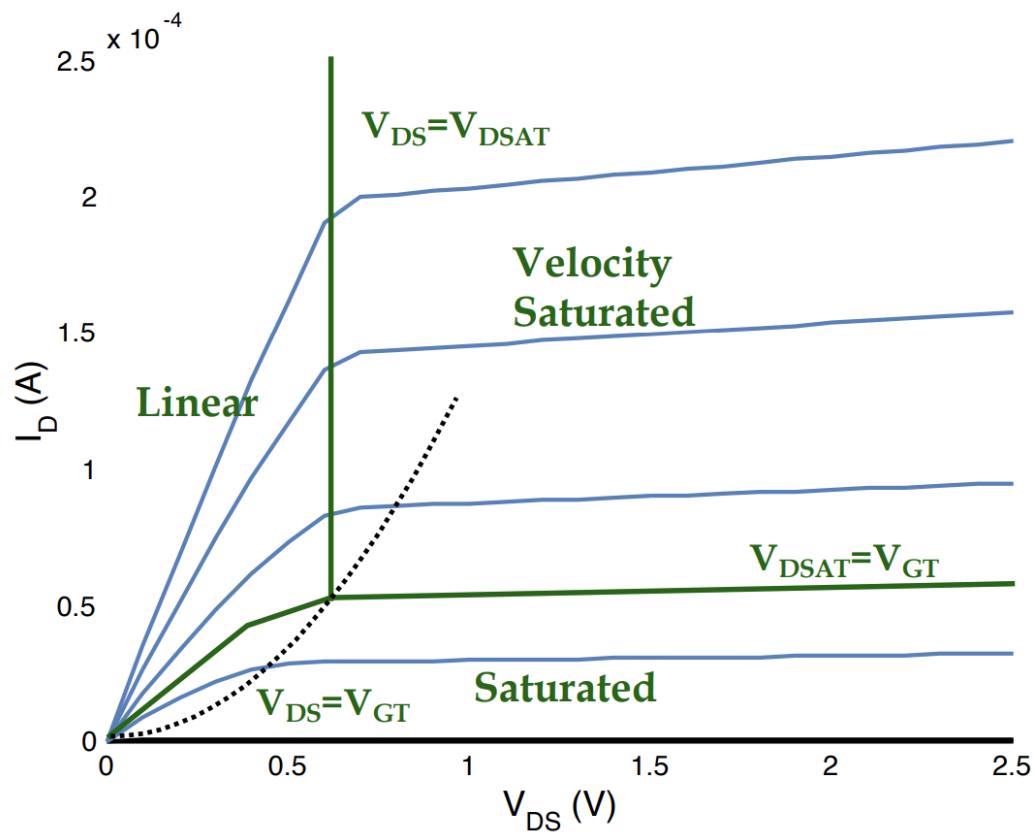
- Electric field is heating up electrons
- Electrons transfer energy to lattice to reach thermal equilibrium

$$\begin{aligned} I_{DSAT} &= \mu_n C_{ox} \frac{W}{L} \left(V_{GS} - VT - \frac{1}{2} V_{DS} \right) V_{DS} \\ &= C_{ox} W \left(V_{GS} - VT - \frac{1}{2} V_{DSAT} \right) \frac{V_{DSAT}}{L} \mu_n \end{aligned}$$

$$I_{DSAT} = WC_{ox} \left[V_{GS} - V_T - \frac{V_{DSAT}}{2} \right] v_{sat}$$

$$\text{where } V_{DSAT} = \frac{L}{\mu_n} v_{sat}$$

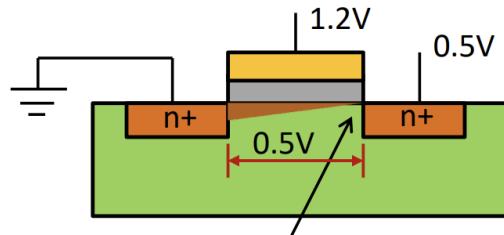
11.4 Velocity saturation



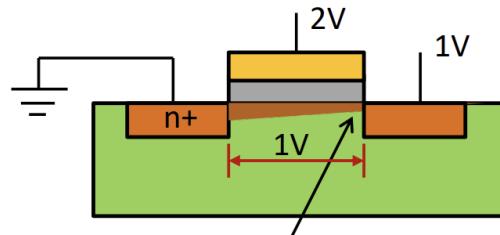
11.4 Velocity saturation

Example

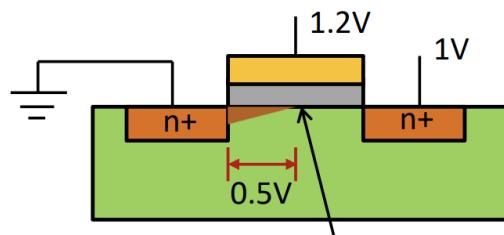
$$V_T = 0.7, \quad V_{gs} = 1.2 \text{ V}, \quad V_{sat} = 1 \text{ V}$$



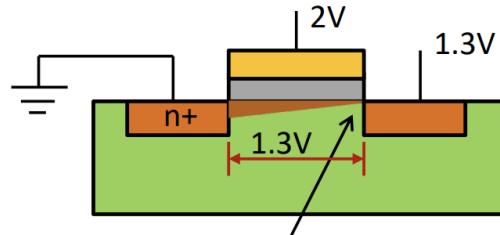
Start to pinch off



- NO pinch off
- Velocity saturation starts

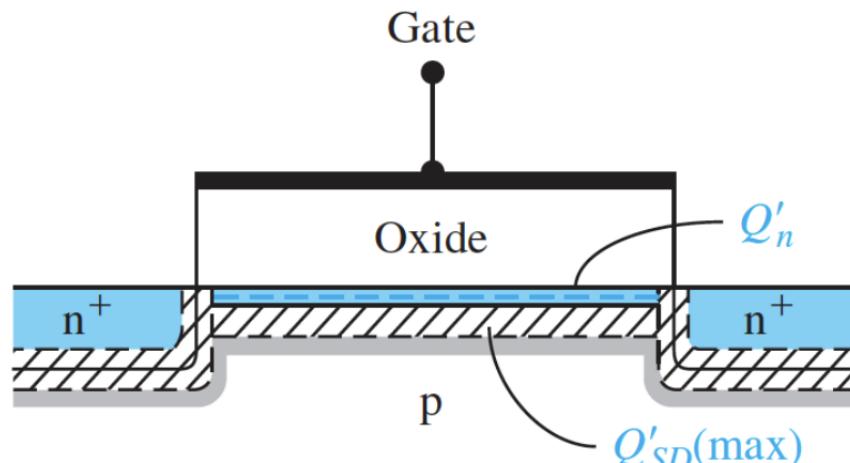


Start to pinch off

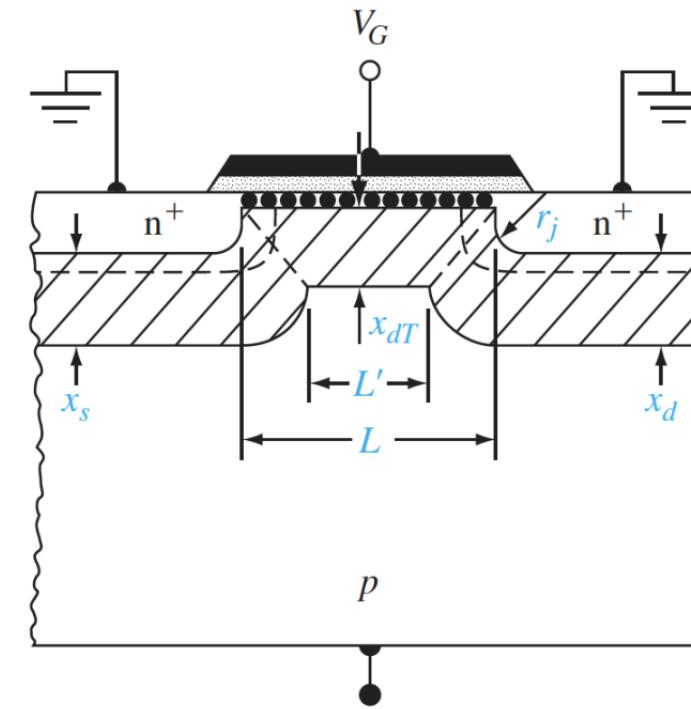


- Starts to pinch off
- Velocity saturation

11.5 Short channel effect



A long channel device



A short channel device

11.5 Short channel effect

- In long channel devices, the depletion regions of source and drain are very small parts of the entire channel.
- In short channel devices, the depletion regions of source and drain reduces the channel length effectively.

Important Notes!

11.4 Velocity Saturation

Unified model

$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) \quad \text{for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$,

$$V_{GT} = V_{GS} - V_T,$$

$$\text{and } V_T = V_{T0} + \gamma (\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

The formula in chapter 11.4 is wrong!!! Here, V_{sb} should be V_{bs} !!!

I suggest that you should use the formula in chapter 10.

Use this one:

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}} [\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}]$$

Important Notes!

Be aware that most of the formulas derived in the lectures are for NMOS!!!