

RC 7

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9.1 The Schottky Barrier Diode

Work function (Φ): energy difference between the vacuum energy level and the Fermi level (depend on doping concentration, not an intrinsic characteristic)

Electron affinity: energy difference between the vacuum energy level and conduction band bottom edge

(Note: here, the notation 'm' means metal and 's' means semiconductor)

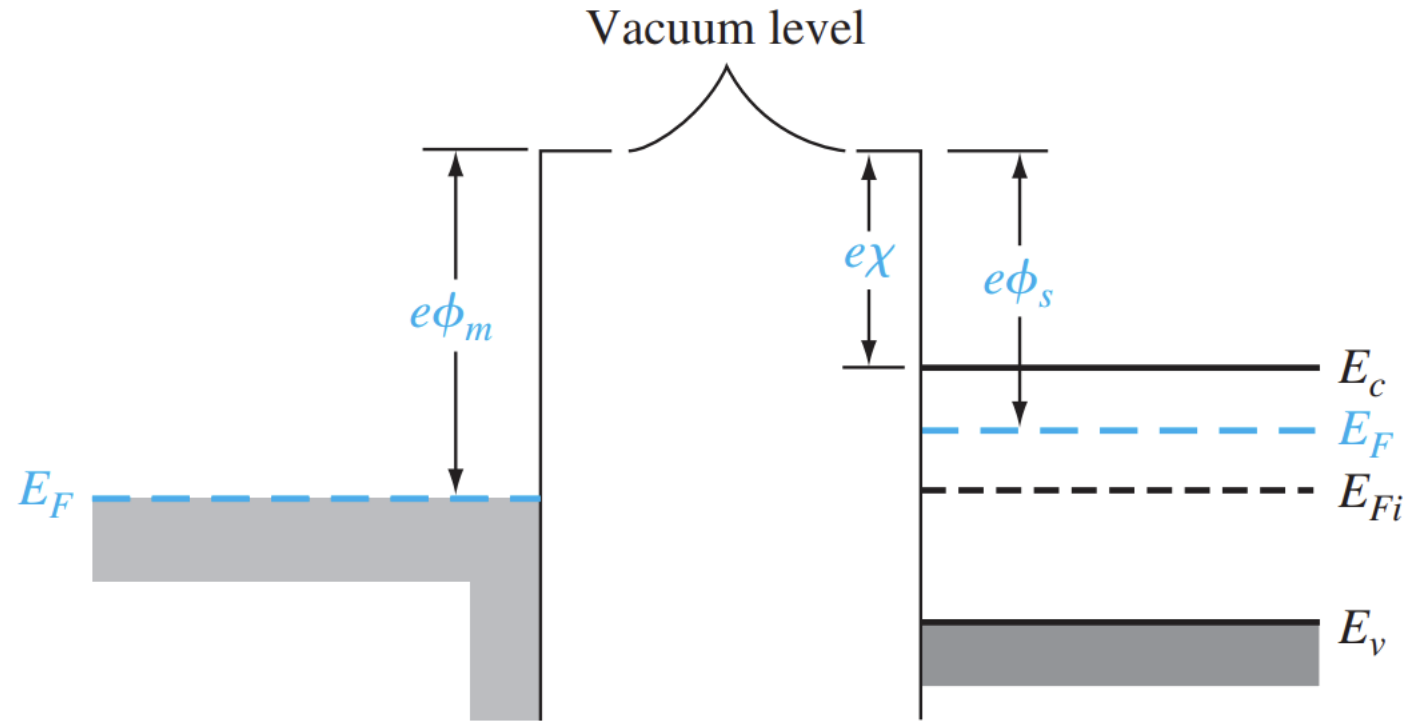


Figure. Energy-band diagram of a metal and semiconductor before contact

9.1 The Schottky Barrier Diode

The parameter ϕ_{B0} is the ideal barrier height of the semiconductor contact, the potential barrier seen by electrons in the metal trying to move into the semiconductor. This barrier is known as the *Schottky barrier* and is given, ideally, by

$$\phi_{B0} = (\phi_m - \chi)$$

On the semiconductor side, V_{bi} is the built-in potential barrier. This barrier, similar to the case of the pn junction, is the barrier seen by electrons in the conduction band trying to move into the metal. The built-in potential barrier is given by

$$V_{bi} = \phi_{B0} - \phi_n$$

which makes V_{bi} a slight function of the semiconductor doping, as is the case in a pn junction.

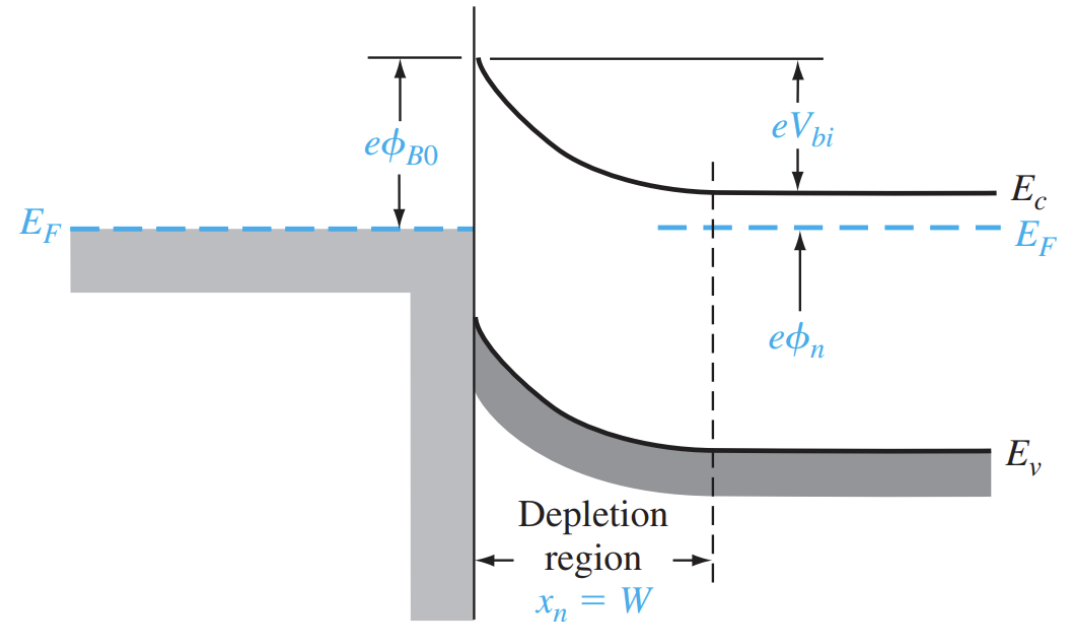


Figure. Ideal energy-band diagram of a metal-n-semiconductor for $\Phi_m > \Phi_s$

9.1 The Schottky Barrier Diode

How to draw the energy-band diagram?

- First, draw the metal and semiconductor part separately.
- Then, in thermal equilibrium, the fermi energy level should be flat. Align the fermi levels in the metal and semiconductor. You may have to bend the conduction and valence band in the semiconductor.

9.1 The Schottky Barrier Diode

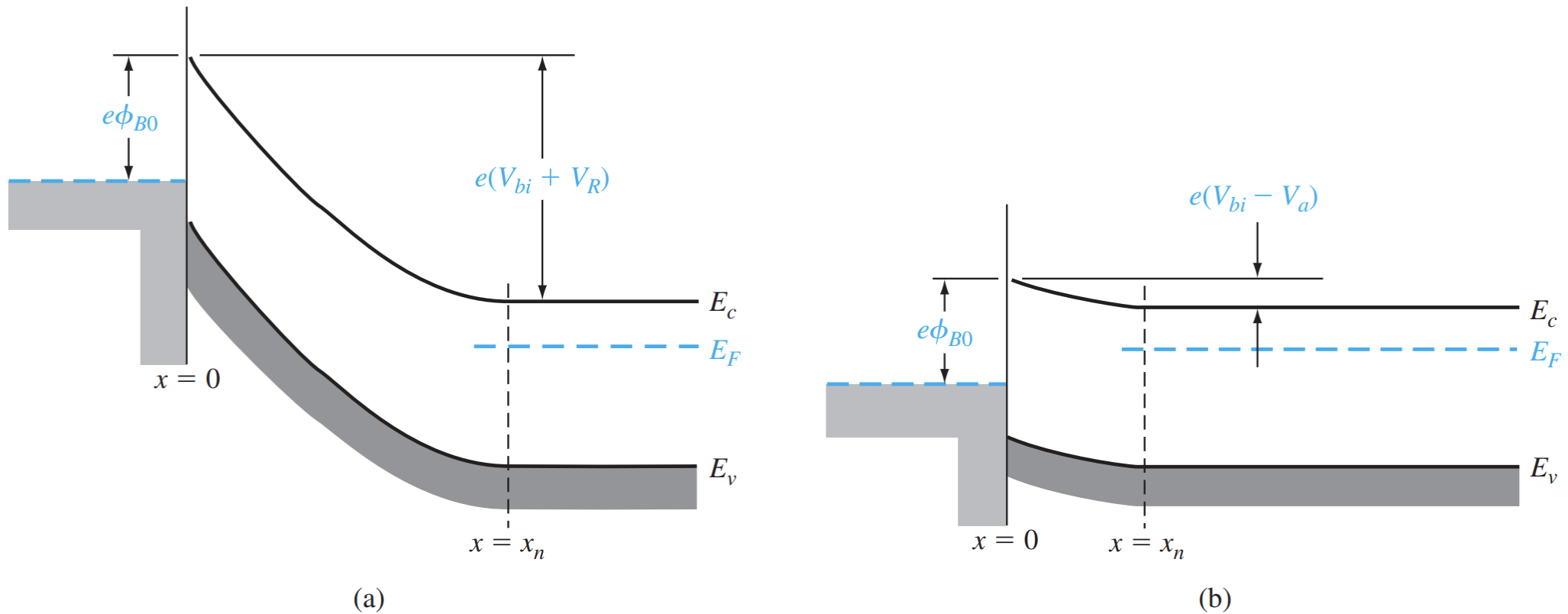


Figure. Ideal energy-band diagram of a metal–semiconductor junction (a) under reverse bias and (b) under forward bias.

9.1 The Schottky Barrier Diode

Ideal Junction Properties

- Electric Field:

$$E = -\frac{eN_d}{\epsilon_s}(x_n - x)$$

- Space Charge Region Width:

$$W = x_n = \left[\frac{2\epsilon_s(V_{bi} + V_R)}{eN_d} \right]^{1/2}$$

(The results are similar to the one-sided p+n junction.)

9.1 The Schottky Barrier Diode

Junction Capacitance

$$C' = eN_d \frac{dx_n}{dV_R} = \left[\frac{e\epsilon_s N_d}{2(V_{bi} + V_R)} \right]^{1/2}$$

$$\left(\frac{1}{C'} \right)^2 = \frac{2(V_{bi} + V_R)}{e\epsilon_s N_d}$$

Here, C' is the capacitance per unit area. V_{bi} is the intersection of the line and the X-axis. The slope can be used to derive the doping concentration N_d .

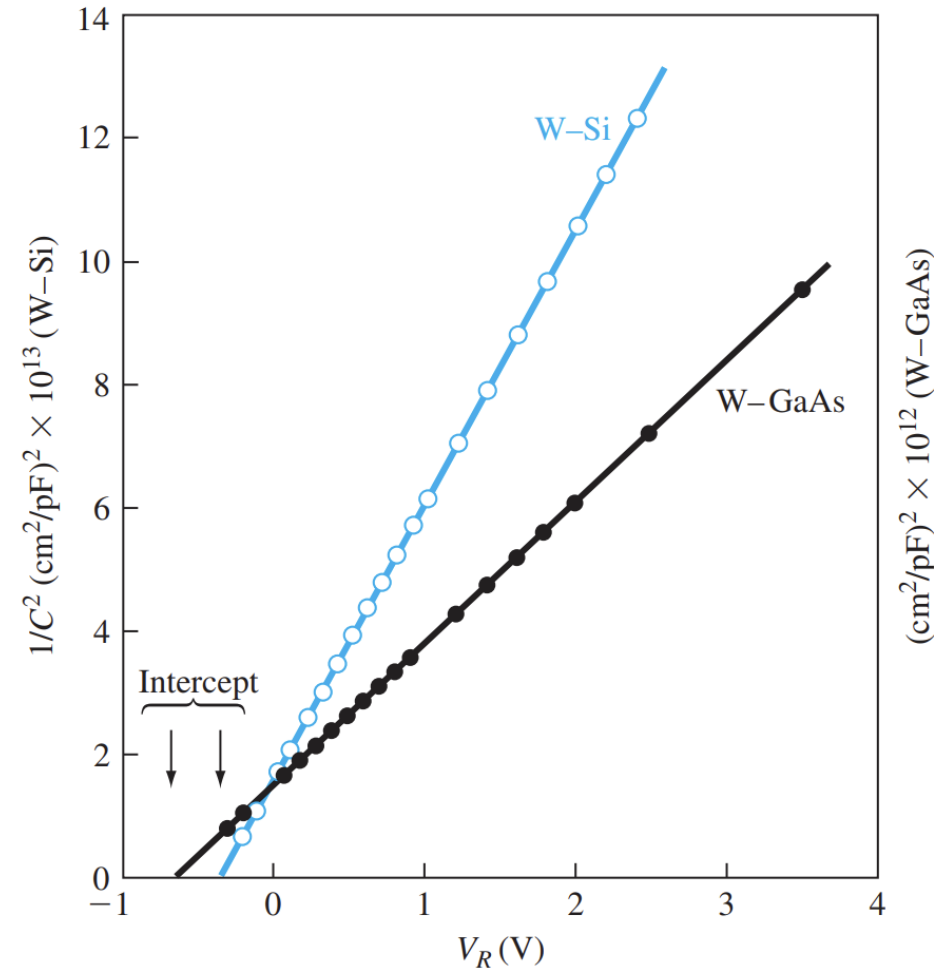


Figure. $1/C'^2$ vs V_R

9.1 The Schottky Barrier Diode

- Current voltage relationship

$$J = J_{sT} \left[\exp \left(\frac{eV_a}{kT} \right) - 1 \right]$$

- Reverse saturation current density

$$J_{sT} = A^* T^2 \exp \left(\frac{-e\phi_{Bn}}{kT} \right)$$

- Richardson constant

$$A^* \equiv \frac{4\pi e m_n^* k^2}{h^3}$$

9.1 The Schottky Barrier Diode

Two differences between a Schottky diode and a pn junction diode

- Reverse current densities

$J_{st} \gg J_s$

$$J_{sT} = A^* T^2 \exp\left(\frac{-e\phi_{Bn}}{kT}\right)$$

$$J_s = \frac{eD_n n_{po}}{L_n} + \frac{eD_p p_{no}}{L_p}$$

The current in a pn junction is determined by the diffusion of minority carriers while the current in a Schottky barrier diode is determined by thermionic emission of majority carriers over a potential barrier.

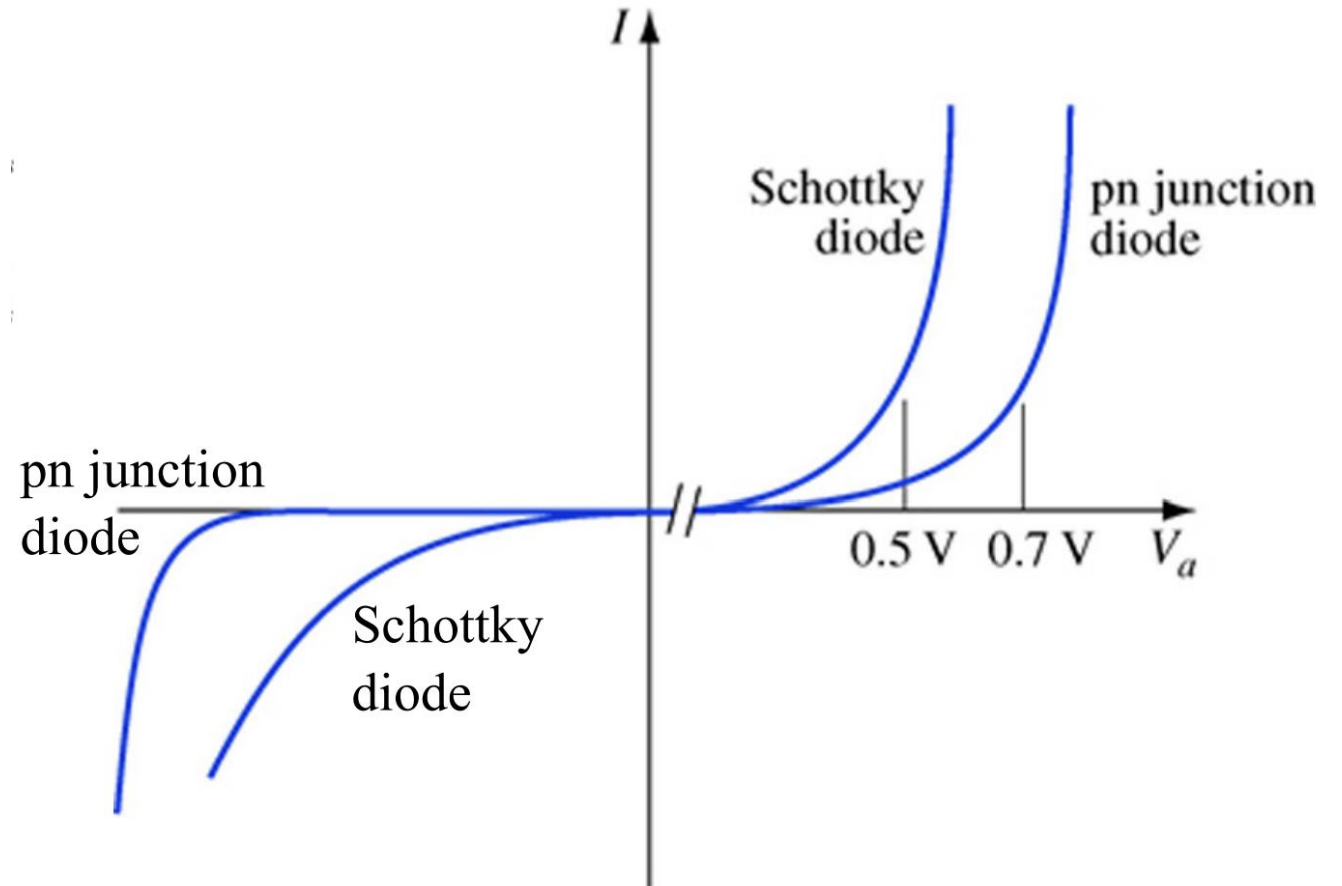


Figure. I-V characteristic plot of Schottky diode and pn junction

9.1 The Schottky Barrier Diode

Two differences between a Schottky diode and a pn junction diode (cont.)

- Switching characteristics

The second major difference between a Schottky barrier diode and a pn junction diode is **in the frequency response**, or **switching characteristics**. In our discussion, we have considered the current in a Schottky diode as being due to the injection of majority carriers over a potential barrier. The energy-band diagram of Figure 9.1, for example, shows that there can be electrons in the metal directly adjacent to empty states in the semiconductor. If an electron from the valence band of the semiconductor were to flow into the metal, this effect would be equivalent to holes being injected into the semiconductor. This injection of holes would create excess minority carrier holes in the n region. However, calculations as well as measurements have shown that the ratio of the minority carrier hole current to the total current is extremely low in most cases.

The Schottky barrier diode, then, is **a majority carrier device**. This fact means that there is **no diffusion capacitance** associated with a **forward-biased** Schottky diode. The elimination of the diffusion capacitance makes the Schottky diode **a higher-frequency device than the pn junction diode**. Also, when switching a Schottky diode from forward to reverse bias, there is **no minority carrier stored charge to remove**, as is the case in the pn junction diode. Since there is no minority carrier storage time, the Schottky diodes can be used in **fast-switching applications**. A typical switching time for a Schottky diode is in the picosecond range, while for a pn junction it is normally in the nanosecond range.

9.2 Metal Semiconductor Ohmic contacts

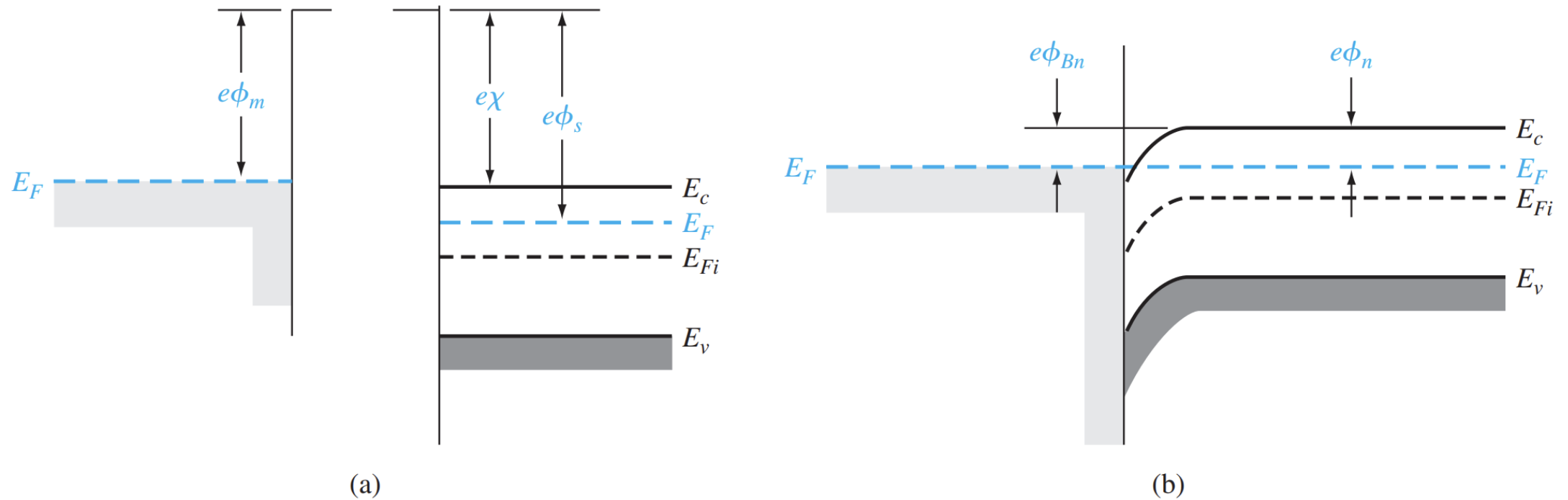


Figure. Ideal energy-band diagram (a) before contact and (b) after contact for a metal-n-type semiconductor junction for $\Phi_m < \Phi_s$

9.2 Metal Semiconductor Ohmic contacts

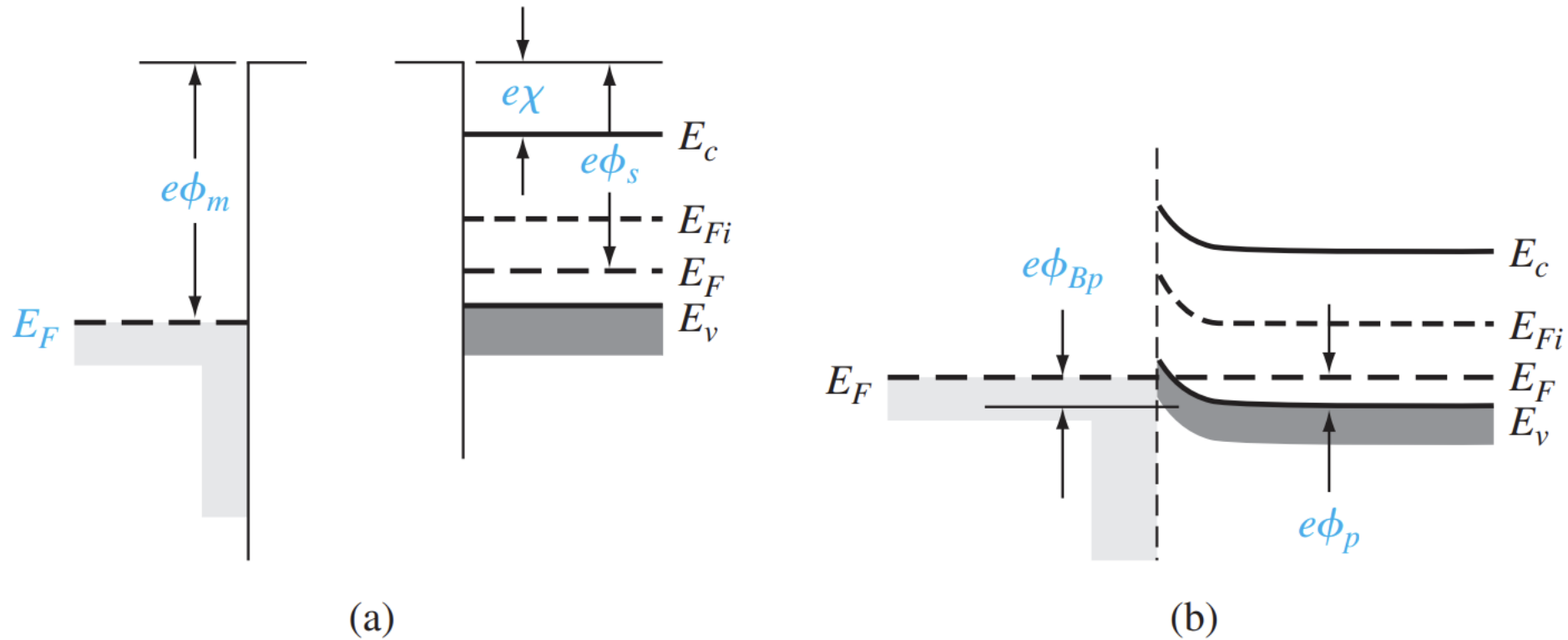
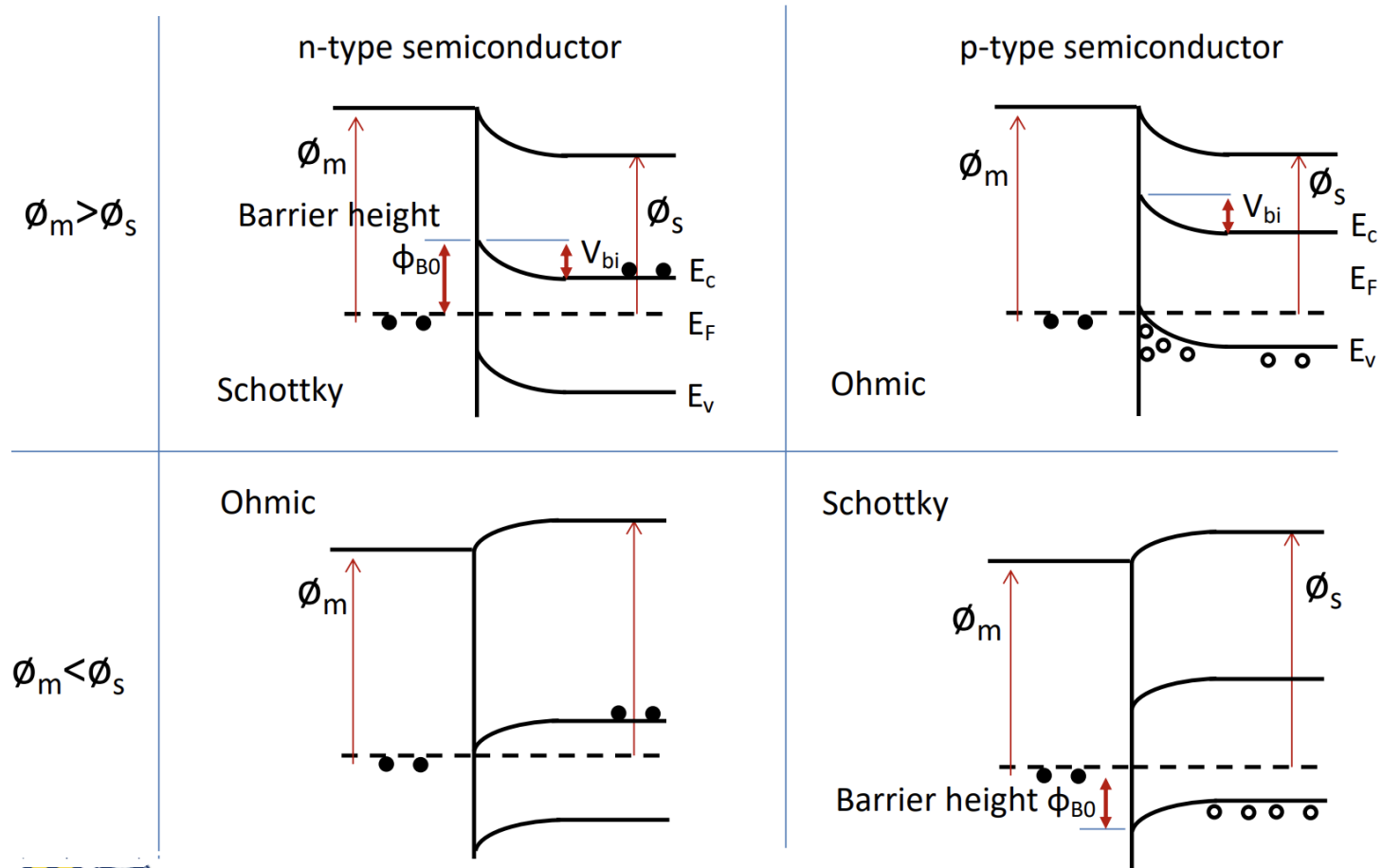


Figure. Ideal energy-band diagram (a) before contact and (b) after contact for a metal-p-type semiconductor junction for $\Phi_m > \Phi_s$

9.2 Metal Semiconductor Ohmic contacts



10.1 The two-terminal MOS structure

MOSFET:

- M: Metal
- O: Oxide
- S: Semiconductor
- F: Field
- E: Effect
- T: Transistor

(Voltage controlled device)

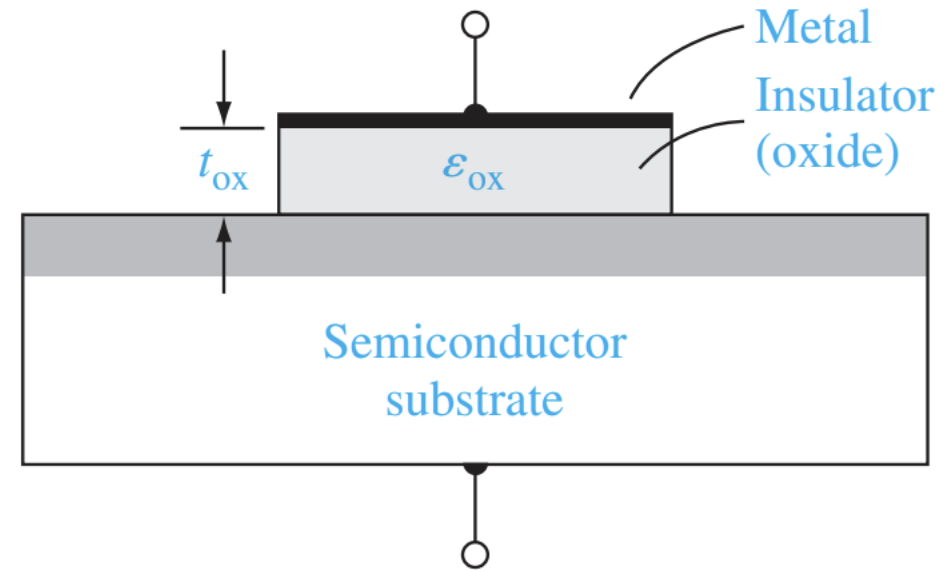


Figure. Basic MOS structure

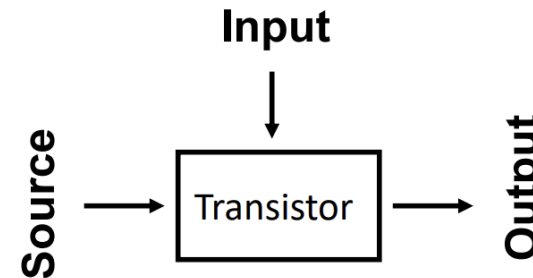
10.1 The two-terminal MOS structure

tran•sis•tor (trán-zìs' ter)

A solid-state electronic device that is used to control the flow of electricity in electronic equipment and consists of a small block of a semiconductor with at least three electrodes

Trans(fer) + (res)istor

Idea: control large output
with small input



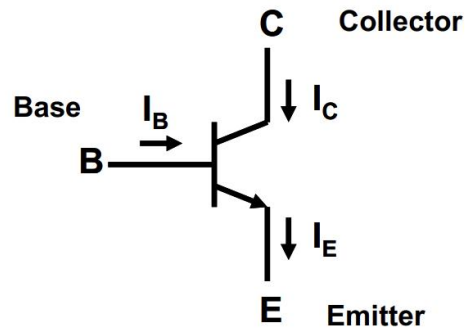
This device should exhibit gain

10.1 The two-terminal MOS structure

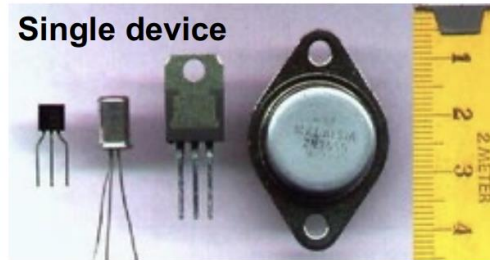
In general, there are two types of transistors

Bipolar (BJT)

A three terminal device in which emitter to collector current is controlled by base current

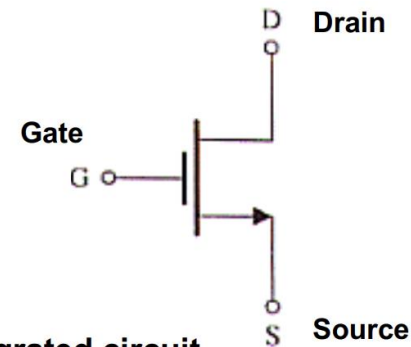


Single device

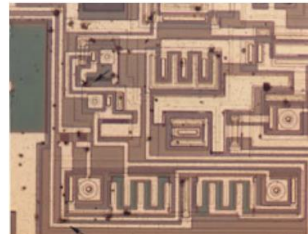


Field-effect (FET)

A transistor in which the output current is controlled by a variable electric field (gate voltage)



Integrated circuit



10.1 The two-terminal MOS structure

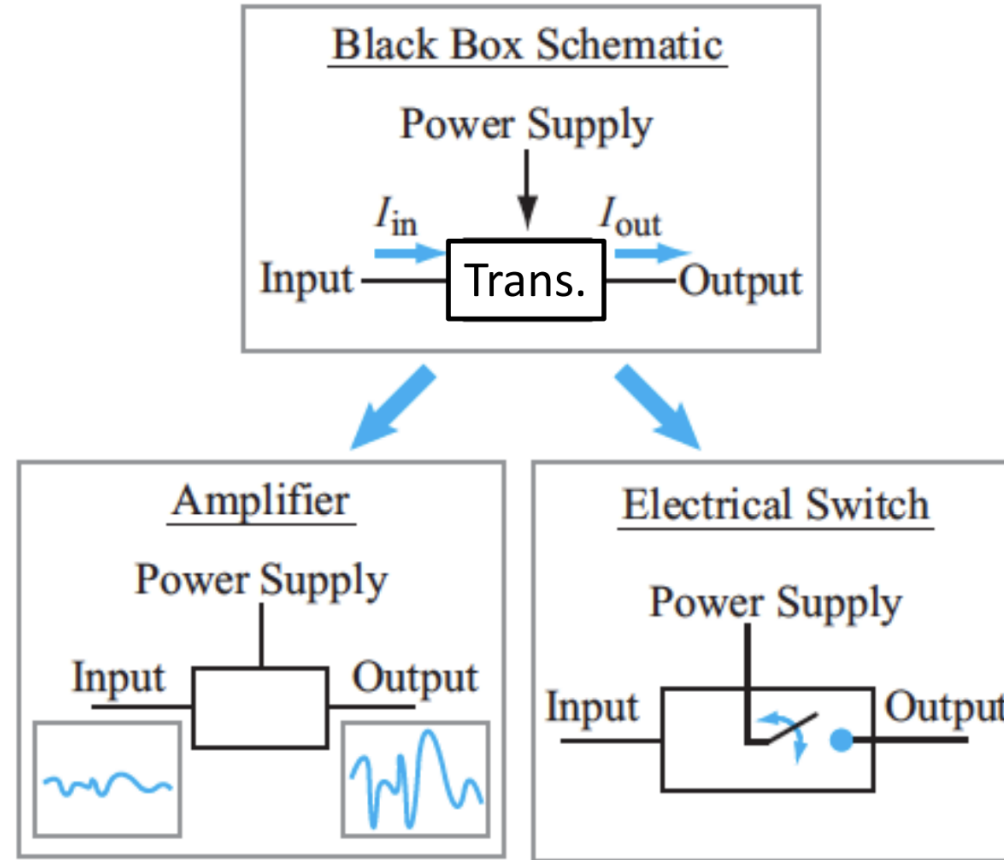


Figure. Applications of MOSFET

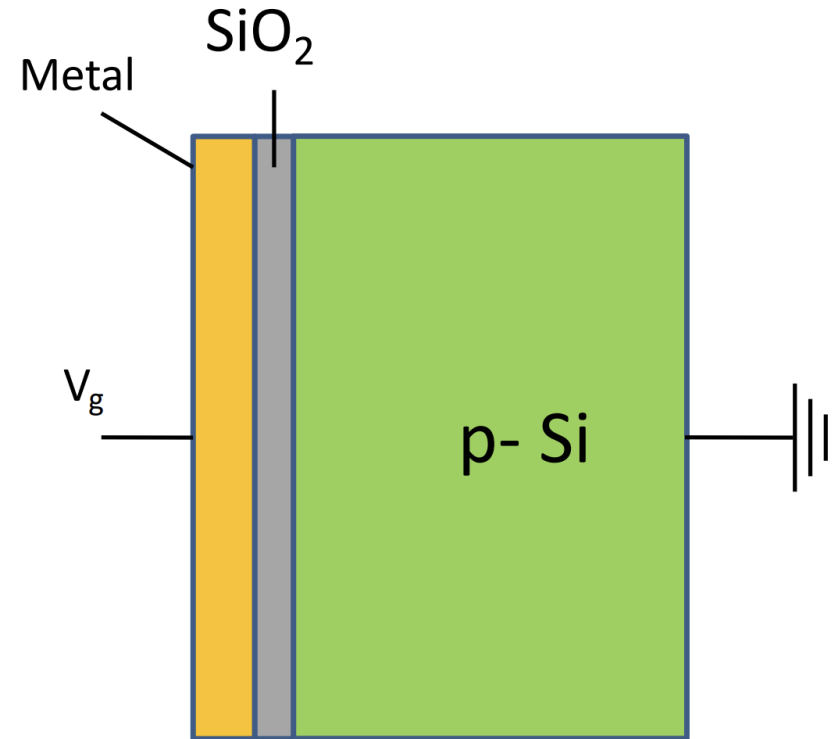
10.1 The two-terminal MOS structure

Take p-type semiconductor as an example:

V_g is the gate voltage, which is applied on the metal side.

The semiconductor side is usually grounded.

The MOS capacitor model is different from the Schottky diode model since it has an oxide layer between the metal and semiconductor.



Metal-insulator-semiconductor (MIS)

10.1 The two-terminal MOS structure

Some Important Terminologies:

- Surface potential (difference between the intrinsic fermi level of the bulk and surface):

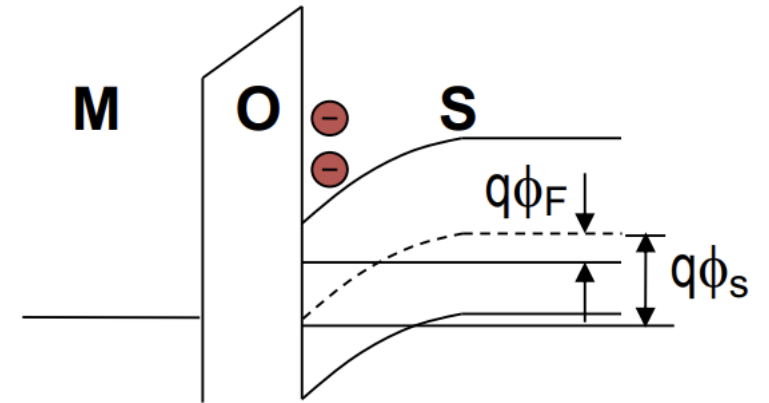
$$\phi_s = \frac{1}{q} [E_i(bulk) - E_i(surface)]$$

- Potential difference (between fermi level and intrinsic fermi level):

$$\phi_{fp} = V_t \ln \left(\frac{N_a}{n_i} \right) \quad \phi_{fn} = V_t \ln \left(\frac{N_d}{n_i} \right)$$

- Space charge width:

$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a} \right)^{1/2}$$



10.1 The two-terminal MOS structure

$V_g < 0$ (Accumulation Mode)

Negative charges will exist on the metal plate due to the negative applied voltage

An electric field will then be induced

This induced electric field will make the holes in semiconductor move towards the oxide-semiconductor interface

Positive charges are accumulated at the interface, so this is called the accumulation mode

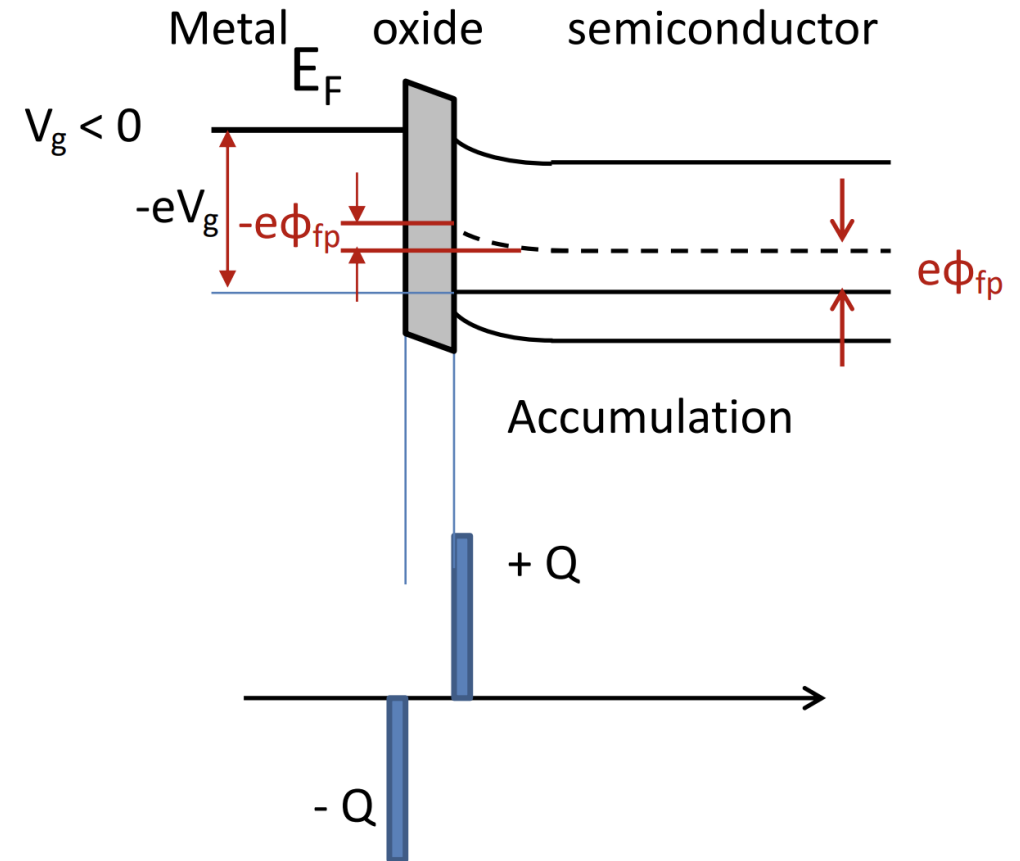


Figure. Energy-band diagram and charge distribution in accumulation mode

10.1 The two-terminal MOS structure

$V_g > 0$ (Depletion Mode)

Positive charges exist on the metal plate

The induced electric field is reversed

Holes in the semiconductor are pushed away from the interface

A negative space charge region is created

Thus, this is called the depletion mode

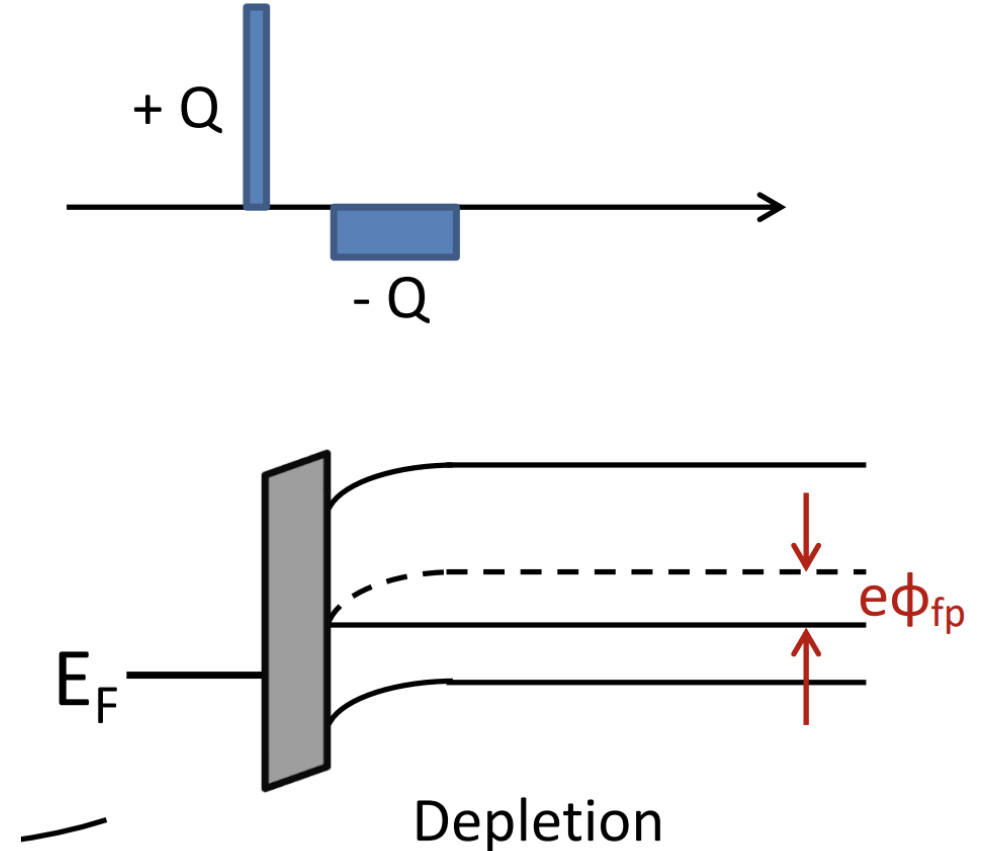


Figure. Energy-band diagram and charge distribution in the depletion mode

10.1 The two-terminal MOS structure

$V_g > 0$ (Weak Inversion)

The induced electric field still increases

The larger negative charge in MOS capacitor implies a larger induced space charge region and more band bending

The intrinsic fermi level at the surface is below the fermi level

The surface close to the interface turns into n-type!

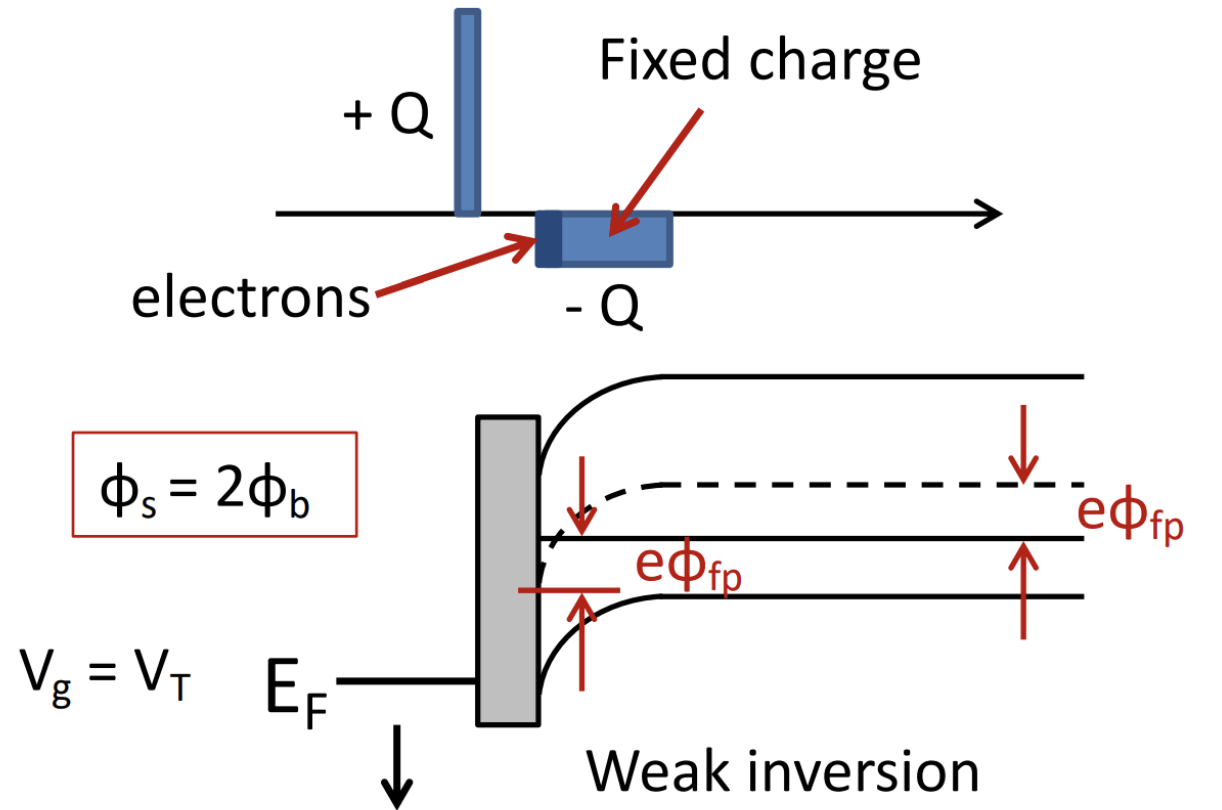


Figure. Energy-band diagram and charge distribution in the weak inversion mode

10.1 The two-terminal MOS structure

$V_g = V_t$ ($\Phi_s = 2 \Phi_f$) Threshold

The electron concentration at the surface is the same as the hole concentration in the bulk material.

If $V_g > V_t$, the conduction band will bend slightly closer to the Fermi level, but the change in the conduction band at the surface is now only a slight function of gate voltage. The electron concentration at the surface, however, is an exponential function of the surface potential. The surface potential may increase by a few (kT/e) volts, which will change the electron concentration by orders of magnitude, but the space charge width changes only slightly. In this case, then, the space charge region has essentially reached a maximum width.

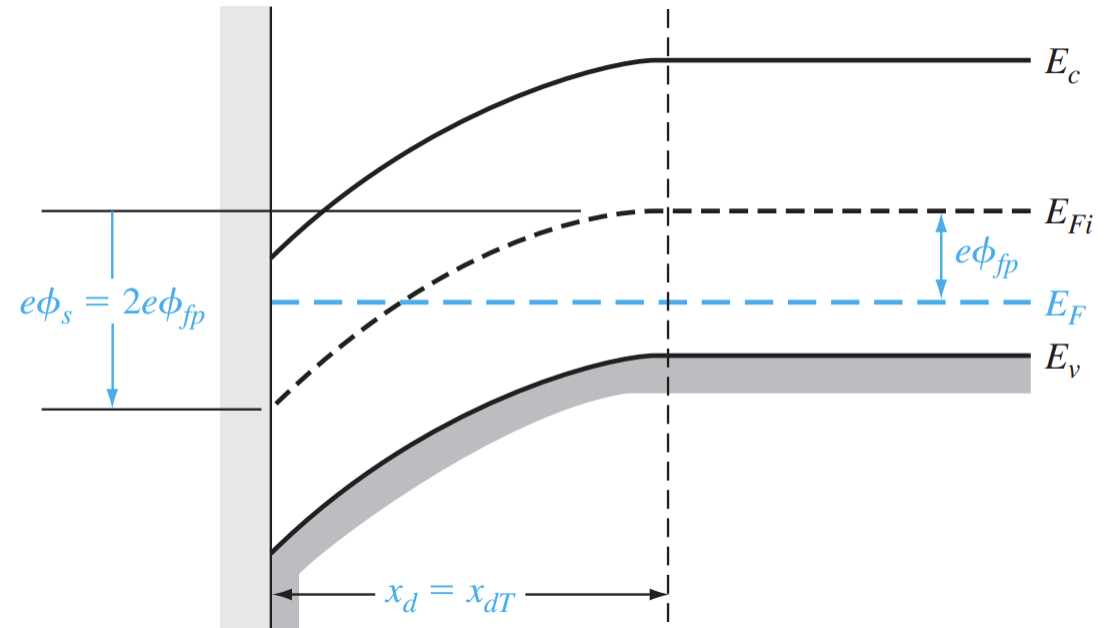


Figure. Energy-band diagram under the threshold voltage

10.1 The two-terminal MOS structure

- Space charge region width

$$x_d = \left(\frac{2\epsilon_s \phi_s}{eN_a} \right)^{1/2}$$

- Maximum depletion width:

Since threshold inversion point is $\phi_s = 2\phi_F$

Then, maximum depletion layer is

$$x_{dT} = \left(\frac{4\epsilon_s \phi_{fp}}{eN_a} \right)^{1/2}$$

10.1 The two-terminal MOS structure

$V_g > V_t$ (Strong Inversion)

The electron concentration at the surface is greater than the hole concentration in the bulk material

So, this is called strong inversion

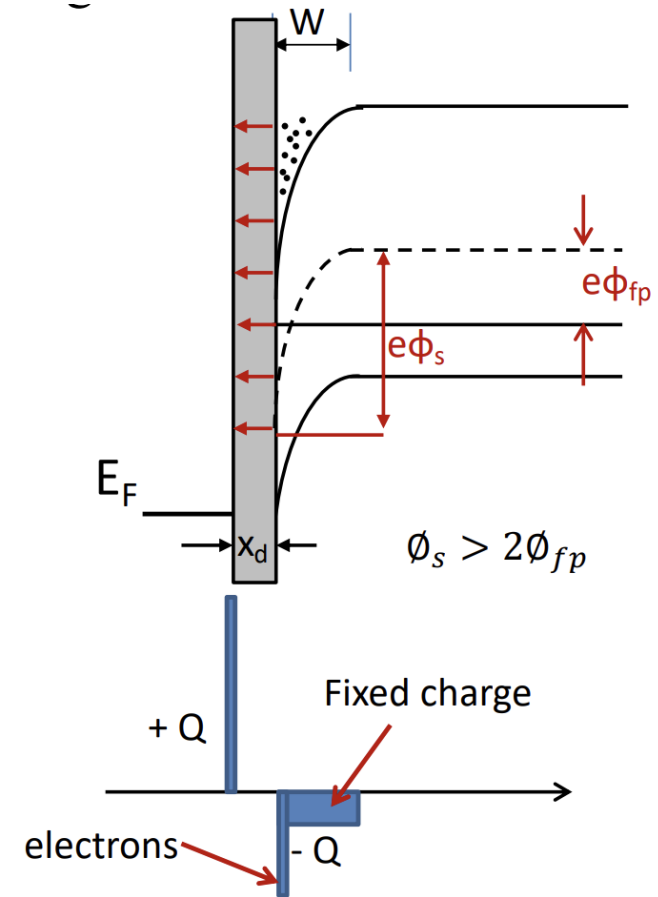


Figure. Energy-band diagram and charge distribution

Thanks!