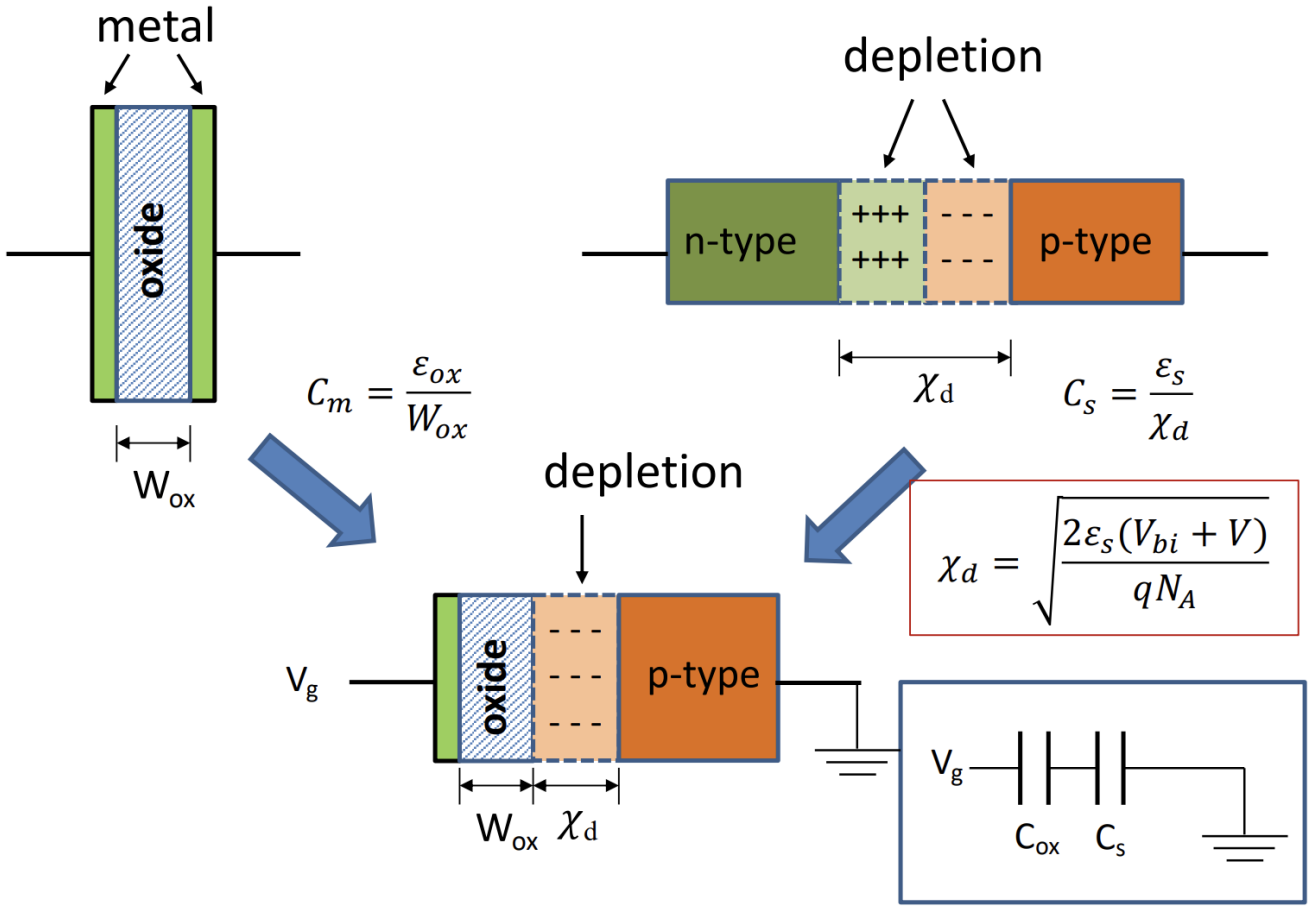
RC8

Contents

10.2 Capacitance-voltage characteristics

MOS capacitance structure is composed of two parts: the oxide capacitance and semiconductor capacitance (caused by depletion region). The two capacitances are in series.
The capacitance of a device is defined by

$$C = \frac{dQ}{dV}$$



10.2 Capacitance-voltage characteristics

Accumulation:
Cs is almost infinite.
A small change in Vg will cause a differential change in charge on the metal side and also hole accumulation charge. So the total capacitance is just Cox.

$$C'(\text{acc}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

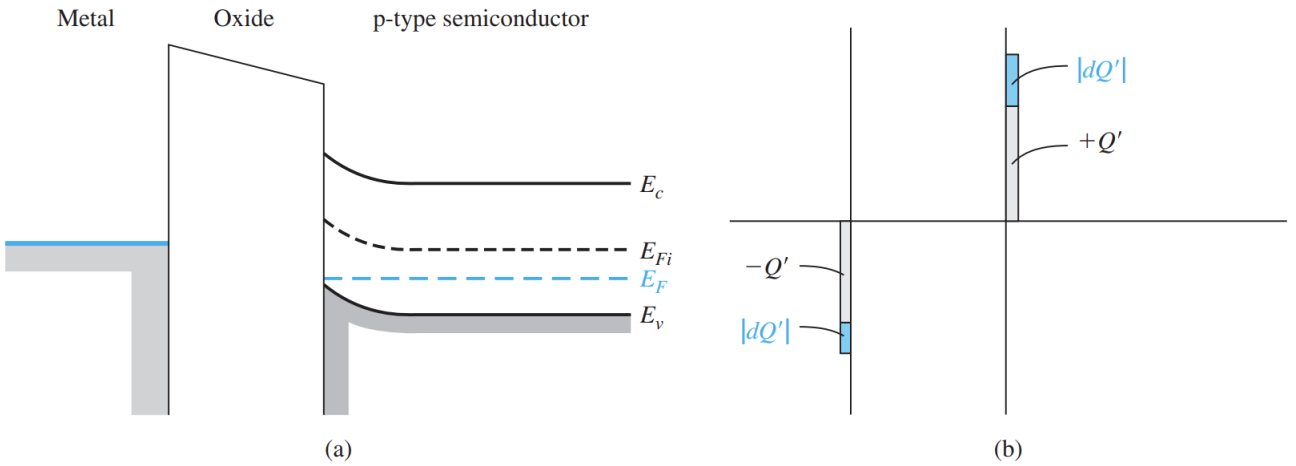


Figure. (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gain voltage

10.2 Capacitance-voltage characteristics

Depletion and weak inversion:
Cs and Cox are in series.

$$C'(\text{depl}) = \frac{C_{ox}C'_{SD}}{C_{ox} + C'_{SD}}$$

And since $C_{ox} = \epsilon_{ox}/t_{ox}$ and $C'_{SD} = \epsilon_s/x_d$,
We have $C'(\text{depl}) = \dfrac{C_{ox}}{1 + \dfrac{C_{ox}}{C'_{SD}}} = \dfrac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right)x_d}$

Obviously, when xd increases, total capacitance decreases. Thus, when the space charge width reaches its maximum, capacitance will reach its minimum.

$$C'_{\text{min}} = \frac{\epsilon_{ox}}{t_{ox} + \left(\dfrac{\epsilon_{ox}}{\epsilon_s}\right)x_{dT}}$$

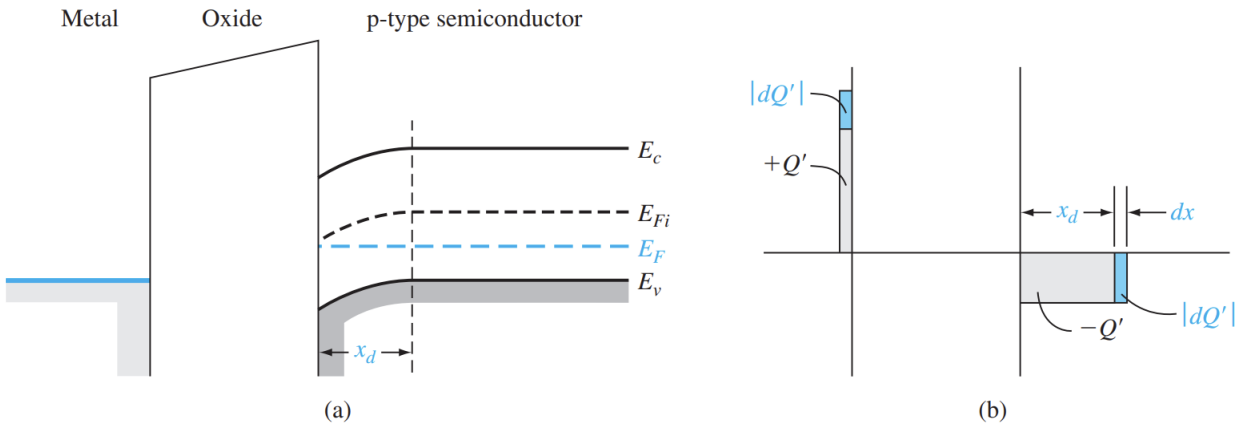


Figure. (a) Energy-band diagram through a MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

10.2 Capacitance-voltage characteristics

Strong inversion:
A small incremental change in the voltage across the MOS capacitor will cause a differential change in the inversion layer charge density.
The space charge width does not change.
As a result, the capacitance will be the oxide capacitance.

$$C'(\text{inv}) = C_{\text{ox}} = \frac{\epsilon_{\text{ox}}}{t_{\text{ox}}}$$

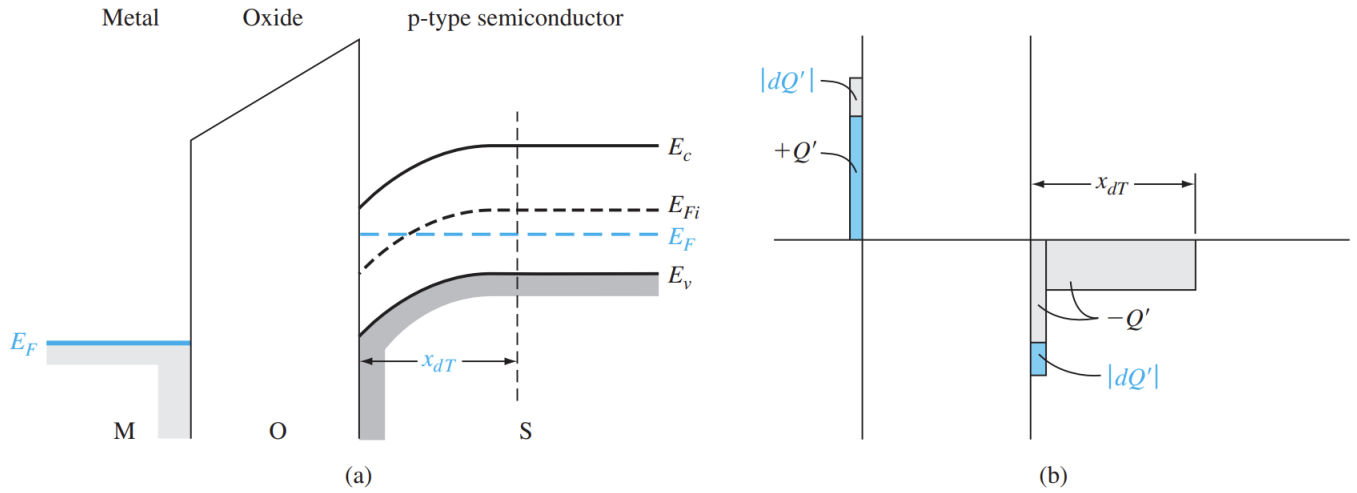


Figure. (a) Energy-band diagram through a MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

10.2 Capacitance-voltage characteristics

Here:
Moderate inversion: the transition region between the point when only the space charge density changes with gate voltage and when only the inversion charge density changes with gate voltage.
Flat band condition: happens between the accumulation and depletion mode.
Capacitance at flat band:

$$C'_{FB} = \frac{\epsilon_{ox}}{t_{ox} + \left(\frac{\epsilon_{ox}}{\epsilon_s}\right)\sqrt{\left(\frac{kT}{e}\right)\left(\frac{\epsilon_s}{eN_a}\right)}}$$

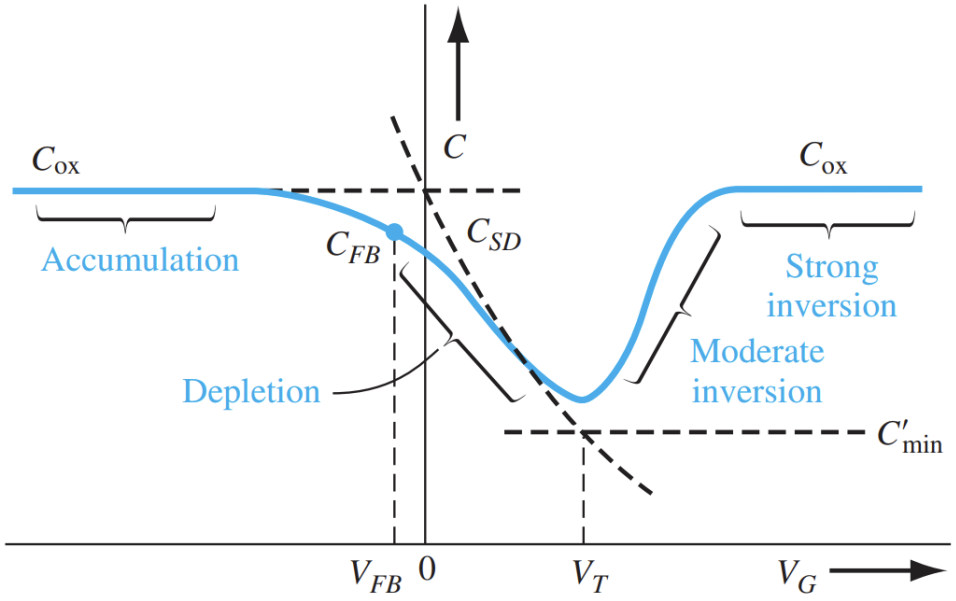


Figure. Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with a p-type substrate

10.2 Capacitance-voltage characteristics

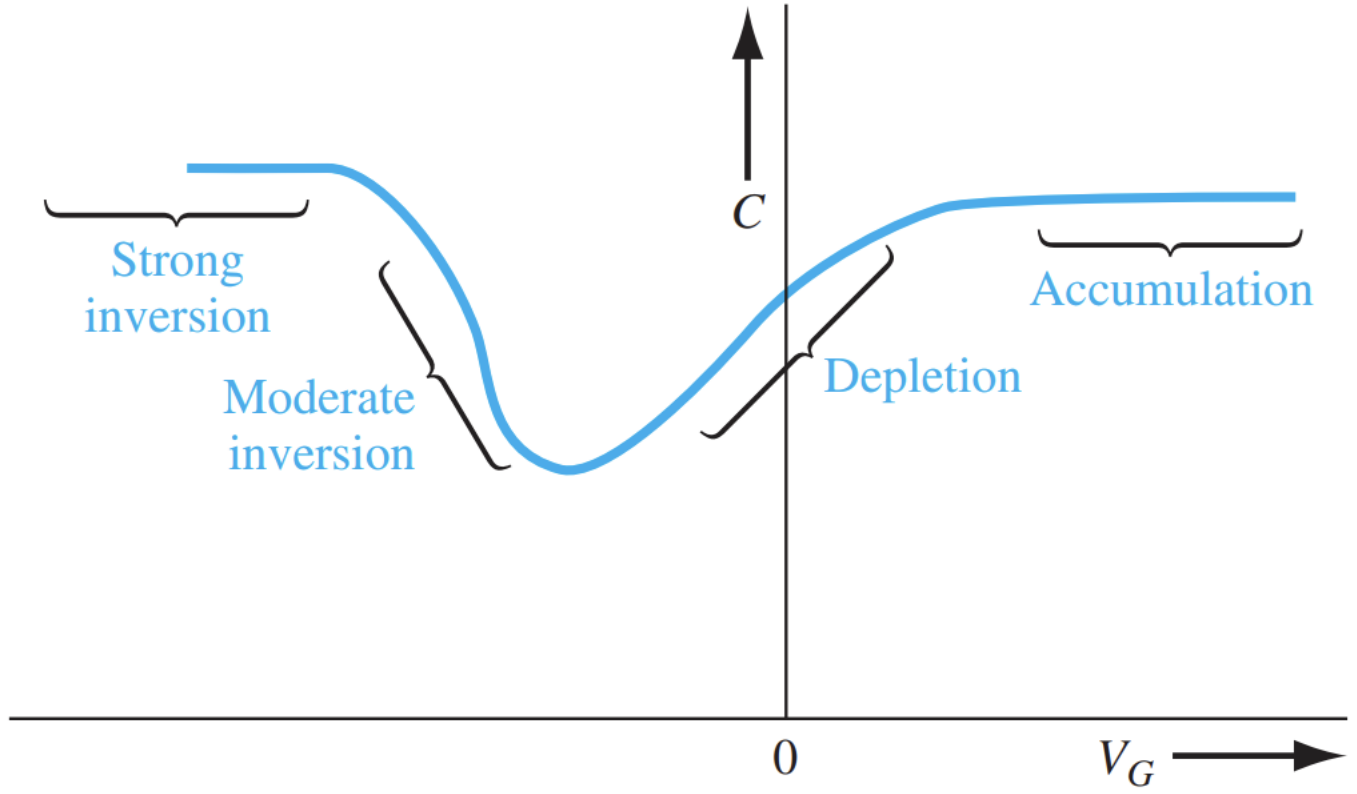


Figure. Ideal low-frequency capacitance versus gate voltage of a MOS capacitor with an n-type substrate.

10.2 Capacitance-voltage characteristics

The threshold voltage should be sum of the voltage across the semiconductor and the oxide.

$$V_T = V_s + V_{ox}$$

At threshold, voltage across the semiconductor should be $V_s = 2\phi_{fp}$

For voltage across the oxide,

$$V_{ox} = \frac{Q_{ox}}{C_{ox}} = \frac{e x_{dT} N_a}{C_{ox}} = \frac{2\sqrt{e\varepsilon_s N_a \varphi_{fp}}}{C_{ox}}$$

Therefore,

$$V_T = 2\emptyset_{fp} + \frac{2\sqrt{e\varepsilon_s N_A \emptyset_{fp}}}{C_{ox}}$$

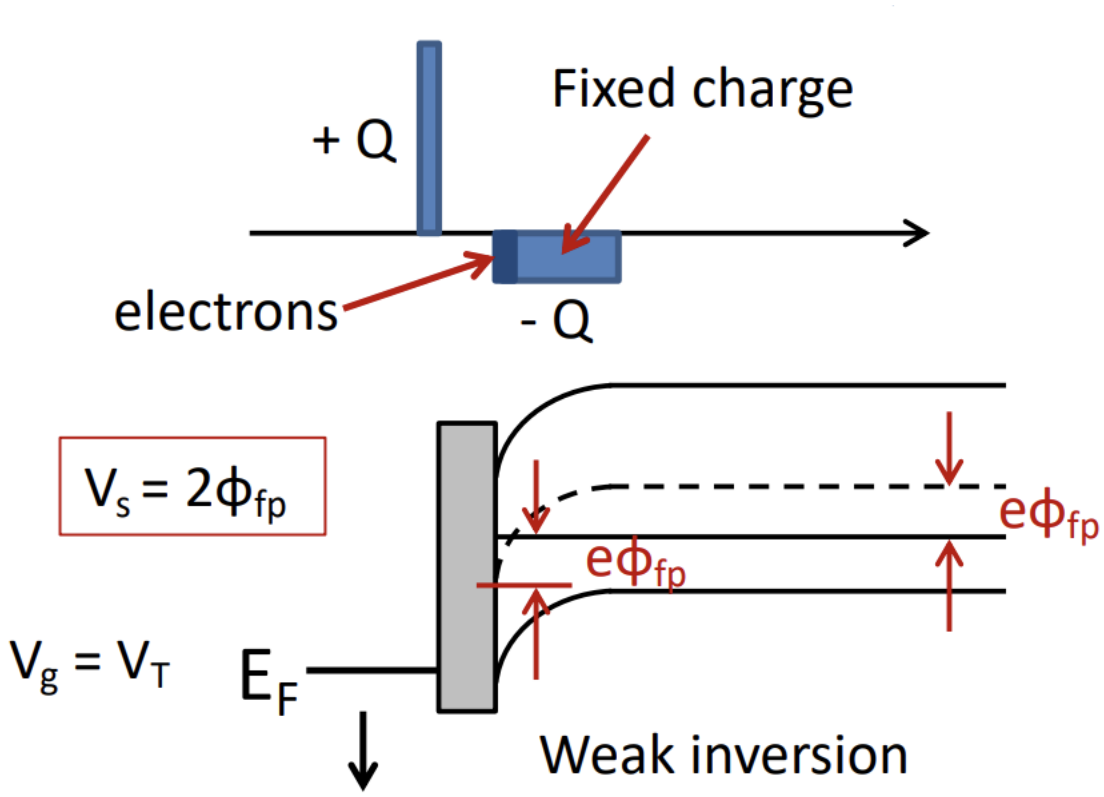


Figure. Energy-band diagram and charge distribution at the threshold voltage

10.2 Capacitance-voltage characteristics

Two sources of electrons (in the inversion layer):

1. Diffusion of minority carrier electrons
2. Thermal generation of electron-hole pairs within the space charge region.

Frequency effects: electron concentration in the inversion layer cannot change rapidly. In the limit of a high frequency, the inversion layer charge will not respond to a differential change in capacitor voltage.

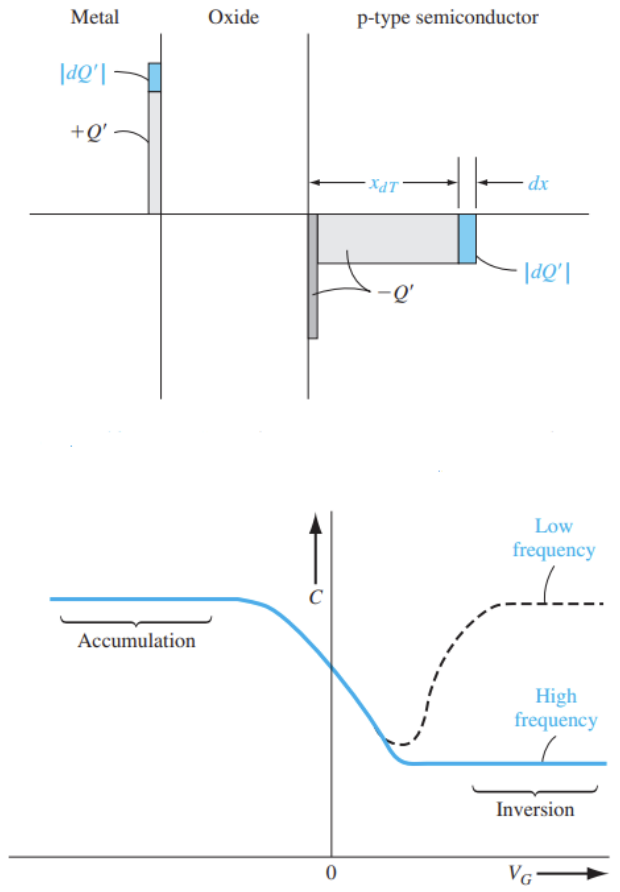


Figure. Charge distribution and low-freq and high-freq capacitance vs gate voltage. (p-type substrate)

10.3 Non-ideal effects

Metal-semiconductor work function difference:

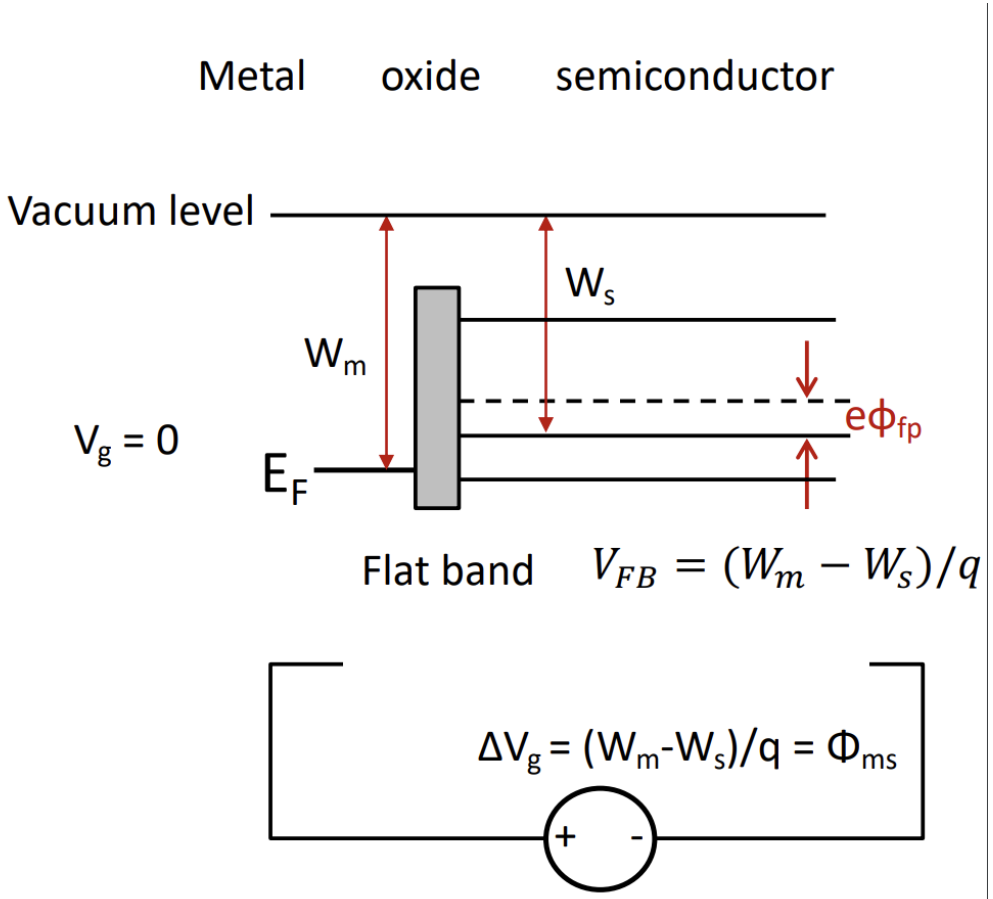
$$\emptyset_{ms} = \emptyset_m - \emptyset_s$$

Here, flat band voltage $V_{FB} = \emptyset_{ms}$

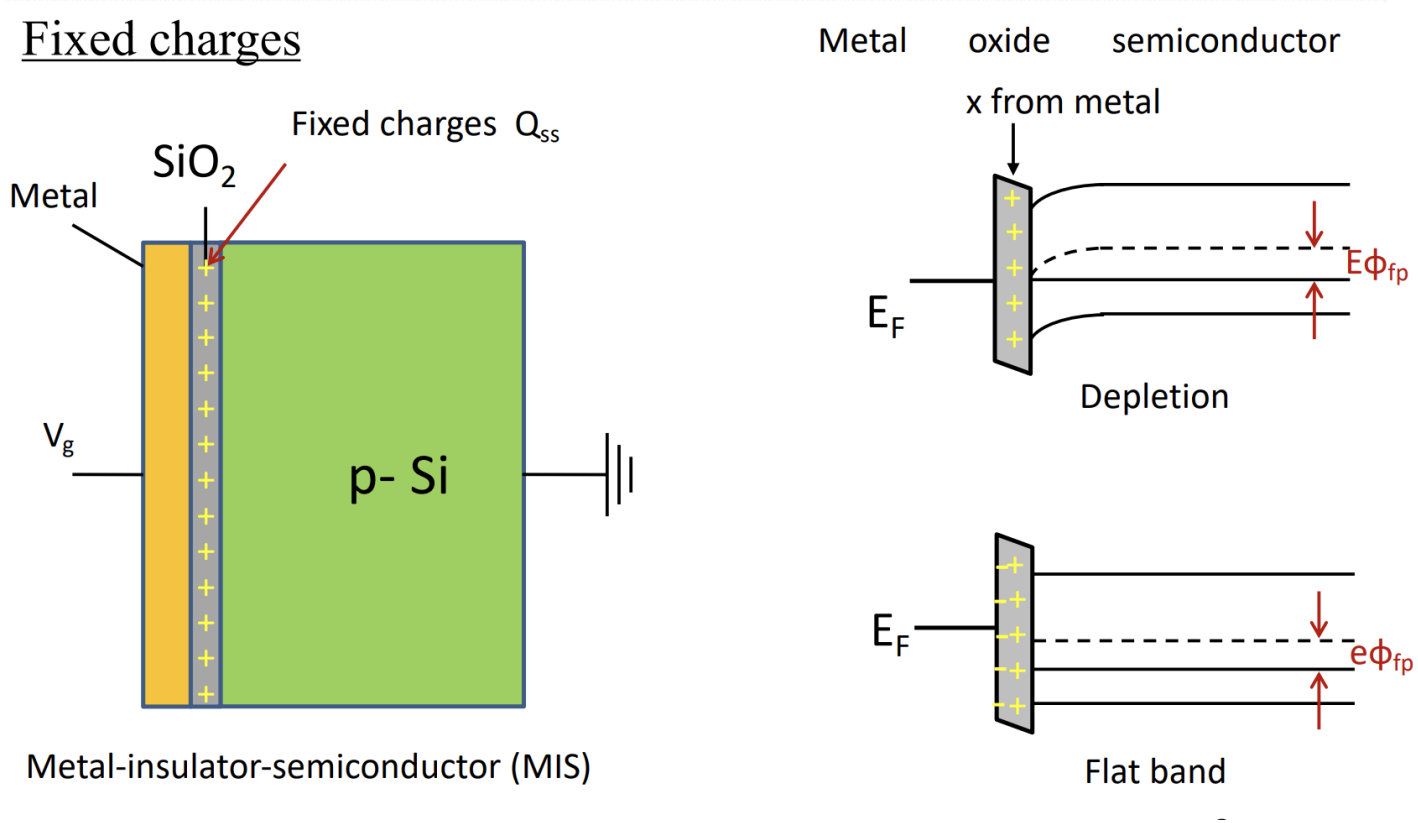
Thus, the threshold voltage

$$V_T = 2\emptyset_{fp} + t_{ox}\sqrt{\frac{4eN_a\varepsilon_{Si}\emptyset_{fp}}{\varepsilon_{ox}^2}} + V_{FB}$$

$$= 2\emptyset_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \emptyset_{ms}$$

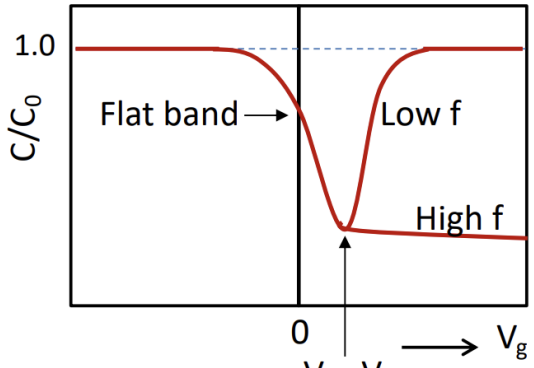


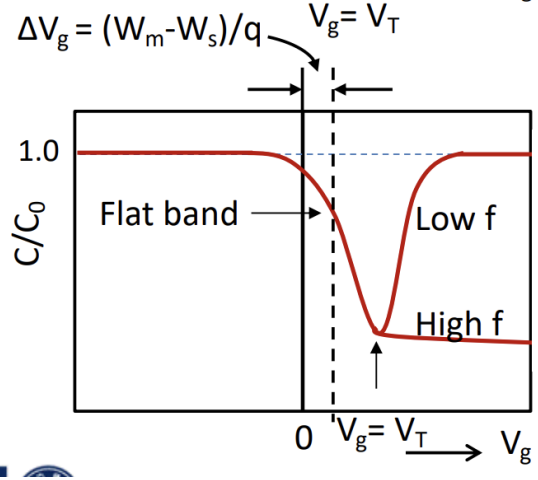
10.3 Non-ideal effects

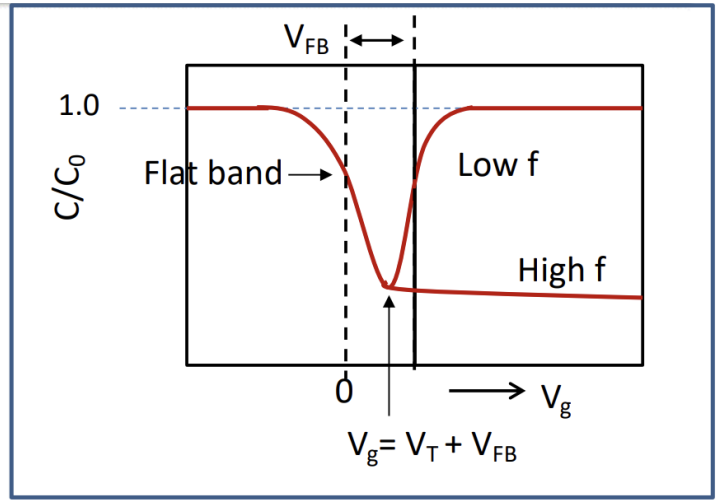


10.3 Non-ideal effects

Fixed charges





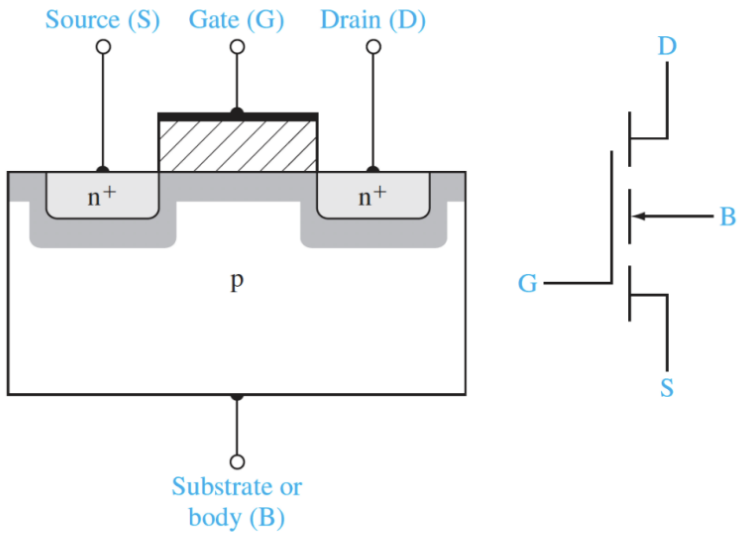


$$V_T = 2\emptyset_{fp} + t_{ox}\sqrt{\frac{4eN_a\varepsilon_{Si}\emptyset_{fp}}{\varepsilon_{ox}^2}} + V_{FB}$$

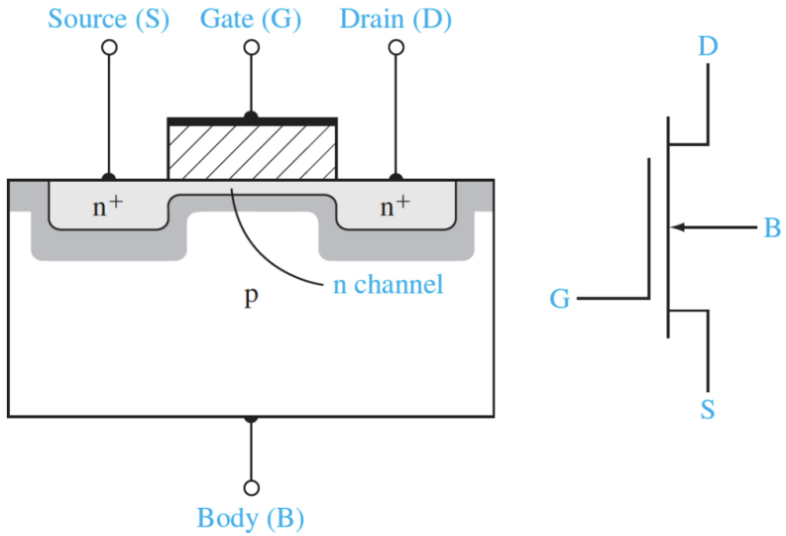
$$= 2\emptyset_{fp} + \frac{|Q_{SD}|}{C_{ox}} + \emptyset_{ms} - \frac{Q_{ss}}{C_{ox}}$$

10.4 The basic MOSFET operation

MOSFET structures



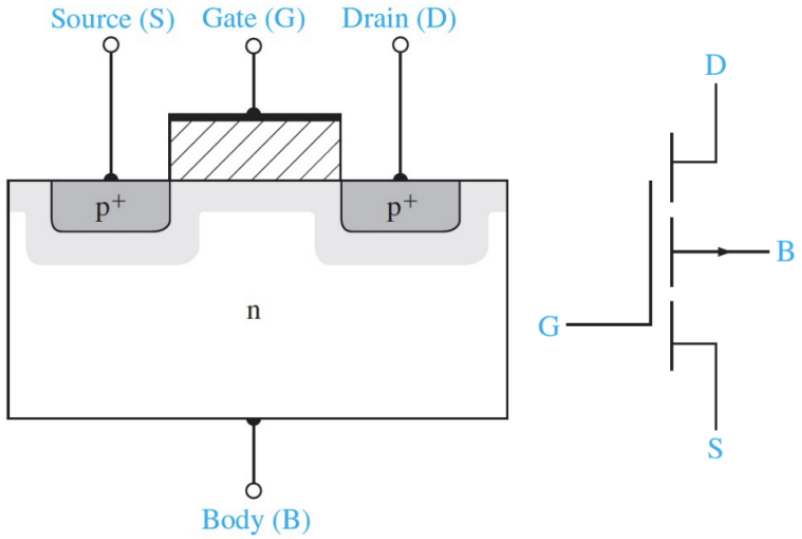
NMOS Enhancement mode



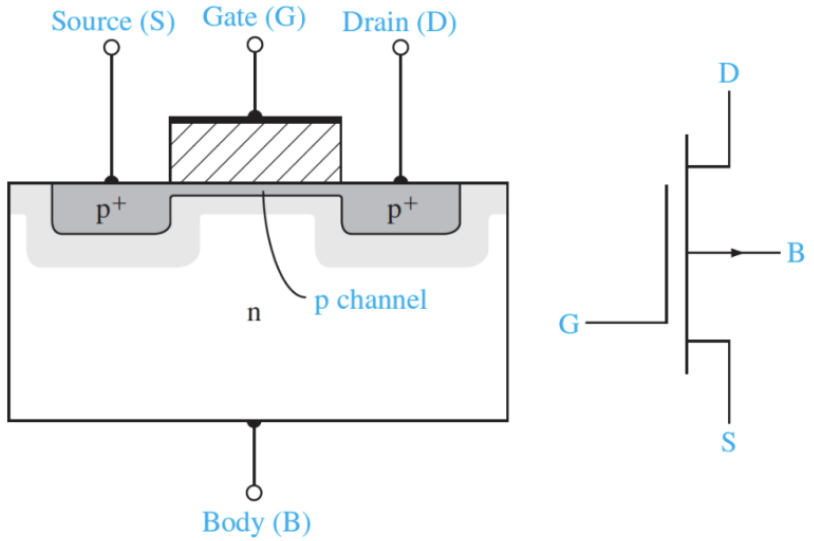
NMOS Depletion mode

10.4 The basic MOSFET operation

MOSFET structures



PMOS Enhancement mode



PMOS Depletion mode

10.4 The basic MOSFET operation

Source and substrate are grounded.
In (a), $V_{GS} < V_T$. There is no electron inversion layer, the drain-to-substrate pn junction is reverse biased, and the drain current is zero.
In (b), $V_{GS} > V_T$. The drain voltage is small. An electron inversion layer is created. Electrons flow from the source to the drain, so the current direction is from the drain to the source.

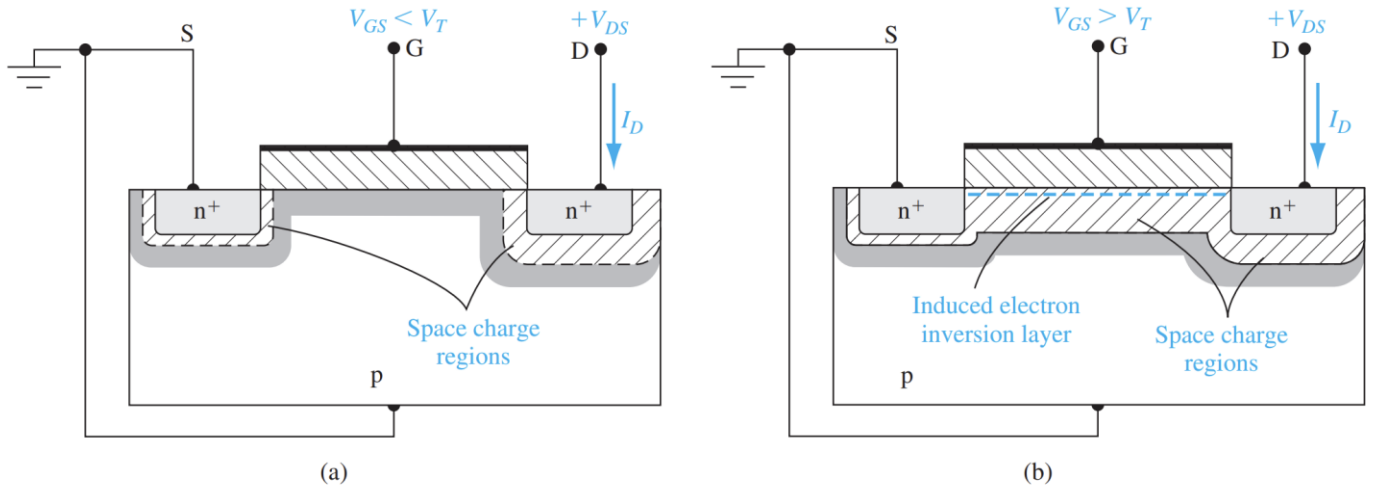


Figure. The n-channel enhancement mode MOSFET (a) with an applied gate voltage VGS < VT and (b) with an applied gate voltage VGS > VT.

10.4 The basic MOSFET operation

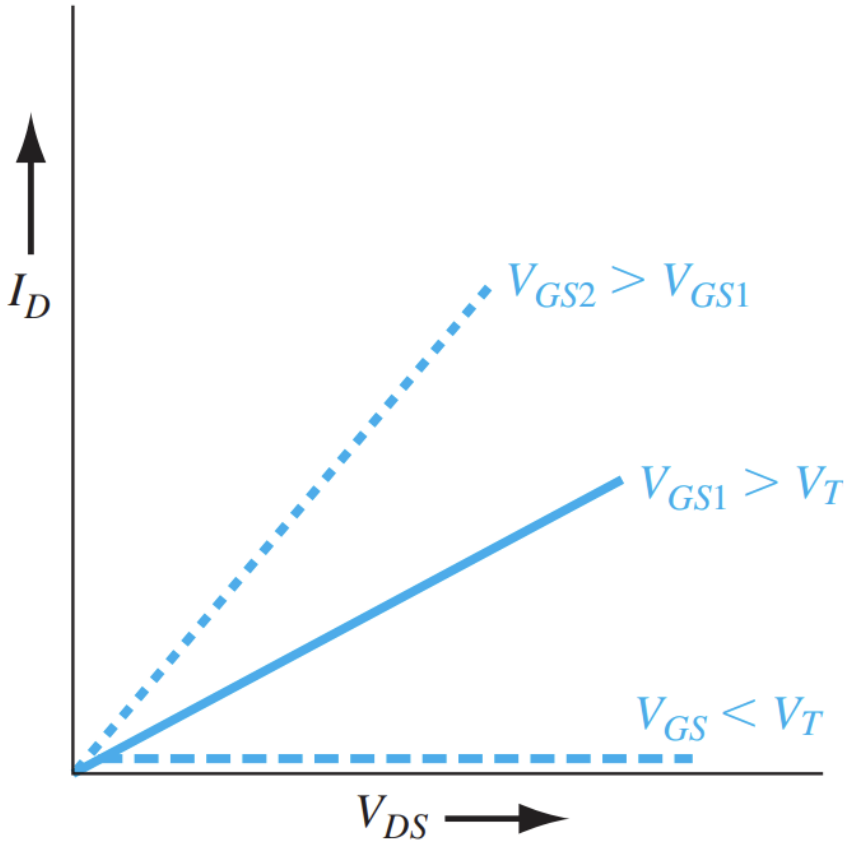


Figure. Id versus Vds characteristics for small values of Vds at three Vgs voltages.

10.4 The basic MOSFET operation

In (a), the thickness of the inversion channel layer qualitatively indicates the relative charge density. It is constant through the entire channel for this case.
In (b), when the drain voltage increases, the voltage drop across the oxide decreases. Thus, the induced inversion charge density decreases.
In (c), the drain voltage continues to decrease. It reaches the point when the voltage across the oxide at the drain is exactly V_T. $V_{DS}(sat) = V_{GS} - V_T$.
In (d), $V_{DS} > V_{DS}(sat)$, electrons enter the channel from the source, travel through the channel towards the drain and are swept by the electric field when they reach the point where inversion electron density is zero.

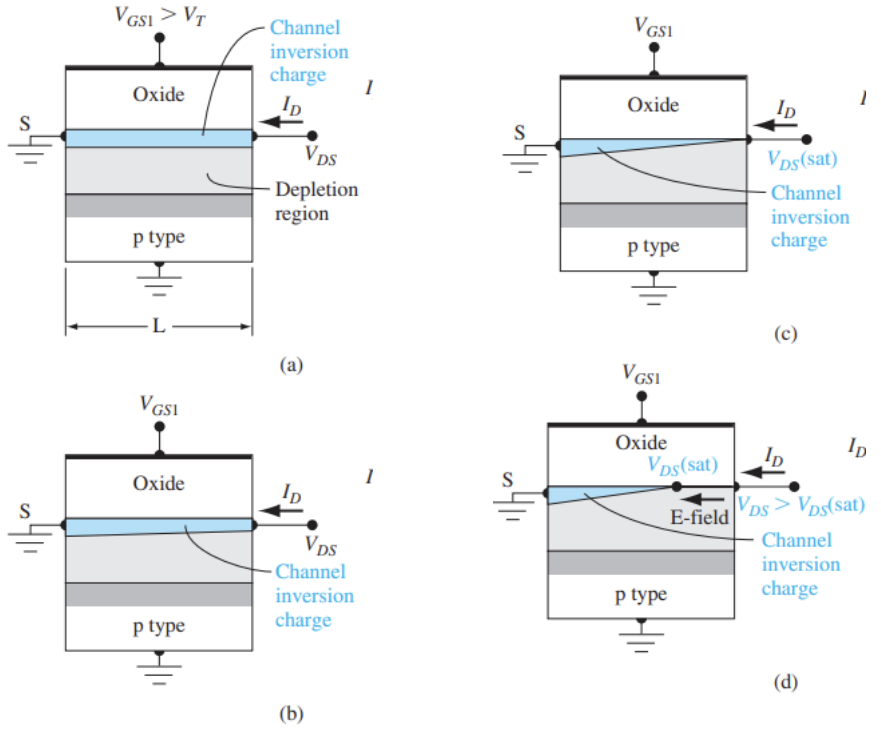


Figure. Cross section when $V_{GS} < V_T$ for (a) a small V_{DS} value; (b) a larger V_{DS} value; (c) a value of $V_{DS} = V_{DS}(sat)$; (d) a value of $V_{DS} > V_{DS}(sat)$

10.4 The basic MOSFET operation

I_D vs. V_{DS} Characteristics

The MOSFET I_D-V_{DS} curve consists of two regions:

1) Resistive or "Triode" Region: $0 < V_{DS} < V_{GS} - V_T$

$$I_D = k_n' \frac{W}{L}\left[V_{GS} - V_T - \frac{V_{DS}}{2}\right]V_{DS}$$

where $k_n' = \mu_n C_{ox}$

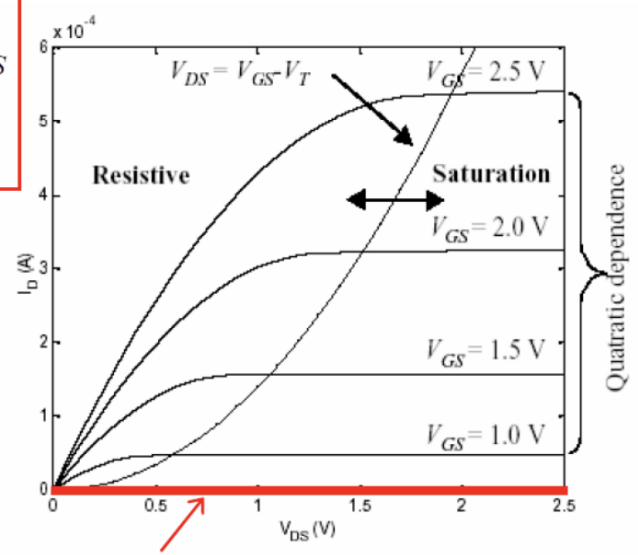
process transconductance parameter

2) Saturation Region:

$V_{DS} > V_{GS} - V_T$

$$I_{DSAT} = \frac{k_n'}{2}\frac{W}{L}(V_{GS} - V_T)^2$$

where $k_n' = \mu_n C_{ox}$



"CUTOFF" region: $V_G < V_T$

10.4 The basic MOSFET operation

$$I_D = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_T)V_{DS}$$

$$\sqrt{I_D(\text{sat})} = \sqrt{\frac{W\mu_n C_{ox}}{2L}}(V_{GS} - V_T)$$

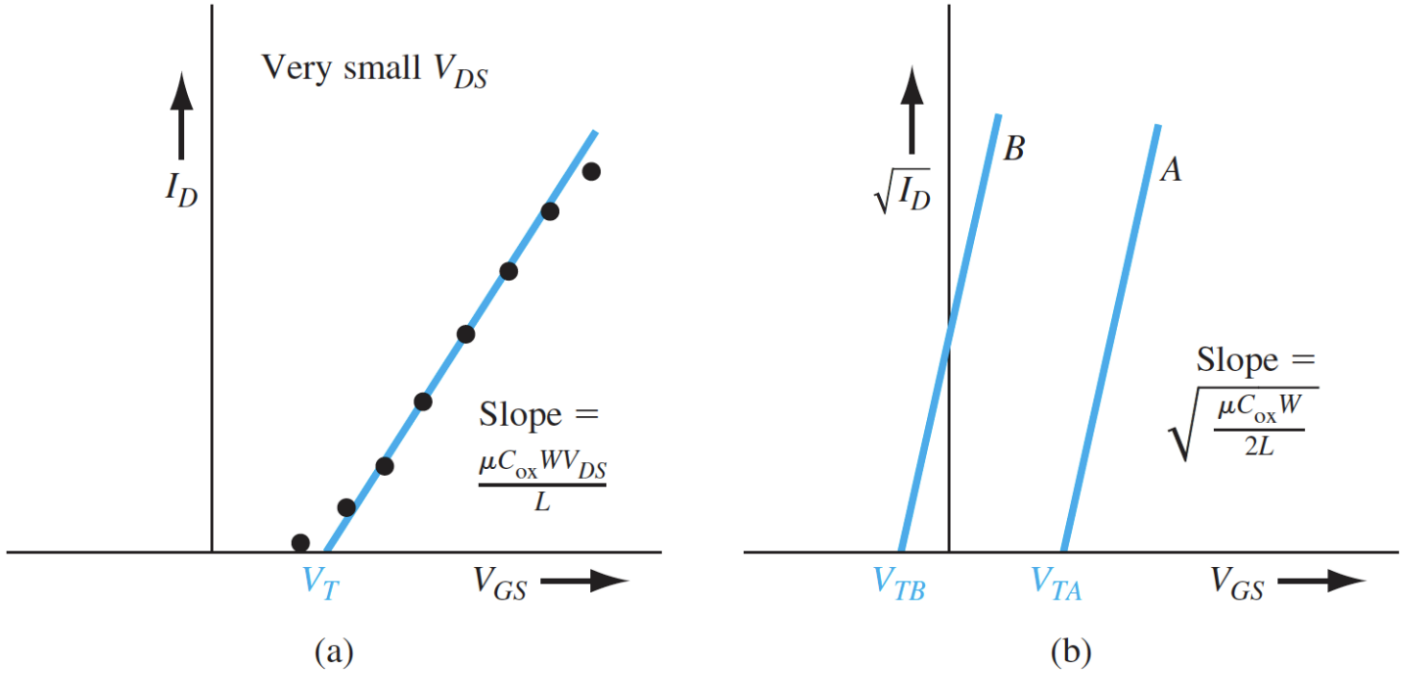
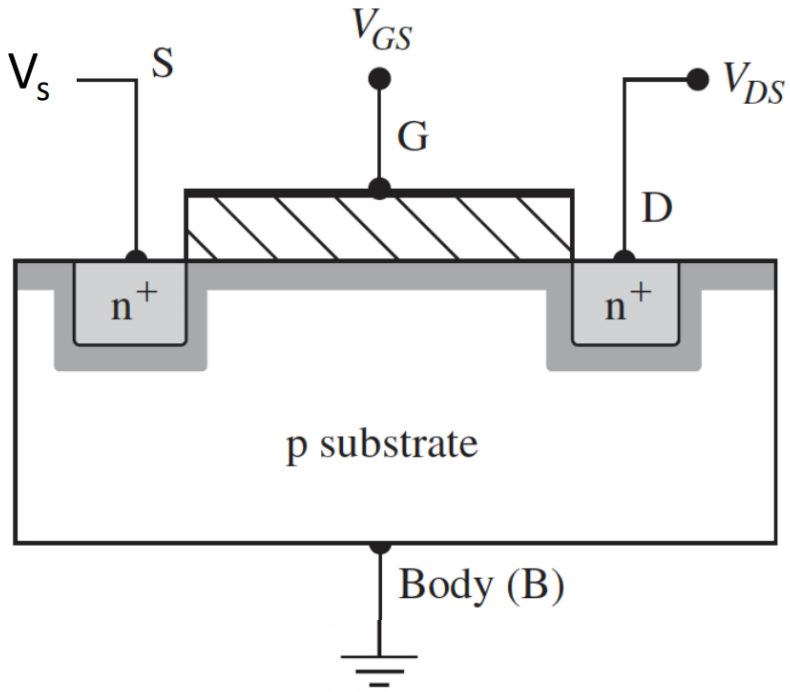
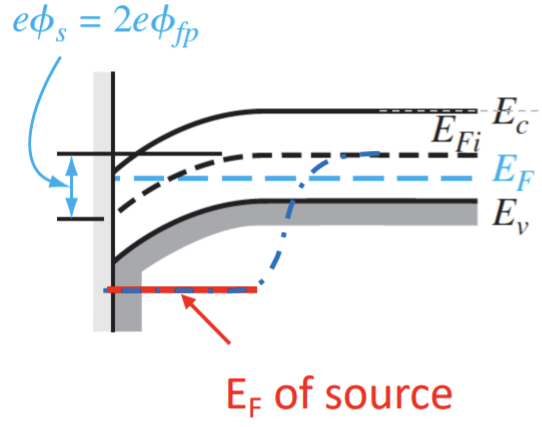


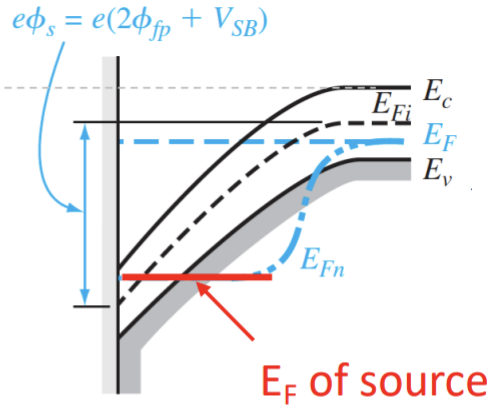
Figure. (a) I_D vs V_{GS} (for small V_{DS}) for enhancement model MOSFET. (b) Ideal $\sqrt{I_D}$ vs V_{GS} in saturation region for enhancement mode (curve A) and depletion mode (curve B) n-channel MOSFET.

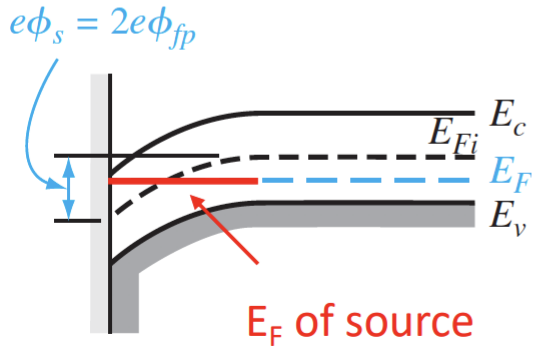
10.4 The basic MOSFET operation

Substrate bias effect









10.4 The basic MOSFET operation

When $V_{SB} = 0$, we had

$$Q'_{SD}\,(\text{max}) = -eN_a x_{dT} = -\sqrt{2e\epsilon_s N_a(2\phi_{fp})}$$

When $V_{SB} > 0$, the space charge width increases and we now have

$$Q'_{SD} = -eN_a x_d = -\sqrt{2e\epsilon_s N_a(2\phi_{fp} + V_{SB})}$$

The change in the space charge density is then

$$\Delta Q'_{SD} = -\sqrt{2e\epsilon_s N_a}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

To reach the threshold condition, the applied gate voltage must be increased. The change in threshold voltage can be written as

$$\Delta V_T = -\frac{\Delta Q'_{SD}}{C_{\text{ox}}} = \frac{\sqrt{2e\epsilon_s N_a}}{C_{\text{ox}}}\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

10.4 The basic MOSFET operation

Body effect coefficient

$$\gamma = \frac{\sqrt{2e\epsilon_s N_a}}{C_{ox}}$$

The equation can be rewritten as

$$\Delta V_T = \gamma\left[\sqrt{2\phi_{fp} + V_{SB}} - \sqrt{2\phi_{fp}}\right]$$

Thanks!