VE320 Intro to Semiconductor Devices

Summer 2024 – Problem Set 5

Due: 11:59pm, July 7th

In all problems, assume the temperature is 300K and all are completely ionization.

1. Define the built-in potential voltage and describe how it maintains thermal equilibrium.

2. Consider the equation $R_n = R_p = \frac{np - n_i^2}{\tau_{p0}(n+n') + \tau_{n0}(p+p')} \equiv R$, where $\tau_{p0} = \frac{1}{N_t C_p}$ and $\tau_{n0} = \frac{1}{N_t C_n}$. Let $\tau_{p0} = 10^{-7} s$ and $\tau_{n0} = 5 \times 10^{-7} s$. Also let $n' = p' = n_i = 10^{15} cm^{-3}$. Assume very low injection that $\delta n \ll n_i$. Calculate $R/\delta n$ for a semiconductor which is (a) n-type ($n_0 \gg p_0$), (b) intrinsic ($n_0 = p_0 = n_i$), and (c) p-type ($p_0 \gg n_0$).

3. Consider an n-type semiconductor as shown in the figure, doped at $N_d = 10^{16} cm^{-3}$ and with a uniform excess carrier generation rate equal to g' = 10^{21}cm^{-3}s^{-1}. Assume that D_p = 10cm^2/s and $\tau_{p0} = 10^{-7} s$. The electric field is zero. (a) Determine the steady-state excess minority carrier concentration versus x if the surface recombination velocity at x=0 is (i) s=0, (ii) s=2000cm/s, and (iii) s=∞. (b) Calculate the excess minority carrier concentration at x=0 for (i) s=0, (ii) s=2000cm/s, and (iii) s=∞.

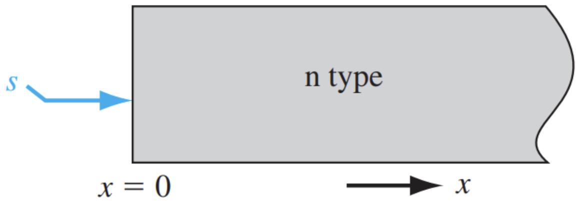

Figure 1. Diagram for problem 3

4. Consider a p1-p2 "isotype" step junction shown in the figure below:

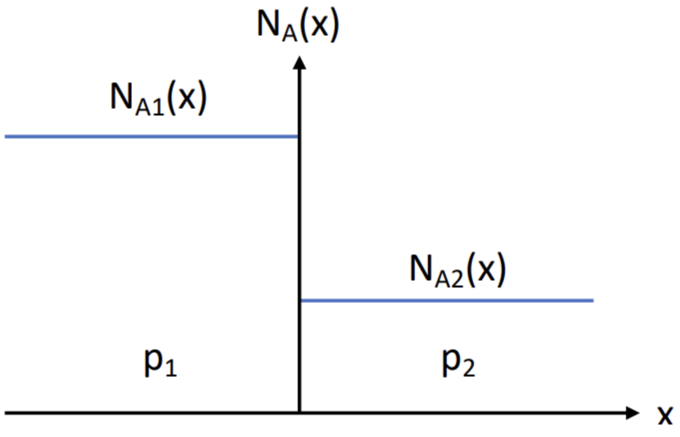

Figure 2. Diagram for problem 4

(a) Draw the energy band diagram of the junction assuming that the doping is non-degenerate throughout. Assume an energy gap of 1.4eV.

(b) Derive an expression for Vbi that exists across the junction in equilibrium.

5. A Ge diode has a p-side doping of $N_a = 5\times10^{16}\text{cm}^{-3}$ and an n-side doping of half that value.

(a) Calculate depletion widths on both sides of the junction and draw the equilibrium energy level diagram as a function of position. Carefully label all energy levels (Ec, Ev and Ef) and boundaries of the depletion region.

(b) Now apply a reverse voltage 0.1V and repeat part a. Include a sketch of the approximate positions of the quasi-Fermi energies.

6. Calculate the capacitance and plot $\frac{1}{C^2}$ vs V_R for the following Si n^+p junctions:

$Na = 10^{15}\text{cm}^{-3}$

(a) Reverse bias voltage = 1V; (b) reverse bias voltage = 5V.

(For n^+p junctions, $N_d \gg N_a$. Use a suitable approximation in your calculation.)

7. In the diagram below (the material is Si) :

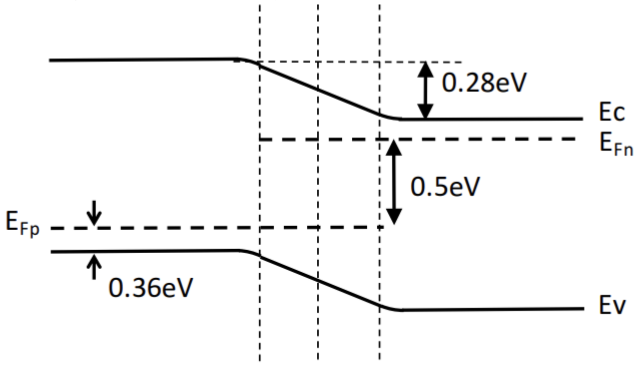

Figure 3. Diagram for problem 7

(a) Is the diode under equilibrium or forward biased or reverse biased? If biased, what is the bias voltage?

(b) Determine the built-in potential of the diode under equilibrium.

(c) Determine N_a and N_d.