EE 4352 Spring 2020

Introduction to VLSI Design Final Project

“8-Bit Power ALU”

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This project is to design 8-bit power ALU which will be able to execute 16 operations. The table below shows the operation codes in the designed ALU.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| s3 | s2 | s1 | s1 | Operation |
| 0 | 0 | 0 | 0 | Addition |
| 0 | 0 | 0 | 1 | Subtraction |
| 0 | 0 | 1 | 0 | Multiplication |
| 0 | 0 | 1 | 1 | Less than comparison |
| 0 | 1 | 0 | 0 | Transfer A |
| 0 | 1 | 0 | 1 | Increment A |
| 0 | 1 | 1 | 0 | Decrement A |
| 0 | 1 | 1 | 1 | 1’ Complement A |
| 1 | 0 | 0 | 0 | Logical AND |
| 1 | 0 | 0 | 1 | Logical OR |
| 1 | 0 | 1 | 0 | Logical XOR |
| 1 | 0 | 1 | 1 | Logical NOR |
| 1 | 1 | 0 | 0 | Logical NAND |
| 1 | 1 | 0 | 1 | Logical XNOR |
| 1 | 1 | 1 | 0 | Greater than comparison |
| 1 | 1 | 1 | 1 | Equal comparison |

Table 1: 8-bit ALU OP Codes

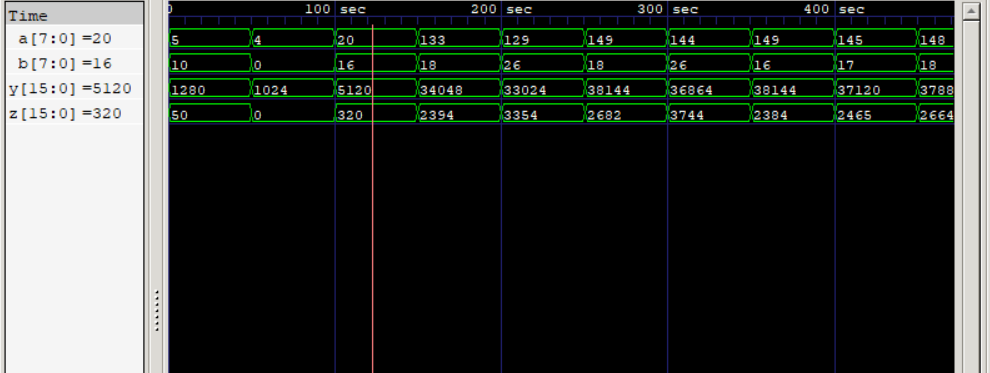
1. Addition and subtraction

The addition and subtraction are designed in one block(add\_sub.v), Cin = 0 for addition and Cin = 1 for subtraction. Below are the simulation results:



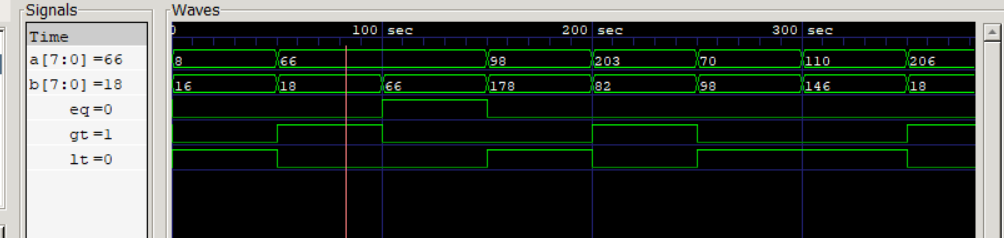
1. Multiplication

Multiplication is on the file Multi8.v and z is the multiplication result. Here is the result:

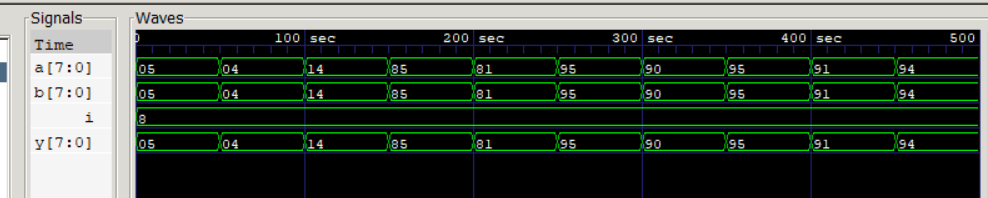


1. Comparator

Less than, Greater than and equal comparisons are in one block (comparator8.v) which is building with a 4-bit comparator. Here is the result:

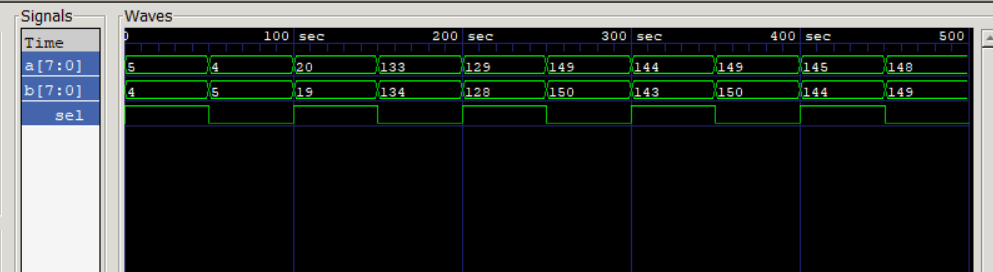


1. Transfer A



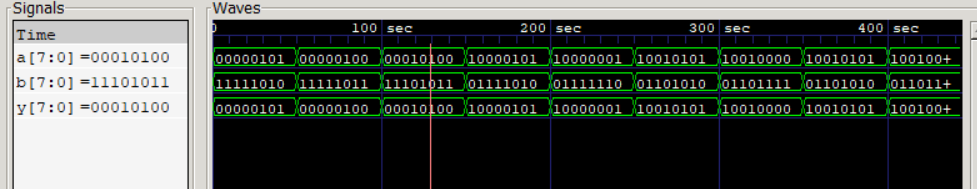
1. Increment and Decrement

These two operations are in one file Incre\_Dere.v; sel = 1 for increment and sel = 0 for decrement, and here is the result:



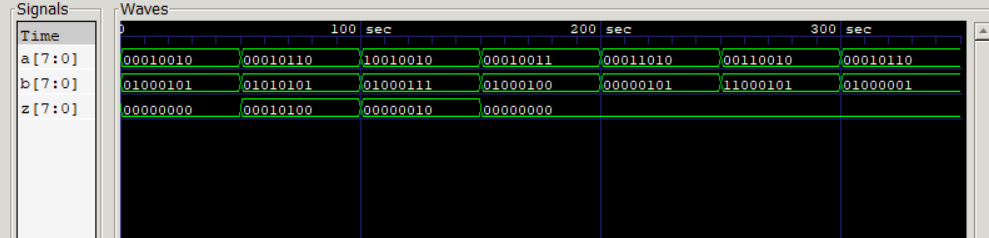
1. 1’s Complement A

This operation is in 1Complement.v:



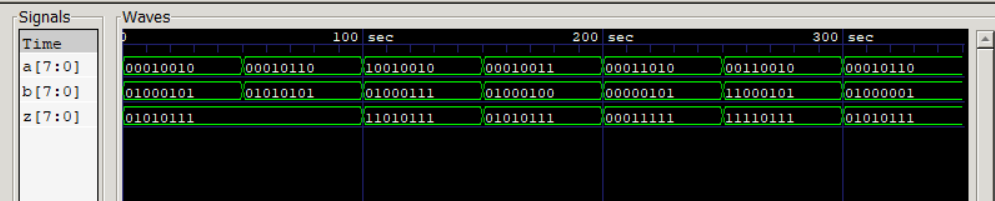
1. AND

The file is in AND8.v



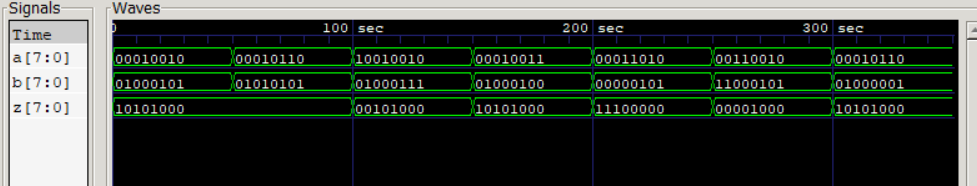
1. OR

The file is in OR8.v



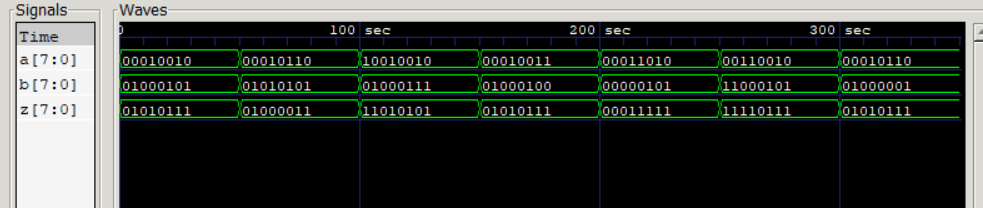
1. NOR

The file is in NOR8.v



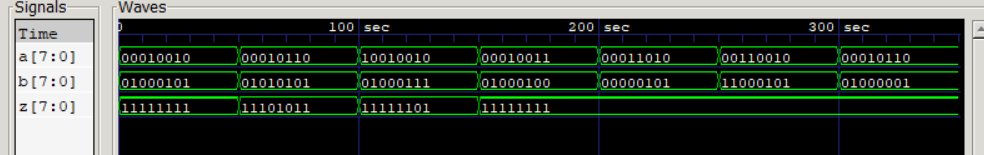
1. XOR

The file is in XOR8.v



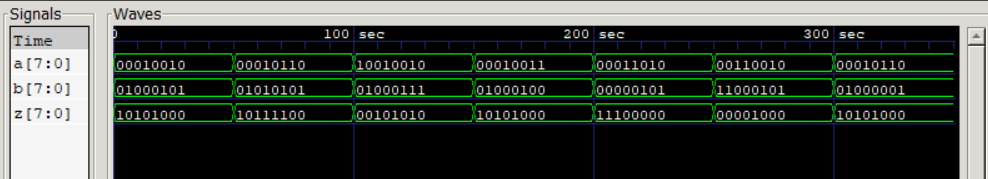
1. NAND

The file is in NAND8.v



1. XNOR

The file is in XNOR8.v



1. ALU

The file is in PowerALU\_Yaohong\_Sabotinova.v

