YAO JIANG CHEAH

R&D Firmware Engineer

EDUCATION

Iowa State University
Bachelor of Science

Major: Electrical Engineering

Graduation Date:
Graduated on May 2019

GPA: 3.82/4.00

CONTACT

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Personal Sites:
https://yaojiangc.github.io/

LinkedIn Profile:
https://www.linkedin.com/in/yjcheah/

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SKILLS

PROGRAMMING:
C, C++, Python, JavaScript, HTML5, CSS3, Verilog, VHDL, Assembly, VBA

EMBEDDED SYSTEM:
ARM, AVR, I2C, SPI, UART, FPGA, RTOS, Linux, USB Drivers, SOCs

IDE/SDK:
Keil, Vivado, IAR, Atmel Studio, ModelSim, Cadence, Quartus Prime, Eclipse, Visual Studio, QT Creator, AutoCAD, MATLAB

LANGUAGES:
Chinese, English, Malay

ADDITIONAL SKILLS:
First Aid Trainer, Advanced First Aid Certificate

PROFESSIONAL EXPERIENCE

Full-Time R&D Firmware Engineer
Broadcom Inc. *[Sep 2019–Present]*
- *Firmware debug & updates written in C*
- *Writing testing and production utilities in Python, C++*
- *Doing white box testing to ensure system reliability.*
- *Implement security piracy checking features in transceivers to ensure system reliability.*

Firmware Engineer Intern
Automed *[March 2019–May 2019]*
- *Updating & Debugging firmware of a livestock delivery device that is running on a STM32 ARM processor with RTOS for multi-threading.*
- *Fully in-charge of developing new firmware version and submit firmware releases for testing.*
- *Analyzing PCB board design drawings for future firmware development in and outside of work.*

Teaching Assistant for Digital Logic & Signal Processing II
Iowa State University *[August 2018–Dec 2018]*
- *In-charge of lab proctors, lab reports and exam paper gradings.*
- *Digital Logic Lab mainly includes using Quartus Prime software to do logic design using both schematic and Verilog coding method and then test it on Altera FPGA board.*
- *Signal Processing II Lab involves using MATLAB and Simulink to do signal analysis as well as filter designs. Lab also touches a little on PI controller.*

TECHNICAL PROJECTS

Sentry Launcher in Embedded Linux
- *Building a Sentry Launcher that shoots at a target with a certain color using the FPGA board with ARM Cortex-A9 processor, VITA camera and a Launcher.*
- *On hardware & programmable logic, VITA camera and launcher are connected with IP cores necessary to convert Bayer/grayscaled image to color image.*
- *On the processing system, a Linux system is being built & flashed into the processor and with initializing support for the VITA camera.*
- *On the software side, a launcher driver was designed by modifying a Linux USB skeleton driver code. A few other software was written including target finder, launcher controlled using buttons, and the final piece of sentry launcher.*
- *Direct memory access and USB drivers were methods called by software.*

PWM Signal Capture & Generate
- *Designing both hardware & software platform using an FPGA with SOCs and on-board ARM Cortex-A9 processor.*
- *Designing state-machine to achieve signal capture & generate.*
- *Designing hardware IP module based on state-machine designed in VHDL.*
- *Writing software/firmware and drivers support in C for the hardware designed to analyze data captured and re-generate pattern.*

Building 32-bit MIPS Microprocessor
- *Building a MIPS microprocessor with RISC architecture using VHDL code that understands 6 different assembly instructions (ADD, ADDI, LW, SW, BEQ, J)*
- *Two different versions of MIPS Microprocessor were built, which are single clock single instruction and multiple clock single instructions (pipelined).*
- *Everything was written in VHDL code from scratch except with ALU, and memory units provided.*