SKILLS

PROGRAMMING:
C, C++, Python, Batch Script, Shell Script, VBA, Verilog, VHDL, Assembly

EMBEDDED SYSTEM:
ARM, AVR, I2C, SPI, UART, Bootloader, FPGA, RTOS, Linux, USB Drivers, SOCs

IDE/SDK:
Keil, Vivado, IAR, Atmel Studio, STM32CubeIDE, ModelSim, Cadence, Quartus Prime, Eclipse, Visual Studio, QT Creator, AutoCAD, MATLAB

LANGUAGES:
Chinese, English, Malay

EDUCATION

Iowa State University
Bachelor of Science

Major: Electrical Engineering

Graduation Date:
Graduated on May 2019

GPA: 3.82/4.00

CONTACT

PHONE: 669-2067405

Personal Sites:
https://yaojiangc.github.io/

LinkedIn Profile:
https://www.linkedin.com/in/yjcheah/

EMAIL: y40jiang@gmail.com

YAO JIANG CHEAH

R&D Firmware Development Engineer

PROFESSIONAL EXPERIENCE

Firmware Engineer

Apple Inc. *[2020–Present]*

- Responsible for accessories firmware development
- Regular bug screenings & investigation
- Develop test automation solutions (continuous integration)

Firmware Development Engineer, R&D

Broadcom Inc. *[2019–2020]*

- Responsible for the full firmware development lifecycle in the ARM based embedded system development using C, including design, development, debug, testing, and maintenance.
- Designed and implemented bootloader system for the embedded system, which including writing the ERS (External Reference Specifications), IRS (Internal Reference Specifications), defining firmware image file structure, bootloader firmware implementation, debug, and testing, as well as programming tools development that work with them to update firmware over I2C interface.
- Designed and implemented switch to transceiver security features using AES-256 algorithms in various transceiver products (with ARM and AVR based microcontrollers) to protect our product from piracy.
- Firmware debug using SWD/JTAG/ICE interface.
- Implemented testing utilities in Python, C++ in both exe and DLL format.
- Performed white box testing using scripts to ensure system reliability.

Firmware Engineer Intern

Automed *[2019]*

- Updating & Debugging firmware of a livestock delivery device that is running on a STM32 ARM processor with RTOS for multi-threading.
- Fully in-charge of firmware development for releases.

Teaching Assistant for Digital Logic & Signal Processing II

Iowa State University *[August 2018–Dec 2018]*

- In-charge of lab proctors, lab reports and exam paper grading.

TECHNICAL PROJECTS

Sentry Launcher in Embedded Linux

- Implemented a Sentry Launcher that shoots at a target with a certain color using the FPGA board with ARM Cortex-A9 processor, VITA camera and a Launcher.
- On hardware & programmable logic, VITA camera and launcher were connected with IP cores necessary to convert Bayer/grayscaled image to color image.
- On the processing system, a Linux system was built & flashed into the processor and with initializing support for the VITA camera.
- On the software side, a launcher driver was designed by modifying a Linux USB skeleton driver code. A few other software was written including target finder, launcher controlled using buttons, and the final piece of sentry launcher.

PWM Signal Capture & Generate

- Designed both hardware & software platform using an FPGA with SOCs and on-board ARM Cortex-A9 processor.
- Designed state-machine to achieve signal capture & generate.
- Designed hardware IP module based on state-machine designed in VHDL.
- Implemented software/firmware and drivers support in C for the hardware designed to analyze data captured and re-generate patterns.

Built 32-bit MIPS Microprocessor

- Built a MIPS microprocessor with RISC architecture using VHDL code that understands 6 different assembly instructions (ADD, ADDI, LW, SW, BEQ, J)
- Two different versions of MIPS Microprocessor were built, which are single clock single Instruction and multiple clock single instructions (pipelined).