Review Test Submission: Exam I - Fall 2020

User	Yaokun Wu
Course	(MERGED) CS 2340.SEC501 - SE 2340.SEC501 - F20
Test	Exam I - Fall 2020
Started	9/24/20 5:32 PM
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Status	Completed
Attempt Score	74 out of 100 points
Time Elapsed	1 hour, 17 minutes out of 1 hour and 20 minutes
Instructions	• Exam time is 75 minutes, and a 5 mins extension is allowed if needed (total of 80 mins). • Exam is open everything, you can use whatever resources available. • Multiple answer questions have at least one correct and at least one incorrect answer. **Select all correct answers and avoid incorrect answers, as incorrect answers have a penalty. Do NOT select all answers, no credit will be given if all answers are selected.** • **Matching questions also have a penalty on incorrect matches.** • **An answer to an essay question must be concise and up-to-the-point and must cover all necessary ingredients to earn full credit. If the question has multiple parts (e.g. What and Why) EACH part MUST be answered separately.** • **For fill the blanks type of questions, do NOT include extra characters unnecessarily**. Where applicable, words shown in a figure of the question must be used. **Read your completed answer and make sure that the sentence makes sense.** • Pay attention to **upper/lower case** in your answers to fill the blanks type questions, since correct answers are case sensitive. Do not make a word upper case for no reason. • **Read the questions CAREFULLY!** • **Good luck!**
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

3 out of 4 points

A program module written in a high-level language, such as C++, must be translated into a object code module that contains the binary representation of data and instructions by a program called **[b]**. A **[c]** then combines several resulting modules and code from system libraries to create an executable file. This executable file then can be put into the main **[d]** of a computer system by a program called **[e]** so that the processor can execute instructions in that executable file.

Specified Answer for: b ✗ assembler

Specified Answer for: c linker

Specified Answer for: d memory

Specified Answer for: e loader

Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	compiler	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	linker	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	memory	
Correct Answers for: e		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	loader	

Question 2

3 out of 4 points

There are many system programs that are used in a computer system.

Selected Answers:
b.
An assembler can produce an executable program that can run on a computer.

A linker combines many object files into one executable file.

c.

d.
A compiler may translate a high-level language program directly to machine code without producing assembly language files.

Answers:
Examples of system programs: assembler, linker, compiler, editor.

a.

b.
An assembler can produce an executable program that can run on a computer.

A linker combines many object files into one executable file.

c.

d.
A compiler may translate a high-level language program directly to machine code without producing assembly language files.

Question 3

3 out of 4 points

Data are stored in the main memory of a computer system so that the processor can carry out data processing.

Selected Answers:

b. Strings are represented as arrays of hexadecimal digits.

c. Negative integer numbers are represented as 2-complimentary binary numbers.

d. Characters are represented as encoded binary numbers.

Answers:

a. Voice and video data are represented as two-dimension arrays of binary strings.

b. Strings are represented as arrays of hexadecimal digits.

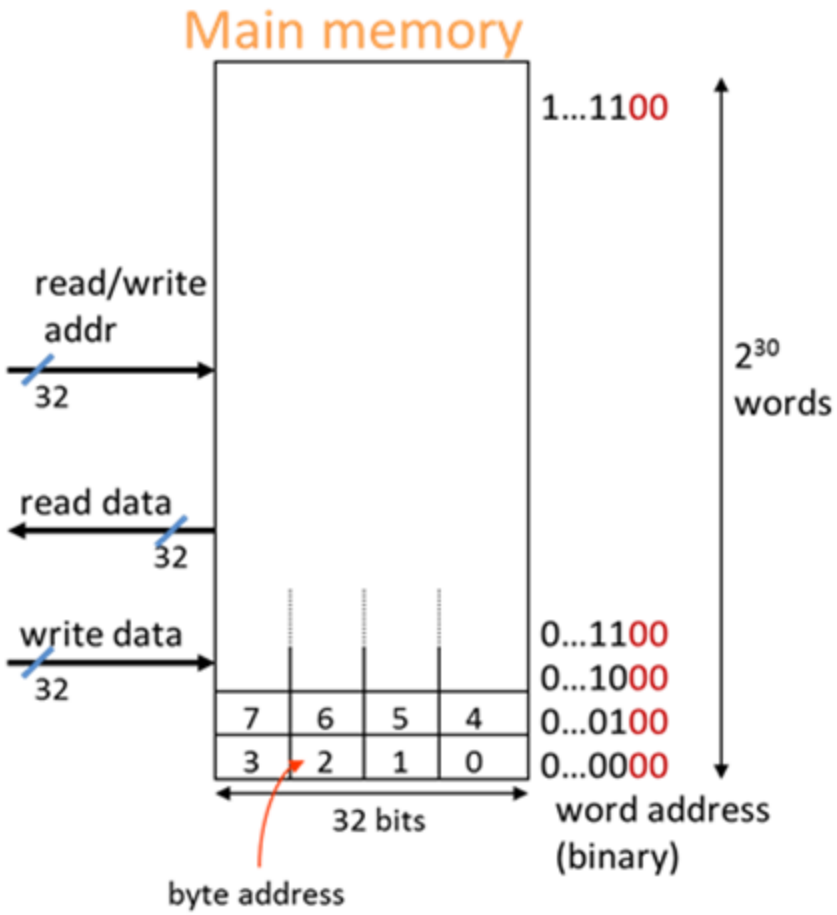
c. Negative integer numbers are represented as 2-complimentary binary numbers.

d. Characters are represented as encoded binary numbers.

Question 4

4 out of 6 points

The main memory of a 32-bit processor is shown in the diagram below and when a 32-bit integer **`0xABCD9876`** is stored at word address **`0...0100`**, the byte address 7 contains the value **`0xAB`**.



This processor uses the **[x]** Endian scheme to store a 32-bit word.

b. Assuming register `$s0` contains `0...1000`, after the following instructions were executed

```
sb   $zero, -2($s0) #
lbu  $t0, -3($s0)   #
```

the byte at byte address **[y]** in the main memory is set to 0, and the content of register `$t0` is **0x[z]**.

Note: do not include '0x' and do not omit leading 0s in the last answer.

Specified Answer for: x ✓ little

Specified Answer for: y ✓ 6

Specified Answer for: z ✗ 98

Correct Answers for: x		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	little	Case Sensitive
Correct Answers for: y		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	6	
Correct Answers for: z		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	00000098	

Question 5

4 out of 4 points

SuperNano is a 3-bit processor that uses sign-magnitude scheme to represent negative integers (thus each integer number is represented as a 3-bit binary number).

In the main memory of a SuperNano-based computer system, -1 is represented as **[a]** and 3 is represented as **[b]**.

Note: do NOT omit leading zeros in your answers.

Specified Answer for: a ✓ 101

Specified Answer for: b ✓ 011

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	101	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	011	

Question 6

5 out of 5 points

A program needs 122,000 CPU clock cycles to run on processor A that has a clock cycle time of 0.5nSec. The same program would require 212,000 CPU clock cycles to run on processor B that has a clock rate of 4GHz. Which processor has better performance and why?

Selected Answer: CPU time for A : 122000 * 0.5 * 10 ^(-9) = 61000 nSec.
CPU time for B: 212000 / (4 * 10 ^9) = 53000 sec.
performance = 1 / execution time. so that performance of B > A.

Correct Answer: CPU Time on A = 122,000 * 0.5 = 61000 nSec
CPU Time on B = 212,000 * 0.25 = 53000 nSec.
✓ Thus B is faster.

Response Feedback: [None Given]

Question 7

4 out of 4 points

SuperNano is a 3-bit processor that uses the 2's complement representation to represent negative integers (thus each integer number is represented as a 3-bit binary number).

In the main memory of a SuperNano-based computer system, -1 is represented as **[a]** and 3 is represented as **[b]**.

Note: do NOT omit leading zeros in your answers.

Specified Answer for: a ✓ 111

Specified Answer for: b ✓ 011

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	111	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	011	

Question 8

5 out of 5 points

MIPS instructions can be grouped into various categories depending on what the instruction does. Match MIPS instructions with their category. In case instructions match with two or more categories choose the most fitting one.

Question	Correct Match	Selected Match
addi	f. arithmetic and logical	f. arithmetic and logical
ori and sll	f. arithmetic and logical	f. arithmetic and logical
j and jr	b. change control flow unconditionally (jumping)	b. change control flow unconditionally (jumping)
beq and bne	d. change control flow conditionally (branching)	d. change control flow conditionally (branching)
lb and sb	e. data transfer	e. data transfer
slt and beq	d. change control flow conditionally (branching)	d. change control flow conditionally (branching)
ll and sc	c. synchronization	c. synchronization
lbu	e. data transfer	e. data transfer
sub	f. arithmetic and logical	f. arithmetic and logical
lw and sw	e. data transfer	e. data transfer

All Answer Choices

a. input/output

b. change control flow unconditionally (jumping)

c. synchronization

d. change control flow conditionally (branching)

e. data transfer

f. arithmetic and logical

g. floating point

Question 9

2 out of 2 points

A RISC architecture processor has instructions that directly manipulate (e.g. add a constant to) data stored in the main memory.

Selected Answer: False
Answers: True
False

Question 10

0 out of 2 points

In a MIPS processor, the PC (Program Counter) is always updated to contain PC + 4 (i.e. increased by 4) after the execution of current instruction.

Selected Answer: True
Answers: True
False

Question 11

0 out of 6 points

A memory location of a computer system that uses the MIPS ISA is shown in hexadecimal below.

0xAE080018

If this 32-bit word represents a MIPS instruction, it would be

[a] **[b]**, **[c]**

Specified Answer for: a sw $t0, $s0, 24

Specified Answer for: b 1010111000001000

Specified Answer for: c 0000000000011000

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	sw	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	$t0	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	24($s0)	

Question 12

3 out of 3 points

A user runs a program on a MIPS-32 processor-based computer system and the clock frequency of the processor is 2 GHz. After this program is completed the system reports that 10 billion instructions were executed, and the average CPI (Cycle-Per-Instruction) is 0.4. What is the CPU time (in seconds) spent on this run?

Selected Answer: 2

Correct Answer: 2

Answer range +/- 0 (2 - 2)

Question 13

1 out of 4 points

In the main memory of a computer system that uses a MIPS processor

Selected Answers:
- a. a 32-bit word must be stored at a memory location whose address is a multiple of 4.
- c. a data word (e.g. an integer) can locate between two instruction words.

Answers:
- a. a 32-bit word must be stored at a memory location whose address is a multiple of 4.
- b. a word (32-bits) does not have any inherent meaning.
- c. a data word (e.g. an integer) can locate between two instruction words.
- d. both data and instructions are stored as hexadecimal digits.

Question 14

4 out of 4 points

A MIPS assembly language statement may have label (optional), operation or assembler directive, operands and comment.

Considering following MIPS assembly language program:

```
        .data                   # data segment
item:.word    10
     .text                    #  code segment
     .globl  main
main:                         # your code goes here
      lw      $t0, item
      add     $s1, $t0,$zero
     li       $v0, 10      # exit to kernel
     ....
     syscall          #  system call (OS)
     .end
```

Fill the following blanks with corresponding items from the MIPS assembly language program above.

The first operation is **[x]**

The second assembler directive is **[y]**

The second label is **[z]**

The first operand of the 3rd instruction is **[v]**

Specified Answer for: x lw

Specified Answer for: y .word

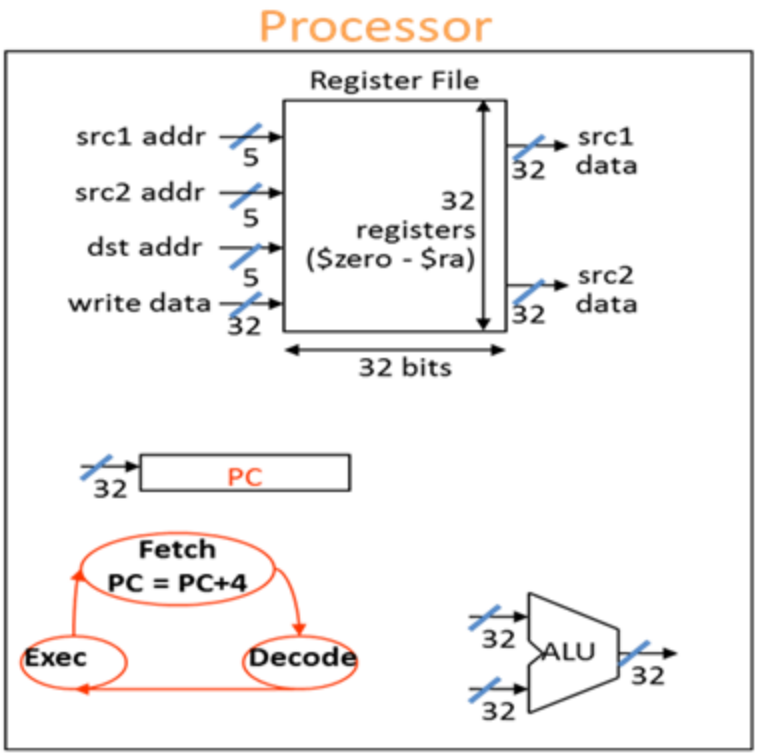
Specified Answer for: z main

Specified Answer for: v $v0

Correct Answers for: x		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	lw	Case Sensitive
Correct Answers for: y		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	.word	Case Sensitive
Exact Match	word	Case Sensitive
Correct Answers for: z		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	main:?	
Correct Answers for: v		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	$v0	Case Sensitive

Question 15

1 out of 5 points (Extra Credit)



The diagram above shows the major functional elements of a MIPS processor. Which element determines the control flow of a program?

Selected Answer:	ALU is the element determines the control flow of a program.
Correct Answer:	the PC
Response Feedback:	[None Given]

Question 16

4 out of 4 points

CPU time is an important performance metric for processors and it is affected by many parameters. Match parameter characteristics and parameter names.

Question	Correct Match	Selected Match
Faster an electrical signal alternates between 'Low' and 'High' levels., shorter the time of its period.	c. Clock rate.	c. Clock rate.
A larger number will make CPU time shorter.	c. Clock rate.	c. Clock rate.
The algorithms used in a program may make it larger or smaller.	a. Instruction count.	a. Instruction count.
The CPU hardware may affect this parameter which can be smaller or bigger than 1.	e. Cycles-per-instruction	e. Cycles-per-instruction

All Answer Choices

a. Instruction count.

b. The propagation speed of a clock signal.

c. Clock rate.

d. The efficiency of the compiler used.

e. Cycles-per-instruction

Question 17

2 out of 4 points

Loading a 32-bit constant (immediate) value into a register is an often needed operation but MIPS ISA does not have a native instruction to support that. Instead, it provides an instruction that can be used with another one to achieve the same result.

For example, the two instructions below will load the constant **`0xF1F2E3E4`** into register **`$t0`**:

```
[a] $t0, [b]
[c] $t0, $t0, [d]
```

Note: the answers must include 0x if the value is in hexadecimal.

Specified Answer for: a ✓ lui

Specified Answer for: b ✗ -3598

Specified Answer for: c ✓ ori

Specified Answer for: d ✗ -7197

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	lui	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	0xF1F2	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	ori	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	0xE3E4	

Question 18

3 out of 3 points

The format of MIPS ISA's branching instructions (beq and bne) is **[a]** format where the least significant 16 bits is used to encode the branching distance (in instructions). Thus the branch distance (from the instruction after the branch instruction) is limited to **[b]** instructions for branching backward and to **[c]** instructions branching forward.

Note: distance must be in decimal, e.g. 1250.

Specified Answer for: a ✓ I

Specified Answer for: b ✓ 32768

Specified Answer for: c ✓ 32767

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Pattern Match*	I\-?	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	32768	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	32767	

Response Feedback: 16-bit field encodes distance in 2's complimentary representation, which is -2^15 (32768) to +2^15 - 1 (32767). The negative range is for branching backward.

Question 19

2 out of 4 points

A MIPS assembly language program has the following code snippet:

```
DotheMath: add  $t0, $s0, $s0
           add  $t0, $t0, $t0
```

This code snippet can be replaced by one MIPS instruction below. Fill the blanks to complete that instruction.

```
DotheMath: [a]  [b], [c], [d]
```

Specified Answer for: a ✗ mult

Specified Answer for: b ✓ $t0

Specified Answer for: c ✓ $s0

Specified Answer for: d ✗ 4

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	sll	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	$t0	Case Sensitive
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	$s0	Case Sensitive

Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	2	

Question 20

5 out of 5 points

The MIPS ISA has only 3 instruction formats: R, I and J. The lw instruction is an **[a]** format instruction and this format has 4 fields: Opcode, Rs, Rt and Imm.

Thus when a MIPS assembler assembles the following instruction

lw $t0, 8($s0)

these fields would have the following values in decimal:

Opcode: **[c]**

Rs: **[d]**

Rt: **[e]**

Imm: **[f]**.

Specified Answer for: a I

Specified Answer for: c 35

Specified Answer for: d 16

Specified Answer for: e 8

Specified Answer for: f 8

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	I	Case Sensitive
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	35	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	16	
Correct Answers for: e		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	8	
Correct Answers for: f		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	8	

Question 21

4 out of 4 points

When a MIPS-32 processor executes the snippet of MIPS assembly language code below:

```
lw $v1, 0($a0)
addi $v0, $v0, 1
sw $v1, 0($a1)
sub  $v0, $t1, $t0
addi $a0, $a0, 1
```

the data segment is accessed **[a]** times, and the text segment is accessed **[b]** times.

Specified Answer for: a ✓ 2

Specified Answer for: b ✓ 5

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	2	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	5	

Question 22

0 out of 4 points

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)
0x10010000	0x6f6f6857	0x00216873	0x000007e4	0xffffff7a

A string is stored in the data segment starting at address 0x10010000 of the memory of a MIPS -32 processor-based computer system using the NULL-terminated method, and a portion of the data segment is shown above. Also, this system uses the little-Endian scheme.

The stored string is "_____".

Note: make sure that your answer contains no extra letters and the characters must be exact as stored in the memory, including cases.

Selected Answer: ✗ Whoosh!..z...

Correct Answer:

Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	Whoosh!	*Case Sensitive*

Question 23

4 out of 4 points

The following two MIPS-32 assembly language statements

```
slt $at, $t1, $t0
beq $at, $zero, Next
```

and the following MIPS-32 assembly language statement that uses a pseudo-instruction

[a] [b], [c], [d]

are equivalent.

Specified Answer for: a ✗ bge

Specified Answer for: b ✗ $t1

Specified Answer for: c ✗ $t0

Specified Answer for: d ✓ Next

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	ble	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	$t0	Case Sensitive
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	$t1	Case Sensitive
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	Next	Case Sensitive

Question 24

1 out of 4 points

Pseudo instructions in MIPS assembly language are

Selected Answers:
- ✗ b. understood by a MIPS processor.
- ✓ d. translated into one or more 32-bit word machine code in memory.

Answers:
- ✓ a. used to narrow the semantic gap between programmers and the ISA.
- b. understood by a MIPS processor.
- c. used by linkers.
- ✓ d. translated into one or more 32-bit word machine code in memory.

Question 25

2 out of 2 points

When computer performance is considered programming language, compiler and instruction set architecture determine how fast instructions are executed.

Selected Answer: False

Answers: True

False

Question 26

5 out of 5 points

A user runs his program on a MIPS-32 processor-based computer system and the clock frequency of the processor is 2 GHz. After this program is completed the system reports that 15 billion instructions were executed, and the average CPI (Cycle-Per-Instruction) is 0.6. What is the CPU time (in seconds) spent on this run?

Selected Answer: 4.5

Correct Answer: 4.5

Answer range +/- 0 (4.5 - 4.5)

Friday, November 13, 2020 9:54:24 PM CST

← OK