Review Test Submission: Exam II - Fall 2020

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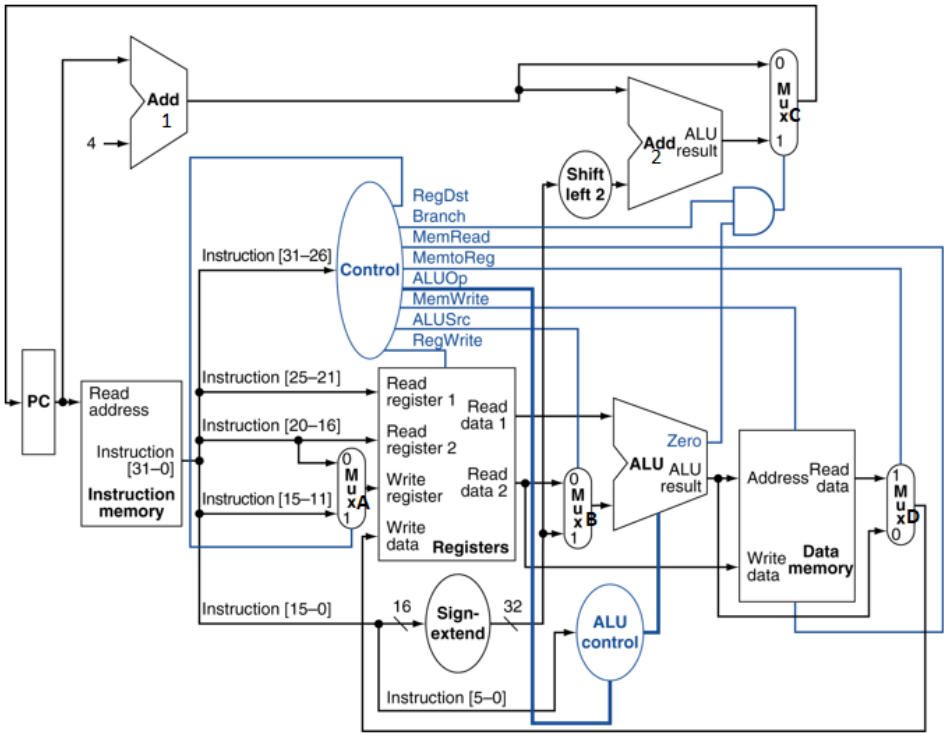
Course	(MERGED) CS 2340.SEC501 - SE 2340.SEC501 - F20
Test	Exam II - Fall 2020
Started	10/29/20 5:30 PM
Submitted	10/29/20 6:42 PM
Status	Completed
Attempt Score	93.25 out of 100 points
Time Elapsed	1 hour, 11 minutes out of 1 hour and 20 minutes
Instructions	• Exam time is 75 minutes, and a 5 mins extension is allowed if needed (total of 80 mins). • Exam is open everything, you can use whatever resources available. • Multiple answer questions have at least one correct and at least one incorrect answer. **Select all correct answers and avoid incorrect answers, as incorrect answers have a penalty. Do NOT select all answers, no credit will be given if all answers are selected.** • **Matching questions also have a penalty on incorrect matches.** • **An answer to an essay question must be concise and up-to-the-point and must cover all necessary ingredients to earn full credit. If the question has multiple parts (e.g. What and Why) EACH part MUST be answered separately.** • **For fill the blanks type of questions, do NOT include extra characters unnecessarily**. Where applicable, words shown in a figure of the question must be used. **Read your completed answer and make sure that the sentence makes sense.** • Pay attention to **upper/lower case** in your answers to fill the blanks type questions, since correct answers are case sensitive. Do not make a word upper case for no reason. • **Read the questions CAREFULLY!** • **Good luck!**
Results Displayed	All Answers, Submitted Answers, Correct Answers, Feedback, Incorrectly Answered Questions

Question 1

4 out of 4 points

In the datapath of a MIPS processor, multiplexers (MUXes) are used to select one out of multiple input data. The control unit of the processor generates the necessary control signals to select the right input when the processor is executing an instruction.

There are four MUXes (Mux A, Mux B, Mux C, and Mux D) shown in the diagram below.



Fill the table below with the correct value of the control signal of those MUXes when the processor is executing the instruction in the 1st column.

Values of the control signals can be 0, 1 or x. A 0 means the input labeled 0 is selected and x indicating 'does not matter'.

Instruction being executed	Mux A	Mux B	Mux C	Mux D
`beq $t0, $zero, Next # content of $t0 = 0`	**[ma]**	**[mb]**	**[mc]**	**[md]**
`lw $t0, 8($s1)`	**[a]**	**[b]**	**[c]**	**[d]**

Specified Answer for: ma ✓ x

Specified Answer for: mb ✓ 0

Specified Answer for: mc ✓ 1

Specified Answer for: md ✓ x

Specified Answer for: a ✓ 0

Specified Answer for: b ✓ 1

Specified Answer for: c ✓ 0

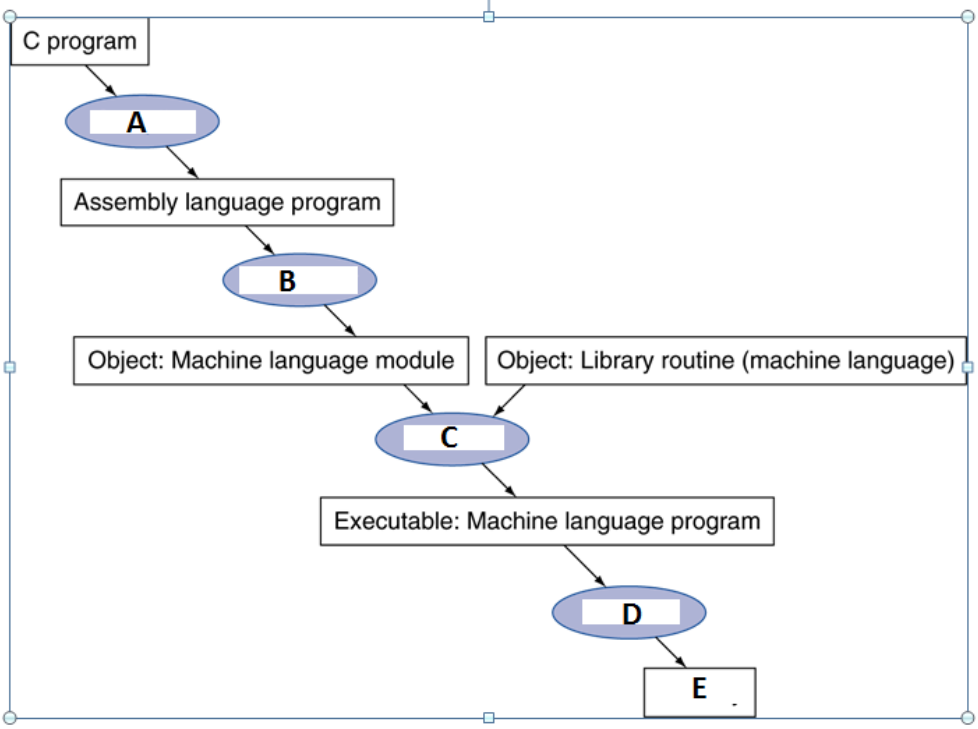
Specified Answer for: d ✓ 1

Correct Answers for: ma		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	x	
Correct Answers for: mb		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	0	
Correct Answers for: mc		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	1	
Correct Answers for: md		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	x	
Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	0	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	1	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	0	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	1	

Question 2

4 out of 4 points

The process of translating a C program into machine code that can be executed by a process is shown below, where E is the main memory of a computer system.



In this process:

A: **[a]**

B: **[b]**

C: **[c]**

D: **[d]**

Specified Answer for: a ✓ Compiler

Specified Answer for: b ✓ Assembler

Specified Answer for: c ✓ Linker

Specified Answer for: d ✓ Loader

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Pattern Match*	(?i) *compiler *	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Pattern Match*	(?i) *assembler *	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Pattern Match*	(?i) *linker *	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Pattern Match*	(?i) *loader *	

Question 3

0 out of 5 points (Extra Credit)

Following is the MIPS assembly code of a subroutine named mysub.

```
mysub:
     addi $sp, $sp, -4      # adjust stack for 1 item
     sw   $s0, 0($sp)       # save $s0
     add  $s0, $zero, $zero #
 L1: add  $t1, $s0, $a1
     lbu  $t2, 0($t1)
     add  $t3, $s0, $a0
     addi $t2, $t2, 32
     sb   $t2, 0($t3)
     beq  $t2, $zero, L2
```

```
    addi $s0, $s0, 1
    j    L1
L2: lw   $s0, 0($sp)        # restore saved $s0
    addi $sp, $sp, 4        # adjust stact pointer
    jr   $ra
```

Assuming that register **$a1** contain the memory address of a string that is terminated with a 0, what does this subroutine do?

Selected Answer: [None Given]
Correct Answer: convert an upper-case string to an lower-case one.
Response Feedback: [None Given]

Question 4

3 out of 3 points

After a MIPS processor executes the following instruction:

nor$ t0, $t1, $zero

the content of register **$t0** is **0x3501B252.**

The content of register $t1 before the execution is 0x_____.

Note: make sure the answer is an 8-digit hexadecimal.

Selected Answer: CAFE4DAD
Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	cafe4dad	

Question 5

3 out of 3 points

Match I/O operations of a processor with I/O register sets.

Question	Correct Match	Selected Match
Instruct the I/O device to perform some action.	d. control	d. control
Check to see if the I/O device is ready.	e. status	e. status
Transfer data to/from the device.	c. data	c. data

All Answer Choices

a. buffer
b. Channel Control Word (CCW)
c. data
d. control
e. status

Question 6

2 out of 2 points

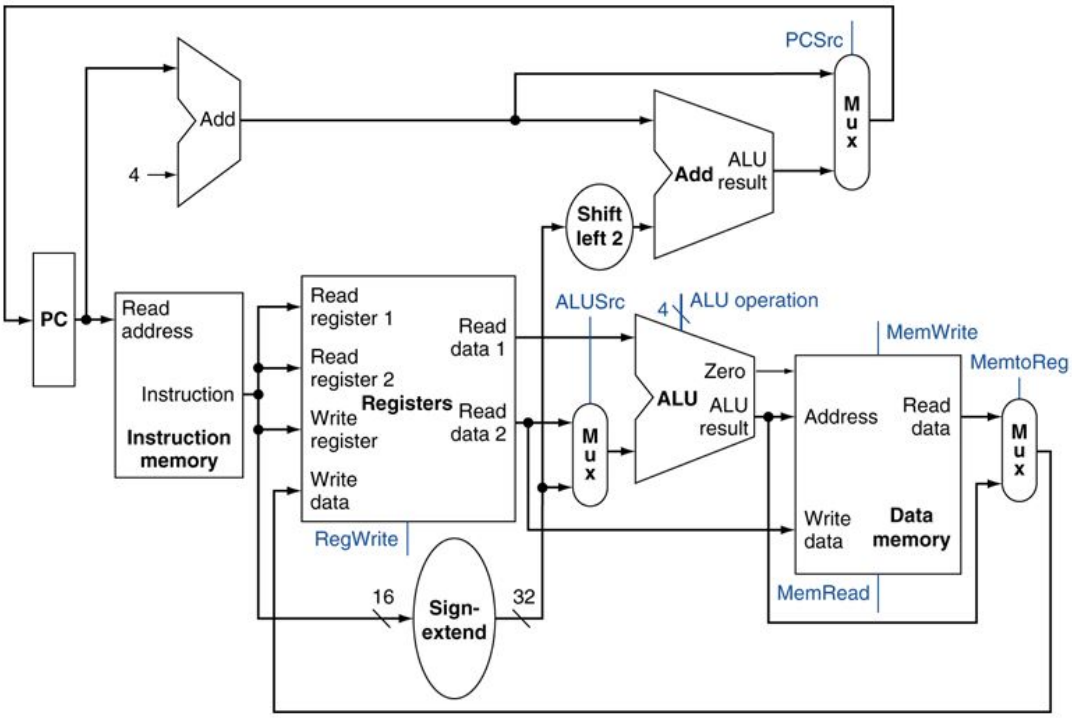
The datapath in a MIPS processor processes only data in registers or data stored in the memory (after being loaded into registers).

Selected Answer: False
Answers: True
False
Response Feedback: Addresses are also processed by the datapath.

Question 7

7 out of 7 points

The full datapath of a MIPS-32 processor is shown in the diagram below.



In this diagram, the function to be carried out by the ALU is determined by the 4-bit ALU control signal as shown in the following table:

ALU control	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set-on-less-than
1100	NOR

Fill the blanks with the value of control signals when the processor is executing the instruction on the left, assuming that if the value of the selector signal of a multiplexer is '0' its input on the top will be selected. If the control signal is not needed for the instruction execution the value 'x' should be used.

Instruction being executed	PCSrc	ALUSrc	ALU operation	MemWrite	MemtoReg	RegWrite	MemRead
`lw $t0, 16($s0)`	[a]	[b]	[c]	[d]	[e]	[f]	[g]

Specified Answer for: a 0

Specified Answer for: b 1

Specified Answer for: c 0010

Specified Answer for: d 0

Specified Answer for: e 0

Specified Answer for: f 1

Specified Answer for: g 1

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	0	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	1	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	0010	

Correct Answers for: d		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	0	
Correct Answers for: e		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	0	
Correct Answers for: f		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	1	
Correct Answers for: g		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	1	

Question 8

4 out of 4 points

In a MIPS processor based computer system, I/O address space **0xffff0000** to **0xffffffff** is reserved for memory-mapped I/O. Assuming that each I/O device needs 3, 1, and 4 32-bit words for control, status and data registers respectively. How many I/O devices can be supported?

Selected Answer: 2048

Correct Answer: 2,048

Answer range +/- 0 (2048 - 2048)

Response Feedback: 8 32-bit words each, address space is 8 * 2048 words.

Question 9

5 out of 5 points

Considering the code of subroutine **sub1** below, fill the blanks to complete it.

```
#
      sub1: addi $sp, $sp, [a]  # make room on the stack to save $t0, $a0, $a1 and $ra
            sw   $t0, 12($sp)   #
            sw   $a1, 8($sp)    #
            sw   $a0, 4($sp)    #
            sw   $ra, 0($sp)    #
            addi $t0, $0, 2
            slt  $t0, $a0, $t0  #
            beq  $t0, $0, else  #
            addi $v0, $0, 1     #
            addi $sp, $sp, [b]  # restore $sp
            jr   $ra            # return
#
      else: addi $a0, $a0, -1   #
            jal  sub1           #
            lw   $ra, [b1]($sp) # restore $ra
            lw   $a0, [b2]($sp) # restore $a0
            lw   $a1, [b3]($sp)    # restore $a1
            lw   $t0, [b4]($sp)    # restore $t0
            [c]  $sp, [d], [e]  #
            mul  $v0, $a0, $v0  #
            jr   $ra            # return
```

There are two types of subroutines: leaf and non-leaf, and the subroutine **sub1** above is a **[f]** subroutine.

Specified Answer for: a -16

Specified Answer for: b 16

Specified Answer for: b1 0

Specified Answer for: b2 4

Specified Answer for: b3 8

Specified Answer for: b4 12

Specified Answer for: c addi

Specified Answer for: d $sp

Specified Answer for: e 16

Specified Answer for: f non-leaf

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	-16	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	16	
Correct Answers for: b1		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	0	
Correct Answers for: b2		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	4	
Correct Answers for: b3		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	8	
Correct Answers for: b4		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	12	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	addi	
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	$sp	Case Sensitive
Correct Answers for: e		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	16	
Correct Answers for: f		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	non-leaf	Case Sensitive

Question 10

4 out of 4 points

Intel's 32-bit processors are based on the IA-32 ISA. This ISA

Selected Answers:
- c. has a micro-engine that is based on RISC (Reduced Instruction Set Computer) design.
- d. supports operations that directly manipulate data in the main memory.

Answers:
- a. has 32-bit registers only.
- b. uses fix length for instructions encoding.
- c. has a micro-engine that is based on RISC (Reduced Instruction Set Computer) design.
- d. supports operations that directly manipulate data in the main memory.

Question 11

5 out of 5 points

There are many addressing modes supported by a MIPS processor. Match the way an operand is obtained by the processor with its addressing mode.

Question	Correct Match	Selected Match
The operand is a constant within the instruction itself	g. Immediate addressing	g. Immediate addressing
The operand is the content of a register	c. Register addressing	c. Register addressing
The operand is at the memory location whose address is the sum of a register and a constant in the instruction	a. Base or displacement addressing	a. Base or displacement addressing
The branch destination address is the sum of the PC and a constant in the instruction	e. PC-relative addressing	e. PC-relative addressing
The jump destination address is the 26 bits of the instruction concatenated with the upper bits of the PC and '00'.	b. Pseudodirect addressing	b. Pseudodirect addressing

All Answer Choices

a. Base or displacement addressing

b. Pseudodirect addressing

c. Register addressing

d. Direct addressing

e. PC-relative addressing

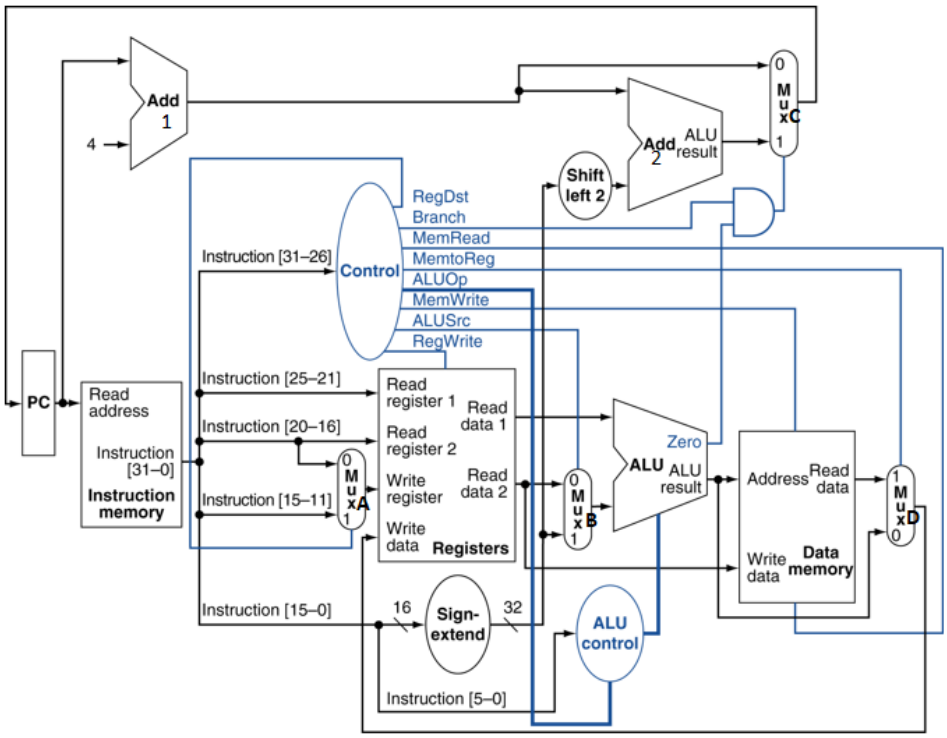
f. Indirect addressing

g. Immediate addressing

Question 12

8 out of 8 points

An (incomplete) datapath of a MIPS processor is shown in the diagram below.



Fill the table below with single character Y or N, with Y indicating that the datapath element is needed when the processor is executing the instruction in the first column.

Instruction being executed	Mux A	Sign-extender	Shift left 2	Mux B	Adder 2	ALU	Data Memory	Mux D
`lw $t0, 4($s1)`	**[ma]**	**[se]**	**[sl]**	**[mb]**	**[a2]**	**[alu]**	**[dm]**	**[md]**

Specified Answer for: ma ✓ Y

Specified Answer for: se ✓ Y

Specified Answer for: sl ✓ N

Specified Answer for: mb ✓ Y

Specified Answer for: a2 ✓ N

Specified Answer for: alu ✓ Y

Specified Answer for: dm ✓ Y

Specified Answer for: md ✓ Y

Correct Answers for: ma		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	y	
Correct Answers for: se		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	y	
Correct Answers for: sl		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	n	

Correct Answers for: mb		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	
Correct Answers for: a2		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	n	
Correct Answers for: alu		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	
Correct Answers for: dm		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	
Correct Answers for: md		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	y	

Question 13

2 out of 4 points

Given the following high level language statements:

```
unsigned int l, n, m = 8;

l = n * m;
```

Assuming `l, n` and `m` are stored in registers `$s0, $s1` and `$s2` respectively, the best MIPS instruction to be used for this calculation is:

[a] [b], [c], [d]

Specified Answer for: a ✗ mul

Specified Answer for: b ✓ $s0

Specified Answer for: c ✓ $s1

Specified Answer for: d ✗ $s2

Correct Answers for: a		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	sll	Case Sensitive
Correct Answers for: b		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	$s0	Case Sensitive
Correct Answers for: c		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	$s1	Case Sensitive
Correct Answers for: d		
Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	3	Case Sensitive

Question 14

2 out of 4 points

An (incomplete) example of MIPS exception handler is shown below.

```
    .ktext
00: excHdl:
01: # Save all of the registers that are used by the kernel.
02:    sw      $t0, _k_save_t0
03:    sw      $t1, _k_save_t1
04:    mfc0    $k0, $13                 # read the Cause register of CP_0
05:    andi    $k0, $k0, 0x7C           # note the position of Exc Code!
06:    lw      $k0, _k_JumpTable($k0)   # a clever trick is used here!
07:    jr      $k0
08:#
09:#
10: _k_IncReturn:   #
11:    mfc0  $k1, $14
12:    addi  $k1, $k1, 4
13:    mtc0  $k1, $14
```

```
14:#
15: _k_Return:    #   Restore all of the registers used by the kernel (except for $1)
16:   lw  $8, _k_save_t0
17:   lw  $9, _k_save_t1
18: # Get EPC, return from exception handling and  got back to user code
19:   mfc0  $k0, $14
20:   eret
```

Assuming that the jump table `_k_JumpTable` has following entries:

```
_k_JumpTable
      .word       0x00800010   #
      .word       0x00800070   #
      .word       0x008000A0   #
      .word       0x008000C0   #
      .word       0x008000F0   #
      .word       0x008001C0   #
      .word       0x008001F0   #
      .word       0x00800220   #
      .word       0x00800270   #
      .word       0x008002B0   #
      .word       0x008002D0   #
      .word       0x008002F0   #
      .word       0x00800310   #
      .word       0x008003C0   #
```

When the MIPS process executes the following instructions:

```
li $s0, 0x0800FF08
lw $t0, 5($s0)
```

the register `$13` of coprocessor 0 has the value 0x**[a]**, and register `$k0` at line 07: will contain 0x**[b]**.
Write the value of register `$13` as a 8-digits hexadecimal assuming that all bits other than the cause bits (bits 6-2) are 0.

Specified Answer for: a ✓ 00000010

Specified Answer for: b ✗ 0x008000F0

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	00000010	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	008000F0	

Question 15

4 out of 4 points

Similarities between ARM and MIPS ISAs include

Selected Answers:
- ✓ b. both are based on RISC (Reduced Instruction Set Computer) design.
- ✓ c. using memory mapped I/Os.

Answers:
- a. using condition codes for branching.
- ✓ b. both are based on RISC (Reduced Instruction Set Computer) design.
- ✓ c. using memory mapped I/Os.
- d. having the same number of addressing modes.

Question 16

3 out of 3 points

The last step in the process of translating a program written in a high-level language (e.g. C) into an executable program is called linking. This is done by a system program named **[a]**. There are two types of linking: **[b]** linking and **[c]** linking where an executable program created by the latter type is larger than one created by the former type.

Specified Answer for: a ✓ linker

Specified Answer for: b ✓ dynamic

Specified Answer for: c ✓ static

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	linker	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
✓ *Exact Match*	dynamic	
Correct Answers for: c		

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	static	

Question 17

6 out of 6 points

The coprocessor_0 in a MIPS processor has a set of registers used to store necessary information when an exception occurs:

```
$8      BadVaddr
$12     Status
$13     Cause
$14     EPC.
```

When a MIPS processor executes the following instructions:

Address Instruction

```
0x00401000 li    $t0, 0x7FFFF0F0
0x00401004 lw    $t0, 2($t0)
0x00401008 ...
```

the contents of these registers are:

$8: 0x**[a]**

$13 : 0x**[b]** Note: assuming all Interrupt Pending (IP) bits are 0, i.e. no interrupt pending.

$14: 0x**[c]**.

Specified Answer for: a 7ffff0f2

Specified Answer for: b 00000010

Specified Answer for: c 00401004

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *7FFFF0F2 *	
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *00000010 *	
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Pattern Match	(?i) *00401004 *	

Question 18

4.25 out of 5 points

To interact with the outside world a computer system needs to process information for input and output devices. Match the concepts used for input/output devices handling with the questions that need to be answered when processing information for input and output devices.

Question	Correct Match	Selected Match
Data registers	a. What	a. What
Control registers	a. What	a. What
Memory mapped I/O	b. Where	b. Where
Input/Output ports	b. Where	b. Where
Using lw and sw instruction to transfer data between processor and I/O devices	b. Where	f. How
Polling	c. When	c. When
Interrupts	c. When	c. When
Direct memory access	f. How	f. How
Programmed I/O	f. How	f. How
Input/Output instructions	b. Where	b. Where

All Answer Choices

a. What

b. Where

c. When

d. Who

e. Which

f. How

Question 19

3 out of 4 points

The ALU (Arithmetic Logical Unit) is an important datapath element in a MIPS processor. The ALU is used

Selected Answers:
- a. to calculate destination addresses of branching instructions.
- b. to calculate memory addresses for load/store instructions.
- d. to perform integer and floating point arithmetic operations.

Answers:
- a. to calculate destination addresses of branching instructions.
- b. to calculate memory addresses for load/store instructions.
- c. to determine the destination address of a jump instruction.
- d. to perform integer and floating point arithmetic operations.

Question 20

5 out of 5 points

The ALU (Arithmetic and Logical Unit) is an important datapath element of a MIPS processor and it performs multiple functions depending on the instruction that is being executed. Match instructions with the function to be performed by the ALU when the processor is executing that instruction.

Question	Correct Match	Selected Match
`add $s0, $t0, $t1`	g. addition	g. addition
`lw $s0, 8($t1)`	g. addition	g. addition
`bne $s0, $t0, Loop`	a. subtraction	a. subtraction
`sub $s0, $t0, $t1`	a. subtraction	a. subtraction
`and $s0, $t0, $t1`	b. AND	b. AND

All Answer Choices

a. subtraction

b. AND

c. set-on-less-than

d. NOT

e. OR

f. NOR

g. addition

Question 21

4 out of 4 points

Assuming registers of an 8-bit processor are used to store signed integers represented in the 2's complementary format, and the two 8-bit registers A and B contain 01011001 and 01000101, respectively.

If 8-bit registers H and L are used to store the result of A x B (i.e. C = A multiplied by B), with H and L contain the upper 8 bits and the lower 8 bits of the result respectively, the content of H is **[a]** and that of L is **[b]**.

Note: Answers must be in 2's complementary binary format and do not omit leading 0s. If overflow or underflow happens the answer must be OVF and UDF, respectively.

Specified Answer for: a 00010111

Specified Answer for: b 11111101

Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**

Exact Match	00010111

Correct Answers for: b

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	11111101	

Question 22

5 out of 5 points

Match exceptions that may occur in a MIPS processor with their correct name.

Question	Correct Match	Selected Match
Undefined opcode	c. trap	c. trap
Divide by zero	c. trap	c. trap
Syscall	c. trap	c. trap
Timer expiration	b. interrupt	b. interrupt
CPU temperature sensor reaches warning threshold	b. interrupt	b. interrupt

All Answer Choices

a. external event

b. interrupt

c. trap

d. external trap

Response Feedback: There is no such thing as external trap or event.

Question 23

3 out of 4 points

The code snippet below calculates the perimeter of an octagon whose sides' length is stored in the memory location labeled as **`length`** and stores the result in the memory location labeled as **`perimeter`**.

Fill the blanks to complete the code snippet such that it will run using the least clock cycles.

```
# data segment
          [x]
length:    .word 5
perimeter: .word 0
# program segment
           [y]
           lw $t0, [a]         # $t0: length
           [b] $t1, [c], [d]   # $t1: perimeter
           [z] [e], perimeter  # $t1 -> memory
# continue
```

Specified Answer for: x .data

Specified Answer for: y .text

Specified Answer for: a length

Specified Answer for: b mul

Specified Answer for: c $t0

Specified Answer for: d 8

Specified Answer for: z sw

Specified Answer for: e $t1

Correct Answers for: x

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	.data	Case Sensitive

Correct Answers for: y

Evaluation Method	Correct Answer	Case Sensitivity
Exact Match	.text	Case Sensitive
Correct Answers for: a		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	length	Case Sensitive
Correct Answers for: b		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	sll	Case Sensitive
Correct Answers for: c		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	$t0	Case Sensitive
Correct Answers for: d		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	3	
Correct Answers for: z		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	sw	Case Sensitive
Correct Answers for: e		
Evaluation Method	**Correct Answer**	**Case Sensitivity**
Exact Match	$t1	Case Sensitive

Question 24

3 out of 3 points

Considering the following MIPS assembly code snippet .

```
mydata:  .word 0x01020304, 0x05060708, 0x090A0B0C0, 0x0D0E0F10, 0xE0001211, 0xA031023A
  ...
  li   $t1, 1
  sll  $t1, $t1, 2
  lw   $s0, mydata($t1)
```

What is the value of register `$s0` after the instruction `lb` was executed? _____

Selected Answer: 0x05060708

Correct Answer:

Evaluation Method	Correct Answer	Case Sensitivity
Pattern Match	(?i)(0x)?05060708	

Friday, November 13, 2020 9:56:14 PM CST

← OK