聆思科技
LISTENAI

Register User Manual

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Update History

Version	Date	Update Description
V1.0	November 22, 2022	Initial release.

Table of Contents

1 {{ CMN_IOMUX_Name }}

1.1 Introduction

选择 GPIO 的复用功能。

1.2 Main Features

每个 GPIO 有 16 个复用功能可以配置，具体的配置功能需要参考 projectsVenusASICDigitalIP-sIOMUXVenus_IO_New.xlsx。

1.3 Function Description

1.4 Basic Block Diagram

1.5 {{ CMN_IOMUX_Name }} Register

1.5.1 Summary of {{ CMN_IOMUX_Name }} Registers

Table 1.1 shows a summary of the {{ CMN_IOMUX_Name }} registers.

Table 1.1 {{ CMN_IOMUX_Name }} Register Summary

Name	Offset	Description
{{ CMN_IOMUX_PAD_GPIOA_Name }}	{{ CMN_IOMUX_PAD_GPIOA_Offset }}	Full name
{{ CMN_IOMUX_PAD_GPIOB_Name }}	{{ CMN_IOMUX_PAD_GPIOB_Offset }}	Full name
{{ CMN_IOMUX_PAD_FLASH_WP_N_Name }}	{{ CMN_IOMUX_PAD_FLASH_WP_N_Offset }}	Full name

1.5.2 Register Description

The abbreviations for the Type column are summarized below.

- RO: read only
- RW: readable and writable

- W1C: readable and write 1 clear

{{ CMN_IOMUX_PAD_GPIOA_Name }} () ({{ CMN_IOMUX_PAD_GPIOA_Offset }})

Table 1.2 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_GPIOB_Name }} () ({{ CMN_IOMUX_PAD_GPIOB_Offset }})

Table 1.3 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_WP_N_Name }} () ({{ CMN_IOMUX_PAD_FLASH_WP_N_Offset }})

Table 1.4 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_MISO_Name }} () ({{ CMN_IOMUX_PAD_FLASH_MISO_Offset }})

Table 1.5 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_CS_N_Name }} () ({{ CMN_IOMUX_PAD_FLASH_CS_N_Offset }})

Table 1.6 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_HOLD_N_Name }} () ({{ CMN_IOMUX_PAD_FLASH_HOLD_N_Offset }})

Table 1.7 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_CLK_Name }} () ({{ CMN_IOMUX_PAD_FLASH_CLK_Offset }})

Table 1.8 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3

{{ CMN_IOMUX_PAD_FLASH_MOSI_Name }} () ({{ CMN_IOMUX_PAD_FLASH_MOSI_Offset }})

Table 1.9 XXX Register

Name	Bit	Type	Description	Reset
name 1	bit 1	type 1	description 1	reset 1
name 2	bit 2	type 2	description 2	reset 2
name 3	bit 3	type 3	description 3	reset 3