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CSK6012 Voice Recognition SoC Datasheet

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Update History

Version	Date	Update Description
V1.0	September 21, 2022	Initial release.

Table of Contents

1 Overview

The CSK6 serial is a dual-core microcontroller embedded with an ARM STAR core and a HiFi4 core. The ARM Star core is designed for 32-bit microcontroller applications, offering high performance, low power, simple instruction set and addressing together with reduced code size compared to exiting solutions. The HiFi4 core is designed for audio coders and decoders such as MP3, AAC, and FLAC. The independent NPU is designed for neural network operation.

The CSK6 serial applies for smart home appliances.

The CSK6 serial can operate up to 300 MHz. Thus it can afford to support a variety of industrial control and applications that requires high CPU performance. The CSK6 serial has an internal 1-MB data SRAM.

Many system-level peripheral functions, such as IO port, DVP, timer, watchdog timer, UART, SPI, I2C, DMA, PLL, USB1.1 (full speed), RTC, and SDIO are supported.

2 Block Diagrams

For the block diagrams, see *Fig. 2.1*.

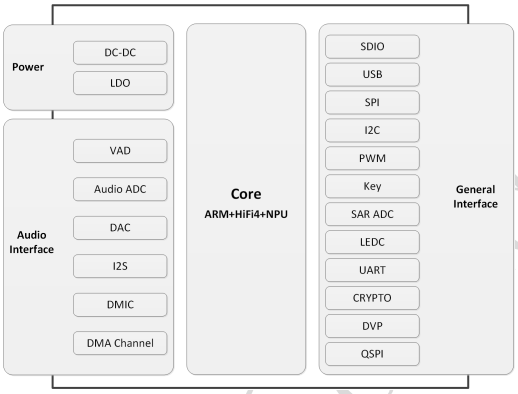


Fig. 2.1 Block Diagram

3 Pin Mapping and Descriptions

3.1 Pin Mapping

For the pin mapping diagram, see *Fig. 3.1*.

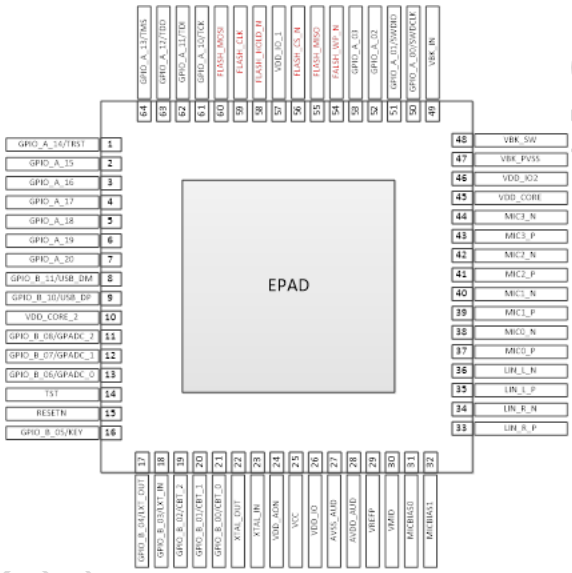


Fig. 3.1 Pin Mapping Diagram

3.2 Pin Descriptions

For pin descriptions, refer to *Table 3.1*.

Table 3.1 Pin Descriptions

Pin Number	Pin Name	Description
1	GPIO_A_14	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
2	GPIO_A_15	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions, (Boot ROM UART programming pin)
3	GPIO_A_16	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions

Continued on next page

Table 3.1 – continued from previous page

Pin Number	Pin Name	Description
4	GPIO_A_17	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
5	GPIO_A_18	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions, (Boot ROM UART programming pin)
6	GPIO_A_19	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
7	GPIO_A_20	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
8	GPIO_B_11/USB_DM	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
9	GPIO_B_10/USB_DP	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
10	VDD_CORE_2	Should connect with VDD_CORE
11	GPIO_B_08/GPADC_2	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
12	GPIO_B_07/GPADC_1	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
13	GPIO_B_06/GPADC_0	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
14	TST	Test pin, default pull up. 0: test mode 1: normal mode
15	RESETN	Reset pin input, default pull up
16	GPIO_B_05/KEYSENSE	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
17	GPIO_B_04	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
18	GPIO_B_03	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
19	GPIO_B_02/CBT_2	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
20	GPIO_B_01/CBT_1	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
21	GPIO_B_00/CBT_0	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
22	XTAL_OUT	24 MHz crystal
23	XTAL_IN	24 MHz crystal
24	VAD_AON	Internal LDO output. 1 μF cap recommended

Continued on next page

Table 3.1 – continued from previous page

Pin Number	Pin Name	Description
25	VCC	Power input: 2.7 V-5.5 V
26	VDD_IO	Internal LDO output, 4.7 μF cap recommended
27	AVSS_AUD	GND
28	AVDD_AUD	Internal LDO output, 2.2 μF cap recommended
29	VREF	Audio codec reference input
30	VMID	Internal LDO output, 4.7 μF cap recommended
31	MICBIAS0	Mic bias output, Cload=2.2 μF
32	MICBIAS1	Mic bias output, Cload=2.2 μF
33	LIN_R_P	LINE right channel differential outputs positive
34	LIN_R_N	LINE right channel differential outputs negative
35	LIN_L_P	LINE left channel differential outputs positive
36	LIN_L_N	LINE left channel differential outputs negative
37	MIC0_P	Mic input positive
38	MIC0_N	Mic input negative
39	MIC1_P	Mic input positive
40	MIC1_N	Mic input negative
41	MIC2_P	Mic input positive
42	MIC2_N	Mic input negative
43	MIC3_P	Mic input positive
44	MIC3_N	Mic input negative
45	VDD_CORE	internal LDO output, 4.7 μF cap recommended, should connect with VDD_CORE_2
46	VDD_IO2	Internal DC-DC input, 10 μF cap recommended
47	VBK_PVSS	DC-DC GND
48	VBK_SW	DC-DC switch out, 3.3 μH inductor connected
49	VBK_IN	DC-DC input power: 2.7 V-5.5 V
50	GPIO_A_00/SWDCLK	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
51	GPIO_A_01/SWDTMS	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
52	GPIO_A_02	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
53	GPIO_A_03	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
54	FLASH_WP_N	Connect with external QSPI Flash
55	FLASH_MISO	Connect with external QSPI Flash
56	FLASH_CS_N	Connect with external QSPI Flash
57	VDD_IO_1	Input power connect with VDD_IO
58	FLASH_HOLD_N	Connect with external QSPI Flash
59	FLASH_CLK	Connect with external QSPI Flash

Continued on next page

Table 3.1 – continued from previous page

Pin Number	Pin Name	Description
60	FLASH_MOSI	Connect with external QSPI Flash
61	GPIO_A_10	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
62	GPIO_A_11	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
63	GPIO_A_12	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
64	GPIO_A_13	Multi-Purpose Digital I/O, please refer to the 60XX_IOMUX.xlsx for the detailed functions
65	EPAD	Connect with GND

Note: The pull up resister is configured as 80 K.

4 Functions

4.1 Core

- The ARM STAR&HiFi4 dual-core operates up to 300 MHz.
- Independent NPU.
- Hardware multiplier and hardware divider.
- The embedded debug module supports the serial debug port (2-wire) and the JTAG debug port (4-wire).

4.2 Memory

- External flash through the QSPI interface.
- Totally 1088-KB SRAM shared by ARM and HiFi4 cores.
- Dedicated 96-KB SRAM for the NPU block.

4.3 Clock Control

- Programmable system clock source.
- External 24-MHz high-speed crystal input to provide reference clock for the system.
- Internal 32-KHz low-speed oscillator with calibration.
- The PLL allows CPU operation up to 300 MHz with the system oscillator.

4.4 IO Port

- Up to 32 GPIO pins.
- GPIO configuration.
- Quasi-bidirectional (pull-up enabled).
- Pull-down.
- Push-pull (output).
- Input only (high-impedance).
- An I/O pin can be configured as an interrupt source through edge/level configuration.
- Flexible IO function selection.
- 5-V tolerance IO for GPIOA.

4.5 GPT

The multi-function timer provides the following 6 usage scenarios depending on the configuration of the channel mode register bit. The maximum output frequency of the PWM is 50 MHz.

- Timer mode
  Support 8/16/32-bit timers
- Input capture mode
  The capture count mode is used to capture the number of input pulses and the capture time mode is used to capture pulse width.
- PWM mode
  PWM can be configured as central-aligned mode (see *Fig. 4.1*) and edge-aligned mode (see *Fig. 4.2*).

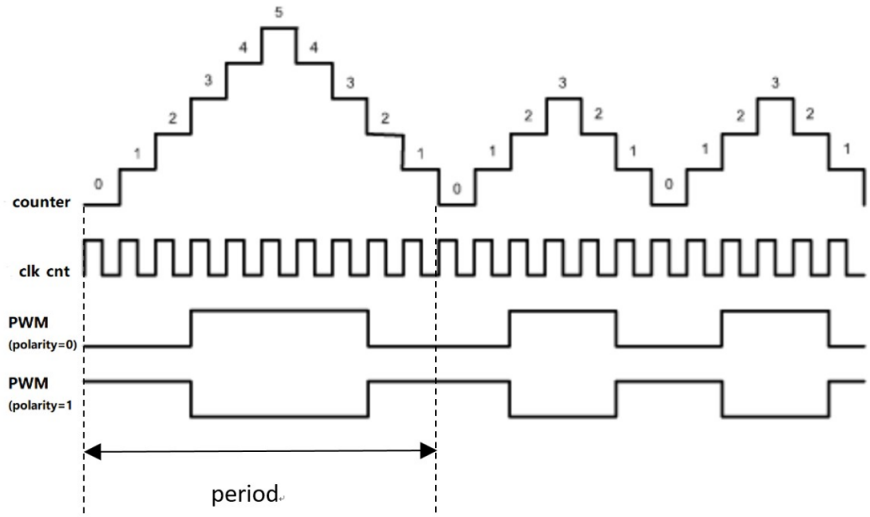


Fig. 4.1 Center-Aligned Mode

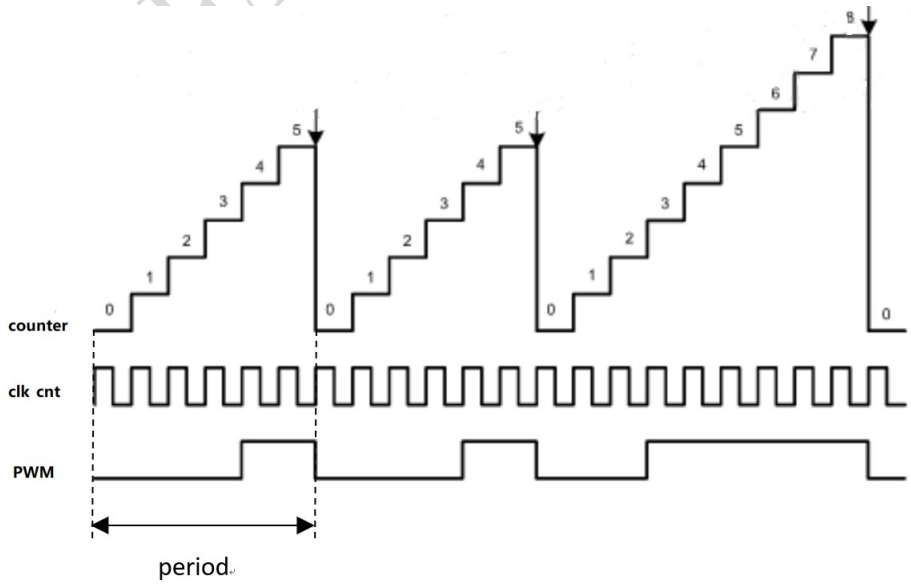


Fig. 4.2 Edge-Aligned Mode

- LEDC output mode

4.6 SAR ADC

- 12-bit resolution, up to 3 channels, up to 1 Msps, 24-MHz ADC clock
- Configurable hardware ADC trigger sources
- User configurable n-times ADC sampling
- Dedicated ADC data FIFO for each ADC channel
- Configurable ADC sampling duration
- Configurable waiting time for the next round of A/D conversion
- Switch on/off control
- ADC trimming
- ADC channel selection
- External/internal VREF selection
- Real voltage caculation:
  Reg_{adc_value} = ADC register value
  Voltage = (Reg_{adc_value} - 2048)/2048*3.3

4.7 Audio Codec

- Audio sample rates support 8 KHz to 96 KHz in the playback (DAC) path.
- Audio sample rates support 8 KHz, 16 KHz, 44.1 KHz, or 48 KHz in the record (ADC) path.
- DAC SNR about 95 dB, THD -85 dB ('A'-weighted @ 8-48 ks/s).
  ADC SNR about 95 dB, THD -85 dB ('A'-weighted @ 8-48 ks/s).
- 32-bit APB control interface to ADC01 separately.
- 32-bit APB control interface to ADC23 and DAC01 separately.
- Programmable gain setting and soft mute control in the digital part.
- Programmable ALC loop/noise Gate setting in the ADC path.
  Programmable ADC high-pass filter (wind noise reduction included).
  The programmable ADC notch filter is selectable.
- ADC01 and ADC23 support two stereo digital microphones.
- Output gain/volume and mute control.

4.8 DVP

- Designed as an AHB master component that can access the memory without any DMAC service.
- Image frame completion notice and buffer switching.
- Support separate components 4:2:2 output format in the line buffer for JPEG encoding.

4.9 IWDG

- Clocked from an internal 32-KHz low-speed oscillator or from a 32768-Hz crystal if available.
- 32-bit free-running counter.

- Selectable timer-out interval.

4.10 UART

- Four UART interfaces (1 for debug).
- Three UARTs support hardware flow control (CTS/RTS) so that WiFi can be supported through UART interfaces.
- UART0 to UART2 support the hardware handshake for DMA.
- Up to 3-Mb/s baudrate settting.

4.11 SPI

- Three SPI interfaces.
- Maximumly 50 Mb/s for the master mode.
- Maximumly 25 Mb/s for the slave mode.
- One SPI of QSPI function must be used for the embedded NOR flash or the external flash.
- Supports the master mode and the slave mode.
- Supports memory mapped access (read-only) through the AHB bus.
- Supports the hardware handshake for DMA.
- Supports the dual I/O and quad I/O modes (QSPI).

4.12 I2C

- Two I2C interfaces are available.
- Programmable to be a master or a slave device.
- Programmable clock/data timing.
- Supports the I2C-bus standard-mode (100 kb/s), fast-mode (400 kb/s), and fast-mode plus (1 Mb/s).
- Supports the hardware handshake for DMA.
- Supports the master-transmit, master-receive, slave-transmit and slave-receive modes.
- Supports the multi-master mode.
- Supports 7-bit and 10-bit addressing.
- Supports general call addressing.
- Supports auto clock stretch.

4.13 RTC

- Supports software compensation by setting the frequency compensation register.
- The frequency of the clock source (before the clock divider) for the counter is 32.768 KHz.
- Separate second, minute, hour, and day counters.

- Periodic interrupts: half-second, second, minute, hour, and day interrupts.
- Programmable alarm interrupt with specified second, minute, and hour numbers.

4.14 NPU

- Matrix and vector operation accelerator.
- AHB master interface for data read and write.
- APB interface for register configuration
- Has interrupt signals
- Support reverse order storage, overflow detection, and location shift

4.15 FCC RAM Controller

- 200 MHz maximumly.
- Arbitrate the data access request from the CPU, HiFi4, NPU, and DMAC.
- Partition the NPU memory into several spaces.
- If the accesses from different agents are in different spaces, all of them can be done without immediately.
- Flexible priority setting: If the accesses from different agents are in the same space, the priority can be set by users through the register.

4.16 PDM2PCM

- Support data conversion of PDM data from digital microphone to standard PCM data.
- CIC filter in the always-on domain, half-band and memory in main power domain.

4.17 CRYPTO

- Support inside chip AES128 + SHA256 for secure communication.
- AHB master interface for data read and write.
- APB interface for register configuration.

4.18 eFuse Controller

- Read eFuse content after receiving reset release signal from the reset sequence control.
- Provide data to Crypto engine for encryption/decryption.
- Provide data to QSPI encryption wrapper to protect the content of the NOR flash.

4.19 True Random Number Generator

- True random generator with mixed analog digital implementation to provide true random numbers.
- Register configuration and generated random numbers can be accessed through the APB bus.

4.20 I2S Interface

- Support extended microphone inputs.
- Support I2S audio inputs and outputs.
- 3 independent I2S modules.
- Input or output signal can be TDM extended.
- Register configuration and data operation through the APB bus.

4.21 USB1.1 Full Speed Device

- One set of USB 1.1 FS Device 12 Mbps.
- On-chip USB Transceiver.
- Supports Control, ISO in/out, Bulk in/out, Interrupt in/out transfers.
- Provides 8 programmable endpoints.
- Supports maximum 1K Bytes for isochronous transfer and maximum 64 Bytes for Bulk and interrupt transfer.
- Each endpoint is configurable.

4.22 SDIO

- Maxim 25 MHz output clock
- Compliant with SD host controller standard specification, version 3.0.
- Supports both DMA and non-DMA data transfers.
- Compliant with SD physical layer specification, version 3.0.
- Supports UHS50/UHS104 SD cards.
- Supports configurable SD bus modes: 4-bit mode and 8-bit mode.
- Compliant with SDIO card specification, version 3.0.
- Compliant with eMMC card specification, version 5.1 mandatory part.
- Supports configurable 1-bit/4-bit SD card bus and 1-bit/4-bit/8-bit EMMC card bus.
- Configurable CPRM function for security.
- Built-in generation and check for 7-bit and 16-bit CRC data.
- Card detection (Insertion/Removal).

4.23 Power Management Unit

- Supports Sleep mode to reduce power consumption.
- Supports the wake up through RTC, timer and Key-in from IO.
- Supports the wake up through VAD.
- Supports system wakeup through touch.

4.24 Touch

- Supports touch point detection.

4.25 Audio ADC&DMIC&I2S

- Audio ADC shares the internal memory with DMIC and I2S. For the restrictions on combination use, refer to *Table 4.1*.

Table 4.1 Restrictions on Combination Use

Occupied ADC/DAC	Available I2S	Available DMIC	Description
ADC01 only, no DAC	I2S1, I2S2	DMIC2, DMIC3	
ADC23 only, no DAC	I2S0, I2S1 or I2S2	DMIC0, DMIC1	I2S1 or I2S2 (either-or)
ADC01+ADC23, no DAC	I2S1 or I2S2	None	I2S1 or I2S2 (either-or)
ADC01 only, with DAC	I2S0, I2S2(IN)	DMIC2, DMIC3	I2S2(IN)
ADC23 only, with DAC	I2S0, I2S1 or I2S2(IN)	DMIC0, DMIC1	I2S1 or I2S2(IN) (either-or)
ADC01+ADC23, with DAC	I2S1 or I2S2(IN)	None	I2S1 or I2S2(IN) (either-or)

4.26 Boot Mode

For descriptions of GPIOB0 and GPIOB1 the boot modes, refer to *Table 4.2*.

Table 4.2 Boot Mode

GPIOB0	GPIOB1	Mode Description
1	1	NOR flash boot
1	0	UART
0	1	Reserved
0	0	DSP boot only

- GPIOA15(RXD) & GPIOA18(TXD) are configured as UART function in the UART boot mode.

5 Electrical Characteristics

5.1 Parameter Conditions

Unless otherwise specified, all voltages are referenced to VSS.

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at 25 °C and the maximum temperature in the range.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm$ 3σ).

5.1.2 Typical Values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{CCIN} = 5 V (for the 2.7 V V_{CCIN} 5 V voltage range). They are given only as design guidelines and are not tested.

5.1.3 Loading Capacitor

The loading capacitor used for pin parameter measurement is 10 pf.

5.1.4 Pin Input Voltage

The input voltage measurement on a pin of the device is through current source device.

5.2 Operating Conditions

5.2.1 Absolute Maximum Ratings

For information about voltage characteristics, refer to *Table 5.1*.

Table 5.1 Voltage Characteristics

Symbol	Ratings	Min	Max	Unit
V_{CCIN}-V_{SS}	External supply voltage	-0.3	5.5	V
V_{IL}	Input Low Voltage on signal pin	-0.3	0.8	V
V_{IH}	Input High Voltage on signal pin (PortA)	2	5.5	V
V_{IH}	Input High Voltage on signal pin (PortB)	2	3.6	V
V_{OL}	Output Low Voltage on signal pin		0.4	V
V_{OH}	Output High Voltage on signal pin	2.4		V

5.2.2 I/O Port Characteristics

For information about I/O Static characteristics, refer to *Table 5.2*.

Table 5.2 I/O Static Characteristics

Sym-bol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO Input low level voltage	2.7 V V_{CCIN} 5.5 V T_A=25 °C	-0.3		0.8	V
V_{IH}	Standard IO input high level voltage(PortA)	2.7 V V_{CCIN} 5.5 V T_A=25 °C	2		5.5	V
V_{IH}	Standard IO input high level voltage(PortB)	2.7 V V_{CCIN} 5.5 V T_A=25 °C	2		3.6	V
V_{hys}	Standard IO Schmitt trigger voltage hysteresis	2.7 V V_{CCIN} 5.5 V T_A=25 °C		220		mV
V_{OL}	Output Low Voltage	2.7 V V_{CCIN} 5.5 V T_A=25 °C			0.4	V
V_{OH}	Output High Voltage	2.7 V V_{CCIN} 5.5 V T_A=25 °C	2.4			V
I_{OL}	Low Level Output Current	2.7 V V_{CCIN} 5.5 V T_A=25 °C		15		mA
I_{OH}	High Level Output Current	2.7 V V_{CCIN} 5.5 V T_A=25 °C		22		mA
I_{Ikg}	Input leakage current	2.7 V V_{CCIN} 5.5 V T_A=25 °C		1		uA
R_{PU}	Pull up equivalent resistor		74 k	80 k	158 k	Ω
R_{PD}	Pull down equivalent resistor		62 k	75 k	203 k	Ω
C_{IO}	I/O pin capacitance			5		pF

Note: Only PORT A is 5V tolerance IO, and the input voltage can be 5.5V maximumly.

5.2.3 IO AC Characteristics

For information about I/O AC characteristics, refer to *Table 5.3*.

Table 5.3 IO AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$F_{max(io)out}$	Maximum frequency	2.7 V V_{CCIN} 5.5 V T_A=25 °C, C_L=10 pf		100		MHz
$T_{f(IO)out}$	Output high to low level fall time and output low to high level rise time	2.7V V_{CCIN} 5.5V T_A=25 °C, C_L=10 pf		2.5		ns
		2.7 V V_{CCIN} 5.5 V T_A=25 °C, C_L=10 pf		2.5		ns

5.2.4 nRESET Pin Characteristics

For information about nRESET pin characteristics, refer to *Table 5.4*.

Table 5.4 nRESET Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Pull up equivalent resistor	2.7 V V_{CCIN} 5.5 V T_A=25 °C		80 k		Ω
$V_{(nRESET)}$	nRESET input pulse	2.7 V V_{CCIN} 5.5 V T_A=25 °C, C_L= 10 pf		1		ms

5.2.5 Supply Current Characteristics

For information about supply current characteristics, refer to *Table 5.5*.

Table 5.5 Supply Current Characteristics

Symbol	Parameter	Conditions	f_{sysclk}(MHz)	Typical	Unit
I_{DD}	Supply current in RUN mode	V_{CCIN} = 5 V, external 24 MHz T_A=25 °C, PLL ON, AP ON, CP ON, NPU ON PSRAM off, NOR flash cached	100	20	mA
	Supply current in VAD& DEEP-SLEEP mode	T_A= 25 °C, deep sleep mode entered, VAD mode enabled with 1 audio ADC on (analog mic not included)	24	1.8	mA
	Supply current in DEEP-SLEEP mode	T_A= 25 °C, deep sleep mode entered	24	700	uA

5.2.6 Wakeup Time from Sleep Modes

For information about wakeup time from sleep modes, refer to *Table 5.6*.

Table 5.6 Wakeup Time from Sleep Modes

Symbol	Parameter	Conditions	Typical	Unit
$t_{WUSLEEP}$	Wakeup from Sleep	External pin wakeup (ROM boot not included)	< 2	ms

5.2.7 External Clock Source Characteristics

For information about external clock source characteristics, refer to *Table 5.7*.

Table 5.7 External Clock Source Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{osc}	External clock source frequency			24		MHz
V_{OSCH}	OSC IN input pin high level voltage			3.3		V
V_{OSCL}	OSC IN input pin low level voltage			0		V
$C_{IN(OSC)}$	OSC IN input capacitance			5		pF
Ducy $_{(OSC)}$	Duty cycle		45		55	%
I_L	OSC IN input leakage current			430		uA

5.2.8 Internal Clock Source Characteristics

For information about internal clock source characteristics, refer to *Table 5.8*.

Table 5.8 Internal Clock Source Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Frequency	2.7 V V_{CCIN} 5.5 V T_A=25 °C		32		KHz
$t_{su(LSI)}$	LSI oscillator startup time	2.7 V V_{CCIN} 5.5 V T_A=25 °C		5		s
$I_{DD(LSI)}$	LSI oscillator power consumption	2.7 V V_{CCIN} 5.5 V T_A=25 °C			1	uA

5.2.9 PLL Characteristics

For information about PLL characteristics, refer to *Table 5.9*.

Table 5.9 PLL Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock			24		MHz
f_{PLL_OUT}	PLL output clock			300		MHz
Jitter	Cycle-to cycle jitter			10		ps

5.2.10 EMC

For information about Electromagnetic Compatibility (EMC), refer to *Table 5.10*.

Table 5.10 EMC??

Symbol	Ratings	Conditions	Class	Maximum Value	Unit
VESD (HBM)	Elec trostatic discharge voltage (human body model)	T_A = 25 °C	2	2000	V
VESD (CDM)	Elec trostatic discharge voltage (charge device model)	T_A = 25 °C		1000	V

6 Package Information

6.1 QFN64 (8*8mm) Package Information

For the package information, see *Fig. 6.1*, *Fig. 6.2*, and *Figure 6-3*.

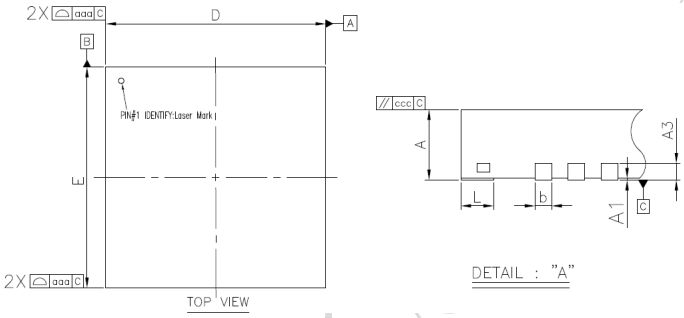


Fig. 6.1 Top View

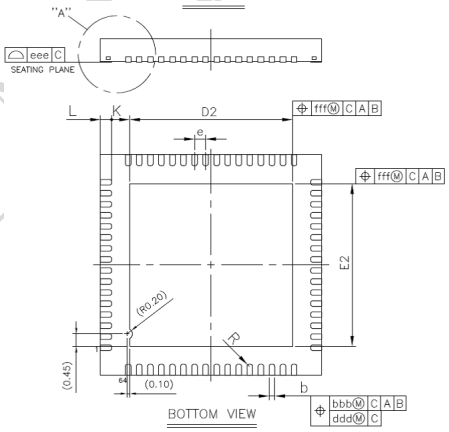
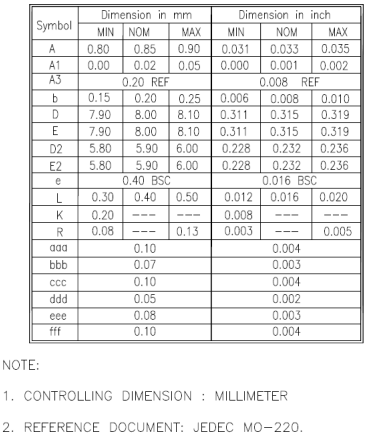


Fig. 6.2 Bottom View



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.20 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	7.90	8.00	8.10	0.311	0.315	0.319
E	7.90	8.00	8.10	0.311	0.315	0.319
D2	5.80	5.90	6.00	0.228	0.232	0.236
E2	5.80	5.90	6.00	0.228	0.232	0.236
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.08	---	0.13	0.003	---	0.005
aaa	0.10			0.004		
bbb	0.07			0.003		
ccc	0.10			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		
fff	0.10			0.004		

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Fig. 6.3 Symbol Dimension

6.2 Thermal Characteristics

The maximum chip junction temperature ($T_J$max) in degrees Celsius can be calculated through the following equation:

```
T_J max = T_A max + (P_D max * \theta_{JA})
```

where:

- $T_A$max is the maximum ambient temperature in °C.
- θ_{JA} is the package junction-to-ambient thermal resistance in °C/W.
- $P_D$max is the sum of P_{INT}max and $P_{I/O}$max ($P_D$max = P_{INT}max + $P_{I/O}$max).
- P_{INT}max is the product of I_{DD} and V_{DD} in Watts. This is the maximum chip internal power.

$P_{I/O}$max represents the maximum power dissipation on output pins and can be calculated through the following equation:

The actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the I/Os at low and high levels in the application are taken into account.

Table 6.1 Package Thermal Characteristics

Symbol	Parameter	Value	Unit
θ_{JA}	Thermal resistance junction-ambient QFN64 – 8*8 mm	28	°C/W
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	°C

7 Reflow Profile

7.1 Reflow Diagram

For the reflow diagram, see *Fig. 7.1*.

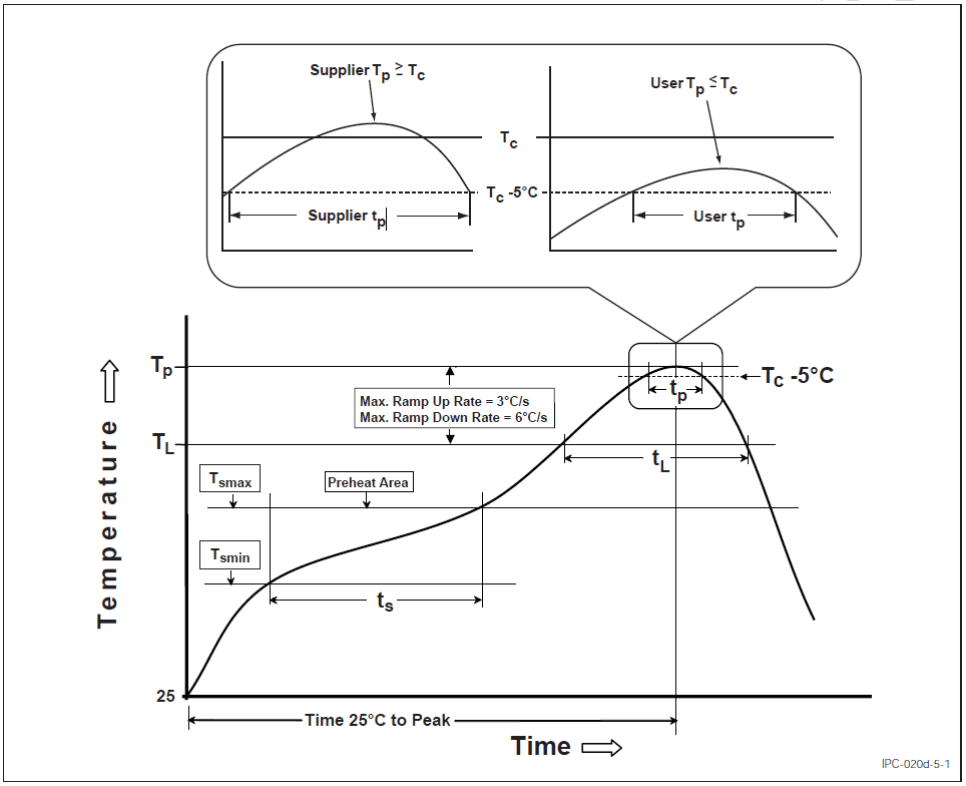


Fig. 7.1 Reflow Diagram

7.2 SMT Reflow Conditions

Table 7.1 Title?

Parameter	Requirement
N2 purge reflow usage	Yes
O2 ppm level	< 1500 ppm
Temperature Min (T_{smin})	150 °C
Temperature Max (T_{smax})	200 °C
Time (t_s)from(T_{smin} to T_{smax})	60-120 seconds
Ramp-up rate (T_L to T_P)	3 °C/second maximumly
Liquidous temperature (T_L)	217 °C
Time(t_L) maintained above T_L	60-150 seconds
Peak package body temperature (T_P)	Tp must not exceed the Classification temp (T_C) in table below
Time(t_p)within 5 °C of the specified classification temperature (T_C)	30 seconds maximumly
Ramp-down rate (T_P to T_L)	6 °C/second maximumly
Time 25 °C to peak temperature	8 minutes maximumly

Table 7.2 Title?

Package Thickness	Volume mm3 < 350	Volume mm3 350-2000	Volume mm3 > 2000
< 1.6 mm	260 °C	260 °C	260 °C
1.6 mm-2.5 mm	260 °C	250 °C	245 °C
> 2.5 mm	250 °C	245 °C	245 °C

8 Weight

The SoC weighs 200 mg.

9 Application Diagram

For the application diagram, see *Fig. 9.1*.

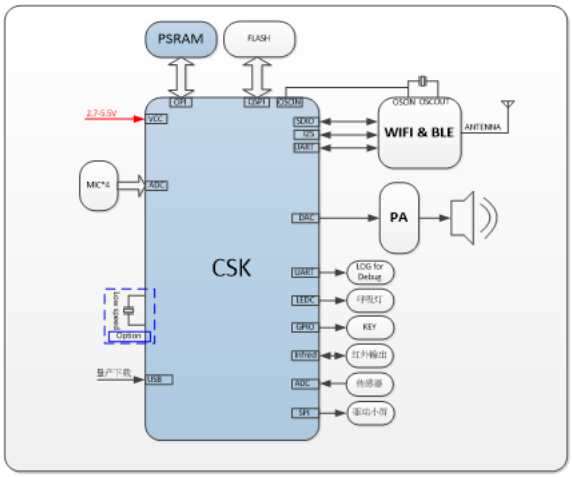


Fig. 9.1 Application Diagram