

**6001 User Manual**

Security: Medium

Version 0.2 2021.05.8

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# 版本记录

|  |  |  |
| --- | --- | --- |
| Version | Description | Owner |
| 0.1 | Create new version |  |
| 0.2 | 添加除了购买的IP之外的自研模块的内容 |  |

# 目录

# {{ CMN\_IOMUX\_Name }}

## Introduction

选择GPIO的复用功能

## Main Features

每个GPIO有16个复用功能可以配置，具体的配置功能需要参考

projects\Venus\ASIC\Digital\IPs\IOMUX\Venus\_IO\_New.xlsx

## Function Description

## Basic Block Diagram

## {{ CMN\_IOMUX\_Name }} Register

### {{ CMN\_IOMUX\_PAD\_GPIOA\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_GPIOA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_GPIOA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_GPIOB\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_GPIOB\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_GPIOB\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_WP\_N\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_WP\_N\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_WP\_N\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_MISO\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_MISO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_MISO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_CS\_N\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_CS\_N\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_CS\_N\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_HOLD\_N\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_HOLD\_N\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_HOLD\_N\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_CLK\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_CLK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_CLK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_IOMUX\_PAD\_FLASH\_MOSI\_Name }}

Offset: {{ CMN\_IOMUX\_PAD\_FLASH\_MOSI\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_IOMUX\_PAD\_FLASH\_MOSI\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CMN\_SYSCTRL\_Name }}

## Introduction

系统控制单元配置了描述整个系统时钟频率以及每个模块的时钟选择。

## Main Features

系统的外部时钟源只有两个，外部32768Hz是可选的，内部有低频RC晶体32KHz

### 外部高频时钟

24MHz晶体是必须的

### 外部低频时钟

32768Hz是可选时钟，如果没有这个时钟，可以选择内部RC32K做为低频时钟

### 内部低频时钟

内部低频RC晶体32KHz

### 两个PLL模块

芯片内共有两个PLL模块，分别对应SYSPLL和AUDPLL，这两个PLL的最大差

异是：

(1)SYSPLL可以产生USB所需要的60MHz时钟

(2)AUDPLL可以生成音频Codec所需要的时钟22.05M，用来支持特殊的采样率入44.1K的需求

这两个PLL产生的其他可用于SYSTEM，PSRAM，Flash的时钟都可以针对对应的模块来选择。

### CBUTTON的时钟

CBUTTON模块的时钟是由其内部产生的，和外部的时钟源无关，用户不用去设置。

## Function Description

时钟区域主要分为下面的几个大的模块，在下一个章节中用不同的颜色来表示

### AP与AP对应的外设

框图中的蓝色表示，其中对应的模块有：



### CP与CP对应的外设

框图中的粉红色表示，其中对应的模块有：



### CMN双核共用对应的外设

框图中的粉红色表示，其中对应的模块有：



### Always On区域对应的外设

框图中的绿色表示，其中对应的模块有：



## Basic Block Diagram



## {{ CMN\_SYSCTRL\_Name }} Register

### {{ CMN\_SYSCTRL\_AON\_WAIT\_XTAL\_Name }}

Offset: {{ CMN\_SYSCTRL\_AON\_WAIT\_XTAL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AON\_WAIT\_XTAL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_TEST\_CTRL\_Name }}

Offset: {{ CMN\_SYSCTRL\_TEST\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_TEST\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_CP\_CTRL1\_Name }}

Offset: {{ CMN\_SYSCTRL\_CP\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_CP\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_SW\_RESET2\_Name }}

Offset: {{ CMN\_SYSCTRL\_SW\_RESET2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_SW\_RESET2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CTRL1\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CTRL2\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CTRL3\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CTRL3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CTRL3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CTRL4\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CTRL4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CTRL4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_CORE\_CLK\_CFG\_Name }}

Offset: {{ CMN\_SYSCTRL\_CORE\_CLK\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_CORE\_CLK\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_BUS\_CLK\_CFG\_Name }}

Offset: {{ CMN\_SYSCTRL\_BUS\_CLK\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_BUS\_CLK\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_NVM\_CLK\_CFG\_Name }}

Offset: {{ CMN\_SYSCTRL\_NVM\_CLK\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_NVM\_CLK\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_UART\_SDIO\_CLK\_Name }}

Offset: {{ CMN\_SYSCTRL\_UART\_SDIO\_CLK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_UART\_SDIO\_CLK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_UART\_CLK\_CFG\_Name }}

Offset: {{ CMN\_SYSCTRL\_UART\_CLK\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_UART\_CLK\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_SPI\_CLK\_CFG\_Name }}

Offset: {{ CMN\_SYSCTRL\_SPI\_CLK\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_SPI\_CLK\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_MISC\_CLK\_CFG1\_Name }}

Offset: {{ CMN\_SYSCTRL\_MISC\_CLK\_CFG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_MISC\_CLK\_CFG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_MISC\_CLK\_CFG2\_Name }}

Offset: {{ CMN\_SYSCTRL\_MISC\_CLK\_CFG2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_MISC\_CLK\_CFG2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_SW\_RESET\_AP\_Name }}

Offset: {{ CMN\_SYSCTRL\_SW\_RESET\_AP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_SW\_RESET\_AP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_SW\_RESET\_CP\_Name }}

Offset: {{ CMN\_SYSCTRL\_SW\_RESET\_CP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_SW\_RESET\_CP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_SW\_RESET\_NPU\_Name }}

Offset: {{ CMN\_SYSCTRL\_SW\_RESET\_NPU\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_SW\_RESET\_NPU\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_CP\_CTRL2\_Name }}

Offset: {{ CMN\_SYSCTRL\_CP\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_CP\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG0\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CRYPTO\_CFG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_CP2AP\_INTE\_Name }}

Offset: {{ CMN\_SYSCTRL\_CP2AP\_INTE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_CP2AP\_INTE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_CP2AP\_INTS\_Name }}

Offset: {{ CMN\_SYSCTRL\_CP2AP\_INTS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_CP2AP\_INTS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG1\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CRYPTO\_CFG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG2\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CRYPTO\_CFG2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG3\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CRYPTO\_CFG3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG4\_Name }}

Offset: {{ CMN\_SYSCTRL\_AP\_CRYPTO\_CFG4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_SYSCTRL\_AP\_CRYPTO\_CFG4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CMN\_MAILBOX\_Name }}

## Introduction

MailBox是一个用于多核间通信的模块，可通过对MailBox寄存器配置，在多个核之间发送中断并传输数据，完成多核之间的通信和协作。

## Main Features

* AMBA APB4.0 Slave接口
* 两个中断输出信号
* 每个中断输出分别具有16个优先级一样的中断可配置
* 有两组分别4个总共8个32bit数据寄存器
* 具有Lock功能，可将数据寄存器Lock

## Function Description

该节描述了如何使用Mailbox中断发送和清除，以及中断的屏蔽和数据锁存的工作原理。该章节出现的带“\_x”的信号和带“N”的寄存器描述均表示（0-15）共16个中断对应的序号。

### AP-to-CP Interrupt

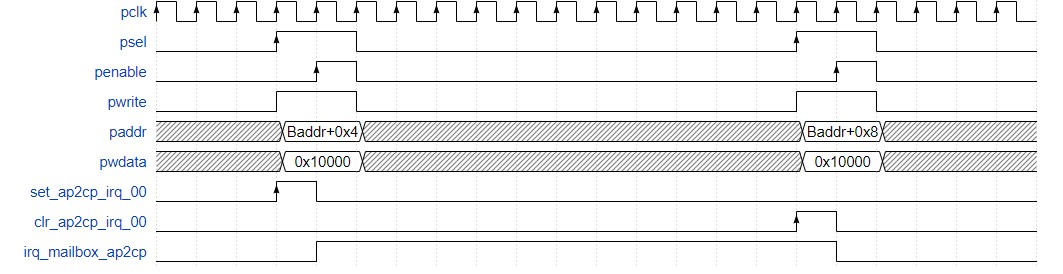
AP-to-CP中断由AP侧的Core发起，AP Core通过写AP\_MAILBOX\_CTRL寄存器[31:16]第n位发送对应序号（n-16）的中断，发送中断之前需要确保对应的中断没有被屏蔽。如果需要携带信息，须提前往AP\_DATA寄存器写入数值。待CP侧接收到中断之后，从AP\_DATA寄存器读取数据，然后查询AP\_MAILBOX\_IRQ获取mailbox内的中断号，并往对应的位写1对中断进行清除。AP-to-CP中断时序如下图：

Figure 2 AP-to-CP中断的产生和清除

由上图可知，AP Core写AP\_MAILBOX\_CTRL. ap2cp\_set\_irq\_N，产生一个set\_ap2cp\_irq\_x的脉冲，下一个时钟周期产生irq\_mailbox\_ap2cp中断;CP Core接收到中断，通过读AP\_MAILBOX\_IRQ寄存器查询Mailbox内部中断号，往对应的位写1产生了一个clr\_ap2cp\_irq\_x的脉冲，irq\_mailbox\_ap2cp中断在该脉冲出现的下一个时钟周期被清除。

### CP-to-AP Interrupt

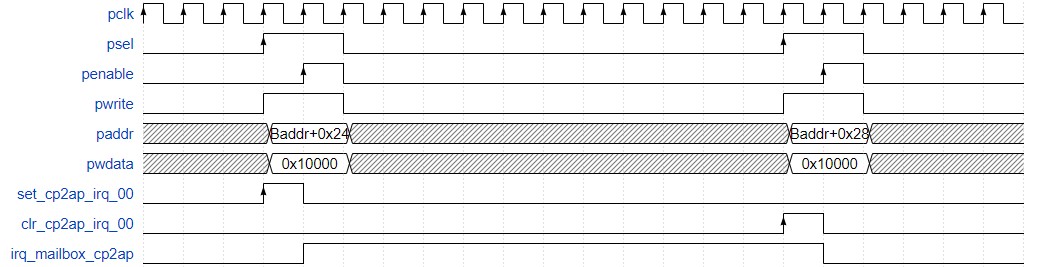
CP-to-AP中断由CP侧的Core发起，CP Core通过写CP\_MAILBOX\_CTRL寄存器[31:16]第n位发送对应序号（n-16）的中断，发送中断之前需确保对应的中断没有被屏蔽。如果需要携带信息，须提前往CP\_DATA（0-3）寄存器写入数值。待AP侧接收到中断之后，从CP\_DATA寄存器读取数据，然后查询CP\_MAILBOX\_IRQ获取mailbox内的中断号，并往对应的位写1对中断进行清除。CP-to-AP中断时序如下图：

Figure 3 CP-to-AP中断的产生和清除

由上图可知，CP Core写CP\_MAILBOX\_CTRL. cp2ap\_set\_irq\_N，产生一个set\_cp2ap\_irq\_x的脉冲，下一个时钟周期产生irq\_mailbox\_cp2ap中断;AP Core接收到中断，通过读CP\_MAILBOX\_IRQ寄存器查询Mailbox内部中断号，往对应的位写1产生了一个clr\_cp2ap\_irq\_x的脉冲，irq\_mailbox\_cp2ap中断在该脉冲出现的下一个时钟周期被清除。

### Mailbox interrupt mask

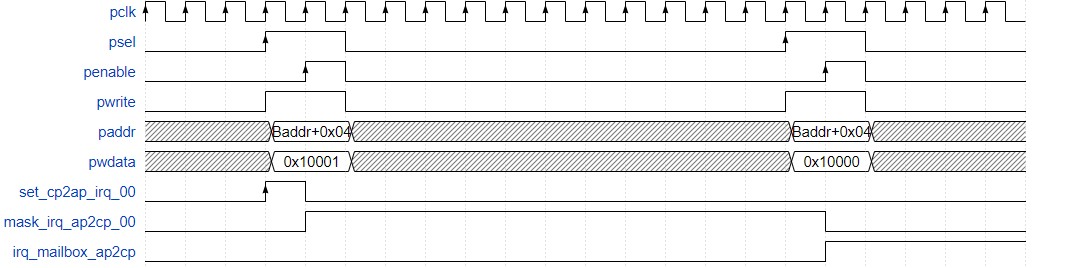
AP-to-CP中断和CP-to-AP中断均支持Mask，通过往AP\_MAILBOX\_CTRL寄存器[15:0]写1可以屏蔽AP-to-CP对应序号的中断；往CP\_MAILBOX\_CTRL寄存器[15:0]写1可以屏蔽CP-to-AP对应序号的中断。原理如下图所示：

Figure 4 Mailbox Interrupt Mask

由图1-4可知，当mask\_ap2cp\_irq\_x为高电平的时候，set\_ap2cp\_irq\_x脉冲到来并不能触发irq\_mailbox\_ap2cp。只有当mask\_ap2cp\_irq\_x为低的时候，set\_ap2cp\_irq\_x才能触发irq\_mailbox\_ap2cp。

### Mailbox lock

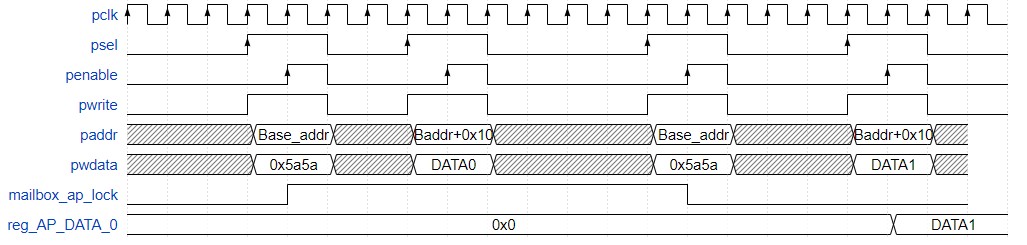
AP侧的Core可以通过对AP\_MAILBOX\_LOCK寄存器写‘h5A5A对AP侧的数据寄存器AP\_DATA（0-3）进行锁存。CP侧的Core可以通过对CP\_MAILBOX\_LOCK寄存器写’h5A5A对CP侧的数据寄存器CP\_DATA（0-3）进行锁存。AP\_MAILBOX\_LOCK和CP\_MAILBOX\_LOCK可以进行查询，为’h1的时候表明LOCK，为’h0的时候表明Un-LOCK。原理图如下所示：

Figure 5 Mailbox 数据寄存器Lock和unLock

由图1-5可知，往AP\_MAILBOX\_LOCK写入0x5a5a，AP\_DATA\_x寄存器被锁住，此时DATA0没有被成功写入reg\_AP\_DATA\_0寄存器中，当第二次往AP\_MAILBOX\_LOCK寄存器写入0x5a5a时，AP\_DATA\_x解锁，此时DATA1被成功写入reg\_AP\_DATA\_0中。

## Basic Block Diagram



## Programming Sequence

本章对Mailbox的软件使用方法作出说明。该流程中操作的寄存器细节可参考3.2章节。

### AP-to-CP Interrupt Programing Examples

AP-to-CP中断是由AP侧的Core通过写AP\_MAILBOX\_CTRL产生的中断，该中断传递到CP侧的Core，触发CP侧的中断，CP侧的Core执行完中断处理程序后，查询中断号，并将对应的中断清除，退出中断返回。



Figure 6 AP-to-CP Mailbox中断流程图

### CP-to-AP Interrupt Programing Examples

CP-to-AP中断是由CP侧的Core通过写CP\_MAILBOX\_CTRL产生的中断，该中断传递到AP侧的Core，触发AP侧的中断，AP侧的Core执行完中断处理程序后，查询中断号，并将对应的中断清除，退出中断返回。



Figure 7 CP-to-AP Mailbox中断流程图

### AP and CP Communication Programing Examples

以下流程图展示了以AP Core为发送端，CP Core为接收端，AP Core往CP Core发送一个Mailbox中断，并附带数据；CP Core接收到AP Core发送过来的Mailbox中断，读取数据，清除中断并返回一个数据，发送中断到AP Core的一个流程。该流程是一个比较典型的Mailbox应用场景，发送端不仅发送中断和数据，还需要接收中断和数据，确保接收端成功接收到中断和正确的数据。



Figure 8 AP and CP Communication Programing Examples

### Mailbox Lock Programing Examples

以下流程图展示了AP Core写完AP\_DATA\_x寄存器之后，再通过AP\_MAILBOX\_LOCK寄存器写入0x5A5A对其进行锁定的操作。锁定之后，AP\_DATA\_x内的值无法被修改，只能被读取。直到AP Core要写入新数据之前，再对AP\_MAILBOX\_LOCK寄存器写入0x5A5A对AP\_DATA\_x进行解锁。



Figure 9 Mailbox Lock Programing Examples

## {{ CMN\_MAILBOX\_Name }} Register

### {{ CMN\_MAILBOX\_AP\_MAILBOX\_LOCK\_Name }}

Offset: {{ CMN\_MAILBOX\_AP\_MAILBOX\_LOCK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_AP\_MAILBOX\_LOCK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_AP\_MAILBOX\_CTRL\_Name }}

Offset: {{ CMN\_MAILBOX\_AP\_MAILBOX\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_AP\_MAILBOX\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_AP\_MAILBOX\_IRQ\_Name }}

Offset: {{ CMN\_MAILBOX\_AP\_MAILBOX\_IRQ\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_AP\_MAILBOX\_IRQ\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty22839\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty22839\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty22839\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty9034\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty9034\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty9034\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty89557\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty89557\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty89557\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty51456\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty51456\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty51456\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_CP\_MAILBOX\_LOCK\_Name }}

Offset: {{ CMN\_MAILBOX\_CP\_MAILBOX\_LOCK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_CP\_MAILBOX\_LOCK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_CP\_MAILBOX\_CTRL\_Name }}

Offset: {{ CMN\_MAILBOX\_CP\_MAILBOX\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_CP\_MAILBOX\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_CP\_MAILBOX\_IRQ\_Name }}

Offset: {{ CMN\_MAILBOX\_CP\_MAILBOX\_IRQ\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_CP\_MAILBOX\_IRQ\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty22683\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty22683\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty22683\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty70559\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty70559\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty70559\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty62871\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty62871\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty62871\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CMN\_MAILBOX\_Empty62962\_Name }}

Offset: {{ CMN\_MAILBOX\_Empty62962\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CMN\_MAILBOX\_Empty62962\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ AON\_PMUCTRL\_Name }}

## Introduction

PMU模块描述芯片的低功耗模式，以及在低功耗模式下不同模块的开关。

## Main Features

### Normal mode

芯片的正常运行模式，在框图中可以看到有红色开关的地方，是可以通过软件配置来进行开关。

### Sleep mode

### Deep Sleep mode

芯片的最低功耗模式。

## Function Description

## Basic Block Diagram

### Normal mode



### Sleep mode

下图中灰色的部分，是在Sleep模式下被关闭的模块



### Deep Sleep mode

Deep Sleep mode和Sleep mode的最大差异就是PSRAM在这个模式下被强制关

闭。



## {{ AON\_PMUCTRL\_Name }} Register

### {{ AON\_PMUCTRL\_AON\_WAIT\_XTAL\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_WAIT\_XTAL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_WAIT\_XTAL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_PMU\_CTRL2\_Name }}

Offset: {{ AON\_PMUCTRL\_PMU\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_PMU\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_CRM\_CTRL1\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_CRM\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_CRM\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_CRM\_CTRL2\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_CRM\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_CRM\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_PCLK\_FRC\_ON\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_PCLK\_FRC\_ON\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_PCLK\_FRC\_ON\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_IWDT\_FEED\_KEY\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_IWDT\_FEED\_KEY\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_IWDT\_FEED\_KEY\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_RSVD\_REG0\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_RSVD\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_RSVD\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_STATUS\_1\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_STATUS\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_STATUS\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_STATUS\_2\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_STATUS\_2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_STATUS\_2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_PMUCTRL\_AON\_STATUS\_3\_Name }}

Offset: {{ AON\_PMUCTRL\_AON\_STATUS\_3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_PMUCTRL\_AON\_STATUS\_3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ AON\_IOMUX\_Name }}

## Introduction

Always on 区域的IO功能配置，处于这个区域的GPIO只有6个，分别是GPIOB0 — GPIOB5

## Main Features

## Function Description

## Basic Block Diagram

## {{ AON\_IOMUX\_Name }} Register

### {{ AON\_IOMUX\_PAD\_AON\_GPIOB\_Name }}

Offset: {{ AON\_IOMUX\_PAD\_AON\_GPIOB\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_IOMUX\_PAD\_AON\_GPIOB\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ APC\_OLD\_Name }}

## Introduction

## Main Features

## Function Description

## Basic Block Diagram

## {{ APC\_OLD\_Name }} Register

### {{ APC\_OLD\_CTRL\_Name }}

Offset: {{ APC\_OLD\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_STATE\_Name }}

Offset: {{ APC\_OLD\_STATE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_STATE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_INT\_EN\_Name }}

Offset: {{ APC\_OLD\_INT\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_INT\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_DMA\_EN\_Name }}

Offset: {{ APC\_OLD\_DMA\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_DMA\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_FIFO\_CTRL\_Name }}

Offset: {{ APC\_OLD\_FIFO\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_FIFO\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_INFIFO\_ST\_Name }}

Offset: {{ APC\_OLD\_INFIFO\_ST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_INFIFO\_ST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_OUTFIFO\_ST\_Name }}

Offset: {{ APC\_OLD\_OUTFIFO\_ST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_OUTFIFO\_ST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_INFIFO\_THRSH\_Name }}

Offset: {{ APC\_OLD\_INFIFO\_THRSH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_INFIFO\_THRSH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_OUTFIFO\_THRSH\_Name }}

Offset: {{ APC\_OLD\_OUTFIFO\_THRSH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_OUTFIFO\_THRSH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_FIFO\_SRCDST\_Name }}

Offset: {{ APC\_OLD\_FIFO\_SRCDST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_FIFO\_SRCDST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S0\_CTRL\_Name }}

Offset: {{ APC\_OLD\_I2S0\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S0\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S0\_STA\_Name }}

Offset: {{ APC\_OLD\_I2S0\_STA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S0\_STA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S0\_PR\_Name }}

Offset: {{ APC\_OLD\_I2S0\_PR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S0\_PR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S1\_CTRL\_Name }}

Offset: {{ APC\_OLD\_I2S1\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S1\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S1\_STA\_Name }}

Offset: {{ APC\_OLD\_I2S1\_STA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S1\_STA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S1\_PR\_Name }}

Offset: {{ APC\_OLD\_I2S1\_PR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S1\_PR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S2\_CTRL\_Name }}

Offset: {{ APC\_OLD\_I2S2\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S2\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S2\_STA\_Name }}

Offset: {{ APC\_OLD\_I2S2\_STA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S2\_STA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_OLD\_I2S2\_PR\_Name }}

Offset: {{ APC\_OLD\_I2S2\_PR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_OLD\_I2S2\_PR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ APC\_Name }}

## Introduction

APC属于CP的音频模块，这个部分不对用户开放

## Main Features

## Function Description

## Basic Block Diagram

## {{ APC\_Name }} Register

### {{ APC\_APC\_CFG\_Name }}

Offset: {{ APC\_APC\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_CFG\_RSVD0\_Name }}

Offset: {{ APC\_APC\_CFG\_RSVD0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_CFG\_RSVD0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_CFG\_RSVD1\_Name }}

Offset: {{ APC\_APC\_CFG\_RSVD1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_CFG\_RSVD1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH0\_CFG\_Name }}

Offset: {{ APC\_APC\_TX\_CH0\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH0\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH1\_CFG\_Name }}

Offset: {{ APC\_APC\_TX\_CH1\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH1\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH0\_CFG\_Name }}

Offset: {{ APC\_APC\_RX\_CH0\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH0\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH1\_CFG\_Name }}

Offset: {{ APC\_APC\_RX\_CH1\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH1\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH2\_CFG\_Name }}

Offset: {{ APC\_APC\_RX\_CH2\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH2\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_0\_Name }}

Offset: {{ APC\_EQCOEF\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_1\_Name }}

Offset: {{ APC\_EQCOEF\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_2\_Name }}

Offset: {{ APC\_EQCOEF\_2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_3\_Name }}

Offset: {{ APC\_EQCOEF\_3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_4\_Name }}

Offset: {{ APC\_EQCOEF\_4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_5\_Name }}

Offset: {{ APC\_EQCOEF\_5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_6\_Name }}

Offset: {{ APC\_EQCOEF\_6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_7\_Name }}

Offset: {{ APC\_EQCOEF\_7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_8\_Name }}

Offset: {{ APC\_EQCOEF\_8\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_8\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_9\_Name }}

Offset: {{ APC\_EQCOEF\_9\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_9\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_10\_Name }}

Offset: {{ APC\_EQCOEF\_10\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_10\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_11\_Name }}

Offset: {{ APC\_EQCOEF\_11\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_11\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_12\_Name }}

Offset: {{ APC\_EQCOEF\_12\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_12\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_13\_Name }}

Offset: {{ APC\_EQCOEF\_13\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_13\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_14\_Name }}

Offset: {{ APC\_EQCOEF\_14\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_14\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_15\_Name }}

Offset: {{ APC\_EQCOEF\_15\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_15\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_16\_Name }}

Offset: {{ APC\_EQCOEF\_16\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_16\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_17\_Name }}

Offset: {{ APC\_EQCOEF\_17\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_17\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_18\_Name }}

Offset: {{ APC\_EQCOEF\_18\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_18\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_19\_Name }}

Offset: {{ APC\_EQCOEF\_19\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_19\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_20\_Name }}

Offset: {{ APC\_EQCOEF\_20\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_20\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_21\_Name }}

Offset: {{ APC\_EQCOEF\_21\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_21\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_22\_Name }}

Offset: {{ APC\_EQCOEF\_22\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_22\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_23\_Name }}

Offset: {{ APC\_EQCOEF\_23\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_23\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_24\_Name }}

Offset: {{ APC\_EQCOEF\_24\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_24\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_25\_Name }}

Offset: {{ APC\_EQCOEF\_25\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_25\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_26\_Name }}

Offset: {{ APC\_EQCOEF\_26\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_26\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_27\_Name }}

Offset: {{ APC\_EQCOEF\_27\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_27\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_28\_Name }}

Offset: {{ APC\_EQCOEF\_28\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_28\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_29\_Name }}

Offset: {{ APC\_EQCOEF\_29\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_29\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_30\_Name }}

Offset: {{ APC\_EQCOEF\_30\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_30\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_31\_Name }}

Offset: {{ APC\_EQCOEF\_31\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_31\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_32\_Name }}

Offset: {{ APC\_EQCOEF\_32\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_32\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_33\_Name }}

Offset: {{ APC\_EQCOEF\_33\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_33\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_34\_Name }}

Offset: {{ APC\_EQCOEF\_34\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_34\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_35\_Name }}

Offset: {{ APC\_EQCOEF\_35\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_35\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_36\_Name }}

Offset: {{ APC\_EQCOEF\_36\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_36\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_37\_Name }}

Offset: {{ APC\_EQCOEF\_37\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_37\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_38\_Name }}

Offset: {{ APC\_EQCOEF\_38\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_38\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_39\_Name }}

Offset: {{ APC\_EQCOEF\_39\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_39\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_40\_Name }}

Offset: {{ APC\_EQCOEF\_40\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_40\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_41\_Name }}

Offset: {{ APC\_EQCOEF\_41\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_41\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_42\_Name }}

Offset: {{ APC\_EQCOEF\_42\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_42\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_43\_Name }}

Offset: {{ APC\_EQCOEF\_43\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_43\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_44\_Name }}

Offset: {{ APC\_EQCOEF\_44\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_44\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_45\_Name }}

Offset: {{ APC\_EQCOEF\_45\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_45\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_46\_Name }}

Offset: {{ APC\_EQCOEF\_46\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_46\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_47\_Name }}

Offset: {{ APC\_EQCOEF\_47\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_47\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_48\_Name }}

Offset: {{ APC\_EQCOEF\_48\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_48\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_EQCOEF\_49\_Name }}

Offset: {{ APC\_EQCOEF\_49\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_EQCOEF\_49\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S0\_CFG0\_Name }}

Offset: {{ APC\_APC\_I2S0\_CFG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S0\_CFG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S0\_CFG1\_Name }}

Offset: {{ APC\_APC\_I2S0\_CFG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S0\_CFG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S1\_CFG0\_Name }}

Offset: {{ APC\_APC\_I2S1\_CFG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S1\_CFG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S1\_CFG1\_Name }}

Offset: {{ APC\_APC\_I2S1\_CFG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S1\_CFG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S2\_CFG0\_Name }}

Offset: {{ APC\_APC\_I2S2\_CFG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S2\_CFG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_I2S2\_CFG1\_Name }}

Offset: {{ APC\_APC\_I2S2\_CFG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_I2S2\_CFG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH0\_L\_DATA\_Name }}

Offset: {{ APC\_APC\_TX\_CH0\_L\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH0\_L\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH0\_R\_DATA\_Name }}

Offset: {{ APC\_APC\_TX\_CH0\_R\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH0\_R\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH1\_L\_DATA\_Name }}

Offset: {{ APC\_APC\_TX\_CH1\_L\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH1\_L\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_TX\_CH1\_R\_DATA\_Name }}

Offset: {{ APC\_APC\_TX\_CH1\_R\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_TX\_CH1\_R\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH0\_L\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH0\_L\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH0\_L\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH0\_R\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH0\_R\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH0\_R\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH1\_L\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH1\_L\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH1\_L\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH1\_R\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH1\_R\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH1\_R\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH2\_L\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH2\_L\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH2\_L\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RX\_CH2\_R\_DATA\_Name }}

Offset: {{ APC\_APC\_RX\_CH2\_R\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RX\_CH2\_R\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_TX\_MSK\_Name }}

Offset: {{ APC\_APC\_INTR\_TX\_MSK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_TX\_MSK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_RX\_MSK\_Name }}

Offset: {{ APC\_APC\_INTR\_RX\_MSK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_RX\_MSK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_TX\_CLR\_Name }}

Offset: {{ APC\_APC\_INTR\_TX\_CLR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_TX\_CLR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_RX\_CLR\_Name }}

Offset: {{ APC\_APC\_INTR\_RX\_CLR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_RX\_CLR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_TX\_IRSR\_Name }}

Offset: {{ APC\_APC\_INTR\_TX\_IRSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_TX\_IRSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_RX\_IRSR\_Name }}

Offset: {{ APC\_APC\_INTR\_RX\_IRSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_RX\_IRSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_TX\_ISR\_Name }}

Offset: {{ APC\_APC\_INTR\_TX\_ISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_TX\_ISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_INTR\_RX\_ISR\_Name }}

Offset: {{ APC\_APC\_INTR\_RX\_ISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_INTR\_RX\_ISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_I2S\_SYNC\_MODE\_Name }}

Offset: {{ APC\_I2S\_SYNC\_MODE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_I2S\_SYNC\_MODE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RSVD\_RW\_REG0\_Name }}

Offset: {{ APC\_APC\_RSVD\_RW\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RSVD\_RW\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RSVD\_RW\_REG1\_Name }}

Offset: {{ APC\_APC\_RSVD\_RW\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RSVD\_RW\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RSVD\_RO\_REG0\_Name }}

Offset: {{ APC\_APC\_RSVD\_RO\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RSVD\_RO\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ APC\_APC\_RSVD\_RO\_REG1\_Name }}

Offset: {{ APC\_APC\_RSVD\_RO\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in APC\_APC\_RSVD\_RO\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ VAD\_Name }}

## Introduction

## Main Features

VAD属于CP的音频模块，这个部分不对用户开放

## Function Description

## Basic Block Diagram

## {{ VAD\_Name }} Register

### {{ VAD\_CTRL\_Name }}

Offset: {{ VAD\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_STATE\_Name }}

Offset: {{ VAD\_STATE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_STATE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_INTEN\_Name }}

Offset: {{ VAD\_INTEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_INTEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_TRACBK\_LEN\_Name }}

Offset: {{ VAD\_TRACBK\_LEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_TRACBK\_LEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_FILTCTRL\_Name }}

Offset: {{ VAD\_FILTCTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_FILTCTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_BLKCTRL\_Name }}

Offset: {{ VAD\_BLKCTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_BLKCTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_ZCHTOL\_Name }}

Offset: {{ VAD\_ZCHTOL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_ZCHTOL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_ZCH\_MINAMP\_Name }}

Offset: {{ VAD\_ZCH\_MINAMP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_ZCH\_MINAMP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_ZCH\_MAXAMP\_Name }}

Offset: {{ VAD\_ZCH\_MAXAMP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_ZCH\_MAXAMP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_AMP\_L\_Name }}

Offset: {{ VAD\_AMP\_L\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_AMP\_L\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_AMP\_H\_Name }}

Offset: {{ VAD\_AMP\_H\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_AMP\_H\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_ZCR\_L\_Name }}

Offset: {{ VAD\_ZCR\_L\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_ZCR\_L\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_ZCR\_H\_Name }}

Offset: {{ VAD\_ZCR\_H\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_ZCR\_H\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VADDEC\_MISC\_Name }}

Offset: {{ VAD\_VADDEC\_MISC\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VADDEC\_MISC\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR1\_B1\_Name }}

Offset: {{ VAD\_VAD\_IIR1\_B1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR1\_B1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR1\_B2\_Name }}

Offset: {{ VAD\_VAD\_IIR1\_B2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR1\_B2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR1\_B3\_Name }}

Offset: {{ VAD\_VAD\_IIR1\_B3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR1\_B3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR1\_MA2\_Name }}

Offset: {{ VAD\_VAD\_IIR1\_MA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR1\_MA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR1\_MA3\_Name }}

Offset: {{ VAD\_VAD\_IIR1\_MA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR1\_MA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR2\_B1\_Name }}

Offset: {{ VAD\_VAD\_IIR2\_B1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR2\_B1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR2\_B2\_Name }}

Offset: {{ VAD\_VAD\_IIR2\_B2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR2\_B2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR2\_B3\_Name }}

Offset: {{ VAD\_VAD\_IIR2\_B3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR2\_B3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR2\_MA2\_Name }}

Offset: {{ VAD\_VAD\_IIR2\_MA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR2\_MA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR2\_MA3\_Name }}

Offset: {{ VAD\_VAD\_IIR2\_MA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR2\_MA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR3\_B1\_Name }}

Offset: {{ VAD\_VAD\_IIR3\_B1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR3\_B1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR3\_B2\_Name }}

Offset: {{ VAD\_VAD\_IIR3\_B2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR3\_B2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR3\_B3\_Name }}

Offset: {{ VAD\_VAD\_IIR3\_B3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR3\_B3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR3\_MA2\_Name }}

Offset: {{ VAD\_VAD\_IIR3\_MA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR3\_MA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR3\_MA3\_Name }}

Offset: {{ VAD\_VAD\_IIR3\_MA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR3\_MA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR4\_B1\_Name }}

Offset: {{ VAD\_VAD\_IIR4\_B1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR4\_B1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR4\_B2\_Name }}

Offset: {{ VAD\_VAD\_IIR4\_B2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR4\_B2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR4\_B3\_Name }}

Offset: {{ VAD\_VAD\_IIR4\_B3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR4\_B3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR4\_MA2\_Name }}

Offset: {{ VAD\_VAD\_IIR4\_MA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR4\_MA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR4\_MA3\_Name }}

Offset: {{ VAD\_VAD\_IIR4\_MA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR4\_MA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR5\_B1\_Name }}

Offset: {{ VAD\_VAD\_IIR5\_B1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR5\_B1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR5\_B2\_Name }}

Offset: {{ VAD\_VAD\_IIR5\_B2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR5\_B2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR5\_B3\_Name }}

Offset: {{ VAD\_VAD\_IIR5\_B3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR5\_B3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR5\_MA2\_Name }}

Offset: {{ VAD\_VAD\_IIR5\_MA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR5\_MA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_VAD\_IIR5\_MA3\_Name }}

Offset: {{ VAD\_VAD\_IIR5\_MA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_VAD\_IIR5\_MA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_START\_ADDR\_Name }}

Offset: {{ VAD\_START\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_START\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_END\_ADDR\_Name }}

Offset: {{ VAD\_END\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_END\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ VAD\_CUR\_ADDR\_Name }}

Offset: {{ VAD\_CUR\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in VAD\_CUR\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ DW\_UART\_Name }}

## Introduction

IP的规格内容，需要PDF转成word放进来

## Main Features

## Function Description

## Basic Block Diagram

## {{ DW\_UART\_Name }} Register

### {{ DW\_UART\_RBR\_Name }}

Offset: {{ DW\_UART\_RBR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_RBR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_THR\_Name }}

Offset: {{ DW\_UART\_THR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_THR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DLL\_Name }}

Offset: {{ DW\_UART\_DLL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DLL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DLH\_Name }}

Offset: {{ DW\_UART\_DLH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DLH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_IER\_Name }}

Offset: {{ DW\_UART\_IER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_IER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_IIR\_Name }}

Offset: {{ DW\_UART\_IIR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_IIR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_FCR\_Name }}

Offset: {{ DW\_UART\_FCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_FCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_LCR\_Name }}

Offset: {{ DW\_UART\_LCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_LCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_MCR\_Name }}

Offset: {{ DW\_UART\_MCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_MCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_LSR\_Name }}

Offset: {{ DW\_UART\_LSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_LSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_MSR\_Name }}

Offset: {{ DW\_UART\_MSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_MSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SCR\_Name }}

Offset: {{ DW\_UART\_SCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_LPDLL\_Name }}

Offset: {{ DW\_UART\_LPDLL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_LPDLL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_LPDLH\_Name }}

Offset: {{ DW\_UART\_LPDLH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_LPDLH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SRBR\_Name }}

Offset: {{ DW\_UART\_SRBR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SRBR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_STHR\_Name }}

Offset: {{ DW\_UART\_STHR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_STHR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_FAR\_Name }}

Offset: {{ DW\_UART\_FAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_FAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_TFR\_Name }}

Offset: {{ DW\_UART\_TFR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_TFR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_RFW\_Name }}

Offset: {{ DW\_UART\_RFW\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_RFW\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_USR\_Name }}

Offset: {{ DW\_UART\_USR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_USR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_TFL\_Name }}

Offset: {{ DW\_UART\_TFL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_TFL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_RFL\_Name }}

Offset: {{ DW\_UART\_RFL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_RFL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SRR\_Name }}

Offset: {{ DW\_UART\_SRR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SRR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SRTS\_Name }}

Offset: {{ DW\_UART\_SRTS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SRTS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SBCR\_Name }}

Offset: {{ DW\_UART\_SBCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SBCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SDMAM\_Name }}

Offset: {{ DW\_UART\_SDMAM\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SDMAM\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SFE\_Name }}

Offset: {{ DW\_UART\_SFE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SFE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_SRT\_Name }}

Offset: {{ DW\_UART\_SRT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_SRT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_STET\_Name }}

Offset: {{ DW\_UART\_STET\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_STET\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_HTX\_Name }}

Offset: {{ DW\_UART\_HTX\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_HTX\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DMASA\_Name }}

Offset: {{ DW\_UART\_DMASA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DMASA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_TCR\_Name }}

Offset: {{ DW\_UART\_TCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_TCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DE\_EN\_Name }}

Offset: {{ DW\_UART\_DE\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DE\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_RE\_EN\_Name }}

Offset: {{ DW\_UART\_RE\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_RE\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DET\_Name }}

Offset: {{ DW\_UART\_DET\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DET\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_TAT\_Name }}

Offset: {{ DW\_UART\_TAT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_TAT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_DLF\_Name }}

Offset: {{ DW\_UART\_DLF\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_DLF\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_RAR\_Name }}

Offset: {{ DW\_UART\_RAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_RAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_TAR\_Name }}

Offset: {{ DW\_UART\_TAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_TAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_LCR\_EXT\_Name }}

Offset: {{ DW\_UART\_LCR\_EXT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_LCR\_EXT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_CPR\_Name }}

Offset: {{ DW\_UART\_CPR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_CPR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_UCV\_Name }}

Offset: {{ DW\_UART\_UCV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_UCV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DW\_UART\_CTR\_Name }}

Offset: {{ DW\_UART\_CTR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DW\_UART\_CTR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ DUAL\_TIMER\_Name }}

## Introduction

ARM的IP，需要PDF转成word

## Main Features

## Function Description

## Basic Block Diagram

## {{ DUAL\_TIMER\_Name }} Register

### {{ DUAL\_TIMER\_LOAD0\_Name }}

Offset: {{ DUAL\_TIMER\_LOAD0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_LOAD0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_VALUE0\_Name }}

Offset: {{ DUAL\_TIMER\_VALUE0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_VALUE0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_CONTROL0\_Name }}

Offset: {{ DUAL\_TIMER\_CONTROL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_CONTROL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_INTCLR0\_Name }}

Offset: {{ DUAL\_TIMER\_INTCLR0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_INTCLR0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_RIS0\_Name }}

Offset: {{ DUAL\_TIMER\_RIS0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_RIS0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_MIS0\_Name }}

Offset: {{ DUAL\_TIMER\_MIS0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_MIS0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_BGLOAD0\_Name }}

Offset: {{ DUAL\_TIMER\_BGLOAD0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_BGLOAD0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_RESERVED\_Name }}

Offset: {{ DUAL\_TIMER\_RESERVED\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_RESERVED\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_LOAD1\_Name }}

Offset: {{ DUAL\_TIMER\_LOAD1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_LOAD1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_VALUE1\_Name }}

Offset: {{ DUAL\_TIMER\_VALUE1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_VALUE1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_CONTROL1\_Name }}

Offset: {{ DUAL\_TIMER\_CONTROL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_CONTROL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_INTCLR1\_Name }}

Offset: {{ DUAL\_TIMER\_INTCLR1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_INTCLR1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_RIS1\_Name }}

Offset: {{ DUAL\_TIMER\_RIS1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_RIS1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_MIS1\_Name }}

Offset: {{ DUAL\_TIMER\_MIS1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_MIS1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ DUAL\_TIMER\_BGLOAD1\_Name }}

Offset: {{ DUAL\_TIMER\_BGLOAD1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in DUAL\_TIMER\_BGLOAD1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ GPT\_Name }}

## Introduction

General Purpose Timer (GPT) is a programmable timer module, which is a set of compact multi-function timers.

## Main Features

The GPT provides following features：

- selectable clk source for each channel : external clk, pclk

- support 4 independent channels

- each channel provides 6 scenarios:

1. one 32bit timer

2. two 16bit timers

3. four 8bit timers

4. one 16bit PWM

5. one 16bit timer and one 8bit PWM

6. two 8bit timers and one 8bit PWM

- each timer support 3 cnt modes: up, down, up/down

- each timer support 4 run modes: single, repeat, free run, keep go

- external pause to suspend all timer/PWM activities

- input capture, configurable capture edge and capture source

- generate one pulse

- support generates interrupt for each timer, and ch\_capture\_int, ledc\_tx\_int for each channel

- support LEDC

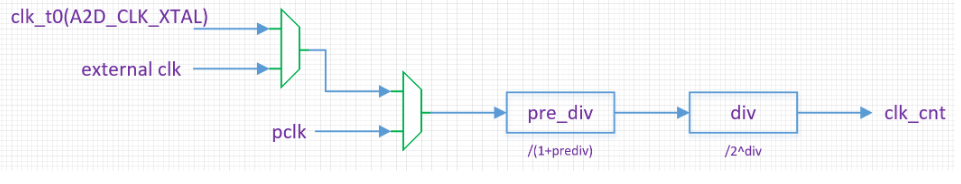
- a 4\*32-bit tx fifo for LEDC transmit

- a 4\*32-bit rx fifo for capture data

## Function Description

### Clock

The clock source for each channel is configurable. It can be selected form external clock, which comes from GPIO , internal clock clk\_t0 and PCLK. Actually, clk\_t0 and external clk are used as an enable signal of PCLK. Prescaler and divider will help to generate count clock (clk\_cnt) with lower frequency, the clk\_cnt is the work clock of counter, shown in Fig. 2.



​ Figure 2. Clock Block for each channel

### Timer

Each channel has a 32-bit counter, which can provides several timers with different bit width, such as 32-bit timer, 16-bit and 8-bit timers, see Tab.1. Using register ch\_mode to select different scenarios. There are three count directions supported, count up, count down, count up/down. In count up mode, the timer will count up to reload value setting by register CHx\_RELOAD. In count down mode the timer will count down from reload value to 0. And for count up/down mode the timer will count up to reload value first, and then count down to 0.

Also the timer run mode is programmable, user can select single, repeat, free run or keep go mode according to application. In free run mode, the timer will be a loop counter from 0 to the maximal value. And in keep go mode after re-enabling the counter, it will continue counting from the counted value when the timer is disabled.

All timer/PWM activity can be paused by external pause signal. The interrupt of each timer will be generated when time up.

### PWM

PWM output is also supported by this module. The register \*chx\_operation\* should be configured as 3 (PWM mode). The period and duty cycle of PWM is programmale by configuring register \*chx\_reload\*. When channel is disabled, PWM output value can be changed by register \*polarity\*. Central aligned and edge aligned are controled by register \*pwm\_out\_mode\*.

For central-aligned mode the period and duty cycle should be set in register \*CHx\_RELOAD\* (for detail please refer to \*Venus\_SoC\_Memory\_Mapping.xls\*). Take the following Fig. 3 central-aligned PWM as an example, setting register \*CHx\_RELOAD\* with period cycle = 5 and duty cycle = 2 and please note that the real period cycle of PWM is \*2×period cycle\*. When counter value is equal to duty cycle the PWM reverse.

For edge-aligned mode in register \*CHx\_RELOAD\* users need to configure high period and low period. The actual high and low period of PWM are \*1 + high period\* and \*1 + low period\* respectively. Take the following Fig.4 edge-aligned PWM as an example, setting register \*CHx\_RELOAD\* with low period = 3 and high period = 1. The period of PWM is \*low period + high period\*.

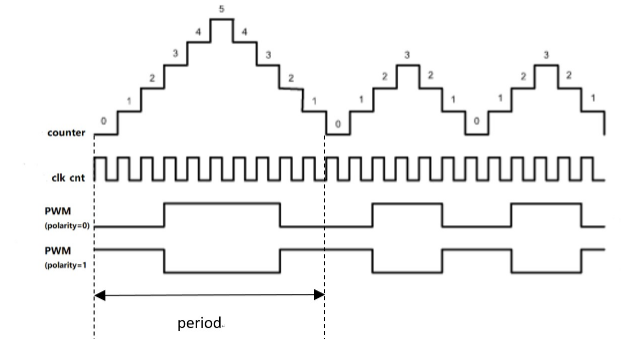


Figure 3. PWM Central-Aligned

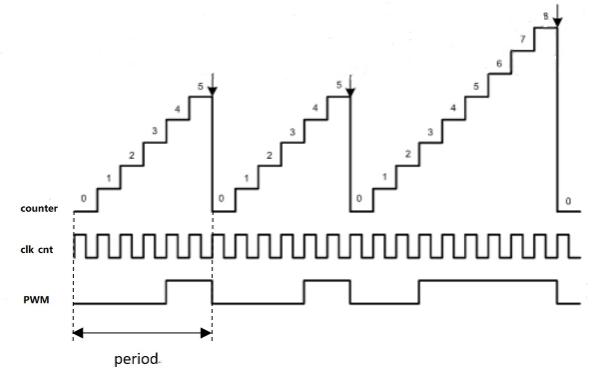
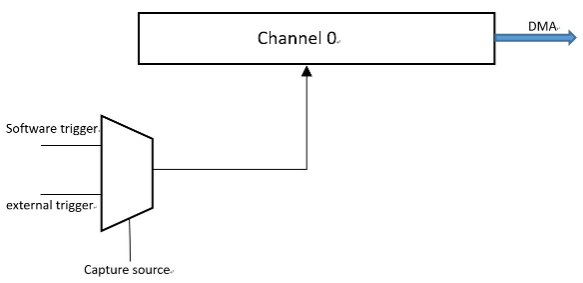


Figure 4. PWM edge-aligned

### Capture

Fig. 5 shows the simple block diagram for one channel in capture operation. Capture count mode is used to capture input pulse count, and capture time mode is used to capture pulse width. Capture source could be software trigger or external trigger. For software trigger user can set the register \*soft\_trigger\_en\*, and GPIO would be used as input pin for external trigger. User can chose rising edge, falling edge or both edge as the capture edge. The register \*chx\_operation\* should be switched to capture count mode or capture time mode, and set \*ch\_mode\* to 32-bit counter. The captured data would be saved in a 4\*32-bit rx\_fifo and can be transferd by CPU or DMA.



### One Pulse

One pulse generation is supported. Set \*operation\*=one\_pulse, and \*ch\_mode\*=1.To generate one high pulse, please set register \*polarity\* to "0" and "1" for low pulse. Register \*reload\* & \*match\_0\* also need to be configured. \*reload\* value is the maxmal value of counter. When timer count up to \*match\_0\*, the pulse will be generated.

### LEDC

1. Timing of data sending

- Period of single bit data: 1.25us ~ 800kHz

- Minimal data accuracy: 0.05us = 50ns ~ 20MHz. Then the module clock should N x 20MHz.

- Uncertainty of rising / falling edge of data: ± 150ns

2. Sequence of data sending

- Single bit data output

- Sending MSB first

- Data transmit in order of GRB (Green, Red, Blue), high bit data at first

+ \*G7, G6, ......, G0, R7, ......, R0, B7, ......, B0\*

+ G7 is MSB

+ B0 is LSB

- Data length of each frame

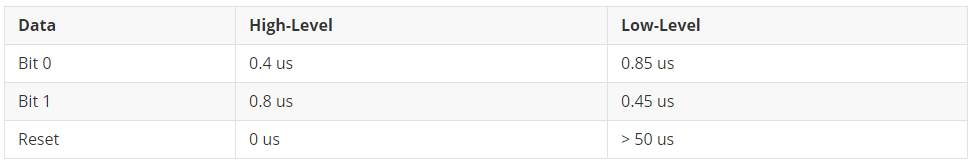
- 24bits of data to reproduce a color

- 3 groups of 8bits each that represent its RGB coding

- Time period of each frame: 24 \* 1.25us = 30us

- Time period reset code (interval of cascade frames): >50us

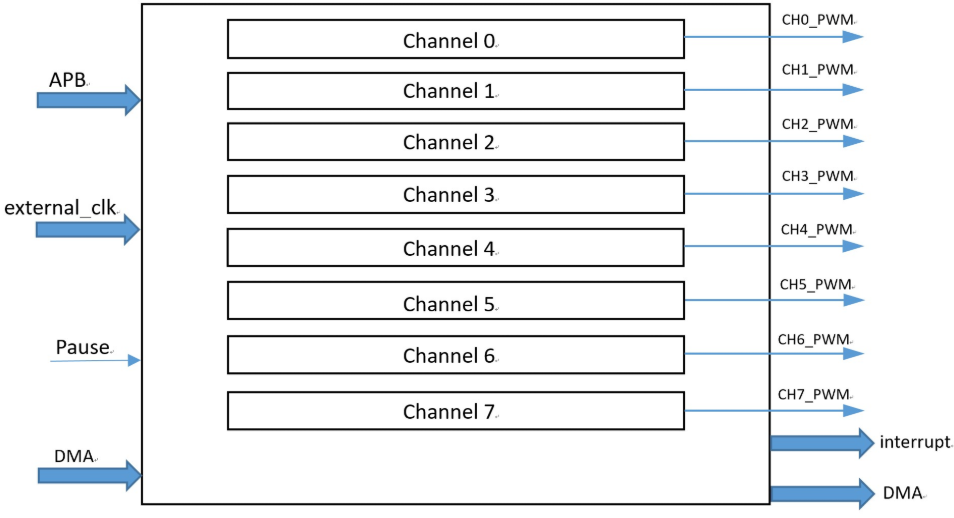
3. Data format (PWM waveform)



A 4\*32-bit tx fifo is provided for LEDC transmit. The data, which is to be send, can be transfered to tx fifo by CPU or DMA. The most significant 8-bit is flag bit: if [31:24]=8'h0 means it's a GRB data code, else it's a reset signal. Register \*chx\_reload\* and \*chx\_match\_0\* are used to configure high- and low-level duty cycle for bit 1 and bit 0. In LEDC mode, \*chx\_operation\* should be switch to LEDC mode and \*ch\_mode\* should be set to 4 (PWM). Central aligned is not supported in LEDC mode so set \*pwm\_out\_mode\* as edge aligned.

## Basic Block Diagram

Figure 1 shows the block diagram of GPT. 8 independent channels are supported. Each channel has a multi-function timer, and can also operate in capture time, capture count, one-pulse, PWM, and LEDC mode. Channel0 - Channel3 support DMA, and for Channel4 - Channel7 the data transmission can be achieved by CPU.



## {{ GPT\_Name }} Register

### {{ GPT\_ID\_Name }}

Offset: {{ GPT\_ID\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ID\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH0\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH1\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH2\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH3\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH4\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH5\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH6\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_CLK\_CTRL\_Name }}

Offset: {{ GPT\_CH7\_CLK\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_CLK\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_CTRL\_Name }}

Offset: {{ GPT\_CH0\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_CTRL\_Name }}

Offset: {{ GPT\_CH1\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_CTRL\_Name }}

Offset: {{ GPT\_CH2\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_CTRL\_Name }}

Offset: {{ GPT\_CH3\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_CTRL\_Name }}

Offset: {{ GPT\_CH4\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_CTRL\_Name }}

Offset: {{ GPT\_CH5\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_CTRL\_Name }}

Offset: {{ GPT\_CH6\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_CTRL\_Name }}

Offset: {{ GPT\_CH7\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_RELOAD\_Name }}

Offset: {{ GPT\_CH0\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_RELOAD\_Name }}

Offset: {{ GPT\_CH1\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_RELOAD\_Name }}

Offset: {{ GPT\_CH2\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_RELOAD\_Name }}

Offset: {{ GPT\_CH3\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_RELOAD\_Name }}

Offset: {{ GPT\_CH4\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_RELOAD\_Name }}

Offset: {{ GPT\_CH5\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_RELOAD\_Name }}

Offset: {{ GPT\_CH6\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_RELOAD\_Name }}

Offset: {{ GPT\_CH7\_RELOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_RELOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CNT\_MODE\_CTRL\_1\_Name }}

Offset: {{ GPT\_CNT\_MODE\_CTRL\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CNT\_MODE\_CTRL\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CNT\_MODE\_CTRL\_0\_Name }}

Offset: {{ GPT\_CNT\_MODE\_CTRL\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CNT\_MODE\_CTRL\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_RUN\_MODE\_CTRL\_1\_Name }}

Offset: {{ GPT\_RUN\_MODE\_CTRL\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_RUN\_MODE\_CTRL\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_RUN\_MODE\_CTRL\_0\_Name }}

Offset: {{ GPT\_RUN\_MODE\_CTRL\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_RUN\_MODE\_CTRL\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_CNT\_Name }}

Offset: {{ GPT\_CH0\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_CNT\_Name }}

Offset: {{ GPT\_CH1\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_CNT\_Name }}

Offset: {{ GPT\_CH2\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_CNT\_Name }}

Offset: {{ GPT\_CH3\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_CNT\_Name }}

Offset: {{ GPT\_CH4\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_CNT\_Name }}

Offset: {{ GPT\_CH5\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_CNT\_Name }}

Offset: {{ GPT\_CH6\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_CNT\_Name }}

Offset: {{ GPT\_CH7\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH\_CNT\_EN\_Name }}

Offset: {{ GPT\_CH\_CNT\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH\_CNT\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH\_NUM\_Name }}

Offset: {{ GPT\_CH\_NUM\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH\_NUM\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH0\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH1\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH2\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH3\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH4\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH5\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH6\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_MATCH\_0\_Name }}

Offset: {{ GPT\_CH7\_MATCH\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_MATCH\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_DMA\_CTRL\_Name }}

Offset: {{ GPT\_DMA\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_DMA\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_IMR\_CH\_Name }}

Offset: {{ GPT\_IMR\_CH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_IMR\_CH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_IMR\_TIMER\_Name }}

Offset: {{ GPT\_IMR\_TIMER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_IMR\_TIMER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_ISR\_CH\_Name }}

Offset: {{ GPT\_ISR\_CH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ISR\_CH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_ISR\_TIMER\_Name }}

Offset: {{ GPT\_ISR\_TIMER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ISR\_TIMER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_ICR\_CH\_Name }}

Offset: {{ GPT\_ICR\_CH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ICR\_CH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_ICR\_TIMER\_Name }}

Offset: {{ GPT\_ICR\_TIMER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ICR\_TIMER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH\_TIMER\_ENABLE\_Name }}

Offset: {{ GPT\_CH\_TIMER\_ENABLE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH\_TIMER\_ENABLE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH0\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH1\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH2\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH3\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH4\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH5\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH6\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_LEDC\_TX\_FIFO\_Name }}

Offset: {{ GPT\_CH7\_LEDC\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_LEDC\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH0\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH0\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH0\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH1\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH1\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH1\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH2\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH2\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH2\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH3\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH3\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH3\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH4\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH4\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH4\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH5\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH5\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH5\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH6\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH6\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH6\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_CH7\_RX\_FIFO\_Name }}

Offset: {{ GPT\_CH7\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_CH7\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_FIFO\_STATUS\_0\_Name }}

Offset: {{ GPT\_FIFO\_STATUS\_0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_FIFO\_STATUS\_0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_FIFO\_STATUS\_1\_Name }}

Offset: {{ GPT\_FIFO\_STATUS\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_FIFO\_STATUS\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_FIFO\_STATUS\_2\_Name }}

Offset: {{ GPT\_FIFO\_STATUS\_2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_FIFO\_STATUS\_2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_FIFO\_CONFIG\_Name }}

Offset: {{ GPT\_FIFO\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_FIFO\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_SHADOW\_SYNC\_Name }}

Offset: {{ GPT\_SHADOW\_SYNC\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_SHADOW\_SYNC\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_SHADOW\_LOAD\_Name }}

Offset: {{ GPT\_SHADOW\_LOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_SHADOW\_LOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_IRSR\_CH\_Name }}

Offset: {{ GPT\_IRSR\_CH\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_IRSR\_CH\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_IRSR\_TIMER\_Name }}

Offset: {{ GPT\_IRSR\_TIMER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_IRSR\_TIMER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPT\_ICR\_FIFO\_Name }}

Offset: {{ GPT\_ICR\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPT\_ICR\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ GPIO\_Name }}

## Introduction

该模块用于配置GPIO相关的功能，如上拉，下拉，数据置位，数据清0，中断使能，中断触发

模式是边沿还是电平。

Andes的IP，需要PDF转word

## Main Features

## Function Description

## Basic Block Diagram

## {{ GPIO\_Name }} Register

### {{ GPIO\_IDREV\_Name }}

Offset: {{ GPIO\_IDREV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_IDREV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_CFG\_Name }}

Offset: {{ GPIO\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DATAIN\_Name }}

Offset: {{ GPIO\_DATAIN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DATAIN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DATAOUT\_Name }}

Offset: {{ GPIO\_DATAOUT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DATAOUT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_CHANNELDIR\_Name }}

Offset: {{ GPIO\_CHANNELDIR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_CHANNELDIR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DOUTCLEAR\_Name }}

Offset: {{ GPIO\_DOUTCLEAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DOUTCLEAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DOUTSET\_Name }}

Offset: {{ GPIO\_DOUTSET\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DOUTSET\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_PULLEN\_Name }}

Offset: {{ GPIO\_PULLEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_PULLEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_PULLTYPE\_Name }}

Offset: {{ GPIO\_PULLTYPE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_PULLTYPE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTREN\_Name }}

Offset: {{ GPIO\_INTREN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTREN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTRMODE0\_Name }}

Offset: {{ GPIO\_INTRMODE0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTRMODE0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTRMODE1\_Name }}

Offset: {{ GPIO\_INTRMODE1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTRMODE1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTRMODE2\_Name }}

Offset: {{ GPIO\_INTRMODE2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTRMODE2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTRMODE3\_Name }}

Offset: {{ GPIO\_INTRMODE3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTRMODE3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_INTRSTATUS\_Name }}

Offset: {{ GPIO\_INTRSTATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_INTRSTATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DEBOUNCEEN\_Name }}

Offset: {{ GPIO\_DEBOUNCEEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DEBOUNCEEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPIO\_DEBOUNCECTRL\_Name }}

Offset: {{ GPIO\_DEBOUNCECTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPIO\_DEBOUNCECTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ SPI\_Name }}

## Introduction

Andes的IP，需要PDF转WORD

## Main Features

## Function Description

## Basic Block Diagram

## {{ SPI\_Name }} Register

### {{ SPI\_IDREV\_Name }}

Offset: {{ SPI\_IDREV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_IDREV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_TRANSFMT\_Name }}

Offset: {{ SPI\_TRANSFMT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_TRANSFMT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_DIRECTIO\_Name }}

Offset: {{ SPI\_DIRECTIO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_DIRECTIO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_TRANSCTRL\_Name }}

Offset: {{ SPI\_TRANSCTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_TRANSCTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_CMD\_Name }}

Offset: {{ SPI\_CMD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_CMD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_ADDR\_Name }}

Offset: {{ SPI\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_DATA\_Name }}

Offset: {{ SPI\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_CTRL\_Name }}

Offset: {{ SPI\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_STATUS\_Name }}

Offset: {{ SPI\_STATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_STATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_INTREN\_Name }}

Offset: {{ SPI\_INTREN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_INTREN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_INTRST\_Name }}

Offset: {{ SPI\_INTRST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_INTRST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_TIMING\_Name }}

Offset: {{ SPI\_TIMING\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_TIMING\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_MEMCTRL\_Name }}

Offset: {{ SPI\_MEMCTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_MEMCTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_SLVST\_Name }}

Offset: {{ SPI\_SLVST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_SLVST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_SLVDATACNT\_Name }}

Offset: {{ SPI\_SLVDATACNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_SLVDATACNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SPI\_CONFIG\_Name }}

Offset: {{ SPI\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SPI\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CRYPTO\_Name }}

## Introduction

CRYPTO 模块主要用于AES加解密和SHA运算

## Main Features

AES只支持AES128，密钥128比特，每次处理一个4 words块。

AES支持ECB，CBC模式

AES加解密一个块需要22周期

SHA为SHA256运算器，每次处理一个16words块，结果为256bits hash。

SHA处理一个块需要67周期

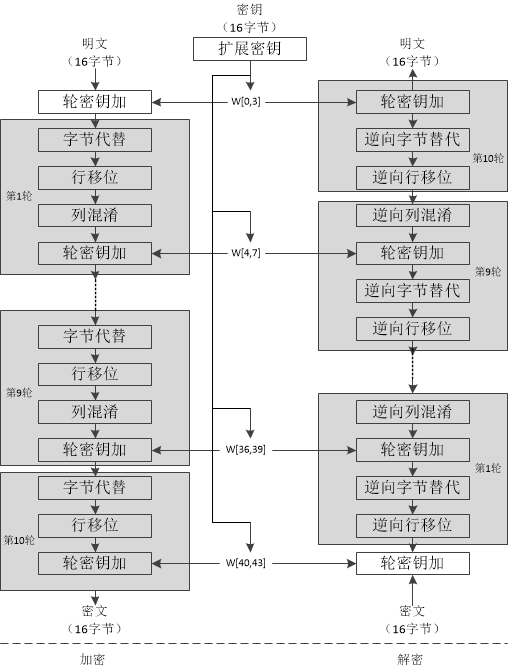
CRYPTO工作模式有以下几种

* AES encrypt only
* AES decrypt only
* SHA only
* AES encrypt with SHA
* AES decrypt with SHA

## Function Description

## Basic Block Diagram

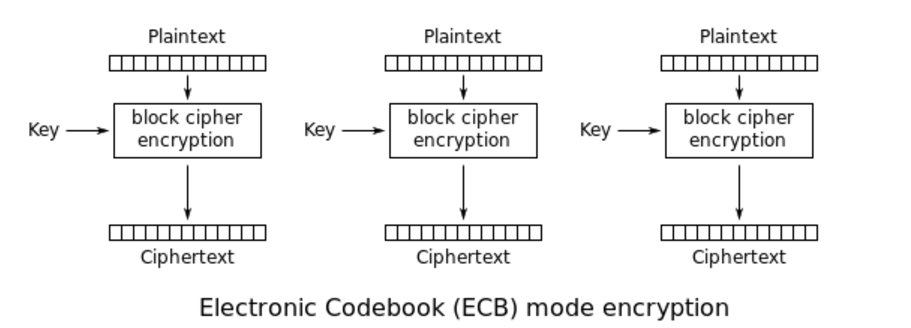
### AES加解密流程

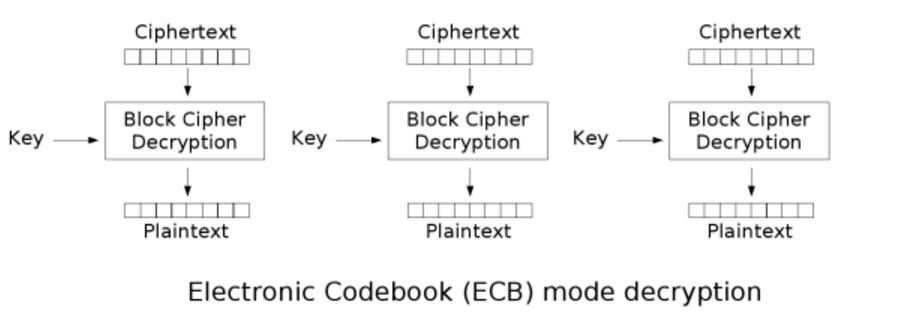


### AES mode

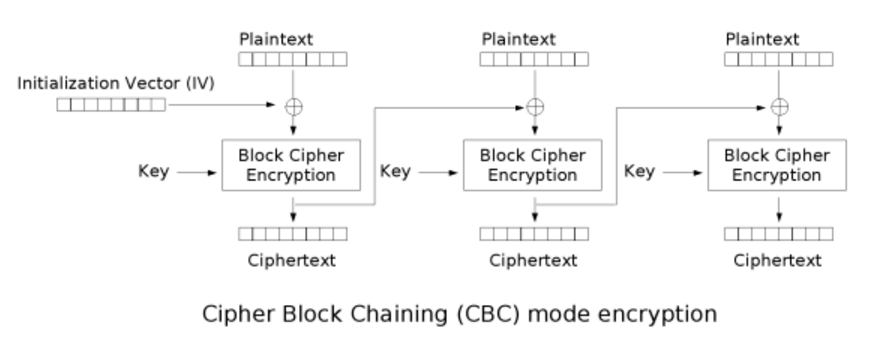
目前AES128只支持ECB和CBC模式

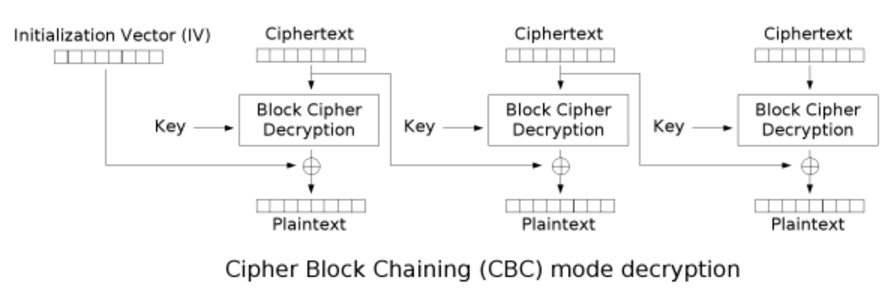
AES ECB mode





AES CBC mode





## {{ CRYPTO\_Name }} Register

### {{ CRYPTO\_CPT\_CTRL\_Name }}

Offset: {{ CRYPTO\_CPT\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_MODE\_Name }}

Offset: {{ CRYPTO\_CPT\_MODE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_MODE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_STATUS\_Name }}

Offset: {{ CRYPTO\_CPT\_STATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_STATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_INT\_EN\_Name }}

Offset: {{ CRYPTO\_CPT\_INT\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_INT\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_INT\_DIS\_Name }}

Offset: {{ CRYPTO\_CPT\_INT\_DIS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_INT\_DIS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_INT\_MASK\_Name }}

Offset: {{ CRYPTO\_CPT\_INT\_MASK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_INT\_MASK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SRC\_ADDR\_Name }}

Offset: {{ CRYPTO\_CPT\_SRC\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SRC\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SRC\_SIZE\_Name }}

Offset: {{ CRYPTO\_CPT\_SRC\_SIZE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SRC\_SIZE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_DST\_ADDR\_Name }}

Offset: {{ CRYPTO\_CPT\_DST\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_DST\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST0\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST1\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST2\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST3\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST4\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST5\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST6\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_SHA\_ST7\_Name }}

Offset: {{ CRYPTO\_CPT\_SHA\_ST7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_SHA\_ST7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_IV0\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_IV0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_IV0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_IV1\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_IV1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_IV1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_IV2\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_IV2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_IV2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_IV3\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_IV3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_IV3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_KEY0\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_KEY0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_KEY0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_KEY1\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_KEY1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_KEY1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_KEY2\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_KEY2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_KEY2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_AES\_KEY3\_Name }}

Offset: {{ CRYPTO\_CPT\_AES\_KEY3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_AES\_KEY3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_CONFIG\_Name }}

Offset: {{ CRYPTO\_CPT\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_VERSION\_Name }}

Offset: {{ CRYPTO\_CPT\_VERSION\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_VERSION\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CRYPTO\_CPT\_FEATURE\_Name }}

Offset: {{ CRYPTO\_CPT\_FEATURE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CRYPTO\_CPT\_FEATURE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ WDT\_Name }}

## Introduction

从IP中来，需要把PDF转成WORD

## Main Features

## Function Description

## Basic Block Diagram

## {{ WDT\_Name }} Register

### {{ WDT\_IDREV\_Name }}

Offset: {{ WDT\_IDREV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in WDT\_IDREV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ WDT\_CTRL\_Name }}

Offset: {{ WDT\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in WDT\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ WDT\_RESTART\_Name }}

Offset: {{ WDT\_RESTART\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in WDT\_RESTART\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ WDT\_WREN\_Name }}

Offset: {{ WDT\_WREN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in WDT\_WREN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ WDT\_ST\_Name }}

Offset: {{ WDT\_ST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in WDT\_ST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ IR\_Name }}

## Introduction

IR (Infrared Radiation) module is designed to send and receive infrared remote control signals.

　　It supports NEC, Toshiba 9012 and Philips RC5 protocols in hardware mode. It also supports other protocols when configured in software mode. The transmitted signals are modulated with carrier frequency. The typical frequency of carrier wave is 38KHz, and duty cycle is 1/3.

## Main Features

- Support AMBA APB bus access

- Support IR transmitting and receiving

- Support NEC, Toshiba 9012 and Philips RC5 protocols in hardware mode

- Support other IR protocols with software programming

- Support programmable carrier frequency and duty cycle

- Support two independent 32\*8 FIFOs

- Use clk\_ir as function clock, pclk as apb clock, and clk\_tx\_ir to generate carrier clock

- Support DMA transfer in software program mode

## Function Description

### Carrier

Why we need carrier? There are many source of Infra-Red light. The sun is the brightest source of all, while light bulbs, candles, central heating system are also the sources of Infra-Red light. Even our bodies radiate Infra-Red light. In fact everything radiates heat, and Infra-Red light.

　　To make sure our IR message receiving without errors, modulation is needed. With modulation we make IR light source blink in a particular frequency. The IR receiver will be turned to that frequency, and ignore others. In modulation, "marks" represent IR light pulsing on and off in a particular frequency. While "space" is the off state, no light emitted.

　　The carrier frequency regularly used are 38KHz, 39.2KHz, 37.916KHz, 42KHz, 40KHz, 44KHz, 38.38KHz and so on. Among them, 38KHz is the most widely used one. 90% infrared radiation transmitters/receivers use 38KHz frequency.

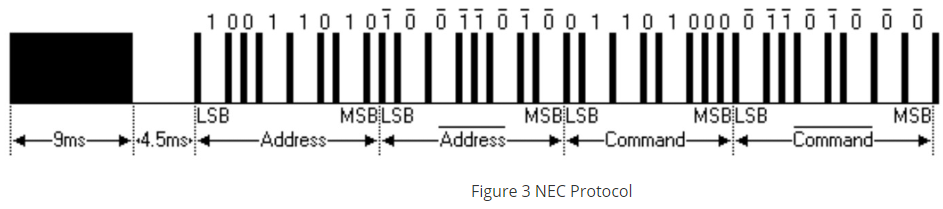
### Protocol

The design support 3 IR protocols: NEC, Toshiba 9012 and Philips RC5.

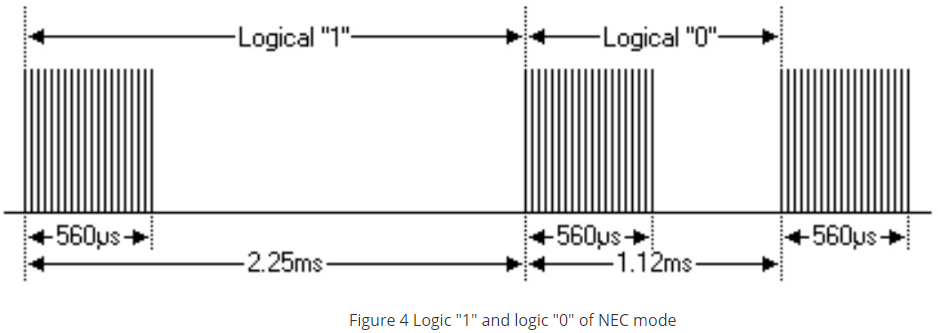
#### Hardware NEC mode

　The NEC protocol contains 8-bit address and 8-bit command. Both address and command are tranmitted twice for reliability. The carrier frequency is 38KHz. Bit time of logic "1" is 2.25ms, and bit time of logic "0" is 1.12ms.

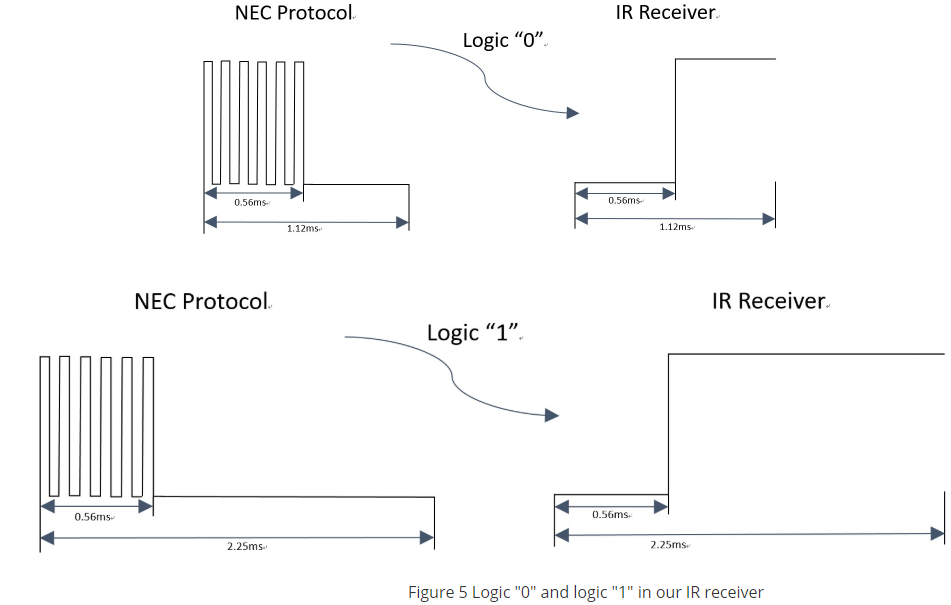
　　The NEC protocol shows below. A message is started with 9ms pulse and 4.5ms space. It's the header of a frame of a message. After that the address and command are both transmitted twice. The second time all bits are inverted and can be used for verification of the received message. The total transmission time is constant because every bit is repeated with its inverted length. During transmission the LSB is transmitted first.



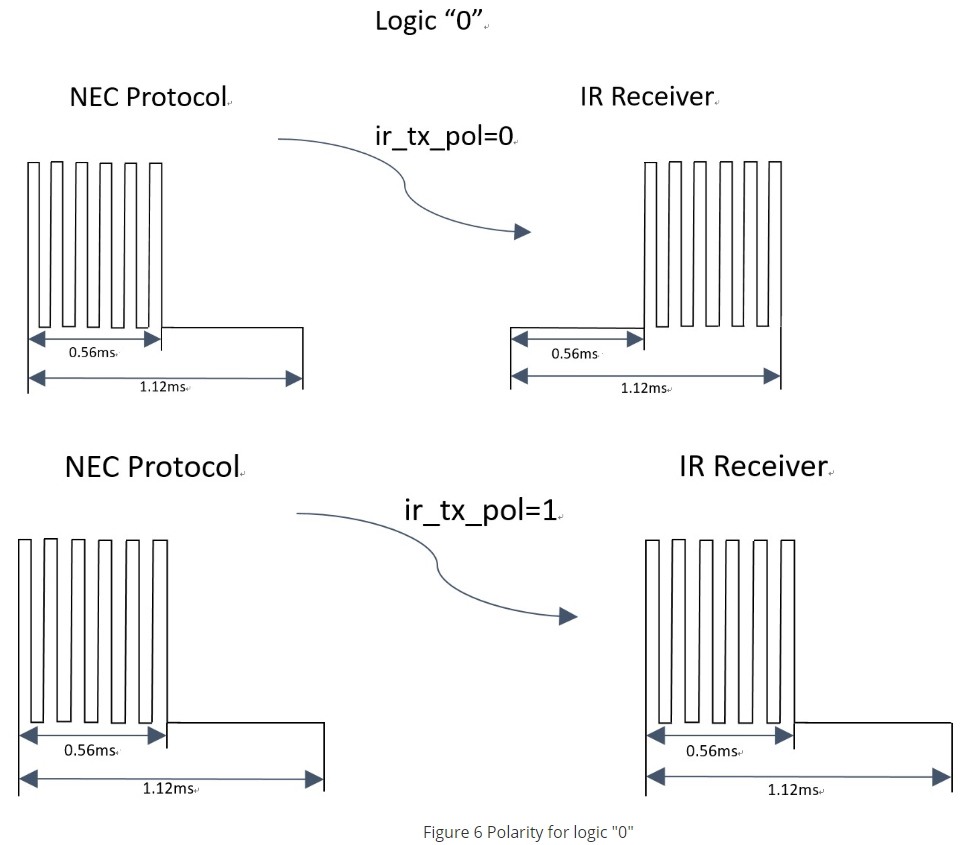
Logic "1" transmitted with 0.56ms pulse first, and total period is 2.25ms. Logic "0" transmitted with 0.56ms pulse first, and total period is 1.12ms. The picture below shows logic "1" and logic "0".



To be noticed, the "pulse" is recognized as level low, while "space" is represented as level high in our IR receivers. The logic "0" and logic "1" in our receiver is recognized as the following picture.

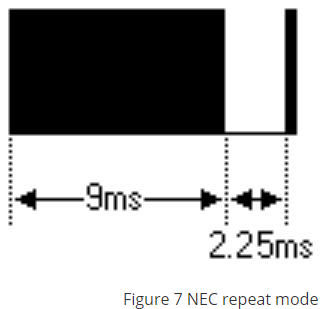


In IR transmitter the output is transmitted with carrier, and the polarity is controlled by register "ir\_tx\_pol". When "ir\_tx\_pol" is "1", the output is just the same as IR protocol. When "ir\_tx\_pol" is "0", the output "mark" and "space" is reversed. Take logic "0" as an example.



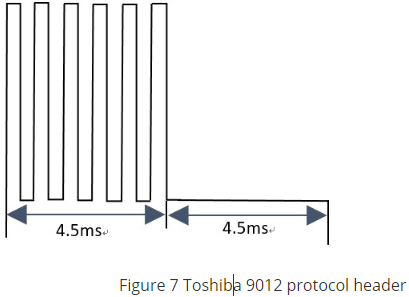
In our design the 8-bit address and 8-bit reversed address are called "usercode". To be honesty, you can write 8-bit address + 8 bit reversed bits into this register, or you can just write 16 bits. It's controlled by software. The 8-bit command and 8-bit reversed command are named as "datacode". Like the usercode, you can also write expand 16 bits or 8-bit + 8-bit reversed.

　　We also support repeat mode in NEC protocol. If the key on the remote control remains pressed, the repeat mode is triggered. Every 110ms a repeat code is transmitted as long as the key remains pressed. The repeat code is simply 9ms pulse followed by a 2.25ms space and 560us pulse.



#### Toshiba

Toshiba 9012 is very similar to NEC mode, it also contains header, usercode and datacode. Unlike NEC protocol, the header of Toshiba 9012 is 4.5ms "mark" + 4.5ms "space".

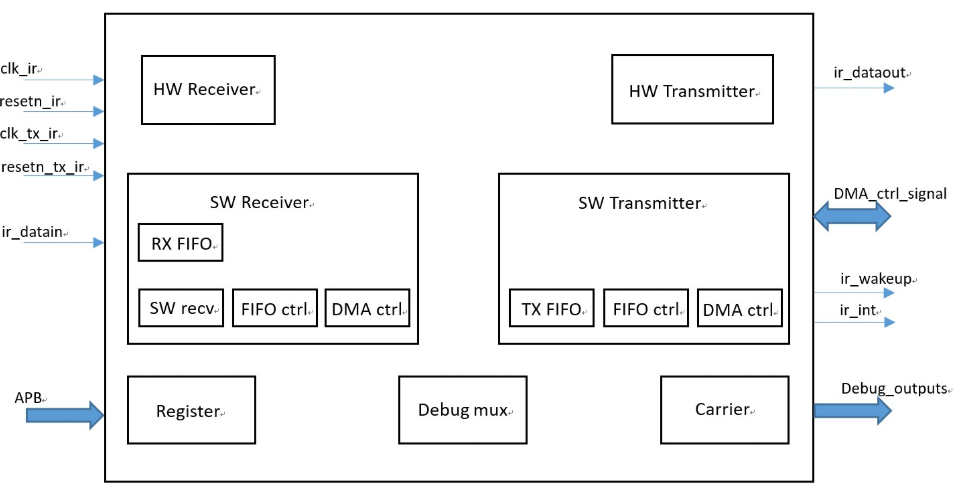


After the header usercode and datacode are transmitted with LSB first. The logic "0" and logic "1" are represented just same as NEC protocol.

#### Philips RC5

The RC-5 code from Philips is possibly the most used protocol by hobbyists, probably because of the wide availability of cheap remote controls. It contains 5-bit address and 6-bit command length. Typical carrier frequency is 36kHz, and constant bit time is 1.778ms.

## Basic Block Diagram



The IR module owns a receiver and a transmitter, both could be configured to software control mode or hardware control mode. In other words, the IR module could be configured into software TX mode, hardware TX mode, software RX mode, hardware RX mode.

　　In software mode, it performs serial-to-parallel conversion on data received from input pad, and parallel-to-serial conversion on data transmitted to output pad. CPU or DMA is responsible for dealing with parallel data between IR FIFO and external memory.

　　The RX FIFO and TX FIFO are both 32\*8, which could be written and read by the processor core over APB bus. CPU can directly write or read these entries. However, DMA operation is more recommended.



　　　　　　　　　　　　　　　　Figure 2 Data Structure

　　The data structure is shown in Figure 2. Each 32-bit value contains two field, "level" indicates whether a high/low level value was received or is going to be transmitted, and "period" is the duration (numbers of clk\_ir clk cycles) for which the level lasts. As in transmit mode, a zero period is interpreted as an end-marker. The transmitter will transmit "thres" (in register "ir\_idle\_thres") instead once it reads this value, and generated transmit ok interrupt.

　　Once the receiver is enable, it measures the duration between input signal edges. The duration measured by clk\_ir clock cycle will be written as "period", the input signal level will also be written into "level" field. The data structure is the same with transmitting. When receiver detects no change in signal level for more than "thres" clock cycle in register "ir\_idle\_thres", the receiver interrupt will be generated.

　　The carrier is generated with input clock clk\_tx\_ir, eg 6MHz, "ir\_carrier\_high" and "ir\_carrier\_low" in register "ir\_carrier\_config" are used to configure the numbers of clk\_tx\_ir clock cycles of output high and output level respectively. "ir\_tx\_pol" in register "ir\_tx\_config" controls the polarity of ir transmit output.

　　After IR transmitted or recevied, an interrupt will be raised. In hardware received mode, an interrupt generated after a complete NEC, Toshiba 9012 or Philips RC5 signals detected. In hardware transmit mode , an interrupt generated after signals transmitted. In software recevied mode, after idle threshold clock cycles of no edge detected, an interrupt is generated. In software transmit mode, a transmit data of zero length indicates the end of transmission (notice: set \*txdata\_hi\_lo\* to "1"), and an interrupt will be generated.

## Programming Guide

### NEC receive

- Configure GPIO

- IR module enable

- Set NEC mode

- Set RX mode

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR received\_ok status, clear interrupt

### NEC transmit

- Configure GPIO

- IR module enable

- Set NEC mode

- Set TX mode

- Configure carry high and carry low

- Set time s1, s3, bit time 1, 2 and bit cycle

- Set tx usercode and datacode

- Set tx polarity

- Enable interrupt

- Enable IR

- Set tx\_start

- Wait for interrupt

- Check IR transmit\_ok status, clear interrupt

### NEC repeat receive

- Configure GPIO

- IR module enable

- Set NEC mode

- Set RX mode

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR received\_ok status, clear interrupt

- Enable interrupt

- Check IR repest status, clear interrupt

### NEC repeat transmit

- Configure GPIO

- IR module enable

- Set NEC mode

- Set TX mode

- Configure carry high and carry low

- Set time s1, s3, bit time 1, 2 and bit cycle

- Set tx usercode and datacode

- Set tx polarity

- Enable interrupt

- Enable IR

- Set tx\_start

- Wait for interrupt

- Check IR transmit\_ok status, clear interrupt

- Set time s2, s4

- Set tx repeat mode

- Set tx\_start

- Wait for interrupt

- Check IR repest status, clear interrupt

### Toshiba 9012 receive

- Configure GPIO

- IR module enable

- Set 9012 mode

- Set RX mode

- Set time s1, s2, s3, s4

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR received\_ok status, clear interrupt

### Toshiba 9012 transmit

- Configure GPIO

- IR module enable

- Set 9012 mode

- Set TX mode

- Configure carry high and carry low

- Set time s1, s3, bit time 1, 2 and bit cycle

- Set tx usercode and datacode

- Set tx polarity

- Enable interrupt

- Enable IR

- Set tx\_start

- Wait for interrupt

- Check IR transmit\_ok status, clear interrupt

### Philips RC5 receive

- Configure GPIO

- IR module enable

- Set RC5 mode

- Set RX mode

- Set time s1, s2, s3, s4

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR received\_ok status, clear interrupt

### Philips RC5 transmit

* Configure GPIO
* IR module enable
* Set RC5 mode
* Set TX mode
* Configure carry high and carry low
* Set time s1, bit time 1 and bit cycle
* Set tx usercode and datacode
* Set tx polarity
* Enable interrupt
* Enable IR
* Set tx\_start
* Wait for interrupt
* Check IR transmit\_ok status, clear interrupt

### software receive

- Configure DMA for ir software receiving

- IR module enable

- Set software mode

- Set RX mode

- Configure rx DMA reg condition

- Enable rx DMA

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR received\_ok status, clear interrupt

### software transmit

- preparing data to be transmitted

- Configure DMA for ir software transmitting

- IR module enable

- Set software mode

- Set TX mode

- Configure carry high and carry low

- Set time s1, bit time 1 and bit cycle

- Set tx usercode and datacode

- Set tx polarity

- Configure tx DMA reg condition

- Enable tx DMA

- Enable interrupt

- Enable IR

- Wait for interrupt

- Check IR transmit\_ok status, clear interrupt

## {{ IR\_Name }} Register

### {{ IR\_IR\_CTRL\_Name }}

Offset: {{ IR\_IR\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TX\_CONFIG\_Name }}

Offset: {{ IR\_IR\_TX\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TX\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_CARRY\_CONFIG\_Name }}

Offset: {{ IR\_IR\_CARRY\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_CARRY\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TIME\_1\_Name }}

Offset: {{ IR\_IR\_TIME\_1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TIME\_1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TIME\_2\_Name }}

Offset: {{ IR\_IR\_TIME\_2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TIME\_2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TIME\_3\_Name }}

Offset: {{ IR\_IR\_TIME\_3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TIME\_3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TIME\_4\_Name }}

Offset: {{ IR\_IR\_TIME\_4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TIME\_4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TIME\_5\_Name }}

Offset: {{ IR\_IR\_TIME\_5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TIME\_5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_RX\_CODE\_Name }}

Offset: {{ IR\_IR\_RX\_CODE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_RX\_CODE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TX\_CODE\_Name }}

Offset: {{ IR\_IR\_TX\_CODE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TX\_CODE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_FSM\_Name }}

Offset: {{ IR\_IR\_FSM\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_FSM\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_TX\_FIFO\_Name }}

Offset: {{ IR\_IR\_TX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_TX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_RX\_FIFO\_Name }}

Offset: {{ IR\_IR\_RX\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_RX\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_DMA\_CONFIG\_Name }}

Offset: {{ IR\_IR\_DMA\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_DMA\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_FIFO\_CONFIG\_Name }}

Offset: {{ IR\_IR\_FIFO\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_FIFO\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_CLEAR\_STATUS\_Name }}

Offset: {{ IR\_IR\_CLEAR\_STATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_CLEAR\_STATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ IR\_IR\_IDLE\_THRES\_Name }}

Offset: {{ IR\_IR\_IDLE\_THRES\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in IR\_IR\_IDLE\_THRES\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ I2C\_Name }}

## Introduction

Andes IP 需要PDF转word

## Main Features

## Function Description

## Basic Block Diagram

## {{ I2C\_Name }} Register

### {{ I2C\_IDREV\_Name }}

Offset: {{ I2C\_IDREV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_IDREV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_CFG\_Name }}

Offset: {{ I2C\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_INTEN\_Name }}

Offset: {{ I2C\_INTEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_INTEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_STATUS\_Name }}

Offset: {{ I2C\_STATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_STATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_ADDR\_Name }}

Offset: {{ I2C\_ADDR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_ADDR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_DATA\_Name }}

Offset: {{ I2C\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_CTRL\_Name }}

Offset: {{ I2C\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_CMD\_Name }}

Offset: {{ I2C\_CMD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_CMD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ I2C\_SETUP\_Name }}

Offset: {{ I2C\_SETUP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in I2C\_SETUP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CP\_UART0\_Name }}

## Introduction

CP的UART0，不开放

## Main Features

## Function Description

## Basic Block Diagram

## {{ CP\_UART0\_Name }} Register

### {{ CP\_UART0\_DATA\_Name }}

Offset: {{ CP\_UART0\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CP\_UART0\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CP\_UART0\_STATE\_Name }}

Offset: {{ CP\_UART0\_STATE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CP\_UART0\_STATE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CP\_UART0\_CTRL\_Name }}

Offset: {{ CP\_UART0\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CP\_UART0\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CP\_UART0\_INTSTATUS\_Name }}

Offset: {{ CP\_UART0\_INTSTATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CP\_UART0\_INTSTATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CP\_UART0\_BAUDDIV\_Name }}

Offset: {{ CP\_UART0\_BAUDDIV\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CP\_UART0\_BAUDDIV\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ SDIO\_Name }}

## Introduction

IP的内容，需要PDF转WORD

## Main Features

## Function Description

## Basic Block Diagram

## {{ SDIO\_Name }} Register

### {{ SDIO\_SDMADR\_Name }}

Offset: {{ SDIO\_SDMADR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_SDMADR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_BSR\_BCR\_Name }}

Offset: {{ SDIO\_BSR\_BCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_BSR\_BCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_ARG1\_Name }}

Offset: {{ SDIO\_ARG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_ARG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_TMR\_CR\_Name }}

Offset: {{ SDIO\_TMR\_CR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_TMR\_CR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_RESP0\_Name }}

Offset: {{ SDIO\_RESP0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_RESP0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_RESP1\_Name }}

Offset: {{ SDIO\_RESP1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_RESP1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_RESP2\_Name }}

Offset: {{ SDIO\_RESP2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_RESP2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_RESP3\_Name }}

Offset: {{ SDIO\_RESP3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_RESP3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_BDP\_Name }}

Offset: {{ SDIO\_BDP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_BDP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_PSR\_Name }}

Offset: {{ SDIO\_PSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_PSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HC1\_PCR\_BGCR\_Name }}

Offset: {{ SDIO\_HC1\_PCR\_BGCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HC1\_PCR\_BGCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CCR\_TCR\_SRR\_Name }}

Offset: {{ SDIO\_CCR\_TCR\_SRR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CCR\_TCR\_SRR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_NISR\_EISR\_Name }}

Offset: {{ SDIO\_NISR\_EISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_NISR\_EISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_NISER\_EISER\_Name }}

Offset: {{ SDIO\_NISER\_EISER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_NISER\_EISER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_NISEN\_EISEN\_Name }}

Offset: {{ SDIO\_NISEN\_EISEN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_NISEN\_EISEN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_AC12ES\_HC2\_Name }}

Offset: {{ SDIO\_AC12ES\_HC2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_AC12ES\_HC2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CAP0\_Name }}

Offset: {{ SDIO\_CAP0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CAP0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CAP1\_Name }}

Offset: {{ SDIO\_CAP1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CAP1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_MCC0\_Name }}

Offset: {{ SDIO\_MCC0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_MCC0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_MCC1\_Name }}

Offset: {{ SDIO\_MCC1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_MCC1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_FACERR\_FERR\_Name }}

Offset: {{ SDIO\_FACERR\_FERR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_FACERR\_FERR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_AESR\_Name }}

Offset: {{ SDIO\_AESR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_AESR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_ALSAR\_Name }}

Offset: {{ SDIO\_ALSAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_ALSAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_AHSAR\_Name }}

Offset: {{ SDIO\_AHSAR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_AHSAR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_PV0\_Name }}

Offset: {{ SDIO\_PV0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_PV0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_PV1\_Name }}

Offset: {{ SDIO\_PV1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_PV1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_PV2\_Name }}

Offset: {{ SDIO\_PV2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_PV2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_PV3\_Name }}

Offset: {{ SDIO\_PV3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_PV3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HCVR\_Name }}

Offset: {{ SDIO\_HCVR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HCVR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR0\_Name }}

Offset: {{ SDIO\_VR0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR1\_Name }}

Offset: {{ SDIO\_VR1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR2\_Name }}

Offset: {{ SDIO\_VR2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR3\_Name }}

Offset: {{ SDIO\_VR3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR4\_Name }}

Offset: {{ SDIO\_VR4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR5\_Name }}

Offset: {{ SDIO\_VR5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR6\_Name }}

Offset: {{ SDIO\_VR6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR7\_Name }}

Offset: {{ SDIO\_VR7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR8\_Name }}

Offset: {{ SDIO\_VR8\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR8\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_VR9\_Name }}

Offset: {{ SDIO\_VR9\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_VR9\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_DHER\_Name }}

Offset: {{ SDIO\_DHER\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_DHER\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HWA\_Name }}

Offset: {{ SDIO\_HWA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HWA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_IPRR\_Name }}

Offset: {{ SDIO\_IPRR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_IPRR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CMCR\_Name }}

Offset: {{ SDIO\_CMCR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CMCR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CMSR\_Name }}

Offset: {{ SDIO\_CMSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CMSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_CMSE\_Name }}

Offset: {{ SDIO\_CMSE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_CMSE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_LWID\_Name }}

Offset: {{ SDIO\_LWID\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_LWID\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HWID\_Name }}

Offset: {{ SDIO\_HWID\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HWID\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_LWIK\_Name }}

Offset: {{ SDIO\_LWIK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_LWIK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HWIK\_Name }}

Offset: {{ SDIO\_HWIK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HWIK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_LWOD\_Name }}

Offset: {{ SDIO\_LWOD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_LWOD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_HWOD\_Name }}

Offset: {{ SDIO\_HWOD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_HWOD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ SDIO\_SCTDP\_Name }}

Offset: {{ SDIO\_SCTDP\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in SDIO\_SCTDP\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CBUTTON\_Name }}

## Introduction

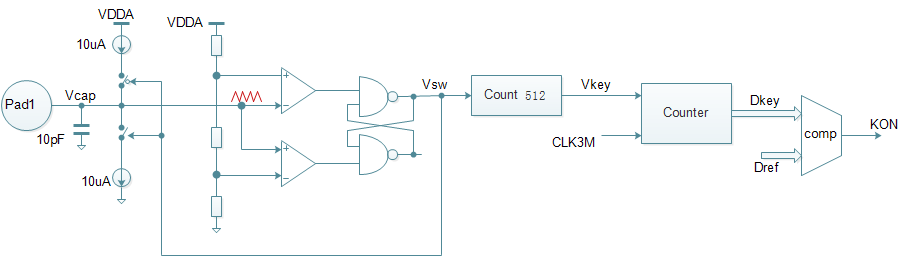
This block is used to control the touch so that correct key data can be sampled and provided to CPU through the co-working of hardware and software.

## Main Features

* APB interface to configure the touch time and configurations
* Interrupt enable is configurable through APB register
* Interrupt signal would be high to notify the CPU key press has been detected when interrupt is enabled
* Multi-key press at the same time is supported

## Function Description

## Basic Block Diagram



**Figure 3-1 Block Diagram**

Figure 3-1 shows the overall scheme of the touch detection and figure 3-2 shows the working waveform. Basically, the analog circuit before vsw is an RC oscillator. When key is pressed, the capacitance would be changed so that the frequency of the oscillator would reflect this change. The count 512 is configurable count. It is used to low the frequency and generate square waveform. The counter is used to count the time when vkey is high to detect the frequency of the analog RC oscillator. Then, by comparing the counter value with the reference value Dref, we can know whether there is key pressing or not. The reference value Dref can be got after initial power on when no key is pressed.

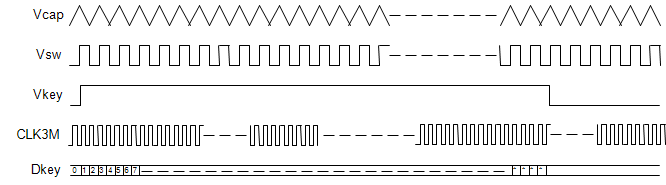


Figure 3-2 working waveform

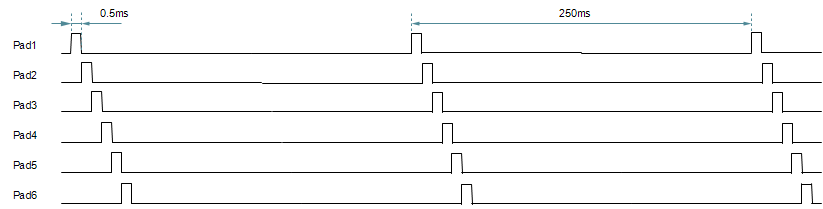


Figure 3-3, Key checking interval

Figure 3-3 shows the key checking sequence. Checking of each key can be done in a short time such as 0.5ms. The key checking of all keys can be done in adjacent time slot one by one. Then, we can power down the circuit to save power consumption for a long time such as 250ms and then start key checking again. When there is key pressing after key checking by using hardware. We can further use software to keep checking the dkey value of one key several times like the waveform shown in Figure 3-4 to make sure there is no incorrect key pressing detected.

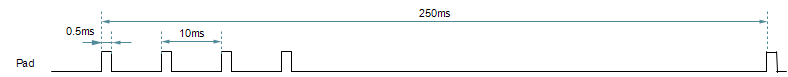


Figure 3-4, Continuous key detection of one key four times

## {{ CBUTTON\_Name }} Register

### {{ CBUTTON\_KEY0\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY0\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY0\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_KEY1\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY1\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY1\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_KEY2\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY2\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY2\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_KEY3\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY3\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY3\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_KEY4\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY4\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY4\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_KEY5\_CONFIG\_Name }}

Offset: {{ CBUTTON\_KEY5\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_KEY5\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_TRAINING\_Name }}

Offset: {{ CBUTTON\_TRAINING\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_TRAINING\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_WAIT\_Name }}

Offset: {{ CBUTTON\_WAIT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_WAIT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_CONFIG\_Name }}

Offset: {{ CBUTTON\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_ANALOG\_CTRL\_Name }}

Offset: {{ CBUTTON\_ANALOG\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_ANALOG\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF0\_Name }}

Offset: {{ CBUTTON\_REF0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF1\_Name }}

Offset: {{ CBUTTON\_REF1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF2\_Name }}

Offset: {{ CBUTTON\_REF2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF3\_Name }}

Offset: {{ CBUTTON\_REF3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF4\_Name }}

Offset: {{ CBUTTON\_REF4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_REF5\_Name }}

Offset: {{ CBUTTON\_REF5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_REF5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_INT\_IRSR\_Name }}

Offset: {{ CBUTTON\_INT\_IRSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_INT\_IRSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA0\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA1\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA2\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA3\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA4\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_RAW\_DATA5\_Name }}

Offset: {{ CBUTTON\_RAW\_DATA5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_RAW\_DATA5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_STEP\_SIZE\_Name }}

Offset: {{ CBUTTON\_STEP\_SIZE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_STEP\_SIZE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_INT\_ISR\_Name }}

Offset: {{ CBUTTON\_INT\_ISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_INT\_ISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_INT\_IMR\_Name }}

Offset: {{ CBUTTON\_INT\_IMR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_INT\_IMR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CBUTTON\_INT\_ICR\_Name }}

Offset: {{ CBUTTON\_INT\_ICR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CBUTTON\_INT\_ICR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

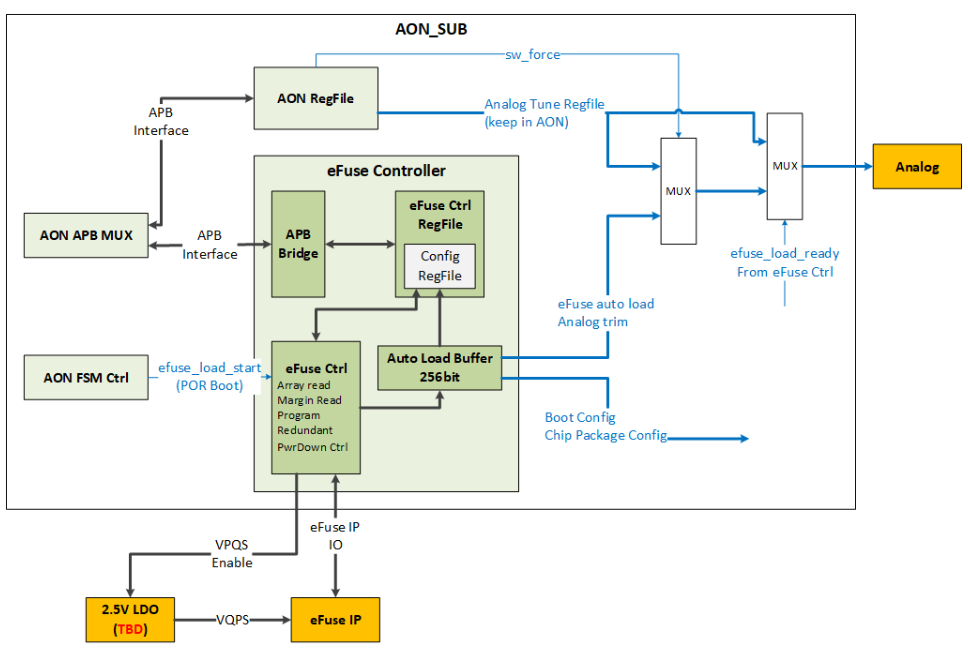
# {{ AON\_EFUSE\_CTRL\_Name }}

## Introduction

## Main Features

## Function Description

## Basic Block Diagram



## Programming Guide

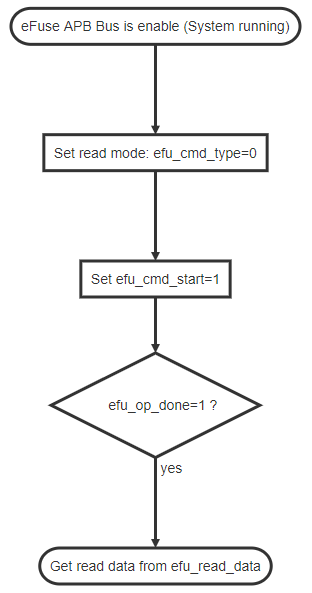
### Array and Margin Read

Note:

1. For register field efu\_cmd\_addr, as the assignment of eFuse bits are always 32-bit. Hence:

- Address [3:0] are 32bit word selection 0 ~ 15.

- Address [8:4] are NOT used in read operation



### Program Mode

Note:

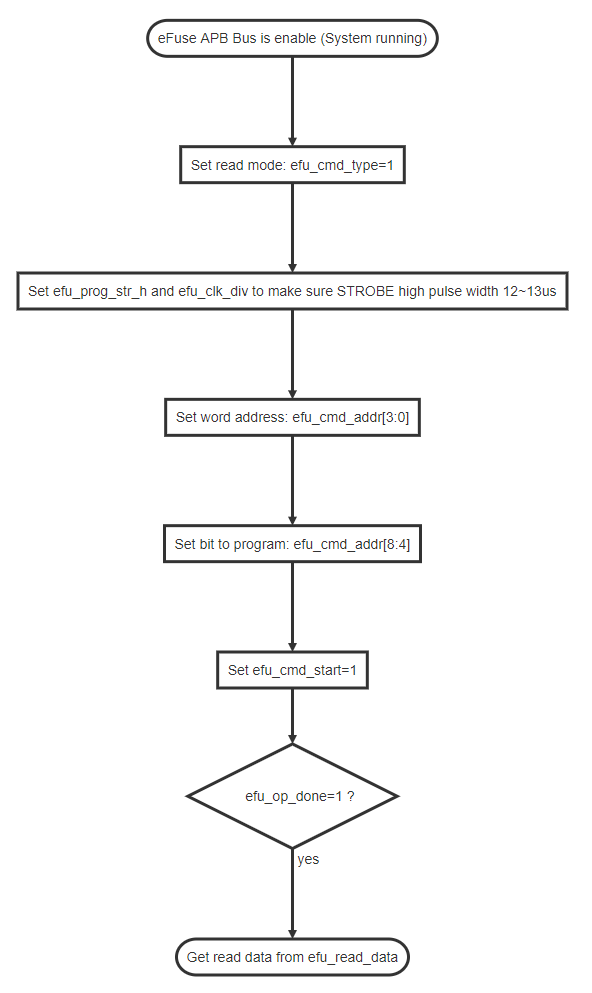
1. For register field efu\_cmd\_addr in program operation:

- Address [8:4] are 32bit selection to program a single bit in each STROBE high pulse.

- Address [3:0] are still 32bit word selection 0 ~ 15

2. eFuse bit NOT programmed, is \*\*default to 0\*\*

3. A bit can ONLY programmed to \*\*1\*\* and \*\*ONLY program once\*\*. Multiple times programming a single bit will cause device error.



### Auto-Load Mode

Note

1. This mode is only start in POR procedure.
2. **First 256 bits** including analog trim, boot configuration and Chip ID are auto-loaded.
3. The auto-load bits can be read from auto\_load\_buffer31:0 ~ auto\_load\_buffer31:0 in eFuse regfile.
4. When auto-load is done, a efuse\_auto\_load\_ready bit can be read from Always-On regfile.

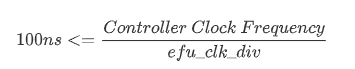
### eFuse Controller Clock Config

#### eFuse Access Timing Requirements

1. CSB/STROBE/PGENB/LOAD信号的切换，均是基于： eFuse controller clock / efu\_clk\_div

2. eFuse Read Timing

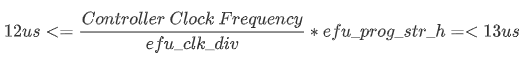
- CSB/STROBE的Setup/Hold分别需要有100ns以上的margin，只需要配置 \*\*efu\_clk\_div\*\*



3. eFuse Program Timing

- 要配置时钟满足eFuse Program STROBE=1 高电平为12-13us

- 要配置 \*\*efu\_clk\_div\*\* 和 \*\*efu\_prog\_str\_h\*\*

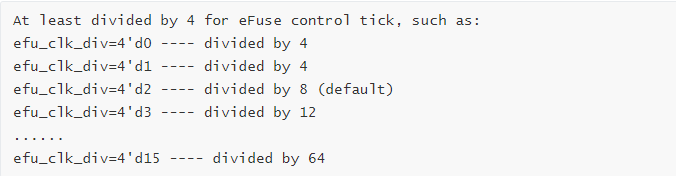


#### Default PCLK: XTAL 24MHz

##### eFuse Controller Clock default: XTAL 24MHz

XTAL 24MHz是系统初始时钟，确保eFuse auto-load正常

##### efu\_clk\_div = 2 (default)

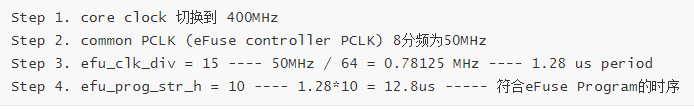


##### XTAL 24MHz / 8 = 3 MHz (default)\*\*

eFuse Read STROBE=1 高电平持续时间333ns，也就是3 MHz的一个tick cycle，确保符合eFuse Read的时序（worst case需要100ns）

#### High Speed PCLK: based on PLL core clock

如果System core clock使用400MHz PLL clock source，eFuse controller PCLK配置参考如下：



## {{ AON\_EFUSE\_CTRL\_Name }} Register

### {{ AON\_EFUSE\_CTRL\_STA\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_STA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_STA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_INT\_EN\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_INT\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_INT\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_CMD\_CTL\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_CMD\_CTL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_CMD\_CTL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_PARA1\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_PARA1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_PARA1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_PARA2\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_PARA2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_PARA2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_RD\_DATA\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_RD\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_RD\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_AUTO\_LOAD\_START\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_AUTO\_LOAD\_START\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_AUTO\_LOAD\_START\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_PROG\_PROTECT\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_PROG\_PROTECT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_PROG\_PROTECT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_PROG\_PROTECT\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_PROG\_PROTECT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_PROG\_PROTECT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_AUTO\_LOAD\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_AUTO\_LOAD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_AUTO\_LOAD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_EFUSE\_CTRL\_DIRECT\_RD\_Name }}

Offset: {{ AON\_EFUSE\_CTRL\_DIRECT\_RD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_EFUSE\_CTRL\_DIRECT\_RD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ PSRAM\_MC\_Name }}

## Introduction

## Main Features

1. support octal SPI with DDR mode(APM protocol PSRAM)
2. clock up to 200Mhz
3. asynchronous working mode with async-FIFO
4. 8-bit command/address/data DQ bus
5. Support 1 chips, support up to 16Mbytes
6. Register configurable write and read initial latencies
7. Support wide operating temperature range by tCEM config register to guarantee robust self-refreshing
8. Support DDR PSRAM with 1K/2K Byte page only.
9. DDR PSRAM controller’s register base address:0xF0800000
10. DDR PSRAM’s memory start:0x6000\_0000(CP), 0x3000\_0000(AP)
11. PVT variation resistance(occasionally re-calibration of delay lines)
12. APM protocol bus protocol compatible
13. Supports up to 5 AHB masters with configurable priority

* fixed priority, round-robin priority and hybrid priority

1. Supports AHB write auto-concatenation
2. Supports AHB read auto-concatenation

## Function Description

## Basic Block Diagram

Below in Fig 1 is the structure of this module.



Fig. 1 Detail Structure

Notes: The accesses of PSRAM mode registers and memory share the same read data FIFO, which has a risk of reading or writing an unknown data when a register and memory access switching happens. A solution is to use separated read FIFOs.

DDR PSRAM controller has some major modules:

DDR AHB slave: AHB memory access from CPU, DMA, Luna, AP2CP master, etc.

DDR PSRAM register: APB register access

DDR interface： DDR signal generation

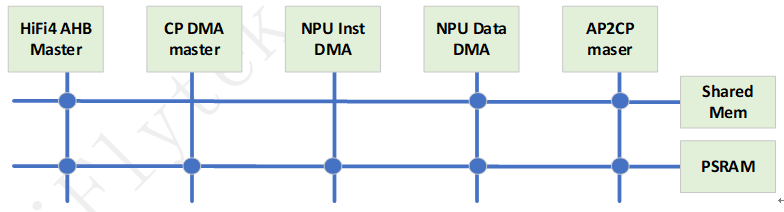
Rd and wr delay chains: delay chains for write and read clock in PHY

FIFOs: 8 FIFOs used for command store and read data buffer

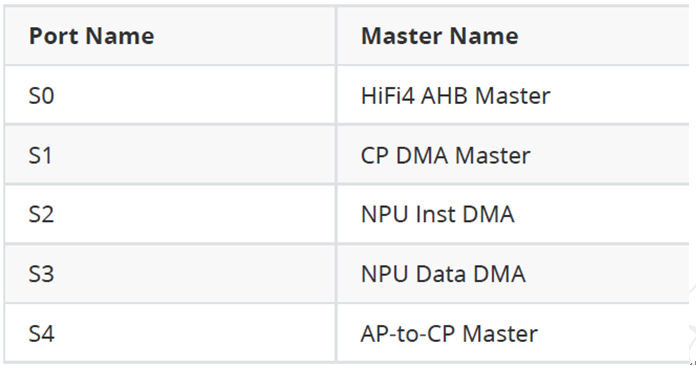
## Sub-modules

### PSRAM controller

#### 系统连接框图



5个Master port各自通过AHB总线连接PSRAM controller，经控制器内部的arbiter访问 PSRAM，port0～port5在Venus项目中实际连接的master如下表所示。



各个端口访问PSRAM的地址，参见Venus\_Chip\_Sepecification的address mapping章节。

### arbiter和FIFO

三种优先级配置：

1. Fixed priority （priority\_ctrl寄存器配置为全0）

Port0 具有最高优先级。port0 至 port5优先级依次降低。

1. 混合优先级

各个port根据priority\_ctrl寄存器对应位所配置的值，分成两组：配置值为1的归并到group1，反之为group0.

group0和group1内各自为round robin；group1和group0为固定优先级：group1高于group1。

3）round-roubin （priority\_ctrl寄存器配置为全1）

各个port的AHB读/写命令，经arbiter之后：

1. 读或写命令进入深度为8的cmd FIFO; 写数据进入32x32-bit wdata FIFO.
2. 每一个port有独立的32x32-bit read FIFO。可最多缓存两个burst16读自动拼接时读取的数据。
3. 所有的port共享一个32x32-bit wdata FIFO.

无正在执行的读命令的情况下，可缓存AHB 写数据个数：

最多2个burst16，或4个burst8，或8个burst4/sngl

### AHB读访问

|  |  |
| --- | --- |
| **读访问类型** | **支持特性** |
| 32-bit WORD  1）sngl 访问 2）INCR 访问（不定长） 3）burst 4/8/16 4）wrap 4/8/16 | 1) wrap类型的访问，必须配置psram mode register 8 bit[2:0]选择合适的wrap模式  2) 读自动拼接：  - 使能ddr\_preft寄存器的rconcat位，支持burst 4/8/16和不定长INCR；设置psram mode register 8 的bit[2:0]==3’b011,即wrap 1K。  - 不支持wrap 4/8/16、SNGL类型的读拼接 |
| BYTE/hword： 1）sngl 访问 2）INCR 访问（不定长） 3）burst 4/8/16 4）wrap 4/8/16 | 不支持自动拼接，且所有的访问都拆分为SNGL读访问。 |
| RAW （read after write）hit | 支持简单的RAW （read after write）hit功能：  若读和写都保持相同长度的访问，如同为burst4，则可使能RAW hit功能。  当新的读命令进入cmd fifo时，若cmd fifo中还有等待的psram 写命令，而且其地址和读命令的地址相同，则直接从 wdata fifo中读取数据，提高访问速度。 |

* + 1. AHB写访问

|  |  |
| --- | --- |
| **写访问类型** | **支持特性** |
| 32-bit WORD 1）sngl 访问 2）INCR 访问（不定长） 3）burst 4/8/16 4）wrap 4/8/16 | 1) wrap类型的访问，必须配置psram mode register 8 bit[2:0]选择合适的wrap模式 2) 写自动拼接：  - 使能ddr\_preft寄存器的wconcat位，支持burst 4/8/16；设置psram mode register 8 的bit[2:0]==3’b011,即wrap 1K。  - 不支持wrap 4/8/16，不定长INCR，SNGL。 |
| AHB 写访问(BYTE/hword)： 1）sngl 访问 2）INCR 访问（不定长） 3）burst 4/8/16 4）wrap 4/8/16 | 1）支持自动将byte/hword burst4/8/16 数据拼接成32位后一次写入psram，但不支持前后地址连续burst的自动拼接。 |

注意：

当write dta/cmd buffer中有写数据未清空时，新的读命令必须等待。

## PHY

PHY本身不主动更新DLL。MC通过ctrlupd\_req来发起一次slave DLL更新：复位read FIFO，更新DLL delay。MC可在如发起类似auto-refresh命令时，同时发起ctrlupd\_req请求来更新DLL，适应温度、电压的漂移。

## {{ PSRAM\_MC\_Name }} Register

### {{ PSRAM\_MC\_MEM\_CMD\_Name }}

Offset: {{ PSRAM\_MC\_MEM\_CMD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MEM\_CMD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_TIM\_CONFIG\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_TIM\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_TIM\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_CLK\_CS\_OE\_CTRL\_Name }}

Offset: {{ PSRAM\_MC\_CLK\_CS\_OE\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_CLK\_CS\_OE\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_WAIT\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_WAIT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_WAIT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_MASTER\_CTRL\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_MASTER\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_MASTER\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DLL\_DELAY\_Name }}

Offset: {{ PSRAM\_MC\_DLL\_DELAY\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DLL\_DELAY\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DLL\_OBS\_REG0\_Name }}

Offset: {{ PSRAM\_MC\_DLL\_OBS\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DLL\_OBS\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DLL\_OBS\_REG1\_Name }}

Offset: {{ PSRAM\_MC\_DLL\_OBS\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DLL\_OBS\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_LOCK\_DONE\_Name }}

Offset: {{ PSRAM\_MC\_LOCK\_DONE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_LOCK\_DONE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DLL\_RSTN\_Name }}

Offset: {{ PSRAM\_MC\_DLL\_RSTN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DLL\_RSTN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DLL\_RESYNC\_Name }}

Offset: {{ PSRAM\_MC\_DLL\_RESYNC\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DLL\_RESYNC\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_CHIP\_CONFIG\_Name }}

Offset: {{ PSRAM\_MC\_CHIP\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_CHIP\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_PREFT\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_PREFT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_PREFT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_FIFO\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_FIFO\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_FIFO\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_MISC\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_MISC\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_MISC\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_PRIO\_CTRL\_Name }}

Offset: {{ PSRAM\_MC\_PRIO\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_PRIO\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_CMD\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_CMD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_CMD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_CMD\_EN\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_CMD\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_CMD\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DEBUG\_Name }}

Offset: {{ PSRAM\_MC\_DEBUG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DEBUG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_DDR\_VERSION\_Name }}

Offset: {{ PSRAM\_MC\_DDR\_VERSION\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_DDR\_VERSION\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR0\_Name }}

Offset: {{ PSRAM\_MC\_MR0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR1\_Name }}

Offset: {{ PSRAM\_MC\_MR1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR2\_Name }}

Offset: {{ PSRAM\_MC\_MR2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR3\_Name }}

Offset: {{ PSRAM\_MC\_MR3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR4\_Name }}

Offset: {{ PSRAM\_MC\_MR4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR6\_Name }}

Offset: {{ PSRAM\_MC\_MR6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ PSRAM\_MC\_MR8\_Name }}

Offset: {{ PSRAM\_MC\_MR8\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in PSRAM\_MC\_MR8\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ TRNG\_Name }}

## Introduction

TRNG 模块用于产生随机数，分别由两个部分组成：模拟TRNG模块和数字TRNG模块。模拟TRNG是一个1bit的随机产生器（主要电路为一个振荡周期易受温度、电压以及随机噪声等影响的振荡环）。数字TRNG连续采样 模拟TRNG的 输出，采样完成后，数字TRNG模块自动Power Down 模拟TRNG模块 ，并产生中断，上报软件。

## Main Features

* APB Bus总线的分频时钟作为数字TRNG的采样时钟
* 模拟TRNG 输出的 单比特随机数采样频率不大于200kbps。可由用户通过寄存器配置为 2^9~2^16（指数为9~16的整数，共8个值可选）；
* 支持数字 TRNG模块在冷热delay时间后，开始采样；
* 支持单次采样时间间隔可配置；
* 支持通过AHB Bus读取 数字TRNG 采集的32bit随机数；
* 支持自动低功耗模式。AHB总线读取TRNG 数据后，完成32bit采样后自动Power Down模拟TRNG电路，进入power down模式
* 用户可通过降低采样率提高TRNG熵率（entropy rate）

## Function Description

TRNG的模块主要信号的时序图如下图所示：

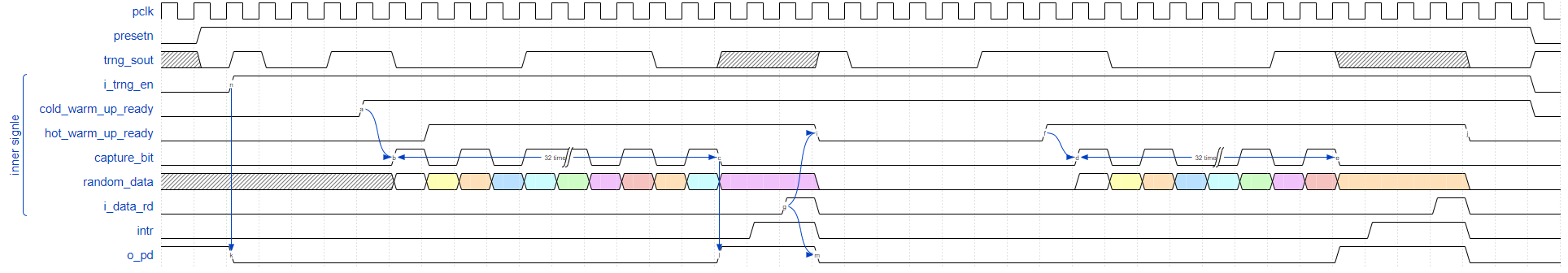


Figure 2 TRNG 时序图

* 通过APB配置i\_trng\_en=1，数字TRNG 模块输出的o\_pd信号拉低，模拟TRNG模块在o\_pd拉低后，开始输出trng\_sout（刚开始模拟输出的trng\_sout信号不稳定，需要延迟采集 ）。
* 在内部计数器计数到CPLD\_TIME时，拉高cold\_warm\_up\_ready信号，此时冷启动完成 。TRNG Core开始采集trng\_sout信号。采样间隔为寄存器配置的DELAY\_TIME。
* 在冷启动完成后，同步开启热启动计数，当内部计数器计数达到 HOT\_TIME时， hot\_warm\_up\_delay信号拉高。
* 在采样数达到32次后，采样结束，此时TRNG Core拉高o\_pd信号，模拟TRNG停止输出trng\_sout信号。
* 通过读取采集到的random\_data数据后，hot\_warm\_up\_ready信号拉低，内部计数器重新开始计数。同时o\_pd信号拉低，模拟TRNG 开始输出trng\_sout信号。
* 在hot\_warm\_up\_ready信号再次拉高后，再次采集32次trng\_sout信号的值 。

## Basic Block Diagram



Figure 1 TRNG Diagram

TRNG 主要 由以下几个主要 模块组成：

* APB Interface：寄存器控制，状态机上报等；
* TRNG CORE：TRNG 控制逻辑，采样逻辑；
* Analog TRNG：TRNG 模拟模块；

## {{ TRNG\_Name }} Register

### {{ TRNG\_TRNG\_CTRL\_Name }}

Offset: {{ TRNG\_TRNG\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_CONFIG\_Name }}

Offset: {{ TRNG\_TRNG\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_STATUS\_Name }}

Offset: {{ TRNG\_TRNG\_STATUS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_STATUS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_INT\_EN\_Name }}

Offset: {{ TRNG\_TRNG\_INT\_EN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_INT\_EN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_INT\_DIS\_Name }}

Offset: {{ TRNG\_TRNG\_INT\_DIS\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_INT\_DIS\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_INT\_MASK\_Name }}

Offset: {{ TRNG\_TRNG\_INT\_MASK\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_INT\_MASK\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_DATA\_Name }}

Offset: {{ TRNG\_TRNG\_DATA\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_DATA\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_TEST\_Name }}

Offset: {{ TRNG\_TRNG\_TEST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_TEST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_VERSION\_Name }}

Offset: {{ TRNG\_TRNG\_VERSION\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_VERSION\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ TRNG\_TRNG\_FEATURE\_Name }}

Offset: {{ TRNG\_TRNG\_FEATURE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in TRNG\_TRNG\_FEATURE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ KEYSENSE\_Name }}

## Introduction

The keysense generates the key sense wakeup signal and ADC hardware trigger signal for key measure.

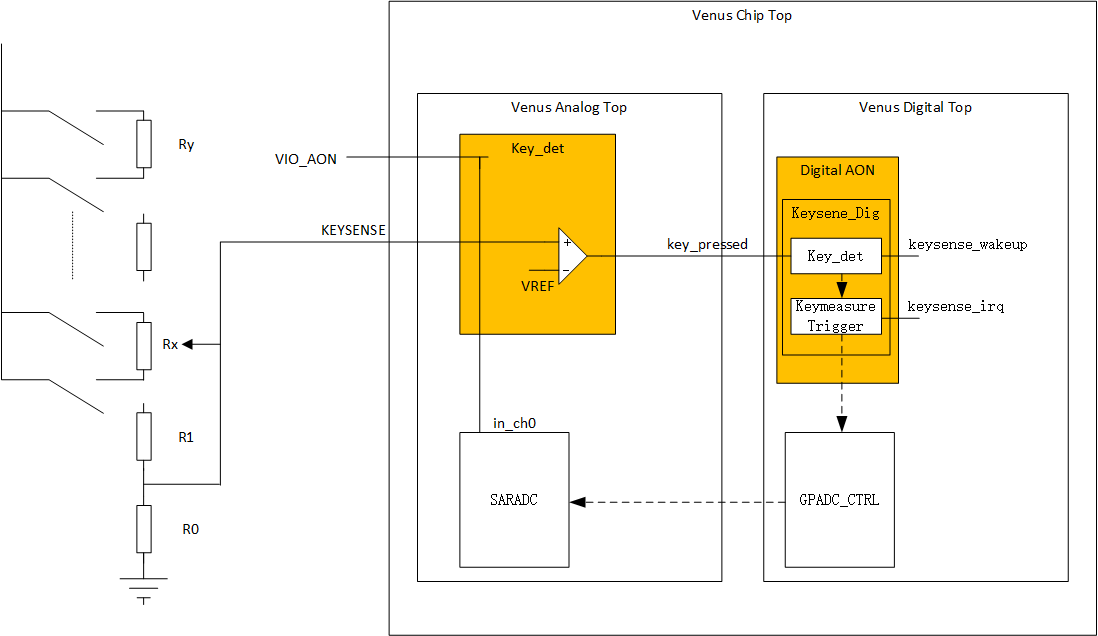


Fig. 1 System application block diagram

The features:

1. Selectable KHz counting clk sources: 32KHz RC osc, 32KHz xtal, a KHz clock divided from 24MHz xtal, etc.
2. Configurable counting threshold for both wakeup and key-measure.
3. Supports key-sense : wakeup and irq.
4. Supports key-measure: hardware SAR ADC triggering control.
5. Supports key-press and key-release irq.

## Main Features

## Function Description

## Basic Block Diagram

Below in Fig 2 is the structure of this module.



Fig. 2 Module Detail Structure

## Programming Guide

1. Set proper value for the wakeup threshold and ADC trigger threshold.
2. Enable the interrupt source needed.
3. Enable keysense.
4. In sleep mode, waking for the key pressing operation and wake up the chip when the key pressing time exceed the wake up threshold. (The wake up signal should be ignored by the AON FSM, when the chip is not in sleep mode. There’s no method to disable the wake up signal in Keysense IP itself. The disable control should be done at the top level.)
5. A wake up/adc\_trigger/keypress/keyrelease irq will be generated if the corresponding interrupt is enabled. AP can respond to the interrupt when it is in active or idle mode.
6. Both in sleep mode or normal working mode, a sensed key can trigger a key-measure operation. Refer to ADC controller spec for more details.

## {{ KEYSENSE\_Name }} Register

### {{ KEYSENSE\_KS\_CFG\_Name }}

Offset: {{ KEYSENSE\_KS\_CFG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_CFG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_STAT\_Name }}

Offset: {{ KEYSENSE\_KS\_STAT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_STAT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_THD\_Name }}

Offset: {{ KEYSENSE\_KS\_THD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_THD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_IMR\_Name }}

Offset: {{ KEYSENSE\_KS\_IMR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_IMR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_ICR\_Name }}

Offset: {{ KEYSENSE\_KS\_ICR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_ICR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_IRSR\_Name }}

Offset: {{ KEYSENSE\_KS\_IRSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_IRSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ KEYSENSE\_KS\_ISR\_Name }}

Offset: {{ KEYSENSE\_KS\_ISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in KEYSENSE\_KS\_ISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ GPADC\_Name }}

## Introduction

* 12-bit resolution, up to 8 channels, up to 1Msps, 24MHz ADC clock
* Configurable hardware ADC trigger sources
* User configurable n-times ADC sampling
* Dedicated ADC Data FIFO for each ADC channel
* Configurable ADC sampling duration
* Configurable waiting time for next Round A/D conversion
* ADC configuration and test logic
* switch on/off control
* ADC trimming
* ADC channel selection
* External/internal VREF selection

## Main Features

## Function Description

* 1. 14-bit to 12-bit ADC data conversion

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| bit num | weight | part2 | part1 | part0 |
| 13 | 1536 | 1024 | 512 | 0 |
| 12 | 1152 | 1024 | 128 | 0 |
| 11 | 640 | 512 | 128 | 0 |
| 10 | 352 | 256 | 64 | 32 |
| 9 | 192 | 128 | 64 | 0 |
| 8 | 104 | 64 | 32 | 8 |
| 7 | 56 | 32 | 16 | 8 |
| 6 | 28 | 16 | 8 | 4 |
| 5 | 16 | 16 | 0 | 0 |
| 4 | 8 | 8 | 0 | 0 |
| 3 | 6 | 4 | 2 | 0 |
| 2 | 3 | 2 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 |
|  | weight sum=4095 | |  |  |

The weight sum of the 14-bit ADC data is 4095, which means it can be exactly represented by a 12-bit binary data.

The bit weight of each bit of the 14-bit ADC data can be further divided into 3 parts as listed in part2/1/0 columns in the above table, so that each part is a 2n number to simplify the calculation.

## Basic Block Diagram

Below in Fig 1 is the structure of this module.



Fig. 1 Detail Structure



## Programming Guide

* 1. ADC application example

1. ADC setup preparation

- Set ADC setup wait time ( ADC\_CR.adc\_setup\_wait register)

- Turn on or off the VREF/VIN buffers

- Select the VREF source; Enable the used ADC channels

- Set an appropriate waiting time before each new round ADC conversion.

- Set the run-round number

- Set FIFO threshold for each ADC channel

2. Enable ADC and wait for the ADC to be setup

- If adc\_complete is HIGH, clear this bit by write 1 to it. Otherwise ADC conversion won’t start even adc\_en=1.

3. Issue a software trigger or waiting for a hardware trigger from keysense

4. Read ADC FIFO data if FIFO threshold reaches

5. Disable ADC if all the n-round conversion is done

## {{ GPADC\_Name }} Register

### {{ GPADC\_ADC\_CR\_Name }}

Offset: {{ GPADC\_ADC\_CR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_CR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_SR\_Name }}

Offset: {{ GPADC\_ADC\_SR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_SR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_CONFIG\_Name }}

Offset: {{ GPADC\_ADC\_CONFIG\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_CONFIG\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_IMR\_Name }}

Offset: {{ GPADC\_ADC\_IMR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_IMR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_ICR\_Name }}

Offset: {{ GPADC\_ADC\_ICR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_ICR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_IRSR\_Name }}

Offset: {{ GPADC\_ADC\_IRSR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_IRSR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_ISR\_Name }}

Offset: {{ GPADC\_ADC\_ISR\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_ISR\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR0\_Name }}

Offset: {{ GPADC\_ADC\_RDR0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR1\_Name }}

Offset: {{ GPADC\_ADC\_RDR1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR2\_Name }}

Offset: {{ GPADC\_ADC\_RDR2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR3\_Name }}

Offset: {{ GPADC\_ADC\_RDR3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR4\_Name }}

Offset: {{ GPADC\_ADC\_RDR4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR5\_Name }}

Offset: {{ GPADC\_ADC\_RDR5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR6\_Name }}

Offset: {{ GPADC\_ADC\_RDR6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_RDR7\_Name }}

Offset: {{ GPADC\_ADC\_RDR7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_RDR7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_FIFO\_THD\_Name }}

Offset: {{ GPADC\_ADC\_FIFO\_THD\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_FIFO\_THD\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_FIFO\_DATA\_CNT\_Name }}

Offset: {{ GPADC\_ADC\_FIFO\_DATA\_CNT\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_FIFO\_DATA\_CNT\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_OFFSET\_A\_Name }}

Offset: {{ GPADC\_ADC\_OFFSET\_A\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_OFFSET\_A\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_GAIN\_A\_Name }}

Offset: {{ GPADC\_ADC\_GAIN\_A\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_GAIN\_A\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_OFFSET\_B\_Name }}

Offset: {{ GPADC\_ADC\_OFFSET\_B\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_OFFSET\_B\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_GAIN\_B\_Name }}

Offset: {{ GPADC\_ADC\_GAIN\_B\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_GAIN\_B\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_OFFSET\_C\_Name }}

Offset: {{ GPADC\_ADC\_OFFSET\_C\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_OFFSET\_C\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_GAIN\_C\_Name }}

Offset: {{ GPADC\_ADC\_GAIN\_C\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_GAIN\_C\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ GPADC\_ADC\_TEST\_Name }}

Offset: {{ GPADC\_ADC\_TEST\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in GPADC\_ADC\_TEST\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ CODEC\_Name }}

## Introduction

在CP端，不开放给用户

## Main Features

## Function Description

## Basic Block Diagram

## {{ CODEC\_Name }} Register

### {{ CODEC\_AUD\_R0\_RSVD\_REG0\_Name }}

Offset: {{ CODEC\_AUD\_R0\_RSVD\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R0\_RSVD\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R1\_GLOBAL0\_Name }}

Offset: {{ CODEC\_AUD\_R1\_GLOBAL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R1\_GLOBAL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R2\_GLOBAL1\_Name }}

Offset: {{ CODEC\_AUD\_R2\_GLOBAL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R2\_GLOBAL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R3\_RSVD\_REG1\_Name }}

Offset: {{ CODEC\_AUD\_R3\_RSVD\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R3\_RSVD\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R4\_RSVD\_REG2\_Name }}

Offset: {{ CODEC\_AUD\_R4\_RSVD\_REG2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R4\_RSVD\_REG2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R5\_ADC\_CTRL0\_Name }}

Offset: {{ CODEC\_AUD\_R5\_ADC\_CTRL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R5\_ADC\_CTRL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R6\_ADC\_CTRL1\_Name }}

Offset: {{ CODEC\_AUD\_R6\_ADC\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R6\_ADC\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R7\_ADC\_CTRL2\_Name }}

Offset: {{ CODEC\_AUD\_R7\_ADC\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R7\_ADC\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R8\_ADC\_CTRL3\_Name }}

Offset: {{ CODEC\_AUD\_R8\_ADC\_CTRL3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R8\_ADC\_CTRL3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R9\_ADC\_CTRL4\_Name }}

Offset: {{ CODEC\_AUD\_R9\_ADC\_CTRL4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R9\_ADC\_CTRL4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R10\_ADC\_CTRL5\_Name }}

Offset: {{ CODEC\_AUD\_R10\_ADC\_CTRL5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R10\_ADC\_CTRL5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R11\_ADC\_CTRL6\_Name }}

Offset: {{ CODEC\_AUD\_R11\_ADC\_CTRL6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R11\_ADC\_CTRL6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R12\_ADC\_CTRL7\_Name }}

Offset: {{ CODEC\_AUD\_R12\_ADC\_CTRL7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R12\_ADC\_CTRL7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R13\_RSVD\_REG3\_Name }}

Offset: {{ CODEC\_AUD\_R13\_RSVD\_REG3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R13\_RSVD\_REG3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R14\_RSVD\_REG4\_Name }}

Offset: {{ CODEC\_AUD\_R14\_RSVD\_REG4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R14\_RSVD\_REG4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R15\_DAC\_CTRL0\_Name }}

Offset: {{ CODEC\_AUD\_R15\_DAC\_CTRL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R15\_DAC\_CTRL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R16\_DAC\_CTRL1\_Name }}

Offset: {{ CODEC\_AUD\_R16\_DAC\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R16\_DAC\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R17\_DAC\_CTRL2\_Name }}

Offset: {{ CODEC\_AUD\_R17\_DAC\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R17\_DAC\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R18\_DAC\_CTRL3\_Name }}

Offset: {{ CODEC\_AUD\_R18\_DAC\_CTRL3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R18\_DAC\_CTRL3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R19\_DAC\_CTRL4\_Name }}

Offset: {{ CODEC\_AUD\_R19\_DAC\_CTRL4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R19\_DAC\_CTRL4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R20\_DAC\_CTRL5\_Name }}

Offset: {{ CODEC\_AUD\_R20\_DAC\_CTRL5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R20\_DAC\_CTRL5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R21\_DAC\_CTRL6\_Name }}

Offset: {{ CODEC\_AUD\_R21\_DAC\_CTRL6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R21\_DAC\_CTRL6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R22\_DAC\_CTRL7\_Name }}

Offset: {{ CODEC\_AUD\_R22\_DAC\_CTRL7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R22\_DAC\_CTRL7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ CODEC\_AUD\_R25\_STATUS0\_Name }}

Offset: {{ CODEC\_AUD\_R25\_STATUS0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in CODEC\_AUD\_R25\_STATUS0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ AON\_CODEC\_Name }}

## Introduction

在CP端，不开放给用户

## Main Features

## Function Description

## Basic Block Diagram

## {{ AON\_CODEC\_Name }} Register

### {{ AON\_CODEC\_AUD\_R0\_RSVD\_REG0\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R0\_RSVD\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R0\_RSVD\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R1\_GLOBAL0\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R1\_GLOBAL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R1\_GLOBAL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R2\_GLOBAL1\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R2\_GLOBAL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R2\_GLOBAL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R3\_RSVD\_REG1\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R3\_RSVD\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R3\_RSVD\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R4\_RSVD\_REG2\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R4\_RSVD\_REG2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R4\_RSVD\_REG2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R5\_ADC\_CTRL0\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R5\_ADC\_CTRL0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R5\_ADC\_CTRL0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R6\_ADC\_CTRL1\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R6\_ADC\_CTRL1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R6\_ADC\_CTRL1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R7\_ADC\_CTRL2\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R7\_ADC\_CTRL2\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R7\_ADC\_CTRL2\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R8\_ADC\_CTRL3\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R8\_ADC\_CTRL3\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R8\_ADC\_CTRL3\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R9\_ADC\_CTRL4\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R9\_ADC\_CTRL4\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R9\_ADC\_CTRL4\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R10\_ADC\_CTRL5\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R10\_ADC\_CTRL5\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R10\_ADC\_CTRL5\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R11\_ADC\_CTRL6\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R11\_ADC\_CTRL6\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R11\_ADC\_CTRL6\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R12\_ADC\_CTRL7\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R12\_ADC\_CTRL7\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R12\_ADC\_CTRL7\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ AON\_CODEC\_AUD\_R25\_STATUS0\_Name }}

Offset: {{ AON\_CODEC\_AUD\_R25\_STATUS0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in AON\_CODEC\_AUD\_R25\_STATUS0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

# {{ FLASH\_DL\_Name }}

## Introduction

不开放用户

## Main Features

## Function Description

## Basic Block Diagram

## {{ FLASH\_DL\_Name }} Register

### {{ FLASH\_DL\_CTRL\_Name }}

Offset: {{ FLASH\_DL\_CTRL\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_CTRL\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_DELAY\_Name }}

Offset: {{ FLASH\_DL\_DELAY\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_DELAY\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_OBS\_REG0\_Name }}

Offset: {{ FLASH\_DL\_OBS\_REG0\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_OBS\_REG0\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_OBS\_REG1\_Name }}

Offset: {{ FLASH\_DL\_OBS\_REG1\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_OBS\_REG1\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_LOCK\_DONE\_Name }}

Offset: {{ FLASH\_DL\_LOCK\_DONE\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_LOCK\_DONE\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_RSTN\_Name }}

Offset: {{ FLASH\_DL\_RSTN\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_RSTN\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |

### {{ FLASH\_DL\_RESYNC\_Name }}

Offset: {{ FLASH\_DL\_RESYNC\_Offset }}

|  |  |  |
| --- | --- | --- |
| {%tc for col in Module\_Register\_Col\_Labels %} | {{ col }} | {%tc endfor %} |
| {%tr for item in FLASH\_DL\_RESYNC\_contents %} | | |
| {%tc for col in item %} | {{ col }} | {%tc endfor %} |
| {%tr endfor %} | | |