

Fast Models

Version 11.9

Fixed Virtual Platforms (FVP) Reference Guide

arm

Fast Models

Fixed Virtual Platforms (FVP) Reference Guide

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Release Information

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Contents

Fast Models Fixed Virtual Platforms (FVP) Reference Guide

Preface

<i>About this book</i>	9
------------------------------	---

Chapter 1

Introduction

1.1 <i>About FVPs</i>	1-12
1.2 <i>Data collection in FVPs</i>	1-13

Chapter 2

Getting Started with Fixed Virtual Platforms

2.1 <i>Loading and running an application on an FVP</i>	2-15
2.2 <i>Configuring the model</i>	2-16
2.3 <i>FVP debug</i>	2-17
2.4 <i>Using the CLCD window</i>	2-18
2.5 <i>Ethernet with VE FVPs</i>	2-21
2.6 <i>Using a terminal with a system model</i>	2-23
2.7 <i>Virtio P9 device component</i>	2-25

Chapter 3

Base Platform FVPs

3.1 <i>FVP_Base_AEMv8A</i>	3-28
3.2 <i>FVP_Base_AEMv8A-AEMv8A</i>	3-37
3.3 <i>FVP_Base_Cortex-A32x1</i>	3-48
3.4 <i>FVP_Base_Cortex-A32x2</i>	3-56
3.5 <i>FVP_Base_Cortex-A32x4</i>	3-65

3.6	<i>FVP_Base_Cortex-A35x1</i>	3-74
3.7	<i>FVP_Base_Cortex-A35x2</i>	3-82
3.8	<i>FVP_Base_Cortex-A35x4</i>	3-91
3.9	<i>FVP_Base_Cortex-A53x1</i>	3-100
3.10	<i>FVP_Base_Cortex-A53x2</i>	3-108
3.11	<i>FVP_Base_Cortex-A53x4</i>	3-116
3.12	<i>FVP_Base_Cortex-A55</i>	3-125
3.13	<i>FVP_Base_Cortex-A55+Cortex-A76</i>	3-135
3.14	<i>FVP_Base_Cortex-A55x1</i>	3-144
3.15	<i>FVP_Base_Cortex-A55x1+Cortex-A75x1</i>	3-152
3.16	<i>FVP_Base_Cortex-A55x2</i>	3-161
3.17	<i>FVP_Base_Cortex-A55x2+Cortex-A75x2</i>	3-170
3.18	<i>FVP_Base_Cortex-A55x4</i>	3-179
3.19	<i>FVP_Base_Cortex-A55x4+Cortex-A75x1</i>	3-188
3.20	<i>FVP_Base_Cortex-A55x4+Cortex-A75x2</i>	3-197
3.21	<i>FVP_Base_Cortex-A55x4+Cortex-A75x4</i>	3-206
3.22	<i>FVP_Base_Cortex-A55x4+Cortex-A76x2</i>	3-215
3.23	<i>FVP_Base_Cortex-A57x1</i>	3-224
3.24	<i>FVP_Base_Cortex-A57x1-A35x1</i>	3-232
3.25	<i>FVP_Base_Cortex-A57x1-A53x1</i>	3-241
3.26	<i>FVP_Base_Cortex-A57x2</i>	3-251
3.27	<i>FVP_Base_Cortex-A57x2-A35x4</i>	3-260
3.28	<i>FVP_Base_Cortex-A57x2-A53x4</i>	3-270
3.29	<i>FVP_Base_Cortex-A57x4</i>	3-280
3.30	<i>FVP_Base_Cortex-A57x4-A35x4</i>	3-289
3.31	<i>FVP_Base_Cortex-A57x4-A53x4</i>	3-300
3.32	<i>FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2</i>	3-311
3.33	<i>FVP_Base_Cortex-A65AEx4</i>	3-320
3.34	<i>FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4</i>	3-330
3.35	<i>FVP_Base_Cortex-A65AEx8</i>	3-340
3.36	<i>FVP_Base_Cortex-A65x1</i>	3-351
3.37	<i>FVP_Base_Cortex-A65x2</i>	3-359
3.38	<i>FVP_Base_Cortex-A65x4</i>	3-368
3.39	<i>FVP_Base_Cortex-A72x1</i>	3-378
3.40	<i>FVP_Base_Cortex-A72x1-A53x1</i>	3-386
3.41	<i>FVP_Base_Cortex-A72x2</i>	3-395
3.42	<i>FVP_Base_Cortex-A72x2-A53x4</i>	3-404
3.43	<i>FVP_Base_Cortex-A72x4</i>	3-415
3.44	<i>FVP_Base_Cortex-A72x4-A53x4</i>	3-424
3.45	<i>FVP_Base_Cortex-A73x1</i>	3-435
3.46	<i>FVP_Base_Cortex-A73x1-A53x1</i>	3-443
3.47	<i>FVP_Base_Cortex-A73x2</i>	3-452
3.48	<i>FVP_Base_Cortex-A73x2-A53x4</i>	3-460
3.49	<i>FVP_Base_Cortex-A73x4</i>	3-471
3.50	<i>FVP_Base_Cortex-A75x1</i>	3-480
3.51	<i>FVP_Base_Cortex-A75x2</i>	3-488
3.52	<i>FVP_Base_Cortex-A75x4</i>	3-497
3.53	<i>FVP_Base_Cortex-A76</i>	3-506
3.54	<i>FVP_Base_Cortex-A76AEx2</i>	3-515
3.55	<i>FVP_Base_Cortex-A76AEx4</i>	3-525

3.56	<i>FVP_Base_Cortex-A76x1</i>	3-535
3.57	<i>FVP_Base_Cortex-A76x2</i>	3-543
3.58	<i>FVP_Base_Cortex-A76x4</i>	3-552
3.59	<i>FVP_Base_Cortex-A77x1</i>	3-561
3.60	<i>FVP_Base_Cortex-A77x2</i>	3-569
3.61	<i>FVP_Base_Cortex-A77x4</i>	3-577
3.62	<i>FVP_Base_Neoverse-E1x1</i>	3-586
3.63	<i>FVP_Base_Neoverse-E1x2</i>	3-594
3.64	<i>FVP_Base_Neoverse-E1x4</i>	3-603
3.65	<i>FVP_Base_Neoverse-N1x1</i>	3-612
3.66	<i>FVP_Base_Neoverse-N1x2</i>	3-620
3.67	<i>FVP_Base_Neoverse-N1x4</i>	3-629
3.68	<i>FVP_Base_RevC-2xAEMv8A</i>	3-638

Chapter 4

BaseR platform FVPs

4.1	<i>FVP_BaseR_Cortex-R52x1</i>	4-652
4.2	<i>FVP_BaseR_Cortex-R52x2</i>	4-661
4.3	<i>FVP_BaseR_Cortex-R52x4</i>	4-670

Chapter 5

VE Platform FVPs

5.1	<i>FVP_VE_Cortex-A15x1</i>	5-681
5.2	<i>FVP_VE_Cortex-A15x1-A7x1</i>	5-689
5.3	<i>FVP_VE_Cortex-A15x2</i>	5-698
5.4	<i>FVP_VE_Cortex-A15x2-A7x2</i>	5-706
5.5	<i>FVP_VE_Cortex-A15x4</i>	5-715
5.6	<i>FVP_VE_Cortex-A15x4-A7x4</i>	5-723
5.7	<i>FVP_VE_Cortex-A17x1</i>	5-734
5.8	<i>FVP_VE_Cortex-A17x1-A7x1</i>	5-742
5.9	<i>FVP_VE_Cortex-A17x2</i>	5-751
5.10	<i>FVP_VE_Cortex-A17x4</i>	5-759
5.11	<i>FVP_VE_Cortex-A17x4-A7x4</i>	5-768
5.12	<i>FVP_VE_Cortex-A5x1</i>	5-778
5.13	<i>FVP_VE_Cortex-A5x2</i>	5-786
5.14	<i>FVP_VE_Cortex-A5x4</i>	5-794
5.15	<i>FVP_VE_Cortex-A7x1</i>	5-803
5.16	<i>FVP_VE_Cortex-A7x2</i>	5-811
5.17	<i>FVP_VE_Cortex-A7x4</i>	5-819
5.18	<i>FVP_VE_Cortex-A9x1</i>	5-828
5.19	<i>FVP_VE_Cortex-A9x2</i>	5-836
5.20	<i>FVP_VE_Cortex-A9x4</i>	5-844
5.21	<i>FVP_VE_Cortex-R4</i>	5-853
5.22	<i>FVP_VE_Cortex-R5x1</i>	5-860
5.23	<i>FVP_VE_Cortex-R5x2</i>	5-868
5.24	<i>FVP_VE_Cortex-R7x1</i>	5-875
5.25	<i>FVP_VE_Cortex-R7x2</i>	5-882
5.26	<i>FVP_VE_Cortex-R8x1</i>	5-889
5.27	<i>FVP_VE_Cortex-R8x2</i>	5-896
5.28	<i>FVP_VE_Cortex-R8x4</i>	5-903

Chapter 6

MPS2 Platform FVPs

6.1	<i>FVP_MPS2_AEMv8M</i>	6-911
6.2	<i>FVP_MPS2_Cortex-M0</i>	6-925
6.3	<i>FVP_MPS2_Cortex-M0plus</i>	6-940
6.4	<i>FVP_MPS2_Cortex-M23</i>	6-955
6.5	<i>FVP_MPS2_Cortex-M3</i>	6-970
6.6	<i>FVP_MPS2_Cortex-M33</i>	6-984
6.7	<i>FVP_MPS2_Cortex-M35P</i>	6-999
6.8	<i>FVP_MPS2_Cortex-M4</i>	6-1014
6.9	<i>FVP_MPS2_Cortex-M7</i>	6-1028
6.10	<i>FVP_MPS2_SSE-200_AEMv8M_pipeline</i>	6-1042
6.11	<i>FVP_MPS2_SSE-200_Cortex-M33</i>	6-1055
6.12	<i>FVP_MPS2_SecurCore-SC000</i>	6-1070
6.13	<i>FVP_MPS2_SecurCore-SC300</i>	6-1085

Preface

This preface introduces the *Fast Models Fixed Virtual Platforms (FVP) Reference Guide*.

It contains the following:

- [About this book](#) on page 9.

About this book

Arm® Fixed Virtual Platform Reference. This manual introduces the Fixed Virtual Platforms, and describes how you can use them with other tools.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction

This chapter introduces the document.

Chapter 2 Getting Started with Fixed Virtual Platforms

This chapter describes how to use FVPs.

Chapter 3 Base Platform FVPs

This chapter lists the Base Platform FVPs and the components in them.

Chapter 4 BaseR platform FVPs

This chapter lists the BaseR Platform FVPs and the components in them.

Chapter 5 VE Platform FVPs

This chapter lists the VE Platform FVPs and the components in them.

Chapter 6 MPS2 Platform FVPs

This chapter lists the MPS2 Platform FVPs and the components in them.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the [Arm® Glossary](#) for more information.

Typographic conventions

italic

Introduces special terminology, denotes cross-references, and citations.

bold

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

monospace

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

monospace italic

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

monospace bold

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments.
For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

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- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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- The title *Fast Models Fixed Virtual Platforms (FVP) Reference Guide*.
- The number 100966_1190_00_en.
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- A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

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Other information

- [Arm® Developer](#).
- [Arm® Information Center](#).
- [Arm® Technical Support Knowledge Articles](#).
- [Technical Support](#).
- [Arm® Glossary](#).

Chapter 1

Introduction

This chapter introduces the document.

It contains the following sections:

- [*1.1 About FVPs* on page 1-12.](#)
- [*1.2 Data collection in FVPs* on page 1-13.](#)

1.1 About FVPs

Fixed Virtual Platforms (FVPs) enable software development without the need for real hardware.

FVPs are supplied as standalone executables for Linux and Windows. You cannot change the composition of FVPs, although you can configure some aspects of their behavior using parameters.

Arm provides different types of FVP, based on the following platforms:

- Armv8-A Base Platform.
- Armv8-R BaseR Platform.
- Arm Versatile™ Express development boards.
- Arm MPS2 or Arm MPS2+ platforms, for Cortex®-M series processors.

FVPs are available for all Cortex-A, Cortex-R, and Cortex-M processors, and they support the CADI, MTI, and Iris interfaces, so can be used for debugging and for trace output.

The Foundation Platform is a basic FVP for running on Linux hosts. It includes an Armv8-A AEM processor model, and is suitable for running bare-metal applications and for booting Linux.

Arm provides validated Linux and Android deliverables for the Armv8-A AEM Base Platform FVP and for the Foundation Platform. These are available on the Arm Community website at [Arm Development Platforms](#). To get started with Linux on Armv8-A FVPs, see [Armv8-A FVPs](#) also on Arm Community.

Related information

[*Base Platform*](#)

[*Microcontroller Prototyping System 2*](#)

[*Versatile Express Model*](#)

1.2 Data collection in FVPs

Arm periodically collects anonymous information about the usage of our products to understand and analyze what components or features you are using, with the goal of improving our products and your experience with them. Product usage analytics contain information such as system information, settings, and usage of specific features of the product. They do not include any personal information.

Host information includes:

- Operating system name, version, and locale.
- Number of CPUs.
- Amount of physical memory.
- Screen resolution.
- Processor and GPU type.

Feature tracking information includes:

Table 1-1 Fast Models analytics data points

Name	Description	Since
Platform name	<ul style="list-style-type: none"> • Tracked: Name of the platform model being run and the version and build number of Fast Models that was used to build the model. • Reported: Percentage of users using the different platforms. • Data type: Text. • Send policy: Every invocation. • Trigger points: On starting the simulation. 	v11.8
Session length	<ul style="list-style-type: none"> • Tracked: Length of time the platform was used. • Reported: Average time the different platforms are used. • Data type: Text. • Send policy: Every invocation. • Trigger points: On exiting the simulation. 	v11.9

Note

- Analytics gathering is enabled by default. Use the `--disable-analytics` command-line option to disable it for the current invocation, or set the `ARM_DISABLE_ANALYTICS` environment variable to a non-zero value to disable it for all invocations.
 - Querying the list of parameters with `--list-params` or the available options using `--help` does not trigger reporting.
-

Chapter 2

Getting Started with Fixed Virtual Platforms

This chapter describes how to use FVPs.

It contains the following sections:

- [2.1 Loading and running an application on an FVP on page 2-15](#).
- [2.2 Configuring the model on page 2-16](#).
- [2.3 FVP debug on page 2-17](#).
- [2.4 Using the CLCD window on page 2-18](#).
- [2.5 Ethernet with VE FVPs on page 2-21](#).
- [2.6 Using a terminal with a system model on page 2-23](#).
- [2.7 Virtio P9 device component on page 2-25](#).

2.1 Loading and running an application on an FVP

There are different ways to launch an FVP, for example from the command prompt, or from Model Debugger or Arm Development Studio.

To run an FVP from the command prompt, enter the model name followed by the model options. To see all available options, use the `--help` option. This is a list of some of the commonly used options for FVPs:

`-a [instance=]filename.axf`

Specifies an application to load, and optionally, the instance to load it on. The file can be in one of the following formats, or in a gzip-compressed version of it:

- ELF.
- Motorola S-Record.
- Intel-Hex.
- Verilog-Hex, in the format:

```
@<address_in_hex> <byte_in_hex>
```

If the FVP contains multiple CPU instances, you can specify the instance to load the image on. The instance name can include a wildcard (*), for example:

```
FVP_Base_AEMv8A-AEMv8A -a cluster0.cpu*=__image.axf
```

Omitting the instance name loads the application on all cores in the first cluster. If the FVP has multiple cores but no clusters, you must specify the instance name.

`--data filename.bin@address`

Loads binary data into memory at the address specified.

`-C instance.parameter=value`

Sets a single model parameter. Parameters are specified using a path that separates the instance names and the parameter using dots. For example, `-C bp.flashloader0.fname=fip.bin`.

Here, `bp` and `flashloader0` are instance names and `fname` is the parameter. To set multiple parameters using a configuration file, use the `-f` option instead. To list all the available parameters, with their type, default value, and description, invoke the model with the `--list-params`, or `-l` option.

`-f config_file.txt`

Specifies the name of a plain text configuration file. Configuration files simplify managing multiple model parameters. You can set the same parameters using this option as with the `-C` option.

`-S`

Starts a CADI debug server. This option allows a CADI-enabled debugger, such as Model Debugger or Arm Development Studio Debugger, to connect to the running model. The model waits for the debugger to connect before starting.

Related information

[Arm Development Studio User Guide](#)

[Model Debugger for Fast Models User Guide](#)

2.2 Configuring the model

When you start the model from the command line, you can configure it using either:

- One or more -C command-line arguments.
- A configuration file and the -f command-line argument.

Each -C command-line argument or line in the configuration file must contain:

- The name of the component instance.
- The parameter to modify.
- Its value.

Use the following format:

instance.parameter=value

The *instance* can be a hierarchical path, with each level separated by a dot “.” character.

————— Note —————

- Comment lines in the configuration file begin with a # character.
- You can set Boolean values using either **true** or **false**, or **1** or **0**.

You can generate a configuration file with all parameters set to default values by redirecting the output from the --list-params option into a new file, for example:

```
FVP_Base_AEMv8A.exe --list-params > params.txt
```

2.3 FVP debug

This section describes how to debug an FVP.

FVP debug options

To debug an FVP, you can either:

- Run the FVP from within a CADI-enabled debugger.
- Start the FVP with the `-S` command-line argument and then connect a CADI-enabled debugger to it.

For information about using your debugger in these ways, see your debugger documentation.

Semihosting support

Semihosting enables code running on a platform model to directly access the I/O facilities on a host computer. Examples of these facilities include console I/O and file I/O.

The simulator handles semihosting by intercepting `HLT 0xF000`, `SVC 0x123456`, or `SVC 0xAB`, depending on whether the processor is in A64, A32 or T32 state. It handles all other HTLs and SVCs as normal.

If the operating system does not use `HLT 0xF000`, `SVC 0x123456`, or `SVC 0xAB` for its own purposes, it is not necessary to disable semihosting support to boot an operating system.

To temporarily or permanently disable semihosting support for a current debug connection, see your debugger documentation.

Related information

[Semihosting for AArch32 and AArch64](#)

[Using semihosting to access resources on the host computer](#)

2.4 Using the CLCD window

When a Base Platform or VE FVP starts, the CLCD window opens, representing the contents of the simulated color LCD frame buffer. It automatically resizes to match the horizontal and vertical resolution that is set in the CLCD peripheral registers.

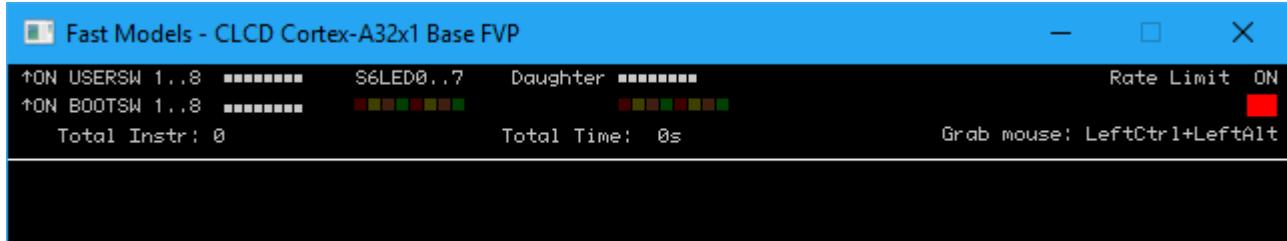


Figure 2-1 CLCD window in its default state at startup

The top section of the CLCD window displays the status information.

USERSW

Eight white boxes show the state of the User DIP switches.

These represent switch S6 on the VE hardware, USERSW[8:1], which is mapped to bits [7:0] of the SYS_SW register at address 0x1C010004.

The switches are in the off position by default. To change its state, click in the area above or below a white box.

BOOTSW

Eight white boxes show the state of the VE Boot DIP switches.

These represent switch S8 on the VE hardware, BOOTSEL[8:1], which is mapped to bits [15:8] of the SYS_SW register at address 0x1C010004.

The switches are in the off position by default.

————— Note —————

Changing Boot DIP switch positions while the model is running can result in unpredictable behavior.

S6LED

Eight colored boxes indicate the state of the VE User LEDs.

These represent the red/yellow/green LEDs on the VE hardware, which are mapped to bits [7:0] of the SYS_LED register at address 0x1C010008.

Daughter

Eight white boxes show the state of the daughterboard DIP switches and eight colored boxes show the state of the daughterboard LEDs.

Total Instr

A counter showing the total number of instructions executed.

Because the FVP models provide a *Programmer's View* (PV) of the system, the CLCD displays total instructions rather than total processor cycles. Timing might differ substantially from the hardware because:

- Bus fabric is simplified.
- Memory latencies are minimized.
- Cycle approximate processor and peripheral models are used.

In general, bus transaction timing is consistent with the hardware, but the timing of operations within the model is not accurate.

Total Time

A counter showing the total elapsed time, in seconds.

This time is wall clock time, not simulated time.

Rate Limit

A feature that disables or enables fast simulation.

Because the system model is highly optimized, your code might run faster than it would on real hardware. This effect might cause timing issues.

Rate Limit is enabled by default. Simulation time is restricted so that it more closely matches real time.

To disable or enable Rate Limit, click the square button. You can configure this option when instantiating the model with the `rate_limit-enable` visualization component parameter.

When you click the **Total Instr** item in the CLCD, the display toggles to show the following:

Instr/sec

The number of instructions that execute per second of wall clock time.

Perf Index

The ratio of real time to simulation time. The larger the ratio, the faster the simulation runs. If you enable the Rate Limit feature, the Perf Index approaches unity.

You can reset the simulation counters by resetting the model.

The FVP CLCD displays the core run state for each core on each cluster using a colored icon. The icons are to the left of the **Total Instr** (or **Inst/sec**) item.



Figure 2-2 Core run state icons for a dual-cluster, quad-core model

Table 2-1 Core run state icon descriptions

Icon	State label	Description
	UNKNOWN	Run status unknown, that is, simulation has not started.
	RUNNING	Core running, is not idle, and is executing instructions.
	HALTED	External halt signal asserted.
	STANDBY_WFE	Last instruction executed was WFE and standby mode has been entered.
	STANDBY_WFI	Last instruction executed was WFI and standby mode has been entered.
	IN_RESET	External reset signal asserted.
	DORMANT	Partial core power down.
	SHUTDOWN	Complete core power down.

If the CLCD window has focus:

- Any keyboard input is translated to PS/2 keyboard data.
- Any mouse activity over the window is translated into PS/2 relative mouse motion data. The data is then streamed to the KMI peripheral model FIFOs.

————— **Note** —————

The simulator only sends relative mouse motion events to the model. As a result, the host mouse pointer does not necessarily align with the target OS mouse pointer.

You can hide the host mouse pointer by pressing the **left Ctrl+left Alt** keys. Press the keys again to redisplay the host mouse pointer. Only the **left Ctrl** key is operational. The **right Ctrl** key does not have the same effect.

If you prefer to use a different key, configure it with the `trap_key` visualization component parameter.

Related information

[VEVisualisation component](#)

2.5 Ethernet with VE FVPs

This section describes how to use Ethernet with VE FVPs.

Using Ethernet with VE FVPs

The VE FVPs have a virtual Ethernet component. This component is a model of the SMSC 91C111 Ethernet controller, and uses a TAP device to communicate with the network. By default, the Ethernet component is disabled.

Host requirements

Before you can use the Ethernet capability of VE FVPs, set up your host computer.

Target requirements

This section describes the target requirements.

Target requirements - about

The VE FVPs include a software implementation of the SMSC 91C111 Ethernet controller. Your target OS must therefore include a driver for this specific device. To use the SMSC chip, configure the kernel. Linux supports the SMSC 91C111.

The configurable SMSC 91C111 component parameters are:

- `enabled`.
- `mac_address`.
- `promiscuous`.

enabled

When the device is disabled, the kernel cannot detect the device.

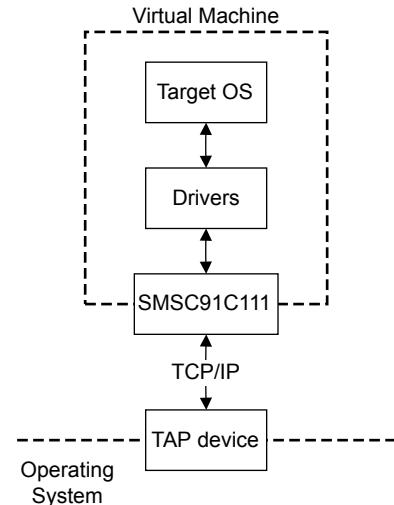


Figure 2-3 Model networking structure block diagram

To perform read and write operations on the TAP device, configure a HostBridge component. The HostBridge component is a virtual *Programmer's View* (PV) model. It acts as a networking gateway to exchange Ethernet packets with the TAP device on the host, and to forward packets to NIC models.

mac_address

There are two options for the `mac_address` parameter.

If a MAC address is not specified, when the simulator is run it takes the default MAC address, which is randomly generated. This random generation provides some degree of MAC address uniqueness when running models on multiple hosts on a local network.

promiscuous

The Ethernet component starts in promiscuous mode by default. In this mode, it receives all network traffic, even any not addressed to the device. Use this mode if you are using a single network device for multiple MAC addresses. Use this mode if, for example, you share the network card between your host OS and the VE FVP Ethernet component.

By default, the Ethernet device on the VE FVP has a randomly generated MAC address and starts in promiscuous mode.

2.6 Using a terminal with a system model

The Terminal component is a virtual component that enables UART data to be transferred between a TCP/IP socket on the host and a serial port on the target.

————— Note ————

To use the Terminal component with a Microsoft Windows 7 client, you must first install Telnet. The Telnet application is not installed on Microsoft Windows 7 by default.

Download the application by following the instructions on the Microsoft web site. Search for “Windows 7 Telnet” to find the Telnet FAQ page. To install Telnet:

1. Select **Start > Control Panel > Programs and Features** to open a window that enables you to uninstall or change programs.
2. Select **Turn Windows features on or off** on the left side of the bar. This opens the Microsoft Windows Features dialog. Select the **Telnet Client** check box.
3. Click **OK**. The installation of Telnet might take several minutes to complete.

The following figure shows a block diagram of one possible relationship between the target and host through the Terminal component. The TelnetTerminal block is what you configure when you define Terminal component parameters. The Virtual Machine is your FVP.

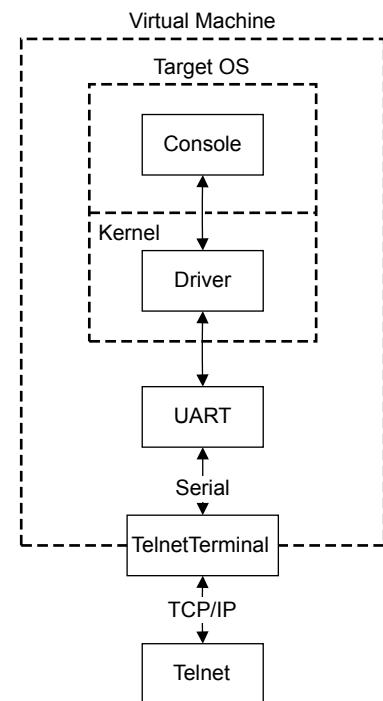


Figure 2-4 Terminal block diagram

On the target side, the console process that is invoked by your target OS relies on a suitable driver being present. Such drivers are normally part of the OS kernel. The driver passes serial data through a UART. The data is forwarded to the TelnetTerminal component, which exposes a TCP/IP port to the world outside of the FVP. This port can be connected to by, for example, a Telnet process on the host.

By default, the FVP starts four telnet Terminals when the model is initialized. You can change the startup behavior for each of the four Terminals by modifying the corresponding component parameters.

If the Terminal connection is broken, for example by closing a client telnet session, the port is re-opened on the host. This might have a different port number if the original one is no longer available. Before the first data access, you can connect a client of your choice to the network socket. If there is no existing

connection when the first data access is made, and the `start_telnet` parameter is `true`, a host telnet session is started automatically.

The port number of a particular Terminal instance can be defined when the FVP starts. The actual value of the port that is used by each Terminal is declared when it starts or restarts, and might not be the value that you specified if the port is already in use. If you are using Model Shell, the port numbers are displayed in the host window in which you started the model.

You can start the Terminal component in either telnet mode or raw mode.

Telnet mode

In telnet mode, the Terminal component supports a subset of the RFC 854 protocol. This means that the Terminal participates in negotiations between the host and client concerning what is and is not supported, but flow control is not implemented.

Raw mode

Raw mode enables the byte stream to pass unmodified between the host and the target. This means that the Terminal component does not participate in initial capability negotiations between the host and client. It acts as a TCP/IP port. You can use this feature to directly connect to your target through the Terminal component.

2.7 Virtio P9 device component

The VirtioP9Device component is included in Base, BaseR, and A-profile VE platforms. It implements a subset of the Plan 9 file protocol over a virtio transport. It enables accessing a directory on the host's filesystem within Linux, or another operating system that implements the protocol, running on a platform model.

Setting up VirtioP9Device

Take the following steps to use this component:

- Use a version of Linux that supports v9fs over virtio and virtio-mmio devices.
- Update the device tree to include the VirtioP9Device component, or specify it on the kernel command-line, as shown below. The address range for both VE and Base platforms is `0x1C140000-0x1C14FFFF`.

The interrupt number is 43, or IRQ 75, for both VE and Base platforms.

- Set the following parameter to the directory on the host that you want to mount in the model:

VE:

```
motherboard.virtiop9device.root_path
```

Base:

```
bp.virtiop9device.root_path
```

- On Linux, mount the host directory by using the following command in the model:

```
$ mount -t 9p -o trans=virtio,version=9p2000.L FM <mount point>
```

Example kernel command-line argument

```
virtio_mmio.device=0x10000@0x1c140000:75
```

Example entry for DTS files

Add this entry next to the corresponding `virtio_block` entry:

```
virtio_p9@0140000 {  
    compatible = "virtio,mmio";  
    reg = <0x0 0x1c140000 0x0 0x1000>;  
    interrupts = <0x0 0x2b 0x4>;  
};
```

Chapter 3

Base Platform FVPs

This chapter lists the Base Platform FVPs and the components in them.

It contains the following sections:

- [3.1 FVP_Base_AEMv8A on page 3-28](#).
- [3.2 FVP_Base_AEMv8A-AEMv8A on page 3-37](#).
- [3.3 FVP_Base_Cortex-A32x1 on page 3-48](#).
- [3.4 FVP_Base_Cortex-A32x2 on page 3-56](#).
- [3.5 FVP_Base_Cortex-A32x4 on page 3-65](#).
- [3.6 FVP_Base_Cortex-A35x1 on page 3-74](#).
- [3.7 FVP_Base_Cortex-A35x2 on page 3-82](#).
- [3.8 FVP_Base_Cortex-A35x4 on page 3-91](#).
- [3.9 FVP_Base_Cortex-A53x1 on page 3-100](#).
- [3.10 FVP_Base_Cortex-A53x2 on page 3-108](#).
- [3.11 FVP_Base_Cortex-A53x4 on page 3-116](#).
- [3.12 FVP_Base_Cortex-A55 on page 3-125](#).
- [3.13 FVP_Base_Cortex-A55+Cortex-A76 on page 3-135](#).
- [3.14 FVP_Base_Cortex-A55x1 on page 3-144](#).
- [3.15 FVP_Base_Cortex-A55x1+Cortex-A75x1 on page 3-152](#).
- [3.16 FVP_Base_Cortex-A55x2 on page 3-161](#).
- [3.17 FVP_Base_Cortex-A55x2+Cortex-A75x2 on page 3-170](#).
- [3.18 FVP_Base_Cortex-A55x4 on page 3-179](#).
- [3.19 FVP_Base_Cortex-A55x4+Cortex-A75x1 on page 3-188](#).
- [3.20 FVP_Base_Cortex-A55x4+Cortex-A75x2 on page 3-197](#).
- [3.21 FVP_Base_Cortex-A55x4+Cortex-A75x4 on page 3-206](#).
- [3.22 FVP_Base_Cortex-A55x4+Cortex-A76x2 on page 3-215](#).
- [3.23 FVP_Base_Cortex-A57x1 on page 3-224](#).

- [3.24 FVP_Base_Cortex-A57x1-A35x1](#) on page 3-232.
- [3.25 FVP_Base_Cortex-A57x1-A53x1](#) on page 3-241.
- [3.26 FVP_Base_Cortex-A57x2](#) on page 3-251.
- [3.27 FVP_Base_Cortex-A57x2-A35x4](#) on page 3-260.
- [3.28 FVP_Base_Cortex-A57x2-A53x4](#) on page 3-270.
- [3.29 FVP_Base_Cortex-A57x4](#) on page 3-280.
- [3.30 FVP_Base_Cortex-A57x4-A35x4](#) on page 3-289.
- [3.31 FVP_Base_Cortex-A57x4-A53x4](#) on page 3-300.
- [3.32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2](#) on page 3-311.
- [3.33 FVP_Base_Cortex-A65AEx4](#) on page 3-320.
- [3.34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4](#) on page 3-330.
- [3.35 FVP_Base_Cortex-A65AEx8](#) on page 3-340.
- [3.36 FVP_Base_Cortex-A65x1](#) on page 3-351.
- [3.37 FVP_Base_Cortex-A65x2](#) on page 3-359.
- [3.38 FVP_Base_Cortex-A65x4](#) on page 3-368.
- [3.39 FVP_Base_Cortex-A72x1](#) on page 3-378.
- [3.40 FVP_Base_Cortex-A72x1-A53x1](#) on page 3-386.
- [3.41 FVP_Base_Cortex-A72x2](#) on page 3-395.
- [3.42 FVP_Base_Cortex-A72x2-A53x4](#) on page 3-404.
- [3.43 FVP_Base_Cortex-A72x4](#) on page 3-415.
- [3.44 FVP_Base_Cortex-A72x4-A53x4](#) on page 3-424.
- [3.45 FVP_Base_Cortex-A73x1](#) on page 3-435.
- [3.46 FVP_Base_Cortex-A73x1-A53x1](#) on page 3-443.
- [3.47 FVP_Base_Cortex-A73x2](#) on page 3-452.
- [3.48 FVP_Base_Cortex-A73x2-A53x4](#) on page 3-460.
- [3.49 FVP_Base_Cortex-A73x4](#) on page 3-471.
- [3.50 FVP_Base_Cortex-A75x1](#) on page 3-480.
- [3.51 FVP_Base_Cortex-A75x2](#) on page 3-488.
- [3.52 FVP_Base_Cortex-A75x4](#) on page 3-497.
- [3.53 FVP_Base_Cortex-A76](#) on page 3-506.
- [3.54 FVP_Base_Cortex-A76AEx2](#) on page 3-515.
- [3.55 FVP_Base_Cortex-A76AEx4](#) on page 3-525.
- [3.56 FVP_Base_Cortex-A76x1](#) on page 3-535.
- [3.57 FVP_Base_Cortex-A76x2](#) on page 3-543.
- [3.58 FVP_Base_Cortex-A76x4](#) on page 3-552.
- [3.59 FVP_Base_Cortex-A77x1](#) on page 3-561.
- [3.60 FVP_Base_Cortex-A77x2](#) on page 3-569.
- [3.61 FVP_Base_Cortex-A77x4](#) on page 3-577.
- [3.62 FVP_Base_Neoverse-EI1x1](#) on page 3-586.
- [3.63 FVP_Base_Neoverse-EI1x2](#) on page 3-594.
- [3.64 FVP_Base_Neoverse-EI1x4](#) on page 3-603.
- [3.65 FVP_Base_Neoverse-N1x1](#) on page 3-612.
- [3.66 FVP_Base_Neoverse-N1x2](#) on page 3-620.
- [3.67 FVP_Base_Neoverse-N1x4](#) on page 3-629.
- [3.68 FVP_Base_RevC-2xAEMv8A](#) on page 3-638.

3.1 FVP_Base_AEMv8A

FVP_Base_AEMv8A contains the following instances:

Table 3-1 FVP_Base_AEMv8A instances

Name	Type	Description
FVP_Base_AEMv8A.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_AEMv8A.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_AEMv8A.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_AEMv8A.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_AEMv8A.bp.hdlcd0.timer.time4	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_AEMv8A.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.cluster0	Cluster_ARMAEMv8-A_MP	ARMAEMv8-A Cluster CT model.
FVP_Base_AEMv8A.cci400	<i>CCl400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_AEMv8A.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_AEMv8A.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_AEMv8A.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_AEMv8A.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_AEMv8A.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_AEMv8A.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_AEMv8A.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_AEMv8A.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_AEMv8A.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_AEMv8A.bp.sp810_sysctrl.clk_div_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_AEMv8A.cluster0.cpu0	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A.cluster0.cpu1	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A.cluster0.cpu2	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A.cluster0.cpu3	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_AEMv8A.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_AEMv8A.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_AEMv8A.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_AEMv8A.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_AEMv8A.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.Timer_2_3.clk_dv0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.Timer_2_3.clk_di_v1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_AEMv8A.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_AEMv8A.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A.bp.Timer_0_1.clk_di_v0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.virtio_net_labelle_r	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.hlcd0.timer.time_r.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_AEMv8A.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_AEMv8A.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_AEMv8A.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_AEMv8A.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_AEMv8A.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_AEMv8A.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_AEMv8A.bp.pl111_clcd.pl11x	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_AEMv8A.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A	FVP_Base_AEMv8A	Base Platform Compute Subsystem for ARMAEMv8AMPCT.
FVP_Base_AEMv8A.bp.Timer_0_1.count	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_AEMv8A.bp.virtiop9device_labeler	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_AEMv8A.bp.pl111_clcd_labeler	<i>Labeller</i>	-
FVP_Base_AEMv8A.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_AEMv8A.bp.pl111_clcd.pl11x	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A.bp.pl111_clcd.pl11x	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_AEMv8A.bp.pl111_clcd.pl11x	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_AEMv8A.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.Timer_2_3.count	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A.bp.Timer_2_3.count	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_AEMv8A.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_AEMv8A.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_AEMv8A.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp终端_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 3-1 FVP_Base_AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A.bp.Timer_0_1.clk_di_v1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A.bp.hdlcd0.timer.time.r.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_AEMv8A.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.

3.2 FVP_Base_AEMv8A-AEMv8A

FVP_Base_AEMv8A-AEMv8A contains the following instances:

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.ap_ref_clk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_AEMv8A_AEMv8A.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A_AEMv8A.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A_AEMv8A.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A_AEMv8A.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_AEMv8A_AEMv8A.cluster1_labeller	<i>Labeler</i>	-
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cldc_labeller	<i>Labeler</i>	-
FVP_Base_AEMv8A_AEMv8A.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_AEMv8A_AEMv8A.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A_AEMv8A.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A_AEMv8A.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_AEMv8A_AEMv8A.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_AEMv8A_AEMv8A.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_AEMv8A_AEMv8A.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_AEMv8A_AEMv8A.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_AEMv8A_AEMv8A.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.clock1_00Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.secure_SRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cled.pl11x_cled.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_AEMv8A_AEMv8A.bp.clock5_0Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cled.pl11x_cled.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_AEMv8A_AEMv8A.cluster0	Cluster_ARMAEMv8-A_MP	ARMAEMv8-A Cluster CT model.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.clock3_2KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_AEMv8A_AEMv8A.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_AEMv8A_AEMv8A.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_AEMv8A_AEMv8A.bp.secure_flashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu0	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_AEMv8A_AEMv8A.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A_AEMv8A.cluster0_1_abeller	<i>Labeller</i>	-
FVP_Base_AEMv8A_AEMv8A.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.pl041_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_AEMv8A_AEMv8A.bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu2	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.bp.secure_flash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A_AEMv8A	FVP_Base_AEMv8A_AEMv8A	Base Platform Compute Subsystem for ARMAEMv8AMPCT and ARMAEMv8AMPCT.
FVP_Base_AEMv8A_AEMv8A.bp.clockLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cled.pl11x_cled	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_AEMv8A_AEMv8A.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_AEMv8A_AEMv8A.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_AEMv8A_AEMv8A.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.secure_DRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.hdlcd0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.nonretardedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_AEMv8A_AEMv8A.bp.audiooutput	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu2.l1dcache	PVCache	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cled.pl11x_cled.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_AEMv8A_AEMv8A.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_AEMv8A_AEMv8A.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_AEMv8A_AEMv8A.bp.virtiop9device_labeller	Labeller	-
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_AEMv8A_AEMv8A.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_AEMv8A_AEMv8A.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.virtio_blockdevice_labeller	Labeller	-
FVP_Base_AEMv8A_AEMv8A.cluster1	Cluster_ARMAEMv8-A_MP	ARMAEMv8-A Cluster CT model.
FVP_Base_AEMv8A_AEMv8A.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_AEMv8A_AEMv8A.bp.pl111_cld	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_AEMv8A_AEMv8A.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_AEMv8A_AEMv8A.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A_AEMv8A.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_AEMv8A_AEMv8A.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.ps2mo use	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_AEMv8A_AEMv8A.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_AEMv8A_AEMv8A.bp.virtiob lockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_AEMv8A_AEMv8A.cluster0.c pu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.bp.termin al_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A_AEMv8A.bp.termin al_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A_AEMv8A.bp.termin al_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A_AEMv8A.bp.termin al_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_AEMv8A_AEMv8A.bp.trusted _watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_AEMv8A_AEMv8A.bp.clock2 4MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.cluster0.c pu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_AEMv8A_AEMv8A.cluster0.1 2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.sp810 _sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_AEMv8A_AEMv8A.bp.hlcd0 .timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.clock3_5MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu1	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu3	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.cluster1.cpu2	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.bp.vis.rec_order.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu3	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu0	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu1	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_AEMv8A_AEMv8A.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_AEMv8A_AEMv8A.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_AEMv8A_AEMv8A.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_AEMv8A_AEMv8A.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_AEMv8A_AEMv8A.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.

Table 3-2 FVP_Base_AEMv8A-AEMv8A instances (continued)

Name	Type	Description
FVP_Base_AEMv8A_AEMv8A.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_AEMv8A_AEMv8A.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_AEMv8A_AEMv8A.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.3 FVP_Base_Cortex-A32x1

FVP_Base_Cortex-A32x1 contains the following instances:

Table 3-3 FVP_Base_Cortex-A32x1 instances

Name	Type	Description
FVP_Base_Cortex_A32x1.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.Timer_2_3.c lk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.trusted_watc hdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x1.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A32x1.cluster0.cpu0.dt lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x1.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x1.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.cci400	CC1400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A32x1.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A32x1.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A32x1.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A32x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A32x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A32x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A32x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A32x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A32x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1	FVP_Base_Cortex_A32x1	Base Platform Compute Subsystem for ARM Cortex A32x1 CT.
FVP_Base_Cortex_A32x1.bp.virtioblockd.device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A32x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A32x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x1.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A32x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A32x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x1.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A32x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x1.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A32x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.bp.virtioblockd device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A32x1.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A32x1.bp.hlcd0.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A32x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A32x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x1.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A32x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x1.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A32x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A32x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A32x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A32x1.cluster0.cpu0	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A32x1.bp.sp810_sysctr1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A32x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A32x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A32x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A32x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A32x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A32x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x1.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x1.bp.pl111_clcd_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-3 FVP_Base_Cortex-A32x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A32x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A32x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A32x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A32x1.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A32x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A32x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x1.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x1.cluster0	Cluster_ARM_Cortex-A32	ARM Cortex-A32 Cluster CT model.
FVP_Base_Cortex_A32x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A32x1.bp.virtio_net_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A32x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.

3.4 FVP_Base_Cortex-A32x2

FVP_Base_Cortex-A32x2 contains the following instances:

Table 3-4 FVP_Base_Cortex-A32x2 instances

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A32x2.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A32x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A32x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A32x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A32x2.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A32x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A32x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A32x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A32x2.bp.hd lcd0	<i>PL370_HDLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A32x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A32x2.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A32x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A32x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x2.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x2.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A32x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A32x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A32x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x2	FVP_Base_Cortex_A32x2	Base Platform Compute Subsystem for ARM Cortex A32x2CT.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.virtioblockd evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A32x2.bp.pl111_clcd.p l11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A32x2.bp.pl011_uart0. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.trusted_watc hdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x2.cluster0.cpu1.dt lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.Timer_2_3.c lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.Timer_2_3.c lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A32x2.bp.pl011_uart2. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A32x2.bp	BasePlatformPeriph erals	Peripherals and address map for the Base Platform.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A32x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A32x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A32x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A32x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A32x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A32x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A32x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A32x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A32x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A32x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A32x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A32x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A32x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x2.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x2.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A32x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A32x2.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A32x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x2.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A32x2.bp.virtio_net_labeler	Labeler	-
FVP_Base_Cortex_A32x2.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A32x2.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.cluster0	Cluster_ARM_Cortex-A32	ARM Cortex-A32 Cluster CT model.
FVP_Base_Cortex_A32x2.bp.pl111_clcd.p111x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A32x2.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A32x2.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A32x2.cluster0.cpu0	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x2.cluster0.cpu1	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x2.bp.generic_wat_chdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A32x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x2.cluster0.cpu0.11.dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x2.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x2.cluster0.cpu1.11.dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-4 FVP_Base_Cortex-A32x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x2.cluster0.cpu1.11.icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.5 FVP_Base_Cortex-A32x4

FVP_Base_Cortex-A32x4 contains the following instances:

Table 3-5 FVP_Base_Cortex-A32x4 instances

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A32x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A32x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A32x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A32x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A32x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A32x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A32x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A32x4.cluster0.cpu3.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x4.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A32x4.bp.pl111_clcd.p111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x4.bp.sp810_sysctrl1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A32x4.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A32x4.bp.smse_91c11_1	SMSC_91C11	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A32x4.bp.pl111_clcd.p111x_clcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x4.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A32x4.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x4.cluster0.cpu1.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A32x4.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x4.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x4.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.cluster0.cpu2	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x4.cluster0.cpu2.11_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A32x4.cluster0.cpu3	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cluster0.cpu0.11_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A32x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A32x4.cluster0.cpu2.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A32x4.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x4.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x4.bp.virtioblockd.device_labeller	Labeller	-

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.virtioblockd device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A32x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A32x4	FVP_Base_Cortex_A32x4	Base Platform Compute Subsystem for ARM Cortex A32x4 CT.
FVP_Base_Cortex_A32x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A32x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A32x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A32x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.cluster0.cpu3.ll1_deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A32x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A32x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A32x4.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A32x4.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A32x4.cluster0	Cluster_ARM_Cortex-A32	ARM Cortex-A32 Cluster CT model.
FVP_Base_Cortex_A32x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x4.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A32x4.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A32x4.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A32x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.hlcd0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A32x4.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x4.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A32x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A32x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A32x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.cluster0.cpu1.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A32x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A32x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A32x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A32x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A32x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A32x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A32x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A32x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A32x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A32x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A32x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A32x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cluster0.cpu0	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x4.cluster0.cpu1	ARM_Cortex-A32	ARM Cortex-A32 CT model.
FVP_Base_Cortex_A32x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A32x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A32x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A32x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A32x4.bp.hdled0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A32x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A32x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A32x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-5 FVP_Base_Cortex-A32x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A32x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A32x4.bp.Timer_2_3.c lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A32x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

3.6 FVP_Base_Cortex-A35x1

FVP_Base_Cortex-A35x1 contains the following instances:

Table 3-6 FVP_Base_Cortex-A35x1 instances

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A35x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A35x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A35x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A35x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A35x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A35x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A35x1.bp.hdlcd0_labeler	<i>Labeller</i>	-

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x1.bp.mmmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A35x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A35x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x1	FVP_Base_Cortex_A35x1	Base Platform Compute Subsystem for ARM Cortex A35x1 CT.
FVP_Base_Cortex_A35x1.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x1.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A35x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A35x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A35x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.virtioblockd evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x1.bp.virtio_net_la beller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A35x1.bp.pl111_clcd.p l11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A35x1.bp.virtiop9devi ce	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A35x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A35x1.bp	BasePlatformPeriph erals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A35x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x1.cluster0.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A35x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A35x1.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A35x1.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x1.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x1.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x1.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x1.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x1.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x1.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x1.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A35x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A35x1.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A35x1.bp.pl111_clcd_1_abeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A35x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x1.cluster0	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.
FVP_Base_Cortex_A35x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A35x1.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A35x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A35x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A35x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A35x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.secureSRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A35x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A35x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x1.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A35x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x1.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A35x1.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A35x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-6 FVP_Base_Cortex-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x1.bp.sp810_sysctr.l.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.sp810_sysctr.l.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.sp810_sysctr.l.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.sp810_sysctr.l.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.7 FVP_Base_Cortex-A35x2

FVP_Base_Cortex-A35x2 contains the following instances:

Table 3-7 FVP_Base_Cortex-A35x2 instances

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A35x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.dummy_loca1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A35x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A35x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A35x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x2.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A35x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.hdled0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x2.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A35x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A35x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A35x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x2	FVP_Base_Cortex_A35x2	Base Platform Compute Subsystem for ARM Cortex A35x2 CT.
FVP_Base_Cortex_A35x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A35x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041 AACI.
FVP_Base_Cortex_A35x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A35x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A35x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A35x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.cluster0.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.virtioblockddevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A35x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A35x2.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x2.bp.hdled0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.hdled0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A35x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A35x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A35x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A35x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A35x2.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A35x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A35x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A35x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A35x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.cluster0.cpu1	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x2.cluster0.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.ve_sysregs	VE_SysRegs	-

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.hdled0.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x2.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A35x2.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A35x2.bp.sp810_sysctr1.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.sp810_sysctr1.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.sp810_sysctr1.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.sp810_sysctr1.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x2.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x2.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x2.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x2.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x2.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A35x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.Timer_2_3.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x2.bp.pl111_clcd.p_l11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A35x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x2.bp.smsc_91c11_1	<i>SMSC_91C11I</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A35x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.cluster0	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.
FVP_Base_Cortex_A35x2.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x2.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A35x2.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A35x2.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x2.bp.pl111_clcd_1_abeller	Labeler	-
FVP_Base_Cortex_A35x2.cluster0.cpu1.11dcache	PVCache	PV Cache.
FVP_Base_Cortex_A35x2.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A35x2.cci400	CC1400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A35x2.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A35x2.bp.hdlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A35x2.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A35x2.bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A35x2.bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A35x2.bp.terminal_0	TelnetTerminal	Telnet terminal interface.

Table 3-7 FVP_Base_Cortex-A35x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x2.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

3.8 FVP_Base_Cortex-A35x4

FVP_Base_Cortex-A35x4 contains the following instances:

Table 3-8 FVP_Base_Cortex-A35x4 instances

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A35x4.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A35x4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.exclusive_monitor	PVBUSExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A35x4.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.cluster0.cpu1.tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.cluster0.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A35x4.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.cluster0	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.
FVP_Base_Cortex_A35x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A35x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x4.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A35x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x4.cluster0.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A35x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A35x4.cluster0.cpu3.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A35x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A35x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A35x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4	FVP_Base_Cortex_A35x4	Base Platform Compute Subsystem for ARM Cortex A35x4 CT.
FVP_Base_Cortex_A35x4.bp.virtioblockd.device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x4.cluster0.cpu0.l1_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A35x4.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A35x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A35x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x4.cluster0.cpu1.icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A35x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A35x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A35x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A35x4.elfloader	<i>ElfLoader</i>	ELF loader component.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.cluster0.cpu3	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A35x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A35x4.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A35x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A35x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A35x4.cluster0.cpu3.ll1_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A35x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A35x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A35x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A35x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A35x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A35x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A35x4.bp.pl111_clcd_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A35x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.virtiop9devi_ce_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A35x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A35x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A35x4.bp.hdlcd0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A35x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A35x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A35x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A35x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A35x4.cluster0.cpu2	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A35x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A35x4.cluster0.cpu1	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A35x4.cluster0.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A35x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A35x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A35x4.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A35x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A35x4.bp.hdled0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A35x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A35x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-8 FVP_Base_Cortex-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A35x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A35x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A35x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A35x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

3.9 FVP_Base_Cortex-A53x1

FVP_Base_Cortex-A53x1 contains the following instances:

Table 3-9 FVP_Base_Cortex-A53x1 instances

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A53x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A53x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x1.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A53x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.virtioblockdevice_labeler	<i>Labeler</i>	-

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A53x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A53x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A53x1.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A53x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A53x1.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A53x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A53x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A53x1.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x1.cluster0	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A53x1.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A53x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A53x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A53x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A53x1.bp.hlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x1.bp.pl111_clcd.pl111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A53x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A53x1.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A53x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A53x1.bp.pl111_clcd_1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A53x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A53x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A53x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A53x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x1	FVP_Base_Cortex_A53x1	Base Platform Compute Subsystem for ARM Cortex A53x1 CT.
FVP_Base_Cortex_A53x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x1.cluster0.cpu0.llcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A53x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A53x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A53x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x1.bp.vis.recorder.recordingDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A53x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A53x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x1.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A53x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.cluster0.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x1.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A53x1.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A53x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.pl041_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A53x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.hlcd0.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x1.bp.sp810_sysctr1.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.sp810_sysctr1.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.sp810_sysctr1.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.sp810_sysctr1.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Cortex_A53x1.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A53x1.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.

Table 3-9 FVP_Base_Cortex-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A53x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A53x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.10 FVP_Base_Cortex-A53x2

FVP_Base_Cortex-A53x2 contains the following instances:

Table 3-10 FVP_Base_Cortex-A53x2 instances

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A53x2.cluster0.cpu0.11.deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A53x2.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A53x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A53x2.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A53x2.bp.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A53x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A53x2.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A53x2.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A53x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A53x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A53x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A53x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A53x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A53x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x2.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A53x2.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x2.bp.sp810_sysctr1.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.sp810_sysctr1.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x2.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A53x2.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.hlcd0_labeler	Labeler	-
FVP_Base_Cortex_A53x2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x2.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A53x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A53x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A53x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x2.cluster0	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A53x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A53x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2	FVP_Base_Cortex_A53x2	Base Platform Compute Subsystem for ARM Cortex A53x2 CT.
FVP_Base_Cortex_A53x2_bp.virtioblockd ^d evice_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A53x2_bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2_bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A53x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x2_bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2_bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x2_bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x2_bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2_bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x2_bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x2_bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x2.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A53x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A53x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A53x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x2.bp.pl111_clcd_labeler	<i>Labeler</i>	-

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x2.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A53x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x2.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A53x2.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A53x2.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A53x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A53x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 3-10 FVP_Base_Cortex-A53x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A53x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A53x2.bp.Timer_2_3.countr1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x2.bp.Timer_2_3.countr0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x2.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A53x2.cluster0.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x2.cluster0.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A53x2.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x2.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

3.11 FVP_Base_Cortex-A53x4

FVP_Base_Cortex-A53x4 contains the following instances:

Table 3-11 FVP_Base_Cortex-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A53x4.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x4.cluster0.cpu3.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A53x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A53x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A53x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A53x4.cluster0.cpu3.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A53x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.hdlcd0.timer.thread	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A53x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A53x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A53x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A53x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.cluster0	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A53x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A53x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A53x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A53x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A53x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A53x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.smsc_91c11_1	<i>SMSC_91C11I</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A53x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A53x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x4.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A53x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A53x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A53x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.cluster0.cpu2.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.cluster0_labelle_r	<i>Labeler</i>	-
FVP_Base_Cortex_A53x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4	FVP_Base_Cortex_A53x4	Base Platform Compute Subsystem for ARM Cortex A53x4 CT.

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.cluster0.cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x4.cluster0.cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A53x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A53x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A53x4.cluster0.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A53x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A53x4.cluster0.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A53x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A53x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A53x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.bp.virtioblockdevice_labeler	<i>Labeler</i>	-

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A53x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A53x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A53x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A53x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A53x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A53x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A53x4.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A53x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A53x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A53x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A53x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A53x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A53x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A53x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-11 FVP_Base_Cortex-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A53x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A53x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A53x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A53x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.12 FVP_Base_Cortex-A55

FVP_Base_Cortex-A55 contains the following instances:

Table 3-12 FVP_Base_Cortex-A55 instances

Name	Type	Description
FVP_Base_Cortex_A55.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55.bp.hdlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55.cluster0.cpu7.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu3.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55	FVP_Base_Cortex_A55	Base Platform Compute Subsystem for ARM Cortex A55 CT.
FVP_Base_Cortex_A55.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55.cluster0.cpu6.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.cluster0.cpu5.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.cluster0.cpu6.11icache	<i>PVCache</i>	PV Cache.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55.cluster0.cpu4.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55.cluster0.cpu6.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.virtioblockdevice_labeller	<i>Labeller</i>	-

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.cluster0.cpu4.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55.bp.pl111_cld	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55.cluster0.cpu6.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55.cluster0.cpu7.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.cluster0.cpu7.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55.cluster0.cpu4.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.cluster0.cpu4.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55.cluster0.cpu0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.cluster0.cpu7	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu6	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu5	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu4	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.bp.vis.recorder.palybackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55.cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55.cluster0.cpu5.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A55.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55.bp.pl111_clcd_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu5.ll1cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu7.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55.bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55.cluster0.cpu2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.cluster0.cpu3.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.cluster0.cpu6.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.p1111_cled.p11x_cled.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.cluster0	Cluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55.cluster0.cpu4.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu5.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.p1180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.cluster0.cpu5.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55.bp.sp810_sysctrl.lkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.sp810_sysctrl.lkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.sp810_sysctrl.lkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.sp810_sysctrl.lkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.cluster0.cpu7.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55.bp.pl111_cled.pl11_1x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55.cluster0_labeller	<i>Labeller</i>	-

Table 3-12 FVP_Base_Cortex-A55 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55.bp.pl111_clcd.p11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55.cluster0.cpu2.ll1cache	<i>PVCache</i>	PV Cache.

3.13 FVP_Base_Cortex-A55+Cortex-A76

FVP_Base_Cortex-A55+Cortex-A76 contains the following instances:

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55_Cortex_A76.cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55_Cortex_A76.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55_Cortex_A76.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55_Cortex_A76.cluster0.subcluster1	Subcluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A55_Cortex_A76.bn.ontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55_Cortex_A76.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55_Cortex_A76.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.vi s.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.cl ock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl 111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55_Cortex_A76.clust er0	Cluster_ARM_Corte x-A55_Cortex-A76	ARM Cortex-A55_Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A55_Cortex_A76.bp.se cureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55_Cortex_A76.bp.h dlcd0.timer.thread_event	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl 111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55_Cortex_A76.bp.Ti mer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.Ti mer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.se cureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.s msc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55_Cortex_A76.bp.vi.s.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55_Cortex_A76.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55_Cortex_A76.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55_Cortex_A76.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55_Cortex_A76.bp.telnetterminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55_Cortex_A76.bp.telnetterminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55_Cortex_A76.bp.telnetterminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55_Cortex_A76.bp.telnetterminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55_Cortex_A76.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55_Cortex_A76.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55_Cortex_A76.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.rfcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55_Cortex_A76.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55_Cortex_A76.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55_Cortex_A76.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.PL031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55_Cortex_A76.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55_Cortex_A76.bp.PL011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55_Cortex_A76.bp.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A55_Cortex_A76.bp.PL111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55_Cortex_A76.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55_Cortex_A76.bp.PL111_clcd_labeller	<i>Labeller</i>	-

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55_Cortex_A76.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55_Cortex_A76.bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55_Cortex_A76.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55_Cortex_A76.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55_Cortex_A76.bp.virtioblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55_Cortex_A76.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55_Cortex_A76.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55_Cortex_A76.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A55_Cortex_A76.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55_Cortex_A76.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A55_Cortex_A76.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55_Cortex_A76.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55_Cortex_A76.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55_Cortex_A76.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55_Cortex_A76.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55_Cortex_A76.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55_Cortex_A76.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A55_Cortex_A76.bp.hostbridge	HostBridge	Host Socket Interface Component.

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.h dlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55_Cortex_A76.bp.v e_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55_Cortex_A76.bp.vi rtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55_Cortex_A76.bp.Ti mer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55_Cortex_A76.bp.tr usted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55_Cortex_A76.bp.cl ock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.d ummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.a p_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55_Cortex_A76	FVP_Base_Cortex_A55_Cortex_A76	Base Platform Compute Subsystem for ARM Cortex A55CT_Cortex A76CT.
FVP_Base_Cortex_A55_Cortex_A76.bp.cl ock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.Ti mer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.h_dlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55_Cortex_A76.bp.h_dlcd0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55_Cortex_A76.bp.vi.s.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread</i> <i>4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-13 FVP_Base_Cortex-A55+Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55_Cortex_A76.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55_Cortex_A76.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55_Cortex_A76.bp.psriram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55_Cortex_A76.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55_Cortex_A76.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55_Cortex_A76.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55_Cortex_A76.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55_Cortex_A76.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55_Cortex_A76.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55_Cortex_A76.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

3.14 FVP_Base_Cortex-A55x1

FVP_Base_Cortex-A55x1 contains the following instances:

Table 3-14 FVP_Base_Cortex-A55x1 instances

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x1.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x1.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x1.cluster0.cpu0.l1_decache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1.cluster0.cpu0.l1_icache	<i>PVCache</i>	PV Cache.

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A55x1.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x1.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x1.cluster0_labeller	Labeller	-
FVP_Base_Cortex_A55x1.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x1.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x1.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x1.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x1.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.smsc_91c11_1	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1.cluster0	Cluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.hlcd0.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x1.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x1.bp.secureRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x1.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x1.bp.virtioblockddevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.hdlcd0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.hdlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x1.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1	FVP_Base_Cortex_A55x1	Base Platform Compute Subsystem for ARM Cortex A55x1 CT.
FVP_Base_Cortex_A55x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-14 FVP_Base_Cortex-A55x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x1.bp.Timer_2_3.c_ounter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x1.bp.Timer_2_3.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.15 FVP_Base_Cortex-A55x1+Cortex-A75x1

FVP_Base_Cortex-A55x1+Cortex-A75x1 contains the following instances:

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.smsc_91c11	SMSC_91C11	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vram	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x1_Cortex_A75x1. cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x1_Cortex_A75x1. clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl111_clcd_labeller	<i>Labeller</i>	-

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.virtio_net_labeller	Labeller	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hdlcd0_labeller	Labeller	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x1_Cortex_A75x1. cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. cluster0.cpu1	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.virtiop9device_labeller	Labeller	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1_Cortex_A75x1. dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hdlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x1_Cortex_A75x1_cluster0	Cluster_ARM_Cortex-A55_Cortex-A75	ARM Cortex-A55_Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1_Cortex_A75x1_bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1_Cortex_A75x1. cc1400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sram	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x1_Cortex_A75x1	FVP_Base_Cortex_A55x1_Cortex_A75 x1	Base Platform Compute Subsystem for ARM Cortex A55x1 CT Cortex A75x1 CT.
FVP_Base_Cortex_A55x1_Cortex_A75x1. gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.

Table 3-15 FVP_Base_Cortex-A55x1+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. cluster0.subcluster1	Subcluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x1_Cortex_A75x1. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

3.16 FVP_Base_Cortex-A55x2

FVP_Base_Cortex-A55x2 contains the following instances:

Table 3-16 FVP_Base_Cortex-A55x2 instances

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.nontrustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2.bp.dummy_loc1_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x2.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x2.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55x2.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.Timer_2_3.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x2.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x2.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x2.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x2.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x2.cluster0.cpu1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.cluster0_labelle_r	<i>Labeler</i>	-

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.virtioblockd evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2.bp.hdled0.timer. timer.thread_event	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x2.bp.hdled0.timer. timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x2.cluster0.cpu1.l1 dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x2.bp.trusted_key_ storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x2.bp.hdled0	<i>PL370_HDLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x2.bp.secureflashlo ader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2.cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x2.bp.pl111_clcd_1 abeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x2.bp.virtiop9devi ce	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A55x2.bp.trusted_rng	<i>RandomNumberGen erator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x2.bp.pl011_uart2. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.hdled0_label ler	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2.cluster0	Cluster_ARM_Corte x-A55	ARM Cortex-A55 Cluster CT model.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x2	FVP_Base_Cortex_A55x2	Base Platform Compute Subsystem for ARM Cortex A55x2 CT.
FVP_Base_Cortex_A55x2.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55x2.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 3-16 FVP_Base_Cortex-A55x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.17 FVP_Base_Cortex-A55x2+Cortex-A75x2

FVP_Base_Cortex-A55x2+Cortex-A75x2 contains the following instances:

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_cluster0.subcluster1	Subcluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2_cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x2_Cortex_A75x2	FVP_Base_Cortex_A55x2_Cortex_A75x2	Base Platform Compute Subsystem for ARM Cortex A55x2CT_Cortex A75x2CT.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.virtioblockdevice_labeller	Labeler	-
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.hlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.mmcc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2_Cortex_A75x2. clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hlcd0	<i>PL370_HDLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.smse_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hlcd0.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp终端_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp终端_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp终端_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x2_Cortex_A75x2_cluster0_labeller	Labeller	-
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2_pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.nontrustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2_Cortex_A75x2_bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.ap_refclk	<i>MemoryMappedGen ericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. cluster0.cpu3	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x2_Cortex_A75x2. cluster0.cpu2	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2_Cortex_A75x2. cluster0	Cluster_ARM_Cortex-A55_Cortex-A75	ARM Cortex-A55_Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x2_Cortex_A75x2. dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-17 FVP_Base_Cortex-A55x2+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x2_Cortex_A75x2. elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x2_Cortex_A75x2. bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.18 FVP_Base_Cortex-A55x4

FVP_Base_Cortex-A55x4 contains the following instances:

Table 3-18 FVP_Base_Cortex-A55x4 instances

Name	Type	Description
FVP_Base_Cortex_A55x4.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.hdlcd0.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.cluster0.cpu3.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4.bp.hd lcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A55x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x4.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu3.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.cluster0.cpu0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x4.bp.trusted_watc.hdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x4.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.bp.generic_wat.chdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4.cluster0	Cluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55x4.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.cluster0.cpu0.11_deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4.bp.dummy_loca1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu1.11_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A55x4.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.smsc_91c11_1	SMSC_91C11	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x4.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x4.cluster0.cpu0.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A55x4.cluster0.cpu2.12_cache	PVCache	PV Cache.
FVP_Base_Cortex_A55x4.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x4.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4.bp.pl111_clcd_1_abeller	Labeler	-
FVP_Base_Cortex_A55x4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x4.bp.pl111_clcd.p111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.hdled0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x4.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.virtioblockd ^{evise_label}	Labeler	-
FVP_Base_Cortex_A55x4.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A55x4.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-18 FVP_Base_Cortex-A55x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4	FVP_Base_Cortex_A55x4	Base Platform Compute Subsystem for ARM Cortex A55x4 CT.
FVP_Base_Cortex_A55x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A55x4.cluster0.cpu1.l1cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A55x4.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.19 FVP_Base_Cortex-A55x4+Cortex-A75x1

FVP_Base_Cortex-A55x4+Cortex-A75x1 contains the following instances:

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.subcluster1	Subcluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.terminal_1	TelnetTerminal	Telnet terminal interface.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x1. clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.virtiop9device_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.nontrustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0	Cluster_ARM_Cortex-A55_Cortex-A75	ARM Cortex-A55_Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.virtioblockdevice_labeller	<i>Labeller</i>	-

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1	FVP_Base_Cortex_A55x4_Cortex_A75x1	Base Platform Compute Subsystem for ARMCortexA55x4CT_CortexA75x1CT.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x4_Cortex_A75x1. gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x4_Cortex_A75x1. pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-19 FVP_Base_Cortex-A55x4+Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x1. dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x1. bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x1. cluster0.cpu4	ARM_Cortex-A75	ARM Cortex-A75 CT model.

3.20 FVP_Base_Cortex-A55x4+Cortex-A75x2

FVP_Base_Cortex-A55x4+Cortex-A75x2 contains the following instances:

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp终端_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp终端_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp终端_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.virtioP9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A75x2_bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x2. cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x4_Cortex_A75x2. dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.virtioblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hdlcd0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x2. elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0.cpu4	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0.cpu5	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2.cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x2.cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x2.cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x4_Cortex_A75x2.bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2	FVP_Base_Cortex_A55x4_Cortex_A75x2	Base Platform Compute Subsystem for ARM Cortex A55x4CT_Cortex A75x2CT.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0.subcluster1	Subcluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.hlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x4_Cortex_A75x2. pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-20 FVP_Base_Cortex-A55x4+Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0	Cluster_ARM_Cortex-A55_Cortex-A75	ARM Cortex-A55_Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x2. cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x2. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.21 FVP_Base_Cortex-A55x4+Cortex-A75x4

FVP_Base_Cortex-A55x4+Cortex-A75x4 contains the following instances:

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl111_clcd.pl11x_clcd.timer.timer.threa d	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cc1400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.mmcc	<i>MMC</i>	Generic Multimedia Card.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4.cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A75x4.cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4.cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x4.cluster0.cpu6	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4_bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hlcd0.timer.timer	<i>ClockTimerThread64</i> 4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.cpu7	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.cpu4	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.cpu5	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0	Cluster_ARM_Cortex-A55_Cortex-A75	ARM Cortex-A55_Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.virtio_net_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0.subcluster1	Subcluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.hlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl111_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivide is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x4_Cortex_A75x4	FVP_Base_Cortex_A55x4_Cortex_A75x4	Base Platform Compute Subsystem for ARM Cortex A55x4CT_Cortex A75x4CT.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x4_Cortex_A75x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x4_Cortex_A75x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A55x4_Cortex_A75x4. gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.virtioblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x4_Cortex_A75x4. pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-21 FVP_Base_Cortex-A55x4+Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A75x4. bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x4_Cortex_A75x4. cluster0_labeller	<i>Labeller</i>	-

3.22 FVP_Base_Cortex-A55x4+Cortex-A76x2

FVP_Base_Cortex-A55x4+Cortex-A76x2 contains the following instances:

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl041_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl180_mci	PL180 MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_2_3	SP804 Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.virtio_net_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd_labeller	Labeller	-
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_0_1	SP804 Timer	ARM Dual-Timer Module(SP804).

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A76x2	FVP_Base_Cortex_A55x4_Cortex_A76x2	Base Platform Compute Subsystem for ARM Cortex A55x4CT_Cortex A76x2CT.
FVP_Base_Cortex_A55x4_Cortex_A76x2. gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A76x2. dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu1	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu0	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu5	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A55x4_Cortex_A76x2. elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl111_clcd.pl11x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cc1400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu3	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.hdlcd0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu2	ARM_Cortex-A55	ARM Cortex-A55 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.subcluster0	Subcluster_ARM_Cortex-A55	ARM Cortex-A55 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0	Cluster_ARM_Cortex-A55_Cortex-A76	ARM Cortex-A55_Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.cpu4	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A55x4_Cortex_A76x2. cluster0.subcluster1	Subcluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.hdlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2_bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-22 FVP_Base_Cortex-A55x4+Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A55x4_Cortex_A76x2. bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

3.23 FVP_Base_Cortex-A57x1

FVP_Base_Cortex-A57x1 contains the following instances:

Table 3-23 FVP_Base_Cortex-A57x1 instances

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x1.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x1.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x1.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.cci400	<i>CCl400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x1.bp.sp810_sysctr1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1.bp.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.sp810_sysctr.lclkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.reset_or	<i>OrGate</i>	Or Gate.

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x1.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x1.cluster0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x1.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.Timer_0_1.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x1.bp.pl041_aaci	<i>PL041 AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x1.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A57x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1.bp.pl011_uart2_clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.secureSRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1	FVP_Base_Cortex_A57x1	Base Platform Compute Subsystem for ARM Cortex A57x1 CT.
FVP_Base_Cortex_A57x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x1.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x1.bp.virtioblockd evice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A57x1.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.Timer_2_3.c ounter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x1.bp.vis.recorder.r ecordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x1.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.pl011_uart3. clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.refcounter	MemoryMappedCoun terModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x1.cluster0.l2_cach e	PVCache	PV Cache.
FVP_Base_Cortex_A57x1.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.trusted_watc hdog	SP805_Watchdog	ARM Watchdog Module(SP805).

Table 3-23 FVP_Base_Cortex-A57x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

3.24 FVP_Base_Cortex-A57x1-A35x1

FVP_Base_Cortex-A57x1-A35x1 contains the following instances:

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A35x1.bp.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.pl03_1_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x1_A35x1.bp.cloc_kLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x1_A35x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x1_A35x1.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x1_A35x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x1_A35x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.virtual_net_labeler	Labeller	-
FVP_Base_Cortex_A57x1_A35x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.cluster0.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A57x1_A35x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x1_A35x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.host_bridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A57x1_A35x1.bp.pl11_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A35x1.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A35x1.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A57x1_A35x1.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x1_A35x1.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x1_A35x1.cluster1.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x1_A35x1.bp.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1_A35x1.cluster0.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A57x1_A35x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.pl111_1_cled.pl111x_cled	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x1_A35x1.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x1_A35x1.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A35x1.bp.virtio_blockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A57x1_A35x1.bp.nont_rustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x1_A35x1.bp.nont rustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A35x1.bp.ps2k eyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1_A35x1.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A57x1_A35x1.bp.cloc k50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.virti op9device_labeller	Labeler	-
FVP_Base_Cortex_A57x1_A35x1.bp.virti op9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A57x1_A35x1.bp.excl usive_monitor	PVBusExclusiveMon itor	Global exclusive monitor.
FVP_Base_Cortex_A57x1_A35x1.bp.trust ed_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x1_A35x1.bp.sp81 0_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.sp81 0_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.sp81 0_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x1_A35x1.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A35x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x1_A35x1.bp.pl180_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x1_A35x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A35x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A35x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A35x1.bp.flash_loader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A35x1.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A35x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x1_A35x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x1_A35x1.bp.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1_A35x1.bp.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A35x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A35x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1_A35x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1_A35x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A35x1.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1_A35x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x1_A35x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1_A35x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A35x1.bp.pl111_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x1_A35x1.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x1_A35x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A35x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x1_A35x1	FVP_Base_Cortex_A57x1_A35x1	Base Platform Compute Subsystem for ARM Cortex A57x1CT and ARM Cortex A35x1CT.
FVP_Base_Cortex_A57x1_A35x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x1_A35x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x1_A35x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x1_A35x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A35x1.bp.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A35x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc_d0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1_A35x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x1_A35x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.pl111_c lcd_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A35x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x1_A35x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A35x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-24 FVP_Base_Cortex-A57x1-A35x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A35x1.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x1_A35x1.cluster1	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.
FVP_Base_Cortex_A57x1_A35x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x1_A35x1.bp.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A35x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x1_A35x1.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1_A35x1.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A35x1.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x1_A35x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x1_A35x1.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A35x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x1_A35x1.bp.secure_flashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A35x1.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.

3.25 FVP_Base_Cortex-A57x1-A53x1

FVP_Base_Cortex-A57x1-A53x1 contains the following instances:

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A57x1_A53x1.bp.pl11_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A53x1.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x1_A53x1.bp.pl11_1_clcd_labeller	Labeller	-
FVP_Base_Cortex_A57x1_A53x1.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x1_A53x1.bp.virtio_p9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A57x1_A53x1.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A53x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x1_A53x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A53x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A53x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x1_A53x1.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1_A53x1.bp.pl03_1_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x1_A53x1.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x1_A53x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.secu_reflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A53x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A57x1_A53x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A53x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.cloc_k32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x1_A53x1.cluster0_labeller	Labeler	-
FVP_Base_Cortex_A57x1_A53x1.bp.nont_rustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A53x1.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x1_A53x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x1_A53x1.bp.pl05_0_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.cluster1.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x1_A53x1.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A53x1	FVP_Base_Cortex_A57x1_A53x1	Base Platform Compute Subsystem for ARM Cortex A57x1CT and ARM Cortex A53x1CT.
FVP_Base_Cortex_A57x1_A53x1.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x1_A53x1.bp.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A53x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x1_A53x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1_A53x1.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x1_A53x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x1_A53x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A53x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A53x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A53x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x1_A53x1.bp.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A57x1_A53x1.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.pl111_1_cled	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x1_A53x1.bp.virtualblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A57x1_A53x1.cluster1.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x1_A53x1.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A53x1.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x1_A53x1.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.virtualnet_labeller	Labeller	-
FVP_Base_Cortex_A57x1_A53x1.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x1_A53x1.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x1_A53x1.bp.virtualop9device_labeller	Labeller	-
FVP_Base_Cortex_A57x1_A53x1.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x1_A53x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x1_A53x1.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x1_A53x1.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x1_A53x1.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.clock_k35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A53x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x1_A53x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x1_A53x1.bp.pl111_1_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x1_A53x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x1_A53x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x1_A53x1.cluster1.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x1_A53x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x1_A53x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A57x1_A53x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x1_A53x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x1_A53x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x1_A53x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x1_A53x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x1_A53x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x1_A53x1.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A53x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x1_A53x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x1_A53x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x1_A53x1.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 3-25 FVP_Base_Cortex-A57x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x1_A53x1.bp.pl111_cled.pl11x_cled.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x1_A53x1.bp.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x1_A53x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x1_A53x1.bp.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

3.26 FVP_Base_Cortex-A57x2

FVP_Base_Cortex-A57x2 contains the following instances:

Table 3-26 FVP_Base_Cortex-A57x2 instances

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.dummy_loca_l_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x2.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A57x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x2.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x2.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x2.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x2.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x2.bp.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2.bp.virtioblockddevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A57x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.hlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2.bp.hlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x2.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x2.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2.bp.hlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x2.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A57x2.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2	FVP_Base_Cortex_A57x2	Base Platform Compute Subsystem for ARM Cortex A57x2 CT.
FVP_Base_Cortex_A57x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A57x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x2.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2.bp.pl111_cled.p111x_cled	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A57x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i> 4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.smsc_91c11_1	SMS_C_91C11	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x2.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2.bp.sp810_sysctr_1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x2.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2.cluster0.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A57x2.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.cluster0.cpu1.l1dcache	PVCache	PV Cache.

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x2.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2.bp(dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2.bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-26 FVP_Base_Cortex-A57x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x2.bp.secureSRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.

3.27 FVP_Base_Cortex-A57x2-A35x4

FVP_Base_Cortex-A57x2-A35x4 contains the following instances:

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x2_A35x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.audiout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x2_A35x4.cluster1.labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlc d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2_A35x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x2_A35x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A35x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2_A35x4.bp.virtiooblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A57x2_A35x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x2_A35x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlc d0.timer.timer.event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu1	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu2	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu3	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x2_A35x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x2_A35x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A35x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A35x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A35x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x2_A35x4.bp.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.Timerr_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2_A35x4.bp.cloc_k35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.bp.pl031 rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x2_A35x4.bp.virti oblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x2_A35x4.cluster1	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.
FVP_Base_Cortex_A57x2_A35x4.bp.vis.recoder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.Timerr_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A35x4.bp.Timerr_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A35x4.bp.reset_or	<i>OrGate</i>	Or Gate.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.pl111_1_clcd.clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2_A35x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.pl111_1_clcd.clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2_A35x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2_A35x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlcd_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x2_A35x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x2_A35x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.pl111_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x2_A35x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x2_A35x4.bp.Timerr_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.Timerr_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x2_A35x4.bp.pl111_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x2_A35x4.bp.pl111_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A35x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A35x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2_A35x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x2_A35x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlc d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A35x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A35x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A35x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x2_A35x4.bp.nont rustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A35x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x2_A35x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x2_A35x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A35x4.bp.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A35x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x2_A35x4.bp.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x2_A35x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.pl18_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x2_A35x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x2_A35x4	FVP_Base_Cortex_A57x2_A35x4	Base Platform Compute Subsystem for ARM Cortex A57x2CT and ARM Cortex A35x4CT.
FVP_Base_Cortex_A57x2_A35x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A35x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x2_A35x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A35x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.dum.my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A35x4.bp.pl11_1_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A35x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x2_A35x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A35x4.bp.nontestedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A35x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x2_A35x4.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-27 FVP_Base_Cortex-A57x2-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A35x4.bp.cloc_k32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A35x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A35x4.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A35x4.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.

3.28 FVP_Base_Cortex-A57x2-A53x4

FVP_Base_Cortex-A57x2-A53x4 contains the following instances:

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.clock_k32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.hdlc_d0.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2_A53x4.bp.clock_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.smsc_91c11	<i>SMSC_91C11I</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x2_A53x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.pl111_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x2_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x2_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.aprefclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x2_A53x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x2_A53x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A53x4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A53x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.hdlc.d0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x2_A53x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A53x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A53x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x2_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A53x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x2_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.cloc_k300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.secu_reflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.nont_rustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.hdlc_d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.virtual_device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.p111_1_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A53x4.bp.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x2_A53x4.bp.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2_A53x4.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x2_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x2_A53x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A53x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x2_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x2_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x2_A53x4.bp.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x2_A53x4.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x2_A53x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x2_A53x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.pl03_1_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.pl05_0_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x2_A53x4.cluster0_labeller	Labeler	-
FVP_Base_Cortex_A57x2_A53x4.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x2_A53x4.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.pl180_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4	FVP_Base_Cortex_A57x2_A53x4	Base Platform Compute Subsystem for ARM Cortex A57x2CT and ARM Cortex A53x4CT.
FVP_Base_Cortex_A57x2_A53x4.bp.hdlcd_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x2_A53x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x2_A53x4.bp.ve_s ysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x2_A53x4.bp.virti oblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A57x2_A53x4.cluster1 .cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x2_A53x4.bp.Time r_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01 1_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.pl11 1_cled_labeller	Labeller	-
FVP_Base_Cortex_A57x2_A53x4.bp.vis.r ecorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x2_A53x4.cluster1 .cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x2_A53x4.bp.secu reflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A53x4.bp.flash 1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A53x4.bp.flash 0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x2_A53x4.bp.flash loader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A53x4.bp.flash loader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x2_A53x4.bp.pl05 0_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x2_A53x4.bp.pl05 0_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x2_A53x4.bp.virti o_net_labeller	Labeller	-
FVP_Base_Cortex_A57x2_A53x4.cluster0	Cluster_ARM_Corte x-A57	ARM Cortex-A57 Cluster CT model.

Table 3-28 FVP_Base_Cortex-A57x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x2_A53x4.bp.hdlc d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A53x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x2_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x2_A53x4.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.hdlc d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x2_A53x4.bp.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x2_A53x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

3.29 FVP_Base_Cortex-A57x4

FVP_Base_Cortex-A57x4 contains the following instances:

Table 3-29 FVP_Base_Cortex-A57x4 instances

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x4.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x4.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A57x4.bp.hdlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x4.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.cluster0.cpu0.11_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x4.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x4.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x4.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A57x4.cluster0.cpu3.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4.bp.hdlcd0.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A57x4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.cluster0.cpu3	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4.cluster0.cpu2	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.cluster0.cpu2.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.cluster0.cpu1.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A57x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x4.cluster0.cpu2.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x4.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x4	FVP_Base_Cortex_A57x4	Base Platform Compute Subsystem for ARM Cortex A57x4 CT.
FVP_Base_Cortex_A57x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4.cluster0.cpu3.l1_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.dummy_loca1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.hdled0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-29 FVP_Base_Cortex-A57x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x4.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x4.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.30 FVP_Base_Cortex-A57x4-A35x4

FVP_Base_Cortex-A57x4-A35x4 contains the following instances:

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x4_A35x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu3	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu2	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.pl03_1 rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x4_A35x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu2	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu3	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu0	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu1	ARM_Cortex-A35	ARM Cortex-A35 CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x4_A35x4.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu0.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu3.tlbc	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu3.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x4_A35x4.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu3.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.reset_or	OrGate	Or Gate.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.pl111_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A57x4_A35x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A35x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A35x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A35x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A35x4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A35x4.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A57x4_A35x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.cloc_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A35x4.bp.pl111_clcd.pl11x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4_A35x4.bp.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x4_A35x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x4_A35x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A35x4.bp.hdlc_d0.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4_A35x4.bp.secure_flashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A35x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x4_A35x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x4_A35x4.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x4_A35x4.cluster1	Cluster_ARM_Cortex-A35	ARM Cortex-A35 Cluster CT model.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.tzc_400	TZC_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.pl11_1_clcd.pl11x_clcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4_A35x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x4_A35x4.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.pl11_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A35x4.bp.vis.receiver.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.hdlc_d0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4_A35x4.bp.virtio_net_labeller	Labeller	-
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A35x4.bp.virtio_blockdevice	VirtioBlockDevice	virtio block device.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x4_A35x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.nontastedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.cloc_k300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.hdlcd_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x4_A35x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A35x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4_A35x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A35x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x4_A35x4	FVP_Base_Cortex_A57x4_A35x4	Base Platform Compute Subsystem for ARM Cortex A57x4CT and ARM Cortex A35x4CT.
FVP_Base_Cortex_A57x4_A35x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4_A35x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x4_A35x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.virtualblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A35x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A35x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A35x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.hdlc_d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A35x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A35x4.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4_A35x4.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A35x4.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x4_A35x4.bp.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4_A35x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x4_A35x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A35x4.bp.pl18_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x4_A35x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-30 FVP_Base_Cortex-A57x4-A35x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A35x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A35x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x4_A35x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A35x4.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x4_A35x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x4_A35x4.bp.Timerr_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A35x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x4_A35x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A35x4.bp.pl11_1_clcd_labeller	<i>Labeller</i>	-

3.31 FVP_Base_Cortex-A57x4-A53x4

FVP_Base_Cortex-A57x4-A53x4 contains the following instances:

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu1.tlrb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A53x4.bp.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.flash_1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A53x4.bp.flash_0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A53x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A57x4_A53x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A57x4_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A57x4_A53x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A57x4_A53x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu1	ARM_Cortex-A57	ARM Cortex-A57 CT model.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu0	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu3	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu2	ARM_Cortex-A57	ARM Cortex-A57 CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A57x4_A53x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A57x4_A53x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A57x4_A53x4.bp.pl11_1_cled.pl11x_cled.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A57x4_A53x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A57x4_A53x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A57x4_A53x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.cluster1_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4_A53x4.bp.secure_flash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A57x4_A53x4.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A57x4_A53x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4_bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A53x4_bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4_bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A57x4_A53x4.cluster1_cpu0.dtib	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4_bp.clock_LCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4_bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A57x4_A53x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4	FVP_Base_Cortex_A57x4_A53x4	Base Platform Compute Subsystem for ARM Cortex A57x4CT and ARM Cortex A53x4CT.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A57x4_A53x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A57x4_A53x4.bp.pl111_1_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A53x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A57x4_A53x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.cloc_k50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster0	Cluster_ARM_Cortex-A57	ARM Cortex-A57 Cluster CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x4_A53x4.bp.virtioblockdevice_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A53x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A57x4_A53x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.bp.nonttrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A53x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.bp.cloc_k300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.audiout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A57x4_A53x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A57x4_A53x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A53x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A53x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A57x4_A53x4.bp.clocdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.pl111_clcd_labeller	<i>Labeller</i>	-

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A57x4_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A57x4_A53x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A57x4_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4_A53x4.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A57x4_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A57x4_A53x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A57x4_A53x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4_A53x4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A57x4_A53x4.bp.pl03_1_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A57x4_A53x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A57x4_A53x4.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A57x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-31 FVP_Base_Cortex-A57x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.bp.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A57x4_A53x4.cluster0.cpu2.tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A57x4_A53x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A57x4_A53x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A57x4_A53x4.bp.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A57x4_A53x4.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A57x4_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.

3.32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2

FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 contains the following instances:

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu1.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0_labeller	Labeller	-

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.subcluster1	Subcluster_ARM_Cortex-A76AE	ARM Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd.pl11x_clcd.timer.timer .thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu1.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0	Cluster_ARM_Cortex-A65AE_Cortex-A76AE	ARM Cortex-A65AE_Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.reset_or	OrGate	Or Gate.

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hlcd0_labeller	Labeller	-
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hlcd0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivide is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd.pl11x_clcd.timer.timer .thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu0.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu0.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.virtioblockdevice_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.subcluster0	Subcluster_ARM_Cortex-A65AE	ARM Cortex-A65AE Cluster CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl111_clcd.pl11x_clcd.timer.timer 4	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.nontrustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu2	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.cluster0.cpu3	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hdlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.virtio_net_labeller	Labeller	-

Table 3-32 FVP_Base_Cortex-A65AEx2+Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2	FVP_Base_Cortex_A65AEx2_Cortex_A76AEx2	Base Platform Compute Subsystem for ARM Cortex A65AEx2CT_Cortex A76AEx2CT.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65AEx2_Cortex_A76 AEx2.elfloader	<i>ElfLoader</i>	ELF loader component.

3.33 FVP_Base_Cortex-A65AEx4

FVP_Base_Cortex-A65AEx4 contains the following instances:

Table 3-33 FVP_Base_Cortex-A65AEx4 instances

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4.bp.hlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4.bp.dummy_1ocal_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.dram_aliases_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx4.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65AEx4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65AEx4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65AEx4.bp.sp810_systctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65AEx4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_2.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_2.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx4.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.sp810_sy.setrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.sp810_sy.setrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.sp810_sy.setrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.sp810_sy.setrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65AEx4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65AEx4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65AEx4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4.cluster0.cpu_2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65AEx4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_3.l2cache	<i>PVCache</i>	PV Cache.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx4.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65AEx4.cluster0.cpu0.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.cluster0.cpu0.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65AEx4.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx4.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4.bp.pl111_clkd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4.bp.virtiop9d_device_labeller	Labeller	-
FVP_Base_Cortex_A65AEx4.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A65AEx4.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx4.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65AEx4.bp.pl111_clkd.pl11x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx4.cluster0	Cluster_ARM_Cortex-A65AE	ARM Cortex-A65AE Cluster CT model.
FVP_Base_Cortex_A65AEx4.pctl	Base_PowerController	Base Platforms Power Controller.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.pl050_k_mi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65AEx4.bp.pl050_k_mi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx4.bp.hdlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx4.bp.clock300_MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_3.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.bp.pl111_clc_d.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4.cluster0.cpu_3.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4.bp.hdlcd0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4.cluster0.cpu_3.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65AEx4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.cluster0.cpu1.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.cluster0.cpu1.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65AEx4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65AEx4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65AEx4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65AEx4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A65AEx4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65AEx4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65AEx4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A65AEx4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65AEx4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4	FVP_Base_Cortex_A65AEx4	Base Platform Compute Subsystem for ARM Cortex A65AEx4CT.
FVP_Base_Cortex_A65AEx4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65AEx4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65AEx4.cluster0.cpu_1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A65AEx4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-33 FVP_Base_Cortex-A65AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65AEx4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.sp805_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx4.cluster0.cpu_0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx4.cluster0.cpu_3.l1icache	<i>PVCache</i>	PV Cache.

3.34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4

FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 contains the following instances:

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.subcluster1	Subcluster_ARM_Cortex-A76AE	ARM Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.subcluster0	Subcluster_ARM_Cortex-A65AE	ARM Cortex-A65AE Cluster CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl041_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0	Cluster_ARM_Cortex-A65AE_Cortex-A76AE	ARM Cortex-A65AE_Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4	FVP_Base_Cortex_A65AEx4_Cortex_A76AEx4	Base Platform Compute Subsystem for ARM Cortex A65AEx4CT_Cortex A76AEx4CT.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu0.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu0.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu2.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu2.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd.pl11x_clcd.timer.timer .thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu6	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.ve_sysregs	VE_SysRegs	-

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.elfloader	<i>ElfLoader</i>	ELF loader component.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu1.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu1.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu7	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu4	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu5	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu3.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.cluster0.cpu3.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd.pl11x_clcd.timer.timer .thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.hlcd0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl111_clcd_labeller	Labeller	-
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-34 FVP_Base_Cortex-A65AEx4+Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65AEx4_Cortex_A76 AEx4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).

3.35 FVP_Base_Cortex-A65AEx8

FVP_Base_Cortex-A65AEx8 contains the following instances:

Table 3-35 FVP_Base_Cortex-A65AEx8 instances

Name	Type	Description
FVP_Base_Cortex_A65AEx8.cluster0.cpu_2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_6.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_5.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.pl011_uar3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A65AEx8.bp.sp810_sctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65AEx8.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_5.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65AEx8.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx8.bp.dram_aliases_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx8.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_3.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.cluster0.cpu3.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu2.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65AEx8.cluster0	Cluster_ARM_Cortex-A65AE	ARM Cortex-A65AE Cluster CT model.
FVP_Base_Cortex_A65AEx8.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx8.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx8.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx8.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65AEx8.cluster0.cpu4.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx8.bp.dummy_1_ocal_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.virtiop9d_evice	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65AEx8.cluster0.cpu5.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu5.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A65AEx8.bp.hdlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65AEx8.bp.clock100_Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8_bp.pl111_clc_d.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.cluster0.cpu4.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu4.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx8.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx8.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx8.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx8.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65AEx8.cluster0.cpu7.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A65AEx8.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.sp810_sctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.sp810_sctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.sp810_sy sctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.sp810_sy sctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu 7.thread1	ARM_Cortex- A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.clockdivider 0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.hostbridg e	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65AEx8.cluster0.cpu 1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.pl111_clc d.pl11x_cld.timer.timer.thread_event	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx8.bp.securefla sh	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu 0.thread0	ARM_Cortex- A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu 0.thread1	ARM_Cortex- A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.bp.pl111_clc d.pl11x_cld.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx8.cluster0.cpu 7.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.dummy_r am	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.cluster0.cpu6.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.hdlcd0.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65AEx8.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65AEx8.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu5.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.cluster0.cpu2.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu7.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65AEx8.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.cluster0.cpu4.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.hdlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx8.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.cluster0.cpu6.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A65AEx8.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_3.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65AEx8.bp.virtiop9d_evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx8.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65AEx8.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx8.bp.pl180_mcி	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65AEx8.cluster0.cpu_4.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65AEx8.bp.nontruster_dromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx8.bp.clockCL_CD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65AEx8.cluster0.cpu_7.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65AEx8.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.smsc_91c_111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx8.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65AEx8.cluster0.cpu6.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.sp805_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx8.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu5.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx8.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65AEx8.cluster0.cpu1.thread1	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu1.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.cluster0.cpu6.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx8.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65AEx8.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu5.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu7.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65AEx8.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx8.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65AEx8.cluster0.cpu7.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65AEx8.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx8.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65AEx8.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx8.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx8.bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65AEx8.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65AEx8.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65AEx8.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65AEx8.bp.pl111_clcd_pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65AEx8	FVP_Base_Cortex_A65AEx8	Base Platform Compute Subsystem for ARM Cortex A65AEx8CT.
FVP_Base_Cortex_A65AEx8.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A65AEx8.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.pl011_ua_rt0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65AEx8.cluster0.cpu_6.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_6.thread0	ARM_Cortex-A65AE	ARM Cortex-A65AE CT model.
FVP_Base_Cortex_A65AEx8.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_4.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.cluster0.cpu_4.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65AEx8.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A65AEx8.bp.pl011_ua_rt2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65AEx8.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.

Table 3-35 FVP_Base_Cortex-A65AEx8 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65AEx8.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx8.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65AEx8.bp.pl111_clcd.pl11x_cled.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65AEx8.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65AEx8.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65AEx8.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65AEx8.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx8.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65AEx8.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65AEx8.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65AEx8.cluster0.cpu3.l2cache	<i>PVCache</i>	PV Cache.

3.36 FVP_Base_Cortex-A65x1

FVP_Base_Cortex-A65x1 contains the following instances:

Table 3-36 FVP_Base_Cortex-A65x1 instances

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A65x1.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x1.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65x1.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65x1.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.cluster0.cpu0.tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x1.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A65x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A65x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A65x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A65x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.cluster0.cpu0.th.read1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.cluster0.cpu0.th.read0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.hdled0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x1.bp.pl111_clcd_1.labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65x1.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A65x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65x1.bp.pl050_kmi0	<i>PL050 KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x1.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65x1.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A65x1.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x1.bp.hlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65x1.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A65x1.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x1.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x1.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x1.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x1.bp.hdled0.timer. timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65x1.bp.exclusive_m onitor	<i>PVBusExclusiveMon itor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65x1.bp.secureDRA M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.virtioblockd evice_labeler	<i>Labeler</i>	-

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-36 FVP_Base_Cortex-A65x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65x1.cluster0	Cluster_ARM_Cortex-A65	ARM Cortex-A65 Cluster CT model.
FVP_Base_Cortex_A65x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x1.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A65x1.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65x1.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x1	FVP_Base_Cortex_A65x1	Base Platform Compute Subsystem for ARM Cortex A65x1 CT.
FVP_Base_Cortex_A65x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.37 FVP_Base_Cortex-A65x2

FVP_Base_Cortex-A65x2 contains the following instances:

Table 3-37 FVP_Base_Cortex-A65x2 instances

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.virtioblockd_device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.cluster0.cpu1.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65x2.cluster0_labelle_r	<i>Labeller</i>	-
FVP_Base_Cortex_A65x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65x2.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A65x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65x2.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x2.cluster0.cpu1.thread0	ARM_Cortex-A65	ARM Cortex-A65 CT model.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x2.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65x2.cluster0.cpu0.thread0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x2.cluster0.cpu0.thread1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65x2.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x2.bp.reset_or	<i>OrGate</i>	Or Gate.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A65x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A65x2.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.sp810_sysctr.l.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65x2.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A65x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.audioout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x2.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A65x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x2.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.cluster0.cpu0.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.bp.virtioblockd evice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65x2.bp.pl050_kmi0. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65x2.cluster0.cpu1.th read1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.hdlcd0.timer timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65x2.bp.sp810_systcr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.trusted_key_ storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65x2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A65x2.cluster0.cpu1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x2.cluster0	Cluster_ARM_Cortex-A65	ARM Cortex-A65 Cluster CT model.
FVP_Base_Cortex_A65x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.bp.dummy_loca1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A65x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A65x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65x2	FVP_Base_Cortex_A65x2	Base Platform Compute Subsystem for ARM CortexA65x2CT.

Table 3-37 FVP_Base_Cortex-A65x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x2.bp.hdled0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.38 FVP_Base_Cortex-A65x4

FVP_Base_Cortex-A65x4 contains the following instances:

Table 3-38 FVP_Base_Cortex-A65x4 instances

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A65x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.cluster0	Cluster_ARM_Cortex-A65	ARM Cortex-A65 Cluster CT model.
FVP_Base_Cortex_A65x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A65x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A65x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.hdled0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65x4.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A65x4.cluster0.cpu1.llidecache	<i>PVCache</i>	PV Cache.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A65x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A65x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A65x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A65x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x4.cluster0.cpu2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A65x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.cluster0.cpu1.th.read0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.cluster0.cpu0.th.read0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.cluster0.cpu0.th.read1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.cluster0.cpu2.11.dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A65x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.cluster0.cpu2.th.read0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A65x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A65x4.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A65x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A65x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A65x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A65x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A65x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A65x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A65x4.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A65x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A65x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A65x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x4.cluster0.cpu0.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A65x4.cluster0.cpu1.thread1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.cluster0.cpu1.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A65x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A65x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A65x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.cluster0.cpu3.th.read1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.cluster0.cpu3.th.read0	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A65x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A65x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A65x4.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A65x4.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A65x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.cluster0.cpu3.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A65x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A65x4.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A65x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A65x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A65x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A65x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A65x4.bp.hlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A65x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x4.cluster0_labeler	<i>Labeler</i>	-

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A65x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A65x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A65x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A65x4.bp.hdlcd0.timer	<i>ClockTimerThread64</i> 4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x4.cluster0.cpu2.thread1	ARM_Cortex-A65	ARM Cortex-A65 CT model.
FVP_Base_Cortex_A65x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A65x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A65x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A65x4	FVP_Base_Cortex_A65x4	Base Platform Compute Subsystem for ARM Cortex A65x4 CT.
FVP_Base_Cortex_A65x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A65x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A65x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A65x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-38 FVP_Base_Cortex-A65x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A65x4.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A65x4.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.39 FVP_Base_Cortex-A72x1

FVP_Base_Cortex-A72x1 contains the following instances:

Table 3-39 FVP_Base_Cortex-A72x1 instances

Name	Type	Description
FVP_Base_Cortex_A72x1.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A72x1.bp.ap.refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A72x1.bp.smse_91c11_1	SMSC_91C11	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A72x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x1.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A72x1.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A72x1.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Cortex_A72x1.bp.hlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A72x1.bp.hlcd0.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A72x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A72x1.bp.hdlcd0.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1.bp.pl111_cled	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A72x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x1.bp.virtiop9device_labeler	<i>Labeler</i>	-

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x1.bp.pl111_clcd_1abeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x1.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x1.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1.bp.mmc	<i>MMC</i>	Generic Multimedia Card.

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A72x1.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A72x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1.bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x1.bp.pl111_clcd.pl111x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x1.cluster0.cpu0.11icache	PVCache	PV Cache.
FVP_Base_Cortex_A72x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x1.bp.sp810_sysctrl1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x1.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x1.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A72x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A72x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1	FVP_Base_Cortex_A72x1	Base Platform Compute Subsystem for ARM Cortex A72x1 CT.
FVP_Base_Cortex_A72x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-39 FVP_Base_Cortex-A72x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1.bp.Timer_0_1.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A72x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A72x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A72x1.bp.pl111_cled.p111x_cled.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

3.40 FVP_Base_Cortex-A72x1-A53x1

FVP_Base_Cortex-A72x1-A53x1 contains the following instances:

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x1_A53x1.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x1_A53x1.bp.virtiooblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A72x1_A53x1.cluster1.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A72x1_A53x1.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A72x1_A53x1.bpvram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.hdlcd0.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1_A53x1.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A72x1_A53x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A72x1_A53x1.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1_A53x1.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1_A53x1	FVP_Base_Cortex_A72x1_A53x1	Base Platform Compute Subsystem for ARM Cortex A72x1CT and ARM Cortex A53x1CT.
FVP_Base_Cortex_A72x1_A53x1.cluster1.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A72x1_A53x1.bpreflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1_A53x1.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.hdlc_d0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A72x1_A53x1.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x1_A53x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x1_A53x1.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A72x1_A53x1.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x1_A53x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x1_A53x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x1_A53x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A72x1_A53x1.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x1_A53x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A72x1_A53x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1_A53x1.bp.virtio9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x1_A53x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A72x1_A53x1.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A72x1_A53x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A72x1_A53x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A72x1_A53x1.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x1_A53x1.bp.terminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1_A53x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x1_A53x1.bp.hdlc0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1_A53x1.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x1_A53x1.bp.pl111_clcd_labeller	<i>Labeller</i>	-

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.pl11_1_cled.pl11x_cled.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x1_A53x1.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1_A53x1.bp.hdlc_d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x1_A53x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x1_A53x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A72x1_A53x1.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1_A53x1.bp.flash_loader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1_A53x1.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x1_A53x1.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x1_A53x1.bp.hdlc_d0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x1_A53x1.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x1_A53x1.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x1_A53x1.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1_A53x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A72x1_A53x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A72x1_A53x1.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x1_A53x1.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x1_A53x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A72x1_A53x1.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x1_A53x1.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x1_A53x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.hdlc_d0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A72x1_A53x1.bp.dum_my_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x1_A53x1.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1_A53x1.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1_A53x1.bp.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1_A53x1.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.nontestedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x1_A53x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x1_A53x1.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A72x1_A53x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.virtio_net_labeller	Labeller	-
FVP_Base_Cortex_A72x1_A53x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.cluster1_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A72x1_A53x1.bp.sp80_5_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x1_A53x1.bp.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1_A53x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1_A53x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x1_A53x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A72x1_A53x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x1_A53x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x1_A53x1.bp.nontestedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x1_A53x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x1_A53x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x1_A53x1.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x1_A53x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x1_A53x1.bp.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x1_A53x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x1_A53x1.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 3-40 FVP_Base_Cortex-A72x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x1_A53x1.bp.pl03_1_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x1_A53x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x1_A53x1.bp.Timerr_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.Timerr_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.cluster0.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x1_A53x1.bp.Timerr_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1_A53x1.bp.Timerr_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x1_A53x1.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x1_A53x1.bp.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.41 FVP_Base_Cortex-A72x2

FVP_Base_Cortex-A72x2 contains the following instances:

Table 3-41 FVP_Base_Cortex-A72x2 instances

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A72x2.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x2.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x2.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.hlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A72x2.pctl	Base_PowerController	Base Platforms Power Controller.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.virtioblockd device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A72x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A72x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A72x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x2	FVP_Base_Cortex_A72x2	Base Platform Compute Subsystem for ARM Cortex A72x2 CT.
FVP_Base_Cortex_A72x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x2.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A72x2.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A72x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A72x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x2.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x2.bp.hdlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x2.bp.pl111_clcd_1_abeller	Labeler	-
FVP_Base_Cortex_A72x2.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x2.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x2.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A72x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2.bp.pl111_clcd.p111x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x2.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A72x2.bp.virtiop9device_labelller	Labeler	-
FVP_Base_Cortex_A72x2.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x2.cluster0_labelller	Labeler	-
FVP_Base_Cortex_A72x2.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x2.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x2.bp.virtioblockdevice_labeler	<i>Labeler</i>	-

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A72x2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.cluster0.cpu1	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A72x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A72x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A72x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.Timer_2_3.couunter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2.cluster0.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A72x2.bp.hdlcd0_labeler	<i>Labeler</i>	-

Table 3-41 FVP_Base_Cortex-A72x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.42 FVP_Base_Cortex-A72x2-A53x4

FVP_Base_Cortex-A72x2-A53x4 contains the following instances:

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A72x2_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2_A53x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x2_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x2_A53x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A72x2_A53x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2_A53x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2_A53x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2_A53x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x2_A53x4.bp.aprefclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.virtio9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.secure_flashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2_A53x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x2_A53x4.bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x2_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.non_trustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2_A53x4.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2_A53x4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.audiout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x2_A53x4.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x2_A53x4.bp.pl111_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x2_A53x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x2_A53x4.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.smsc_91c11	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A72x2_A53x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A72x2_A53x4.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x2_A53x4.bp.nontestedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x2_A53x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x2_A53x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A72x2_A53x4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu1	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A72x2_A53x4.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x2_A53x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.bp.ve_s ysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x2_A53x4.bp.pl04 1_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.bp.secu reflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x2_A53x4.bp.cloc k35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc d0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc d0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.cloc k100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x2_A53x4.cluster1 .cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x2_A53x4.bp.sp80 5_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x2_A53x4.bp.vis.r ecorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A72x2_A53x4.bp.pl111_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i> 4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A72x2_A53x4.bp.cloc_kLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A72x2_A53x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x2_A53x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x2_A53x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A72x2_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x2_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A72x2_A53x4.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4	FVP_Base_Cortex_A72x2_A53x4	Base Platform Compute Subsystem for ARM Cortex A72x2CT and ARM Cortex A53x4CT.
FVP_Base_Cortex_A72x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2_A53x4.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x2_A53x4.bp.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.pl11_1_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x2_A53x4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x2_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x2_A53x4.bp.hdlc_d0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x2_A53x4.bp.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A72x2_A53x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x2_A53x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x2_A53x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.cluster1_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A72x2_A53x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A72x2_A53x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x2_A53x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2_A53x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x2_A53x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x2_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x2_A53x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A72x2_A53x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x2_A53x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.

Table 3-42 FVP_Base_Cortex-A72x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x2_A53x4.bp.dmc _phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x2_A53x4.bp.dum my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.43 FVP_Base_Cortex-A72x4

FVP_Base_Cortex-A72x4 contains the following instances:

Table 3-43 FVP_Base_Cortex-A72x4 instances

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.virtio_net_labeler	Labeler	-
FVP_Base_Cortex_A72x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x4.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4.bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A72x4.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x4.bp.pl111_clcd.p111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.cluster0.cpu0.11dcache	PVCache	PV Cache.
FVP_Base_Cortex_A72x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4.bp.sp810_sysctr1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x4.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A72x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A72x4.bp.virtioblockd_device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.cluster0.cpu2.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A72x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A72x4.cluster0.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A72x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A72x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x4.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastrucuture component.
FVP_Base_Cortex_A72x4.cluster0.cpu1	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A72x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A72x4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x4.bp.sp810_sysctr1.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.sp810_sysctr1.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.sp810_sysctr1.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4.bp.hdlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A72x4.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x4.bp.sp810_sysctr1.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.cluster0.cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A72x4.cluster0.l2_cach e	PVCache	PV Cache.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A72x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x4.cluster0.cpu1.11_deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x4.bp.pl111_clcd.p111x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.secureSRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A72x4.cluster0.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4.bp.hdlcd0_labeler	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4.bp.pl111_clcd_1abeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x4.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x4.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4.bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x4.cluster0.cpu2	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4.cluster0.cpu3	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.hdlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x4.bp.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A72x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A72x4.bp.Timer_0_1.countr0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4.bp.Timer_0_1.countr1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4	FVP_Base_Cortex_A72x4	Base Platform Compute Subsystem for ARM Cortex A72x4CT.
FVP_Base_Cortex_A72x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A72x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x4.bp.Timer_2_3.countr0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4.bp.Timer_2_3.countr1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-43 FVP_Base_Cortex-A72x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.cluster0.cpu3.11.icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A72x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.

3.44 FVP_Base_Cortex-A72x4-A53x4

FVP_Base_Cortex-A72x4-A53x4 contains the following instances:

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.dram._alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A72x4_A53x4.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.cluster0.i2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A72x4_A53x4.bp.hdlcd_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A72x4_A53x4.cluster0	Cluster_ARM_Cortex-A72	ARM Cortex-A72 Cluster CT model.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu2	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu3	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu1	ARM_Cortex-A72	ARM Cortex-A72 CT model.
FVP_Base_Cortex_A72x4_A53x4.bp.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x4_A53x4.bp.pl18_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A72x4_A53x4.bp.hdlc_d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A72x4_A53x4.bp.secu_reflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4_A53x4.bp.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A72x4_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4	FVP_Base_Cortex_A72x4_A53x4	Base Platform Compute Subsystem for ARM Cortex A72x4CT and ARM Cortex A53x4CT.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4_A53x4.bp.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A72x4_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A72x4_A53x4.bp.virtio9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x4_A53x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x4_A53x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A72x4_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.nontestedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4_A53x4.bp.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.nont_rustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4_A53x4.bp.flash_loader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A72x4_A53x4.bp.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A72x4_A53x4.bp.virtio9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4_A53x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu0	ARM_Cortex-A72	ARM Cortex-A72 CT model.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A72x4_A53x4.bp.refco_unter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A72x4_A53x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x4_A53x4.bp.sp805_wdog	SP805 Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.bp.hdlc0.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.flash_0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4_A53x4.bp.flash_1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A72x4_A53x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A72x4_A53x4.bp.hdlc_d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4_A53x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.bp.cloc_k300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A72x4_A53x4.bp.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A72x4_A53x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A72x4_A53x4.bp.pl03_1_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A72x4_A53x4.bp.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.secu_reflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A72x4_A53x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A72x4_A53x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A72x4_A53x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A72x4_A53x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A72x4_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 3-44 FVP_Base_Cortex-A72x4-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A72x4_A53x4.cluster1.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A72x4_A53x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A72x4_A53x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A72x4_A53x4.bp.hdlc0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A72x4_A53x4.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A72x4_A53x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A72x4_A53x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A72x4_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

3.45 FVP_Base_Cortex-A73x1

FVP_Base_Cortex-A73x1 contains the following instances:

Table 3-45 FVP_Base_Cortex-A73x1 instances

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.secureSRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.cluster0.cpu0.l1_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.cluster0_labelle_r	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A73x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A73x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A73x1.bp终端_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp终端_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1.bp终端_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.cluster0.cpu0	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A73x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A73x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A73x1.bp.clock300MHz_z	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A73x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A73x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A73x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A73x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.ve_sysregs	<i>VE_SysRegs</i>	-
FVP_Base_Cortex_A73x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.hlcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A73x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.pl111_cldc.p111x_cldc.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A73x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A73x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A73x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A73x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.audioout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A73x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x1.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A73x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A73x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A73x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1.bp.virtioblockddevice_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1	FVP_Base_Cortex_A73x1	Base Platform Compute Subsystem for ARM Cortex A73x1 CT.
FVP_Base_Cortex_A73x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x1.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A73x1.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A73x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x1.cluster0	Cluster_ARM_Cortex-A73	ARM Cortex-A73 Cluster CT model.
FVP_Base_Cortex_A73x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A73x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A73x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A73x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).

Table 3-45 FVP_Base_Cortex-A73x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A73x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1.bp.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A73x1.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A73x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1.bp.pl111_clcd.pl111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A73x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A73x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.46 FVP_Base_Cortex-A73x1-A53x1

FVP_Base_Cortex-A73x1-A53x1 contains the following instances:

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.hdlc d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x1_A53x1.bp.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.hdlc d0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1_A53x1.bp.vis.r ecorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.virti op9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A73x1_A53x1.bp.Time r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.Time r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.dmc _phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.ps2 mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x1_A53x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.ps2k eyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1_A53x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A73x1_A53x1.bp.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A73x1_A53x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A73x1_A53x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A73x1_A53x1.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x1_A53x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x1_A53x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1_A53x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1_A53x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x1_A53x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.nont rustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1_A53x1.bp.pl18 0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A73x1_A53x1.bp.sp81 0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.sp81 0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.sp81 0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.sp81 0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.vedc c	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A73x1_A53x1.bp.Time r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.Time r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.refco unter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A73x1_A53x1.bp.pl01 1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x1_A53x1.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A73x1_A53x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A73x1_A53x1.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x1_A53x1.bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A73x1_A53x1.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A73x1_A53x1.bp.pl05_0_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.hdlc_d0.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1_A53x1.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.clockdivider1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1_bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x1_A53x1_bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1_cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1_bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1_A53x1_bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1_A53x1_bp.pl11_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1_A53x1_bp.pl11_1_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x1_A53x1_cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1_A53x1_bp.smse_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A73x1_A53x1_bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x1_A53x1_bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x1_A53x1_bp.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1_cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A73x1_A53x1_cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1_bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A73x1_A53x1_bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.cloc_k300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1_A53x1.bp.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x1_A53x1.bp.secu_reflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1_A53x1.cluster0.cpu0	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x1_A53x1.bp.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x1_A53x1.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A73x1_A53x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A73x1_A53x1.bp.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A73x1_A53x1.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x1_A53x1.bp.sp80_5_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x1_A53x1.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x1_A53x1.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A73x1_A53x1.dapme_mlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A73x1_A53x1.bp.ap_rfclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A73x1_A53x1.bp.cloc_kLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1	FVP_Base_Cortex_A73x1_A53x1	Base Platform Compute Subsystem for ARM Cortex A73x1CT and ARM Cortex A53x1CT.
FVP_Base_Cortex_A73x1_A53x1.bp.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1.bp.secure_flash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x1_A53x1.bp.flash_loader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1_A53x1.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1_A53x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A73x1_A53x1.bp.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A73x1_A53x1.bp.hdlc_d0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x1_A53x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.cloc_k35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1_A53x1.bp.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1_A53x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A73x1_A53x1.bp.nonttrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x1_A53x1.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1_A53x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.hdlcd_d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A73x1_A53x1.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x1_A53x1.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x1_A53x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x1_A53x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.virtualblockdevice_labeller	<i>Labeller</i>	-

Table 3-46 FVP_Base_Cortex-A73x1-A53x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x1_A53x1.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A73x1_A53x1.bp.pl04_1_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A73x1_A53x1.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x1_A53x1.cluster0	Cluster_ARM_Cortex-A73	ARM Cortex-A73 Cluster CT model.
FVP_Base_Cortex_A73x1_A53x1.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A73x1_A53x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A73x1_A53x1.cci400	CC1400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A73x1_A53x1.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x1_A53x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x1_A53x1.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x1_A53x1.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x1_A53x1.bp.pl03_1_RTC	PL031 RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A73x1_A53x1.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.

3.47 FVP_Base_Cortex-A73x2

FVP_Base_Cortex-A73x2 contains the following instances:

Table 3-47 FVP_Base_Cortex-A73x2 instances

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A73x2.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x2.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A73x2.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A73x2.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A73x2.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A73x2.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.virtio_net_labeler	Labeller	-
FVP_Base_Cortex_A73x2.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A73x2.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A73x2.bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A73x2.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A73x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A73x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A73x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2.bp.vis.recorder.recordingDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A73x2.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A73x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2.cluster0.cpu1.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A73x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.ve_sysregs	<i>VE_SysRegs</i>	-
FVP_Base_Cortex_A73x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.cluster0.l2_cache	<i>PVCache</i>	PV Cache.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A73x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A73x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A73x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.cluster0	Cluster_ARM_Cortex-A73	ARM Cortex-A73 Cluster CT model.
FVP_Base_Cortex_A73x2.cluster0.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A73x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A73x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2.cluster0.cpu1	ARM_Cortex-A73	ARM Cortex-A73 CT model.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A73x2.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x2.bp.virtioblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A73x2.cluster0_labeller	Labeller	-
FVP_Base_Cortex_A73x2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A73x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x2.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.cluster0.cpu0.11icache	PVCache	PV Cache.
FVP_Base_Cortex_A73x2.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A73x2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.hlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2.bp.hlcd0.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A73x2.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x2	FVP_Base_Cortex_A73x2	Base Platform Compute Subsystem for ARM Cortex A73x2 CT.
FVP_Base_Cortex_A73x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A73x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A73x2.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.cluster0.cpu0	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A73x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A73x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A73x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x2.bp.virtioblockd ^{evi} c	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A73x2.bp.pl111_clcd_1 ^{abeller}	<i>Labeler</i>	-
FVP_Base_Cortex_A73x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.hdled0.timer. ⁴ timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-47 FVP_Base_Cortex-A73x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A73x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A73x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A73x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A73x2.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

3.48 FVP_Base_Cortex-A73x2-A53x4

FVP_Base_Cortex-A73x2-A53x4 contains the following instances:

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2_A53x4.bp.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2_A53x4.bp.flash_loader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2_A53x4.bp.flash_loader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A73x2_A53x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A73x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.pl03_1 rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A73x2_A53x4.bp.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x2_A53x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x2_A53x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x2_A53x4.bp.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.dummy_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x2_A53x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc_d0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2_A53x4.bp.pl111_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu1	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu0	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A73x2_A53x4	FVP_Base_Cortex_A73x2_A53x4	Base Platform Compute Subsystem for ARM Cortex A73x2CT and ARM Cortex A53x4CT.

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.refco unter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A73x2_A53x4.cluster1 .cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.Tim er_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x2_A53x4.bp.vedc c	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A73x2_A53x4.cluster1 .cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.dmc _phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.bp.Tim er_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2_A53x4.bp.Tim er_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x2_A53x4.bp.secu reflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2_A53x4.cluster0 .cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc d0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A73x2_A53x4.bp.virti oblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A73x2_A53x4.cluster0 .cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc d0.timer.timer.thread_event	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x2_A53x4.bp.flash 1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2_A53x4.bp.flash 0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc d0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x2_A53x4.bp.cloc k32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.pl11 1_clcd_labeller	<i>Labeller</i>	-

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.secu reflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2_A53x4.bp.pl04 1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A73x2_A53x4.bp.vis.r ecorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.cluster1 .cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.cluster1 .cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.Time r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.Time r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.cluster1 .cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.dum my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.bp.cloc k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.gene ric_watchdog	<i>MemoryMappedGen ericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A73x2_A53x4.bp.virti op9device	<i>VirtioP9Device</i>	virtio P9 server.

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A73x2_A53x4.cluster0	Cluster_ARM_Cortex-A73	ARM Cortex-A73 Cluster CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster1	Cluster_ARM_Cortex-A53	ARM Cortex-A53 Cluster CT model.
FVP_Base_Cortex_A73x2_A53x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x2_A53x4.bp.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc_d0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x2_A53x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A73x2_A53x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A73x2_A53x4.bp.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x2_A53x4.cluster0.labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A73x2_A53x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A73x2_A53x4.bp.clock_kLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A73x2_A53x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x2_A53x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A73x2_A53x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A73x2_A53x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.dum_my_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu3.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.virtio_net_labeller	Labeler	-
FVP_Base_Cortex_A73x2_A53x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.cluster0.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A73x2_A53x4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.host_bridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A73x2_A53x4.bp.pl11_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2_A53x4.bp.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x2_A53x4.bp.vis.recorder.recordingDivide	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A73x2_A53x4.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A73x2_A53x4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x2_A53x4.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu2	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu3	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu0	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu1	ARM_Cortex-A53	ARM Cortex-A53 CT model.
FVP_Base_Cortex_A73x2_A53x4.bp.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x2_A53x4.cluster0.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.cloc_k35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A73x2_A53x4.bp.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A73x2_A53x4.bp.virti_loblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x2_A53x4.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.nont_rustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x2_A53x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x2_A53x4.bp.nont_rustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x2_A53x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x2_A53x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x2_A53x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A73x2_A53x4.bp.cloc_k50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.virti_0p9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x2_A53x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x2_A53x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A73x2_A53x4.bp.hdlc_d0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2_A53x4.bp.pl111_1_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x2_A53x4.bp.pl180_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).

Table 3-48 FVP_Base_Cortex-A73x2-A53x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x2_A53x4.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x2_A53x4.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.

3.49 FVP_Base_Cortex-A73x4

FVP_Base_Cortex-A73x4 contains the following instances:

Table 3-49 FVP_Base_Cortex-A73x4 instances

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A73x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A73x4.cluster0.cpu1	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x4.cluster0.cpu0	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x4.cluster0.cpu3	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x4.cluster0.cpu2	ARM_Cortex-A73	ARM Cortex-A73 CT model.
FVP_Base_Cortex_A73x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A73x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A73x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A73x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A73x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x4.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.cluster0.cpu3.11_dcache	<i>PVCache</i>	PV Cache.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A73x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A73x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A73x4.bp.ve_sysregs	<i>VE_SysRegs</i>	-
FVP_Base_Cortex_A73x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A73x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x4.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A73x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A73x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A73x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A73x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.hdled0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A73x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A73x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A73x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A73x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A73x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A73x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A73x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A73x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A73x4.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A73x4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A73x4.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A73x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A73x4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4	FVP_Base_Cortex_A73x4	Base Platform Compute Subsystem for ARM Cortex A73x4 CT.
FVP_Base_Cortex_A73x4.bp.virtioblockd_device_labeller	Labeller	-
FVP_Base_Cortex_A73x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.hlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A73x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A73x4.bp.pl111_clcd_1.abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A73x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A73x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A73x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A73x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A73x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A73x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A73x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x4.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A73x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A73x4.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x4.cluster0	Cluster_ARM_Cortex-A73	ARM Cortex-A73 Cluster CT model.
FVP_Base_Cortex_A73x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A73x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A73x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A73x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A73x4.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A73x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.hlcd0.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A73x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A73x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A73x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-49 FVP_Base_Cortex-A73x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A73x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A73x4.cci400	<i>CCl400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A73x4.bp.pl011_uart0. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.cluster0_labelle r	<i>Labeler</i>	-
FVP_Base_Cortex_A73x4.bp.clock300MH z	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A73x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

3.50 FVP_Base_Cortex-A75x1

FVP_Base_Cortex-A75x1 contains the following instances:

Table 3-50 FVP_Base_Cortex-A75x1 instances

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A75x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A75x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A75x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A75x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A75x1.bp.hdlcd0.timer	<i>ClockTimerThread64</i> <i>4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x1.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x1.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A75x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x1.cci400	<i>CCI400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A75x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A75x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A75x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.Timer_0_1.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A75x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A75x1.bp.Timer_2_3.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A75x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A75x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A75x1.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A75x1.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A75x1.bp.hdled0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A75x1.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A75x1.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A75x1.bp.pl111_clcd.pl111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x1.cluster0.cpu0	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x1.cluster0_labelle	Labeler	-
FVP_Base_Cortex_A75x1.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A75x1.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x1.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x1.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x1.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x1.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x1.bp.pl111_clcd.p111x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A75x1.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A75x1.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A75x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A75x1.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x1.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x1.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A75x1.bp.pl111_clcd.p111x_clcd.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x1.cluster0.cpu0.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A75x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.hdlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x1.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A75x1.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A75x1.bp.virtioblockd evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A75x1.bp.sp810_systrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.sp810_systrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.sp810_systrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.sp810_systrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.pl111_clcd.p l11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x1.bp.pl011_uart1. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.pl111_clcd_1 abeller	<i>Labeller</i>	-
FVP_Base_Cortex_A75x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x1.cluster0	Cluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A75x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A75x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x1.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x1.bp.hdled0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A75x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.

Table 3-50 FVP_Base_Cortex-A75x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x1	FVP_Base_Cortex_A75x1	Base Platform Compute Subsystem for ARM Cortex A75x1 CT.
FVP_Base_Cortex_A75x1.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A75x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.vis.recorder.recordingDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x1.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A75x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A75x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.

3.51 FVP_Base_Cortex-A75x2

FVP_Base_Cortex-A75x2 contains the following instances:

Table 3-51 FVP_Base_Cortex-A75x2 instances

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A75x2.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x2.cluster0	Cluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A75x2.bp.pl111_clcd_1abeller	Labeler	-
FVP_Base_Cortex_A75x2.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A75x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A75x2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A75x2.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x2.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A75x2.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Cortex_A75x2.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x2.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x2.cluster0.cpu0.12_icache	PVCache	PV Cache.
FVP_Base_Cortex_A75x2.cluster0.cpu0.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A75x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.generic_wat chdog	<i>MemoryMappedGen ericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A75x2.bp.pl111_clcd.p l11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A75x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.sp810_sysctr 1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A75x2.bp.ap_refclk	<i>MemoryMappedGen ericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A75x2.cluster0.cpu0.l1 deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x2.bp.secureflashlo ader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x2.cluster0.cpu0.itl b	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x2.bp.nontrusteddro mloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A75x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A75x2.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x2.bp.trusted_watc_hdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A75x2.bp.clock300MHZ	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x2.bp.hlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x2.bp.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A75x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A75x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A75x2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.hdlcd0_labeler	Labeler	-
FVP_Base_Cortex_A75x2.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x2.bp.hdlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x2.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A75x2.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A75x2.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A75x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A75x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x2.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x2.bp.virtioblockd.device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A75x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x2.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A75x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A75x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A75x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A75x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A75x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A75x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A75x2.cluster0.cpu1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A75x2.bp.virtioblockddevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A75x2.bp.reset_or	<i>OrGate</i>	Or Gate.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2	FVP_Base_Cortex_A75x2	Base Platform Compute Subsystem for ARM Cortex A75x2 CT.
FVP_Base_Cortex_A75x2.cluster0.cpu1.ll_deache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x2.cluster0.cpu1.ll_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A75x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A75x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A75x2.cluster0.cpu1	ARM_Cortex-A75	ARM Cortex-A75 CT model.

Table 3-51 FVP_Base_Cortex-A75x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x2.cluster0.cpu0	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x2.bp.virtiop9device_labeller	<i>Labeller</i>	-

3.52 FVP_Base_Cortex-A75x4

FVP_Base_Cortex-A75x4 contains the following instances:

Table 3-52 FVP_Base_Cortex-A75x4 instances

Name	Type	Description
FVP_Base_Cortex_A75x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A75x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A75x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A75x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A75x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x4.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A75x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A75x4.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A75x4.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A75x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A75x4.cluster0	Cluster_ARM_Cortex-A75	ARM Cortex-A75 Cluster CT model.
FVP_Base_Cortex_A75x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x4.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A75x4.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.hdled0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A75x4.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.cluster0.cpu2.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A75x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A75x4.cluster0.cpu0.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A75x4.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x4.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.bp.tzc_400	TZC_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A75x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.cluster0.cpu2.l2 cache	PVCache	PV Cache.
FVP_Base_Cortex_A75x4.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A75x4.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.dummy_loca1_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x4.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A75x4.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A75x4.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A75x4.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A75x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.cluster0.cpu3	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x4.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.cluster0.cpu2	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.cluster0.cpu1	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.cluster0.cpu0	ARM_Cortex-A75	ARM Cortex-A75 CT model.
FVP_Base_Cortex_A75x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A75x4.cluster0.cpu1.l11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A75x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x4.cluster0.cpu0.l12_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A75x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A75x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A75x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A75x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A75x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A75x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A75x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A75x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A75x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A75x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A75x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A75x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A75x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A75x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A75x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.hlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x4.bp.virtioblockd_device_labeller	<i>Labeler</i>	-

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A75x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A75x4.cluster0.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.cluster0.cpu3.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A75x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A75x4.cluster0.cpu2.dt lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A75x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.hdled0.timer. timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A75x4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A75x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A75x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4	FVP_Base_Cortex_A75x4	Base Platform Compute Subsystem for ARM Cortex A75x4 CT.
FVP_Base_Cortex_A75x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A75x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A75x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-52 FVP_Base_Cortex-A75x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A75x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A75x4.cluster0.cpu2.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A75x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A75x4.bp.trusted_watc_hdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A75x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A75x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A75x4.bp.virtio_net_labeler	<i>Labeller</i>	-

3.53 FVP_Base_Cortex-A76

FVP_Base_Cortex-A76 contains the following instances:

Table 3-53 FVP_Base_Cortex-A76 instances

Name	Type	Description
FVP_Base_Cortex_A76.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A76.bp.pl111_clcd.pl1_1x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76.cluster0.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A76.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A76.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76.bp.sp810_sysctrl.lkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A76.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A76.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.virtio_net_labeler	<i>Labeler</i>	-

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.hlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76.bp.hlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A76.cluster0.cpu1.11icache	PVCache	PV Cache.
FVP_Base_Cortex_A76.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.pl111_cled_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76.bp.pl111_cled.pl11x_cled.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76.bp.sp810_sysctrl.lkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.sp810_sysctrl.lkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.sp810_sysctrl.lkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A76.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A76.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76_bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76_bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76_bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76_bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76	FVP_Base_Cortex_A76	Base Platform Compute Subsystem for ARM Cortex A76CT.
FVP_Base_Cortex_A76.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76.cluster0.cpu0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76_bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A76.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76.cluster0.cpu2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76_bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.cluster0.cpu3	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76.cluster0.cpu0	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76.cluster0.cpu1	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76.cluster0.cpu3.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A76.cluster0.cpu3.l2cache	PVCache	PV Cache.
FVP_Base_Cortex_A76.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A76.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76.cluster0.cpu0.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A76.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A76.bp.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.virtioblockdevice_labeller	Labeller	-
FVP_Base_Cortex_A76.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76_bp_ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A76.cluster0_labeller	Labeller	-
FVP_Base_Cortex_A76.cluster0.cpu0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A76.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A76.cluster0	Cluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A76.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A76.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76.cluster0.cpu2.ll1icahe	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A76.bp.hdlcd0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76.cluster0.cpu2	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 3-53 FVP_Base_Cortex-A76 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A76.bp.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

3.54 FVP_Base_Cortex-A76AEx2

FVP_Base_Cortex-A76AEx2 contains the following instances:

Table 3-54 FVP_Base_Cortex-A76AEx2 instances

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.pl111_clc.d.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx2.bp.clock24 MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.hlcd0	PL370_HDLC	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A76AEx2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76AEx2.bp.audioout	AudioOut_SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A76AEx2.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx2.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx2.bp.pl111_clc.d.pl11x_clcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76AEx2.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A76AEx2.bp.clock300 MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.dram_ali as_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76AEx2.bp.clock100 Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.pl111_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76AEx2.bp.virtiop9d_evice_labeller	Labeller	-
FVP_Base_Cortex_A76AEx2.clockdivider_0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.cluster0.cpu_0.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx2.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_Cortex_A76AEx2.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.cluster0.cpu_1.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx2.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A76AEx2.bp.hdlcd0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx2.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76AEx2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx2.bp.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76AEx2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76AEx2.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76AEx2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76AEx2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76AEx2.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76AEx2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A76AEx2.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76AEx2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx2.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76AEx2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.pl011_ua_rt3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.smsc_91c_111	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A76AEx2.bp.pl011_ua_rt3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx2.bp.pl011_ua_rt0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx2.bp.pl011_ua_rt1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76AEx2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx2.bp.clock35_MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76AEx2.bp.pl011_ua_rt2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.clock32K_Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76AEx2.cluster0.cpu0	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A76AEx2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx2.cluster0.cpu0.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx2.cluster0	Cluster_ARM_Cortex-A76AE	ARM Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A76AEx2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76AEx2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A76AEx2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A76AEx2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A76AEx2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A76AEx2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A76AEx2.bp.sp810_syctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.sp810_syctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.sp810_syctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.sp810_syctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.cluster0.cpu0.011icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76AEx2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx2.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76AEx2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A76AEx2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76AEx2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76AEx2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A76AEx2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76AEx2.bp.virtioblockdevice_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76AEx2	FVP_Base_Cortex_A76AEx2	Base Platform Compute Subsystem for ARM Cortex A76AE2CT.
FVP_Base_Cortex_A76AEx2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76AEx2.cluster0.cpu1	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.pl111_clc.d.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx2.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76AEx2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.sp810_systrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76AEx2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx2.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76AEx2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.cluster0.cpu.1.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A76AEx2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.cluster0.cpu_0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A76AEx2.bp.pl111_clk_d_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76AEx2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76AEx2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76AEx2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.

Table 3-54 FVP_Base_Cortex-A76AEx2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx2.bp.sp805_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76AEx2.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.

3.55 FVP_Base_Cortex-A76AEx4

FVP_Base_Cortex-A76AEx4 contains the following instances:

Table 3-55 FVP_Base_Cortex-A76AEx4 instances

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A76AEx4.cluster0	Cluster_ARM_Cortex-A76AE	ARM Cortex-A76AE Cluster CT model.
FVP_Base_Cortex_A76AEx4.cluster0.cpu3.11dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.cluster0_labeller	Labeler	-
FVP_Base_Cortex_A76AEx4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76AEx4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.hlcd0.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx4.cluster0.cpu0.11dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76AEx4.bp.hlcd0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76AEx4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1.l1dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx4.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx4.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx4.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76AEx4.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1.l2cache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76AEx4.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.virtioblockdevice_labeller	Labeler	-
FVP_Base_Cortex_A76AEx4.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx4.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76AEx4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76AEx4.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.tzc_400	TZC_400	TrustZone Address Space Controller.
FVP_Base_Cortex_A76AEx4.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A76AEx4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.hdlcd0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.cluster0.cpu3.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A76AEx4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76AEx4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A76AEx4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A76AEx4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx4.cluster0.cpu_0.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.cluster0.cpu_2.11icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76AEx4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A76AEx4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76AEx4.cluster0.cpu_0.12cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.pl011_ua_rt0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd.clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.dummy_1_ocal_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd.clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76AEx4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.cluster0.cpu_0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.bp.pl011_ua_rt3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76AEx4.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76AEx4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.sp810_sctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76AEx4.cluster0.cpu3.311icache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76AEx4.bp.hdlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A76AEx4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd.p.l11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76AEx4.bp.virtiop9d.device_labeller	Labeller	-
FVP_Base_Cortex_A76AEx4.cluster0.cpu2.211dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76AEx4.bp.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx4.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76AEx4.cluster0.cpu0	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A76AEx4.cluster0.cpu2	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A76AEx4.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76AEx4.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd.p.l11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76AEx4	FVP_Base_Cortex_A76AEx4	Base Platform Compute Subsystem for ARM Cortex A76AEx4CT.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76AEx4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76AEx4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A76AEx4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76AEx4.bp.sp805_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76AEx4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A76AEx4.bp.virtiop9d_device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A76AEx4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76AEx4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76AEx4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76AEx4.bp.clock100_Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76AEx4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76AEx4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76AEx4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76AEx4.cluster0.cpu2.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76AEx4.cluster0.cpu3	ARM_Cortex-A76AE	ARM Cortex-A76AE CT model.
FVP_Base_Cortex_A76AEx4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76AEx4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.sp810_sy sctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.sp810_sy sctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.sp810_sy sctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.sp810_sy sctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76AEx4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A76AEx4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A76AEx4.bp.pl111_clk_d_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76AEx4.bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76AEx4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-55 FVP_Base_Cortex-A76AEx4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76AEx4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76AEx4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76AEx4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A76AEx4.bp.dram_aliases_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

3.56 FVP_Base_Cortex-A76x1

FVP_Base_Cortex-A76x1 contains the following instances:

Table 3-56 FVP_Base_Cortex-A76x1 instances

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A76x1.cci400	<i>CCl400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A76x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A76x1.cluster0	Cluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A76x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A76x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76x1.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76x1.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.ve_sysregs	<i>VE_SysRegs</i>	-
FVP_Base_Cortex_A76x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A76x1.bp.hlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A76x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76x1.bp.virtioblockd ^d evice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A76x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A76x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A76x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.vis.recorder.recordingDivide ^r r	<i>ClockDivider</i>	A ClockDivide ^r r is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivide ^r r), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.cluster0.cpu0.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76x1.bp.vedcc	<i>VEDCC</i>	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A76x1.bp.secureSRA M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76x1.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A76x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x1.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A76x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A76x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x1.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A76x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x1.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x1.cluster0.cpu0	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A76x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A76x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x1.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76x1.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.sp810_systcl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.sp810_systcl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76x1.bp.secureDRA_M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-56 FVP_Base_Cortex-A76x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x1.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A76x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76x1.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.sp810_sysctrl_1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x1	FVP_Base_Cortex_A76x1	Base Platform Compute Subsystem for ARM Cortex A76x1CT.
FVP_Base_Cortex_A76x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

3.57 FVP_Base_Cortex-A76x2

FVP_Base_Cortex-A76x2 contains the following instances:

Table 3-57 FVP_Base_Cortex-A76x2 instances

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.nontrustedromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x2.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76x2.bp.sp810_sysctr1.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.sp810_sysctr1.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.sp810_sysctr1.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A76x2.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Cortex_A76x2.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.dummy_loca1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A76x2.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A76x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76x2.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A76x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A76x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A76x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x2.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A76x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x2.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x2.bp.sp810_sysctr1.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x2.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x2.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x2.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x2.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A76x2.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x2.cluster0.cpu1.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A76x2.cluster0.cpu1.11_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A76x2.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x2.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x2.bp.hdled0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A76x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76x2.bp.pl111_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A76x2.cluster0	Cluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A76x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.virtiop9device_labeller	<i>Labeller</i>	-

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A76x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x2.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.virtio_net_labeler	<i>Labeler</i>	-

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A76x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x2.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A76x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x2.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A76x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A76x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x2.bp.virtioblockd ^e vice_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x2.bp.exclusive_m ^o nitor	<i>PVBusExclusiveMonⁱtior</i>	Global exclusive monitor.
FVP_Base_Cortex_A76x2.cluster0.cpu0.itl ^b	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x2.cluster0.cpu0	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x2.cluster0.cpu1	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x2.cluster0.cpu1.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x2.bp.trusted_nv_c ^o unter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76x2.cluster0_labelle ^r	<i>Labeler</i>	-
FVP_Base_Cortex_A76x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-57 FVP_Base_Cortex-A76x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x2.bp.secureSRA M	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x2	FVP_Base_Cortex_A76x2	Base Platform Compute Subsystem for ARM Cortex A76x2CT.
FVP_Base_Cortex_A76x2.bp.smsc_91c11 1	<i>SMSC_91C11I</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A76x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

3.58 FVP_Base_Cortex-A76x4

FVP_Base_Cortex-A76x4 contains the following instances:

Table 3-58 FVP_Base_Cortex-A76x4 instances

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.cluster0.cpu2.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A76x4.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A76x4.bp.virtioblockd_device_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A76x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x4.bp.dummy_loc1_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.virtio_net_labeler	Labeler	-
FVP_Base_Cortex_A76x4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A76x4.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x4.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.virtiop9device_labeler	Labeler	-
FVP_Base_Cortex_A76x4.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A76x4.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.pl111_clcd.pl111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x4.cci400	CC1400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A76x4.cluster0_labeler	Labeler	-
FVP_Base_Cortex_A76x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.bp.reset_or	OrGate	Or Gate.
FVP_Base_Cortex_A76x4.cluster0.cpu0	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x4.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A76x4.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A76x4.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.cluster0	Cluster_ARM_Cortex-A76	ARM Cortex-A76 Cluster CT model.
FVP_Base_Cortex_A76x4.bp.pl111_clcd.p111x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x4.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A76x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_Base_Cortex_A76x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A76x4.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A76x4.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu3.l2_cache	PVCache	PV Cache.
FVP_Base_Cortex_A76x4.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.pl111_clcd_1_abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A76x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.cluster0.cpu3.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A76x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A76x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A76x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A76x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu2.itlb	<i>TlbCadi</i>	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A76x4.cluster0.cpu0.11_decache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.mmmc	<i>MMC</i>	Generic Multimedia Card.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.hdled0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A76x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A76x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A76x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A76x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A76x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A76x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A76x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu1.ll_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu2.ll_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A76x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A76x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A76x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A76x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.cluster0.cpu3.ll_dcache	<i>PVCache</i>	PV Cache.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A76x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A76x4.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A76x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A76x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A76x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.cluster0.cpu1	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A76x4.cluster0.cpu2	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x4.cluster0.cpu3	ARM_Cortex-A76	ARM Cortex-A76 CT model.
FVP_Base_Cortex_A76x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A76x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A76x4.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.cluster0.cpu2.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A76x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A76x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A76x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A76x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A76x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A76x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-58 FVP_Base_Cortex-A76x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A76x4.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.pl111_clcd.p_l11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A76x4.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A76x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A76x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A76x4	FVP_Base_Cortex_A76x4	Base Platform Compute Subsystem for ARM Cortex A76x4 CT.

3.59 FVP_Base_Cortex-A77x1

FVP_Base_Cortex-A77x1 contains the following instances:

Table 3-59 FVP_Base_Cortex-A77x1 instances

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x1.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A77x1.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Cortex_A77x1.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x1.bp.pl111_clcd_1.abeller	Labeler	-
FVP_Base_Cortex_A77x1.bp.mmc	MMC	Generic Multimedia Card.
FVP_Base_Cortex_A77x1.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A77x1.bp.pl111_clcd.p111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x1.clockdivider0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.cluster0.cpu0.l2cache	PVCache	PV Cache.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A77x1.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A77x1.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x1.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.virtiop9device_labeller	Labeller	-
FVP_Base_Cortex_A77x1.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A77x1.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A77x1.bp.hdlcd0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A77x1.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A77x1.bp.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A77x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A77x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A77x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x1.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x1.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.hdlcd0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.hd lcd0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A77x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A77x1	FVP_Base_Cortex_A77x1	Base Platform Compute Subsystem for ARM Cortex A77x1CT.
FVP_Base_Cortex_A77x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A77x1.cluster0	Cluster_ARM_Cortex-A77	ARM Cortex-A77 Cluster CT model.
FVP_Base_Cortex_A77x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A77x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A77x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A77x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.sp810_sysctr1.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.hlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x1.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.elfloader	<i>ElfLoader</i>	ELF loader component.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.sp810_sysctr1	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Cortex_A77x1.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x1.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x1.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Cortex_A77x1.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Cortex_A77x1.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A77x1.bp.pl111_clcd.p111x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x1.bp.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.hdlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x1.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A77x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A77x1.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.cluster0.cpu0	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x1.bp.virtioblockd.device_labeller	Labeller	-

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A77x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A77x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A77x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A77x1.cluster0.cpu0.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x1.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A77x1.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A77x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A77x1.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A77x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 3-59 FVP_Base_Cortex-A77x1 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x1.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x1.bp.sp810_sysctr1.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Cortex_A77x1.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x1.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Cortex_A77x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x1.bp.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x1.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.

3.60 FVP_Base_Cortex-A77x2

FVP_Base_Cortex-A77x2 contains the following instances:

Table 3-60 FVP_Base_Cortex-A77x2 instances

Name	Type	Description
FVP_Base_Cortex_A77x2.cluster0.cpu1.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x2.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A77x2.bp.sp810_systrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.sp810_systrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.sp810_systrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.sp810_systrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.elfloader	ElfLoader	ELF loader component.
FVP_Base_Cortex_A77x2.cluster0.cpu0.11_icache	PVCache	PV Cache.
FVP_Base_Cortex_A77x2.bp.pl111_cled_1abeller	Labeler	-

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A77x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A77x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A77x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A77x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.Timer_0_1.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.Timer_0_1.c_lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x2.bp.hdled0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A77x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Cortex_A77x2.cluster0	Cluster_ARM_Cortex-A77	ARM Cortex-A77 Cluster CT model.
FVP_Base_Cortex_A77x2.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A77x2.bp.Timer_2_3.c_lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.cluster0.cpu0.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x2.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x2.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A77x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A77x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A77x2.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A77x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A77x2	<i>FVP_Base_Cortex_A77x2</i>	Base Platform Compute Subsystem for ARM Cortex A77x2CT.
FVP_Base_Cortex_A77x2.bp.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A77x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.cluster0.cpu1.11_dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A77x2.cluster0.cpu0.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Cortex_A77x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.sp810_sysctr1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A77x2.bp.virtioblockdevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A77x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x2.bp.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x2.bp.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A77x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A77x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A77x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.cluster0.cpu1.l2_cache	<i>PVCache</i>	PV Cache.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A77x2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A77x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A77x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x2.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A77x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A77x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A77x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A77x2.bp.pl111_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x2.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-60 FVP_Base_Cortex-A77x2 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A77x2.cluster0.cpu1	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x2.cluster0.cpu0	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x2.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A77x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A77x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A77x2.bp.mmmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Cortex_A77x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A77x2.cluster0.cpu1.11_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.61 FVP_Base_Cortex-A77x4

FVP_Base_Cortex-A77x4 contains the following instances:

Table 3-61 FVP_Base_Cortex-A77x4 instances

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x4.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x4.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x4.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Cortex_A77x4.cluster0.cpu1.l1_dcache	PVCache	PV Cache.
FVP_Base_Cortex_A77x4.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.bp.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A77x4.bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A77x4.bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_Base_Cortex_A77x4.bp.hd lcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.pl111_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x4.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Cortex_A77x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Cortex_A77x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Cortex_A77x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.bp.virtioblockddevice_labeller	<i>Labeller</i>	-
FVP_Base_Cortex_A77x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.cluster0.cpu0.tlb	TlbCadi	TLB - instruction, data or unified.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Cortex_A77x4.bp.Timer_2_3.c lk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.bp.Timer_2_3.c lk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Cortex_A77x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Cortex_A77x4.bp.Timer_0_1.c ounter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x4.bp.Timer_0_1.c ounter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x4.bp.virtiop9devi ce	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Cortex_A77x4.bp.Timer_2_3.c ounter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x4.bp.Timer_2_3.c ounter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Cortex_A77x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Cortex_A77x4.cluster0.cpu3	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x4.cluster0.cpu1.itl b	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Cortex_A77x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.cluster0.cpu2.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.bp.hdlcd0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Cortex_A77x4.cluster0	Cluster_ARM_Cortex-A77	ARM Cortex-A77 Cluster CT model.
FVP_Base_Cortex_A77x4.cluster0.cpu0.l1d cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.cluster0.cpu1	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x4.cluster0.cpu0	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x4.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Cortex_A77x4.cluster0.cpu2	ARM_Cortex-A77	ARM Cortex-A77 CT model.
FVP_Base_Cortex_A77x4.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.smsc_91c11_1	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_Base_Cortex_A77x4.bp.hdlcd0_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Cortex_A77x4.cluster0.cpu3.l2 cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Cortex_A77x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Cortex_A77x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x4.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x4.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Cortex_A77x4.bp.sp810_sysctr1.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4	FVP_Base_Cortex_A77x4	Base Platform Compute Subsystem for ARM Cortex A77x4 CT.
FVP_Base_Cortex_A77x4.bp.pl111_clcd.p111x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x4.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.cluster0.cpu1.l2cache	PVCache	PV Cache.
FVP_Base_Cortex_A77x4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Cortex_A77x4.cluster0.cpu2.l1icache	PVCache	PV Cache.
FVP_Base_Cortex_A77x4.bp.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A77x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Cortex_A77x4.gic_distributor	GIC_IRI	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Cortex_A77x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Cortex_A77x4.bp.dummy_loc1_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.cluster0.cpu3.dt_lb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x4.bp.sp810_sysctr1.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.sp810_sysctr1.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.sp810_sysctr1.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Cortex_A77x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Cortex_A77x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Cortex_A77x4.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x4.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x4.cluster0.cpu3.l1_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Cortex_A77x4.bp.virtioblockddevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Cortex_A77x4.cluster0.cpu0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.cluster0.cpu1.l1_icache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Cortex_A77x4.bp.sp810_sysctrl1	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Cortex_A77x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Cortex_A77x4.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Cortex_A77x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x4.cluster0.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Cortex_A77x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Cortex_A77x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Cortex_A77x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Cortex_A77x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.ve_sysregs	VE_SysRegs	-

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A77x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.pl111_clcd.p111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Cortex_A77x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Cortex_A77x4.bp.pl111_clcd_1abeller	<i>Labeler</i>	-
FVP_Base_Cortex_A77x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Cortex_A77x4.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Cortex_A77x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Cortex_A77x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-61 FVP_Base_Cortex-A77x4 instances (continued)

Name	Type	Description
FVP_Base_Cortex_A77x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Cortex_A77x4.bp.pl111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Cortex_A77x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Cortex_A77x4.bp.pl111_clcd.p111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Cortex_A77x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Cortex_A77x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Cortex_A77x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Cortex_A77x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Cortex_A77x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.

3.62 FVP_Base_Neoverse-E1x1

FVP_Base_Neoverse-E1x1 contains the following instances:

Table 3-62 FVP_Base_Neoverse-E1x1 instances

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_E1x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Neoverse_E1x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_E1x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.cluster0.cpu0.d_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_E1x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_E1x1.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_E1x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Neoverse_E1x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.cluster0.cpu0.i_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x1.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_E1x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_E1x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x1.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x1.bp.virtioblock_device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Neoverse_E1x1.bp.flashloader_1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x1.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_E1x1.bp.smsc_91c11	SMSC_91C11I	SMSC 91C111 ethernet controller.
FVP_Base_Neoverse_E1x1.bp.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_E1x1.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Neoverse_E1x1.bp.pl111_clcd.pl11x_clcd.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_E1x1.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_E1x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_E1x1.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.pl111_clcd.pl11x_clcd.timer.timer_thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_E1x1.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Neoverse_E1x1.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x1.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.hdlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.pl111_clcd. pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x1.bp.pl111_clcd. labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Neoverse_E1x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Neoverse_E1x1.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x1.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Neoverse_E1x1.bp.vis.recorder. .playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.pl111_clcd. pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x1.bp.dummy_loc al_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.clock300M Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_E1x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.virtio_net_1_abeller	<i>Labeler</i>	-
FVP_Base_Neoverse_E1x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Neoverse_E1x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.trusted_wat_chdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.cluster0.cpu0.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.cluster0.cpu0.1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Neoverse_E1x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_E1x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x1.bp.pl031 rtc	<i>PL031 RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_E1x1.bp.pl111_clcd.pl11x_clcd	<i>PL11x CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_E1x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_E1x1.bp.sp805_wdog	<i>SP805 Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x1.bp.pl180_mci	<i>PL180 MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Neoverse_E1x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_E1x1.cluster0.cpu0.1_2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1	FVP_Base_Neoverse_E1x1	Base Platform Compute Subsystem for ARMNeoverseE1x1CT.
FVP_Base_Neoverse_E1x1.bp.virtioblock_device_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_E1x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x1.cluster0.cpu0.1_1icache	<i>PVCache</i>	PV Cache.

Table 3-62 FVP_Base_Neoverse-E1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x1.bp.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_E1x1.bp.reset_or	OrGate	Or Gate.
FVP_Base_Neoverse_E1x1.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x1.bp mmc	MMC	Generic Multimedia Card.
FVP_Base_Neoverse_E1x1.cluster0	Cluster_ARM_Neoverse-E1	ARM Neoverse-E1 Cluster CT model.
FVP_Base_Neoverse_E1x1.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Neoverse_E1x1.cluster0.cpu0.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x1.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x1.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x1.bp.hdlcd0_labeller	Labeller	-
FVP_Base_Neoverse_E1x1.bp.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x1.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x1.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x1.bp.hdlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x1.bp.trusted_nv_counter	NonVolatileCounter	Trusted Non-Volatile Counter unit.

3.63 FVP_Base_Neoverse-E1x2

FVP_Base_Neoverse-E1x2 contains the following instances:

Table 3-63 FVP_Base_Neoverse-E1x2 instances

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Neoverse_E1x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.cluster0.cpu1.i_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x2.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Neoverse_E1x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_E1x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Neoverse_E1x2.bp.virtioblock_device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Neoverse_E1x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_E1x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Neoverse_E1x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_E1x2.bp.hdlcd0.time.r.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_E1x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x2.bp.virtio_net_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x2.bp.sp810_sysctr.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.sp810_sysctr.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.sp810_sysctr.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.sp810_sysctr.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.cluster0	Cluster_ARM_Neoverse-E1	ARM Neoverse-E1 Cluster CT model.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_E1x2.cluster0.cpu0.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x2.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x2.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x2.bp.ps2keybaord	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Neoverse_E1x2.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_E1x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Neoverse_E1x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.vis.recorder.recordingDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Neoverse_E1x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Neoverse_E1x2.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x2.cluster0.cpu1.12cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x2.cluster0.cpu1.1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_E1x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.cluster0.cpu0.1ldcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x2.bp.virtiop9device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x2.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Neoverse_E1x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Neoverse_E1x2.bp.ve_sysregs	<i>VE_SysRegs</i>	-
FVP_Base_Neoverse_E1x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x2.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_E1x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_E1x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_E1x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_E1x2.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x2.cluster0.cpu0.1_2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x2.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x2.cluster0.cpu1.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x2.cluster0.cpu1.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x2.cluster0.cpu0.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_E1x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_E1x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x2.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x2.bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x2.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Neoverse_E1x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Neoverse_E1x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Neoverse_E1x2	FVP_Base_Neoverse_E1x2	Base Platform Compute Subsystem for ARMNeoverseE1x2CT.
FVP_Base_Neoverse_E1x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_E1x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_E1x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x2.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.cluster0.cpu1.d_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.virtioblock device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Neoverse_E1x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_E1x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_E1x2.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x2.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_E1x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 3-63 FVP_Base_Neoverse-E1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x2.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x2.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_E1x2.cluster0.cpu0.1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_E1x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_E1x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

3.64 FVP_Base_Neoverse-E1x4

FVP_Base_Neoverse-E1x4 contains the following instances:

Table 3-64 FVP_Base_Neoverse-E1x4 instances

Name	Type	Description
FVP_Base_Neoverse_E1x4.cluster0.cpu2.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.bp.virtio_net_labeler	<i>Labeler</i>	-
FVP_Base_Neoverse_E1x4.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Neoverse_E1x4.cluster0	Cluster_ARM_Neoverse-E1	ARM Neoverse-E1 Cluster CT model.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.12cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.11cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_E1x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Neoverse_E1x4.bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_E1x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x4.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.cluster0.cpu2.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Neoverse_E1x4.cluster0.cpu3.1_2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_E1x4.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_E1x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.hlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.1_1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x4.cluster0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Neoverse_E1x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Neoverse_E1x4.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_E1x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_E1x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_E1x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x4.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_E1x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_E1x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Neoverse_E1x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x4.bp.hlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.sp810_sysctr.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.sp810_sysctr.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.sp810_sysctr.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.sp810_sysctr.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_E1x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_E1x4.cluster0.cpu3.thread0	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.
FVP_Base_Neoverse_E1x4.cluster0.cpu3.thread1	ARM_Neoverse-E1	ARM Neoverse-E1 CT model.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_E1x4.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.clock32KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x4.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_E1x4.bp.hdlcd0.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_E1x4.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Neoverse_E1x4.bp.refcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_E1x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_E1x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Neoverse_E1x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Neoverse_E1x4.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_E1x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x4.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_E1x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Neoverse_E1x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_E1x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_E1x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.smsc_91c11	SMS_C_91C111	SMSC 91C111 ethernet controller.
FVP_Base_Neoverse_E1x4.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.d.tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_E1x4.bp.dram_alias_warning	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x4.cluster0.cpu2.1.2cache	PVCache	PV Cache.
FVP_Base_Neoverse_E1x4.cluster0.cpu2.1.1icache	PVCache	PV Cache.
FVP_Base_Neoverse_E1x4.bp.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.cluster0.cpu2.1.1dcache	PVCache	PV Cache.
FVP_Base_Neoverse_E1x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.cluster0.cpu0.1.1dcache	PVCache	PV Cache.
FVP_Base_Neoverse_E1x4.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.cluster0.cpu0.i_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_E1x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_E1x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_E1x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_E1x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_E1x4.bp.virtioblock_device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Neoverse_E1x4.bp.virtioblock_device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_E1x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Neoverse_E1x4	FVP_Base_Neoverse_E1x4	Base Platform Compute Subsystem for ARMNeoverseE1x4CT.
FVP_Base_Neoverse_E1x4.cluster0.cpu1.l2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_E1x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Neoverse_E1x4.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-64 FVP_Base_Neoverse-E1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_E1x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_E1x4.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_E1x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_E1x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Neoverse_E1x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.virtiop9device_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_E1x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_E1x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Neoverse_E1x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

3.65 FVP_Base_Neoverse-N1x1

FVP_Base_Neoverse-N1x1 contains the following instances:

Table 3-65 FVP_Base_Neoverse-N1x1 instances

Name	Type	Description
FVP_Base_Neoverse_N1x1.cluster0_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_N1x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_N1x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_N1x1.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x1.bp.ps2keybaord	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_N1x1.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Neoverse_N1x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Neoverse_N1x1.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.virtioblock_device	<i>VirtioBlockDevice</i>	virtio block device.

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.virtioblock device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_N1x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_N1x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Neoverse_N1x1.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x1.cluster0.cpu0.1 1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_N1x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.pl050_kmi 1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_N1x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x1.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Neoverse_N1x1.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Neoverse_N1x1.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x1.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x1.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x1.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x1.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x1.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.hlcd0.time.r.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.sp810_sysctr.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Neoverse_N1x1.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_N1x1.cluster0.cpu0.1_l1cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x1.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x1.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x1.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x1.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_N1x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.sp810_sysctr.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x1.bp.sp810_sysctr.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.cluster0	Cluster_ARM_Neoverse-N1	ARM Neoverse-N1 Cluster CT model.
FVP_Base_Neoverse_N1x1.cluster0.cpu0	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Neoverse_N1x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Neoverse_N1x1.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Neoverse_N1x1.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_N1x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Neoverse_N1x1	FVP_Base_Neoverse_N1x1	Base Platform Compute Subsystem for ARMNeoverseN1x1CT.

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_N1x1.bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x1.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_N1x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_N1x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_N1x1.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_N1x1.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_N1x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.cluster0.cpu0.1_2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x1.bp.dummy_C_F	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Neoverse_N1x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Neoverse_N1x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x1.bp.virtio_net_labeler	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x1.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Neoverse_N1x1.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_N1x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Neoverse_N1x1.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd_labeler	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x1.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_N1x1.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_N1x1.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-65 FVP_Base_Neoverse-N1x1 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x1.bp.hdled0	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_N1x1.bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd. pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_N1x1.bp.hdled0.time r.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x1.bp.hostbridge	HostBridge	Host Socket Interface Component.
FVP_Base_Neoverse_N1x1.bp.virtiop9dev ice_labeler	Labeler	-
FVP_Base_Neoverse_N1x1.bp.smsc_91c1 11	SMS_C_91C11	SMSC 91C111 ethernet controller.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd. pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x1.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x1.bp.pl111_clcd. pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x1.bp.clock300M Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.66 FVP_Base_Neoverse-N1x2

FVP_Base_Neoverse-N1x2 contains the following instances:

Table 3-66 FVP_Base_Neoverse-N1x2 instances

Name	Type	Description
FVP_Base_Neoverse_N1x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_N1x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.virtioblock_device_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x2.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Neoverse_N1x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_N1x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_Neoverse_N1x2.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x2.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x2.bp.dummy_lo_cal_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Neoverse_N1x2.bp.pl111_cled.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_N1x2.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_N1x2.cluster0.cpu0	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x2.cluster0.cpu1	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_N1x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_Neoverse_N1x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_N1x2.bp.pl111_clcd. pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_N1x2.bp.pl050_kmi_1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_N1x2.bp.pl050_kmi_0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_N1x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_N1x2.cluster0.cpu1. tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_Neoverse_N1x2.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_N1x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Neoverse_N1x2.bp.flashloader_1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x2.bp.flashloader_0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_N1x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Neoverse_N1x2.bp mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Neoverse_N1x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_N1x2.cluster0.cpu0.1 1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x2.cluster0.cpu1.1 1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.cluster0.cpu0.1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x2.bp.hlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x2.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_N1x2.bp.pl111_clcd_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_N1x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2	FVP_Base_Neoverse_N1x2	Base Platform Compute Subsystem for ARMNeoverseN1x2CT.
FVP_Base_Neoverse_N1x2.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Neoverse_N1x2.bp.virtioblock device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Neoverse_N1x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_Base_Neoverse_N1x2.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.vis.recorder .recordingDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.cluster0	Cluster_ARM_Neoverse-N1	ARM Neoverse-N1 Cluster CT model.
FVP_Base_Neoverse_N1x2.cluster0_labeler	<i>Labeler</i>	-

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_N1x2.cluster0.cpu1.1ldcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x2.bp.sp810_sysctr.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.sp810_sysctr.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.sp810_sysctr.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.sp810_sysctr.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i> 4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.hdled0_labeller	<i>Labeler</i>	-
FVP_Base_Neoverse_N1x2.bp.pl011_uart_0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x2.bp.smsc_91c11	<i>SMSC_91C11</i>	SMSC 91C111 ethernet controller.
FVP_Base_Neoverse_N1x2.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_N1x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_N1x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_N1x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x2.bp.hdled0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x2.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x2.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x2.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x2.bp.tzc_400	Tzc_400	TrustZone Address Space Controller.
FVP_Base_Neoverse_N1x2.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_N1x2.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_N1x2.bp.dummy_C_F	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_N1x2.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_N1x2.cluster0.cpu1.12cache	PVCache	PV Cache.
FVP_Base_Neoverse_N1x2.bp.pl111_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x2.pctl	Base_PowerController	Base Platforms Power Controller.
FVP_Base_Neoverse_N1x2.bp.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.cluster0.cpu0.12cache	PVCache	PV Cache.
FVP_Base_Neoverse_N1x2.bp.virtiop9device_labeler	Labeler	-

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_N1x2.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_N1x2.bp.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Neoverse_N1x2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_Base_Neoverse_N1x2.bp.virtio_net_1_abeller	Labeller	-
FVP_Base_Neoverse_N1x2.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x2.bp.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x2.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Neoverse_N1x2.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.secureflash_loader	FlashLoader	A device that can preload a gzipped image into flash at startup.

Table 3-66 FVP_Base_Neoverse-N1x2 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x2.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x2.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

3.67 FVP_Base_Neoverse-N1x4

FVP_Base_Neoverse-N1x4 contains the following instances:

Table 3-67 FVP_Base_Neoverse-N1x4 instances

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_Neoverse_N1x4.cluster0.cpu0.1_lcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_Neoverse_N1x4.bp.hdled0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_Neoverse_N1x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_Neoverse_N1x4.cluster0.cpu1.1_2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.vis.recorder_recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.clock300MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_Neoverse_N1x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_Neoverse_N1x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_Neoverse_N1x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_Neoverse_N1x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu1.1icache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_Neoverse_N1x4.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_Neoverse_N1x4.cluster0.cpu3.12cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.cluster0.cpu2.12cache	<i>PVCache</i>	PV Cache.

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd.pl11x_clcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_N1x4.cluster0	Cluster_ARM_Neoverse-N1	ARM Neoverse-N1 Cluster CT model.
FVP_Base_Neoverse_N1x4.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_Neoverse_N1x4.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.bp.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_Neoverse_N1x4.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x4.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.cluster0.cpu2.l1icache	PVCache	PV Cache.
FVP_Base_Neoverse_N1x4.bp.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.virtio_net_1_abeller	<i>Labeler</i>	-
FVP_Base_Neoverse_N1x4.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu3.1_l1cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_Neoverse_N1x4.bp.hdled0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x4.cluster0.cpu2	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x4	FVP_Base_Neoverse_N1x4	Base Platform Compute Subsystem for ARMNeoverseN1x4CT.
FVP_Base_Neoverse_N1x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_Neoverse_N1x4.cluster0.cpu3.1_l1cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.smsc_91c11_11	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_Neoverse_N1x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_Neoverse_N1x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_Neoverse_N1x4.cluster0.cpu0.i_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_Neoverse_N1x4.bp.hdled0.time.r.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_Neoverse_N1x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_Neoverse_N1x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_Neoverse_N1x4.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_Neoverse_N1x4.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_N1x4.bp.virtiop9dev.ice_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x4.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_Neoverse_N1x4.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_Neoverse_N1x4.bp.dummy_C_F	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_Neoverse_N1x4.bp.virtioblock_device_labeller	Labeller	-
FVP_Base_Neoverse_N1x4.dapmemlogger	PVBusLogger	Bus Logger.
FVP_Base_Neoverse_N1x4.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_Neoverse_N1x4.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.bp.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_Base_Neoverse_N1x4.bp.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_N1x4.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_Base_Neoverse_N1x4.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x4.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_Neoverse_N1x4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivide is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.cluster0_labeller	Labeller	-
FVP_Base_Neoverse_N1x4.cci400	CC1400	Cache Coherent Interconnect for AXI4 ACE.
FVP_Base_Neoverse_N1x4.bp.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_Neoverse_N1x4.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_Neoverse_N1x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_Neoverse_N1x4.bp.virtioblock device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_Base_Neoverse_N1x4.cluster0.cpu1.i tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_Neoverse_N1x4.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x4.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x4.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x4.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_Neoverse_N1x4.bp.trusted_wat chdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_Neoverse_N1x4.bp.clock24M Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_Neoverse_N1x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_Base_Neoverse_N1x4.bp.hdled0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_Neoverse_N1x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.clock35M Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.cluster0.cpu0.1 2cache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 3-67 FVP_Base_Neoverse-N1x4 instances (continued)

Name	Type	Description
FVP_Base_Neoverse_N1x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.cluster0.cpu3	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x4.cluster0.cpu0	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x4.cluster0.cpu1	ARM_Neoverse-N1	ARM Neoverse-N1 CT model.
FVP_Base_Neoverse_N1x4.bp.hdled0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_Neoverse_N1x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_Base_Neoverse_N1x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_Neoverse_N1x4.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_Neoverse_N1x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_Base_Neoverse_N1x4.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.hdled0_labeller	<i>Labeller</i>	-
FVP_Base_Neoverse_N1x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_Neoverse_N1x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

3.68 FVP_Base_RevC-2xAEMv8A

FVP_Base_RevC-2xAEMv8A contains the following instances:

Table 3-68 FVP_Base_RevC-2xAEMv8A instances

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce0.incoming_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd.cd.pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_RevC_2xAEMv8A.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.bp.ve_sysregs	VE_SysRegs	-
FVP_Base_RevC_2xAEMv8A.bp.tzc_400	TZC_400	TrustZone Address Space Controller.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u3	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.clock24_MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u0	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.reset_or	OrGate	Or Gate.
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce1.to_client_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.clockCL_CD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce1.msix_pba_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.bp.ps2keyb oard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_RevC_2xAEMv8A.bp.sp810_s ysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.sp810_s ysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.sp810_s ysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.sp810_s ysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.dapmemlog ger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.clockdivide r1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.clockdivide r0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci.pcidevi ce0.dmalogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.tbu0_pr e_smmu_logger	<i>PVBusLogger</i>	Bus Logger.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.pci.pci_smuv3_msirewriter	<i>MSIRewriter</i>	Recognise writes to the GITS_TRANSLATER register and rewrite them to go to the GITS_TRANSLATE64R register. The DeviceID is expected to be in the bottom 32 bits of ExtendedID of the transaction. Debug transactions and reads are not rewritten. This component can also, optionally, apply a 16 bit 'label' to the top 16 bits of the MasterID in the same way that the Labeller component does.
FVP_Base_RevC_2xAEMv8A.bp.trusted_key_storage	<i>RootKeyStorage</i>	Trusted Root-Key Storage unit.
FVP_Base_RevC_2xAEMv8A.pci.pcidevice1.lost_transactions_to_pcie	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_Base_RevC_2xAEMv8A.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_RevC_2xAEMv8A.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_RevC_2xAEMv8A.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_RevC_2xAEMv8A.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu1	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.nontrust_edrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_RevC_2xAEMv8A.pci.pci_smuv3.mmu	<i>SMMUv3AEM</i>	SMMUv3 AEM.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu3.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_RevC_2xAEMv8A.pci.pcidevice1.lost_mastered_transactions	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_Base_RevC_2xAEMv8A.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_RevC_2xAEMv8A.pci.pcidevice0.lost_mastered_transactions	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_Base_RevC_2xAEMv8A.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.cluster1	Cluster_ARMAEMv8-A_MP	ARMAEMv8-A Cluster CT model.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.cluster0	Cluster_ARMAEMv8-A_MP	ARMAEMv8-A Cluster CT model.
FVP_Base_RevC_2xAEMv8A.bp.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_Base_RevC_2xAEMv8A.bp.virtioblockdevice_labeller	Labeler	-
FVP_Base_RevC_2xAEMv8A.cluster0.cpu2.l1icache	PVCache	PV Cache.
FVP_Base_RevC_2xAEMv8A.pci.pcidevice1.incoming_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pci.buslogger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.pcidevice0.msix_table_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pci.pcidevice.to_client_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.pcidevice1	PCIDevice	PCI Wrapper for memory mapped components.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu3.l1icache	PVCache	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.secureflashloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu0.l1icache	PVCache	PV Cache.
FVP_Base_RevC_2xAEMv8A.cluster0.l2_cache	PVCache	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0_labeller	Labeler	-
FVP_Base_RevC_2xAEMv8A.bp.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_RevC_2xAEMv8A.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pc_i.pcidevice.lost_mastered_transactions	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_RevC_2xAEMv8A.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_RevC_2xAEMv8A.bp.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u0.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.pl041_aci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd_labeller	<i>Labeller</i>	-
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_Base_RevC_2xAEMv8A.pci.pvbus2_pci.devicelogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.pcivirtioblockdevice0	<i>VirtioPCIBlockDevice</i>	virtio PCI block device.
FVP_Base_RevC_2xAEMv8A.pci.pcivirtioblockdevice1	<i>VirtioPCIBlockDevice</i>	virtio PCI block device.
FVP_Base_RevC_2xAEMv8A.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u1.itlb	TlbCadi	TLB - instruction, data or unified.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_RevC_2xAEMv8A.cluster0.cpu1	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.dram_aliases_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_RevC_2xAEMv8A.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu1.tlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_Base_RevC_2xAEMv8A.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pci	PCIDevice	PCI Wrapper for memory mapped components.
FVP_Base_RevC_2xAEMv8A.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.cluster0_labeler	<i>Labeler</i>	-
FVP_Base_RevC_2xAEMv8A.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.pl111_cd.pl11x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_Base_RevC_2xAEMv8A.cluster1.cpu2.l1dcache	<i>PVCache</i>	PV Cache.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.pci.pcidevices1.dmalogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pcis1.pcidevice.msix_pba_logger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_Base_RevC_2xAEMv8A.pci.smmulogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.cci550	<i>CC1550</i>	This is a cache coherent interconnect.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.pci.pcidevices1.msix_table_logger	<i>PVBusLogger</i>	Bus Logger.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pc_i.pcidevice.lost_transactions_to_pcie	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_Base_RevC_2xAEMv8A.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_Base_RevC_2xAEMv8A.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_RevC_2xAEMv8A.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_Base_RevC_2xAEMv8A.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u2	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.gic_distributor	<i>GIC_IRI</i>	GIC Interrupt Redistribution Infrastructure component.
FVP_Base_RevC_2xAEMv8A.bp.virtiop9_device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u0	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u2	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pc_i.pcidevice.dmalogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u3	ARMAEMv8-A_MP	ARMAEMv8-A MP CT model.
FVP_Base_RevC_2xAEMv8A.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_RevC_2xAEMv8A.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_Base_RevC_2xAEMv8A.bp.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_Base_RevC_2xAEMv8A.bp.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_Base_RevC_2xAEMv8A.cluster1_labeller	<i>Labeller</i>	-
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce0.msix_pba_logger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_Base_RevC_2xAEMv8A.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_Base_RevC_2xAEMv8A.bp.clock30_0MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_Base_RevC_2xAEMv8A.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce0.lost_transactions_to_pcie	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_Base_RevC_2xAEMv8A.pci.pvbus2_pci	PVBus2PCI	PVBus to PCI Bridge.

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.cluster0.cp_u1.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.clock10_0Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pc_i.ahci	<i>AHCI_SATA</i>	AHCI controller with attached SATA disks and PCIe interface.
FVP_Base_RevC_2xAEMv8A.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_Base_RevC_2xAEMv8A.pci.pvbus2_pci.cfglogger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.pl111_lcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_Base_RevC_2xAEMv8A.cluster1.cp_u3.l1icache	<i>PVCache</i>	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.clock35_MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.virtiop9_device_labeller	<i>Labeller</i>	-
FVP_Base_RevC_2xAEMv8A.pci.ahci_pc_i.pcidevice.msix_table_logger	<i>PVBusLogger</i>	Bus Logger.
FVP_Base_RevC_2xAEMv8A.pci.pcidevi_ce0	PCIDevice	PCI Wrapper for memory mapped components.
FVP_Base_RevC_2xAEMv8A.bp.virtio_net_labeller	<i>Labeller</i>	-

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A	FVP_Base_RevC_2xAEMv8A	Base Platform Compute Subsystem for ARMAEMv8AMPCT and ARMAEMv8AMPCT.
FVP_Base_RevC_2xAEMv8A.pci.pvbus2_pci.dmalogger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_Base_RevC_2xAEMv8A.pci.pcidevice0.to_client_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci	BasePlatformPCIRevC	PCI addon for the Base Platform.
FVP_Base_RevC_2xAEMv8A.cluster1.cpu2.ll1icache	PVCache	PV Cache.
FVP_Base_RevC_2xAEMv8A.bp.clock50_Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pci	AHCI_PCI	-
FVP_Base_RevC_2xAEMv8A.bp.generic_watchdog	MemoryMappedGenericWatchdog	ARM Generic Watchdog.
FVP_Base_RevC_2xAEMv8A.bp.clock32_KHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.pci.ahci_pcii.pcidevice.incoming_memory_logger	PVBusLogger	Bus Logger.
FVP_Base_RevC_2xAEMv8A.bp.nontrust_edromloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_Base_RevC_2xAEMv8A.bp.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_Base_RevC_2xAEMv8A.pci.pcismmuv3_smuv3	SMMUv3_FOR_PCIE	System MMUv3 configured for PCI-E Sub-system.
FVP_Base_RevC_2xAEMv8A.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 3-68 FVP_Base_RevC-2xAEMv8A instances (continued)

Name	Type	Description
FVP_Base_RevC_2xAEMv8A.bp.pl050_k_mi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_Base_RevC_2xAEMv8A.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_Base_RevC_2xAEMv8A.bp.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_Base_RevC_2xAEMv8A.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Chapter 4

BaseR platform FVPs

This chapter lists the BaseR Platform FVPs and the components in them.

It contains the following sections:

- [*4.1 FVP_BaseR_Cortex-R52x1* on page 4-652.](#)
- [*4.2 FVP_BaseR_Cortex-R52x2* on page 4-661.](#)
- [*4.3 FVP_BaseR_Cortex-R52x4* on page 4-670.](#)

4.1 FVP_BaseR_Cortex-R52x1

FVP_BaseR_Cortex-R52x1 contains the following instances:

Table 4-1 FVP_BaseR_Cortex-R52x1 instances

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x1.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_BaseR_Cortex_R52x1.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd.pl11x_cled.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x1.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_BaseR_Cortex_R52x1.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x1.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x1.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_BaseR_Cortex_R52x1.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_BaseR_Cortex_R52x1.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1	FVP_BaseR_Cortex_R52x1	Base Platform Compute Subsystem for ARM Cortex R52x1 CT.
FVP_BaseR_Cortex_R52x1.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_BaseR_Cortex_R52x1.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x1.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.trusted_watchdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x1.bp.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.hdlcd0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x1.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.nontrustedrom	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x1.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x1.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x1.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_BaseR_Cortex_R52x1.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x1.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_BaseR_Cortex_R52x1.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.virtiop9device_labeler	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x1.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x1.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_BaseR_Cortex_R52x1.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_BaseR_Cortex_R52x1.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_BaseR_Cortex_R52x1.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x1.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_BaseR_Cortex_R52x1.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x1.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_BaseR_Cortex_R52x1.bp.smsc_91c11	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_BaseR_Cortex_R52x1.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x1.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x1.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x1.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x1.cluster0_labeler	<i>Labeler</i>	-

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_BaseR_Cortex_R52x1.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_BaseR_Cortex_R52x1.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x1.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_BaseR_Cortex_R52x1.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_BaseR_Cortex_R52x1.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_BaseR_Cortex_R52x1.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x1.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.hdlcd0_labeller	<i>Labeller</i>	-
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_BaseR_Cortex_R52x1.cluster0.cpu0	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x1.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.clock32KH z	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.Timer_0_1. clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.Timer_0_1. clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.pl011_uart 0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.virtioblock device_labeller	<i>Labeller</i>	-
FVP_BaseR_Cortex_R52x1.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd. pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_BaseR_Cortex_R52x1.cluster0.gic_ir i	<i>gic_iri</i>	GIC IRI internal to cluster.
FVP_BaseR_Cortex_R52x1.bp.virtioblock device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_BaseR_Cortex_R52x1.bp.pl011_uart 2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x1.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_BaseR_Cortex_R52x1.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x1.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x1.flash_ram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.cluster0.cpu0.1_l1cache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x1.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_BaseR_Cortex_R52x1.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_BaseR_Cortex_R52x1.bp.dummy_C_F	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_BaseR_Cortex_R52x1.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.ve_sysregs	VE_SysRegs	-
FVP_BaseR_Cortex_R52x1.bp.pl011_uart_3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.pl011_uart_3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x1.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x1.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_BaseR_Cortex_R52x1.bp.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_BaseR_Cortex_R52x1.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_BaseR_Cortex_R52x1.dapmemlogger	PVBusLogger	Bus Logger.
FVP_BaseR_Cortex_R52x1.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.tzc_400	TZC_400	TrustZone Address Space Controller.
FVP_BaseR_Cortex_R52x1.bp.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x1.bp.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x1.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_BaseR_Cortex_R52x1.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x1.bp.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x1.bp.mmc	MMC	Generic Multimedia Card.
FVP_BaseR_Cortex_R52x1.bp.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.hdlcd0.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x1.bp.flashloader_0	FlashLoader	A device that can preload a gzipped image into flash at startup.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.flashloader_1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x1.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x1.bp.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_BaseR_Cortex_R52x1.bp.pl011_uart_2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x1.bp.pl011_uart_1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x1.bp.pl011_uart_0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x1.bp.pl050_kmi_0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.virtio_net_1_abeller	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x1.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 4-1 FVP_BaseR_Cortex-R52x1 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x1.bp.sp810_sysctr.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x1.cluster0	ARM_CortexR52	ARM CortexR52 MP CT model.

4.2 FVP_BaseR_Cortex-R52x2

FVP_BaseR_Cortex-R52x2 contains the following instances:

Table 4-2 FVP_BaseR_Cortex-R52x2 instances

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.secureflash	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x2.bp.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.secureSRA_M	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.virtiop9dev_ice_labeller	Labeller	-
FVP_BaseR_Cortex_R52x2.bp.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_BaseR_Cortex_R52x2.bp.smsc_91c11	SMSC_91C11	SMSC 91C11 ethernet controller.
FVP_BaseR_Cortex_R52x2.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x2.bp.ap_refclk	MemoryMappedGenericTimer	ARM Generic Timer.
FVP_BaseR_Cortex_R52x2.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_BaseR_Cortex_R52x2.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_BaseR_Cortex_R52x2.bp.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.flash_ram0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2	FVP_BaseR_Cortex_R52x2	Base Platform Compute Subsystem for ARM Cortex R52x2CT.
FVP_BaseR_Cortex_R52x2.bp.virtioblock_device_labeller	Labeller	-
FVP_BaseR_Cortex_R52x2.bp.Timer_2_3_clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.Timer_2_3_clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x2.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x2.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_BaseR_Cortex_R52x2.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_BaseR_Cortex_R52x2.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.
FVP_BaseR_Cortex_R52x2.cluster0.cpu0.1.dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x2.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.pl050_kmi_1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.secureflash_loader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x2.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_BaseR_Cortex_R52x2.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x2.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd_4	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x2.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_BaseR_Cortex_R52x2.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x2.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x2.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x2.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_BaseR_Cortex_R52x2.cluster0	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x2.bp.virtio_net_1_abeller	<i>Labeler</i>	-

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.hlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_BaseR_Cortex_R52x2.bp.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x2.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_BaseR_Cortex_R52x2.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x2.bp.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x2.bp.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x2.bp.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_BaseR_Cortex_R52x2.bp.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_BaseR_Cortex_R52x2.bp.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x2.bp.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x2.bp.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.cluster0.cpu0	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x2.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.cluster0_labeller	Labeler	-
FVP_BaseR_Cortex_R52x2.bp.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x2.bp.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x2.bp.pl031_RTC	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_BaseR_Cortex_R52x2.cluster0.cpu1	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x2.bp.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x2.bp.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x2.bp.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x2.bp.trusted_rng	RandomNumberGenerator	Random Number Generator unit.
FVP_BaseR_Cortex_R52x2.bp.vis	VEVisualisation	Display window for VE using Visualisation library.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.cluster0.gic_ir_i	gic_iri	GIC IRI internal to cluster.
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x2.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_BaseR_Cortex_R52x2.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x2.bp.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x2.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x2.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x2.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x2.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_BaseR_Cortex_R52x2.cluster0.cpu0.1icache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x2.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_BaseR_Cortex_R52x2.bp.dummy_C_F	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.ps2keyboar d	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_BaseR_Cortex_R52x2.bp.hdlcd0_labeller	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x2.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_BaseR_Cortex_R52x2.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x2.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_BaseR_Cortex_R52x2.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_BaseR_Cortex_R52x2.cluster0.cpu1.1dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x2.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x2.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.virtioblock_device	<i>VirtioBlockDevice</i>	virtio block device.
FVP_BaseR_Cortex_R52x2.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_BaseR_Cortex_R52x2.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x2.bp.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.hlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x2.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_BaseR_Cortex_R52x2.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x2.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x2.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x2.bp.ve_sysregs	VE_SysRegs	-
FVP_BaseR_Cortex_R52x2.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x2.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 4-2 FVP_BaseR_Cortex-R52x2 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x2.cluster0.cpu1.1.l1icache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x2.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_BaseR_Cortex_R52x2.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_BaseR_Cortex_R52x2.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x2.bp.audioout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.

4.3 FVP_BaseR_Cortex-R52x4

FVP_BaseR_Cortex-R52x4 contains the following instances:

Table 4-3 FVP_BaseR_Cortex-R52x4 instances

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_BaseR_Cortex_R52x4.bp.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x4.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_BaseR_Cortex_R52x4.bp.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.cluster0.cpu0.1licache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.bp.ap_refclk	<i>MemoryMappedGenericTimer</i>	ARM Generic Timer.
FVP_BaseR_Cortex_R52x4.cluster0.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.bp.hdlcd0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x4.bp.hdlcd0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x4.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_BaseR_Cortex_R52x4.bp.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4	FVP_BaseR_Cortex_R52x4	Base Platform Compute Subsystem for ARM Cortex R52x4 CT.
FVP_BaseR_Cortex_R52x4.bp.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.nontrustedrom	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x4.bp	BasePlatformPeripherals	Peripherals and address map for the Base Platform.
FVP_BaseR_Cortex_R52x4.bp.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_BaseR_Cortex_R52x4.bp.tzc_400	<i>TZC_400</i>	TrustZone Address Space Controller.
FVP_BaseR_Cortex_R52x4.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.dram_alias_warning	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_BaseR_Cortex_R52x4.bp.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.dapmemlogger	<i>PVBusLogger</i>	Bus Logger.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.cluster0.gic_ir_i	gic_iri	GIC IRI internal to cluster.
FVP_BaseR_Cortex_R52x4.bp.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_BaseR_Cortex_R52x4.bp.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_BaseR_Cortex_R52x4.cluster0.cpu0	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x4.bp.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_BaseR_Cortex_R52x4.bp.virtio_net_1_abeller	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x4.bp.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_BaseR_Cortex_R52x4.bp.flashloader_1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x4.bp.flashloader_0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x4.bp.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_BaseR_Cortex_R52x4.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.virtioblock_device	<i>VirtioBlockDevice</i>	virtio block device.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.hlcd0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x4.bp.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd_labeller	<i>Labeller</i>	-
FVP_BaseR_Cortex_R52x4.bp.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x4.bp.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x4.bp.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x4.bp.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_BaseR_Cortex_R52x4.pctl	<i>Base_PowerController</i>	Base Platforms Power Controller.
FVP_BaseR_Cortex_R52x4.cluster0.cpu3.1_1dcache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.cluster0.cpu3.1_1icache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.bp.refcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_BaseR_Cortex_R52x4.bp.nontrustedromloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x4.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.flash_ram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.clock32KHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.elfloader	<i>ElfLoader</i>	ELF loader component.
FVP_BaseR_Cortex_R52x4.bp.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x4.bp.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_BaseR_Cortex_R52x4.bp.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.secureflashloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_BaseR_Cortex_R52x4.bp.trusted_rng	<i>RandomNumberGenerator</i>	Random Number Generator unit.
FVP_BaseR_Cortex_R52x4.bp.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_BaseR_Cortex_R52x4.bp.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x4.bp.ve_sysregs	VE_SysRegs	-

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.smsc_91c11	SMS_C_91C11	SMSC 91C111 ethernet controller.
FVP_BaseR_Cortex_R52x4.bp.clock300MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x4.bp.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_BaseR_Cortex_R52x4.bp.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_BaseR_Cortex_R52x4.bp.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_BaseR_Cortex_R52x4.bp.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_BaseR_Cortex_R52x4.bp.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.hdlcd0_labeler	Labeler	-
FVP_BaseR_Cortex_R52x4.bp.trusted_key_storage	RootKeyStorage	Trusted Root-Key Storage unit.
FVP_BaseR_Cortex_R52x4.bp.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_BaseR_Cortex_R52x4.bp.ps2keyboar_d	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.trusted_watchdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_BaseR_Cortex_R52x4.bp.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_BaseR_Cortex_R52x4.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd.pl11x_c lcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x4.bp.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.hdlcd0	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_BaseR_Cortex_R52x4.bp.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.bp.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.bp.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_BaseR_Cortex_R52x4.bp.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x4.bp.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x4.bp.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x4.bp.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_BaseR_Cortex_R52x4.cluster0.cpu0.1.l1cache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.bp.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_BaseR_Cortex_R52x4.bp.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.cluster0.cpu2.1.l1cache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.bp.hdlcd0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_BaseR_Cortex_R52x4.cluster0.cpu3	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_BaseR_Cortex_R52x4.bp.reset_or	<i>OrGate</i>	Or Gate.
FVP_BaseR_Cortex_R52x4.bp.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_BaseR_Cortex_R52x4.bp.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_BaseR_Cortex_R52x4.bp.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.clockdivider0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_BaseR_Cortex_R52x4.cluster0	ARM_CortexR52	ARM CortexR52 MP CT model.

Table 4-3 FVP_BaseR_Cortex-R52x4 instances (continued)

Name	Type	Description
FVP_BaseR_Cortex_R52x4.cluster0.cpu1.1_l1icache	<i>PVCache</i>	PV Cache.
FVP_BaseR_Cortex_R52x4.cluster0.cpu3.i_tlb	TlbCadi	TLB - instruction, data or unified.
FVP_BaseR_Cortex_R52x4.bp.secureflash	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_BaseR_Cortex_R52x4.bp.virtiop9dev_ice_labeler	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x4.bp.trusted_nv_counter	<i>NonVolatileCounter</i>	Trusted Non-Volatile Counter unit.
FVP_BaseR_Cortex_R52x4.bp.generic_watchdog	<i>MemoryMappedGenericWatchdog</i>	ARM Generic Watchdog.
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x4.bp.virtioblock_device_labeler	<i>Labeler</i>	-
FVP_BaseR_Cortex_R52x4.bp.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_BaseR_Cortex_R52x4.cluster0.cpu1	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x4.cluster0.cpu2	ARM_CortexR52	ARM CortexR52 MP CT model.
FVP_BaseR_Cortex_R52x4.bp.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_BaseR_Cortex_R52x4.bp.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_BaseR_Cortex_R52x4.cluster0_labeler	<i>Labeler</i>	-

Chapter 5

VE Platform FVPs

This chapter lists the VE Platform FVPs and the components in them.

It contains the following sections:

- [5.1 FVP_VE_Cortex-A15x1](#) on page 5-681.
- [5.2 FVP_VE_Cortex-A15x1-A7x1](#) on page 5-689.
- [5.3 FVP_VE_Cortex-A15x2](#) on page 5-698.
- [5.4 FVP_VE_Cortex-A15x2-A7x2](#) on page 5-706.
- [5.5 FVP_VE_Cortex-A15x4](#) on page 5-715.
- [5.6 FVP_VE_Cortex-A15x4-A7x4](#) on page 5-723.
- [5.7 FVP_VE_Cortex-A17x1](#) on page 5-734.
- [5.8 FVP_VE_Cortex-A17x1-A7x1](#) on page 5-742.
- [5.9 FVP_VE_Cortex-A17x2](#) on page 5-751.
- [5.10 FVP_VE_Cortex-A17x4](#) on page 5-759.
- [5.11 FVP_VE_Cortex-A17x4-A7x4](#) on page 5-768.
- [5.12 FVP_VE_Cortex-A5x1](#) on page 5-778.
- [5.13 FVP_VE_Cortex-A5x2](#) on page 5-786.
- [5.14 FVP_VE_Cortex-A5x4](#) on page 5-794.
- [5.15 FVP_VE_Cortex-A7x1](#) on page 5-803.
- [5.16 FVP_VE_Cortex-A7x2](#) on page 5-811.
- [5.17 FVP_VE_Cortex-A7x4](#) on page 5-819.
- [5.18 FVP_VE_Cortex-A9x1](#) on page 5-828.
- [5.19 FVP_VE_Cortex-A9x2](#) on page 5-836.
- [5.20 FVP_VE_Cortex-A9x4](#) on page 5-844.
- [5.21 FVP_VE_Cortex-R4](#) on page 5-853.
- [5.22 FVP_VE_Cortex-R5x1](#) on page 5-860.
- [5.23 FVP_VE_Cortex-R5x2](#) on page 5-868.

- [5.24 FVP_VE_Cortex-R7x1 on page 5-875.](#)
- [5.25 FVP_VE_Cortex-R7x2 on page 5-882.](#)
- [5.26 FVP_VE_Cortex-R8x1 on page 5-889.](#)
- [5.27 FVP_VE_Cortex-R8x2 on page 5-896.](#)
- [5.28 FVP_VE_Cortex-R8x4 on page 5-903.](#)

5.1 FVP_VE_Cortex-A15x1

FVP_VE_Cortex-A15x1 contains the following instances:

Table 5-1 FVP_VE_Cortex-A15x1 instances

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.cluster.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x1.motherboard.telnet_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1.motherboard.telnet_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1.motherboard.telnet_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1.motherboard.telnet_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1.motherboard.sp8_10_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.pl11_1_cled.pl11x_cled.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1.motherboard.sp8_10_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x1.motherboard.sp8_10_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.daughterboard.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.pl04_1_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x1.daughterboard.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.daughterboard.no_nsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x1.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.daughterboard.ve_dcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x1.daughterboard.hd_lcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x1.motherboard.mmcc	MMC	Generic Multimedia Card.
FVP_VE_Cortex_A15x1.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x1.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x1.motherboard.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1.daughterboard.hd lcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1.motherboard.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A15x1.motherboard.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.cluster.l2_cache	PVCache	PV Cache.
FVP_VE_Cortex_A15x1.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1.cluster	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.
FVP_VE_Cortex_A15x1.motherboard.dummy_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x1.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A15x1.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A15x1.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x1.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x1.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x1.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.daughterboard.hd lcd	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x1.motherboard.pl18_0_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x1.motherboard.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x1.motherboard.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1.motherboard.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1.daughterboard.hdclock.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x1.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1.motherboard.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.pl11_1_cled.pl11x_cled.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x1.daughterboard.secureROloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1.motherboard.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1.motherboard.ps2_keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1.cluster.cpu0.11icache	PVCache	PV Cache.
FVP_VE_Cortex_A15x1.motherboard.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x1.daughterboard.int_router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x1.motherboard.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x1.globalcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x1.daughterboard.hd_lcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x1.motherboard.pl05_0_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.daughterboard.exclusive_monitor	PVBuseExclusiveMonitor	Global exclusive monitor.
FVP_VE_Cortex_A15x1.motherboard.virtioP9device	VirtioP9Device	virtio P9 server.
FVP_VE_Cortex_A15x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x1.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-1 FVP_VE_Cortex-A15x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1	FVP_VE_Cortex_A15x1	Top level component of the Cortex_A15x1 Versatile Express inspired model.
FVP_VE_Cortex_A15x1.motherboard.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x1.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x1.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x1.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1.motherboard.pl111_1_cled.pl111x_cled.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

5.2 FVP_VE_Cortex-A15x1-A7x1

FVP_VE_Cortex-A15x1-A7x1 contains the following instances:

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.daughterboard.secureROloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1_A7x1.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl111_cldc.pl11x_cldc.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x1_A7x1.motherboard.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x1_A7x1.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x1_A7x1.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1_A7x1.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1_A7x1.motherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1_A7x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl111_cled.pl11x_cled.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.coretile.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.coretile.v7_vgic	<i>v7_VGIC</i>	System VGIC architecture version v7.
FVP_VE_Cortex_A15x1_A7x1.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.hdlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.ps2keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x1_A7x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A15x1_A7x1.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x1_A7x1.daughterboard.nonsecure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.cpu0.lldcache	PVCache	PV Cache.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x1_A7x1.motherboard.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.coretile	ARM_Cortex_A15x1_A7x1_CT	Dual cluster ARM Cortex-A15x1 and ARM Cortex-A7x1 Core Tile.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x1_A7x1.motherboard.virtiop9device	VirtioP9Device	virtio P9 server.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.hdlcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x1_A7x1.daughterboard.hdlcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x1_A7x1.coretile.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A15x1_A7x1.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x1_A7x1.coretile.dualclustersystemconfigurationblock	<i>DualClusterSystemConfigurationBlock</i>	Dual Cluster System Configuration Block.
FVP_VE_Cortex_A15x1_A7x1.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard终端3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1_A7x1.motherboard终端0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1_A7x1.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.cpu0.ll1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x1_A7x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1_A7x1.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x1_A7x1.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x1_A7x1.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A15x1_A7x1.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.coretile.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x1_A7x1	FVP_VE_Cortex_A15x1_A7x1	Top level component of the Cortex A15x1 A7x1 Versatile Express inspired model.
FVP_VE_Cortex_A15x1_A7x1.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x1_A7x1.daughterboard.hlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x1_A7x1.motherboa rd.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-2 FVP_VE_Cortex-A15x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x1_A7x1.coretile.globalconcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x1_A7x1.coretile.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.secureROM	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x1_A7x1.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x1_A7x1.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x1_A7x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x1_A7x1.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x1_A7x1.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.3 FVP_VE_Cortex-A15x2

FVP_VE_Cortex-A15x2 contains the following instances:

Table 5-3 FVP_VE_Cortex-A15x2 instances

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2.daughterboard.hdlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x2.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x2.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A15x2.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2.motherboard.dummy_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.hdlcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2.daughterboard.int_router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x2.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x2.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x2.motherboard.pl11_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2.motherboard.virtualblockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A15x2.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2.motherboard.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2.globalcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.pl11_1_clcd.pl11x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x2.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x2.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x2.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x2.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.mmcc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A15x2.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x2.cluster.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2.daughterboard.no_nsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x2.cluster.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2.motherboard.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x2.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.daughterboard.hd_lcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x2.motherboard.sp8_05_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x2.daughterboard.ve_dcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x2.cluster.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x2.cluster.cpu1	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x2.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x2.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x2.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A15x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x2.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.cloc_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A15x2.motherboard.pl03_1_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A15x2.motherboard.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.daughterboard.hd_lcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2.motherboard.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.cluster	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.
FVP_VE_Cortex_A15x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-3 FVP_VE_Cortex-A15x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2.motherboard.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A15x2.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2.motherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x2.cluster.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A15x2.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2	FVP_VE_Cortex_A15x2	Top level component of the Cortex_A15x2 Versatile Express inspired model.
FVP_VE_Cortex_A15x2.motherboard.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x2.motherboard.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x2.motherboard.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

5.4 FVP_VE_Cortex-A15x2-A7x2

FVP_VE_Cortex-A15x2-A7x2 contains the following instances:

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.coretile.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2_A7x2.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.hdled.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2_A7x2.motherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard终端_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2_A7x2.coretile.globalscounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.secureROM	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2_A7x2.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x2_A7x2.coretile.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.motherboard.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.coretile.du alclustersystemconfigurationblock	<i>DualClusterSystemC onfigurationBlock</i>	Dual Cluster System Configuration Block.
FVP_VE_Cortex_A15x2_A7x2.daughterb oard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.daughterb oard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.coretile.cl uster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.motherboa rd.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu0.011dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2_A7x2.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.coretile	ARM_Cortex_A15x2_A7x2_CT	Dual cluster ARM Cortex-A15x2 and ARM Cortex-A7x2 Core Tile.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.hdlcd	<i>PL370_HDLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x2_A7x2.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x2_A7x2.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.cpu0.011icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x2_A7x2.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x2_A7x2.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x2_A7x2.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.daughterboard.nonsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x2_A7x2	FVP_VE_Cortex_A15x2_A7x2	Top level component of the Cortex A15x2 A7x2 Versatile Express inspired model.
FVP_VE_Cortex_A15x2_A7x2.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2_A7x2.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x2_A7x2.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu0.l1icache	<i>PVCache</i>	PV Cache.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.hdlcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_cldc.pl11x_cldc.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x2_A7x2.coretile.v7_vgic	<i>v7_VGIC</i>	System VGIC architecture version v7.
FVP_VE_Cortex_A15x2_A7x2.motherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.coretile.clock0.cpu1	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x2_A7x2.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x2_A7x2.coretile.clock1.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A15x2_A7x2.coretile.clock1.cpu1	ARM_Cortex-A7	ARM Cortex-A7 CT model.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2_A7x2.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x2_A7x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2_A7x2.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2_A7x2.motherboard.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x2_A7x2.coretile.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.hdlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x2_A7x2.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x2_A7x2.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x2_A7x2.coretile.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 5-4 FVP_VE_Cortex-A15x2-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x2_A7x2.daughterboard.hlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x2_A7x2.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x2_A7x2.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x2_A7x2.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.5 FVP_VE_Cortex-A15x4

FVP_VE_Cortex-A15x4 contains the following instances:

Table 5-5 FVP_VE_Cortex-A15x4 instances

Name	Type	Description
FVP_VE_Cortex_A15x4.daughterboard.int_router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x4.motherboard.clk35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.globalcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x4.motherboard.pl05_0_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x4.motherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.mm_c	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A15x4.motherboard.clkLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.no_nsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x4.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.cluster.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.daughterboard.hd_lcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x4.daughterboard.hd_lcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x4.motherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.cloc_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x4.motherboard.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x4.cluster.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.motherboard.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.pl18_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x4.daughterboard.hlcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x4.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x4.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.motherboard.pl03_1_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A15x4.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.sp8_10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.hd_lcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x4.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.cluster.cpu2	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4.cluster.cpu3	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4.cluster.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4.cluster.cpu1	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4.motherboard.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A15x4.cluster.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.cluster.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4.motherboard.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x4.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x4.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A15x4.cluster.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4.motherboard.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4.cluster.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.cluster.cpu2.11icache	<i>PVCache</i>	PV Cache.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4.daughterboard.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x4.motherboard.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.Timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.cluster	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.
FVP_VE_Cortex_A15x4.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.motherboard.pl05_0_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x4.motherboard.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4.cluster.cpu1.11icache	PVCache	PV Cache.
FVP_VE_Cortex_A15x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x4.motherboard.telnet0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A15x4.motherboard.telnet1	TelnetTerminal	Telnet terminal interface.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.motherboard.telnet_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4.motherboard.telnet_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.motherboard.sp8_10_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A15x4.cluster.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x4.cluster.cpu3.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.motherboard.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.hlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x4.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-5 FVP_VE_Cortex-A15x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x4.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x4.motherboard.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4.cluster.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4	FVP_VE_Cortex_A15x4	Top level component of the Cortex_A15x4 Versatile Express inspired model.
FVP_VE_Cortex_A15x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A15x4.motherboard.virtioP9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A15x4.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x4.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

5.6 FVP_VE_Cortex-A15x4-A7x4

FVP_VE_Cortex-A15x4-A7x4 contains the following instances:

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x4_A7x4.coretile.dualclustersystemconfigurationblock	<i>DualClusterSystemConfigurationBlock</i>	Dual Cluster System Configuration Block.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A15x4_A7x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0	Cluster_ARM_Cortex-A15	ARM Cortex-A15 Cluster CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.hlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A15x4_A7x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.hlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A15x4_A7x4.daughterboard.nonsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4_A7x4.motherboard终端_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4_A7x4.motherboard终端_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4_A7x4.motherboard终端_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4_A7x4.motherboard终端_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu2.l1dcache	<i>PVCache</i>	PV Cache.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4_A7x4.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A15x4_A7x4.coretile.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A15x4_A7x4.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A15x4_A7x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A15x4_A7x4.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.custer0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.hdlcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x4_A7x4.coretile.custer1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A15x4_A7x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4_A7x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu2.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu2	ARM_Cortex-A7	ARM Cortex-A7 CT model.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4_A7x4.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.globalcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A15x4_A7x4.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A15x4_A7x4.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.coretile.v7_vgic	<i>v7_VGIC</i>	System VGIC architecture version v7.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A15x4_A7x4.coretile.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.smsc_91c11	<i>SMSC_91C11</i>	SMSC 91C11 ethernet controller.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4_A7x4.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4	FVP_VE_Cortex_A15x4_A7x4	Top level component of the Cortex A15x4 A7x4 Versatile Express inspired model.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu3.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A15x4_A7x4.motherboard.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A15x4_A7x4.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A15x4_A7x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu1.11dcache	<i>PVCache</i>	PV Cache.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu3	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu2	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu1	ARM_Cortex-A15	ARM Cortex-A15 CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu3.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A15x4_A7x4.coretile	ARM_Cortex_A15x4_A7x4_CT	Dual cluster ARM Cortex-A15x4 and ARM Cortex-A7x4 Core Tile.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu3.lldcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu2.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu0.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu0	ARM_Cortex-A15	ARM Cortex-A15 CT model.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A15x4_A7x4.coretile.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu1	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4_A7x4.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A15x4_A7x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A15x4_A7x4.coretile.cluster1.cpu3	ARM_Cortex-A7	ARM Cortex-A7 CT model.

Table 5-6 FVP_VE_Cortex-A15x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A15x4_A7x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A15x4_A7x4.daughterboard.hlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

5.7 FVP_VE_Cortex-A17x1

FVP_VE_Cortex-A17x1 contains the following instances:

Table 5-7 FVP_VE_Cortex-A17x1 instances

Name	Type	Description
FVP_VE_Cortex_A17x1.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x1.motherboard.cloc_k100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1.daughterboard.dram_aliased	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1.motherboard.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A17x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A17x1.globalcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A17x1.motherboard.pl180_0_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A17x1.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1.daughterboard.hlcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1.motherboard.cloc_k35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.cloc_k50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.daughterboard.hdlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A17x1.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A17x1.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x1.motherboard.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A17x1.motherboard.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A17x1.motherboard.mmcc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A17x1.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A17x1.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A17x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.motherboard.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A17x1.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A17x1.cluster	Cluster_ARM_Cortex-A17	ARM Cortex-A17 Cluster CT model.
FVP_VE_Cortex_A17x1	FVP_VE_Cortex_A17x1	Top level component of the Cortex_A17x1 Versatile Express inspired model.
FVP_VE_Cortex_A17x1.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A17x1.daughterboard.hdlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1.motherboard.pl111_1_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A17x1.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.cluster.cpu0	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x1.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.pl05_0_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x1.motherboard.pl05_0_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x1.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1.motherboard.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1.motherboard.virtioblockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A17x1.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x1.motherboard.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.pl03_1 rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A17x1.motherboard.pl05_0_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A17x1.motherboard.ps2 mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x1.gic400	GIC_400	GIC-400 Generic Interrupt Controller.
FVP_VE_Cortex_A17x1.daughterboard.no nsecure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1.motherboard.pl111_1_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1.daughterboard.int router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A17x1.motherboard.flash_h0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1.motherboard.flash_h1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1.motherboard.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A17x1.motherboard.pl111_1_clcd.pl11x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x1.motherboard.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.pl111_1_cled.pl11x_cled	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A17x1.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1.daughterboard.hdlcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x1.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A17x1.motherboard.cloc_k24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1.motherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x1.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.

Table 5-7 FVP_VE_Cortex-A17x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1.motherboard.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A17x1.cluster.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x1.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A17x1.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

5.8 FVP_VE_Cortex-A17x1-A7x1

FVP_VE_Cortex-A17x1-A7x1 contains the following instances:

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.cpu0.011icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1_A7x1.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1_A7x1.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A17x1_A7x1.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1_A7x1.coretile	ARM_Cortex_A17x1_A7x1_CT	Dual cluster ARM Cortex-A17x1 and ARM Cortex-A7x1 Core Tile.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.hdlcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.hdlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A17x1_A7x1.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.nonsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1_A7x1.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.coretile.dualclustersystemconfigurationblock	<i>DualClusterSystemConfigurationBlock</i>	Dual Cluster System Configuration Block.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0	Cluster_ARM_Cortex-A17	ARM Cortex-A17 Cluster CT model.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A17x1_A7x1.motherboard.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.v7_vgic	<i>v7_VGIC</i>	System VGIC architecture version v7.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1_A7x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A17x1_A7x1.coretile.cci400	<i>CC1400</i>	Cache Coherent Interconnect for AXI4 ACE.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A17x1_A7x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.coretile.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.cpu0	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1_A7x1.coretile.globalconcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.l2_cache	<i>PVCache</i>	PV Cache.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A17x1_A7x1.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x1_A7x1.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1_A7x1.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1_A7x1.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster1.cpu0.itlb	TLbCadi	TLB - instruction, data or unified.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1_A7x1.motherboard.vis.recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.coretile.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x1_A7x1	FVP_VE_Cortex_A17x1_A7x1	Top level component of the Cortex A17x1 A7x1 Versatile Express inspired model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.daughterboard.hlcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x1_A7x1.motherboard.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x1_A7x1.motherboard.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A17x1_A7x1.motherboard.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x1_A7x1.motherboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.smsc_91c111	SMS_C_91C111	SMS_C 91C111 ethernet controller.
FVP_VE_Cortex_A17x1_A7x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A17x1_A7x1.motherboard.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl111_clcd.pl111x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dram_aliases	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1_A7x1.motherboard.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A17x1_A7x1.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-8 FVP_VE_Cortex-A17x1-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x1_A7x1.daughterboard.hdlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

5.9 FVP_VE_Cortex-A17x2

FVP_VE_Cortex-A17x2 contains the following instances:

Table 5-9 FVP_VE_Cortex-A17x2 instances

Name	Type	Description
FVP_VE_Cortex_A17x2.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A17x2.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.daughterboard.hd_lcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x2.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x2.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x2.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A17x2.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x2.motherboard.telnet_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A17x2.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.pl111_1_cled	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A17x2.motherboard.dum_my_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.sp8_05_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A17x2.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A17x2.cluster.cpu0	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x2.cluster.cpu1.11icache	PVCache	PV Cache.
FVP_VE_Cortex_A17x2.motherboard.pl04_1_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A17x2.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.cluster.cpu0.11icache	PVCache	PV Cache.
FVP_VE_Cortex_A17x2.motherboard.mmcc	MMC	Generic Multimedia Card.
FVP_VE_Cortex_A17x2.motherboard.sp8_10_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.sp8_10_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.sp8_10_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.sp8_10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x2.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x2.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x2.daughterboard.no_nsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x2.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.pl03_1_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A17x2.motherboard.pl05_0_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x2.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A17x2.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.cloc_k100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.globalcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A17x2.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2	FVP_VE_Cortex_A17x2	Top level component of the Cortex_A17x2 Versatile Express inspired model.
FVP_VE_Cortex_A17x2.daughterboard.int_router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A17x2.motherboard.flash_h1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x2.motherboard.flash_h0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A17x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.pl111_1_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x2.cluster.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x2.motherboard.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A17x2.daughterboard.hd_lcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x2.motherboard.pl111_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x2.motherboard.pl111_1_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x2.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.daughterboard.hlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x2.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x2.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x2.gic400	<i>GIC_400</i>	GIC-400 Generic Interrupt Controller.
FVP_VE_Cortex_A17x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A17x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A17x2.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x2.daughterboard.hlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A17x2.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x2.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x2.cluster.l2_cache	<i>PVCache</i>	PV Cache.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.motherboard.cloc_kCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.cluster.cpu1	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x2.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x2.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x2.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x2.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A17x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A17x2.daughterboard.hdlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x2.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A17x2.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x2.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A17x2.cluster	Cluster_ARM_Cortex-A17	ARM Cortex-A17 Cluster CT model.
FVP_VE_Cortex_A17x2.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x2.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x2.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-9 FVP_VE_Cortex-A17x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x2.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x2.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x2.motherboard.dummy_my_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x2.motherboard.pl01_1_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.ps2_keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x2.motherboard.pl11_1_clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A17x2.daughterboard.dram_aliased	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x2.motherboard.pl05_0_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x2.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x2.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x2.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x2.motherboard.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A17x2.motherboard.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x2.motherboard.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.10 FVP_VE_Cortex-A17x4

FVP_VE_Cortex-A17x4 contains the following instances:

Table 5-10 FVP_VE_Cortex-A17x4 instances

Name	Type	Description
FVP_VE_Cortex_A17x4.motherboard.pl11_1_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4.motherboard.pl18_0_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A17x4.motherboard.pl01_1_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A17x4.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.pl11_1_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x4.motherboard.pl04_1_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A17x4.cluster.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.daughterboard.hd_lcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x4.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4.motherboard.pl03_1 rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A17x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.daughterboard.hdlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4.motherboard.Timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A17x4.motherboard.audiout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A17x4.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4.motherboard.vesysregs	<i>VE_SysRegs</i>	-
FVP_VE_Cortex_A17x4.cluster.cpu1.llcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x4.cluster.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.daughterboard.hdlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.motherboard.mm c	MMC	Generic Multimedia Card.
FVP_VE_Cortex_A17x4.daughterboard.se cureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.Tim er_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4.motherboard.Tim er_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4.motherboard.pl01 1_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.ps2 mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x4.daughterboard.se cure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4.daughterboard.no nsecure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4.motherboard.sp8 10_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A17x4.globalcounter	MemoryMappedCou nterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A17x4.motherboard.cloc k100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.cluster.cpu0.l1dc ache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.virti oblockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A17x4.cluster.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.daughterboard.sr am	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.dum my_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.motherboard.Timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.cluster.cpu1	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4	FVP_VE_Cortex_A17x4	Top level component of the Cortex_A17x4 Versatile Express inspired model.
FVP_VE_Cortex_A17x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A17x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4.cluster.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A17x4.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.motherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.gic400	<i>GIC_400</i>	GIC-400 Generic Interrupt Controller.
FVP_VE_Cortex_A17x4.motherboard.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.pl11_1_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A17x4.motherboard.pl01_1_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.motherboard.dummy_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.cluster.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.daughterboard.hlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4.cluster.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.pl05_0_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4.cluster.cpu2	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.motherboard.pl05_0_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.daughterboard.int_router	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A17x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.cluster	Cluster_ARM_Cortex-A17	ARM Cortex-A17 Cluster CT model.
FVP_VE_Cortex_A17x4.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x4.motherboard.pl05_0_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x4.motherboard.pl05_0_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x4.motherboard.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x4.motherboard.pl01_1_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4.motherboard.pl01_1_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4.motherboard.pl01_1_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A17x4.motherboard.pl11_1_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A17x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A17x4.motherboard.virtio_p9device	VirtioP9Device	virtio P9 server.
FVP_VE_Cortex_A17x4.motherboard.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.cluster.cpu3.ll1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4.motherboard.terminal_3	TelnetTerminal	Telnet terminal interface.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A17x4.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4.cluster.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.pl111_1_cldc.pl11x_cldc.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x4.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.cluster.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4.motherboard.pl111_1_cldc.pl11x_cldc.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4.cluster.cpu0	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4.cluster.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A17x4.cluster.cpu3	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.

Table 5-10 FVP_VE_Cortex-A17x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.

5.11 FVP_VE_Cortex-A17x4-A7x4

FVP_VE_Cortex-A17x4-A7x4 contains the following instances:

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.hostbridge	HostBridge	Host Socket Interface Component.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu1.l1icache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A17x4_A7x4.coretile.v7_vgic	v7_VGIC	System VGIC architecture version v7.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu2	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.secure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu1	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A17x4_A7x4.coretile.clockdivider1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu3.ll1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu3.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu0.ll1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu2.ll1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0	Cluster_ARM_Cortex-A17	ARM Cortex-A17 Cluster CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A17x4_A7x4.daughterboard.hdlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.virtioblockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4_A7x4.daughterboard.nonsecure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.coretile	ARM_Cortex_A17x4_A7x4_CT	Dual cluster ARM Cortex-A17x4 and ARM Cortex-A7x4 Core Tile.
FVP_VE_Cortex_A17x4_A7x4	FVP_VE_Cortex_A17x4_A7x4	Top level component of the Cortex A17x4 A7x4 Versatile Express inspired model.
FVP_VE_Cortex_A17x4_A7x4.coretile.globalcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu0.11icache	<i>PVCache</i>	PV Cache.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.audioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu3	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.hlcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4_A7x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A17x4_A7x4.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu3.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.l2_cache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.hlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4_A7x4.motherboard.virtiop9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A17x4_A7x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A17x4_A7x4.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu2.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.coretile.dualclustersystemconfigurationblock	<i>DualClusterSystemConfigurationBlock</i>	Dual Cluster System Configuration Block.
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu3.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4_A7x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu1	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu0	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu3	ARM_Cortex-A17	ARM Cortex-A17 CT model.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu2	ARM_Cortex-A17	ARM Cortex-A17 CT model.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4_A7x4.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.hlcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A17x4_A7x4.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4_A7x4.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu2.llicache	<i>PVCache</i>	PV Cache.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A17x4_A7x4.daughterboard.hlcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu1.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A17x4_A7x4.motherboard.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A17x4_A7x4.motherboard.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu2.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu3.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A17x4_A7x4.motherboard.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dram_aliased	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A17x4_A7x4.coretile.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.exclusive_monitor	PVBUSExclusiveMonitor	Global exclusive monitor.

Table 5-11 FVP_VE_Cortex-A17x4-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster0.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A17x4_A7x4.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A17x4_A7x4.coretile.cci400	CCI400	Cache Coherent Interconnect for AXI4 ACE.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl111_clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A17x4_A7x4.motherboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard终端_0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.Timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A17x4_A7x4.daughterboard.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A17x4_A7x4.coretile.cluster1.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A17x4_A7x4.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.12 FVP_VE_Cortex-A5x1

FVP_VE_Cortex-A5x1 contains the following instances:

Table 5-12 FVP_VE_Cortex-A5x1 instances

Name	Type	Description
FVP_VE_Cortex_A5x1.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.vis.recorder.playbackDivide	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A5x1.daughterboard.hdlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x1.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x1.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x1.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x1.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.daughterboard.hlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A5x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A5x1.motherboard.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.daughterboard.ved_cc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A5x1.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x1.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x1.motherboard.Timerr_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.Timerr_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.Timerr_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.Timerr_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.clock_50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.motherboard.vis.re_corder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A5x1.motherboard.mmci	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A5x1.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A5x1.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x1.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x1.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.daughterboard.hlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A5x1.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x1.motherboard.virtio_blockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A5x1.motherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x1.daughterboard.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.daughterboard.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A5x1.motherboard.clock_35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A5x1.motherboard.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.daughterboard.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.sp81_0_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.motherboard.Time_r_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x1.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x1.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x1.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x1.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x1.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x1.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x1.daughterboard.secureROloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A5x1.motherboard.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.virtio_p9device	VirtioP9Device	virtio P9 server.
FVP_VE_Cortex_A5x1.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x1.motherboard.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A5x1.motherboard.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x1.motherboard.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x1.motherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x1.motherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x1.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.motherboard.Time_r_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x1.motherboard.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x1.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A5x1.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x1.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x1.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x1.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x1.motherboard.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A5x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x1.motherboard.pl041_aaci	<i>PL041 AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A5x1.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.daughterboard.hdl_cd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A5x1.motherboard.Time_r_2_3	<i>SP804 Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x1.motherboard.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x1.motherboard.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x1.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A5x1.cluster.cpu0	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x1	FVP_VE_Cortex_A5x1	Top level component of the Cortex-A5x1 Versatile Express inspired model.
FVP_VE_Cortex_A5x1.cluster	Cluster_ARM_Cortex-A5MP	ARM CORTEXA5MP Cluster CT model.

Table 5-12 FVP_VE_Cortex-A5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x1.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A5x1.motherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x1.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A5x1.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A5x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x1.motherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.13 FVP_VE_Cortex-A5x2

FVP_VE_Cortex-A5x2 contains the following instances:

Table 5-13 FVP_VE_Cortex-A5x2 instances

Name	Type	Description
FVP_VE_Cortex_A5x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A5x2.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A5x2.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A5x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A5x2.motherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x2.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x2.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x2.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x2.motherboard.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A5x2.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A5x2.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A5x2.motherboard.vis.receiver	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A5x2.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A5x2.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x2.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A5x2.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A5x2.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A5x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.pl1111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x2.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.daughterboard.hdl_cd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A5x2.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x2.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.daughterboard.hdl_cd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x2.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x2.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A5x2.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A5x2.cluster	Cluster_ARM_Cortex-A5MP	ARM CORTEXA5MP Cluster CT model.
FVP_VE_Cortex_A5x2.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x2.motherboard.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A5x2.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.motherboard.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.cluster.cpu1.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x2.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x2.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x2.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x2.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x2.motherboard.vis.receiver.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x2.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x2.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x2.motherboard.flash_0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A5x2.motherboard.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.daughterboard.intr_outer	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A5x2.motherboard.Time_r_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x2.motherboard.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.daughterboard.non.secure_region	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x2.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x2.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x2.motherboard.pl111.clcd.pl111x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x2.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A5x2.cluster.cpu0.11dcache	PVCache	PV Cache.
FVP_VE_Cortex_A5x2.motherboard.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.psram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.motherboard.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.motherboard.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A5x2.daughterboard.hlcd	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A5x2.motherboard.clock_50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A5x2.daughterboard.dram_limit_8	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x2.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x2.daughterboard.dram_limit_4	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x2.motherboard.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x2.cluster.cpu1.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A5x2.motherboard.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.cluster.cpu1.l1icache	PVCache	PV Cache.
FVP_VE_Cortex_A5x2.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.daughterboard.ved_cc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A5x2.motherboard.clock_24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.cluster.cpu0	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.

Table 5-13 FVP_VE_Cortex-A5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x2.cluster.cpu1	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x2.motherboard.audio_out	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A5x2.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x2.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x2.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x2	FVP_VE_Cortex_A5x2	Top level component of the Cortex-A5x2 Versatile Express inspired model.
FVP_VE_Cortex_A5x2.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x2.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A5x2.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

5.14 FVP_VE_Cortex-A5x4

FVP_VE_Cortex-A5x4 contains the following instances:

Table 5-14 FVP_VE_Cortex-A5x4 instances

Name	Type	Description
FVP_VE_Cortex_A5x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A5x4.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x4.daughterboard.hlcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x4.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x4.daughterboard.hlcd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x4.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x4.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x4.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x4.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A5x4.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A5x4.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A5x4.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.motherboard.mmcc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A5x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A5x4.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x4.cluster.cpu3.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x4.motherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.cluster.cpu2.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.motherboard.audio_out	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A5x4.motherboard.Timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.Timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A5x4.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x4.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A5x4.daughterboard.hdl_cd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A5x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.cluster	Cluster_ARM_Cortex-A5MP	ARM CORTEXA5MP Cluster CT model.
FVP_VE_Cortex_A5x4.cluster.cpu0	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x4.cluster.cpu1	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x4.cluster.cpu2	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x4.cluster.cpu3	ARM_Cortex-A5MP	ARM CORTEXA5MP CT model.
FVP_VE_Cortex_A5x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A5x4.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x4.motherboard.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A5x4.motherboard.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A5x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A5x4.motherboard.dummy_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.cluster.cpu3.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.cluster.cpu1.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A5x4.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x4.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x4.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x4.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A5x4.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A5x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.motherboard.Timerr_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.Timerr_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A5x4.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A5x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A5x4.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.cluster.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.cluster.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x4.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A5x4.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A5x4.cluster.cpu3.l1dcache	<i>PVCache</i>	PV Cache.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.daughterboard.hdl_cd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A5x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.clock_50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A5x4.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A5x4.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A5x4.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A5x4.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A5x4.motherboard.Time_r_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x4.motherboard.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A5x4.cluster.cpu2.llicache	PVCache	PV Cache.
FVP_VE_Cortex_A5x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A5x4	FVP_VE_Cortex_A5x4	Top level component of the Cortex-A5x4 Versatile Express inspired model.
FVP_VE_Cortex_A5x4.motherboard.Time_r_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A5x4.motherboard.dum_my_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A5x4.motherboard.clock_35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.Time_r_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A5x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A5x4.daughterboard.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A5x4.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).

Table 5-14 FVP_VE_Cortex-A5x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A5x4.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A5x4.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

5.15 FVP_VE_Cortex-A7x1

FVP_VE_Cortex-A7x1 contains the following instances:

Table 5-15 FVP_VE_Cortex-A7x1 instances

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A7x1.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A7x1.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A7x1.motherboard.clock_35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A7x1.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A7x1.motherboard.pl011_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.vis.receiver.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.daughterboard.secureSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.motherboard.sp810_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A7x1.motherboard.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.Timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x1.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x1.motherboard.clock_24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.daughterboard.hdl_cd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A7x1.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A7x1.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A7x1.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x1.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x1.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.Time_r_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A7x1.daughterboard.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.virtio_blockdevice	VirtioBlockDevice	virtio block device.
FVP_VE_Cortex_A7x1.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x1.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x1.motherboard.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A7x1.motherboard.virtio_p9device	VirtioP9Device	virtio P9 server.
FVP_VE_Cortex_A7x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A7x1.motherboard.Time_r_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x1	FVP_VE_Cortex_A7x1	Top level component of the Cortex_A7x1 Versatile Express inspired model.
FVP_VE_Cortex_A7x1.daughterboard.intr_outer	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A7x1.motherboard.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.daughterboard.hdl_cd.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x1.motherboard.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A7x1.motherboard.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A7x1.motherboard.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A7x1.motherboard.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_A7x1.motherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x1.motherboard.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x1.motherboard.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x1.cluster.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x1.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x1.cluster.l2_cache	PVCache	PV Cache.
FVP_VE_Cortex_A7x1.motherboard.Timerr_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.Timerr_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.globalcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A7x1.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x1.motherboard.Timerr_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x1.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A7x1.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x1.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x1.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A7x1.motherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.motherboard.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x1.motherboard.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x1.motherboard.clock_50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x1.motherboard.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A7x1.motherboard.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A7x1.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x1.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x1.cluster	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A7x1.daughterboard.dram_aliased	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x1.daughterboard.dmc_phy	RAMDevice	RAM device, can be dynamic or static ram.

Table 5-15 FVP_VE_Cortex-A7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x1.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x1.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x1.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x1.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A7x1.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A7x1.daughterboard.hdl_cd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A7x1.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x1.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A7x1.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.

5.16 FVP_VE_Cortex-A7x2

FVP_VE_Cortex-A7x2 contains the following instances:

Table 5-16 FVP_VE_Cortex-A7x2 instances

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x2.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x2.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x2.motherboard.mmccard	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A7x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A7x2.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x2.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x2.motherboard.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A7x2.motherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.Time_r_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A7x2.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.vis.receiver.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x2.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x2.motherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x2.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x2.motherboard.clock_50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x2.cluster.cpu1.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A7x2.globalcounter	MemoryMappedCounterModule	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A7x2.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x2.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A7x2.motherboard.dum_my_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.clock_35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.cluster.cpu1.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x2.motherboard.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x2.motherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A7x2.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A7x2.daughterboard.sram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.daughterboard.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_VE_Cortex_A7x2.motherboard.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.daughterboard.hdl_cd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x2.cluster.cpu1	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x2	FVP_VE_Cortex_A7x2	Top level component of the Cortex_A7x2 Versatile Express inspired model.
FVP_VE_Cortex_A7x2.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A7x2.motherboard.audio_out	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A7x2.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x2.daughterboard.intr_outer	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A7x2.motherboard.clock_CLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.daughterboard.hdl_cd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A7x2.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x2.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x2.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x2.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x2.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x2.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A7x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x2.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A7x2.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x2.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.daughterboard.hdl_cd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x2.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x2.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x2.cluster.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x2.motherboard.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x2.motherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A7x2.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.Time_r_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x2.motherboard.sp81_0_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.sp81_0_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.sp81_0_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.Time_r_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x2.motherboard.Time_r_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x2.motherboard.Time_r_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x2.motherboard.ps2mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x2.motherboard.sp81_0_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A7x2.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x2.motherboard.dum_my_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A7x2.daughterboard.hlcd	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A7x2.cluster.cpu1.l1icache	PVCache	PV Cache.

Table 5-16 FVP_VE_Cortex-A7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x2.motherboard.pl041_aaci	PL041 AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A7x2.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A7x2.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A7x2.motherboard.vis.recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A7x2.cluster.cpu0.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A7x2.daughterboard.dram_aliased	TZSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x2.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x2.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x2.cluster	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A7x2.motherboard.hostbridge	HostBridge	Host Socket Interface Component.
FVP_VE_Cortex_A7x2.cluster.l2_cache	PVCache	PV Cache.

5.17 FVP_VE_Cortex-A7x4

FVP_VE_Cortex-A7x4 contains the following instances:

Table 5-17 FVP_VE_Cortex-A7x4 instances

Name	Type	Description
FVP_VE_Cortex_A7x4.cluster.cpu2.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.cluster.l2_cache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.cluster.cpu3.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A7x4.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x4.motherboard.mmcc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A7x4.cluster.cpu1.dtib	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A7x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A7x4.cluster.cpu3.dtib	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x4.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x4.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A7x4.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x4.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A7x4.motherboard.Time_r_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.Time_r_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.hdcd.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd.pl111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A7x4.daughterboard.ved_cc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A7x4.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A7x4.cluster.cpu0.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.cluster.cpu1.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd.pl111x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A7x4.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x4.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x4.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.cluster.cpu3.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.motherboard.sp81_0_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A7x4.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A7x4.globalcounter	<i>MemoryMappedCounterModule</i>	Memory Mapped Counter Module for Generic Timers.
FVP_VE_Cortex_A7x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.cluster.cpu1.llicache	<i>PVCache</i>	PV Cache.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A7x4.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.Time_r_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A7x4.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x4.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A7x4.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.cluster.cpu2.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.motherboard.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A7x4	FVP_VE_Cortex_A7x4	Top level component of the Cortex_A7x3 Versatile Express inspired model.
FVP_VE_Cortex_A7x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.cluster	Cluster_ARM_Cortex-A7	ARM Cortex-A7 Cluster CT model.
FVP_VE_Cortex_A7x4.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.cluster.cpu3.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A7x4.motherboard.clock_35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A7x4.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.cluster.cpu2	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x4.cluster.cpu3	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x4.cluster.cpu0	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x4.cluster.cpu1	ARM_Cortex-A7	ARM Cortex-A7 CT model.
FVP_VE_Cortex_A7x4.cluster.cpu2.itlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x4.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A7x4.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x4.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x4.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x4.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A7x4.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A7x4.daughterboard.hhdlcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x4.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x4.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A7x4.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A7x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A7x4.motherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A7x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A7x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.cluster.cpu2.dtlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A7x4.daughterboard.dram_aliased	TzSwitch	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A7x4.daughterboard.hlcd	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A7x4.motherboard.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A7x4.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.clock_50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.secureRO	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A7x4.motherboard.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.pl050_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.cluster.cpu0.dtlb	TlbCadi	TLB - instruction, data or unified.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A7x4.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A7x4.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A7x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A7x4.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.dmc	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A7x4.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-17 FVP_VE_Cortex-A7x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A7x4.motherboard.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A7x4.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

5.18 FVP_VE_Cortex-A9x1

FVP_VE_Cortex-A9x1 contains the following instances:

Table 5-18 FVP_VE_Cortex-A9x1 instances

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.audio.out	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A9x1.daughterboard.hdl_cd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x1.motherboard.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A9x1.motherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A9x1.motherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x1.motherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x1.motherboard.Time_r_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x1.motherboard.Time_r_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x1.motherboard.Time_r_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x1.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.vis.recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.daughterboard.hdl_cd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A9x1.daughterboard.ved_cc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A9x1.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x1.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.flash_1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x1.motherboard.Time_r_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.Time_r_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A9x1.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A9x1.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x1.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x1.motherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x1.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x1.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x1.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A9x1.daughterboard.hdlcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A9x1.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A9x1.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A9x1.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A9x1.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A9x1.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x1.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x1.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x1.motherboard.Tmr_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.Tmr_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x1.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A9x1.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x1.motherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A9x1.cluster.cpu0	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.Time_r_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x1.motherboard.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A9x1.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x1.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x1.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x1.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x1.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x1.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A9x1.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x1.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A9x1.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x1.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x1.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A9x1.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x1	FVP_VE_Cortex_A9x1	Top level component of the Cortex-A9x1 Versatile Express inspired model.
FVP_VE_Cortex_A9x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A9x1.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.clock_50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.daughterboard.hdl_cd	<i>PL370_HLCD</i>	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A9x1.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A9x1.cluster	Cluster_ARM_Cortex-A9MP	ARM CORTEXA9MP Cluster CT model.
FVP_VE_Cortex_A9x1.motherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.clock_35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A9x1.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x1.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A9x1.motherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-18 FVP_VE_Cortex-A9x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x1.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x1.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x1.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A9x1.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A9x1.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x1.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

5.19 FVP_VE_Cortex-A9x2

FVP_VE_Cortex-A9x2 contains the following instances:

Table 5-19 FVP_VE_Cortex-A9x2 instances

Name	Type	Description
FVP_VE_Cortex_A9x2.daughterboard.hdl_cd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x2.motherboard.pl041_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A9x2.motherboard.vram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.daughterboard.ved_cc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A9x2.motherboard.clock_100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.pl180_mci	PL180_MCI	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A9x2.motherboard.Time_r_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.Time_r_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_A9x2.motherboard.pl031_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A9x2.daughterboard.secureROloader	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x2.motherboard.virtio_p9device	VirtioP9Device	virtio P9 server.

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.cluster.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x2.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A9x2.daughterboard.dram_aliased	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x2.motherboard.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A9x2.motherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.cluster.cpu1.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x2.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x2.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.Timerr_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.Timerr_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x2.daughterboard.introuter	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A9x2.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A9x2.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x2.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x2.motherboard.clock_35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.cluster	Cluster_ARM_Cortex-A9MP	ARM CORTEXA9MP Cluster CT model.
FVP_VE_Cortex_A9x2.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x2.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.daughterboard.secureDRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.flash_1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x2.motherboard.flash_0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x2.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A9x2.motherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A9x2.daughterboard.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_VE_Cortex_A9x2.motherboard.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd.pl111x_clcd.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A9x2.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x2.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x2.daughterboard.hdl_cd.timer.timer_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A9x2.motherboard.mmcc	MMC	Generic Multimedia Card.
FVP_VE_Cortex_A9x2.motherboard.clock_50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.cluster.cpu1.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A9x2.motherboard.dummy_local_dap_rom	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.vis.receiver.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.daughterboard.hdl_cd	PL370_HDLC	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x2.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x2.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x2.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x2.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x2.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x2.cluster.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x2.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A9x2.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x2.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A9x2.daughterboard.hdl_cd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x2.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.cluster.cpu0	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x2.cluster.cpu1	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x2.motherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A9x2.motherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.daughterboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A9x2.motherboard.Timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x2.motherboard.Timer_2_3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x2	FVP_VE_Cortex_A9x2	Top level component of the Cortex-A9x2 Versatile Express inspired model.
FVP_VE_Cortex_A9x2.motherboard.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.Timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x2.daughterboard.hlcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x2.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x2.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x2.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-19 FVP_VE_Cortex-A9x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x2.motherboard.Time_r_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x2.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x2.motherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A9x2.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A9x2.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x2.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x2.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x2.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x2.motherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.motherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x2.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

5.20 FVP_VE_Cortex-A9x4

FVP_VE_Cortex-A9x4 contains the following instances:

Table 5-20 FVP_VE_Cortex-A9x4 instances

Name	Type	Description
FVP_VE_Cortex_A9x4.cluster.cpu3.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_A9x4.cluster.cpu3.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x4.motherboard.Timerr_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.Timerr_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.smsc_91c11	SMSC_91C11	SMSC 91C11 ethernet controller.
FVP_VE_Cortex_A9x4.daughterboard.hldcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x4.cluster	Cluster_ARM_Cortex-A9MP	ARM CORTEXA9MP Cluster CT model.
FVP_VE_Cortex_A9x4.motherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x4.motherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x4.daughterboard.hldcd	PL370_HLCD	ARM PrimeCell HD Color LCD Controller (Nominal Designation PL370).
FVP_VE_Cortex_A9x4.daughterboard.secureDRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.daughterboard.vedcc	VEDCC	Daughterboard Configuration Control (DCC).
FVP_VE_Cortex_A9x4.daughterboard.dmc	RAMDevice	RAM device, can be dynamic or static ram.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.daughterboard.non_secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x4.daughterboard.intr_outer	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_A9x4.motherboard.Tmr_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.Tmr_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_A9x4.motherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.daughterboard.secure_region	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x4.motherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_A9x4.cluster.cpu0	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x4.cluster.cpu1	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x4.cluster.cpu2	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x4.cluster.cpu3	ARM_Cortex-A9MP	ARM CORTEXA9MP CT model.
FVP_VE_Cortex_A9x4.daughterboard.dram_limit_8	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.cluster.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.motherboard	VEMotherBoard	Model inspired by the ARM Versatile Express Motherboard.
FVP_VE_Cortex_A9x4.daughterboard.dram_limit_4	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x4.motherboard.Timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x4.motherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_A9x4.motherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_A9x4.cluster.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.motherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.motherboard.Timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_A9x4.daughterboard.hcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x4.motherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x4.motherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.motherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.cluster.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.motherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x4.motherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_A9x4.daughterboard.sram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.cluster.cpu1.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x4.daughterboard.secureRO	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_A9x4.daughterboard.hdl_cd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A9x4.motherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_A9x4.motherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_A9x4.motherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x4.motherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x4.motherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x4.motherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_A9x4.motherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.daughterboard.clockLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_A9x4.motherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_A9x4.motherboard.Timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x4.motherboard.Timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x4.motherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.cluster.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_A9x4.motherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_A9x4.daughterboard.secureROloader	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_A9x4.cluster.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.motherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd.pl111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_A9x4.motherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd.pl111x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_A9x4	FVP_VE_Cortex_A9x4	Top level component of the Cortex-A9x4 Versatile Express inspired model.
FVP_VE_Cortex_A9x4.motherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x4.motherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x4.motherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x4.motherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_A9x4.daughterboard.dmc_phy	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.daughterboard.hdl_cd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.daughterboard	VEDaughterBoard	Daughtercard, inspired by the ARM Versatile Express development platform.
FVP_VE_Cortex_A9x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.cluster.cpu2.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x4.cluster.cpu3.llicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.motherboard.vram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.motherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_A9x4.motherboard.dum_my_local_dap_rom	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.motherboard.Timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x4.motherboard.Timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_A9x4.motherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_A9x4.motherboard.virtio_p9device	<i>VirtioP9Device</i>	virtio P9 server.
FVP_VE_Cortex_A9x4.motherboard.sp81_0_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.sp81_0_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.sp81_0_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.motherboard.sp81_0_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x4.cluster.cpu2.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_A9x4.daughterboard.secureSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_A9x4.cluster.cpu0.utlb	TlbCadi	TLB - instruction, data or unified.
FVP_VE_Cortex_A9x4.motherboard.pl111_clcd.pl111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_A9x4.motherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_A9x4.motherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-20 FVP_VE_Cortex-A9x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_A9x4.daughterboard.dram_aliases	<i>TZSwitch</i>	Allow TrustZone secure/normal bus signals to be routed separately.
FVP_VE_Cortex_A9x4.motherboard.virtio_blockdevice	<i>VirtioBlockDevice</i>	virtio block device.

5.21 FVP_VE_Cortex-R4

FVP_VE_Cortex-R4 contains the following instances:

Table 5-21 FVP_VE_Cortex-R4 instances

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.dum_my_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R4.vemotherboard.clock_100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R4.daughterboard.pl111_cled.pl11x_cled	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R4.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.daughterboard	VEDaughterBoardCortex_R4	Cortex-R4 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R4.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.clock_50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.dum_my_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.clock_35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R4.daughterboard.pl310_l2cc	<i>PL310_L2CC</i>	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R4.vemotherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R4.daughterboard.core.cpu0.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R4.vemotherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R4.vemotherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R4.vemotherboard.pl031_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R4.vemotherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R4.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.daughterboard.core	ARM_Cortex-R4	ARM CORTEXR4 CT model.
FVP_VE_Cortex_R4.daughterboard.pl111_cldc.pl11x_cldc.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R4.vemotherboard.pl111_cldc.pl11x_cldc.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R4.daughterboard.pl111_cldc.pl11x_cldc.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R4.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R4.vemotherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R4.vemotherboard.sp810_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.sp810_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.vis.recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.pl011_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R4.vemotherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R4.daughterboard.veinteerruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R4.vemotherboard.pl111_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R4.vemotherboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.daughterboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R4.vemotherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R4.vemotherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R4.vemotherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R4.vemotherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R4.vemotherboard.audio_out	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R4.vemotherboard.terminal_4	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.vis.re_corder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R4.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R4.vemotherboard.mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R4.daughterboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R4.daughterboard.core.cpu0.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R4.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R4.vemotherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R4.daughterboard.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R4.vemotherboard.pl111_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R4.vemotherboard.ve_sy_sregs	VE_SysRegs	-
FVP_VE_Cortex_R4.vemotherboard.dum_my_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R4	FVP_VE_Cortex_R4	Top level component of the Cortex_R4 Versatile Express inspired model.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R4.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R4.vemotherboard.vis.receiver.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R4.vemotherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R4.vemotherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R4.daughterboard.clock_CLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 5-21 FVP_VE_Cortex-R4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R4.vemotherboard.clock_24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R4.vemotherboard.timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart4	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R4.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R4.vemotherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R4.vemotherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R4.vemotherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R4.vemotherboard.video_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R4.vemotherboard.ps2keybord	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R4.daughterboard.pl390_gic	<i>PL390_GIC</i>	Generic Interrupt Controller (PL390).
FVP_VE_Cortex_R4.vemotherboard.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

5.22 FVP_VE_Cortex-R5x1

FVP_VE_Cortex-R5x1 contains the following instances:

Table 5-22 FVP_VE_Cortex-R5x1 instances

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.pl11_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R5x1.vemotherboard.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1	FVP_VE_Cortex_R5x1	Top level component of the Cortex_R5x1 Versatile Express inspired model.
FVP_VE_Cortex_R5x1.daughterboard.clockLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R5x1.vemotherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R5x1.vemotherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R5x1.vemotherboard.pl11_clcd.pl11x_clcd.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R5x1.vemotherboard.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x1.vemotherboard.pl11_clcd.pl11x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x1.daughterboard.core.cpu0	ARM_Cortex-R5	ARM CORTEXR5 CT model.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.vid_eo_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x1.vemotherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R5x1.vemotherboard.pl0_11_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x1.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x1.vemotherboard.dummmy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R5x1.daughterboard.cloc_kdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R5x1.vemotherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R5x1.vemotherboard.pl11_80_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R5x1.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x1.vemotherboard.pl0_50_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R5x1.vemotherboard.pl0_50_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R5x1.vemotherboard.pl0_50_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R5x1.vemotherboard.sp8_05_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R5x1.vemotherboard.sp8_10_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R5x1.daughterboard.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x1.daughterboard.pl3_10_l2cc	PL310_L2CC	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R5x1.vemotherboard.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x1.daughterboard.pl3_90_gic	PL390_GIC	Generic Interrupt Controller (PL390).
FVP_VE_Cortex_R5x1.vemotherboard.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x1.vemotherboard.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x1.vemotherboard.terminal_4	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x1.vemotherboard.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.smsc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R5x1.vemotherboard.vis_recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R5x1.vemotherboard mmc	MMC	Generic Multimedia Card.
FVP_VE_Cortex_R5x1.vemotherboard.pl11_11_clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.daughterboard.pl11_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R5x1.vemotherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R5x1.vemotherboard.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R5x1.vemotherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_R5x1.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R5x1.daughterboard.pl11_clcd.pl11x_clcd.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_R5x1.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.daughterboard.core	Cluster_ARM_Cortex-R5	ARM CORTEXR5 Cluster CT model.
FVP_VE_Cortex_R5x1.vemotherboard.pram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x1.daughterboard.pl11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x1.daughterboard.pl11_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R5x1.vemotherboard.timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x1.vemotherboard.timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart4	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x1.vemotherboard.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.sp810_sysctrl.clkdiv_clk3	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.sp810_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.vis_recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.vis_recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.daughterboard	VEDaughterBoardCorex_R5x1	Cortex-R5x1 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R5x1.vemotherboard.clockCLCD	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R5x1.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x1.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.daughterboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R5x1.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R5x1.vemotherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x1.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.daughterboard.vei_nterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R5x1.vemotherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R5x1.daughterboard.pl11_11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R5x1.vemotherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-22 FVP_VE_Cortex-R5x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x1.vemotherboard.pl0_11_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x1.vemotherboard.dummymy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

5.23 FVP_VE_Cortex-R5x2

FVP_VE_Cortex-R5x2 contains the following instances:

Table 5-23 FVP_VE_Cortex-R5x2 instances

Name	Type	Description
FVP_VE_Cortex_R5x2	FVP_VE_Cortex_R5x2	Top level component of the Cortex_R5x2 Versatile Express inspired model.
FVP_VE_Cortex_R5x2.daughterboard.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart4	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart4.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.daughterboard.pl390_gic	PL390_GIC	Generic Interrupt Controller (PL390).
FVP_VE_Cortex_R5x2.vemotherboard.dummymy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x2.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R5x2.vemotherboard.pl0_31 rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R5x2.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R5x2.vemotherboard.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R5x2.vemotherboard.audiout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R5x2.daughterboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.daughterboard.pl11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R5x2.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R5x2.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R5x2.vemotherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R5x2.vemotherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R5x2.daughterboard.pl11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R5x2.vemotherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl011_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R5x2.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R5x2.vemotherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.daughterboard.vei_nterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R5x2.vemotherboard.video_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.daughterboard.core	Cluster_ARM_Cortex-R5	ARM CORTEXR5 Cluster CT model.
FVP_VE_Cortex_R5x2.vemotherboard.p1111_clcd.p111x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x2.vemotherboard.psram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x2.vemotherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_R5x2.vemotherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R5x2.daughterboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.p1011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R5x2.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x2.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x2.vemotherboard.p1180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl11_11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R5x2.vemotherboard.vis_recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R5x2.daughterboard.pl3_10_l2cc	<i>PL310_L2CC</i>	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R5x2.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x2.vemotherboard.timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R5x2.vemotherboard.pl11_11_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R5x2.daughterboard.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.sp8_10_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R5x2.vemotherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R5x2.vemotherboard.pl11_11_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x2.vemotherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.vemotherboard.pl0_50_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R5x2.vemotherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl0_50_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.vemotherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl0_50_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R5x2.daughterboard.pl11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x2.vemotherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R5x2.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.vemotherboard.terminal_4	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R5x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-23 FVP_VE_Cortex-R5x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R5x2.vemotherboard.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R5x2.vemotherboard.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R5x2.vemotherboard.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x2.vemotherboard.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R5x2.daughterboard	VEDaughterBoardCortex_R5x2	Cortex-R5x2 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R5x2.vemotherboard.hostbridge	HostBridge	Host Socket Interface Component.
FVP_VE_Cortex_R5x2.daughterboard.pl111_clcd.pl111x_clcd.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R5x2.vemotherboard.smc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R5x2.daughterboard.pl111_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R5x2.daughterboard.core.cpu1	ARM_Cortex-R5	ARM CORTEXR5 CT model.
FVP_VE_Cortex_R5x2.vemotherboard.vis_recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R5x2.daughterboard.core.cpu0	ARM_Cortex-R5	ARM CORTEXR5 CT model.
FVP_VE_Cortex_R5x2.vemotherboard.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R5x2.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.

5.24 FVP_VE_Cortex-R7x1

FVP_VE_Cortex-R7x1 contains the following instances:

Table 5-24 FVP_VE_Cortex-R7x1 instances

Name	Type	Description
FVP_VE_Cortex_R7x1.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x1.vemotherboard.ps2keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R7x1.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R7x1.vemotherboard.timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x1.vemotherboard.pl11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R7x1.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x1.daughterboard.core.cpu0	ARM_Cortex-R7	ARM CORTEXR7 CT model.
FVP_VE_Cortex_R7x1.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R7x1.vemotherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x1.vemotherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R7x1.vemotherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.pl011_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x1.vemotherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_R7x1.vemotherboard.pl011_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x1.vemotherboard.pl011_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x1.vemotherboard.pl011_uart4	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x1.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.vemotherboard.au_dioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R7x1.vemotherboard.pl0_50_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R7x1.vemotherboard.pl1_80_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R7x1.vemotherboard.sp8_05_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R7x1.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x1.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1	FVP_VE_Cortex_R7x1	Top level component of the Cortex_R7x1 Versatile Express inspired model.
FVP_VE_Cortex_R7x1.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x1.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.vemotherboard.clo ck35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.ve _sysregs	VE_SysRegs	-
FVP_VE_Cortex_R7x1.vemotherboard.sp8 10_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R7x1.vemotherboard.pl1 11_clcd.pl11x_clcd.timer.timer.thread_eve nt	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R7x1.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.pl1 11_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R7x1.vemotherboard.vid eo_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x1.vemotherboard.pl0 50_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R7x1.vemotherboard.pl0 50_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R7x1.vemotherboard.sp8 10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.sp8 10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.clo ckCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.vemotherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x1.vemotherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x1.vemotherboard.ps2mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R7x1.vemotherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x1.vemotherboard.visrecorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R7x1.vemotherboard.terminal_4	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x1.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R7x1.vemotherboard.sp810_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.daughterboard.veinterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R7x1.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R7x1.vemotherboard.pl1111_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.daughterboard.peri_ph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.sp810_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R7x1.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R7x1.daughterboard.core	Cluster_ARM_Cortex-R7	ARM CORTEXR7 Cluster CT model.
FVP_VE_Cortex_R7x1.vemotherboard.vis_recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.daughterboard.core.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R7x1.vemotherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R7x1.daughterboard.core.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R7x1.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.dummymy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.vemotherboard.pl0_11_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.dummmy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R7x1.vemotherboard.pl11_clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R7x1.vemotherboard.pl0_11_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x1.vemotherboard.pl0_50_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.daughterboard.pl3_10_l2cc	<i>PL310_L2CC</i>	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R7x1.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R7x1.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R7x1.vemotherboard.pl0_11_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.vemotherboard.sm_sc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R7x1.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-24 FVP_VE_Cortex-R7x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x1.vemotherboard.psr.am	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x1.vemotherboard.pl0_31_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R7x1.vemotherboard.dummymy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x1.vemotherboard.pl0_11_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x1.daughterboard	VEDaughterBoardCortex_R7x1	Cortex_R7x1 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R7x1.vemotherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

5.25 FVP_VE_Cortex-R7x2

FVP_VE_Cortex-R7x2 contains the following instances:

Table 5-25 FVP_VE_Cortex-R7x2 instances

Name	Type	Description
FVP_VE_Cortex_R7x2.daughterboard.pl310_l2cc	PL310_L2CC	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R7x2.daughterboard.vei_ninterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R7x2.vemotherboard.pl011_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.sm_sc_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R7x2.vemotherboard.terminal_4	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R7x2.vemotherboard.timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x2.vemotherboard.dummy_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu1	ARM_Cortex-R7	ARM CORTEXR7 CT model.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu0	ARM_Cortex-R7	ARM CORTEXR7 CT model.
FVP_VE_Cortex_R7x2.vemotherboard.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x2.vemotherboard.timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x2.vemotherboard.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R7x2.vemotherboard.timer_0_1	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R7x2.vemotherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x2.vemotherboard.vis_recorder	VisEventRecorder	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R7x2.vemotherboard.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R7x2.vemotherboard.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x2.vemotherboard.pl11_11clcd.pl11x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R7x2.vemotherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.daughterboard.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu1.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R7x2.vemotherboard.vis_recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R7x2.vemotherboard.pl111_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R7x2.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu0.lliCache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R7x2	FVP_VE_Cortex_R7x2	Top level component of the Cortex_R7x2 Versatile Express inspired model.
FVP_VE_Cortex_R7x2.vemotherboard.pl1180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R7x2.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R7x2.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R7x2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl050_kmi1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl111_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R7x2.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R7x2.vemotherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard.sp805_wdog	SP805_Watchdog	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R7x2.vemotherboard.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R7x2.daughterboard.core	Cluster_ARM_Cortex-R7	ARM CORTEXR7 Cluster CT model.
FVP_VE_Cortex_R7x2.vemotherboard.timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R7x2.vemotherboard.pl011_uart1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.vis_recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu1.lldcache	PVCache	PV Cache.
FVP_VE_Cortex_R7x2.vemotherboard.pl050_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R7x2.vemotherboard.clock24MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.timer_0_1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.audiodioout	AudioOut SDL	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R7x2.vemotherboard.pl011_uart3.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl050_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_R7x2.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R7x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x2.vemotherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R7x2.daughterboard.core.cpu0.11deache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R7x2.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R7x2.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R7x2.vemotherboard.dummmy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R7x2.vemotherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R7x2.vemotherboard.sp10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl11_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R7x2.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart4	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x2.vemotherboard.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x2.vemotherboard.pl0_11_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R7x2.vemotherboard.vid_eo_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R7x2.vemotherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.

Table 5-25 FVP_VE_Cortex-R7x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R7x2.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_50_kmi0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.daughterboard	VEDaughterBoardCortex_R7x2	Cortex_R7x2 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R7x2.vemotherboard.timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R7x2.vemotherboard.pl0_31_rtc	PL031_RTC	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R7x2.vemotherboard.hostbridge	HostBridge	Host Socket Interface Component.
FVP_VE_Cortex_R7x2.vemotherboard.pram	RAMDevice	RAM device, can be dynamic or static ram.

5.26 FVP_VE_Cortex-R8x1

FVP_VE_Cortex-R8x1 contains the following instances:

Table 5-26 FVP_VE_Cortex-R8x1 instances

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.vis.recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.daughterboard	VEDaughterBoardCortex_R8x1	Cortex_R8x1 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R8x1.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R8x1.vemotherboard.pl050_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x1.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R8x1.vemotherboard.pl050_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl041_aaci	<i>PL041_AACI</i>	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R8x1.vemotherboard.dummymy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x1.vemotherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x1.vemotherboard.timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.daughterboard.dram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x1.daughterboard.periph_clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl0_50_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.dummy_usb	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x1.vemotherboard.sp8_10_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R8x1.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R8x1.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl0_11_uart0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1	FVP_VE_Cortex_R8x1	Top level component of the Cortex_R8x1 Versatile Express inspired model.
FVP_VE_Cortex_R8x1.vemotherboard.pl0_11_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl0_11_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.daughterboard.core.cpu0.lliicache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x1.daughterboard.vei_nterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R8x1.vemotherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R8x1.vemotherboard.terminal_4	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x1.vemotherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_R8x1.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R8x1.vemotherboard.dummy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.telnet_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x1.vemotherboard.telnet_2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x1.vemotherboard.telnet_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x1.daughterboard.core	Cluster_ARM_Cortex-R8	ARM CORTEXR8 Cluster CT model.
FVP_VE_Cortex_R8x1.vemotherboard.telnet_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x1.vemotherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R8x1.daughterboard.core.cpu0	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x1.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R8x1.vemotherboard.flashloader1	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R8x1.vemotherboard.pl050_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x1.vemotherboard.pl111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x1.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x1.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x1.vemotherboard.video_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x1.vemotherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.pl11_clcd	PL111_CLCD	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R8x1.vemotherboard.timer_2_3	SP804_Timer	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart1	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart0	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart3	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x1.vemotherboard.pl011_uart4	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x1.vemotherboard.sp810_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.daughterboard.exclusive_monitor	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_VE_Cortex_R8x1.vemotherboard.vis_recorder.recordingDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.clock50Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_R8x1.vemotherboard.flash1	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R8x1.vemotherboard.flash0	IntelStrataFlashJ3	Intel Strata Flash J3 LISA+ model.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.vis_recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R8x1.daughterboard.pl3_10_l2cc	<i>PL310_L2CC</i>	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R8x1.daughterboard.core.cpu0.l1lcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x1.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R8x1.vemotherboard.psr_am	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x1.vemotherboard.pl1_80_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R8x1.vemotherboard.timer_2_3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.pl1_11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R8x1.vemotherboard.timer_0_1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x1.vemotherboard.timer_0_1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x1.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.smc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.

Table 5-26 FVP_VE_Cortex-R8x1 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x1.vemotherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.p11_11_clcd.p111x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R8x1.vemotherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.sp8_10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x1.vemotherboard.p10_31_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R8x1.vemotherboard.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.

5.27 FVP_VE_Cortex-R8x2

FVP_VE_Cortex-R8x2 contains the following instances:

Table 5-27 FVP_VE_Cortex-R8x2 instances

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.terminal_4	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R8x2.vemotherboard.timer_0_1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.dummy_CF	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R8x2.daughterboard.core.cpu0.l1dcache	PVCache	PV Cache.
FVP_VE_Cortex_R8x2.vemotherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R8x2.vemotherboard.pl050_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.timer_2_3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x2.vemotherboard.hostbridge	HostBridge	Host Socket Interface Component.
FVP_VE_Cortex_R8x2.vemotherboard.sp810_sysctrl.clkdiv_clk1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x2.vemotherboard.timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x2.vemotherboard.pl011_uart4	PL011_Uart	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x2.vemotherboard.video_ram	RAMDevice	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x2.vemotherboard.pl011_uart2	PL011_Uart	ARM PrimeCell UART(PL011).

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x2.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.daughterboard.core.cpu1.l1icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x2.daughterboard.periph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.dummy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x2.daughterboard.core.cpu1.l1dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x2.vemotherboard.psr_am	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2	FVP_VE_Cortex_R8x2	Top level component of the Cortex_R8x2 Versatile Express inspired model.
FVP_VE_Cortex_R8x2.vemotherboard.sp8_05_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).
FVP_VE_Cortex_R8x2.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R8x2.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.ps2_mouse	PS2Mouse	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R8x2.vemotherboard.vis_recorder.playbackDivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R8x2.vemotherboard.ve_sysregs	VE_SysRegs	-
FVP_VE_Cortex_R8x2.vemotherboard.pl0_50_kmi1	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk2	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.daughterboard.core	Cluster_ARM_Cortex-R8	ARM CORTEXR8 Cluster CT model.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_41_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R8x2.vemotherboard.pl0_50_kmi0	PL050_KMI	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart4.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.daughterboard.core.cpu0.11icache	PVCache	PV Cache.

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.timer_2_3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.p11_11_clcd.p111x_clcd.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R8x2.vemotherboard.terminal_1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x2.vemotherboard.terminal_0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x2.vemotherboard.terminal_3	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x2.vemotherboard.p10_31_rtc	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R8x2.vemotherboard.clock100Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.daughterboard.p13_10_l2cc	<i>PL310_L2CC</i>	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R8x2.vemotherboard.p11_11_clcd.p111x_clcd.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x2.vemotherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R8x2.vemotherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.ps2_keyboard	<i>PS2Keyboard</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R8x2.vemotherboard.pl11_80_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R8x2.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R8x2.vemotherboard.dummy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x2.vemotherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R8x2.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R8x2.vemotherboard.flashloader0	<i>FlashLoader</i>	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R8x2.vemotherboard.sp810_sysctrl	<i>SP810_SysCtrl</i>	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R8x2.vemotherboard.sm_sc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R8x2.vemotherboard.timer_2_3_clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R8x2.daughterboard.core.cpu0	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x2.daughterboard.core.cpu1	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x2.vemotherboard.vis_recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R8x2.vemotherboard.pl11_clcd.pl11x_clcd	<i>PL11x_CLCD</i>	Internal component used by PL110 and PL111 CLCD controllers.

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x2.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.
FVP_VE_Cortex_R8x2.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x2.vemotherboard.pl0_11_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.clock35MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl1_11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x2.vemotherboard.pl0_50_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.terminal_2	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 5-27 FVP_VE_Cortex-R8x2 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x2.vemotherboard.ck50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.daughterboard.venterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R8x2.vemotherboard.ckCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.audiodioout	<i>AudioOut_SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R8x2.vemotherboard.vis.recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x2.vemotherboard.pl111_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R8x2.daughterboard	VEDaughterBoardCortex_R8x2	Cortex_R8x2 DaughterBoard for Versatile Express.

5.28 FVP_VE_Cortex-R8x4

FVP_VE_Cortex-R8x4 contains the following instances:

Table 5-28 FVP_VE_Cortex-R8x4 instances

Name	Type	Description
FVP_VE_Cortex_R8x4.vemotherboard.dummmy_CF	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart1	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart2	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart3	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart4	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.audioout	<i>AudioOut SDL</i>	SDL based Audio Output for PL041_AACI.
FVP_VE_Cortex_R8x4.vemotherboard.flash0	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R8x4.vemotherboard.flash1	<i>IntelStrataFlashJ3</i>	Intel Strata Flash J3 LISA+ model.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_50_kmi1	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x4.vemotherboard.pl0_50_kmi0	<i>PL050_KMI</i>	ARM PrimeCell PS2 Keyboard/Mouse Interface(PL050).
FVP_VE_Cortex_R8x4.vemotherboard.sp8_10_sysctrl.clkdiv_clk2	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4.vemotherboard.sp8_10_sysctrl.clkdiv_clk3	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.sp8_10_sysctrl.clkdiv_clk0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.sp8_10_sysctrl.clkdiv_clk1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.dummymy_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x4.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.timer_0_1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.timer_0_1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.clockCLCD	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.timer_0_1	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu0.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_VE_Cortex_R8x4.vemotherboard.timer_2_3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x4.vemotherboard.timer_2_3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x4.vemotherboard.timer_2_3	<i>SP804_Timer</i>	ARM Dual-Timer Module(SP804).
FVP_VE_Cortex_R8x4.vemotherboard.pl011_uart0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.pl011_uart3.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.daughterboard	VEDaughterBoardCorex_R8x4	Cortex_R8x4 DaughterBoard for Versatile Express.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu2.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.pram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x4.vemotherboard.clock24MHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.pl031_RTC	<i>PL031_RTC</i>	ARM PrimeCell Real Time Clock(PL031).
FVP_VE_Cortex_R8x4.daughterboard.core.cpu3.11dcache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard mmc	<i>MMC</i>	Generic Multimedia Card.

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4.vemotherboard.sp8_10_sysctrl	SP810_SysCtrl	Only EB relevant functionalities are fully implemented.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu2.11icache	PVCache	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.terminal_3	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R8x4.vemotherboard.terminal_2	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R8x4.vemotherboard.terminal_1	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R8x4.vemotherboard.terminal_0	TelnetTerminal	Telnet terminal interface.
FVP_VE_Cortex_R8x4.daughterboard.vei_nterruptmapper	VEInterruptMapper	Interrupt Mapping peripheral (non-cascaded).
FVP_VE_Cortex_R8x4.vemotherboard.clock100Hz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu1.11icache	PVCache	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.pl11_11clcd.pl11x_clcd	PL11x_CLCD	Internal component used by PL110 and PL111 CLCD controllers.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_50_kmi1.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu1.11deache	PVCache	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.ve__sysregs	VE_SysRegs	-
FVP_VE_Cortex_R8x4.vemotherboard.vis	VEVisualisation	Display window for VE using Visualisation library.
FVP_VE_Cortex_R8x4.vemotherboard.flashloader1	FlashLoader	A device that can preload a gzipped image into flash at startup.
FVP_VE_Cortex_R8x4.vemotherboard.flashloader0	FlashLoader	A device that can preload a gzipped image into flash at startup.

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4.daughterboard.peri_ph_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.daughterboard.dram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x4.vemotherboard.terminal_4	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_VE_Cortex_R8x4.vemotherboard.pl11_11_clcd.pl11x_clcd.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x4.vemotherboard.vis_recorder.recordingDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.pl180_mci	<i>PL180_MCI</i>	ARM PrimeCell Multimedia Card Interface (PL180).
FVP_VE_Cortex_R8x4.vemotherboard.pl11_11_clcd	<i>PL111_CLCD</i>	ARM PrimeCell Color LCD Controller(PL111).
FVP_VE_Cortex_R8x4.vemotherboard.vis_recorder	<i>VisEventRecorder</i>	Event recorder component for visualisation component (allows to playback and record interactive GUI sessions).
FVP_VE_Cortex_R8x4.vemotherboard.video_ram	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu0.11icache	<i>PVCache</i>	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.ps2_mouse	<i>PS2Mouse</i>	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart0	<i>PL011_Uart</i>	ARM PrimeCell UART(PL011).
FVP_VE_Cortex_R8x4.vemotherboard.sp805_wdog	<i>SP805_Watchdog</i>	ARM Watchdog Module(SP805).

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4.vemotherboard.pl0_50_kmi0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart4.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.sm_sc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_VE_Cortex_R8x4.vemotherboard.pl11_cled.pl11x_cled.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_VE_Cortex_R8x4.vemotherboard	VEMotherBoardR	Model inspired by the ARM Versatile Express Motherboard for R profile.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu0	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu1	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu2	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu3	ARM_Cortex-R8	ARM CORTEXR8 CT model.
FVP_VE_Cortex_R8x4.vemotherboard.vis_recorder.playbackDivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.dummymy_usb	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_VE_Cortex_R8x4.daughterboard.exclusive_monitor	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_VE_Cortex_R8x4.daughterboard.core	Cluster_ARM_Cortex-R8	ARM CORTEXR8 Cluster CT model.

Table 5-28 FVP_VE_Cortex-R8x4 instances (continued)

Name	Type	Description
FVP_VE_Cortex_R8x4	FVP_VE_Cortex_R8x4	Top level component of the Cortex_R8x4 Versatile Express inspired model.
FVP_VE_Cortex_R8x4.daughterboard.core.cpu3.1l1icache	PVCache	PV Cache.
FVP_VE_Cortex_R8x4.vemotherboard.clock35MHz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_11_uart2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.timer_0_1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x4.vemotherboard.timer_0_1.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_VE_Cortex_R8x4.vemotherboard.pl11_clcd.pl11x_clcd.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_VE_Cortex_R8x4.vemotherboard.pl0_41_aaci	PL041_AACI	ARM PrimeCell Advanced Audio CODEC Interface(PL041).
FVP_VE_Cortex_R8x4.daughterboard.pl3_10_l2cc	PL310_L2CC	ARM PrimeCell Level 2 Cache Controller (PL310).
FVP_VE_Cortex_R8x4.vemotherboard.ps2_keyboard	PS2Keyboard	Interface component, which takes the keypress/release signals from the Visualisation component and translates them into clocked PS2Data signals which can be routed to a PL050_KMI component.
FVP_VE_Cortex_R8x4.vemotherboard.timer_2_3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_VE_Cortex_R8x4.vemotherboard.timer_2_3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Chapter 6

MPS2 Platform FVPs

This chapter lists the MPS2 Platform FVPs and the components in them.

It contains the following sections:

- [6.1 FVP_MPS2_AEMv8M on page 6-911](#).
- [6.2 FVP_MPS2_Cortex-M0 on page 6-925](#).
- [6.3 FVP_MPS2_Cortex-M0plus on page 6-940](#).
- [6.4 FVP_MPS2_Cortex-M23 on page 6-955](#).
- [6.5 FVP_MPS2_Cortex-M3 on page 6-970](#).
- [6.6 FVP_MPS2_Cortex-M33 on page 6-984](#).
- [6.7 FVP_MPS2_Cortex-M35P on page 6-999](#).
- [6.8 FVP_MPS2_Cortex-M4 on page 6-1014](#).
- [6.9 FVP_MPS2_Cortex-M7 on page 6-1028](#).
- [6.10 FVP_MPS2_SSE-200_AEMv8M_pipeline on page 6-1042](#).
- [6.11 FVP_MPS2_SSE-200_Cortex-M33 on page 6-1055](#).
- [6.12 FVP_MPS2_SecurCore-SC000 on page 6-1070](#).
- [6.13 FVP_MPS2_SecurCore-SC300 on page 6-1085](#).

6.1 FVP_MPS2_AEMv8M

FVP_MPS2_AEMv8M contains the following instances:

Table 6-1 FVP_MPS2_AEMv8M instances

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M	FVP_MPS2_AEMv8M	-
FVP_MPS2_AEMv8M.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_AEMv8M.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_AEMv8M.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_AEMv8M.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.a_cg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.a_cg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.a_cg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.a_cg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.pl022_ss_p_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_AEMv8M.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_AEMv8M.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_AEMv8M.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_AEMv8M.fvp_mps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_AEMv8M.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_AEMv8M.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.PSRAM_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_AEMv8M.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.fpga_sys_ctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_AEMv8M.fvp_mps2.uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_mpc_iotss_ssram1	<i>IoTSS_MemoryProtectionController</i>	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.telnetterm_minall	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.dma3.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.GPIO_connection_test.GPIO1_port_test	<i>GPIO1_Connection_Test</i>	-
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.svos_du altimer.svos_dualltimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.ahb_ppc _iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.ahb_ppc _iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.UART2. clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.pl022_ss p_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.dma3_id au_labeller	LabellerIdauSecurity	-
FVP_MPS2_AEMv8M.fvp_mps2.dma2.ti mer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.svos_du altimer.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.c lockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.ti mer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.c pu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_AEMv8M.fvp_mps2.dma2.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.msdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.msdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_AEMv8M.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualltimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.clock50_Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.mpc_iot_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.ram0_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.s32k_timer.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.sys_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.aborting_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_AEMv8M.fvp_mps2.stub_i2c1	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.timer1.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.ram2_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer2.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mem_switch_internal_sram_mpc	PVBusRouter	Allow transactions to be routed arbitrarily.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.svos_du altimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.r am1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.dma1.ti mer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.spiden_ or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.dma1.ti mer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_AEMv8M.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_se cure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_v isualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.s 32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.dma0_id au_labeller	LabellerIdauSecurit y	-
FVP_MPS2_AEMv8M.fvp_mps2.svos_du altimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200. mpc_iotss_internal_sram1.gating_disabled _thread_event	<i>SchedulerThreadEve nt</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.gpio_1_ or_3	<i>OrGate</i>	Or Gate.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.fpga_sys_ctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_AEMv8M.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.dma1.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.mps2_cmsdk_dultimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.dma2.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.access_cg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.access_cg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_AEMv8M.fvp_mps2.fpga_sys_ctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.ssram1	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.ssram2	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.PSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_AEMv8M.fvp_mps2.dma0.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_internal_sram3	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.clk25Mhz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_AEMv8M.fvp_mps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_dualltimer.svos_dualltimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_psram	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer1.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_AEMv8M.fvp_mps2.mem_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.stub_spi0	RAMDevice	RAM device, can be dynamic or static ram.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_AEMv8M.fvp_mps2.stub_spi2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.dma0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_AEMv8M.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_AEMv8M.fvp_mps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_AEMv8M.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_AEMv8M.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_labeller	LabellerIdauSecurity	-
FVP_MPS2_AEMv8M.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_AEMv8M.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_AEMv8M.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.

Table 6-1 FVP_MPS2_AEMv8M instances (continued)

Name	Type	Description
FVP_MPS2_AEMv8M.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_AEMv8M.fvp_mps2.svos_du_altimer.svos_dualtimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_AEMv8M.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.spniden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_AEMv8M.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_AEMv8M.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_AEMv8M.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_AEMv8M.cpu0	ARM_AEMv8M	ARM AEMv8M CT model.
FVP_MPS2_AEMv8M.cpu1	ARM_AEMv8M	ARM AEMv8M CT model.
FVP_MPS2_AEMv8M.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_AEMv8M.fvp_mps2.switch_svos_dualtimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_AEMv8M.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

6.2 FVP_MPS2_Cortex-M0

FVP_MPS2_Cortex-M0 contains the following instances:

Table 6-2 FVP_MPS2_Cortex-M0 instances

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.dma2.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_cmsdk_dualtimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200_secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cpu1core_ppu	<i>PPUV0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.stub_sp_i0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M0.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cmsdk_dualtimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M0.fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.armcortexm0ct	ARM_Cortex-M0	ARM CORTEXM0 CT model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_ssram2	<i>IoTSS_AccessControlGate</i>	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_io.tss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0.fvp_mps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.dma3_i_dau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0.fvp_mps2.dma1	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0.fvp_mps2.dma2	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0.fvp_mps2.dma3	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0.fvp_mps2.dma1.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.ram2_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.stub_i2s	RAMDevice	RAM device, can be dynamic or static ram.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.pl022_ssp_mps2.prescaler	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.PSRA_M_M7	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer0.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.fpga_sysctrl.callBack100HzCounter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.hostbridge	HostBridge	Host Socket Interface Component.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.ram0_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.dma3.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2 gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.switch_svos_dualtimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.spnide_n_or_gate	<i>OrGate</i>	Or Gate.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M0.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200_s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200_s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200_ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.dma1.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.iotss_cpidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0	FVP_MPS2_Cortex_M0	-
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M0.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_dualtimer.svos_dualtimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.stub_sp_i2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M0.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0.fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M0.fvp_mps2.svos_d ualtimer.svos_dualtimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.

Table 6-2 FVP_MPS2_Cortex-M0 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-

6.3 FVP_MPS2_Cortex-M0plus

FVP_MPS2_Cortex-M0plus contains the following instances:

Table 6-3 FVP_MPS2_Cortex-M0plus instances

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.iotsss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.ram2_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_exclusive_monitor_zbtssram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_exclusive_monitor_zbtssram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cmsdk_dualtimer.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub_spi0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.uart_overflows_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.crypto_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_timer1.counter	CounterModule	Internal component used by SP804 Timer module.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.armcortexm0plusct	ARM_Cortex-M0+	ARM CORTEXM0+ CT model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualltimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M0plus.fvp_mps2.expand_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M0plus.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus	FVP_MPS2_Cortex_M0plus	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub_spi2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_zbtssram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpcc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpcc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpcc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO1_Connection_Test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpss2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO0_Port_Transfer	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.swatch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.iotss_cpuidentity	<i>IoTSS_CPUIdentity</i>	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.VGA_interface	<i>MPS2_VGA</i>	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.idau_labeller	<i>LabellerIdauSecurity</i>	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.touchescreen_interface	<i>MPS2_TouchScreen</i>	MPS2 Touch Screen.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mem_switch_internal_sram_mpc	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0plus.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.clk25khz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer3.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mp52_timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.telnetterminal1	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M0plus.fvp_mps2.telnetterminal0	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cordio_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cpu1core_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mem_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.mp_s2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mp_s2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M0plus.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mp_s2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.spn_iden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mp_s2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.PS_RAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.nid_en_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse_200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.mhu0	<i>IoTSS_MessageHandlingUnit</i>	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer0	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer1	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer2	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer3	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_psram	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualtimer.svos_dualtimer1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.fpg_a_sysctrl.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.sys_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma2	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.spi_deny_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.nmi_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cmsdk_dualtimer.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mem_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cmsdk_dualtimer.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.PSRAM_M7	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.exclusive_monitor_zbtssram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.stub_i2s	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.platform_switch_dma1	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.platform_switch_dma0	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	PVBusExclusiveMonitor	Global exclusive monitor.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.execclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M0plus.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M0plus.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2.dma0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M0plus.fvp_mps2	FVP_MPS2	MPS2 DUT.

Table 6-3 FVP_MPS2_Cortex-M0plus instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.svo_s_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.ap_b_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M0plus.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M0plus.fvp_mps2.ap_b_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.

6.4 FVP_MPS2_Cortex-M23

FVP_MPS2_Cortex-M23 contains the following instances:

Table 6-4 FVP_MPS2_Cortex-M23 instances

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M23.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M23.fvp_mps2.dma0	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M23.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_cmsdk_dualltimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_cmsdk_dualltimer.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.cpu_wait_or_gate_1	OrGate	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.cpu_wait_or_gate_0	OrGate	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disable_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.ahb_pc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.cpu0core_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.s32k_timer.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.UAR_T0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M23.fvp_mps2.ahb_pc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.apb_pc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.apb_pc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.apb_pc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M23.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.clock_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M23.fvp_mps2.spnid_en_or_gate	<i>OrGate</i>	Or Gate.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M23.fvp_mps2.PSRA_M_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M23.fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M23.fvp_mps2.uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1_securitymodifier	SecurityModifier	-

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.ram0_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.cpu0dbg_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.sys_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.platform_switch_dma0	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23	FVP_MPS2_Cortex_M23	-
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.timer1.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.UAR_T0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M23.fvp_mps2.UAR_T2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.dma0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mpc_iotss_internal_sram1.gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mpc_iotss_internal_sram2.gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.switch_svos_dualtimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.UAR_T1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.cmsdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M23.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M23.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M23.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M23.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.stub_spi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.stub_spi2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.dma2.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.spide_n_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M23.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M23.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M23.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.exclusive_monitor_zbtssram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M23.cpu0	ARM_Cortex-M23	ARM CORTEXM23 CT model.
FVP_MPS2_Cortex_M23.cpu1	ARM_Cortex-M23	ARM CORTEXM23 CT model.
FVP_MPS2_Cortex_M23.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20.0.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M23.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M23.fvp_mps2.dma0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.fpga_sysctrl.callBack100HzCounter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mpc_iotss_internal_sram3.gating_disable_d_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_exclusive_monitor_zbtsram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_exclusive_monitor_zbtsram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M23.fvp_mps2.UART2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.telnetterminal1	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M23.fvp_mps2.telnetterminal0	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.mem_switch_internal_sram	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M23.fvp_mps2.mps2_cmsdk_dualltimer.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M23.fvp_mps2.dma2	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M23.fvp_mps2.sse20_0.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.

Table 6-4 FVP_MPS2_Cortex-M23 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M23.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

6.5 FVP_MPS2_Cortex-M3

FVP_MPS2_Cortex-M3 contains the following instances:

Table 6-5 FVP_MPS2_Cortex-M3 instances

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.iotss_cpidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualltimer.svos_dualtimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualltimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualltimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualltimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_1cd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M3.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M3.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.dma1.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.dma2.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_io_tss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M3.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.dma0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M3.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M3.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M3.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M3.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.dma1.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M3.fvp_mps2.dma1_securitymodifier	SecurityModifier	-

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M3.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.platformswitch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M3.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.dma3.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M3.fvp_mps2.spnidene_or_gate	<i>OrGate</i>	Or Gate.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_daultimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cmsdk_daultimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.cpu_await_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.cpu_await_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_daultimer.svos_dualtimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.PSRA_M_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.switch_svos_daultimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_cmsdk_daultimer	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.dma0	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M3.fvp_mps2.dma3.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.dbgen_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_zbtsram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.armcortexm3ct	ARM_Cortex-M3	ARM CORTEXM3 CT model.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer1.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.niden_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.stub_i2c1	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_cmsdk_dualtimer.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer0.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M3.fvp_mps2.mem_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M3.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M3.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M3.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M3.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M3.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_zbtsram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200_iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.mem_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.clk25khz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200_iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200_nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M3.fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.pl022_ssp_mps2.prescaler	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.dma3.timer	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M3.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M3.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svostimer0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svostimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2 gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M3.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M3.fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3	FVP_MPS2_Cortex_M3	-
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M3.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.platform_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M3.fvp_mps2.smse_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M3.fvp_mps2.stub_sp_i0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M3.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M3.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

Table 6-5 FVP_MPS2_Cortex-M3 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M3.fvp_mps2.stub_sp_i2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.telnettermal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M3.fvp_mps2.telnettermal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cmsdk_dualtimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.sse200.cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M3.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

6.6 FVP_MPS2_Cortex-M33

FVP_MPS2_Cortex-M33 contains the following instances:

Table 6-6 FVP_MPS2_Cortex-M33 instances

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.spide_n_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.stub_s_pi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.stub_s_pi2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram3.gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.clock_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M33.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M33.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2__mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M33.fvp_mps2.dma3.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M33.fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M33.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M33.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M33.fvp_mps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M33.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_ssram1_gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.UAR_T0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M33.fvp_mps2.UAR_T1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M33.fvp_mps2.UAR_T2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.apb_pc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.apb_pc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.apb_pc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M33	FVP_MPS2_Cortex_M33	-
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.ahb_pc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.ahb_pc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.PSRAM_M_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_psram1.gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_zbtssram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.cpu1	ARM_Cortex-M33	ARM CORTEXM33 CT model.
FVP_MPS2_Cortex_M33.cpu0	ARM_Cortex-M33	ARM CORTEXM33 CT model.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M33.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M33.fvp_mps2.UAR_T0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram0.gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M33.fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M33.fvp_mps2.dma0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.UAR_T2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M33.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M33.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram2_gating_disable_d_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M33.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.spnid_en_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M33.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M33.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.clock_50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_exclusive_monitor_zbtsram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_exclusive_monitor_zbtsram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.platform_switch_dma1	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.timer0.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.crypto_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.iotss_internal_ssram0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M33.fvp_mps2.dma2.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M33.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.exclusive_monitor_iotss_internal_ssram3	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.cmsdk_dualltimer.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse200.cmsdk_dualltimer.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M33.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M33.fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M33.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M33.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M33.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.mpc_iotss_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M33.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M33.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M33.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M33.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-6 FVP_MPS2_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M33.fvp_mps2.telnett_erminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M33.fvp_mps2.sse20_0.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

6.7 FVP_MPS2_Cortex-M35P

FVP_MPS2_Cortex-M35P contains the following instances:

Table 6-7 FVP_MPS2_Cortex-M35P instances

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.UAR_T1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.UAR_T0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.UAR_T2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.UAR_T0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M35P.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_spi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma_0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M35P.fvp_mps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.pl02_2_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M35P.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_O2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_O3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_O0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_O1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M35P.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M35P.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M35P	FVP_MPS2_Cortex_M35P	-
FVP_MPS2_Cortex_M35P.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M35P.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_mpc_iotss_ssram1_gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3.timer.thread.event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M35P.fvp_mps2.spide_n_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualtimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M35P.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M35P.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.cpu1	ARM_Cortex-M35P	ARM CORTEXM35P CT model.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse20.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.switch_svos_dualtimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M35P.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M35P.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M35P.fvp_mps2.spniden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mem_switch_internal_sram_mpc	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M35P.fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.sys_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M35P.fvp_mps2.fpga_sysctrl.callBack100HzCounter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M35P.fvp_mps2.UART2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.iotss_internal_sram0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.iotss_internal_sram1	RAMDevice	RAM device, can be dynamic or static ram.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M35P.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse2_00.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.host_bridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M35P.cpu0	ARM_Cortex-M35P	ARM CORTEXM35P CT model.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M35P.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M35P.fvp_mps2.pl02_2_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.nide_n_or_gate	<i>OrGate</i>	Or Gate.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.gpio_1_or_3	OrGate	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer0.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M35P.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M35P.fvp_mps2.expansion_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.stub_spi2	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M35P.fvp_mps2.PSRAM_M7	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M35P.fvp_mps2.dbgen_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.bus_error_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M35P.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-7 FVP_MPS2_Cortex-M35P instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.sse200.cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M35P.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M35P.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

6.8 FVP_MPS2_Cortex-M4

FVP_MPS2_Cortex-M4 contains the following instances:

Table 6-8 FVP_MPS2_Cortex-M4 instances

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2 gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M4.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M4.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M4.fvp_mps2.apb_pp_c_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.apb_pp_c_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.apb_pp_c_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200_ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200_clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.dbgem_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.ahb_pp_c_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.ahb_pp_c_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M4.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M4.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M4.fvp_mps2.smse_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M4.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200_iotss_internal_ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.stub_sp_i2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_cmsdk_dualtimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_duallimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_duallimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_duallimer.svos_dualtimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.dma0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M4.armcortexm4ct	ARM_Cortex-M4	ARM CORTEXM4 CT model.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_duallimer.svos_dualtimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_duallimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_mpc_iotss_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.stub_i2_c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.dma3.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M4.fvp_mps2.PSRA_M_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.stub_i2_s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M4.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M4.fvp_mps2.clock5_0Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M4.fvp_mps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cordio_ppu	<i>PPUVo</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M4.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_exclusive_monitor_zbtsram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.telnetterminal2	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_1cd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.nmi_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mem_switch_internal_sram_mpc	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M4.fvp_mps2.dma3.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.ram3_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.dma0	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M4.fvp_mps2.dma1	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M4.fvp_mps2.dma2	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M4.fvp_mps2.dma3	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.dma0.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_io_tss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M4.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M4.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M4.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M4.fvp_mps2 uart_overflows_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mem_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.UART0.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_t timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M4.fvp_mps2.fpga_systemctrl.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.dbg_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M4	FVP_MPS2_Cortex_M4	-
FVP_MPS2_Cortex_M4.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M4.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter0	CounterModule	Internal component used by SP804 Timer module.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M4.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M4.fvp_mps2.cpu_wait_or_gate_1	OrGate	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.cpu_wait_or_gate_0	OrGate	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.dma1.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.ram0_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.timer1.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M4.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.bus_error_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M4.clk25Mhz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M4.fvp_mps2.dma0.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M4.fvp_mps2.exclusive_monitor_psram	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.expansion_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M4.fvp_mps2.stub_sp_i0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cpu1core_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.

Table 6-8 FVP_MPS2_Cortex-M4 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M4.fvp_mps2.dma2.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M4.fvp_mps2.spnide_n_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.dma2.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_cpu0	<i>IoTSS_AccessControlGate</i>	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.acg_cpu1	<i>IoTSS_AccessControlGate</i>	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M4.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_Cortex_M4.fvp_mps2.dma1.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M4.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

6.9 FVP_MPS2_Cortex-M7

FVP_MPS2_Cortex-M7 contains the following instances:

Table 6-9 FVP_MPS2_Cortex-M7 instances

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_Cortex_M7.fvp_mps2.ahb_pp_c_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.ahb_pp_c_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.switch_svos_dualltimer	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.clk25khz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.default_ahb_slave	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_psram_iotss	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.dma2.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_cmsdk_dualltimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer1.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.niden_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.fpga_sysctrl.callBack100HzCounter	CounterModule	Internal component used by SP804 Timer module.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cmsdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.dma1.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.platform_bus_switch	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.crypto_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.dma2.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.bus_error_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M7.fvp_mps2.gpio_1_or_3	OrGate	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.telnet_terminal2	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_Cortex_M7.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M7.fvp_mps2.platform_switch_dma0	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.platform_switch_dma1	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.dma1.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M7.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M7.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0.timer.timer_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_Cortex_M7.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M7.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M7.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualltimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_Cortex_M7.fvp_mps2.dma1.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_Cortex_M7.fvp_mps2.UART2.clk_divider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer0.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.nmi_or_gate	OrGate	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_Cortex_M7.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M7.armcortexm7ct	ARM_Cortex-M7	ARM CORTEXM7 CT model.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.stub_sp_i2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.stub_sp_i0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_d_ualtimer.svos_dualtimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_d_ualtimer.svos_dualtimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.clock5_0Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M7.fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_Cortex_M7.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M7.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M7	FVP_MPS2_Cortex_M7	-

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200_dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200_s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_Cortex_M7.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_Cortex_M7.fvp_mps2.sse200_ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_Cortex_M7.fvp_mps2.sse200_cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.cpu_await_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.cpu_await_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M7.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M7.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M7.fvp_mps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_Cortex_M7.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M7.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_Cortex_M7.fvp_mps2.PSRA_M_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-9 FVP_MPS2_Cortex-M7 instances (continued)

Name	Type	Description
FVP_MPS2_Cortex_M7.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_Cortex_M7.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_Cortex_M7.fvp_mps2.mps2_cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_Cortex_M7.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.spniden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_Cortex_M7.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_Cortex_M7.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_Cortex_M7.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.

6.10 FVP_MPS2_SSE-200_AEMv8M_pipeline

FVP_MPS2_SSE-200_AEMv8M_pipeline contains the following instances:

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances

Name	Type	Description
fvp_mps2.PSRAM_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.svos_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
aborting_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
fvp_mps2.dma2_securitymodifier	SecurityModifier	-
fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
fvp_mps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.gpio_0_or_2	<i>OrGate</i>	Or Gate.
fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.dma2.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.svos_dualtimer.svos_dualtimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.cmsdk_dualtimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.cmsdk_dualtimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.svos_dualtimer.svos_dualtimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.svos_dualtimer.svos_dualtimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.svos_dualltimer.svos_dualltimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.dma0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.signal_router	SignalRouter	Signal router.
fvp_mps2.touchscreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
fvp_mps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
fvp_mps2.dma0_securitymodifier	SecurityModifier	-
fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
fvp_mps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
fvp_mps2.dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
fvp_mps2.sse200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
fvp_mps2.sse200.cmsdk_dualltimer.clk_div_0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.cmsdk_dualltimer.clk_div_1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.stub_spi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.dma3.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.mpc_iotss_internal_sram_0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
fvp_mps2.dma3.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.dma0	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
fvp_mps2.dma1	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
fvp_mps2.dma2	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.dma3	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
fvp_mps2.nmi_or_gate	OrGate	Or Gate.
fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.sse200.cpu0core_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.sse200	SSE200	SSE-200 subsystem.
fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.mpc_iotss_internal_ssram3.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.
fvp_mps2.mem_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
fvp_mps2.stub_spi2	RAMDevice	RAM device, can be dynamic or static ram.
fvp_mps2	FVP_MPS2	MPS2 DUT.
fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
top	FVP_MPS2_SSE_200_AEMv8M_pipeline	-
fvp_mps2.sse200.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
fvp_mps2.PSRAM	RAMDevice	RAM device, can be dynamic or static ram.
fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
cpu0	ARM_AEMv8M	ARM AEMv8M CT model.
cpu1	ARM_AEMv8M	ARM AEMv8M CT model.
fvp_mps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.dma2.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.dma3_securitymodifier	SecurityModifier	-
fvp_mps2.sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.spniden_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
fvp_mps2.dma1.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.
fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.svos_dualltimer.svos_dualltimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
fvp_mps2.svos_dualtimer	SVOS_DualTimer	-
fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
fvp_mps2.dma1.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
fvp_mps2.dma1_securitymodifier	SecurityModifier	-
fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
fvp_mps2.svos_dualltimer.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
fvp_mps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.

Table 6-10 FVP_MPS2_SSE-200_AEMv8M_pipeline instances (continued)

Name	Type	Description
fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.

6.11 FVP_MPS2_SSE-200_Cortex-M33

FVP_MPS2_SSE-200_Cortex-M33 contains the following instances:

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer0.clk_d1v1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer1.counte_r0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer0.clk_di_v0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2.timer.timer	ClockTimerThread4	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer2.clk_di_v1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer1.counte_r1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_switch_extra_psram_iotss	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cpu0core_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub_i2c1	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.spiden_or_gate	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.expansion_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO_connection_test.GPIO1_port_te_st	GPIO1_Connection_Test	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dbgen_or_gate	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.nmi_or_gate	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2 gpio_1_or_3	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cpu0dbg_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2.timer.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer3.counte_r0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer3.counte_r1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.exclusive_monitor_iotss_intern al_sram0	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.exclusive_monitor_iotss_intern al_sram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.exclusive_monitor_iotss_intern al_sram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.exclusive_monitor_iotss_intern al_sram3	PVBusExclusiveMonitor	Global exclusive monitor.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub_spi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.smsc_91c111	<i>SMSC_91C111</i>	SMSC 91C111 ethernet controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer0.counte r0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer0.counte r1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cmsdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SSE_200_Cortex_M33.clk25_khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33	FVP_MPS2_SSE_200_Cortex_M33	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1	PL080_DMAM	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mem_switch_ppu	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.clockdivider	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.cpu0	ARM_Cortex-M33	ARM CORTEXM33 CT model.
FVP_MPS2_SSE_200_Cortex_M33.cpu1	ARM_Cortex-M33	ARM CORTEXM33 CT model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.platform_bus_switch	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.ram2_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_switch_extra_psram_mmps2	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram3.gating_disabled_thread_event	SchedulerThreadEvent nt	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.spniden_or_gate	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1.timer.thread_event	SchedulerThreadEvent nt	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer2.counterv1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram1	<i>IoTSS_MemoryProtectionController</i>	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram0	<i>IoTSS_MemoryProtectionController</i>	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram3	<i>IoTSS_MemoryProtectionController</i>	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_sram2	<i>IoTSS_MemoryProtectionController</i>	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.clk25_Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_exclusive_monitor_zbtssram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer2.clk_dv0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_systemcontrol	IoTSS_SystemControl	IoT Subsystem System Control registers.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mem_switch_internal_ssram_mp_c	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mem_switch_internal_ssram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.mpc_iotss_internal_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.cmsdk_dultimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualtimer.svos_dualtimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_zbtsram2	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_zbtsram1	PVBusExclusiveMonitor	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.telnetterminal1	TelnetTerminal	Telnet terminal interface.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.exclusive_squasher	PVBusExclusiveSquasher	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.s32k_timer.counter	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub_spi2	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_internal_sram0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_internal_sram1	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_internal_sram2	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_internal_sram3	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_cmsdk_dualltimer.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_cmsdk_dualltimer.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.PSRAM_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-11 FVP_MPS2_SSE-200_Cortex-M33 instances (continued)

Name	Type	Description
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.dbg_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma2.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.sse200.crypto_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.niden_or_gate	OrGate	Or Gate.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.svos_dualltimer.svos_dualltimer2.counte_r0	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SSE_200_Cortex_M33.fvp_m_ps2.dma1_idau_labeller	LabellerIdauSecurity	-

6.12 FVP_MPS2_SecurCore-SC000

FVP_MPS2_SecurCore-SC000 contains the following instances:

Table 6-12 FVP_MPS2_SecurCore-SC000 instances

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0	<i>PL080_DMAC</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_cmsdk_dualtimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_SecurCore_SC000.fvp_mps2.hostbridge	<i>HostBridge</i>	Host Socket Interface Component.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.spniden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cmsdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2 uart_overflows_or_gate	<i>OrGate</i>	Or Gate.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_SecurCore_SC000.fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.expansion_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_exclusive_monitor_zbtssram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_exclusive_monitor_zbtssram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	<i>IoTSS_PeripheralProtectionController</i>	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	<i>IoTSS_PeripheralProtectionController</i>	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.PSRAM	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub_spi2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.PSRAM_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.ram2_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1_securitymodifier	<i>SecurityModifier</i>	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO_connection_test	<i>GPIO_Connection_Test</i>	-

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC000.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.clk25khz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cpu1core_ppu	<i>PPUV0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0.timer.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.ahb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.ahb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_cmsdk_dualltimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_cmsdk_dualltimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma1.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2	FVP_MPS2	MPS2 DUT.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000	FVP_MPS2_SecurCore_SC000	-
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC000.fvp_mps2 gpio_0_or_2	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.armsc000ct	ARM_SC000	ARM SC000 CT model.
FVP_MPS2_SecurCore_SC000.dap_buslogger	PVBusLogger	Bus Logger.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div1	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SecurCore_SC000.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter1	CounterModule	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.smse_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.dbg_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub_i2s	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC000.fvp_mps2.stub_spi0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma0.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.pl022_ssp_mps2.prescaler	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma3.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.iotss_systemcontrol	<i>IoTSS_SystemControl</i>	IoT Subsystem System Control registers.
FVP_MPS2_SecurCore_SC000.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC000.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC000.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer3	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer2	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer0	<i>CMSDK_DualTimer</i>	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.fpga_sysctrl	<i>FPGA_SysCtrl</i>	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer1	<i>CMSDK_Timer</i>	ARM Timer Module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.svos_dualltimer.svos_dualltimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.s32k_watchdog	<i>CMSDK_Watchdog</i>	ARM Watchdog Module.

Table 6-12 FVP_MPS2_SecurCore-SC000 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC000.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC000.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.

6.13 FVP_MPS2_SecurCore-SC300

FVP_MPS2_SecurCore-SC300 contains the following instances:

Table 6-13 FVP_MPS2_SecurCore-SC300 instances

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cordio_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.spiden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualtimer.svos_dualtimer3.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mem_switch_internal_sram	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.ram0_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_switch_extra_psram_io_tss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.clock32kHz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SecurCore_SC300.fvp_mps2	FVP_MPS2	MPS2 DUT.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer1.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART2	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART1	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART0	CMSDK_UART	ARM CMSDK UART Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_systeminfo	IoTSS_SystemInfo	IoT Subsystem System Information registers.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.nonsecure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.nmi_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.apb_ppc_iotss_expansion2	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.apb_ppc_iotss_expansion0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.apb_ppc_iotss_expansion1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_internal_sram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_internal_sram3	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_internal_sram0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_internal_sram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.ram3_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dbgen_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_systemcontrol	<i>IoTSS_SystemControl</i>	IoT Subsystem System Control registers.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.s32k_timer.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer1.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.ahb_ppc_iotss_expansion0	<i>IoTSS_PeripheralProtectionController</i>	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.ahb_ppc_iotss_expansion1	<i>IoTSS_PeripheralProtectionController</i>	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mem_switch_ppu	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2.timer.timer	<i>ClockTimerThread4</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.clock50Hz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer2.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mem_switch_internal_sram_mpc	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.signal_router	SignalRouter	Signal router.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cpu1core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram3	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram0	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.exclusive_monitor_iotss_internal_sram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART1.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.armsc300ct	ARM_SC300	ARM SC300 CT model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cpu1dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.stub_i2s	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.stub_i2c1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.telnetterminal1	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.niden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.telnetterminal0	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC300.fvp_mps2.fpga_sysctrl.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mem_switch_extra_psram_iotss	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.clk25Mhz	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer	SVOS_DualTimer	-

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200	SSE200	SSE-200 subsystem.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_switch_extra_psram_mps2	PVBusRouter	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.pl022_ssp_mps2.prescaler	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.expansion_warning_memory	WarningMemory	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0.timer	ClockTimerThread	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.PSRAM	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.stub_spi2	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.stub_spi0	RAMDevice	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1.timer.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.clk25khz	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2_idau_labeller	LabellerIdauSecurity	-

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram2.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_psram_iotss	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.bus_error_warning_memory	<i>WarningMemory</i>	Memory that prints warnings, and RAZ/WIs or aborts.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mhu0	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mhu1	IoTSS_MessageHandlingUnit	IoT Subsystem Message Handling Unit.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.cpu_wait_or_gate_1	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.cpu_wait_or_gate_0	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART0.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.apb_ppc_iotss_subsystem0	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.apb_ppc_iotss_subsystem1	IoTSS_PeripheralProtectionController	IoT Subsystem Peripheral Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.s32k_timer.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO_connection_test.GPIO1_port_test	GPIO1_Connection_Test	-

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram1.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.gpio_1_or_3	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.VGA_interface	MPS2_VGA	VGA display interface between main bus and visualisation.
FVP_MPS2_SecurCore_SC300.fvp_mps2.platform_switch_dma1	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.platform_switch_dma0	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer0.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram0	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.timer1.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.clockdivider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.s32k_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.UART2.clk_divider	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_visualisation	MPS2_Visualisation	Display window for MPS2 using Visualisation library.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.sys_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cmsdk_dualltimer.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.telnetterminal2	<i>TelnetTerminal</i>	Telnet terminal interface.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.ram1_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer0.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mem_switch_extra_psram_mps2	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.timer0.clk_div	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.cmsdk_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram0.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram3.gating_disabled_thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.PSRAM_M7	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.fpga_sysctrl.callBack100HzCounter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.crypto_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.timer1.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cpu0dbg_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.touchescreen_interface	MPS2_TouchScreen	MPS2 Touch Screen.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.cpu0core_ppu	<i>PPUv0</i>	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.ssram2	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.ssram1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.dap_buslogger	<i>PVBusLogger</i>	Bus Logger.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_psram	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.switch_svos_dualltimer	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.platform_bus_switch	<i>PVBusRouter</i>	Allow transactions to be routed arbitrarily.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer3.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1.timer	<i>ClockTimerThread</i>	A ClockTimerThread(64) is a drop-in replacement for a ClockTimer(64) component. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.fpga_sysctrl	FPGA_SysCtrl	FPGA SysCtrl timers LEDs and switches.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_zbtsram1	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_cmsdk_dualltimer.counter0	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_monitor_zbtsram2	<i>PVBusExclusiveMonitor</i>	Global exclusive monitor.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer2.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_cmsdk_dualltimer	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2	<i>PL080_DMAM</i>	ARM PrimeCell DMA Controller(PL080/081).

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3	PL080_DMAC	ARM PrimeCell DMA Controller(PL080/081).
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram2	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mpc_iotss_ssram3	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.mpc_iotss_internal_sram1	IoTSS_MemoryProtectionController	IoT Subsystem Memory Protection Controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.hostbridge	HostBridge	Host Socket Interface Component.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3.timer.thread_event	SchedulerThreadEvent	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3.timer.thread	SchedulerThread	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC300.fvp_mps2.smse_91c111	SMSC_91C111	SMSC 91C111 ethernet controller.
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO_connection_test	GPIO_Connection_Test	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.gpio_0_or_2	OrGate	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.nmi_or_gate	OrGate	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma3.timer.timer	ClockTimerThread64	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.ram2_ppu	PPUv0	ARM Power Policy Unit (PPU) architectural model.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_timer0.clk_div	ClockDivider	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO_connection_test.GPIO0_port_trans	GPIO_Port_Transfer	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_sram2	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_sram3	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_sram0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_sram1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma2.timer.thread_event	<i>SchedulerThreadEvent</i>	A SchedulerThreadEvent instance is an auto-reset boolean condition variable other threads can wait on.
FVP_MPS2_SecurCore_SC300.fvp_mps2.exclusive_squasher	<i>PVBusExclusiveSquasher</i>	Squashes the exclusive attribute on bus transactions.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_audio	MPS2_Audio	MPS2 Audio.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_secure_control_register_block	MPS2_SecureCtrl	MPS2 Secure Control Register Block.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma0_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.s32k_timer	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.secure_watchdog	CMSDK_Watchdog	ARM Watchdog Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This mean that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.iotss_cpuidentity	IoTSS_CPUIdentity	IoT Subsystem CPU_IDENTITY registers.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer0	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer1	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer2	CMSDK_DualTimer	ARM Dual-Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2.svos_dualltimer.svos_dualltimer3	CMSDK_DualTimer	ARM Dual-Timer Module.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2_uart_overflows_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2_GPIO1	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC300.fvp_mps2_dma2.timer.timer.thread	<i>SchedulerThread</i>	A SchedulerThread instance represents a co-routine thread in the simulation.
FVP_MPS2_SecurCore_SC300.fvp_mps2_sse200.timer0.counter	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2_stub1	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2_stub0	<i>RAMDevice</i>	RAM device, can be dynamic or static ram.
FVP_MPS2_SecurCore_SC300.fvp_mps2_dma1_idau_labeller	LabellerIdauSecurity	-
FVP_MPS2_SecurCore_SC300.fvp_mps2_pl022_ssp_mps2	PL022_SSP_MPS2	ARM PrimeCell Synchronous Serial Port(PL022).
FVP_MPS2_SecurCore_SC300.fvp_mps2_sse200.signal_router	SignalRouter	Signal router.
FVP_MPS2_SecurCore_SC300.fvp_mps2_spniden_or_gate	<i>OrGate</i>	Or Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2_cmsdk_sysctrl	CMSDK_SysCtrl	Cortex-M Simple System Control.
FVP_MPS2_SecurCore_SC300.fvp_mps2_svos_dualltimer.svos_dualltimer0.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.
FVP_MPS2_SecurCore_SC300.fvp_mps2_mps2_timer1	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2_mps2_timer0	CMSDK_Timer	ARM Timer Module.
FVP_MPS2_SecurCore_SC300.fvp_mps2_dma0.timer.timer	<i>ClockTimerThread64</i>	A ClockTimerThread64 is a drop-in replacement for ClockTimer64. The main difference to the ClockTimer component is that the ClockTimerThread runs the signal() callback from a proper scheduler thread. This means that the signal() function may directly or indirectly invoke wait() functions to wait for time or events. This is not allowed for the ClockTimer component which does not use a thread. Components which issue bus transactions from within the timer signal() callback must use ClockTimerThread(64) rather than ClockTimer(64).
FVP_MPS2_SecurCore_SC300.fvp_mps2_svos_dualltimer.svos_dualltimer1.counter1	<i>CounterModule</i>	Internal component used by SP804 Timer module.

Table 6-13 FVP_MPS2_SecurCore-SC300 instances (continued)

Name	Type	Description
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_cmsdk_dualtimer.clk_div0	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_cmsdk_dualtimer.clk_div1	<i>ClockDivider</i>	A ClockDivider is a library component that takes a ClockSignal on its input port (which could come from the output of a MasterClock, or from another ClockDivider), and generates a new ClockSignal on its output port, representing a clock frequency that is related to the input clock by the ratio of the multiply and divide parameters.
FVP_MPS2_SecurCore_SC300.fvp_mps2.mps2_lcd	MPS2_LCD	MPS2 LCD I2C interface.
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO0	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC300	FVP_MPS2_SecurCore_SC300	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO2	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC300.fvp_mps2.GPIO3	CMSDK_GPIO	ARM PrimeCell General Purpose Input/Output.
FVP_MPS2_SecurCore_SC300.fvp_mps2.dma1_securitymodifier	SecurityModifier	-
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_cpu0	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.
FVP_MPS2_SecurCore_SC300.fvp_mps2.sse200.acg_cpu1	IoTSS_AccessControlGate	IoT Subsystem Access Control Gate.