CS2100: Computer Organisation

Tutorial #7: Combinational Circuits

(Week 9: 16 – 20 March 2020)

Answers

Note that for questions on logic design, you may assume that logical constants 0 and 1 are always available. However, complemented literals are not available unless otherwise stated.

Tutorial questions

1. A certain circuit takes in a 4-bit unsigned binary number *ABCD*, and outputs a 2-bit binary number *EF* that is the result of the **input value modulo 3** (i.e. the remainder of the input value divided by 3).

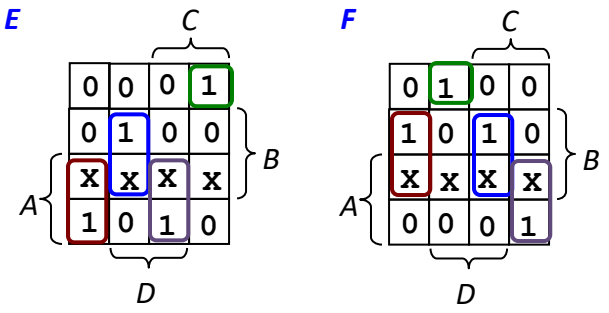
   For example, if *ABCD* is 1000 (which represents the decimal value 8), then the output *EF* is 10 (decimal value 2).

   You are also told that 1100, 1101, 1110 and 1111 will not appear as input to the circuit.

   Fill in the truth table below and express *E* and *F* in simplified SOP form.

   Based on your expressions for *E* and *F*, what would the output be if the following invalid inputs are fed into the circuit? (a) *ABCD* = 1100; (b) *ABCD* = 1101.

Inputs				Outputs	
A	***B***	***C***	***D***	***E***	***F***
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	1	0	0	1
1	0	1	1	1	0
1	1	0	0	X	X
1	1	0	1	X	X
1	1	1	0	X	X
1	1	1	1	X	X



Answers:

E = A·C'·D' + B·C'·D + A·C·D + A'·B'·C·D'

F = B·C'·D' + B·C·D + A·C·D' + A'·B'·C'·D

(a) If *ABCD* = 1100, then *EF* = **11**

(b) If *ABCD* = 1101, then *EF* = **10**

2. [AY2013/14 Semester 2 Exam Q8)

a. You want to construct a circuit that takes in a 4-bit unsigned binary number *ABCD* and outputs a 4-bit unsigned binary number *EFGH* where *EFGH* = (*ABCD* + 1) / 2. Note that the division is an integer division. For example, if *ABCD* = 0110 (or 6 in decimal), then *EFGH* = 0011 (or 3 in decimal). If *ABCD* = 1101 (or 13 in decimal), then *EFGH* = 0111 (or 7 in decimal).

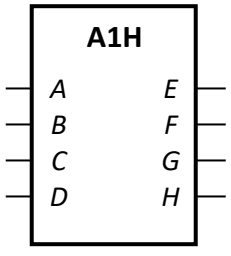
   Construct the above circuit using a single **4-bit parallel adder** and at most one logic gate with no restriction on its fan-in.

b. The following table shows the 4221 code and 8421 code (also known as BCD code) for the ten decimal digits 0 through 9.

Digit	4221 code	8421 code
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0110	0100
5	1001	0101
6	1100	0110
7	1101	0111
8	1110	1000
9	1111	1001

   You want to construct a 4221-to-8421 decimal code converter, which takes in a 4-bit 4221 decimal code *PQRS* and generates the corresponding 4-bit 8421 decimal code *WXYZ*.

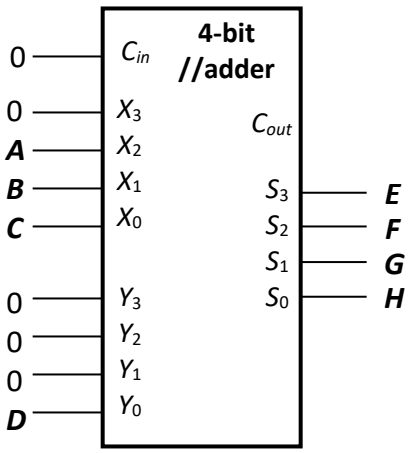
   Let's call the circuit you created in part (a) above the A1H (Add-1-then-Half) device, represented by the block diagram below. Implement your 4221-to-8421 decimal code converter using this A1H device with the fewest number of additional logic gates.



Answers:

2(a)

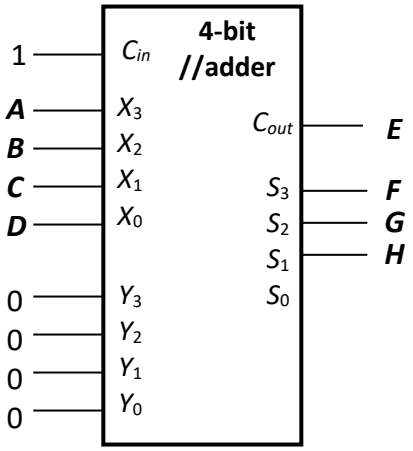
Solution 1:



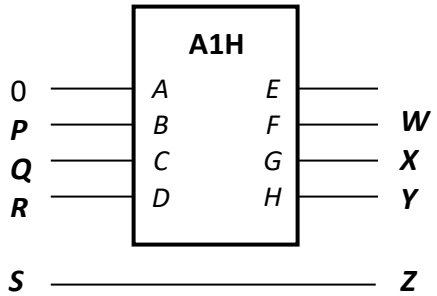
A	B	C	D	E	F	G	H
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	1	1
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	0
1	0	0	1	0	1	0	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	1	0
1	1	0	0	0	1	1	0
1	1	0	1	0	1	1	1
1	1	1	0	0	1	1	1
1	1	1	1	1	0	0	0

Solution 2:

Or $Y_0 = 1$; $C_{in} = 0$

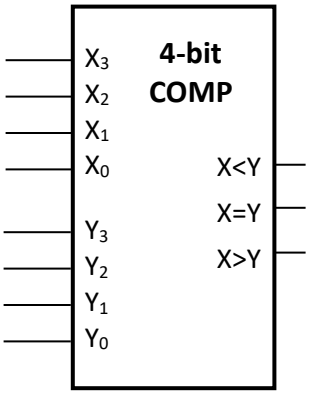


2(b)



P	Q	R	S	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	1	0	0	1	0	0
1	0	0	1	0	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	0	1	1	1
1	1	1	0	1	0	0	0
1	1	1	1	1	0	0	1

3. Given a 4-bit magnitude comparator as shown on the right, implement the following 4-variable Boolean functions using only this single magnitude comparator with no other logic gates. (Note that there could be multiple answers.)



(a) $F(A,B,C,D) = \Sigma m(12 - 15)$.

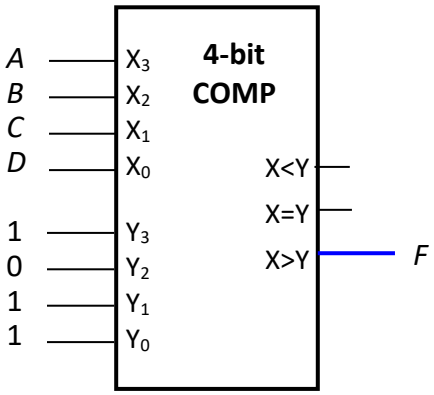
(b) $G(A,B,C,D) = \Sigma m(0, 6, 9, 15)$.

(c) $H(A,B,C,D) = \Sigma m(0, 1, 6, 7, 8, 9, 14, 15)$.

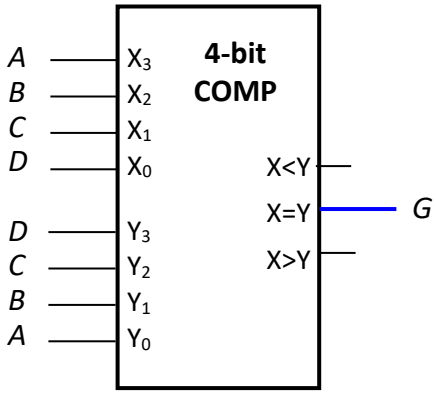
(d) $Z(A,B,C,D) = \Sigma m(1, 3, 5, 7, 9, 11, 13)$.

Answers:

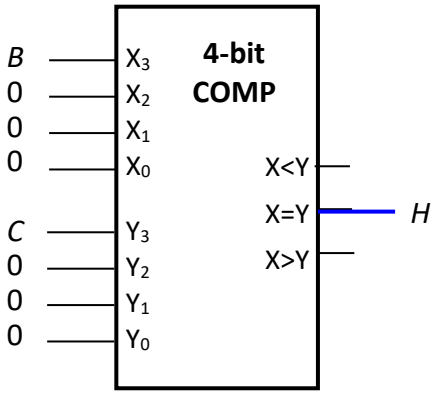
(a)



(b)

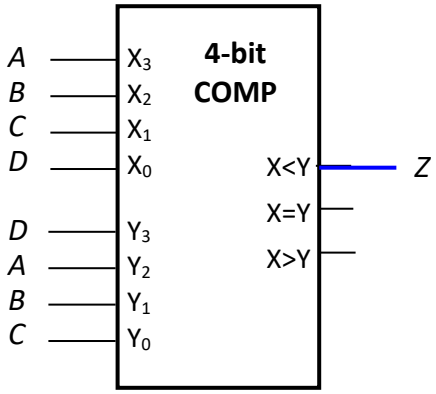


(c)



As long as $B = C$.

(d)



or (possibly other answers?)