CS2100 Computer Organisation

Tutorial #9: Sequential Circuits

(Week 11: 30 March – 3 April 2020)

Answers

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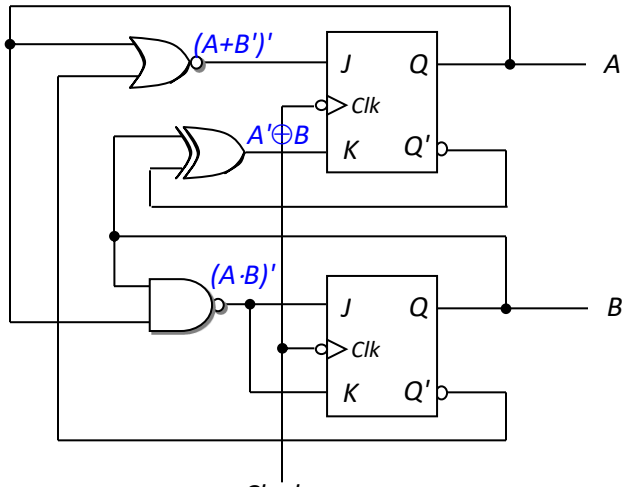
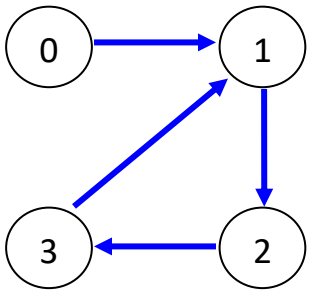
1. [AY2011/12 Semester 2 exam]
   The sequential circuit with state *AB* shown below contains two ***JK* flip-flops**. Complete the state table and hence draw the state diagram. In your state diagram, you may write the state values in binary or decimal.

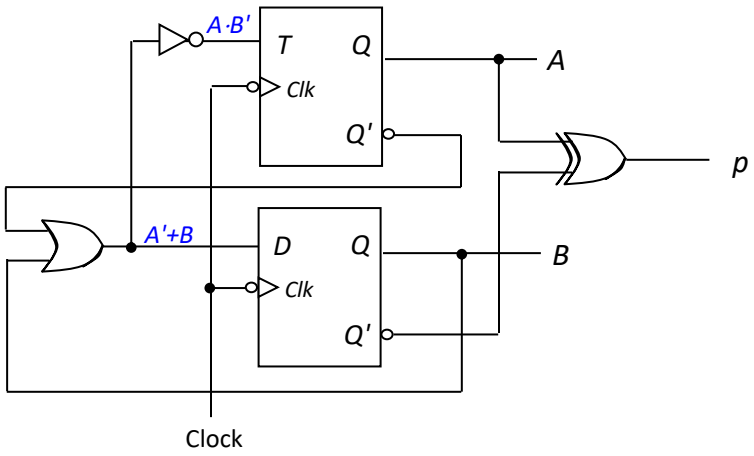


Answer:

Present state		Flip-flop inputs			Next state	
A	***B***	***JA = A'·B***	***KA = A'⊕B***	***JB=KB =(A·B)'***	A^+	B^+
0	0	0	1	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	1	0	1	0	0	1



2. A four-state sequential circuit below consists of a ***T* flip-flop** and a ***D* flip-flop**. Analyze the circuit.



(a) Complete the state table and hence draw the state diagram.
(b) Assuming that the circuit is initially at state 0, what is the final state and the outputs generated after 3 clock cycles?

A state is called a ***sink*** if once the circuit enters this state, it never moves out of that state.

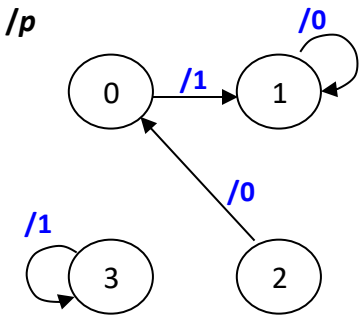
(c) How many sinks are there for this circuit?
(d) Which is likely to be an unused state in this circuit?

Answers:

(a)

$p = A \cdot B + A' \cdot B'$
$TA = A \cdot B'$
$DB = A' + B$

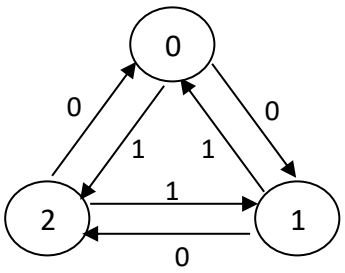
Present state		Output	Flip-flop inputs		Next state	
A	***B***	***p***	***TA***	***DB***	***A+***	***B+***
0	0	**1**	**0**	**1**	**0**	**1**
0	1	**0**	**0**	**1**	**0**	**1**
1	0	**0**	**1**	**0**	**0**	**0**
1	1	**1**	**0**	**1**	**1**	**1**



(b) After 3 clock cycles, the circuit is in state 1, and it generated 100 as output.
(c) There are 2 sinks: states 1 and 3.
(d) State 3 is likely to be an unused state.

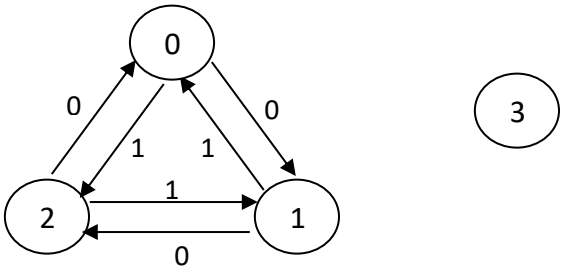
3. Given the state transition diagram on the right with states *AB* and input *x*, implement the circuit using ***JK* flip-flop**s and the fewest number of logic gates.

   Fill in the state table below and draw the circuit. You do not need to follow the simplest SOP expression in your implementation as that might not give you a circuit with the fewest logic gates.



Present state		Input	Next state		Flip-flop *A*		Flip-flop *B*	
A	***B***	***x***	A^+	B^+	***JA***	***KA***	***JB***	***KB***
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

State 3 is unused. Can you complete the following state diagram with the unused state?



A circuit is **self-correcting** if for some reason the circuit enters into any unused (invalid) state, it is able to transit to a valid state after a finite number of transitions. Is your circuit self-correcting, and why?

Answers:

Using K-maps to find simplified expressions for flip-flop inputs.

Present state		Input	Next state		Flip-flop *A*		Flip-flop *B*	
A	***B***	***x***	***A*⁺**	***B*⁺**	***JA***	***KA***	***JB***	***KB***
0	0	0	**0**	**1**	**0**	**d**	**1**	**d**
0	0	1	**1**	**0**	**1**	**d**	**0**	**d**
0	1	0	**1**	**0**	**1**	**d**	**d**	**1**
0	1	1	**0**	**0**	**0**	**d**	**d**	**1**
1	0	0	**0**	**0**	**d**	**1**	**0**	**d**
1	0	1	**0**	**1**	**d**	**1**	**1**	**d**
1	1	0	**d**	**d**	**d**	**d**	**d**	**d**
1	1	1	**d**	**d**	**d**	**d**	**d**	**d**

d = don't care

JB

A \ *Bx*	00	01	11	10
0	1	0	d	d
1	0	1	d	d

JA

A \ *Bx*	00	01	11	10
0	0	1	0	1
1	d	d	d	d

KA

A \ *Bx*	00	01	11	10
0	d	d	d	d
1	1	1	d	d

KB

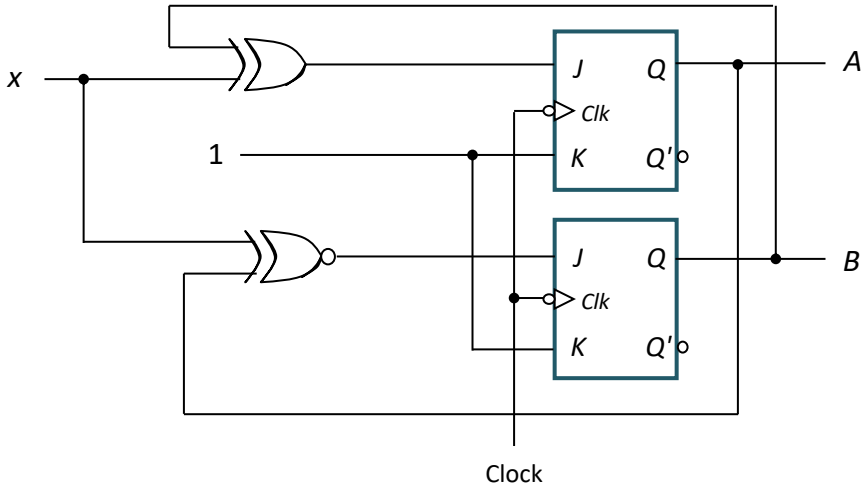
A \ *Bx*	00	01	11	10
0	d	d	1	1
1	d	d	d	d

JA = B·x′ + B′·x = B ⊕ x

KA = 1

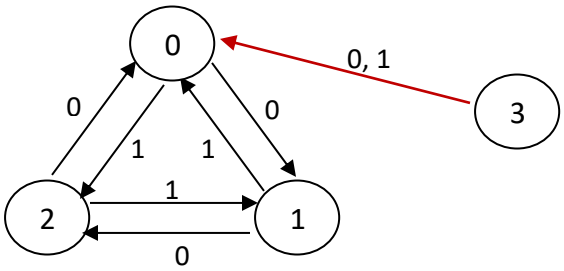
JB = A′·x′ + A·x = A ⊙ x

KB = 1

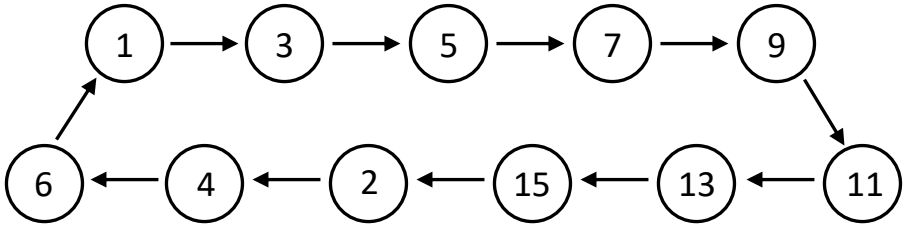


After committing the expressions for the flip-flop inputs, the don't-care values below are replaced with actual values (in parentheses). The state diagram with the unused state 3 is shown below. It is a self-correcting circuit, since there is an arrow out from state 3 to a used state.

Present state		Input	Next state		Flip-flop *A*		Flip-flop *B*	
A	***B***	***x***	A^+	B^+	***JA***	***KA***	***JB***	***KB***
0	0	0	**0**	**1**	**0**	**d(1)**	**1**	**d(1)**
0	0	1	**1**	**0**	**1**	**d(1)**	**0**	**d(1)**
0	1	0	**1**	**0**	**1**	**d(1)**	**d(1)**	**1**
0	1	1	**0**	**0**	**0**	**d(1)**	**d(0)**	**1**
1	0	0	**0**	**0**	**d(0)**	**1**	**0**	**d(1)**
1	0	1	**0**	**1**	**d(1)**	**1**	**1**	**d(1)**
1	1	0	**d(0)**	**d(0)**	**d(1)**	**d(1)**	**d(0)**	**d(1)**
1	1	1	**d(0)**	**d(0)**	**d(0)**	**d(1)**	**d(1)**	**d(1)**



4. [AY2018/19 Semester 2 exam]
   A sequential circuit goes through the following states, whose state values are shown in decimal:

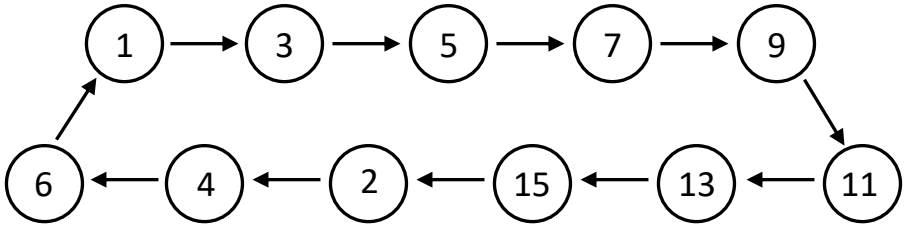


   The states are represented by 4-bit values *ABCD*. Implement the sequential circuit using a *D* flip-flop for *A*, *T* flip-flops for *B* and *C*, and a *JK* flip-flop for *D*.

   (a) Write out the **simplified SOP expressions** for all the flip-flop inputs.

   (b) Implement your circuit according to your simplified SOP expressions obtained in part (a). Complete the given state diagram, by indicating the next state for each of the five unused states.

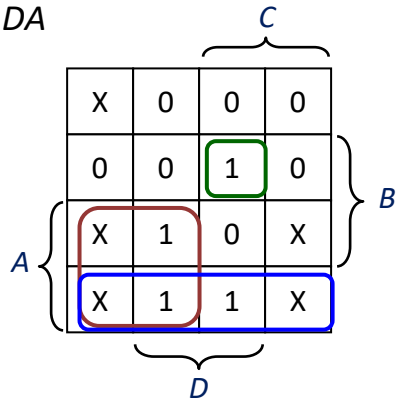
   (c) Is your circuit self-correcting? Why?



Answers:

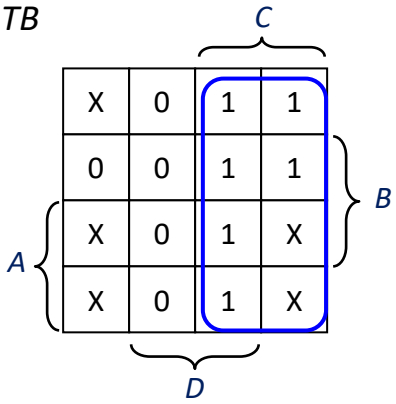
Current state				Next state							
A	*B*	*C*	*D*	$DA=A^+$	B^+	C^+	D^+	*TB*	*TC*	*JD*	*KD*
0	0	0	0	X(0)	X(0)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
0	0	0	1	0	0	1	1	0	1	X	0
0	0	1	0	0	1	0	0	1	1	0	X
0	0	1	1	0	1	0	1	1	1	X	0
0	1	0	0	0	1	1	0	0	1	0	X
0	1	0	1	0	1	1	1	0	1	X	0
0	1	1	0	0	0	0	1	1	1	1	X
0	1	1	1	1	0	0	1	1	1	X	0
1	0	0	0	X(1)	X(0)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
1	0	0	1	1	0	1	1	0	1	X	0
1	0	1	0	X(1)	X(1)	X(0)	X(0)	X(1)	X(1)	X(0)	X(0)
1	0	1	1	1	1	0	1	1	1	X	0
1	1	0	0	X(1)	X(1)	X(1)	X(0)	X(0)	X(1)	X(0)	X(0)
1	1	0	1	1	1	1	1	0	1	X	0
1	1	1	0	X(0)	X(0)	X(1)	X(1)	X(1)	X(0)	X(1)	X(1)
1	1	1	1	0	0	1	0	1	0	X	1

DA



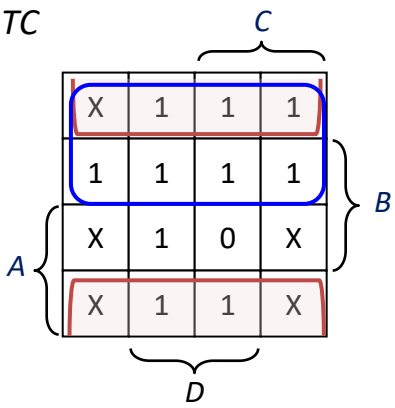
$DA = A \cdot B' + A \cdot C' + A' \cdot B \cdot C \cdot D$

TB



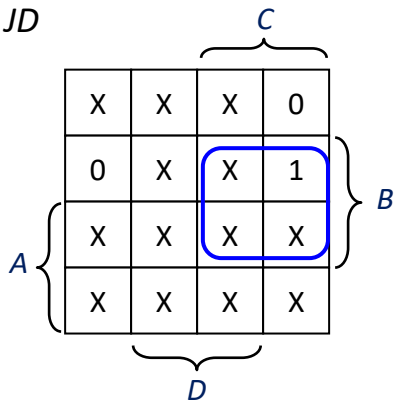
$TB = C$

TC



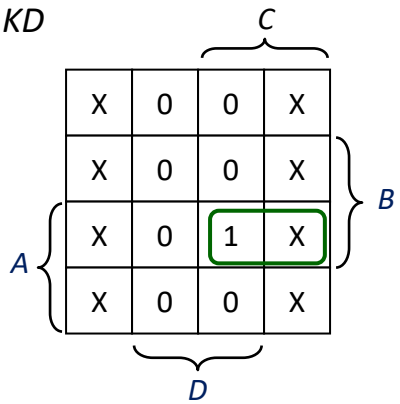
$TC = A' + B' + C'$

JD



$JD = B \cdot C$

KD



$KD = A \cdot B \cdot C$

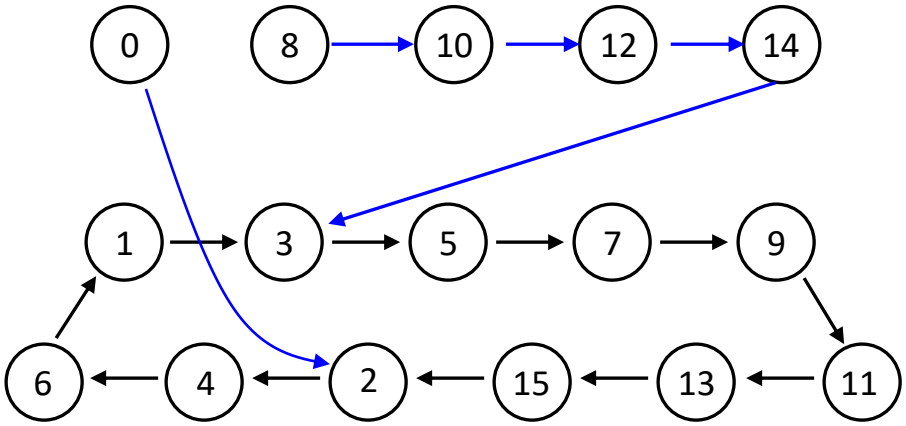
DA = ***A·B′ + A·C′ + A′·B·C·D***

TB = ***C***

TC = ***A′ + B′ + C′***

JD = ***B·C***

KD = ***A·B·C***



The circuit is self-correcting as any unused state can transit to a used state after a finite number of cycles.