CS2100: Computer Organisation

Tutorial #7: Combinational Circuits

(Week 9: 16 – 20 March 2020)

Note that for questions on logic design, you may assume that logical constants 0 and 1 are always available. However, complemented literals are not available unless otherwise stated.

LumiNUS Discussion Questions

D1. Design a circuit, without using any logic gate, that takes a 3-bit input *ABC* representing an unsigned integer *x*, and produces a 5-bit output *VWXYZ* which is equivalent to 4*x*+2. What are *V*, *W*, *X*, *Y* and *Z*?

D2. The following algorithm to convert binary to standard Gray code sequence is given in Digital Logic Design page 35:

1. Retain the MSB.
2. From left to right, add each adjacent pair of binary code bits to get the next Gray code bit, discarding the carry.

The following example shows the conversion of binary number $(10110)_2$ to its corresponding standard Gray code value, $(11101)_{\text{Gray}}$.

$$\boxed{\begin{array}{cccccc} 1 & 0 & 1 & 1 & 0 & \text{Binary} \\ \downarrow & & & & & \\ \mathbf{1} & & & & & \text{Gray} \end{array}}$$

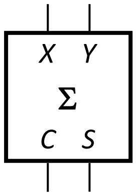
$$\boxed{\begin{array}{ccccccc} \underline{1} & + & \underline{0} & 1 & 1 & 0 & \text{Binary} \\ & & \downarrow & & & & \\ 1 & & \mathbf{1} & & & & \text{Gray} \end{array}}$$

$$\boxed{\begin{array}{ccccccc} 1 & \underline{0} & + & \underline{1} & 1 & 0 & \text{Binary} \\ & & & \downarrow & & & \\ 1 & 1 & & \mathbf{1} & & & \text{Gray} \end{array}}$$

$$\boxed{\begin{array}{ccccccc} 1 & 0 & \underline{1} & + & \underline{1} & 0 & \text{Binary} \\ & & & & \downarrow & & \\ 1 & 1 & 1 & & \mathbf{0} & & \text{Gray} \end{array}}$$

$$\boxed{\begin{array}{ccccccc} 1 & 0 & 1 & \underline{1} & + & \underline{0} & \text{Binary} \\ & & & & & \downarrow & \\ 1 & 1 & 1 & 0 & & \mathbf{1} & \text{Gray} \end{array}}$$

Given a half-adder as shown on the right where *X* and *Y* are its inputs and *C* (carry) and *S* (sum) its outputs, implement a 5-bit binary to Gray code converter to convert the binary value *ABCDE* to its equivalent Gray code *PQRST* by using the fewest number of half-adders without any additional logic gates.



Tutorial questions

1. A certain circuit takes in a 4-bit unsigned binary number *ABCD*, and outputs a 2-bit binary number *EF* that is the result of the **input value modulo 3** (i.e. the remainder of the input value divided by 3).

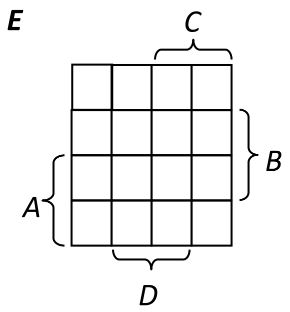
   For example, if *ABCD* is 1000 (which represents the decimal value 8), then the output *EF* is 10 (decimal value 2).

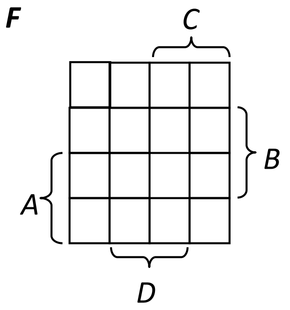
   You are also told that 1100, 1101, 1110 and 1111 will not appear as input to the circuit.

   Fill in the truth table below and express *E* and *F* in simplified SOP form.

   Based on your expressions for *E* and *F*, what would the output be if the following invalid inputs are fed into the circuit? (a) *ABCD* = 1100; (b) *ABCD* = 1101.

Inputs				Outputs	
A	***B***	***C***	***D***	***E***	***F***
0	0	0	0		
0	0	0	1		
0	0	1	0		
0	0	1	1		
0	1	0	0		
0	1	0	1		
0	1	1	0		
0	1	1	1		
1	0	0	0		
1	0	0	1		
1	0	1	0		
1	0	1	1		
1	1	0	0		
1	1	0	1		
1	1	1	0		
1	1	1	1		





2. [AY2013/14 Semester 2 Exam Q8)

   a. You want to construct a circuit that takes in a 4-bit unsigned binary number *ABCD* and outputs a 4-bit unsigned binary number *EFGH* where *EFGH* = (*ABCD* + 1) / 2. Note that the division is an integer division. For example, if *ABCD* = 0110 (or 6 in decimal), then *EFGH* = 0011 (or 3 in decimal). If *ABCD* = 1101 (or 13 in decimal), then *EFGH* = 0111 (or 7 in decimal).

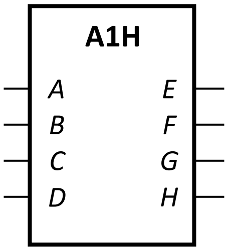
      Construct the above circuit using a single **4-bit parallel adder** and at most one logic gate with no restriction on its fan-in.

   b. The following table shows the 4221 code and 8421 code (also known as BCD code) for the ten decimal digits 0 through 9.

Digit	4221 code	8421 code
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0110	0100
5	1001	0101
6	1100	0110
7	1101	0111
8	1110	1000
9	1111	1001

You want to construct a 4221-to-8421 decimal code converter, which takes in a 4-bit 4221 decimal code *PQRS* and generates the corresponding 4-bit 8421 decimal code *WXYZ*.

Let's call the circuit you created in part (a) above the A1H (Add-1-then-Half) device, represented by the block diagram below. Implement your 4221-to-8421 decimal code converter using this A1H device with the fewest number of additional logic gates.



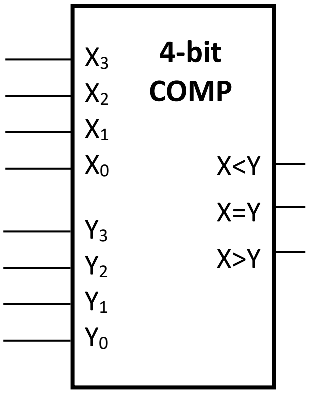
3. Given a 4-bit magnitude comparator as shown on the right, implement the following 4-variable Boolean functions using only this single magnitude comparator with no other logic gates. (Note that there could be multiple answers.)

   (a) $F(A,B,C,D) = \Sigma m(12 - 15)$.

   (b) $G(A,B,C,D) = \Sigma m(0, 6, 9, 15)$.

   (c) $H(A,B,C,D) = \Sigma m(0, 1, 6, 7, 8, 9, 14, 15)$.

   (d) $Z(A,B,C,D) = \Sigma m(1, 3, 5, 7, 9, 11, 13)$.


4-bit COMP
X3
X2
X1
X0
Y3
Y2
Y1
Y0
X<Y
X=Y
X>Y