SCALING A RECONFIGURABLE DATAFLOW ACCELERATOR

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Abstract

With the slowdown of Moore's Law, specialized hardware accelerators are gaining tractions for delivering 100-1000x performance improvement over general-purpose processors in a variety of applications domains, such as cloud computing, biocomputing, artificial intelligence, etc. [1, 2, 3]. As the performance scaling in multicores is coming to a limit [4], a new class of accelerators–reconfigurable dataflow architectures (RDAs)–is promising in offering high-throughput and energy-efficient acceleration that keeps up with the performance demand. Instead of dynamically fetching instructions like in traditional processors, RDAs have flexible datapath that can be statically configured to spatially parallelize and pipeline the program across distributed on-chip resources. The pipelined execution model and explicitly-managed scratchpad in RDAs eliminate the performance, area, and energy overhead in dynamic scheduling and conventional memory hierarchy.

To adapt to the compute intensity in modern data-analytic workloads, particularly in the deep learning domain, RDAs are increasing to a scale that was unprecedented before. With an area footprint of 133mm^2 at 28nm, Plasticine is a hierarchical RDA supplying 12.3 TFLOPs of computing power [5]. Prior work has shown an up to 76x performance/watt benefit from Plasticine over a Stradix V FPGA due to an advantage in clock frequency and resource density. The increase in scale introduces new challenges in network-on-chip design to maintain the throughput and energy efficiency of RDAs. Furthermore, targeting and managing RDAs at this scale also require new strategies in mapping, memory management, and flexible control to fully utilize their compute power.

In this work, we focus on two aspects of the software-hardware co-design that impact the usability and scalability of the Plasticine accelerator. Although RDAs are flexible to support a wide range of applications, the biggest challenge that hinders the adoption of these accelerators is the required low-level knowledge in microarchitecture design and hardware constraints in order to efficiently implement a new application. To address this challenge, we introduce a compiler stack–SARA–that raises the programming abstraction of Plasticine to an imperative-style domain-specific language

(DSL) with nested control flow for general spatial architectures. Besides architecture-agnostic, this abstraction contains explicit loop constructs, enabling cross-kernel optimizations that are often not explored when programming RDAs. SARA efficiently translates imperative control constructs to a streaming dataflow graph that scale performance with distributed on-chip resources. By virutalizing resources, SARA systematically handles the physical constraints, hiding the low-level physical limitations from the programmers. To address the scalability challenge with increasing chip sizes in RDAs, we present a comprehensive study on the network-on-chip design space for RDAs [6]. We found that network performance highly correlates to network bandwidth, as supposed to latency, for RDAs with streaming dataflow execution model. Lastly, we show that a static-dynamic hybrid network design can sustain performance in a scalable fashion with high energy efficiency.

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I would like to thank my mother and the little green men from Mars.

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Chapter 1

Introduction (WIP)

1.1 The Rising of Hardware Acceleration

With the end of Dennard Scaling [7], the amount of performance one can extract from a CPU is reaching a limit. To provide general-purpose flexibility, CPUs spend the majority of resources and energy on overheads, including dynamic-instruction fetching and decoding, branch prediction, and a cache hierarchy, etc., with less than 20% of the energy on the actual computation [8]. Even worse, power wall is limiting the entire multicore family to reach the doubled performance per generation scaling enabled by technology scaling in the past [4].

For this reason, hardware acceleration is emerging in various compute-intensive application domains to provide orders of magnitude acceleration, enabling algorithms that were otherwise infeasible [3, 2, 9, 10]. Examples include widely adopted General-Purpose Graphics Processing Units (GPGPUs) in computational genomics, signal processing, graph processing, and deep learning, etc. [3, 2, 1]. Moreover, many recent efforts are spent on leveraging application domain knowledge in hardware design to enable continued performance scaling while meeting the power budget [11]. As artificial intelligence receiving great success in industry and business, past years have seen a growing interest in machine learning accelerators; these accelerators contain specialized circuits for ML kernels that dramatically improve the compute efficiency [12, 13, 14, 15, 16, 17].

Nonetheless, it is non-trivial to achieve good utilization of these accelerators. While the peak FLOPS of GPU has increased by over 20x in the past 10 years, the achievable FLOPS is not increasing accordingly [18, 19]. The massive threads in GPU require embarrassedly parallel workloads to

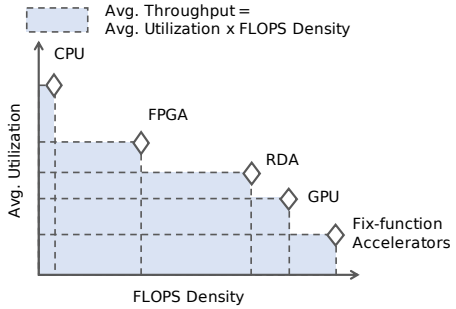


Figure 1.1: Tradeoff between the average utilization of the peak FLOPS over a range of applications vs. the peak compute density among different architectures. The shaded area indicates the effective FLOPS achieved. With all the dynamic scheduling hardware in CPUs, such as prefetching and branch prediction, CPU can achieve a fairly decent instruction per cycle (IPC) for data-analytic workloads that have a regular control flow. However, overheads to support flexibility, security, and programmability in CPU result in a low FLOPS density. While GPU and fix-function accelerators have a high FLOPS density, they are prone to underutilization due to variation in application characteristics. Fine-grained reconfigurable datapath makes it easy to utilize on-chip resources of an FPGA. However, the soft logics and overheads in routing resources lead to a low resource density and clock frequency. RDAs have the right balance between flexibility and efficiency, which gives a good overall average utilization.

fully saturate the compute throughput. GPU's bulk-synchronous nature also causes poor cache efficiency; data are spilled off-chip before getting reused [20]. On the outer hand, while extremely efficient for certain models, machine learning accelerators are highly specialized for specific kernels, especially general matrix multiply (GEMM) and convolution. However, ML algorithms evolve much faster than the development and manufacture cycle of hardware, leading to inefficiency or even unsupported applications. For example, hybrid models, such as Mask R-CNN [21] and DeepLab [22], contain combinations of GEMM-compatible and incompatible operations, both computationally expensive. Fix-functional accelerators focusing on GEMM operations, such as TPU [13], have to rely on CPUs for unsupported operations or convert non-GEMM operations to GEMM operations, resulting in a severe performance gap between the peak and effective FLOPS [23]. Figure 1.1 illustrate a tradeoff between average utilization of the peak FLOPS over a range of data and the peak FLOPS available on the hardware.

Reconfigurable spatial architectures overcome this limitation by changing its datapath based on applications' needs. Applications are configured at the circuit-level without dynamic instruction fetching and decoding, hence improving energy-efficiency [24, 25]. In addition to instruction, data, and task-level parallelism explored by processor architectures, spatial architectures also explore instruction and task-level pipelining that further increase the compute throughput [26]. Exploring

Architectures	DySER [36]	TI [41]	revel [49]	Plasticine [5]	Gorgon [46]
OPS	128GOPS	64GOPS	300GOPS	12.3TFLOPS	38.4TFLOPS

Table 1.1: OPS comparison of different CGRAs. Gorgon is a Plasticine variant proposed for joint machine learning and database acceleration.

pipeline parallelism enables spatial architectures to achieve a high-throughput without massively parallelize every stage of the program. Flexible datapath also permits resource distribution proportional to the compute intensity of program stages. A key performance optimization on reconfigurable accelerators is an application-level design space exploration searching for the best resource distribution scheme that balances the compute pipeline [27].

One of the mainstream reconfigurable spatial architecture is Field Programmable Gate Arrays (FPGAs) that support fine-grain, bit-level reconfigurability with a soft logic fabric [28]. The flexible interconnect and lookup table-based logic gate can be configured to implement arbitrary datapath. FPGAs have been used to deploy services commercially [29, 30, 31] and can be rented on the AWS F1 cloud [32]. Although around for a long time, FPGAs are not broadly accepted among high-level application programmers due to their low-level programming interface and long compilation time. Fine-tuning applications on FPGAs require expertise in digital design and takes a long development cycle, which hinder their accessibility to the general software community. As an application-level accelerator, FPGAs also suffer from overhead in fine-grained reconfigurability; studies have shown that over 60% of the chip area of an FPGA is spent on routing resources [33, 24, 25].

In contrast to fine-grained reconfigurable architectures, Coarse-Grained Reconfigurable Arrays (CGRAs) are spatial architectures with coarse-grained building blocks, such as ALUs, register files, and memory controllers, distributed in a programmable, word or vector-level static interconnect [34, 35, 36, 37, 38, 39, 40]. We refer a subclass of CGRAs with dataflow-driven execution model as Reconfigurable Dataflow Architectures (RDAs)[1] [5, 41, 42, 43, 44, 45]. Lately, RDAs are emerging as a new class of spatial accelerators that retain the desired level of flexibility and energy efficiency without the area overhead and low clock frequency of bit-level reconfigurability. Our previously proposed RDA–Plasticine–has demonstrated a promising acceleration of dense, sparse, database, and streaming applications [5, 46, 47, 48]. To meet the computing demand of recent data-analytic workload, Plasticine is a large-scale RDA compared to traditional CGRAs. Table 1.1 shows the OPS comparison across a few CGRAs proposed in the prior works.

[1] Dataflow overlay architectures on FPGA are technically also RDAs, which are not the primary concern in the discussion of this work.

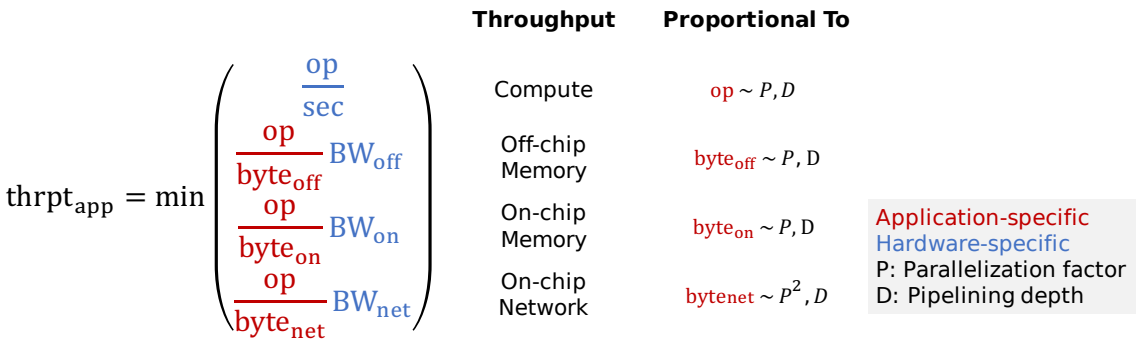


Figure 1.2: High-level performance model of a spatial architecture.

The scale of Plasticine introduces challenges in network-on-chip design to sustain bandwidth requirements while staying energy-efficient. The compilation strategy also needs to explore multiple-levels of concurrency in the program to saturate the compute throughput of the large-scale RDA; this strategy must introduce minimum synchronization overhead to maximize the scalability of the mapped design.

1.2 The Need for Flexible Interconnects

Applications are mapped to RDAs by distributing computations spatially across multiple processing blocks and executing them in a pipelined, data-driven fashion. In traditional Networks-on-Chip (NoCs) for multicore systems, communication is the result of explicit message passing between parallel workers or cache misses that generate messages for coherence protocol; these traffic are bursty and relatively infrequent. On RDAs, however, applications are distributed by parallelizing and pipelining; pipelining introduces frequent and throughput-sensitive communication. Applications with different characteristics, such as compute vs. memory-bound, also exhibit very different communication patterns.

Figure 1.2 shows a high-level performance model of a spatially pipelined and parallelized reconfigurable architecture. Due to pipelined execution, the performance of a spatial architecture is dominant by throughput as supposed to latency. Compute, on and off-chip memory accesses, and network become a integrated pipeline; overall performance is limited by the pipeline stage with lowest throughput. The red terms in the equation are application-specific and capture the compute, memory, or IO-bound characteristics. The blue terms are the bandwidth and FLOPS available on

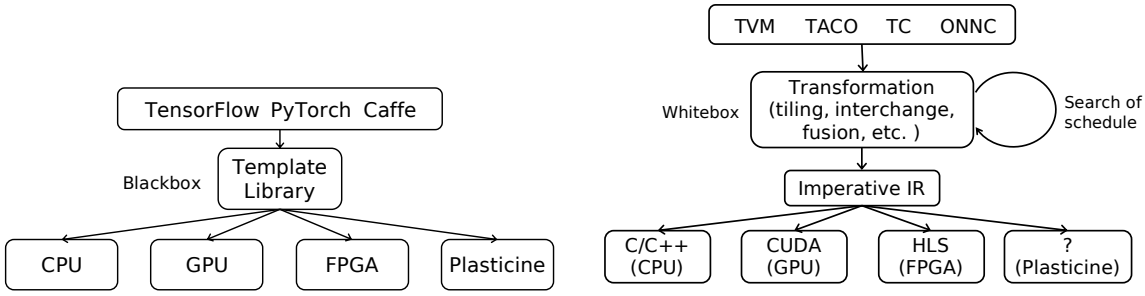
the hardware. While the compute and memory access in application increases linearly with parallelization factor and pipelining depth, the required network bandwidth from application increases quadratically with increasing parallelism. This means as we going to larger chip size, the network bandwidth must grow super linearly to achieve a perfect performance scaling, unless exploring pipeline parallelism.

RDAs need the right amount of interconnect flexibility to achieve good resource utilization; an inflexible interconnect constrains the space of valid application mappings and hinders resource utilization. Furthermore, in the quest to increase compute density, RDA data paths now contain increasingly coarse-grained processing blocks such as pipelined, vectorized functional units [5, 37, 50]. Plasticine, as an example, has a 512-bit vector bus, which necessitates coarser communication and higher on-chip interconnect bandwidth to avoid creating performance bottlenecks. Although many hardware accelerators with large, vectorized data paths have fixed local networks [51], there is a need for more flexible global networks to adapt to future applications. Consequently, interconnect design for these RDAs involves achieving a balance between the often conflicting requirements of high bandwidth and high flexibility.

1.3 The Gap between High-Level DSLs and Dataflow Accelerators

Recent years have seen an explosion of hardware accelerators, primarily motivated by AI applications [16, 17, 52, 12, 53, 15, 14, 54, 55, 56, 57, 58]. Research in software infrastructures for these accelerators, however, is just emerging. Unlike CPUs, accelerators do not support a standard instruction set architecture (ISA), alleviating the overhead from layers of abstractions and the burden of backward compatibility. Nonetheless, lack of a common abstraction makes it very hard to share compiler infrastructure across accelerators.

Most RDAs comes with a co-designed software layer that is very low-level and restrictive, requiring expertise knowledge in hardware architecture to efficiently target the accelerator. On the other side, machine learning frameworks [59, 60, 61, 62, 63, 64] provide high-level and succinct front-end abstraction that targets multiple hardware platforms. Yet most of theses frameworks only target mainstream accelerators, such as GPUs and FPGAs. Very few of the accelerators mentioned above can support more than a few proof-of-concept models with a end-to-end integration with these frameworks.



(a) Blackbox approach. (b) Whitebox approach.

Figure 1.3: Big picture of machine learning frameworks.

Part of the reason behind this is the massive engineering effort to program these accelerators. Frameworks like TensorFlow [59] and PyTorch [60] uses a template library approach, as shown in Figure 1.3 (a). These frameworks treats operations in the ML dataflow graph as blackbox kernels and implement every operation for every backend, requiring expensive engineering hours and hardware expertise to fine tune each accelerator. Furthermore, cross-kernel optimizations, such as fusion, often provide orders of magnitude improvement in efficiency. Recent studies in sparse ML also show promising speedup on large ML models [14]. However, sparse kernels require various data formats with very different implementation than the dense version [65]. In the blackbox approach, each fused operation and data format corresponds to a new blackbox kernel. As a result, the combination of required templates easily becomes untractable.

The alternative whitebox approach showin in Figure 1.3 (b) uses a succinct front-end representation, such as index notations [62], to express the computation of a kernel. This representation, however, cannot be directly mapped to accelerators due to various physical constraints. The framework then uses a series of transformations and optimizations to reformulate the kernel to an imperative implementation that can be supported by the accelerator. The transformation is often target-specific and studies have demonstrated ML-based cost models to facilitate the automatic searching of backend-specific schedules [66]. Next, the compiler can easily translates the imperative IR to the imperative front-ends of different accelerators.

To enable an easy integration of the whitebox approach, we introduce a compiler–SARA–that raise the programming abstraction of Plasticine to an imperative, loop-based language for general reconfigurable hardware—Spatial [67]. Plasticine is a purely dataflow accelerator without a centralized scheduler that executes instructions. This design makes the architecture very scalable to achieve FLOPS comparable to high-end GPUs and FPGAs. Nonetheless, it is not intuitive nor easy

to implement a linear algebra kernel with the low-level declarative streaming configurations. By support imperative constructs on a data-flow architecture efficiently, SARA not only improves the programmability of Plasticine, but also enables cross kernel optimizations on Plasticine. These optimizations have demonstrated an average 30x speedup over a Tesla V100 GPU and 2x speedup over a Stratix 10 FPGA from a Plasticine with much less on-chip resource than the baseline architectures [68] .

1.4 Contribution

In this work, we start by detailing the key considerations involved in building an RDA network, including those arising from network design, RDA architecture, and the characteristics of spatially mapped applications. Network designs must be carefully considered because vectorization magnifies inefficiencies: the increased network area of a vectorized design ensures that any overhead has a significant impact. Next, we evaluate the performance, area, and power requirements of several interconnection designs using cycle-accurate simulation and ASIC synthesis of a switch and router with a $28\,\mathrm{nm}$ industrial technology library. We then explore a variety of design points, including static, dynamic, and hybrid networks, decreased flit widths and VC counts for dynamic networks and different flow-control strategies for static networks.

We show that RDA network designs must consider application characteristics and the execution model of the underlying architecture. Performance scales strongly with network bandwidth, with an 8x average performance gap between the best and worst configurations. The hybrid network gives the best network energy-efficiency: a 1.83x average improvement over the static network. On pipelined architectures, hybrid networks can also match the performance per area of higher bandwidth, purely static networks with less than 8% performance loss.

The key contributions of this paper are:

1. An analysis of key communication patterns exhibited by spatial architectures.

2. A network-aware compiler flow that efficiently targets static, dynamic, and hybrid networks with varying granularities.

3. A quantitative analysis of the performance, area, and energy trade-offs involved in choosing an RDA network, using benchmarks drawn from various application domains.

1.5 Outline

The rest of this thesis is organized as follow: **??** gives a background on the execution schedule of spatial architectures, the front-end imperative language of SARA compiler, and the targeting architecture–Plasticine. **??** goes over the SARA compiler. **??** details the augmentations to the Plasticine architectures and the Network-on-chip study. **??** summarizes the related work. **??** concludes our work.

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