

Yoav Arbiv

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+ EXPERIENCE

Intel | Programmable IP Engineering

Sept 2021 - Dec 2021

- Designed a performance model of Intel memory controller IP using SystemC to enable microarchitectural exploration
- Developed a modular performance modelling framework in Platform Architect Ultra, reducing developer workload
- Investigated performance modelling methodologies and reported findings at an Intel tech talk

Intel | SoC Design Engineering

Jan 2021 - Apr 2021

- Designed an algorithm to optimize individual SoC voltages, improving worst-case power and delay metrics by ~15%
- Led development of a webapp which visualizes post-silicon tuning, allowing for interactive SoC binning
- Modified CAD fitter system to increase speed of FPGA arithmetic, then validated optimizations experimentally

A Thinking Ape | Backend Engineer

Jan 2020 - Apr 2020

- Re-architected WebSocket implementation system-wide, improving response time and decreasing API load by ~66%
- Automated data aggregation and reporting for app metrics
- Profiled and improved endpoint response times by >100ms

D2L | Fullstack Developer

May 2019 - Aug 2019

- Created a fullstack notetaking app with React and Node with a custom NLP question generation algorithm
- Leveraged microservices to improve response time by >100%
- Redesigned database to increase query speed by ~25%

North (now Google) | Software Engineer

Sept 2018 - Dec 2018

- Developed phone-to-glasses communication protocol to enable rapid developer iteration
- Resolved an issue in the glasses rendering pipeline, increasing frame refresh rate by >90% in certain use cases

+ TECHNOLOGIES

Languages

C, C++, JavaScript, Verilog, Python, Java, Asm, Rust

Frameworks & Libraries

SystemC/TLM2, React, TypeScript, Node, MongoDB, SQL, Flask, Django, Qt, Android NDK

Tools

ModelSim, Vivado, Platform Architect, Cadence Virtuoso, Git, Eclipse, Visual Studio

+ PROJECTS

Quietr Noise Cancelling | C

- Collaborated on an embedded device that provides active noise reduction using several transceivers
- Implemented FXLMS on an STM32 to emit destructive antinoise using closed-loop controls

RISC-V CPU | Verilog, Python

- Developed a single-core pipelined CPU which implements the RISC-V ISA in Verilog
- Wrote Python testbench that feeds in RISC binaries and verifies functionality by checking CPU memory

XY Controller | C

- Designed software for a 2D controller which visits a series of coordinates and visualizes progress on LCD
- Wrote embedded state machine to drive motors, check sensors, and poll a keypad

+ EDUCATION

University of Waterloo | 3.9 GPA

Expected Apr 2022

BASc, Honours Computer Engineering