Yoav Arbiv

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+ EXPERIENCE

ByteDance (TikTok) | Software Engineer
July 2022 - Present

• Designed and built features to improve TikTok Live reliability for millions of users worldwide
• Developed systems to intelligently schedule traffic on fault detection, improving user QoS and reducing support hours
• Implemented fallback paths to increase microservice resilience in case of external failure
• Integrated a data deletion service and refactored key MySQL tables to ensure GDPR compliance
• Analyzed traffic data to drive design decisions
• Led introduction of automated testing in select services

Intel | SoC Design Engineer Intern
Jan 2021 - Apr 2021, Sept 2021 - Dec 2021

• Modelled Intel memory controller IP using SystemC to enable rapid microarchitectural iteration
• Developed an interactive tool to optimize SoC voltage tuning, improving worst-case power/delay metrics by ~15%

A Thinking Ape | Backend Engineer Intern
Jan 2020 - Apr 2020

• Re-architected WebSocket implementation system-wide, improving response time and decreasing API load by ~66%
• Profiled and load tested critical endpoints using FlameGraph and Locust, optimizing by >100ms
• Leveraged BigQuery for automated data aggregation and reporting for key app metrics

D2L | Fullstack Developer Intern
May 2018 – Aug 2018

• Created an e-learning platform MVP with React, Node, and Flask which uses NLP to generate questions from coursework

North (now Google) | Software Engineer Intern
Sept 2018 – Dec 2018

• Developed features and resolved critical bugs for an Android-based smart glasses platform

+ TECHNOLOGIES

Languages
Go, Python, C, C++, JavaScript, Java, Rust

Frameworks & Libraries
MySQL, Thrift, Kafka, Redis, React, TypeScript, Node, BigQuery, MongoDB, Flask, Django

Tools
Kibana, Grafana, Git, Unix, Postman, FlameGraph

+ PROJECTS

Quietr Noise Cancelling | C

• Collaborated on an embedded device that provides active noise reduction using several transceivers
• Implemented FXLMS on an STM32 to emit destructive antinoise using closed-loop controls

RISC-V CPU | Verilog, Python

• Designed a single-core pipelined CPU which implements the RISC-V ISA in Verilog
• Developed a Python testbench using binaries to verify functionality by checking simulated memory

XY Controller | C

• Designed software for a 2D controller which visits a series of coordinates and visualizes progress on LCD
• Implemented an embedded state machine to drive motors, check sensors, and poll a keypad

+ EDUCATION

University of Waterloo | 3.9 GPA
Sept 2017 - Apr 2022

BASc, Honours Computer Engineering