Achronix
Data Acceleration

Product Brief

Achronix Tool Suite

Achronix Tool Suite Highlights

The Achronix® Tool Suite

- Enables Design Implementation of Speedster®7t FPGAs and Speedcore™ eFGPA IP:
  - Industry-standard design flow supporting RTL design entry (Verilog and VHDL)
  - Supports both pre- and post-routing timing simulation
  - Provides all back-end place-and-route functions
  - Performs timing analysis to determine FMAX and critical paths
  - Provides comprehensive area and timing reports, minimizing the effort in fitting and achieving timing closure
  - Intuitive graphical user interface (GUI) with advanced physical view for placement and viewing of critical paths
  - Full scripting support using Tcl

Features and Capabilities:

- Floorplanner – view and edit placement and routing
- IP configuration – create and edit IP, including the I/O designer toolkit used to configure Speedster7t hard IP functions
- Programmer and debugging interface – including Snapshot debugger for real-time design debugging
- Multi-process view – allows running multiple flows in parallel to explore various optimizations for a single design

Complete Design Flow Support:

- Industry-standard Synopsys Synplify Pro design synthesis included
- Support for industry-standard simulation tools (separate license required)
  - Mentor Graphics ModelSim Simulation
  - Synopsys VCS
  - Aldec Riviera

Operating System Support:

- Red Hat Enterprise Linux/CentOS 6.x or 7.x (64 bit)
- Microsoft Windows 10 (64 bit)

The Achronix Tool Suite works in conjunction with industry-standard synthesis tools, allowing FPGA designers (for both stand-alone and embedded) to easily map their designs into Achronix FPGA technology.

Advanced Functionality

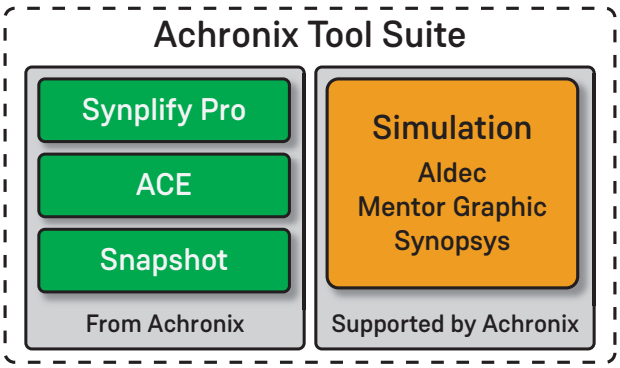
In addition to the standard tools such as place-and-route and bitstream generation, the Achronix Tool Suite includes advanced functionality:

- Static (sign-off) timing analysis
- Advance floorplaning tools that support the complex hard IP found in the I/O ring of Speedster7t FPGAs with the I/O Designer Toolkit

Synthesis Included

Achronix provides ACE together with an Achronix-optimized version of Synplify Pro from Synopsys, the industry standard for producing high-performance and cost-effective FPGA designs. Synplify Pro software uses a single, easy-to-use interface and has the ability to perform incremental synthesis and intuitive HDL code analysis.

Access to Debug



Snapshot is the real-time design debugging tool for Achronix FPGAs and cores. The Snapshot debugger, which is embedded in ACE, delivers a practical platform to observe the signals of a user's design in real-time. To use the Snapshot debugger, the Snapshot macro needs to be instantiated inside the user's RTL. After instan-

tiating, the user will be able to debug the design through the Snapshot Debugger GUI within ACE.

Support for the Complete Design Flow

Achronix simulation libraries are supported by ModelSim from Mentor Graphics, VCS from Synopsys and Riviera from Aldec (these tools are not supplied directly by Achronix).

Standard RTL (VHDL and Verilog) input together with simulation with industry-standard simulators ensures the Achronix design flow is straightforward for existing FPGA designers.

The ACE Design Flow

The diagram to the right shows the Achronix design flow supported by ACE. RTL describing the behavior of the design is synthesized using Synplify PRO from Synopsys — an industry-standard synthesis tool.

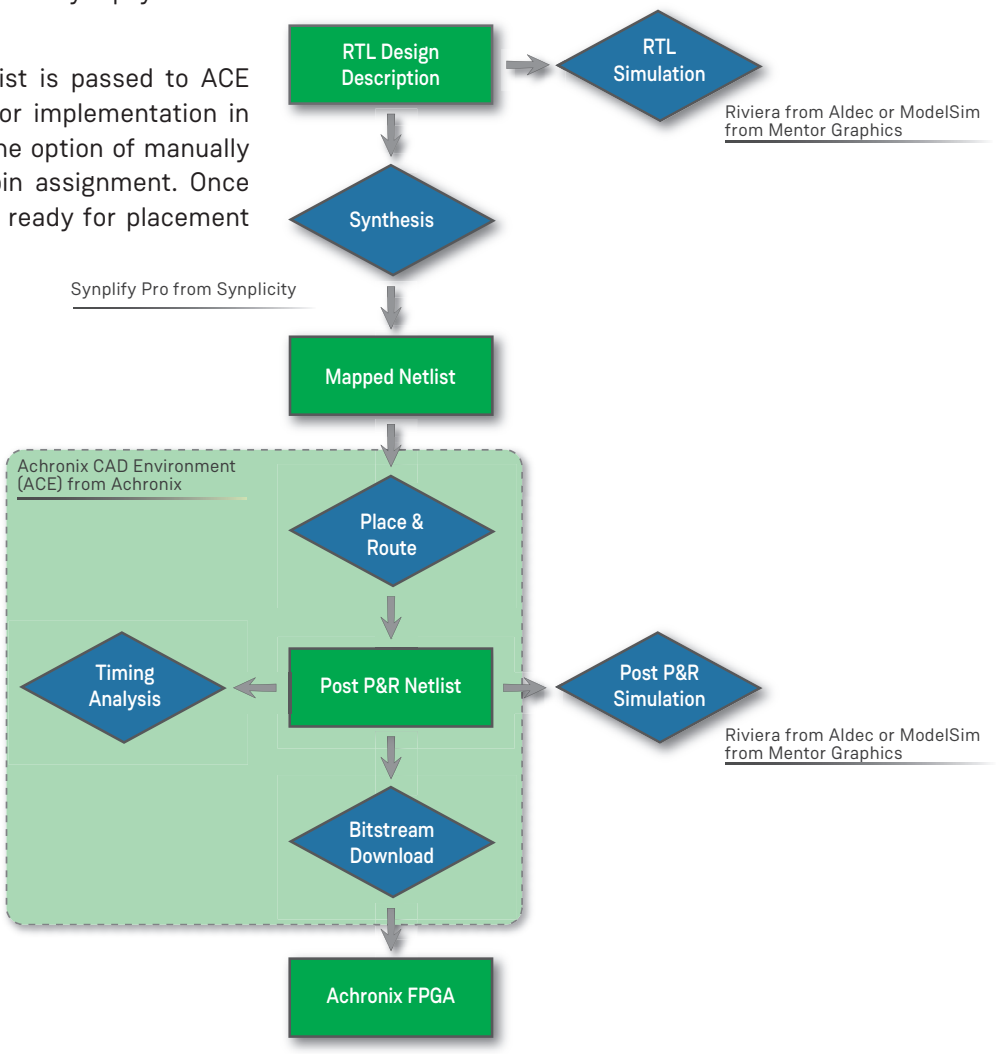
Once synthesized, the gate-level netlist is passed to ACE where it is compiled and processed for implementation in the Achronix technology. Users have the option of manually assigning I/O or allowing automatic pin assignment. Once the device pinout is set, the design is ready for placement and routing — the design is mapped into the physical building blocks in the FPGA and the routing between these building blocks is assigned.

Once place and route is complete, the SRAM switching elements needed for device configuration are finalized and the tools generate a bitstream for device programming.

At the conclusion of place and route, final timing information is available for analysis using ACE's built-in timing analysis capability. Gate-level timing simulation can also be performed using industry-standard simulation tools from Mentor Graphics, Synopsys or Aldec.

The ACE design flow also puts great importance on the protecting user IP. Throughout the design flow, data encryption is supported including a 256-bit AES encryption of the device configuration information. This capability protects valuable intellectual property and prevents design tampering.

With support for both Microsoft Windows and Linux operating systems, the Achronix ACE Tool Suite is available via download. For more information, visit: www.achronix.com/getting-started-achronix.



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