GateMate[™] FPGA



Suitable from university projects up to high volume applications

Supported by:



on the basis of a decision by the German Bundestag

Overview

The GateMate[™] FPGA family of Cologne Chip[™] AG addresses all application requirements of small to medium size FPGAs. Very low power and speed applications are feasible. Logic capacity, power consumption, package size and PCB compatibility are best in class. GateMate[™] FPGAs combine these features with lowest cost in industry making the devices well suited from University projects to high volume applications. Because of the outstanding Circuit size/Cost ratio, even new applications now can use the benefits of FPGAs.

All this is based on a novel FPGA architecture combining a special logic element called Cologne Programmable Element (CPE) with a smart routing engine. Furthermore, arbitrary size Multipliers are usable. Memory aware applications can use block dual-port SRAMs with bit widths from 1 to 80 bits. Even bit-wise enable is feasible.

General Purpose IOs (GPIOs) can use different voltage levels from 1.2 to 2.5 Volt. GPIOs can be configured as single-ended or LVDS differential type. Furthermore a high speed SERDES interface is available.

GateMate[™] FPGAs are supported by EasyConvert[™], that enables the transfer of existing FPGA designs



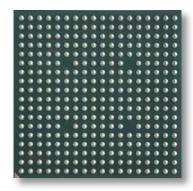
without new synthesis. Worldclass P&R-software maps and implements the design into GateMate[™] FPGA.

A Static Timing Analysis (STA) is also performed and gives evidence about critical pathes and the overall performance of a design. The design can be easily simulated using Verilog netlist and SDF timing extraction.

The devices are manufactured using Global-foundries[™] 28 nm SLP (Super Low Power) process. Due to manufacturing in Europe, there is no danger of trade restrictions or high taxation.

Complimentary design conversion service





FBGA 324 ball 15x15 mm with 0.8 mm ball pitch package of GateMate™ CCGM1A1

GateMate™ Features

- Logic capacity from 40.000 to more than a million LUT-4 equivalent cells
- DPSRAM 1.280 Mbit
- Novel architecture with new programmable element (CPE)
- CPE consists of LUT tree with 8 inputs
- 3 operation areas: low power, economy, speed
- FPGA in ball grid package for low size and high pin count

- Pricing starts from \$US 10 for GateMate[™] CCGM1A1 device in volume quantities
- Design conversion service free of charge for GateMate[™] customers
- Only 2 signal layers on PCB necessary
- Low configuration bit count
- Very fast configuration using 4 bit SPI interface up to 100 MHz
- No excessive start-up currents

Multiple clocking schemas

designed and manufactured in Germany

- Only two supply voltages needed, that can be applied in any order
- Dual-ported Block RAMs with 1-80 bits data width, also configurable as FIFO
- Multipliers with arbitrary factor sizes implementable
- SERDES 2.5 Gb/s
- General Purpose IOs (GPIO) configurable as single-ended or differential (LVDS)
- Pullup/Pulldown resistors configurable
- Support for ADC and DAC with additional IP cores
- Core voltage depending on application mode:
 0.9 V, 1.0 V, 1.1 V
- Low Power 28 nm SLP Globalfoundries[™] process technology
- Made in Europe
- EasyConvert[™] software to migrate existing designs to GateMate[™]
- GateMate[™] Place&Route with automatic clock Skew analysis and fixing
- Static Timing Analysis for performance evaluation
- Available in different size versions (see table)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
Α	GND	VDD_ WC	IO_NA _A0	IO_NA _A1	VDD_ NA	IO_NA _A4	GND	IO_NA _A7	IO_NB _B0	GND	IO_NB _B2	IO_NB _B4	GND	IO_NB _B7	IO_EB _B8	VDD_ EB	IO_EB _B5	GND	Α
В	IO_WC _A8	IO_WC _B8	IO_NA _B0	IO_NA _B1	IO_NA _A2	IO_NA _B4	VDD_ NA	IO_NA _B7	IO_NB _A0	VDD_ NB	IO_NB _A2	IO_NB _A4	VDD_ NB	IO_NB _A7	IO_EB _A8	GND	IO_EB _A5	VDD_ EB	В
С	GND	VDD_	IO_WC _A7	IO_WC _B7	IO_NA _B2	IO_NA _A3	IO_NA _A5	IO_NA _A6	IO_NA _A8	IO_NB _B1	IO_NB _B3	IO_NB _B5	IO_NB _B6	IO_NB _B8	IO_EB _B7	IO_EB _B6	IO_EB _B4	IO_EB _A4	С
D	IO_WC _A5	IO_WC _B5	IO_WC _A6	IO_WC _B6	VDD_ WC	IO_NA _B3	IO_NA _B5	IO_NA _B6	IO_NA _B8	IO_NB _A1	IO_NB _A3	IO_NB _A5	IO_NB _A6	IO_NB _A8	IO_EB _A7	IO_EB _A6	IO_EB _B2	IO_EB _A2	D
E	IO_WC _A3	IO_WC _B3	IO_WC _A4	IO_WC _B4	GND	VDD_ NA	GND	VDD_ NA	GND	VDD_ NB	GND	VDD_ NB	GND	VDD_ EB	IO_EB _B3	IO_EB _A3	VDD_ EB	GND	E
F	GND	VDD_ WC	IO_WC _A2	IO_WC _B2	VDD_ WC	GND	VDD_ NA	GND	VDD	GND	VDD_ NB	GND	VDD_ EB	GND	IO_EB _B1	IO_EB _A1	IO_EB _B0	IO_EB _A0	F
G	IO_WC _A0	IO_WC	IO_WC _A1	IO_WC _B1	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B8	IO_EA _A8	IO_E A _B7	IO_EA _A7	G
Н	IO_WB _A7	IO_WB _B7	IO_WB _A8	IO_WB _B8	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA _B6	IO_EA _A6	VDD_ EA	GND	н
J	GND	VDD_ WB	IO_WB _A6	IO_WB _B6	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B5	IO_EA _A5	IO_E A _B4	IO_E A _A4	J
K	IO_WB _A5	IO_WB _B5	IO_WB _A4	IO_WB _B4	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	IO_EA _B3	IO_EA _A3	IO_E A _B2	IO_EA _A2	ĸ
L	IO_WB _A3	IO_WB _B3	IO_WB _A2	IO_WB _B2	GND	VDD	GND	VDD	GND	VDD	GND	VDD	GND	VDD_ EA	IO_EA _B1	IO_EA _A1	VDD_ EA	GND	L
М	GND	VDD_ WB	IO_WB _A1	IO_WB _B1	VDD_ WB	GND	VDD	GND	VDD	GND	VDD	GND	VDD	IO_EA _B0	IO_EA _A0	GND	IO_SB _A3	IO_SB _B3	М
N	IO_WB _A0	IO_WB _B0	IO_WA _A8	IO_WA	VDD_ WA	VDD	GND	VDD	GND	VDD	VDD_ SB	GND	VDD_ SB	IO_SB _A8	IO_SB _B8	N.C.	GND	VDD_ SB	N
Р	IO_WA _A7	IO_WA _B7	VDD_ WA	GND	VDD_ WA	VDD_ SA	GND	VDD_ SA	GND	VDD_ SA	IO_SB _A4	IO_SB _A7	IO_SB _B7	IO_SB _A6	IO_SB _B6	VDD_ PLL	IO_SB _A2	IO_SB _B2	Р
R	IO_WA _A6	IO_WA _B6	IO_WA _A5	IO_WA _B5	IO_WA _A0	IO_SA _A1	IO_SA _A2	10_SA _A4	IO_SA _A6	IO_SA _A7	IO_SB _B4	GND	IO_SB _A5	IO_SB _B5	VDD_ SB	GND	IO_SB _A1	IO_SB _B1	R
Т	VDD_ WA	IO_WA _A4	IO_WA _B4	GND	IO_WA _B0	IO_SA _B1	IO_SA _B2	IO_SA _B4	IO_SA _B6	IO_SA _B7	GND	SER_ CLK	SER_ CLK_N	VDD _CLK	RST_N	VDD_ SER_P[]	GND	VDD_ SB	Т
U	IO_WA _A3	IO_WA _B3	VDD_ WA	IO_WA _A1	IO_SA _A0	VDD_ SA	IO_SA _A3	IO_SA _A5	VDD_ SA	IO_SA _A8	SER_ RX_P	VDD_ SER	SER_ TX_P	GND	GND	TEST MODE	IO_SB _A0	IO_SB _B0	U
٧	GND	IO_WA _A2	IO_WA _B2	IO_WA _B1	IO_SA _B0	GND	IO_SA _B3	IO_SA _B5	GND	IO_SA _B8	SER_ RX_N	SER_ RTERM	SER_ TX_N	GND	POR_ ADJ	GND	VDD_ SER	GND	٧
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	

Package Connections of **GateMate[™] CCGM1A1** with ball positions and signal names

Device	Rel. size	cize Cologne Programmable Elements 1) 2)				Block RAM 3)		SERDES	I/Os		Package	
		CPEs	8-Inp-LUT trees	FF/Latches	20Kb	40Kb			single-ended	differential	balls	size (mm)
CCGM1A1	1	20,480	20,480	40,960	64	32	4	1	162	81	324BGA	15x15
CCGM1A2	2	40,960	40,960	81,920	128	64	8	2	162	81	324BGA	15x15
CCGM1A4	4	81,920	81,920	163,840	256	128	16	4	162	81	324BGA	15x15
CCGM1A9	9	184,320	184,320	368,640	576	288	36	9	tbd	tbd	tbd	tbd
CCGM1A16	16	327,680	327,680	655,360	1,024	512	64	16	tbd	tbd	tbd	tbd
CCGM1A25	25	512,000	512,000	1,024,000	1,600	800	100	25	tbd	tbd	tbd	tbd

1) CPEs have 2x4 or 8 inputs connected to a LUT tree $\,$

2) Each CPE can be used as 2x2 Multiplier tile

3) Block RAM can have a data width of 1-80 bits



Cologne Chip AG Eintrachtstr. 113 50668 Koeln, Germany eMail: info@colognechip.com Web: www.colognechip.com Tel: +49.221.91240