Vlsi final project :2

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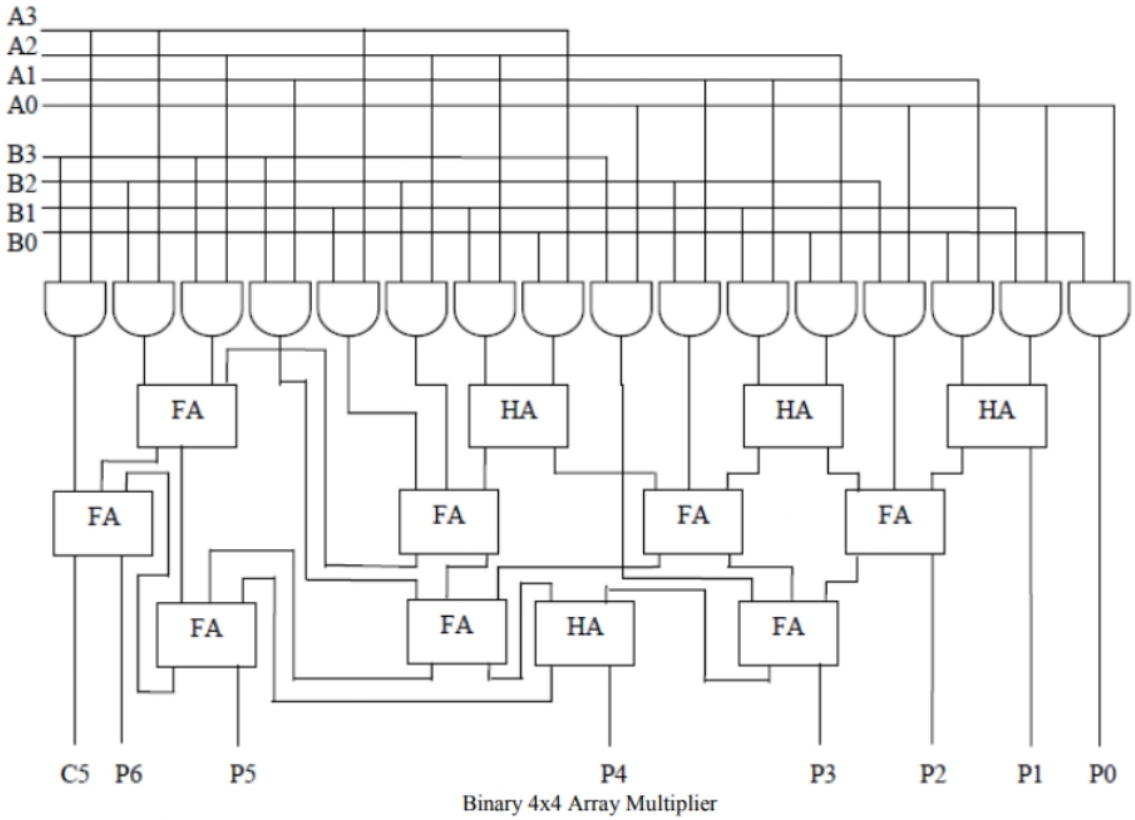
The circuit need to be implemented



Binary 4x4 Array Multiplier

Implementation by ngspice:

The technology file taken is 180nm. The implementation is by using 4 four-bit adders which are implemented by xor gates. For the final circuit different subcircuits are called accordingly.

And then delay is calculated and shown below .

Delay calculation shown below

```
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
A0: 0 A1: 0 A2: 0 A3: 0
B0: 0 B1: 0 B2: 0 B3: 0
Maximum Delay: 3.56815E-11
--------------------------
```

Implementation in verilog

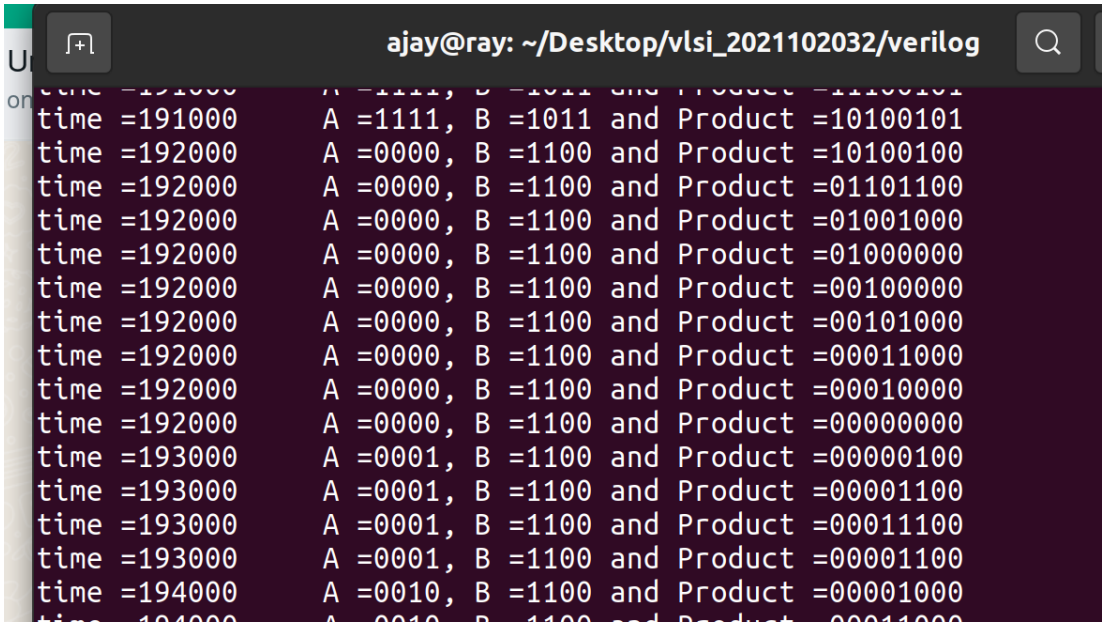
Logic file are written for all the subfiles and finally included in the multiplier file.

Command in the terminal : 1. iverilog -o test_tb Multiplier_4x4.v Multiplier_4x4_tb.v

2. vvp test_tb

Output:

The logic implementation can be verified by the following output.



Implementation by magic:

Here the technology file included is TSMC_180nm.txt .

Command in terminal: magic multiplier.mag

In magic nand gate implementation is done. Xor gate is implemented by using 4 nand gate.

After then using xor gate half adder and full adder is designed to get the final multiplier circuit.

Output