IPA Final Quiz

Marking Scheme:
All MCQs will be marked according to the number of correct answers provided, i.e., if the marks for the question is x and there are n right answers, each correct answer will get x/n marks.
Every wrong answer in MCQs will fetch you -0.25 marks
The marking for descriptive questions will be decided by the instructor.

Points: 30/40

1. If the pipeline stages can be altered, how can we eliminate stalling and avoid load/use hazard encountered in a 5-stage pipeline?
(0/3 Points)

we can avoid a load/use data hazard with a combination of stalling and forwarding. This requ

2. If a conditional branch instruction is mispredicted, how many instructions will be fetched and replaced with bubbles in a 5 stage pipelined architecture?
(2/2 Points)

- 1
- 3
- 0
- 2 ✓

3. If there are 64 sets in a direct-mapped cache, 4 lines per set and 8 bytes per cache block, how many bits are tag bits for a memory address with 16-bit memory address?
(2/2 Points)

- 8
- 11
- 7 ✓
- 4

4. What happens if the sum of the working set sizes in Virtual memory paging is greater than the DRAM memory size? Please explain.
(3/3 Points)

Thrashing happens if the sum of the working set sizes in Virtual memory paging is greater tha

5. Suppose a large program has 1 million instructions to execute and the processor executing the program runs at a maximum frequency of 1 GHz. If 40% of the instructions run in 5 clock cycles, 30% run in 4 clock cycles and remaining 30% run in 3 clock cycles, what is the execution time of the program?
(2/2 Points)

- 3.1 msec
- 3.5 msec
- 5.1 msec
- 4.1 msec ✓

6. What is/are true about processes in an Operating System?
(2/2 Points)

- [x] Two processes can be sequential or concurrent ✓

- [ ] Each process gets entire access to the CPU
- [x] Processes get a part of the CPU bandwidth ✓
- [ ] Processes are allocated an entire memory space

7. What are the advantages and disadvantages of a E-way set associate cache? Please answer with example.
(0/3 Points)

Advantages
The placement policy is a trade-off between direct-mapped and fully associative cache.
It offers the flexibility of using replacement algorithms if a cache miss occurs.
Disadvantages
The placement policy will not effectively use all the available cache lines in the cache and suffers from conflict miss.
Example -
Consider the main memory of 16 kilobytes, which is organized as 4-byte blocks, and a 2-way set-associative cache of 256 bytes with a block size of 4 bytes. Because the main memory is 16kB, we need a minimum of 14 bits to uniquely represent a memory address. Since each cache block is of size 4 bytes and is 2-way set-associative, the total number of sets in the cache is 256/(4 * 2), which equals 32 sets.
The incoming address to the cache is divided into bits for Offset, Index, and Tag.

Offset corresponds to the bits used to determine the byte to be accessed from the cache line. Because the cache lines are 4 bytes long, there are 2 offset bits.
The index corresponds to bits used to determine the set of the Cache. There are 32 sets in the cache, and because 2^5 = 32, there are 5 index bits.
Tag corresponds to the remaining bits. This means there are 14 – (5+2) = 7 bits, which are stored in the tag field to match the address on cache request.
These are the memory addresses and cache line on which they set-
Address 0x0000 (tag - 0b00_0000, index – 0b00_0000, offset – 0b00) corresponds to block 0 of the memory and maps to the set 0 of the cache. The block occupies a cache line in set 0, determined by the replacement policy for the cache.
Address 0x0004 (tag - 0b00_0000, index – 0b00_0001, offset – 0b00) corresponds to block 1 of the memory and maps to the set 1 of the cache. The block occupies a cache line in set 0, determined by the replacement policy for the cache.
Address 0x00FF (tag – 0b00_0000, index – 0b11_1111, offset – 0b11) corresponds to block 63 of the memory and maps to the set 63 of the cache. The block occupies a cache line in set 63, determined by the replacement policy for the cache.
Address 0x0100 (tag – 0b00_0001, index – 0b00_0000, offset – 0b00) corresponds to block 64 of the memory and maps to the set 0 of the cache. The block occupies a cache line in set

8. What kind of cache misses cannot be avoided?
(2/2 Points)

- Conflict miss
- Cold miss ✓
- Capacity miss
- All of the above

9. int sum_array_3d(int a[M][N][N])
{
    int i, j, k, sum = 0;

    for (i = 0; i < M; i++)
        for (j = 0; j < N; j++)
            for (k = 0; k < N; k++)
                sum += a[k][i][j];
    return sum;
}

How will you transform the above code to achieve stride-1 reference pattern for good spatial locality?
(3/3 Points)

To convert this program to a new program that achieves stride-1 reference pattern, we have to simply switch the indices in the line 'sum += a[k][i][j]' to 'sum += a[i][j][k]'. This works due to the fact that the matrix is accessed in the same row-major order in which it is stored in the memory.

```
int sum_array_3d(int a[M][N][N])
{
    int i, j, k, sum = 0;

    for (i = 0; i < M; i++)
        for (j = 0; j < N; j++)
            for (k = 0; k < N; k++)
                sum += a[i][j][k];
    return sum;
}
```

10. Which instruction causes a write in the memory stage of the processor?
(2/2 Points)

- [ ] jmp
- [ ] popq

- [x] rmmovq ✓
- [x] call ✓

11. How is page table used in a VM address translation? Please explain briefly.
(3/3 Points)

Virtual memory address translation uses a page table. A page table is a structured array in me

12. In a synchronous DRAM consisting of 64 supercells each having 8 bits of data, how many RAS and CAS selects will be necessary to get the supercells (4,1), (4,7), (6,7), (7,6)?
(2/2 Points)

- ( ) 4 RAS and 3 CAS
- ( ) 4 RAS and 4 CAS
- (•) 3 RAS and 4 CAS ✓
- ( ) 3 RAS and 3 CAS

13. How can you avoid the load/use hazard for a 5-stage pipeline? Please explain.
(1/3 Points)

One very general technique for avoiding hazards involves stalling, where the processor holds back one or more instructions in the pipeline until the hazard condition no longer holds. Our processor can avoid data hazards by holding back instruction in the decode stage until the instructions generating its source operands have passed through the write-back stage. Instead of stalling, a result value that can be passed directly from one pipeline stage to an earlier one is commonly known as data forwarding (or simply forwarding, and sometimes bypassing). To exploit data forwarding to its full extent, we can also pass newly

14. What is the hit rate in an instruction cache if there are 10% instruction fetches causing a miss?
(2/2 Points)

- ( ) None of the above

- (•) 0.9 ✓
- ( ) 0.5
- ( ) 0.1

15. If there is enough cache capacity compared to the size of a cache block, what are the types of cache misses that a direct-mapped cache encounters?
(2/2 Points)

- [ ] Capacity miss
- [x] Cold miss ✓
- [x] Conflict miss ✓
- [ ] All of the above

16. What is/are the problems in a processor design with no pipeline?
(2/2 Points)

- [ ] none of the above
- [ ] complex design
- [x] suboptimal use of hardware resources ✓
- [x] high clock cycle time ✓

17. Which of the following instructions do not result in incrementing the PC value by 1 in a sequential processor?
(0/2 Points)

- [ ] ret ✓
- [x] popq
- [x] addq
- [x] rmmovq