Intro to Processor Architecture – Spring 2022

End Sem Exam

Max Time: 90 minutes **Max Marks: 70**

Instructions

The MCQs will be marked according to the number of correct answers provided, i.e., if the mark for the question is x and there are n right answers, each correct answer will get x/n marks. Every wrong answer in MCQs will fetch you -0.25 marks.
The marking for descriptive questions will be decided by the instructor.

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1) A large program has 1 million instructions which needs to be executed by the processor with frequency of 1 GHz. If 30% of the instructions run in 4 clock cycles, another 30% instructions run in 5 clock cycles, 20% instructions run in 6 clock cycles and the remaining 20% instructions run in 7 clock cycles, what is the execution time of the program? **(2 marks)**

2) Please explain 3 reasons with appropriate diagrams why a sequential processor design is not optimal. **(5 marks)**

3) How does data forwarding help in improving the throughput of a pipelined processor? Please explain with the help of all the scenarios of data forwarding. **(5 marks)**

4) How can you avoid the load/use hazard for a 5-stage pipeline? Please explain. **(3 marks)**

5) If the pipeline stages can be altered, how can we eliminate stalling and avoid load/use hazard encountered in a 5-stage pipeline? **(5 marks)**

6)
```
int sum_array_3d(int a[N][N][N])
{
int i, j, k, sum = 0;

for (i = 0; i < N; i++)
    for (j = 0; j < N; j++)
        for (k = 0; k < N; k++)
            sum += a[k][i][j];
return sum;
}
```
How will you transform the above code to achieve stride-1 reference pattern for good spatial locality? **(3 marks)**

7) What are the advantages and disadvantages of a E-way set associate cache? Please answer with example. **(3 marks)**

8) a) What is the hit rate in an instruction cache if there are 20% instruction fetches causing a miss?
b) What is the percentage improvement in hit rate in an instruction cache if the original case of 30% instructions causing a miss is improved to 10% instructions causing a miss by eliminating conflict misses? **(5 marks)**

9) What happens if the sum of the working set sizes in Virtual memory paging is greater than the DRAM memory size? Please explain. **(2 marks)**

10) How is page table used in a VM address translation? Please explain briefly. **(3 marks)**

11) What is the significance of Translation Lookaside buffer. Briefly explain. **(4 marks)**

12) What is the need of multilevel page table for VM address translation and how is the address decoded for the multilevel page table. Assume there are 2 levels in the page table for your explanation. **(5 marks)**

13) If a program execution is monitored for time of execution in a desktop, you will find that the program executes with different execution times in each run. Please provide 3 reasons why there will be variation of execution time for the same program? **(5 marks)**

14) If a conditional branch instruction is mispredicted, how many instructions will be fetched and replaced with bubbles in a 5 stage pipelined architecture? **(2 marks)**

a) 0
b) 1
c) 2
d) 3

15) What kind of cache misses cannot be avoided? **(2 marks)**

a) Conflict miss
b) Cold miss
c) Capacity miss
d) All of the above

16) If there is enough cache capacity compared to the size of a cache block, what are the types of cache misses that a direct-mapped cache encounters? **(2 marks)**

a) Cold miss
b) Capacity miss
c) Conflict miss
d) All of the above

17) If there are 64 sets in a direct-mapped cache, 4 lines per set and 8 bytes per cache block, how many bits are tag bits for a 16-bit memory address? **(2 marks)**

a) 4
b) 7
c) 8
d) 11

18) What is the throughput of a 5-way pipelined architecture where combinational logic at each stage requires 100 ps and the register delay is 20 ps? **(2 marks)**

a) 4.33 GIPS
b) 6.33 GIPS
c) 8.33 GIPS
d) 1.67 GIPS

19) Please mention 3 problems that arise due to pipelined processor architecture and explain why they are important to address. **(5 marks)**

20) How is cache management different from virtual memory management? Please explain by highlighting about the entities which manage them and what do they do. **(5 marks)**