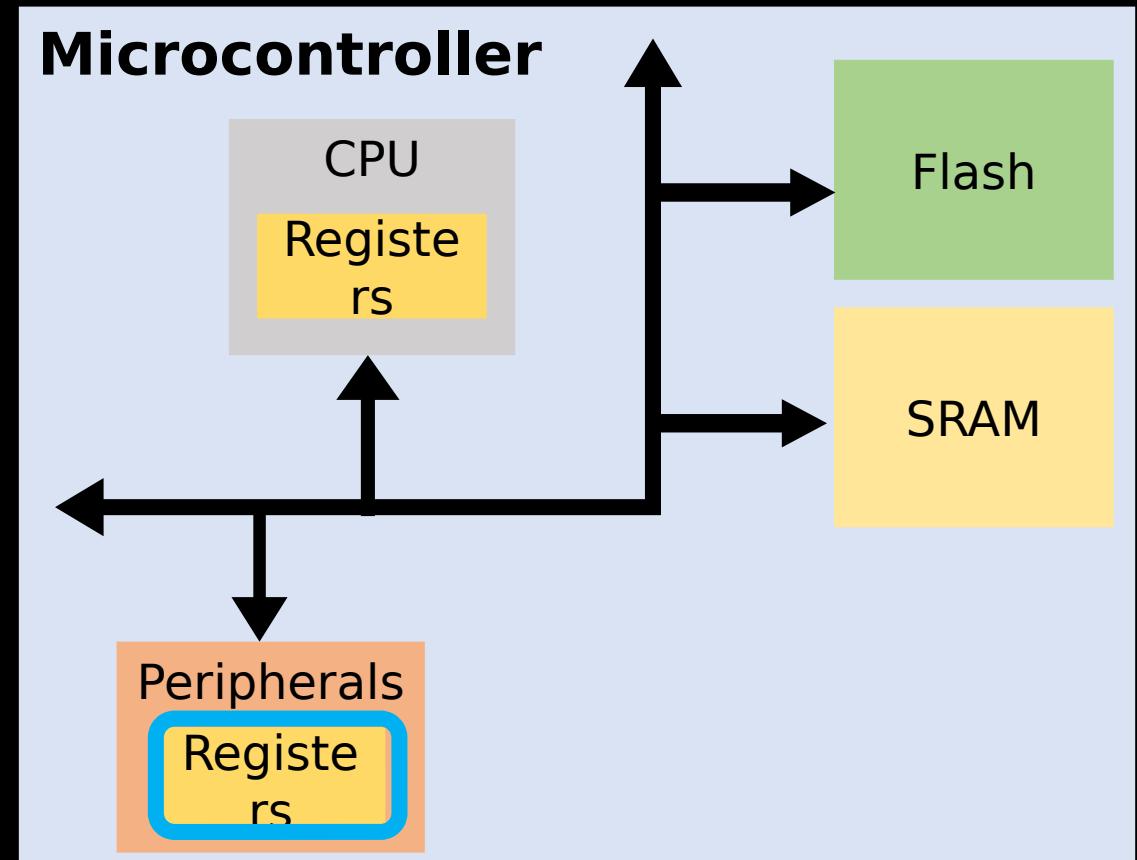


IO Port Configuration Example

Embedded Software Essentials

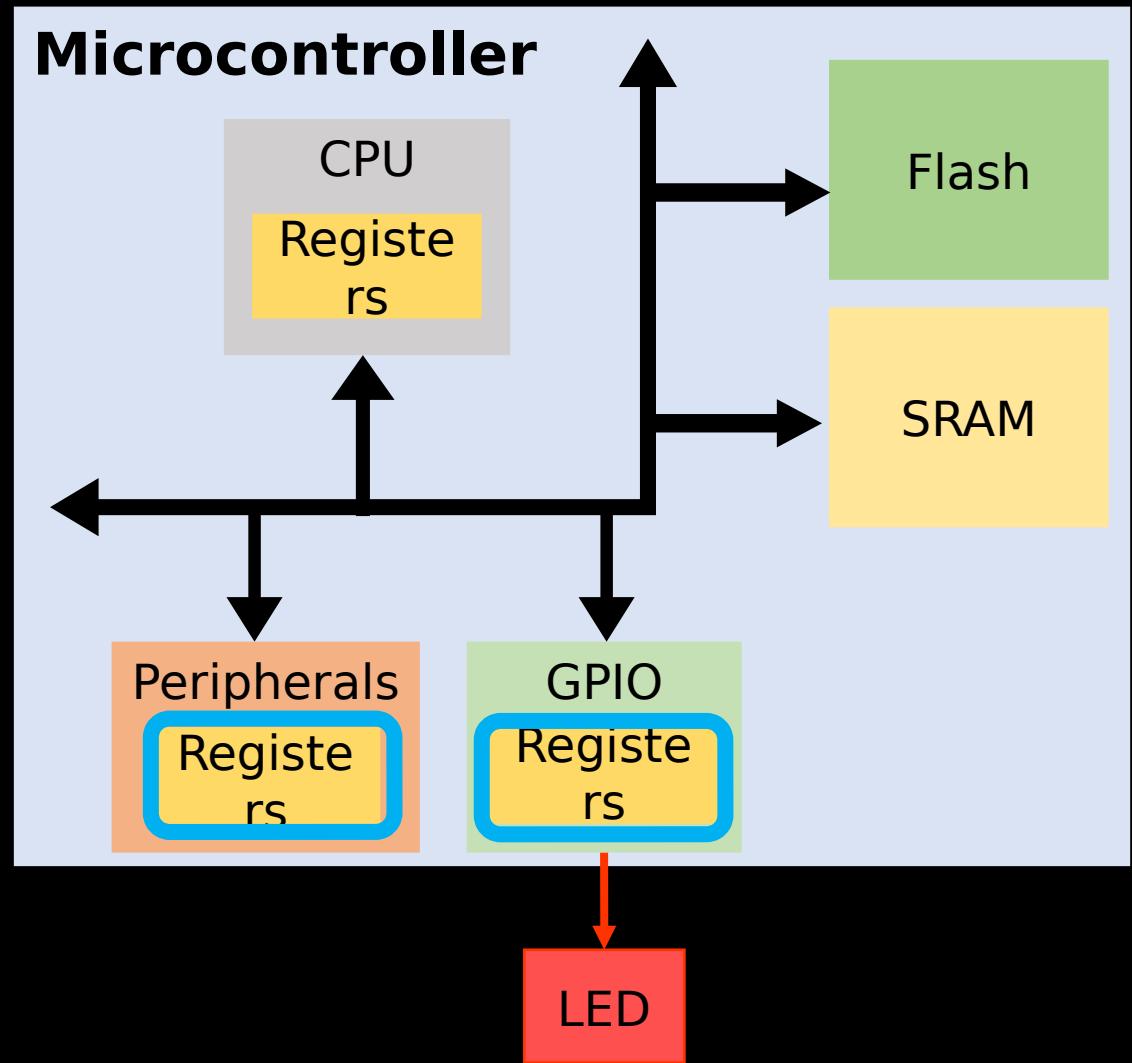
Peripherals [S1a]

- **Peripherals**: External to CPU specialized support hardware
- Similar process to configure peripherals
 - Pointers
 - Memory Reads/Writes
 - Use of Bit Manipulation



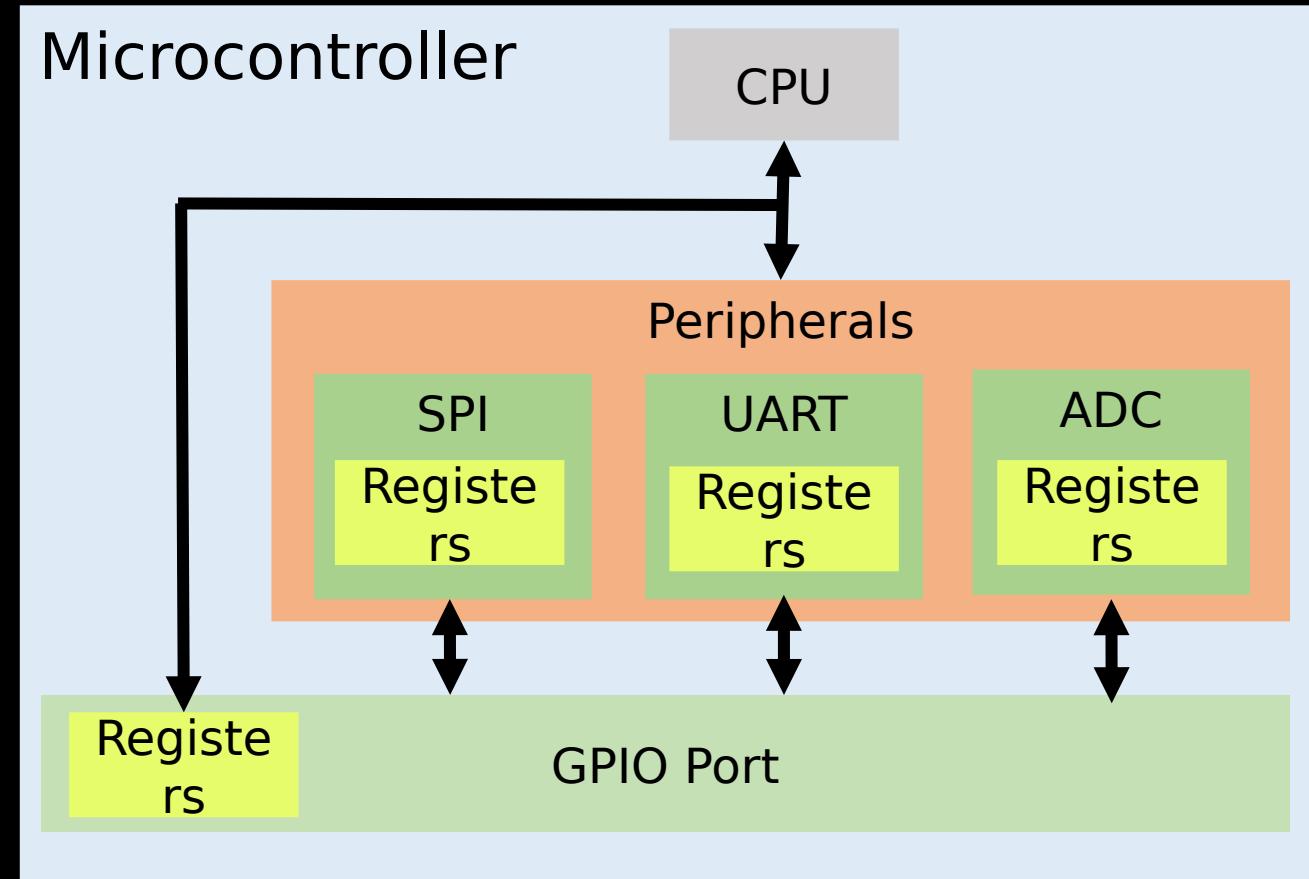
Peripherals [S1b]

- **Peripherals**: External to CPU specialized support hardware
- Similar process to configure peripherals
 - Pointers
 - Memory Reads/Writes
 - Use of Bit Manipulation
- GPIO - General Purpose Input/Output



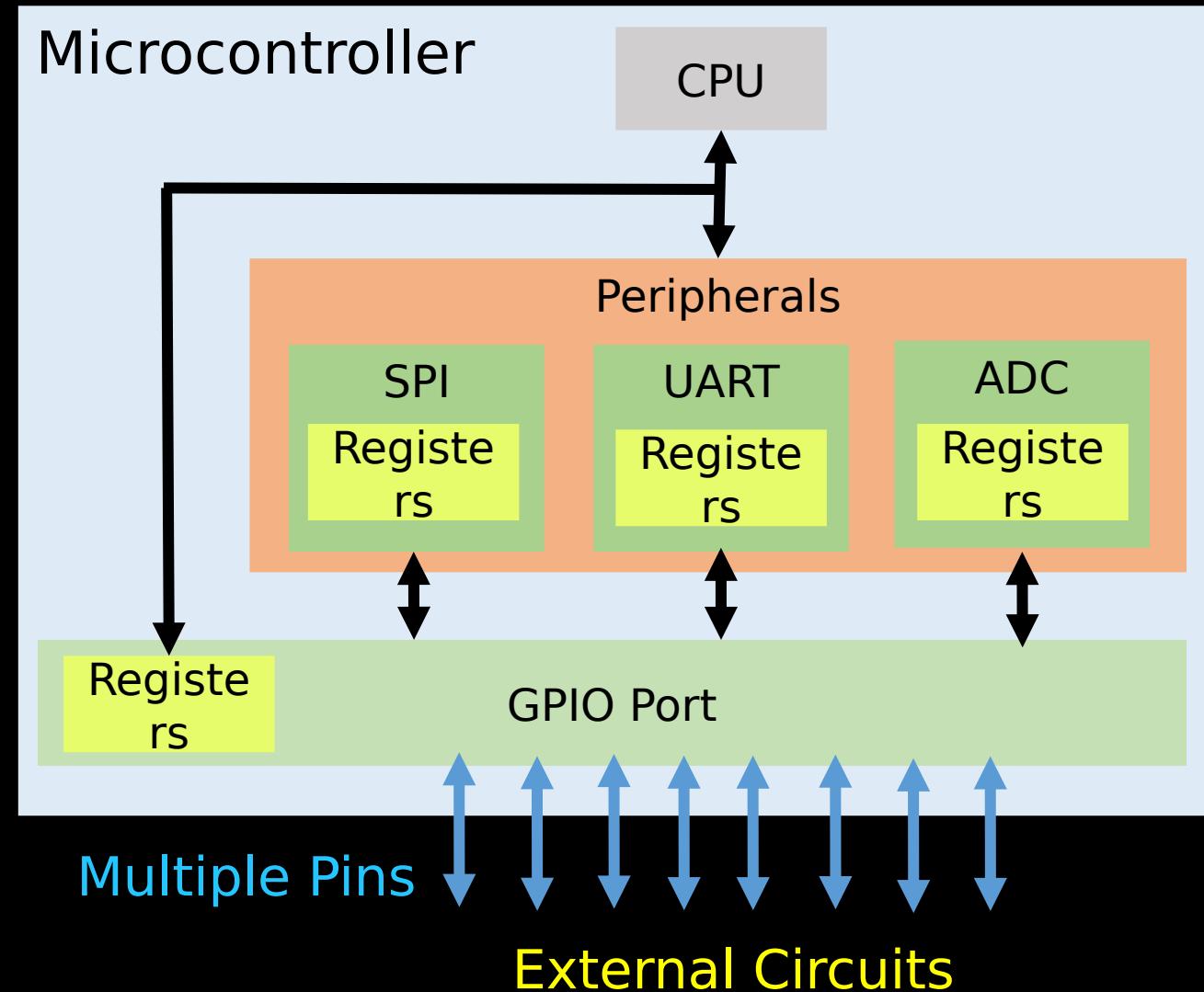
Input Output Systems [S2a]

- **Input/Output:** method to get data in/out of microcontroller
 - GIO
 - IO
 - GPIO (General Purpose IO)



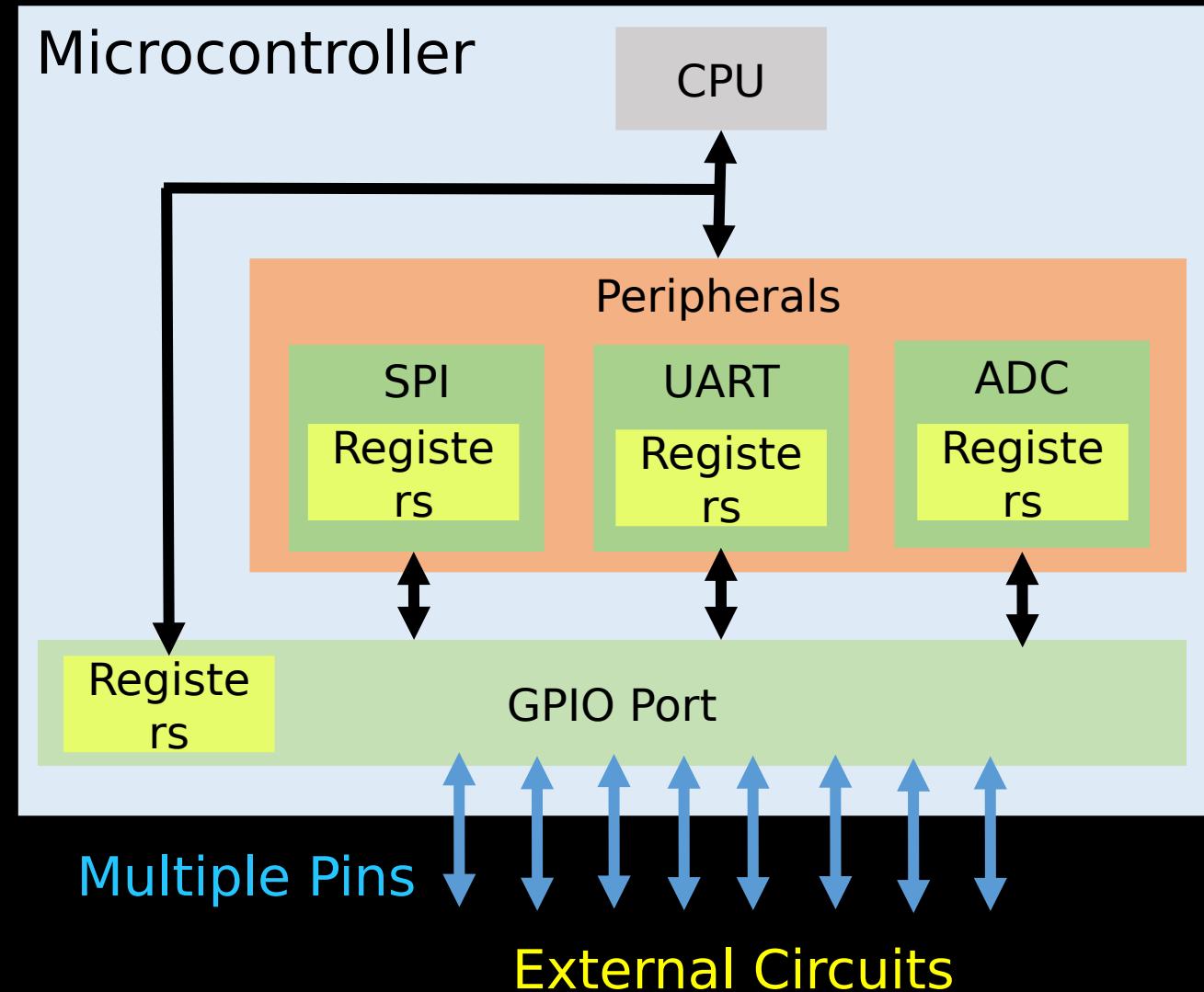
Input Output Systems [S2b]

- **Input/Output:** method to get data in/out of microcontroller
 - GIO
 - IO
 - GPIO (General Purpose IO)

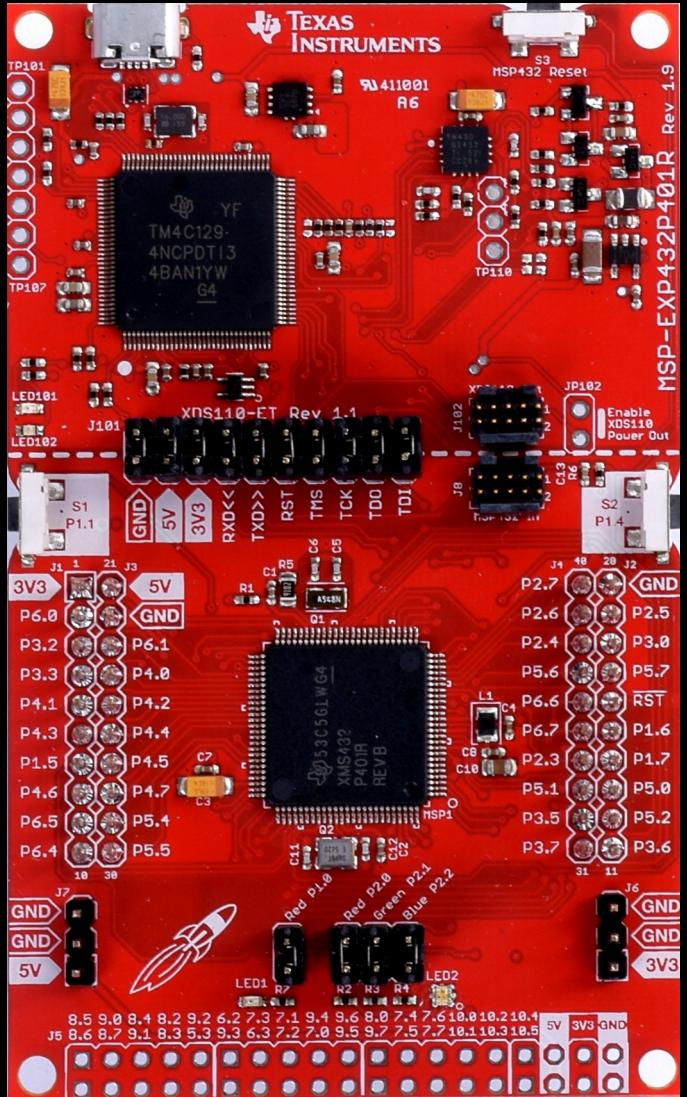


Input Output Systems [S2c]

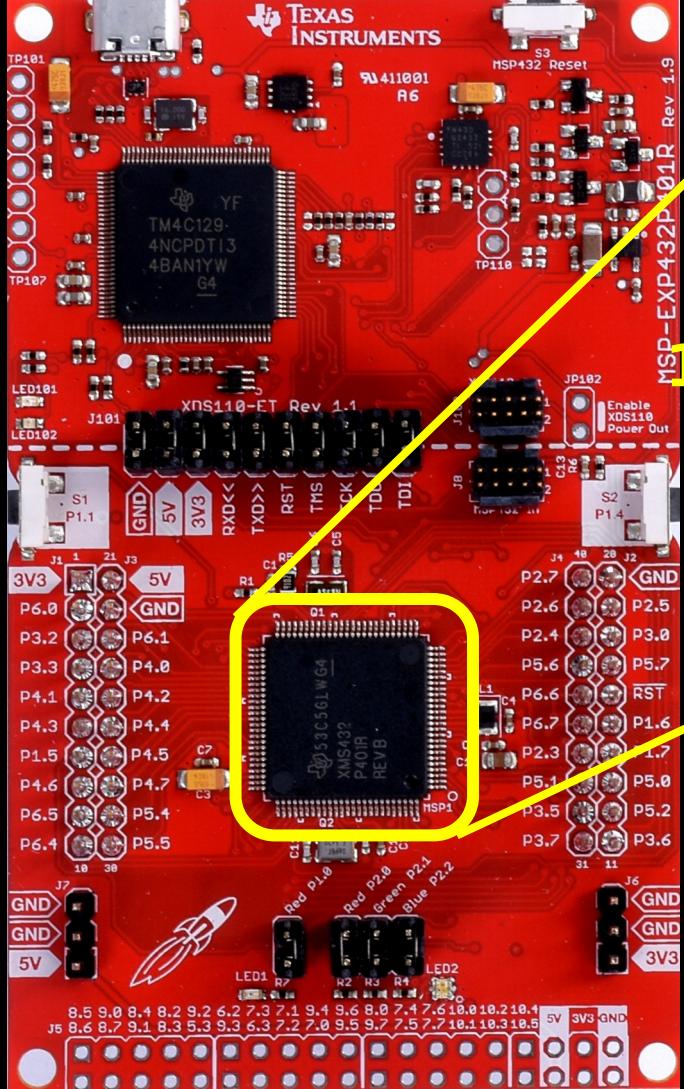
- **Input/Output:** method to get data in/out of microcontroller
 - GIO
 - IO
 - GPIO (General Purpose IO)
- Pin - physical connection to microcontroller
- Port - combination of pins



MSP432 Ports [S3a]



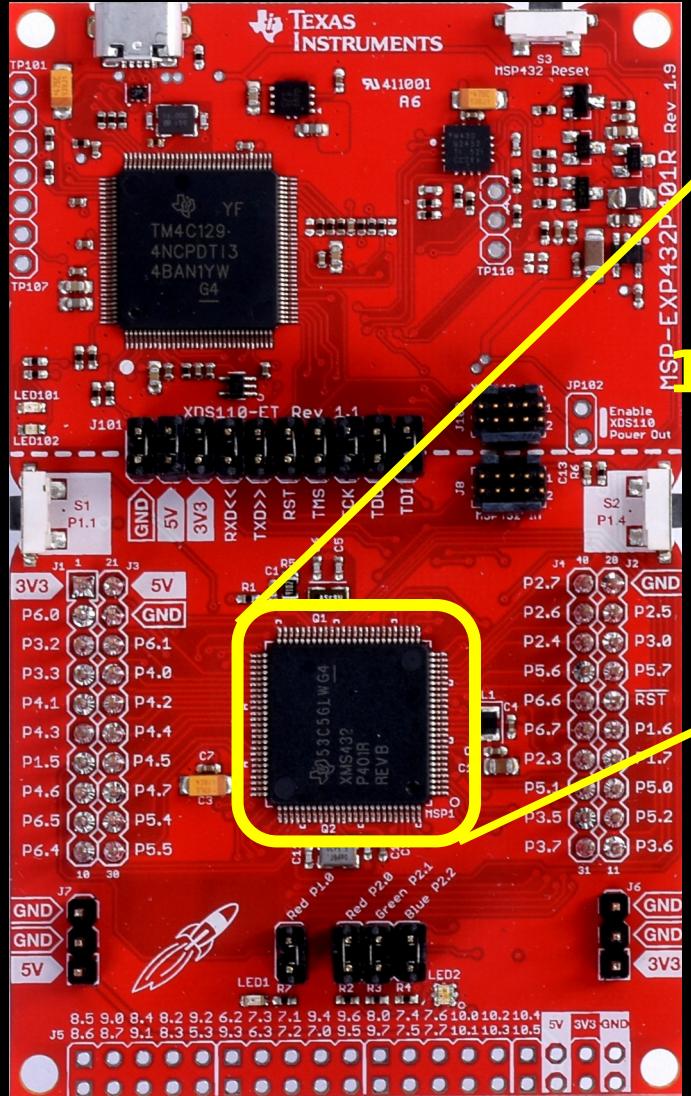
MSP432 Ports [S3b]



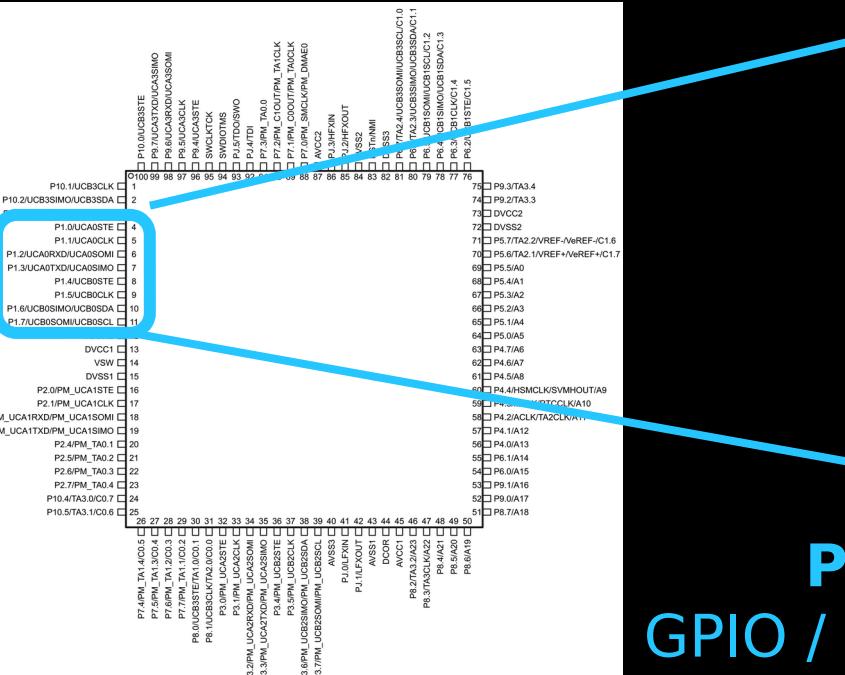
10 Ports

P1.0/UCB3CLK	1	P1.0/UCB3M0/UCB3SDA	2	P1.0/UCB3M0/UCB3SCL	3	P1.0/UCB3SOMI	4	P1.1/UCAC0CLK	5	P1.1/UCAD0STE	6	P1.2/UCARD10/UCAGSOMI	7	P1.2/UCARD10/UCAGSOMO	8	P1.3/UCB05CLK	9	P1.3/UCB05M0/UCB05SDA	10	P1.3/UCB05M0/UCB05SCL	11	VCCINT	12	VDDA	13	VSSA	14	DVS1	15	P2.0/PM_UCA1STE	16	P2.1/PM_UCA1CLK	17	P2.2/PM_UCA1RXD/PM_UCA1SOMI	18	P2.3/PM_UCA1TXD/PM_UCA1SOMO	19	P2.4/PM_TA0_1	20	P2.5/PM_TA0_2	21	P2.6/PM_TA0_3	22	P2.7/PM_TA0_4	23	P10.4/TA3.0/C0.7	24	P10.5/TA3.1/C0.6	25	P1.0/UCB3CLK	26	P1.0/UCB3M0/UCB3SDA	27	P1.0/UCB3M0/UCB3SCL	28	P1.0/UCB3SOMI	29	P1.1/UCAC0CLK	30	P1.1/UCAD0STE	31	P1.2/UCARD10/UCAGSOMI	32	P1.2/UCARD10/UCAGSOMO	33	P1.3/UCB05CLK	34	P1.3/UCB05M0/UCB05SDA	35	P1.3/UCB05M0/UCB05SCL	36	P1.4/PM_UCB3STE	37	P1.4/PM_UCB3CLK	38	P1.4/PM_UCB3M0/UCB3SDA	39	P1.4/PM_UCB3M0/UCB3SCL	40	P1.4/PM_UCB3SOMI	41	P1.5/PM_UCA1STE	42	P1.5/PM_UCA1CLK	43	P1.6/PM_UCA1RXD/PM_UCA1SOMI	44	P1.7/PM_UCA1TXD/PM_UCA1SOMO	45	P1.8/PM_TA0_1	46	P1.9/PM_TA0_2	47	P1.10/PM_TA0_3	48	P1.11/PM_TA0_4	49	P1.12/PM_TA0_5	50	P1.13/PM_TA0_6	51	P1.14/PM_TA0_7	52	P1.15/PM_TA0_8	53	P1.16/PM_TA0_9	54	P1.17/PM_TA0_10	55	P1.18/PM_TA0_11	56	P1.19/PM_TA0_12	57	P1.20/PM_TA0_13	58	P1.21/PM_TA0_14	59	P1.22/PM_TA0_15	60	P1.23/PM_TA0_16	61	P1.24/PM_TA0_17	62	P1.25/PM_TA0_18	63	P1.26/PM_TA0_19	64	P1.27/PM_TA0_20	65	P1.28/PM_TA0_21	66	P1.29/PM_TA0_22	67	P1.30/PM_TA0_23	68	P1.31/PM_TA0_24	69	P1.32/PM_TA0_25	70	P1.33/PM_TA0_26	71	P1.34/PM_TA0_27	72	P1.35/PM_TA0_28	73	P1.36/PM_TA0_29	74	P1.37/PM_TA0_30	75	P1.38/PM_TA0_31	76	P1.39/PM_TA0_32	77	P1.40/PM_TA0_33	78	P1.41/PM_TA0_34	79	P1.42/PM_TA0_35	80	P1.43/PM_TA0_36	81	P1.44/PM_TA0_37	82	P1.45/PM_TA0_38	83	P1.46/PM_TA0_39	84	P1.47/PM_TA0_40	85	P1.48/PM_TA0_41	86	P1.49/PM_TA0_42	87	P1.50/PM_TA0_43	88	P1.51/PM_TA0_44	89	P1.52/PM_TA0_45	90	P1.53/PM_TA0_46	91	P1.54/PM_TA0_47	92	P1.55/PM_TA0_48	93	P1.56/PM_TA0_49	94	P1.57/PM_TA0_50	95	P1.58/PM_TA0_51	96	P1.59/PM_TA0_52	97	P1.60/PM_TA0_53	98	P1.61/PM_TA0_54	99	P1.62/PM_TA0_55	100
--------------	---	---------------------	---	---------------------	---	---------------	---	---------------	---	---------------	---	-----------------------	---	-----------------------	---	---------------	---	-----------------------	----	-----------------------	----	--------	----	------	----	------	----	------	----	-----------------	----	-----------------	----	-----------------------------	----	-----------------------------	----	---------------	----	---------------	----	---------------	----	---------------	----	------------------	----	------------------	----	--------------	----	---------------------	----	---------------------	----	---------------	----	---------------	----	---------------	----	-----------------------	----	-----------------------	----	---------------	----	-----------------------	----	-----------------------	----	-----------------	----	-----------------	----	------------------------	----	------------------------	----	------------------	----	-----------------	----	-----------------	----	-----------------------------	----	-----------------------------	----	---------------	----	---------------	----	----------------	----	----------------	----	----------------	----	----------------	----	----------------	----	----------------	----	----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	----	-----------------	-----

MSP432 Ports [S3c]



10 Ports



P1.0/UCA0STE	<input type="checkbox"/>	4
P1.1/UCA0CLK	<input type="checkbox"/>	5
P1.2/UCA0RXD/UCA0SOMI	<input type="checkbox"/>	6
P1.3/UCA0TXD/UCA0SIMO	<input type="checkbox"/>	7
P1.4/UCB0STE	<input type="checkbox"/>	8
P1.5/UCB0CLK	<input type="checkbox"/>	9
P1.6/UCB0SIMO/UCB0SDA	<input type="checkbox"/>	10
P1.7/UCB0SOMI/UCB0SCL	<input type="checkbox"/>	11

Port 1 - 8 Pins
GPIO / Primary / Secondary

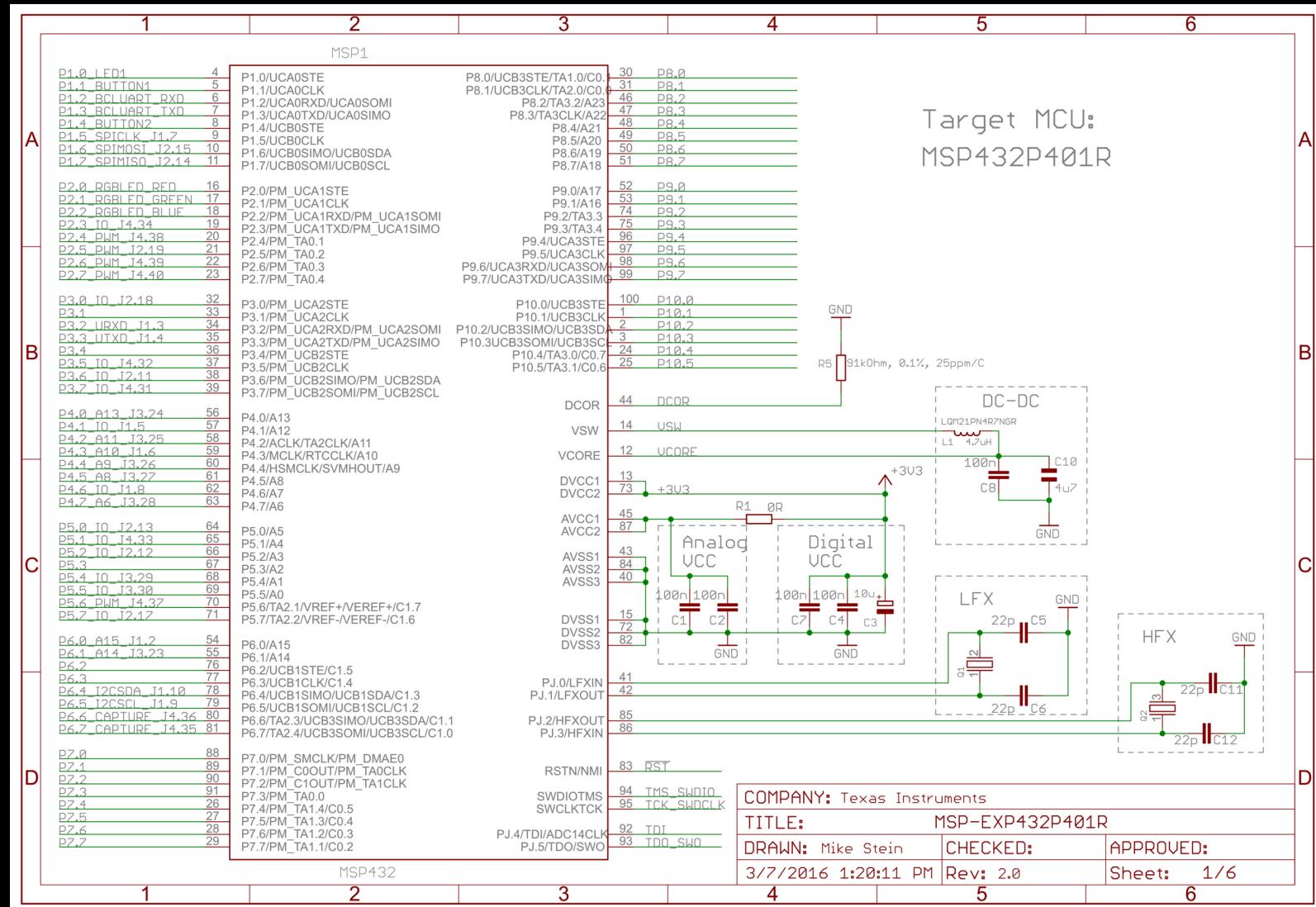
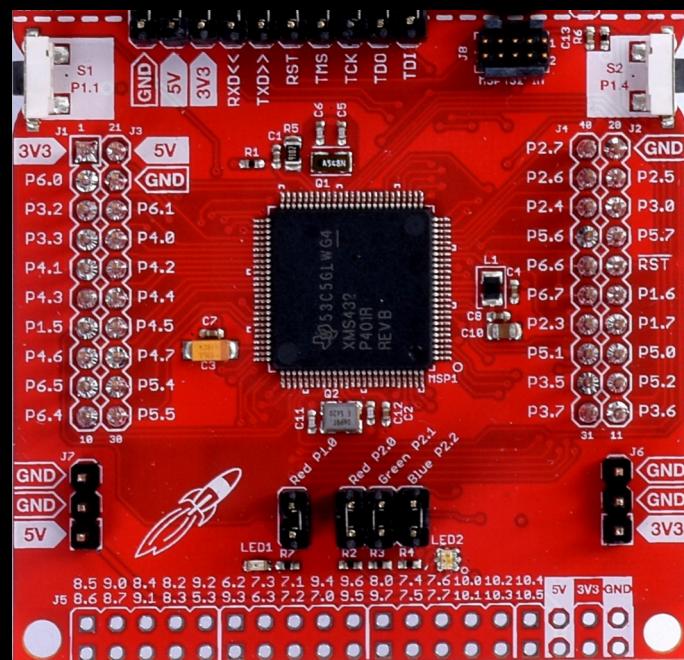
Port 1 Pin 0 = P1.0

Primary Mode = SPI Chip Select

Port 1 Pin 7 = P1.7

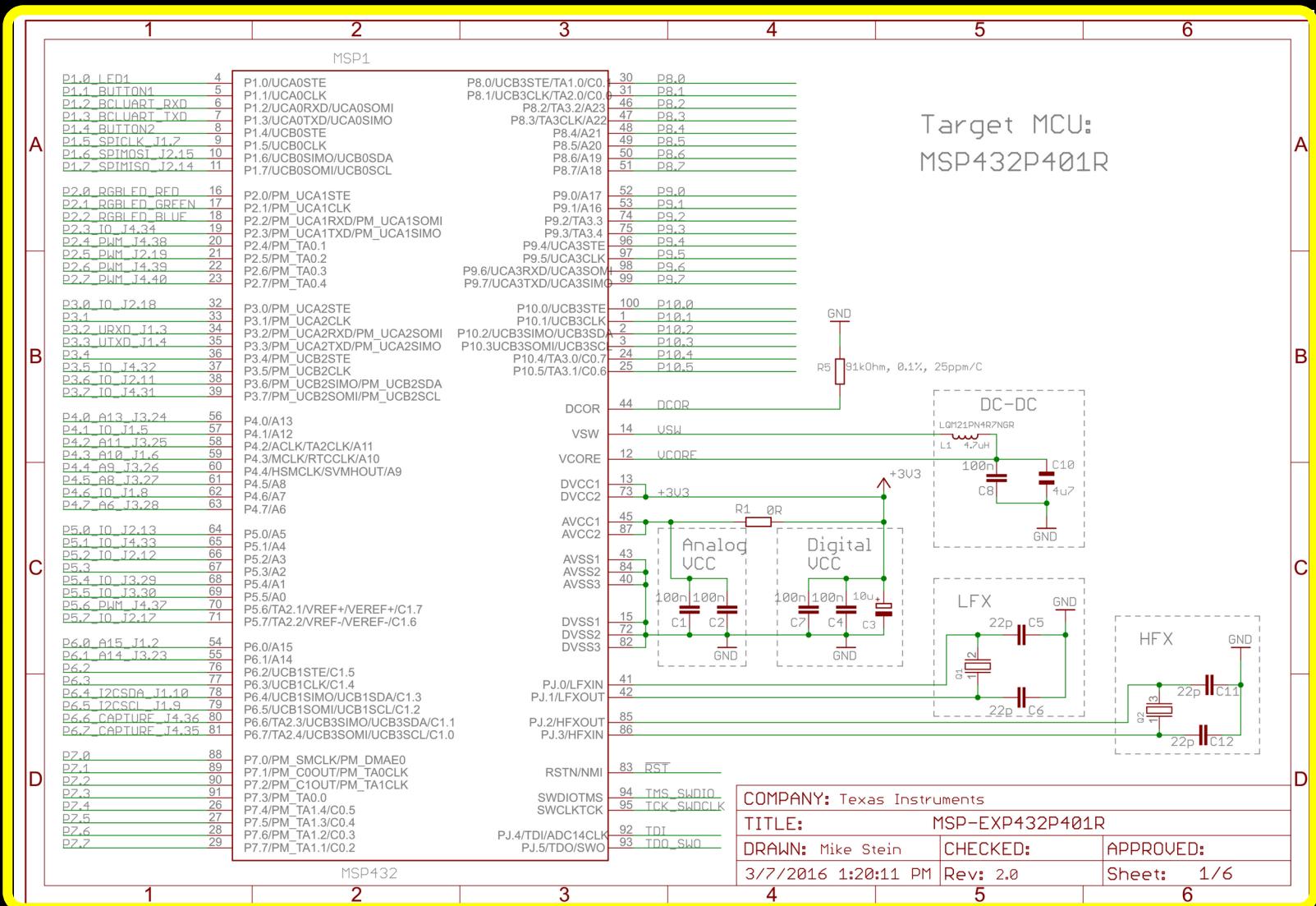
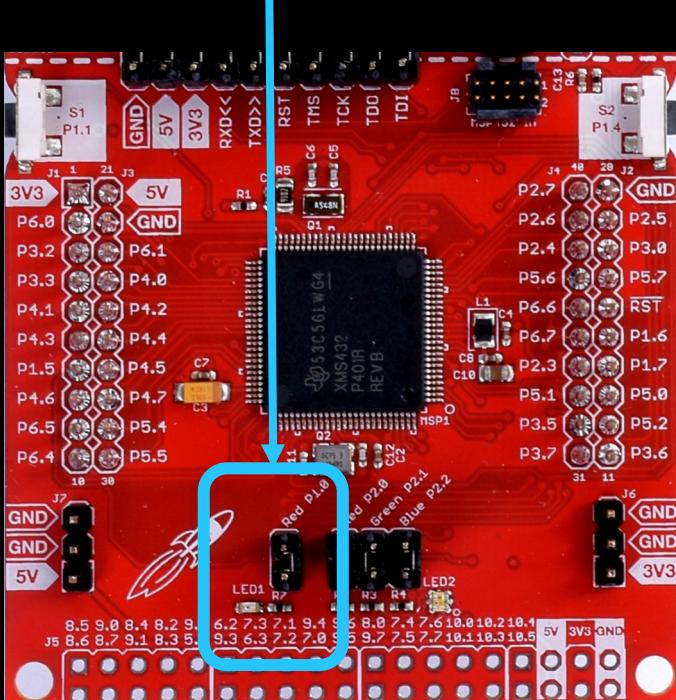
Primary Mode = SPI Slave-Out-Master-In Data (**UCB0SOMI**)
Secondary Mode = I²C Clock (**UCB0SCL**)

MSP432 Ports [S4a]

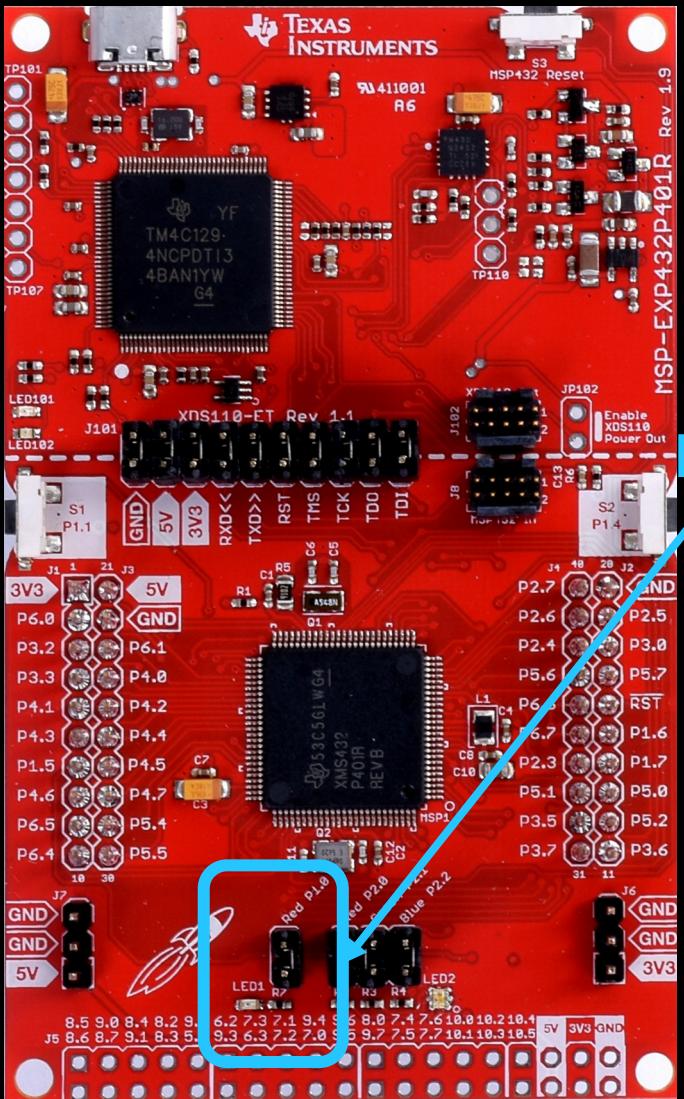


MSP432 Ports [S4b]

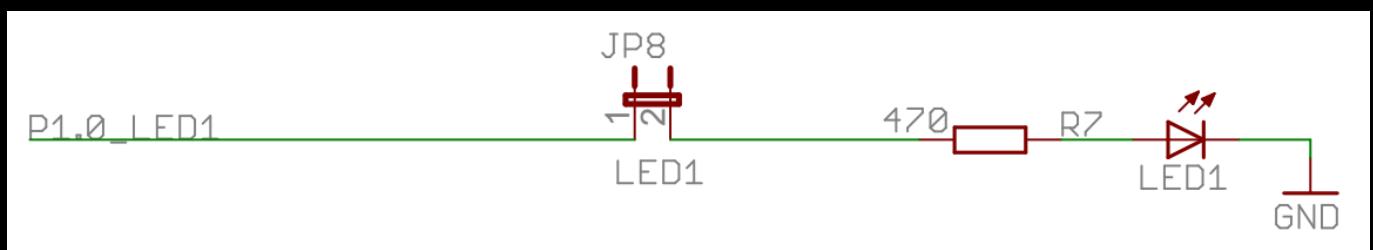
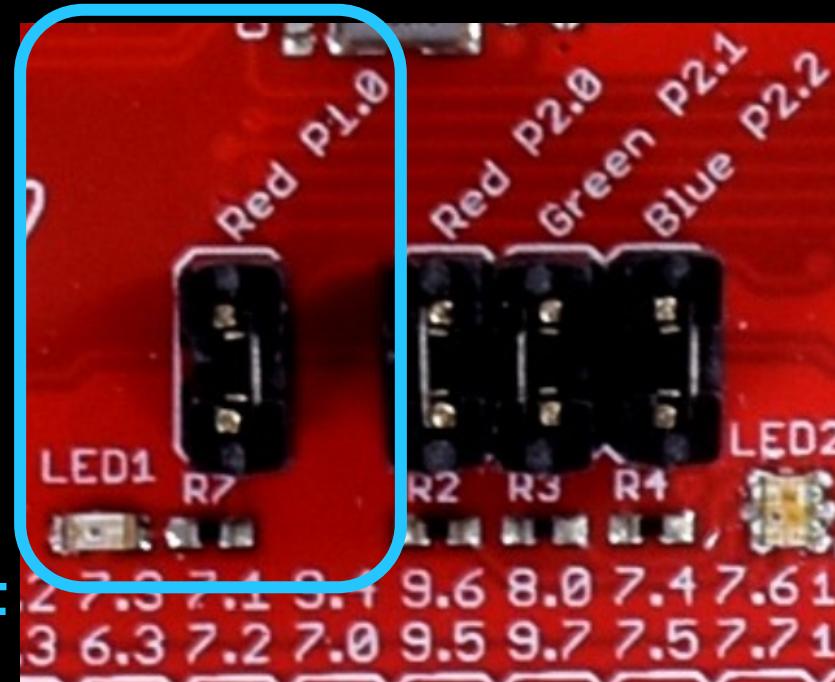
**LaunchPad Schematic:
Microcontroller Connections
P1.0 Red LED Circuit**



MSP432 Ports [S4a]

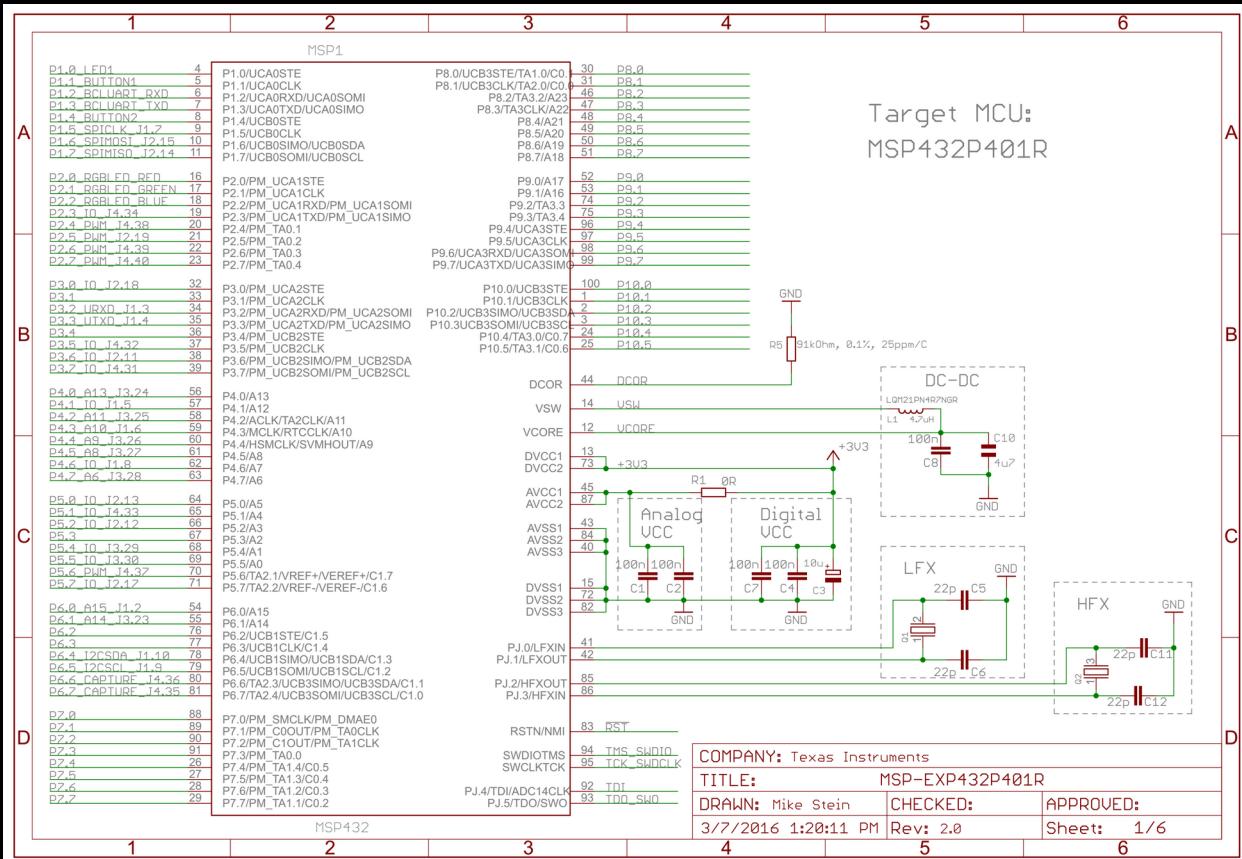


P1.0 Red LED Circuit



LED Schematic for P1.0

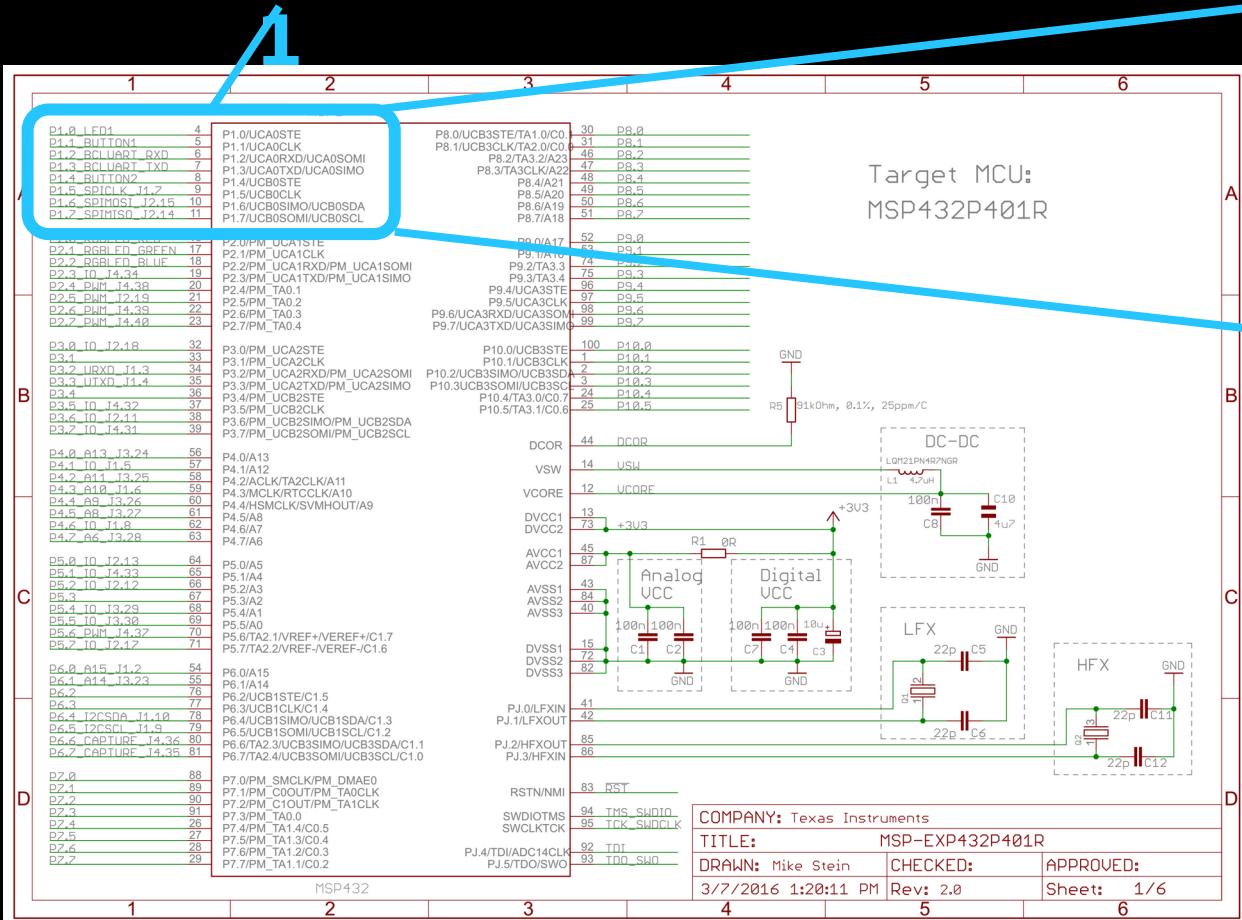
MSP432 Launchpad Schematic [S5a]



MSP432 Launchpad Schematic

[S5b]

MSP432 Port



P1.0_LFD1

P1.1_BUTTON1

P1.2_BCL_UART_RXD

P1.3_BCL_UART_TXD

P1.4_BUTTON2

P1.5_SPICLK_J1.7

P1.6_SPIMOST_J2.15

P1.7_SPIMISO_J2.14

P1.0/UCA0STE

P1.1/UCA0CLK

P1.2/UCA0RXD/UCA0SOMI

P1.3/UCA0TXD/UCA0SIMO

P1.4/UCB0STE

P1.5/UCB0CLK

P1.6/UCB0SOMI/UCB0SDA

P1.7/UCB0SIMO/UCB0SCL

Schematic Label for P1.0:
P1.0_LED1

P1.0_LFD1

JP8



1 2



RED LED Schematic

Launchpad Schematic:
MSP432 Pinout

MSP432 Launchpad Schematic [S5c]

MSP432 Pinout Port 1

P1.0_LFD1	4
P1.1_BUTTON1	5
P1.2_BCI_UART_RXD	6
P1.3_BCI_UART_TXD	7
P1.4_BUTTON2	8
P1.5_SPICLK_J1.7	9
P1.6_SPMOST_J2.15	10
P1.7_SPMISO_J2.14	11

Pin Number Modes



MSP432 Pin Descriptions

Table 6-32. Port P1 (P1.0 to P1.7) Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS OR SIGNALS ⁽¹⁾		
			P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA0STE	0	P1.0 (I/O)	I: 0; O: 1	0	0
		UCA0STE	X ⁽²⁾	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.1/UCA0CLK	1	P1.1 (I/O)	I: 0; O: 1	0	0
		UCA0CLK	X ⁽²⁾	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		
P1.2/UCA0RXD/UCA0SOMI	2	P1.2 (I/O)	I: 0; O: 1	0	0
		UCA0RXD/UCA0SOMI	X ⁽²⁾	0	1
		N/A	0	1	0
		DVSS	1		
		N/A	0	1	1
		DVSS	1		

MSP432 Launchpad Schematic [S5d]

MSP432 Pinout Port 1

P1.0_LFD1	4
P1.1_BUTTON1	5
P1.2_BCI_UART_RXD	6
P1.3_BCI_UART_TXD	7
P1.4_BUTTON2	8
P1.5_SPICLK_J1.7	9
P1.6_SPIMOSI_J2.15	10
P1.7_SPIMISO_J2.14	11

Pin Number Modes

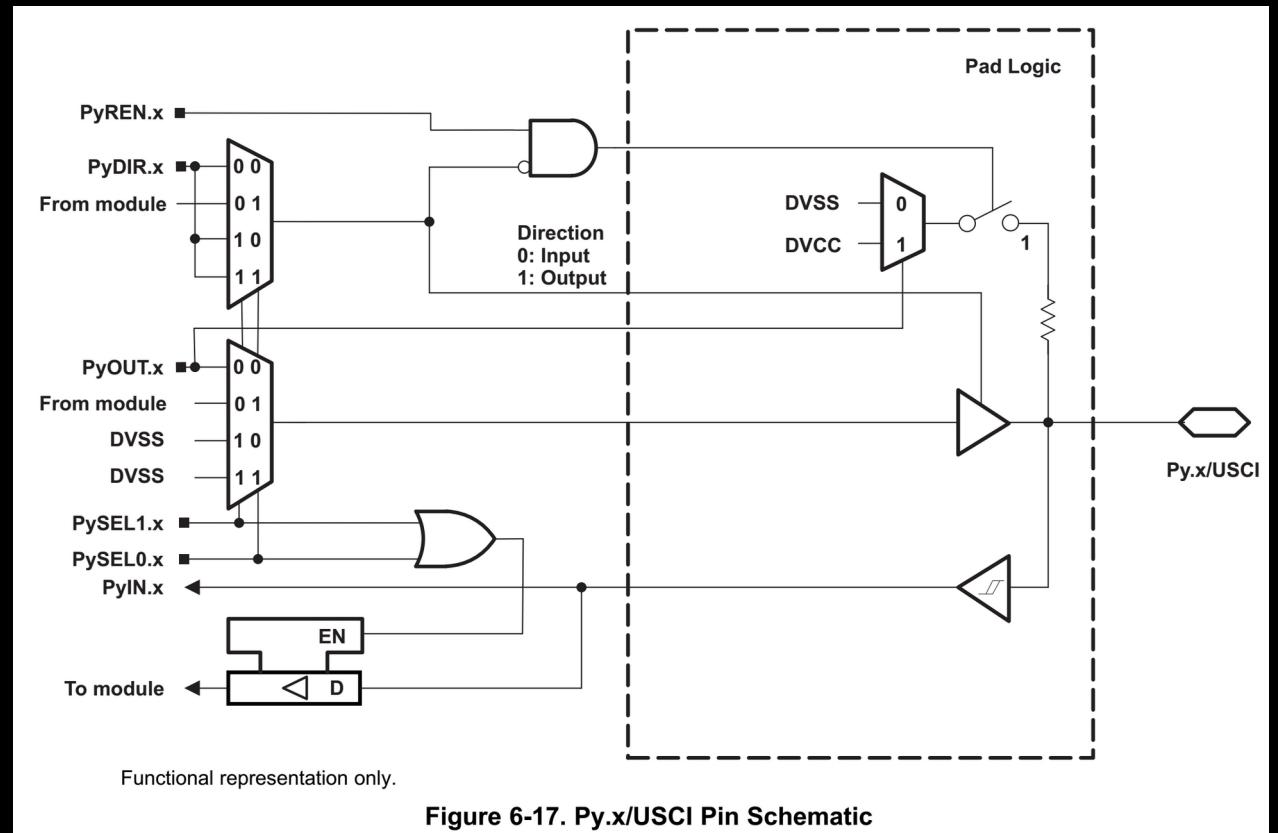
MSP432 Pin Descriptions

Table 6-32. Port P1 (P1.0 to P1.7) Pin Functions				
PIN NAME (P1.x)	x	CONTROL BITS OR SIGNALS (*)		
		P1DIR.x	P1SEL1.x	P1SEL0.x
P1.0/UCA0STE	0	P1.0 (I/O)	I: 0; O: 1	0
		UCA0STE	X ⁽²⁾	0
		N/A	0	1
		DVSS	1	0
		N/A	0	1
		DVSS	1	1
P1.1/UCA0CLK	1	P1.1 (I/O)	I: 0; O: 1	0
		UCA0CLK	X ⁽²⁾	0
		N/A	0	1
		DVSS	1	0
		N/A	0	1
		DVSS	1	1
P1.2/UCA0RXD/UCA0SOMI	2	P1.2 (I/O)	I: 0; O: 1	0
		UCA0RXD/UCA0SOMI	X ⁽²⁾	0
		N/A	0	1
		DVSS	1	0
		N/A	0	1
		DVSS	1	1

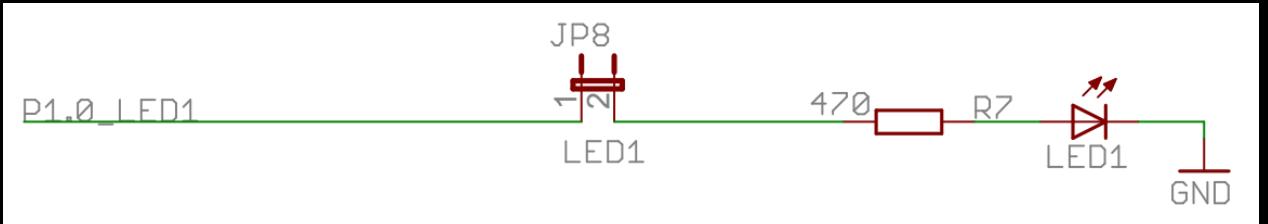
Port P1Sel0.x /P1Sel1.x
registers Select Mode for
each Pin in Port

Configuring the LED [S6a]

- To configure LED on P1.0¹

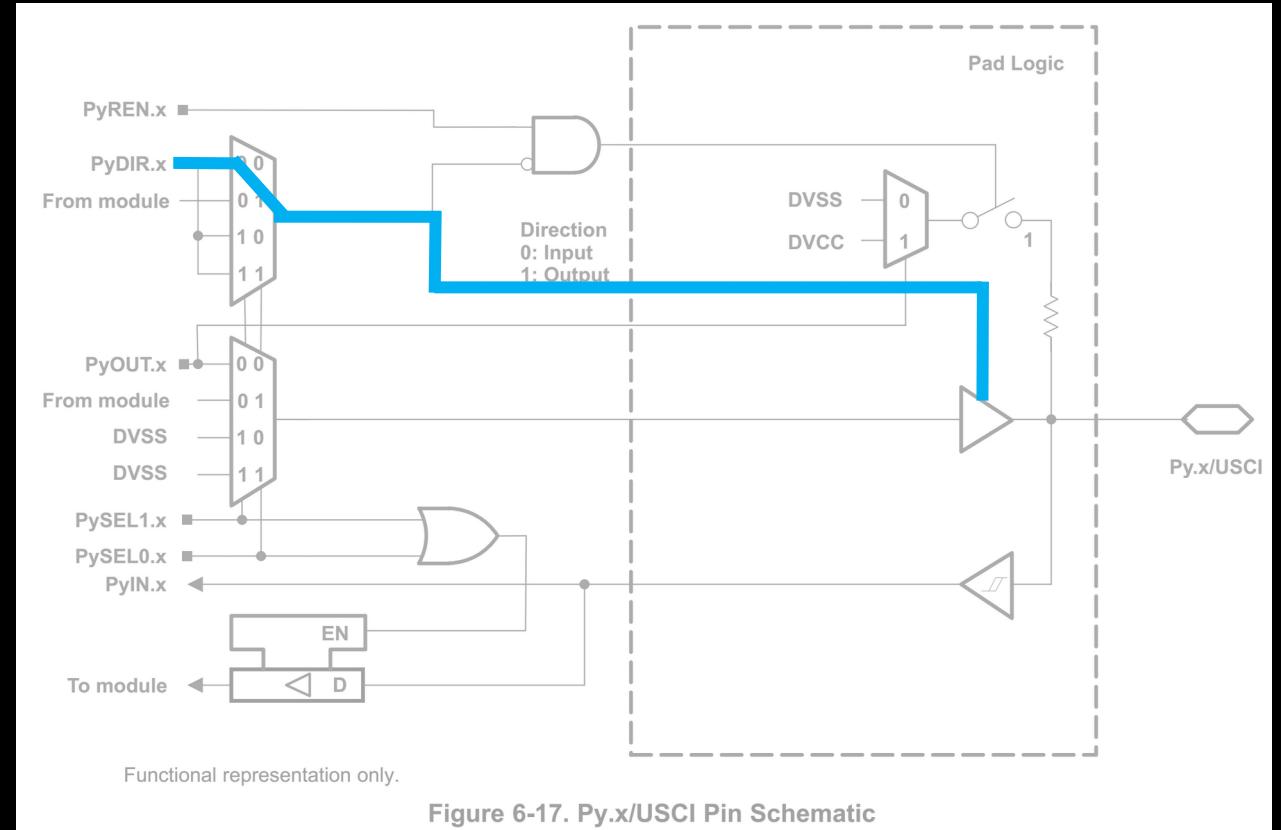


¹Also Required to Set Pin to I/O Mode (P1SELx). This is set by default

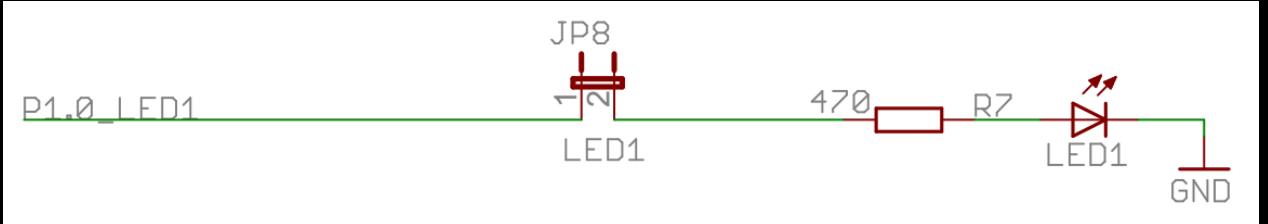


Configuring the LED [S6b]

- To configure LED on P1.0¹
 - Set direction to output
(P1DIR)

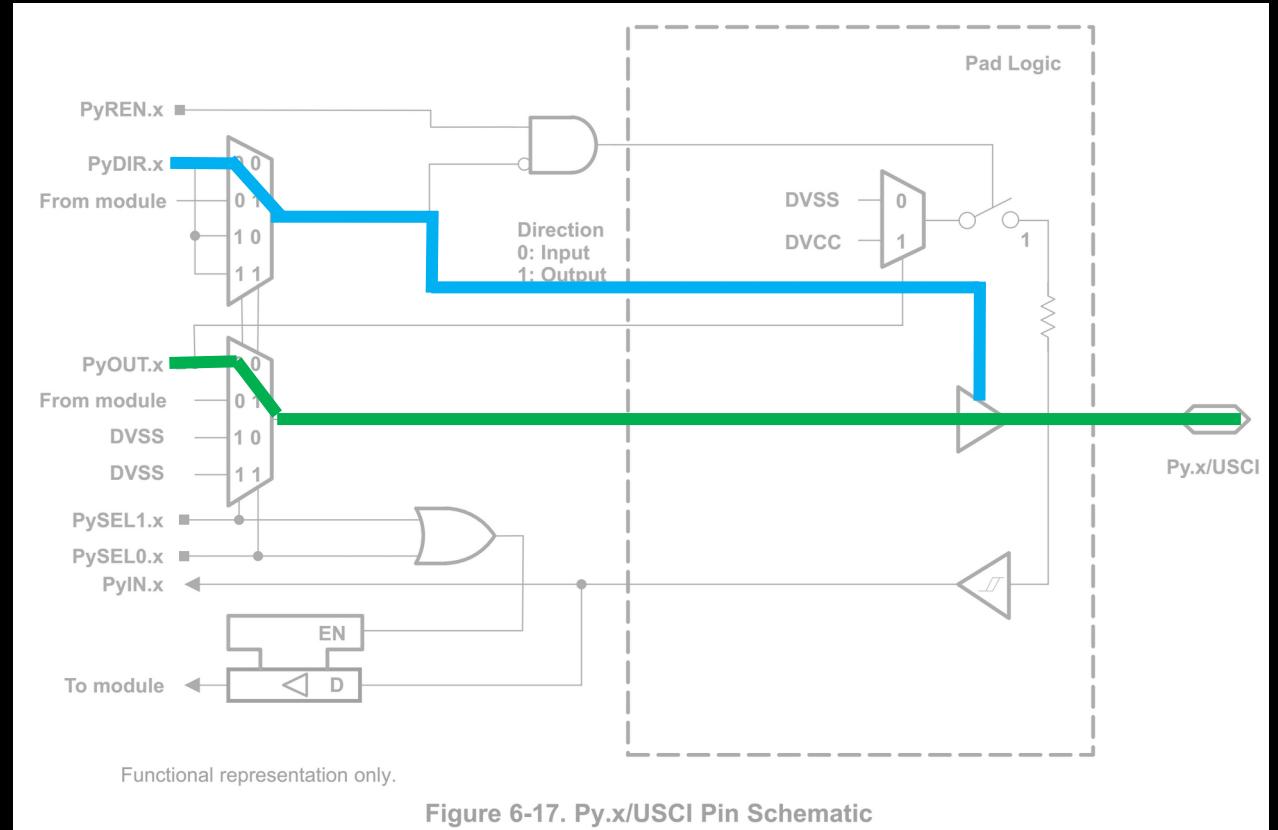


¹Also Required to Set Pin to I/O Mode (P1SELx). This is set by default

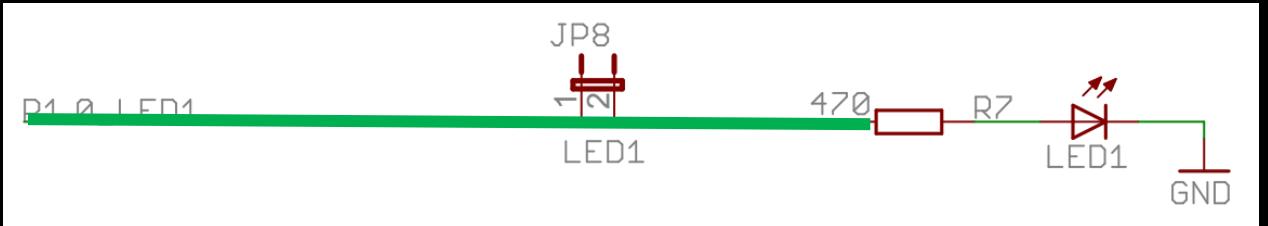


Configuring the LED [S6c]

- To configure LED on P1.0¹
 - Set direction to output (**P1DIR**)
 - Set P1.0 output to high (**P1OUT**)



¹Also Required to Set Pin to I/O Mode (P1SELx). This is set by default



Configuring the LED [S6d]

- To configure LED on P1.0¹
 - Set direction to output (**P1DIR**)
 - Set P1.0 output to high (**P1OUT**)
- To turn on LED, **P1.0_LED1** voltage needs to be a Logical HIGH ☐ VCC(3.3v)

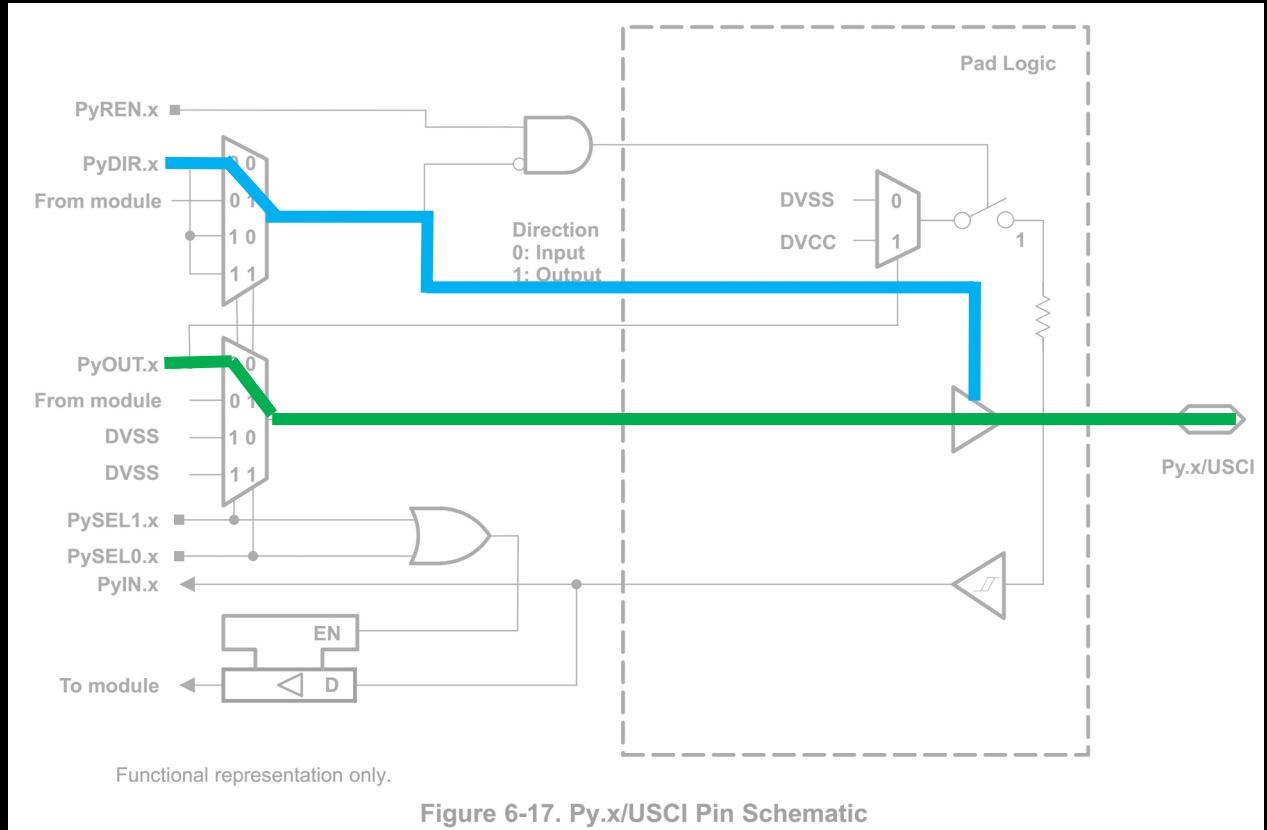
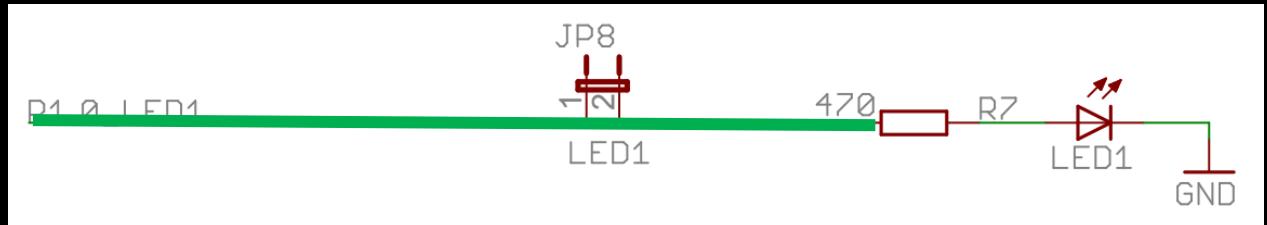


Figure 6-17. Py.x/USCI Pin Schematic



¹Also Required to Set Pin to I/O Mode (P1SELx). This is set by default

Configuring the LED [S6e]

- To configure LED on P1.0¹
 - Set direction to output (**P1DIR**)
 - Set P1.0 output to high (**P1OUT**)
- To turn on LED, **P1.0_LED1** voltage needs to be a Logical HIGH ☐ VCC(3.3v)

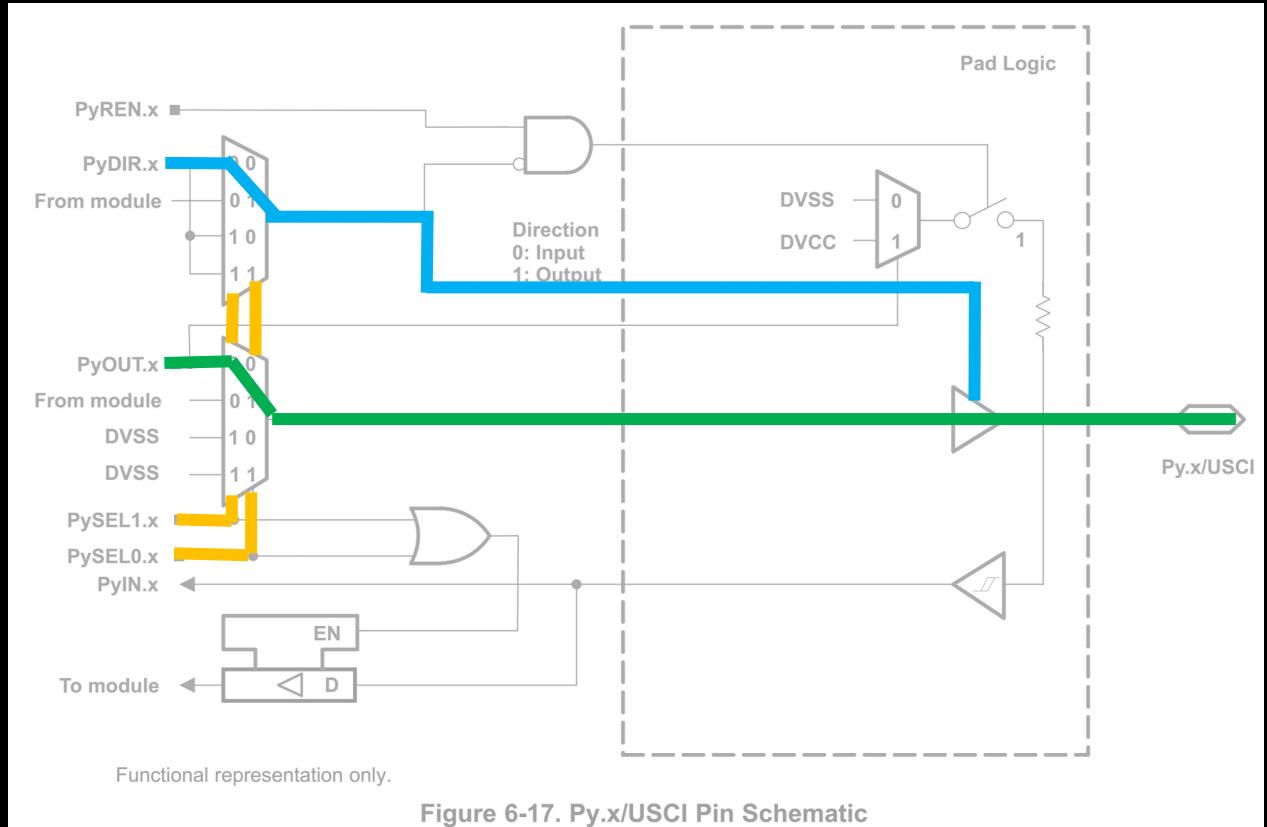
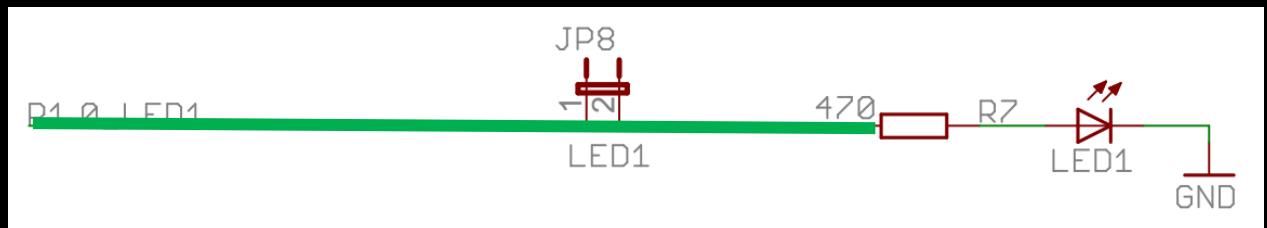


Figure 6-17. Py.x/USCI Pin Schematic



¹Also Required to Set Pin to I/O Mode (**P1SELx**). This is set by default

Configuring IO Port [S7a]

- Technical reference manual provides configuration steps
- Digital IO has own section
 - Important to read through this

www.ti.com

Digital I/O Introduction

10.1 Digital I/O Introduction

The digital I/O features include:

- Independently programmable individual I/Os
- Any combination of input or output
- Individually configurable interrupts for ports (available for certain ports only)
- Independent input and output data registers
- Individually configurable pullup or pulldown resistors
- Wake-up capability from ultra-low-power modes (available for certain ports only)
- Individually configurable high drive I/Os (available for certain I/Os only)

Devices within the family may have up to eleven digital I/O ports implemented (P1 to P10 and PJ). Most ports contain eight I/O lines; however, some ports may contain less (see the device-specific data sheet for ports available). Each I/O line is individually configurable for input or output direction, and each can be individually read or written. Each I/O line is individually configurable for pullup or pulldown resistors.

Certain ports have interrupt and wakeup capability from ultra-low-power modes (see device specific data sheet for ports with interrupt and wakeup capability). Each interrupt can be individually enabled and configured to provide an interrupt on a rising or falling edge of an input signal. All interrupts are fed into an encoded Interrupt Vector register, allowing the application to determine which sub-pin of a port has generated the event.

Individual ports can be accessed as byte-wide ports or can be combined into half-word-wide ports. Port pairs P1 and P2, P3 and P4, P5 and P6, P7 and P8, and so on, are associated with the names PA, PB, PC, PD, and so on, respectively. All port registers are handled in this manner with this naming convention. The main exception are the interrupt vector registers, for example, interrupts for ports P1 and P2 must be handled through P1IV and P2IV, PAIV does not exist.

When writing to port PA with half-word operations, all 16 bits are written to the port. When writing to the lower byte of port PA using byte operations, the upper byte remains unchanged. Similarly, writing to the upper byte of port PA using byte instructions leaves the lower byte unchanged. When writing to a port that contains less than the maximum number of bits possible, the unused bits are don't care. Ports PB, PC, PD, PE, and PF behave similarly.

Reading port PA using half-word operations causes all 16 bits to be transferred to the destination. Reading the lower or upper byte of port PA (P1 or P2) and storing to memory using byte operations causes only the lower or upper byte to be transferred to the destination, respectively. When reading from ports that contain fewer than the maximum bits possible, unused bits are read as zeros (similarly for port PJ).

Configuring IO Port [S7b]

- Two important registers
 - IO Direction Register (**P1DIR**)
 - IO Output Register (**P1OUT**)
- Register section provides the software configuration steps using Bit Manipulation

Table 10-3. Digital I/O Registers			
Offset	Acronym	Register Name	Section
0Eh	P1IV	Port 1 Interrupt Vector	Section 10.4.1
1Eh	P2IV	Port 2 Interrupt Vector	Section 10.4.1
2Eh	P3IV	Port 3 Interrupt Vector	Section 10.4.1
3Eh	P4IV	Port 4 Interrupt Vector	Section 10.4.1
4Eh	P5IV	Port 5 Interrupt Vector	Section 10.4.1
5Eh	P6IV	Port 6 Interrupt Vector	Section 10.4.1
6Eh	P7IV	Port 7 Interrupt Vector	Section 10.4.1
7Eh	P8IV	Port 8 Interrupt Vector	Section 10.4.1
8Eh	P9IV	Port 9 Interrupt Vector	Section 10.4.1
9Eh	P10IV	Port 10 Interrupt Vector	Section 10.4.1
00h	P1IN	Port 1 Input	Section 10.4.2
<hr/>			
02h	P1OUT or PAOUT_L	Port 1 Output	Section 10.4.3
04h	P1DIR or PADIR_L	Port 1 Direction	Section 10.4.4
06h	P1REN or PAREN_L	Port 1 Resistor Enable	Section 10.4.5
08h	P1DS or PADS_L	Port 1 Drive Strength	Section 10.4.6
0Ah	P1SEL0 or PASEL0_L	Port 1 Select 0	Section 10.4.7
0Ch	P1SEL1 or PASEL1_L	Port 1 Select 1	Section 10.4.8
16h	P1SELC or PASELC_L	Port 1 Complement Selection	Section 10.4.9
18h	P1IES or PAIES_L	Port 1 Interrupt Edge Select	Section 10.4.10
1Ah	P1IE or PAIE_L	Port 1 Interrupt Enable	Section 10.4.11
1Ch	P1IFG or PAIFG_L	Port 1 Interrupt Flag	Section 10.4.12

Configuring IO Port [S7c]

- Two important registers
 - IO Direction Register (**PxDIR**)
 - IO Output Register (**PxOUT**)
- PxOUT, PxDIR
 - X = Port Number
- Examples:
 - P2OUT
 - P1DIR

10.4.4 *PxDIR Register*

Port X Direction Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-4. PxDIR Register



Table 10-7. PxDIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port X direction. 0b = Port configured as input 1b = Port configured as output

10.4.3 *PxOUT Register*

Port X Output Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-3. PxOUT Register



Table 10-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port X output. When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

P1DIR Register [S8a]

- Port Direction Register sets pin to:
 - 0: an input
 - 1: an output

10.4.4 PxDIR Register

Port X Direction Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-4. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 10-7. PxDIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port X direction. 0b = Port configured as input 1b = Port configured as output

P1DIR Register [S8b]

- Port Direction Register sets pin to:
 - 0: an input
 - 1: an output

```
/* Configure P1.0 output */  
P1->DIR |= BIT0;
```

10.4.4 PxDIR Register

Port X Direction Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-4. PxDIR Register

7	6	5	4	3	2	1	0
PxDIR							
rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0	rw-0

Table 10-7. PxDIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port X direction. 0b = Port configured as input 1b = Port configured as output

P1DIR Register [S8a]

- Port Direction Register sets pin to:
 - 0: an input
 - 1: an output

```
/* Configure P1.0 output */  
P1->DIR |= BIT0;
```

rw-0: Bit is Read/Write & defaults to 0

10.4.4 PxDIR Register

Port X Direction Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-4. PxDIR Register



Table 10-7. PxDIR Register Description

Bit	Field	Type	Reset	Description
7-0	PxDIR	RW	0h	Port X direction. 0b = Port configured as input 1b = Port configured as output

P1OUT Register [S9a]

- Port Output Register sets output to:
 - 0: Output set to LOW (GND)
 - 1: Output set to HIGH (VCC)

10.4.3 PxOUT Register

Port X Output Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-3. PxOUT Register

7	6	5	4	3	2	1	0
PxOUT							
rw	rw	rw	rw	rw	rw	rw	rw

Table 10-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port X output. When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected

P1OUT Register [S9b]

- Port Output Register sets output to:
 - 0: Output set to LOW (GND)
 - 1: Output set to HIGH (VCC)

```
/* Configure P1.0
output */
P1->DIR |= BIT0;

/* Set P1.0 HIGH */
P1->OUT |= BIT0;
```

10.4.3 PxOUT Register

Port X Output Register (X = 1, 2, 3, 4, 5, 6, 7, 8, 9, 10 or J)

Figure 10-3. PxOUT Register



Table 10-6. PxOUT Register Description

Bit	Field	Type	Reset	Description
7-0	PxOUT	RW	Undefined	Port X output. When I/O configured to output mode: 0b = Output is low. 1b = Output is high. When I/O configured to input mode and pullups/pulldowns enabled: 0b = Pulldown selected 1b = Pullup selected