Design Verification Project
“SPI – Track”

Group members :

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Introduction:

This master plan defines the scope and strategy for the Design Verification Project, which is dedicated to verifying the Serial Peripheral Interface (SPI) and Wishbone protocols. It provides a structured overview of the verification phases, milestones, and objectives.

Phase1: building the SPI and WB UVCs

Deadline:
END of Monday , 19-March.

Overview:

1. Develop SPI UVC (Rahf)

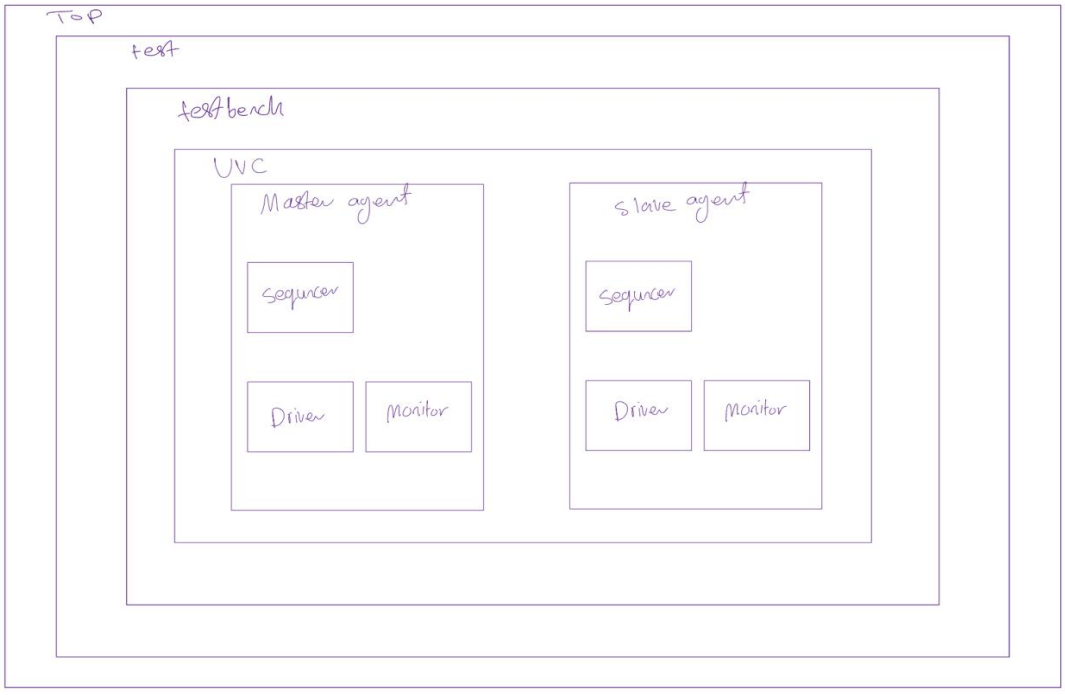
   Ensure that SPI transactions between Master and Slave function correctly.

2. Develop Wishbone UVC (Yasir)

   Ensure the Wishbone Master correctly generates bus transactions.

3. Verify SPI and Wishbone are Working Independently Before DUT Integration.

Architecture:
For both the SPI and WB



Verification Plan:

1. SPI UVC

No.	Test Case	Test Description	Test Type
1	**Basic Write Transaction**	SPI Master sends a single byte to Slave.	Directed
2	**Burst Write**	Master sends multiple bytes in sequence.	Directed
3	**SPI Mode Tests (0-3)**	Verify CPOL/CPHA combinations.	Directed
4	**Loop back Test**	MOSI connected to MISO to check data transfer.	Directed

2. WB UVC

No.	Test Case	Test Description	Test Type
1	**Write Transaction**	Generate data in master then ensure correct receive in slave side	Directed
2	**Read Transaction**	Generate data in slave then ensure correct receive in master side	Directed
3	**address = Data Transaction**	Send data to all SPI peripheral addresses (from master to sleave) and ensure correct receiving in slave	Directed
4	**Write Transaction to invalid address**	Send data to invalid addresses (from master to sleave) and ensure error response	Directed
7	**Stress test**	Perform random transactions write transactions & read transactions	Ranadom

Phase2: Test each DUT separately using its corresponding UVC.

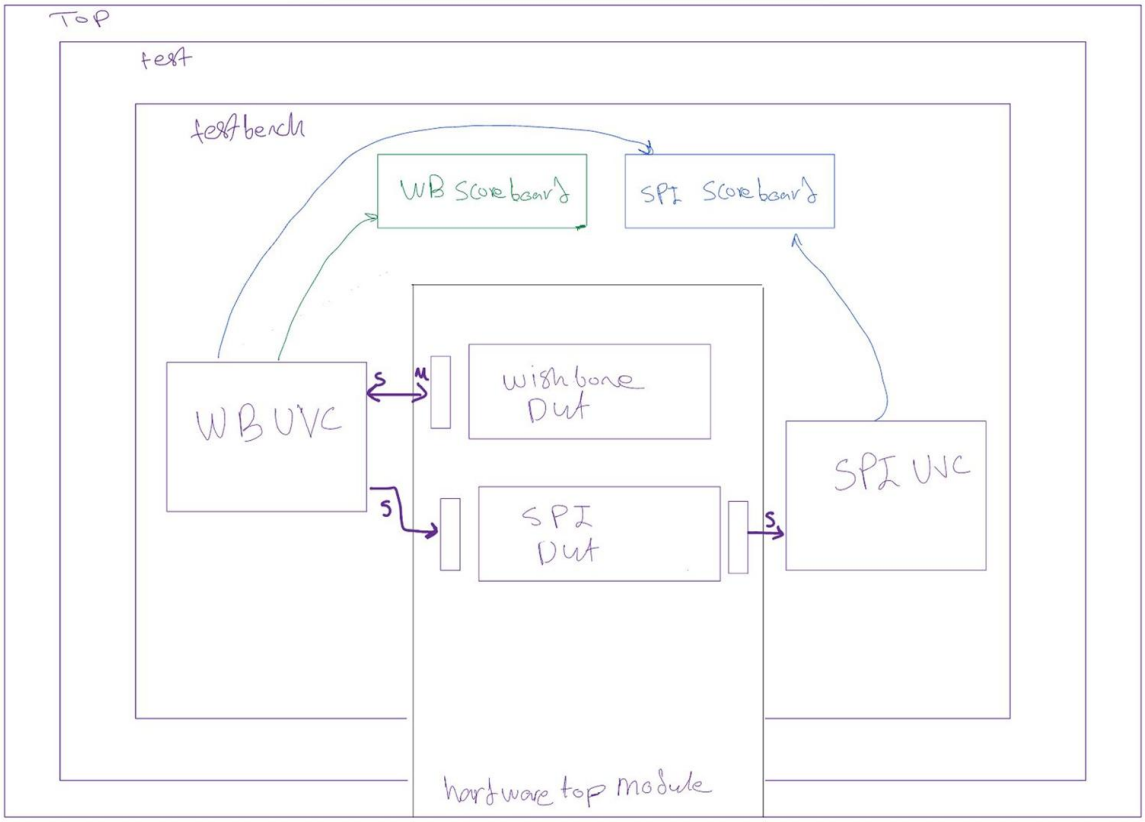
Deadline:
End of Tuesday, 18-March.

Overview:

This phase ensures that each DUT functions correctly within its UVC before moving to full system integration.

1. **SPI & Wishbone UVC Integration:**
    - Connect the SPI and Wishbone UVCs to their respective DUTs.
    - Verify correct interaction between the interfaces and the DUTs.
2. **End-to-End Data Flow Verification:**
    - Ensure SPI Master transactions are processed correctly by the SPI DUT and translated into Wishbone transactions.
    - Validate that responses from the Wishbone Slave are correctly received by the SPI Master.

Architecture:



Verification Plan:

TBC.

Phase 3: Integration of SPI DUT & WB DUT together.

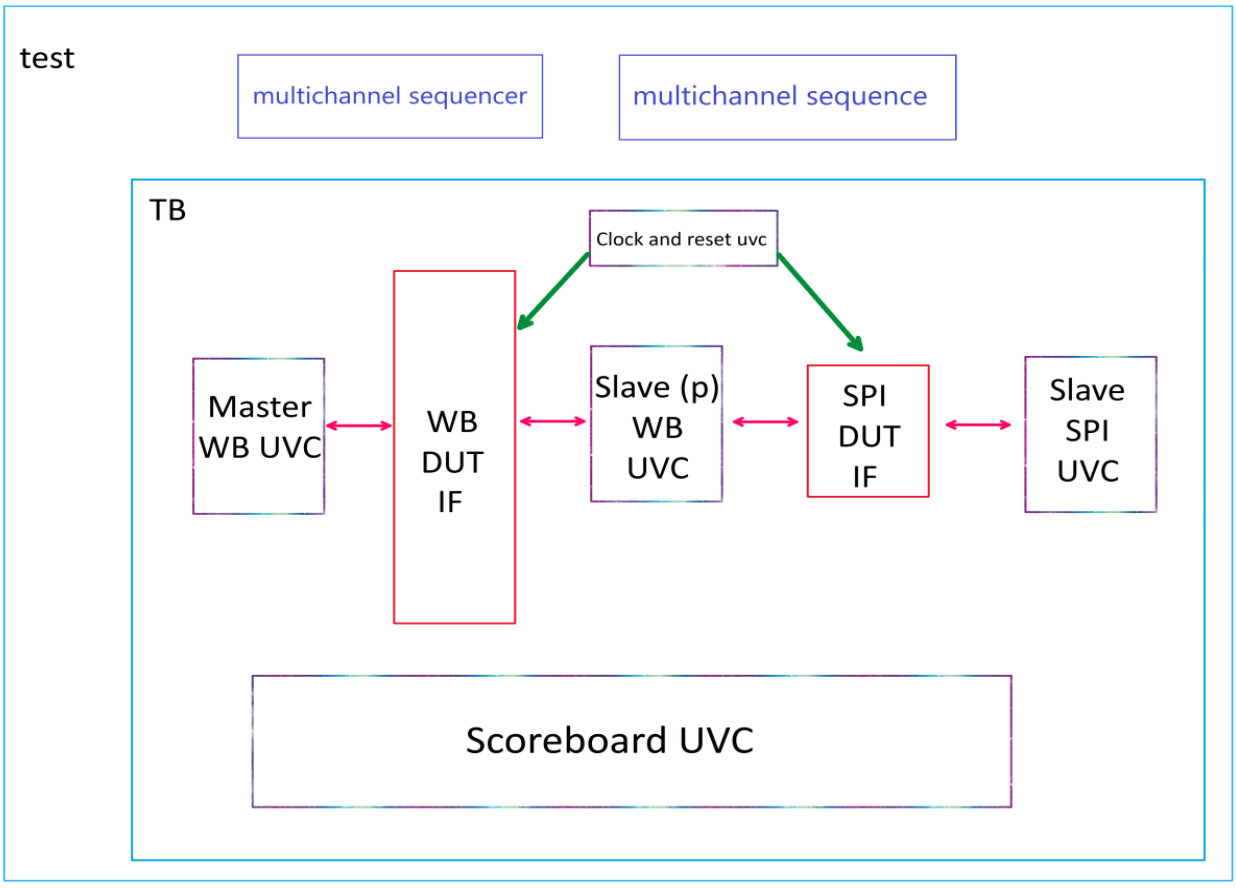
Deadline:
END of Wednesday, 19-March.

Overview:

This phase consists of two primary tasks:

1. Integrating SPI DUT and WB DUT into single testbench.
2. Developing a scoreboard module UVC.
3. create a clock and rest UVC which will generate the clock and reset signal to the system.

Architecture:



Path 1: Integration of SPI DUT & WB DUT into the Testbench

Description:

1. integrate SPI DUT and WB DUT into the testbench while ensuring smooth interaction between three UVCs:

- **WB Master Agent:** Generates packets, sends them to WB DUT, and receives packets from SPI DUT via WB DUT.
- **WB Passive Slave Agent:** Monitors traffic between SPI DUT and WB DUT.
- **SPI Slave Agent (Passive Mode):** Collects packets from SPI DUT and generates/sends packets to SPI DUT.

This will be done by creating a multichannel sequencer and a multichannel sequence.

2. create a clock and rest UVC which will generate the clock and reset signal to the system

Verification Plan:
TBC.

Path 2: Development of Scoreboard Module UVC

Description:
Develop a scoreboard module UVC with a reference model to verify the three UVCs (WB Master, WB Passive Slave, and SPI Slave).

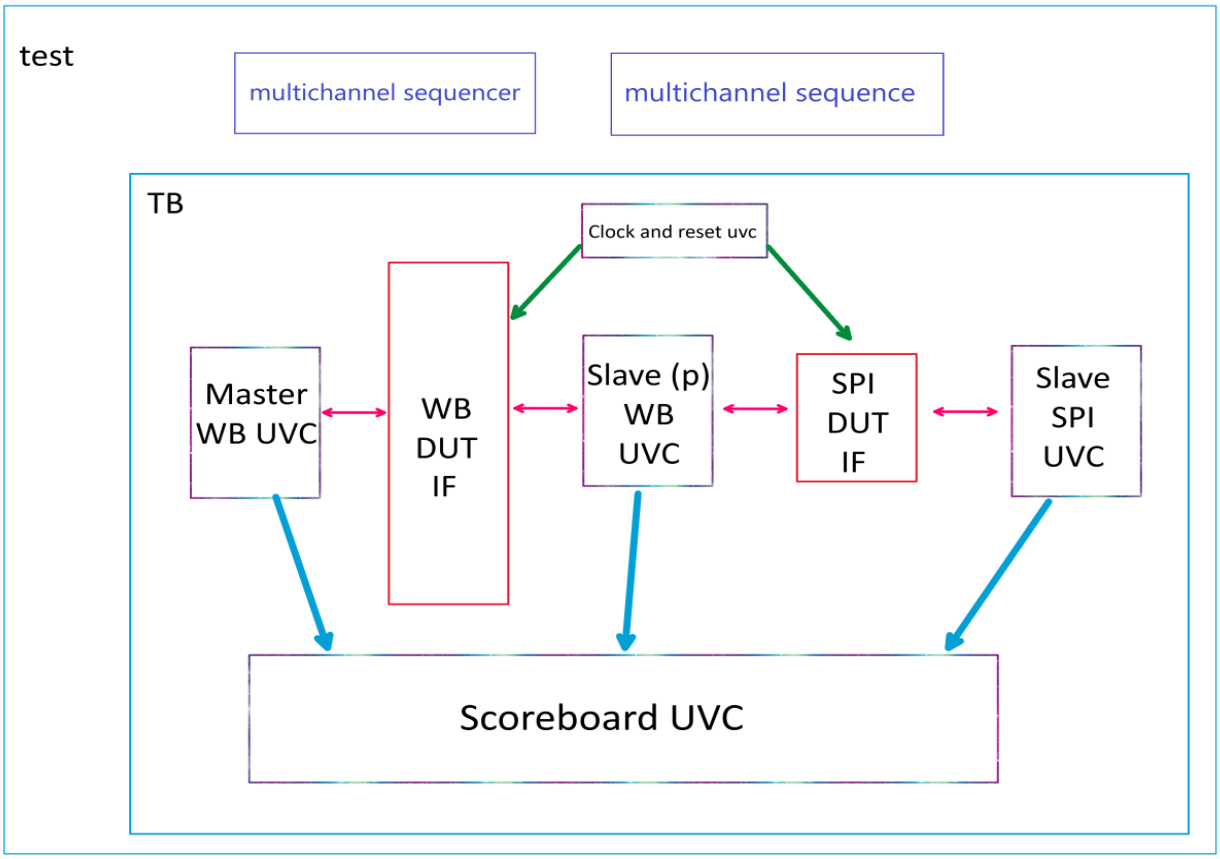
Verification Plan:
TBC.

Phase 4: Integration of Interface UVCs and Scoreboard Module UVCs

Deadline:
END of Thursday, 20-March.

Overview:
This phase focuses on integrating all components and performing the final test.

Architecture:



Verification Plan:
TBC.