CX-301: Project

Wishbone Interconnect Specifications

Version 1.1

1. Overview

This Wishbone Interconnect is a simple router that directs transactions from the master to the correct peripheral based on the address. It supports a 32-bit address and 32-bit data bus and uses standard Wishbone signals. The data bus is bidirectional, meaning data flows from the master to the slave during write transactions and from the slave to the master during read transactions.

2. Address Mapping

Transactions are routed using the following address ranges:

Peripheral	Address Range (Hex)
SPI_1	0x00000000 – 0x0000000F
SPI_2	0x00000010 – 0x0000001F
UART	0x00000020 – 0x0000003F

Any transaction with an address outside these ranges should generate an error response.

3. Operation

Address Decoding & Routing:
The interconnect decodes the incoming 32-bit address and routes the transaction as follows:

- Addresses 0–15 → SPI_1
- Addresses 16–31 → SPI_2
- Addresses 32–63 → UART

Data Transfer:
The interconnect supports bidirectional data flow:

Write Transactions: Data flows from the master to the targeted slave. STB signal acts as a slave select and is one for only the targeted slave. Other signals, like data, address, control signals are forwarded to all the slaves. Because the slave select (STB) is one for only the targeted slave. Other slaves will simply ignore this transaction.
Read Transactions: Data flows from the targeted slave back to the master. In this case a multiplexer selects the Read Data from the targeted slave according to the address range.

Error Handling:
If an address falls outside the defined ranges, the interconnect returns an error signal.

4. Interface Signals

- **Address (ADR):** 32-bit input
- **Data (DAT):** 32-bit bidirectional bus
- **Control Signals:** Standard Wishbone signals (e.g., WE, STB, ACK) are used as defined by the SPI and UART peripherals.

5. Conclusion

This Wishbone Interconnect acts as a simple router, directing transactions to SPI_1, SPI_2, or UART based on the address. It supports both write (master-to-slave) and read (slave-to-master) transactions on its bidirectional data bus, and it flags any invalid addresses with an error.