

be introduced into the PSpice library without modifying the procedures already described. In this sense, use of the PSpice package is a true "building experience" with the possibility of analyzing some very complicated networks only a few statements away.

PSpice Windows Design Center Analysis

The transistor selection under PSpice Windows is found by first clicking **Draw** on the menu bar of the **Schematics** window. Next choose **Get New Part** followed by **Browse** to view the available list. Find **eval.slb** in the **library** list and after clicking the entry move through the list of available devices. As you click from one item to the next, a **Description** box will appear above the entry describing the type of device. Once the transistor of choice is chosen, simply click on the device and **OK**; it will appear on the screen for placement. Chapter 4 will describe how to modify the parameters of the chosen transistor and how to perform an analysis of the transistor network.

§ 3.2 Transistor Construction

PROBLEMS

1. What names are applied to the two types of BJT transistors? Sketch the basic construction of each and label the various minority and majority carriers in each. Draw the graphic symbol next to each. Is any of this information altered by changing from a silicon to a germanium base?
2. What is the major difference between a bipolar and a unipolar device?

§ 3.3 Transistor Operation

3. How must the two transistor junctions be biased for proper transistor amplifier operation?
4. What is the source of the leakage current in a transistor?
5. Sketch a figure similar to Fig. 3.3 for the forward-biased junction of an *npn* transistor. Describe the resulting carrier motion.
6. Sketch a figure similar to Fig. 3.4 for the reverse-biased junction of an *npn* transistor. Describe the resulting carrier motion.
7. Sketch a figure similar to Fig. 3.5 for the majority- and minority-carrier flow of an *npn* transistor. Describe the resulting carrier motion.
8. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?
9. If the emitter current of a transistor is 8 mA and I_B is 1/100 of I_C , determine the levels of I_C and I_B .

§ 3.4 Common-Base Configuration

10. From memory, sketch the transistor symbol for a *pnp* and an *npn* transistor, and then insert the conventional flow direction for each current.
11. Using the characteristics of Fig. 3.7, determine V_{BE} at $I_E = 5$ mA for $V_{CB} = 1$ V, 10 V, and 20 V. Is it reasonable to assume on an approximate basis that V_{CB} has only a slight effect on the relationship between V_{BE} and I_E ?
12. (a) Determine the average ac resistance for the characteristics of Fig. 3.10b.
(b) For networks in which the magnitude of the resistive elements is typically in kilohms, is the approximation of Fig. 3.10c a valid one [based on the results of part (a)]?
13. (a) Using the characteristics of Fig. 3.8, determine the resulting collector current if $I_E = 4.5$ mA and $V_{CB} = 4$ V.
(b) Repeat part (a) for $I_E = 4.5$ mA and $V_{CB} = 16$ V.
(c) How have the changes in V_{CB} affected the resulting level of I_C ?
(d) On an approximate basis, how are I_E and I_C related based on the results above?

- 14.** (a) Using the characteristics of Figs. 3.7 and 3.8, determine I_C if $V_{CB} = 10$ V and $V_{BE} \approx 800$ mV.
 (b) Determine V_{BL} if $I_C = 5$ mA and $V_{CB} = 10$ V.
 (c) Repeat part (b) using the characteristics of Fig. 3.10b.
 (d) Repeat part (b) using the characteristics of Fig. 3.10c.
 (e) Compare the solutions for V_{BL} for parts (b), (c), and (d). Can the difference be ignored if voltage levels greater than a few volts are typically encountered?
- 15.** (a) Given an α_{dc} of 0.998, determine I_C if $I_E = 4$ mA.
 (b) Determine α_{dc} if $I_E = 2.8$ mA and $I_B = 20$ μ A.
 (c) Find I_E if $I_B = 40$ μ A and α_{dc} is 0.98.
- 16.** From memory, and memory only, sketch the common-base BJT transistor configuration (for *npn* and *pnp*) and indicate the polarity of the applied bias and resulting current directions.

§ 3.5 Transistor Amplifying Action

- 17.** Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if $V_i = 500$ mV and $R = 1$ k Ω . (The other circuit values remain the same.)
- 18.** Calculate the voltage gain ($A_v = V_L/V_i$) for the network of Fig. 3.12 if the source has an internal resistance of 100 Ω in series with V_i .

§ 3.6 Common-Emitter Configuration

- 19.** Define I_{CBO} and I_{CEO} . How are they different? How are they related? Are they typically close in magnitude?
- 20.** Using the characteristics of Fig. 3.14:
 (a) Find the value of I_C corresponding to $V_{BE} = +750$ mV and $V_{CE} = +5$ V.
 (b) Find the value of V_{CE} and V_{BE} corresponding to $I_C = 3$ mA and $I_B = 30$ μ A.
- * **21.** (a) For the common-emitter characteristics of Fig. 3.14, find the dc beta at an operating point of $V_{CE} = +8$ V and $I_C = 2$ mA.
 (b) Find the value of α corresponding to this operating point.
 (c) At $V_{CE} = +8$ V, find the corresponding value of I_{CEO} .
 (d) Calculate the approximate value of I_{CBO} using the dc beta value obtained in part (a).
- * **22.** (a) Using the characteristics of Fig. 3.14a, determine I_{CEO} at $V_{CE} = 10$ V.
 (b) Determine β_{dc} at $I_B = 10$ μ A and $V_{CE} = 10$ V.
 (c) Using the β_{dc} determined in part (b), calculate I_{CBO} .
- 23.** (a) Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 80$ μ A and $V_{CE} = 5$ V.
 (b) Repeat part (a) at $I_B = 5$ μ A and $V_{CE} = 15$ V.
 (c) Repeat part (a) at $I_B = 30$ μ A and $V_{CE} = 10$ V.
 (d) Reviewing the results of parts (a) through (c), does the value of β_{dc} change from point to point on the characteristics? Where were the higher values found? Can you develop any general conclusions about the value of β_{dc} on a set of characteristics such as those provided in Fig. 3.14a?
- * **24.** (a) Using the characteristics of Fig. 3.14a, determine β_{ac} at $I_B = 80$ μ A and $V_{CE} = 5$ V.
 (b) Repeat part (a) at $I_B = 5$ μ A and $V_{CE} = 15$ V.
 (c) Repeat part (a) at $I_B = 30$ μ A and $V_{CE} = 10$ V.
 (d) Reviewing the results of parts (a) through (c), does the value of β_{ac} change from point to point on the characteristics? Where are the high values located? Can you develop any general conclusions about the value of β_{ac} on a set of collector characteristics?
 (e) The chosen points in this exercise are the same as those employed in Problem 23. If Problem 23 was performed, compare the levels of β_{dc} and β_{ac} for each point and comment on the trend in magnitude for each quantity.
- 25.** Using the characteristics of Fig. 3.14a, determine β_{dc} at $I_B = 25$ μ A and $V_{CE} = 10$ V. Then calculate α_{dc} and the resulting level of I_E . (Use the level of I_C determined by $I_C = \beta_{dc}I_B$.)
- 26.** (a) Given that $\alpha_{dc} = 0.987$, determine the corresponding value of β_{dc} .
 (b) Given $\beta_{dc} = 120$, determine the corresponding value of α .
 (c) Given that $\beta_{dc} = 180$ and $I_C = 2.0$ mA, find I_E and I_B .

27. From memory, and memory only, sketch the common-emitter configuration (for *npn* and *pnp*) and insert the proper biasing arrangement with the resulting current directions for I_B , I_C , and I_E .

§ 3.7 Common-Collector Configuration

28. An input voltage of 2 V rms (measured from base to ground) is applied to the circuit of Fig. 3.21. Assuming that the emitter voltage follows the base voltage exactly and that V_{be} (rms) = 0.1 V, calculate the circuit voltage amplification ($A_v = V_o/V_i$) and emitter current for $R_E = 1 \text{ k}\Omega$.
29. For a transistor having the characteristics of Fig. 3.14, sketch the input and output characteristics of the common-collector configuration.

§ 3.8 Limits of Operation

30. Determine the region of operation for a transistor having the characteristics of Fig. 3.14 if $I_{C_{\max}} = 7 \text{ mA}$, $V_{CE_{\max}} = 17 \text{ V}$, and $P_{C_{\max}} = 40 \text{ mW}$.
31. Determine the region of operation for a transistor having the characteristics of Fig. 3.8 if $I_{C_{\max}} = 6 \text{ mA}$, $V_{CB_{\max}} = 15 \text{ V}$, and $P_{C_{\max}} = 30 \text{ mW}$.

§ 3.9 Transistor Specification Sheet

32. Referring to Fig. 3.23, determine the temperature range for the device in degrees Fahrenheit.
33. Using the information provided in Fig. 3.23 regarding $P_{D_{\max}}$, $V_{CE_{\max}}$, $I_{C_{\max}}$ and $V_{CE_{ss}}$, sketch the boundaries of operation for the device.
34. Based on the data of Fig. 3.23, what is the expected value of I_{CEO} using the average value of β_{dc} ?
35. How does the range of h_{FE} (Fig. 3.23(j), normalized from $h_{FE} = 100$) compare with the range of h_{fe} (Fig. 3.23(f)) for the range of I_C from 0.1 mA to 10 mA?
36. Using the characteristics of Fig. 3.23b, determine whether the input capacitance in the common-base configuration increases or decreases with increasing levels of reverse bias potential. Can you explain why?
- * 37. Using the characteristics of Fig. 3.23f, determine how much the level of h_{fe} has changed from its value at 1 mA to its value at 10 mA. Note that the vertical scale is a log scale that may require reference to Section 11.2. Is the change one that should be considered in a design situation?
- * 38. Using the characteristics of Fig. 3.23j, determine the level of β_{dc} at $I_C = 10 \text{ mA}$ at the three levels of temperature appearing in the figure. Is the change significant for the specified temperature range? Is it an element to be concerned about in the design process?

§ 3.10 Transistor Testing

39. (a) Using the characteristics of Fig. 3.24, determine β_{ac} at $I_C = 14 \text{ mA}$ and $V_{CE} = 3 \text{ V}$.
(b) Determine β_{dc} at $I_C = 1 \text{ mA}$ and $V_{CE} = 8 \text{ V}$.
(c) Determine β_{ac} at $I_C = 14 \text{ mA}$ and $V_{CE} = 3 \text{ V}$.
(d) Determine β_{dc} at $I_C = 1 \text{ mA}$ and $V_{CE} = 8 \text{ V}$.
(e) How does the level of β_{ac} and β_{dc} compare in each region?
(f) Is the approximation $\beta_{dc} \approx \beta_{ac}$ a valid one for this set of characteristics?

* Please note: Asterisks indicate more difficult problems.

which states in the fixed bias circuit with the double-subscript notation

$$V_{CE} = V_C - V_E$$

where V_{CE} is the voltage from collector to emitter and V_C and V_E are the collector and emitter to ground respectively. But in this case since $V_E = 0$

$$V_{CE} = V_C$$

In addition, since

$$V_{BE} = V_B - V_E$$

and $V_E = 0$ V, then

$$V_{BE} = V_B$$

Keep in mind that voltage levels such as V_{CE} are determined by placing the (positive) lead of the voltmeter at the collector terminal with the black (negative) lead at the emitter terminal as shown in Fig. 4.6. V_C is the voltage from collector to ground and is measured as shown in the same figure. In this case the two readings are identical, but in the networks to follow the two can be quite different. Clearly understanding the difference between the two measurements can prove to be quite important in the troubleshooting of transistor networks.

Figure 4.6 Measuring V_{CE} and V_C .

EXAMPLE 4.1

Determine the following for the fixed-bias configuration of Fig. 4.7.

- I_{B_0} and I_{C_0} .
- V_{CE_0} .
- V_B and V_C .
- V_{BC} .

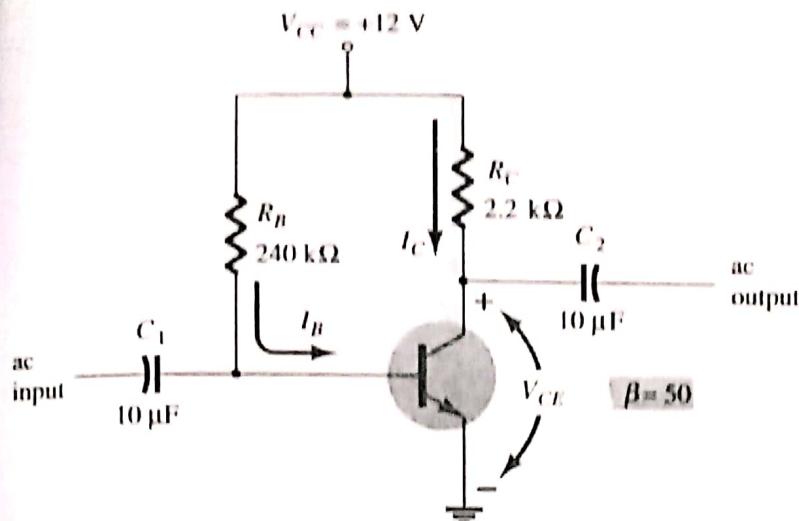


Figure 4.7 DC fixed-bias circuit for Example 4.1.

Solution

$$(a) \text{ Eq. (4.4): } I_{B_0} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega} = 47.08 \mu\text{A}$$

$$\text{Eq. (4.5): } I_{C_0} = \beta I_{B_0} = (50)(47.08 \mu\text{A}) = 2.35 \text{ mA}$$

$$(b) \text{ Eq. (4.6): } V_{CE_0} = V_{CC} - I_{C_0} R_C \\ = 12 \text{ V} - (2.35 \text{ mA})(2.2 \text{ k}\Omega) \\ = 6.83 \text{ V}$$

$$(c) V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{CE} = 6.83 \text{ V}$$

(d) Using double-subscript notation yields

$$V_{BC} = V_B - V_C = 0.7 \text{ V} - 6.83 \text{ V} \\ = -6.13 \text{ V}$$

with the negative sign revealing that the junction is reversed-biased, as it should be for linear amplification.

Transistor Saturation

The term *saturation* is applied to any system where levels have reached their maximum values. A saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the saturation region the current is a maximum value *for the particular design*. Change the design and the corresponding saturation level may rise or drop. Of course, the highest saturation level is defined by the maximum collector current as provided by the specification sheet.

Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted. An operating point in the saturation region is depicted in Fig. 4.8a. Note that it is in a region where the characteristic curves join and the collector-to-emitter voltage is at or below

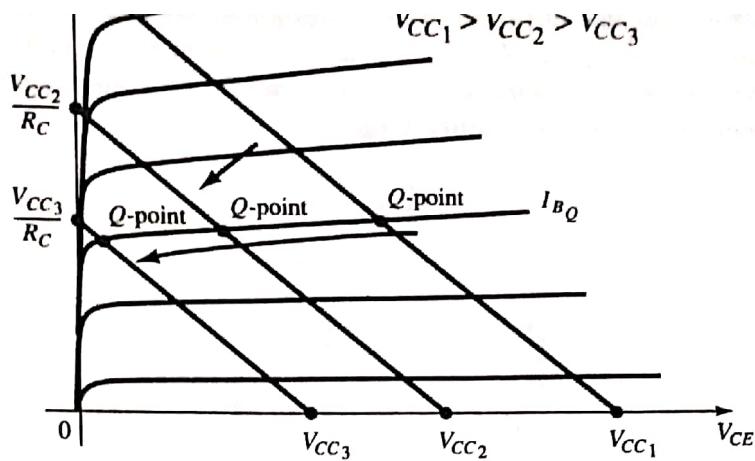


Figure 4.15 Effect of lower values of V_{CC} on the load line and Q -point.

Given the load line of Fig. 4.16 and the defined Q -point, determine the required values of V_{CC} , R_C , and R_B for a fixed-bias configuration.

EXAMPLE 4.3

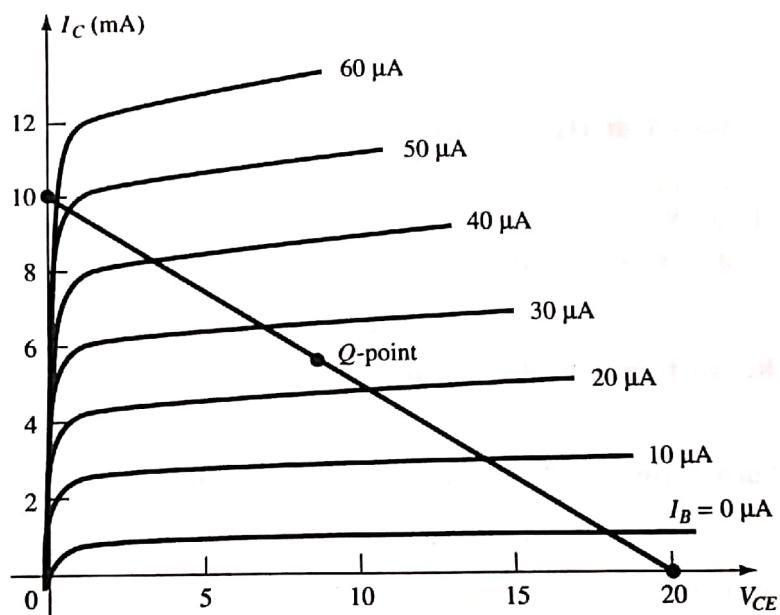


Figure 4.16 Example 4.3

Solution

From Fig. 4.16,

$$V_{CE} = V_{CC} = 20 \text{ V at } I_C = 0 \text{ mA}$$

$$I_C = \frac{V_{CC}}{R_C} \text{ at } V_{CE} = 0 \text{ V}$$

and

$$R_C = \frac{V_{CC}}{I_C} = \frac{20 \text{ V}}{10 \text{ mA}} = 2 \text{ k}\Omega$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

and

$$R_B = \frac{V_{CC} - V_{BE}}{I_B} = \frac{20 \text{ V} - 0.7 \text{ V}}{25 \mu\text{A}} = 772 \text{ k}\Omega$$

4.3 Fixed-Bias Circuit

EXAMPLE 4.4

For the emitter bias network of Fig. 4.22, determine

- (a) I_B
- (b) I_C
- (c) V_{CE}
- (d) V_C
- (e) V_E
- (f) V_B
- (g) V_{BC}

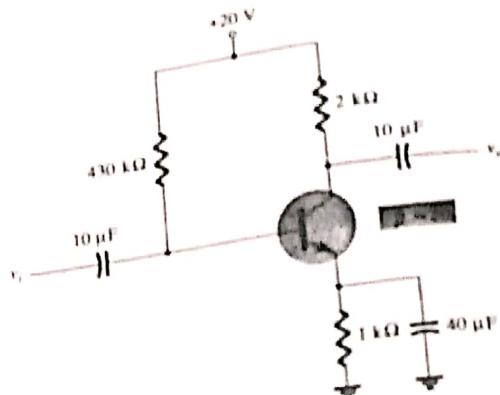


Figure 4.22 Emitter-stabilized bias circuit for Example 4.4

Solution

$$(a) \text{Eq. (4.17): } I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20 \text{ V} - 0.7 \text{ V}}{430 \text{ k}\Omega + (51)(1 \text{ k}\Omega)} \\ = \frac{19.3 \text{ V}}{481 \text{ k}\Omega} = 40.1 \mu\text{A}$$

$$(b) I_C = \beta I_B \\ = (50)(40.1 \mu\text{A}) \\ = 2.01 \text{ mA}$$

$$(c) \text{Eq. (4.19): } V_{CE} = V_{CC} - I_C(R_C + R_E) \\ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega + 1 \text{ k}\Omega) = 20 \text{ V} - 6.03 \text{ V} \\ = 13.97 \text{ V}$$

$$(d) V_C = V_{CC} - I_C R_C \\ = 20 \text{ V} - (2.01 \text{ mA})(2 \text{ k}\Omega) = 20 \text{ V} - 4.02 \text{ V} \\ = 15.98 \text{ V}$$

$$(e) V_E = V_C - V_{CE} \\ = 15.98 \text{ V} - 13.97 \text{ V} \\ = 2.01 \text{ V}$$

$$\text{or } V_E = I_E R_E \equiv I_C R_E \\ = (2.01 \text{ mA})(1 \text{ k}\Omega) \\ = 2.01 \text{ V}$$

$$(f) V_B = V_{BE} + V_E \\ = 0.7 \text{ V} + 2.01 \text{ V} \\ = 2.71 \text{ V}$$

$$(g) V_{BC} = V_B - V_C \\ = 2.71 \text{ V} - 15.98 \text{ V} \\ = -13.27 \text{ V} \quad (\text{reverse-biased as required})$$

Improved Bias Stability

The addition of the emitter stabilizer, that is, the dc bias voltage set by the circuit when one parameter changes. While a mathematical analysis of the improvement can

Prepare a table and compare the results calculated from Fig. 4.22 for the changes in I_C .

Solution

Using the results calculated yields the following:

The BJT collector current value of β . I_B is

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Saturation

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Improved Bias Stability

The addition of the emitter resistor to the dc bias of the BJT provides improved stability; that is, the dc bias currents and voltages remain closer to where they were set by the circuit when outside conditions, such as temperature, and transistor beta, change. While a mathematical analysis is provided in Section 4.12, some comparison of the improvement can be obtained as demonstrated by Example 4.5.

Prepare a table and compare the bias voltage and currents of the circuits of Figs. 4.7 and Fig. 4.22 for the given value of $\beta = 50$ and for a new value of $\beta = 100$. Compare the changes in I_C and V_{CE} for the same increase in β .

EXAMPLE 4.5

Solution

Using the results calculated in Example 4.1 and then repeating for a value of $\beta = 100$ yields the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	47.08	2.35	6.83
100	47.08	4.71	1.64

The BJT collector current is seen to change by 100% due to the 100% change in the value of β . I_B is the same and V_{CE} decreased by 76%.

Using the results calculated in Example 4.4 and then repeating for a value of $\beta = 100$, we have the following:

β	I_B (μA)	I_C (mA)	V_{CE} (V)
50	40.1	2.01	13.97
100	36.3	3.63	9.11

Now the BJT collector current increases by about 81% due to the 100% increase in β . Notice that I_B decreased, helping maintain the value of I_C —or at least reducing the overall change in I_C due to the change in β . The change in V_{CE} has dropped to about 35%. The network of Fig. 4.22 is therefore more stable than that of Fig. 4.7 for the same change in β .

Saturation Level

The collector saturation level or maximum collector current for an emitter-bias design can be determined using the same approach applied to the fixed-bias configuration: Apply a short circuit between the collector–emitter terminals as shown in Fig. 4.23 and calculate the resulting collector current. For Fig. 4.23:

$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C + R_E} \quad (4.25)$$

The addition of the emitter resistor reduces the collector saturation level below that obtained with a fixed-bias configuration using the same collector resistor.

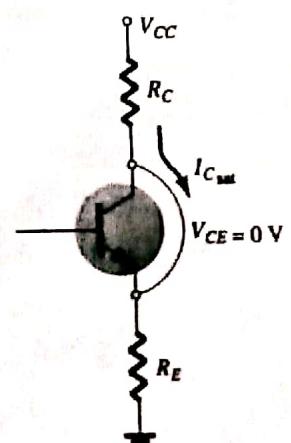


Figure 4.23 Determining $I_{C_{\text{sat}}}$ for the emitter-stabilized bias circuit.

IPLE 4.6

Determine the saturation current for the network of Example 4.4.

Solution

$$\begin{aligned}I_{C_{sat}} &= \frac{V_{CC}}{R_C + R_E} \\&= \frac{20 \text{ V}}{2 \text{ k}\Omega + 1 \text{ k}\Omega} = \frac{20 \text{ V}}{3 \text{ k}\Omega} \\&= 6.67 \text{ mA}\end{aligned}$$

which is about twice the level of I_{C_0} for Example 4.4.

Load-Line Analysis

The load-line analysis of the emitter-bias network is only slightly different from that encountered for the fixed-bias configuration. The level of I_B as determined by Eq. (4.17) defines the level of I_B on the characteristics of Fig. 4.24 (denoted I_{B_Q}).

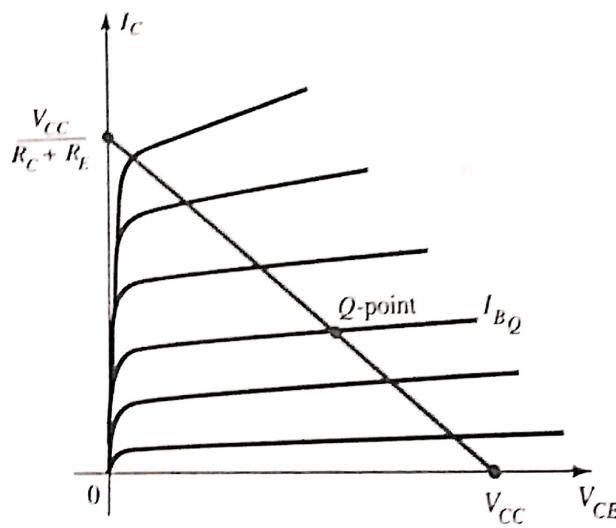


Figure 4.24 Load line for the emitter-bias configuration.

The collector-emitter loop equation that defines the load line is the following:

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

Choosing $I_C = 0 \text{ mA}$ gives

$$V_{CE} = V_{CC}|_{I_C=0 \text{ mA}} \quad (4.26)$$

R_{Th}: The voltage source is replaced by a short-circuit equivalent as shown in

$$R_{Th} = R_1 \parallel R_2$$

Fig. 4.28



Fig. 4.29 Determining R_{Th}

Thevenin voltage of Fig. 4.29 determined as follows:

Applying the voltage-divider rule:

$$E_{Th} = V_{R_2} = \frac{R_2 V_{CC}}{R_1 + R_2}$$

(4.29)

The Thevenin network is then redrawn as shown in Fig. 4.30 and I_B can be determined by first applying Kirchhoff's voltage law in the clockwise direction indicated

$$E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$$

Substituting $I_E = \beta + 1 I_B$ and solving for I_B yields

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \quad (4.30)$$

Although Eq. (4.30) initially appears different from those developed earlier, note that the numerator is again a difference of two voltage levels and the denominator is similar to Eq. (4.17).

Once I_B is known the remaining quantities of the network can be found in the same manner as developed for the emitter-bias configuration. That is,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (4.31)$$

which is exactly the same as Eq. (4.19). The remaining equations for V_E , V_C , and V_I are also the same as obtained for the emitter-bias configuration.

EXAMPLE 4.7

Determine the dc bias voltage V_{CE} and the current I_C for the voltage-divider configuration of Fig. 4.31.

Approximate Analysis

The input section of the voltage-divider configuration can be represented by the network of Fig. 4.32. The resistance R_i is the equivalent resistance between base and ground for the transistor with an emitter resistor R_F . Recall from Section 4.4 [Eq. (4.18)] that the reflected resistance between base and emitter is defined by $R_i = (\beta + 1)R_F$. If R_i is much larger than the resistance R_2 , the current I_B will be much smaller than I_2 (current always seeks the path of least resistance), and I_2 will be approximately equal to I_1 . If we accept the approximation that I_B is essentially zero amperes compared to I_1 or I_2 , then $I_1 = I_2$ and R_1 and R_2 can be considered series

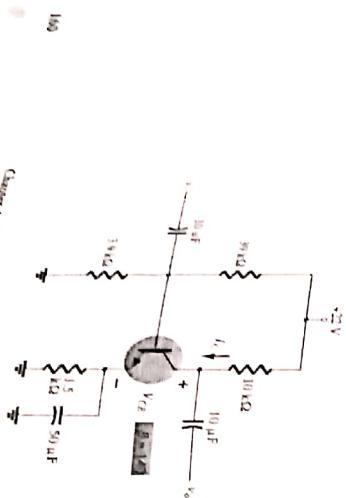


Figure 4.31 Beta-gated β circuit for Example 4.7.

Chapter 4 $| E_{Th} = V_{BE} - I_1 R_1$

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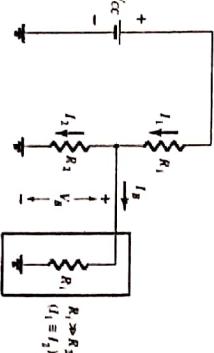


Figure 4.32 Approximate circuit for calculating the approximate base voltage V_i .

$$\begin{aligned} \text{Solution} \\ \text{Eq. (4.28): } R_{Th} &= R_1 \parallel R_2 \\ &= \frac{(39 \text{ k}\Omega)(3.9 \text{ k}\Omega)}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 3.55 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} \text{Eq. (4.29): } E_{Th} &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(3.9 \text{ k}\Omega)(22 \text{ V})}{39 \text{ k}\Omega + 3.9 \text{ k}\Omega} = 2 \text{ V} \\ \text{Eq. (4.30): } I_B &= \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1) R_E} \\ &= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (14)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 211.5 \text{ k}\Omega} \\ I_C &= \beta I_B \\ &= (140)(6.05 \mu\text{A}) \\ &= 0.85 \text{ mA} \end{aligned}$$

$$\begin{aligned} \text{Eq. (4.31): } V_{CE} &= V_{CC} - I_C(R_C + R_E) \\ &= 22 \text{ V} - (0.85 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega) \\ &= 22 \text{ V} - 9.78 \text{ V} \\ &= 12.22 \text{ V} \end{aligned}$$

elements. The voltage across R_2 , which is actually the base voltage, can be determined using the voltage-divider rule (hence the name for the configuration). That is,

$$V_B = \frac{R_2 V_{CC}}{R_1 + R_2} \quad (4.32)$$

Since $R = (\beta + 1)R_t \geq \beta R_t$ the condition that will define whether the approximate approach can be applied will be the following:

$$\beta R_t \geq 10R_2$$

In other words, if beta times the value of R_E is at least 10 times the value of R_2 , the approximate approach can be applied with a high degree of accuracy.

Once V_B is determined, the level of V_E can be calculated from

$$V_E = V_B - V_{BE}$$

and the emitter current can be determined from

$$I_E = \frac{V_E}{R_E} \quad (4.33)$$

and

$$I_{C_E} \equiv I_E \quad (4.36)$$

The collector-to-emitter voltage is determined by

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

but since $I_E \approx I_C$,

$$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad (4.37)$$

Note in the sequence of calculations from Eq. (4.33) through Eq. (4.37) that β does not appear and I_B was not calculated. The Q -point (as determined by I_{C_E}) is therefore independent of the value of beta.

EXAMPLE 4.8

Repeal the analysis of Fig 4.31 using the approximate technique and compare solutions for I_C and V_{CE} .

Solution

Repeat the exact analysis of Example 4.7 if β is reduced to 70 and compare solutions for I_{C_E} and V_{CE} . The results for I_{C_E} and V_{CE} are certainly close and considering the actual variation in parameter values one can certainly be considered as accurate as the other. The larger the level of R , compared to R_2 , the closer the approximate to the exact solution. Example 4.10 will compare solutions at a level well below the condition established by Eq. (4.33).

EXAMPLE 4.9

Repeal the analysis of Fig 4.31 using the approximate technique and compare solutions for I_C and V_{CE} .

Solution

This example is not a comparison of exact versus approximate methods but a testing of how much the Q -point will move if the level of β is cut in half. R_{Th} and E_{Th} are the same:

$$R_{Th} = 3.55 \text{ k}\Omega, \quad E_{Th} = 2 \text{ V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ k}\Omega + (70)(1.5 \text{ k}\Omega)} = \frac{1.3 \text{ V}}{3.55 \text{ k}\Omega + 105 \text{ k}\Omega}$$

$$= 11.81 \mu\text{A}$$

$$I_{C_E} = \frac{\beta I_B}{\beta + 1}$$

▲

$$= 0.83 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$= 22 \text{ V} - (0.83 \text{ mA})(10 \text{ k}\Omega + 1.5 \text{ k}\Omega)$$

$$= 12.46 \text{ V}$$

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Note that the level of V_E is the same as E_{Th} determined in Example 4.7. Essentially, therefore, the primary difference between the exact and approximate techniques is the effect of R_{Th} in the exact analysis that separates E_{Th} and V_B .

$$\text{Eq. (4.34): } V_E = V_B - V_{BE}$$

$$= 2 \text{ V} - 0.7 \text{ V}$$

$$= 1.3 \text{ V}$$

Eq. (4.34): $V_E = V_B - V_{BE}$

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Tabulating the results, we have:

	I_{C_E}	V_{C_E}
140	0.85 mA	12.22 V
70	0.83 mA	12.46 V

The results clearly show the relative insensitivity of the circuit to the change in β . Even though β is drastically cut in half, from 140 to 70, the levels of I_{C_E} and V_{C_E} are essentially the same.

EXAMPLE 4.10

Determine the levels of I_{C_E} and V_{C_E} for the voltage-divider configuration of Fig. 4.33 using the exact and approximate techniques and compare solutions. In this case the conditions of Eq. (4.33) will not be satisfied, but the results will reveal the difference in solution if the criterion of Eq. (4.33) is ignored.

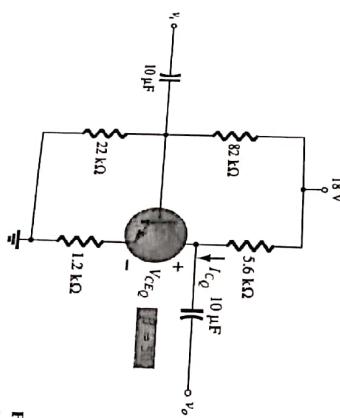


Figure 4.33 Voltage-divider configuration for Example 4.10

Solution

Exact Analysis:

$$\text{Eq. (4.33): } \beta R_i \geq 10R_2$$

$$(50)(1.2\text{k}\Omega) \geq 10(22\text{k}\Omega)$$

$$60\text{k}\Omega \not\geq 220\text{k}\Omega \text{ (not satisfied)}$$

$$E_{Th} = \frac{R_2 V_{CC}}{R_1 + R_2} = \frac{22\text{k}\Omega(18\text{V})}{82\text{k}\Omega + 22\text{k}\Omega} = 3.81\text{V}$$

$$I_B = \frac{E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E} = \frac{3.81\text{V} - 0.7\text{V}}{17.35\text{k}\Omega + (5)(1.2\text{k}\Omega)} = \frac{3.11\text{V}}{78.55\text{k}\Omega}$$

$$\begin{aligned} I_{C_E} &= \beta I_B = (50)(39.6\mu\text{A}) = 1.98\text{mA} \\ &= 18\text{V} - I_C(R_C + R_E) \\ &= 18\text{V} - (1.98\text{mA})(5.6\text{k}\Omega + 1.2\text{k}\Omega) \end{aligned}$$

Chapter 4 DC Biasing—BJTs

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Approximate Analysis:

$$V_B = E_{Th} = 3.81\text{V}$$

$$V_E = V_B - V_{BE} = 3.81\text{V} - 0.7\text{V} = 3.11\text{V}$$

$$I_{C_E} \equiv I_E = \frac{V_E}{R_E} = \frac{3.11\text{V}}{1.2\text{k}\Omega} = 2.59\text{mA}$$

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

$$\begin{aligned} &= 18\text{V} - (2.59\text{mA})(5.6\text{k}\Omega + 1.2\text{k}\Omega) \\ &= 3.88\text{V} \end{aligned}$$

Tabulating the results, we have:

	I_{C_E}	V_{C_E}
Exact	1.98 mA	4.54 V
Approximate	2.59 mA	3.88 V

The results reveal the difference between exact and approximate solutions. I_{C_E} is about 30% greater with the approximate solution, while V_{C_E} is about 10% less. The results are notably different in magnitude, but even though βR_E is only about three times larger than R_2 , the results are still relatively close to each other. For the future, however, our analysis will be dictated by Eq. (4.33) to ensure a close similarity between exact and approximate solutions.

Transistor Saturation

The output collector-emitter circuit for the voltage-divider configuration has the same appearance as the emitter-biased circuit analyzed in Section 4.4. The resulting equation for the saturation current (when V_{CE} is set to zero volts on the schematic) is therefore the same as obtained for the emitter-biased configuration. That is,

$$I_{C_{sat}} = I_{C_{max}} = \frac{V_{CC}}{R_C + R_E} \quad (4.38)$$

Load-Line Analysis

The similarities with the output circuit of the emitter-biased configuration result in the same intersections for the load line of the voltage-divider configuration. The load line will therefore have the same appearance as that of Fig. 4.24, with

$$I_C = \frac{V_{CC}}{R_C + R_E} \Big|_{V_{CE}=0\text{V}} \quad (4.39)$$

$$V_{CE} = V_{CC} \Big|_{I_C=0\text{mA}} \quad (4.40)$$

The level of I_B is of course determined by a different equation for the voltage-divider bias and the emitter-bias configurations.

(where $I'_C \approx I_C$,

and

which is exactly as obtained for the emitter-bias and voltage-divider bias configurations.

Determine the quiescent levels of I_{CQ} and V_{CEQ} for the network of Fig. 4.37.

Solution

$$\text{Eq. (4.41): } I_B = \frac{V_{CC} - V_{BE}}{R_E + \beta(R_C + R_F)}$$

$$(4.41) \quad = \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (90)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)}$$

to equations for the difference of available the collector and the back path results in like the reflection

$$= 3.69 \text{ V}$$

4.6 DC Bias with Voltage Feedback

Figure 4.36 Collector-emitter loop for the network of Fig. 4.34.

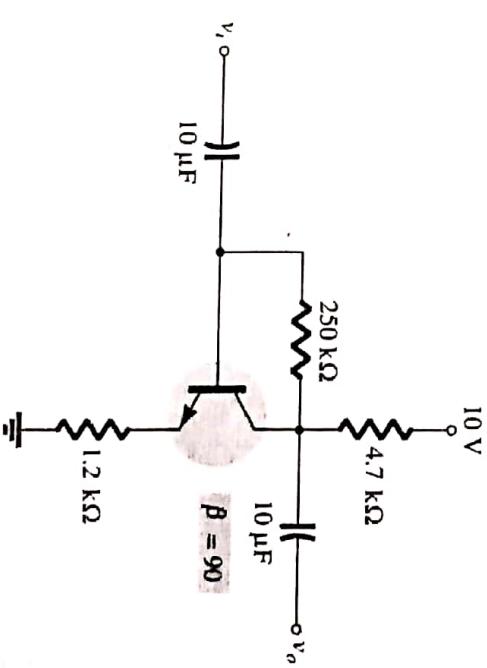


Figure 4.37 Network for Example 4.11.

EXAMPLE 4.12

Repeat Example 4.11 using a beta of 135 (50% more than Example 4.11).

Solution

It is important to note in the solution for I_a in Example 4.11 that the second term in the denominator of the equation is larger than the first. Recall in a recent discussion that the larger this second term is compared to the first, the less the sensitivity to changes in beta. In this example the level of beta is increased by 50%, which will increase the magnitude of this second term even more compared to the first. It is more important to note in these examples, however, that once the second term is relatively large compared to the first, the sensitivity to changes in beta is significantly less.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} = \frac{10 \text{ V} - 0.7 \text{ V}}{250 \text{ k}\Omega + (135)(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)}$$

$$= \frac{9.3 \text{ V}}{250 \text{ k}\Omega + 796.5 \text{ k}\Omega} = \frac{9.3 \text{ V}}{1046.5 \text{ k}\Omega}$$

$$= 8.89 \mu\text{A}$$

and

$$I_{C_v} = \beta I_B$$

$$= (135)(8.89 \mu\text{A})$$

$$= 1.2 \text{ mA}$$

with

$$V_{CE_v} = V_{CC} - I_{C_v}R_C + R_E$$

$$= 10 \text{ V} - (1.2 \text{ mA})(4.7 \text{ k}\Omega + 1.2 \text{ k}\Omega)$$

$$= 10 \text{ V} - 7.08 \text{ V}$$

$$= 2.92 \text{ V}$$

Even though the level of beta increased 50%, the level of I_{C_v} only increased 12.1% while the level of V_{CE_v} decreased about 20.9%. If the network were a fixed-bias design, a 50% increase in beta would have resulted in a 50% increase in I_{C_v} and a dramatic change in the location of the Q-point.

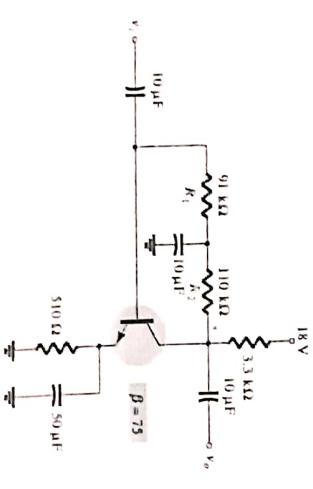
EXAMPLE 4.13 Determine the dc level of I_B and V_C for the network of Fig. 4.38.


Figure 4.38 Network for Example 4.13

Load-Line Analysis
Continuing with the approximation $I'_C = I_C$ the equation for the saturation current is the same as obtained for the voltage-divider and emitter-biased configurations. That is,

$$I_{C_s} = I_{C_{ss}} = \frac{V_{CC}}{R_C + R_E} \quad (4.43)$$

Saturation Conditions

Using the approximation $I'_C = I_C$ the equation for the saturation current is the same as obtained for the voltage-divider and emitter-biased configurations. That is,

4.7 MISCELLANEOUS BIAS CONFIGURATIONS

There are a number of BJT bias configurations that do not match the basic mold of those analyzed in the previous sections. In fact, there are variations in design that would require many more pages than is possible in a book of this type. However, the primary purpose here is to emphasize those characteristics of the device that permit a dc analysis of the configuration and to establish a general procedure toward the desired solution. For each configuration discussed thus far the first step has been the derivation of an expression for the base current. Once the base current is known, the collector current and voltage levels of the output circuit can be determined quite

Solution

In this case the base resistance for the dc analysis is composed of two resistors with a capacitor connected from their junction to ground. For the dc mode, the capacitor assumes the open-circuit equivalence and $R_B = R_1 + R_2$.

Solving for I_B gives

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

$$= \frac{18 \text{ V} - 0.7 \text{ V}}{(9) \text{ k}\Omega + 110 \text{ k}\Omega + (75)(3.3 \text{ k}\Omega + 0.51 \text{ k}\Omega)}$$

$$= \frac{17.3 \text{ V}}{201 \text{ k}\Omega + 285.75 \text{ k}\Omega} = \frac{17.3 \text{ V}}{486.75 \text{ k}\Omega}$$

$$= 35.5 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (75)(35.5 \mu\text{A})$$

$$= 2.66 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C \approx V_{CC} - I_C R_C$$

$$= 18 \text{ V} - (2.66 \text{ mA})(3.3 \text{ k}\Omega)$$

$$= 18 \text{ V} - 8.78 \text{ V}$$

$$= 9.22 \text{ V}$$

directly. This is not to imply that all solutions will take this path, but it does suggest a possible route to follow if a new configuration is encountered.

The first example is simply one where the emitter resistor has been dropped from the voltage-feedback configuration of Fig. 4.34. The analysis is quite similar but does require dropping R_E from the applied equation.

EXAMPLE 4.14

For the network of Fig. 4.39,

- Determine I_{C_E} and $V_{CE}^{(T)}$.
- Find V_B , V_C , V_E , and V_{BE} .

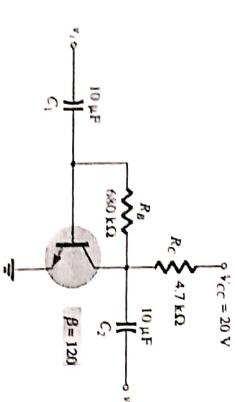


Figure 4.39 Collector feedback
with $R_E = 0 \Omega$

Solution

(a) The absence of R_E reduces the reflection of resistive levels to simply that of R_C and the equation for I_B reduces to

$$I_B = \frac{V_{CC} - V_{BE}}{R_b + \beta R_C}$$

$$= \frac{20 \text{ V} - 0.7 \text{ V}}{6.4 \text{ k}\Omega + (120)(4.7 \text{ k}\Omega)} = \frac{19.3 \text{ V}}{1.244 \text{ M}\Omega}$$

$$I_{C_E} = \beta I_B = (120)(15.51 \mu\text{A})$$

$$= 1.86 \text{ mA}$$

$$V_{CE}^{(T)} = V_{CC} - I_C R_C$$

$$= 20 \text{ V} - (1.86 \text{ mA})(4.7 \text{ k}\Omega)$$

$$= 11.26 \text{ V}$$

$$V_B = V_{BE} = 0.7 \text{ V}$$

$$V_C = V_{TR} = 11.26 \text{ V}$$

$$V_E = 6 \text{ V}$$

$$V_{BE} = V_B - V_E = 0.7 \text{ V} - 11.26 \text{ V}$$

$$= -10.56 \text{ V}$$

Determine V_C and V_B for the network of Fig. 4.40.

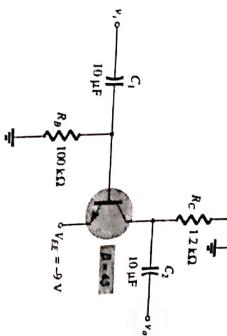


Figure 4.40 Example 4.15

Solution
Applying Kirchhoff's voltage law in the clockwise direction for the base-emitter loop will result in

$$-I_B R_B - V_{BE} + V_{EE} = 0$$

$$-I_B R_B - V_{BE} + 9 \text{ V} = 0$$

$$I_B = \frac{V_{EE} - V_{BE}}{R_B}$$

$$= \frac{9 \text{ V} - 0.7 \text{ V}}{100 \text{ k}\Omega}$$

$$= \frac{8.3 \text{ V}}{100 \text{ k}\Omega}$$

$$= 83 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (45)(83 \mu\text{A})$$

$$= 3.735 \text{ mA}$$

$$V_C = -I_C R_C$$

$$= -(3.735 \text{ mA})(1.2 \text{ k}\Omega)$$

$$= -4.48 \text{ V}$$

$$V_B = -I_B R_B$$

$$= -(83 \mu\text{A})(100 \text{ k}\Omega)$$

$$= -8.3 \text{ V}$$

EXAMPLE 4.15

For the network of Fig. 4.39,

- Determine I_{C_E} and $V_{CE}^{(T)}$.
- Find V_B , V_C , V_E , and V_{BE} .

In the next example the applied voltage is connected to the emitter leg, and R_E is connected directly to ground. Initially, it appears somewhat unusual and quite different from those encountered thus far, but one application of Kirchhoff's voltage law to this basic circuit will result in the desired base current.

The next example employs a network referred to as an *emitter-follower* configuration. When the same network is analyzed on an ac basis we will find that the output and input signals are in phase (one following the other) and the output voltage is slightly less than the applied signal. For the dc analysis the collector is grounded and the applied voltage is in the emitter leg.

EXAMPLE 4.16

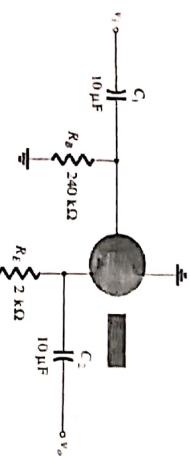
 Determine V_{CEQ} and I_E for the network of Fig. 4.41.


Figure 4.41 Common-emitter (emitter-follower) configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit will result in

$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

but

$$I_E = (\beta + 1)I_B$$

and

$$V_{EE} - V_{BE} - (\beta + 1)I_B R_E - I_B R_B = 0$$

with

$$I_B = \frac{V_{EE} - V_{BE}}{R_B + (\beta + 1)R_E}$$

Substituting values yields

$$I_B = \frac{20 \text{ V} - 0.7 \text{ V}}{240 \text{ k}\Omega + (91)(2 \text{ k}\Omega)}$$

$$= \frac{19.3 \text{ V}}{240 \text{ k}\Omega + 182 \text{ k}\Omega} = \frac{19.3 \text{ V}}{422 \text{ k}\Omega}$$

$$= 45.73 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (90)(45.73 \mu\text{A})$$

$$= 4.12 \text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit, we have

$$-V_{CE} + I_E R_E + V_{EE} = 0$$

but

$$I_E = (\beta + 1)I_B$$

and

$$V_{CEQ} = V_{EE} - (\beta + 1)I_B R_E$$

$$= 20 \text{ V} - (91)(45.73 \mu\text{A})(2 \text{ k}\Omega)$$

$$= 11.68 \text{ V}$$

$$I_E = 4.16 \text{ mA}$$

All of the examples thus far have employed a common-emitter or common-collector configuration. In the next example we investigate the common-base configuration. The collector current is then available to perform an analysis of the output circuit.

Determine the voltage V_{CB} and the current I_B for the common-base configuration of Fig. 4.42.

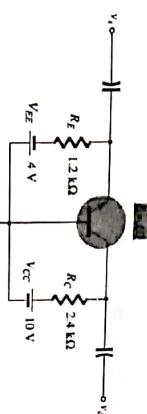
EXAMPLE 4.17


Figure 4.42 Common-base configuration.

Solution

Applying Kirchhoff's voltage law to the input circuit yields

$$I_E = \frac{V_{EE} - V_{BE}}{R_E}$$

and

Substituting values, we obtain

$$I_E = \frac{4 \text{ V} - 0.7 \text{ V}}{1.2 \text{ k}\Omega} = 2.75 \text{ mA}$$

Applying Kirchhoff's voltage law to the output circuit gives

$$-V_{CB} + I_E R_C - V_{CE} = 0$$

and

$$V_{CB} = V_{CC} - I_E R_C \text{ with } I_C \approx I_E$$

$$= 10 \text{ V} - (2.75 \text{ mA})(2.4 \text{ k}\Omega)$$

$$= 3.4 \text{ V}$$

$$I_B = \frac{I_C}{\beta}$$

$$= \frac{2.75 \text{ mA}}{60}$$

$$= 45.8 \mu\text{A}$$

Example 4.18 employs a split supply and will require the application of Thevenin's theorem to determine the desired unknowns.

4.7 Miscellaneous Bias Configurations

EXAMPLE 4.18

Determine V_C and V_H for the network of Fig. 4.43.

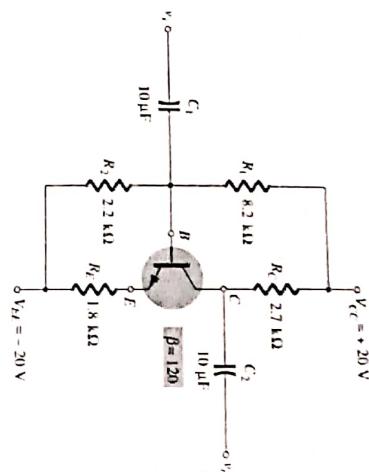


Figure 4.43 Example 4.18

Solution

The Thevenin resistance and voltage are determined for the network to the left of the base terminal as shown in Figs. 4.44 and 4.45.

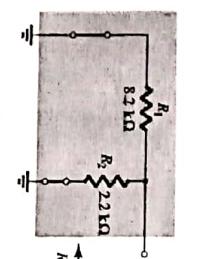


Figure 4.44 Determining R_{Th}

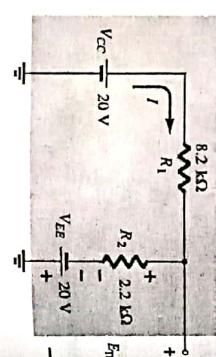


Figure 4.45 Determining E_{Th}

R_{Th} :

$$R_{Th} = 8.2 \text{ k}\Omega \parallel 2.2 \text{ k}\Omega = 1.73 \text{ k}\Omega$$

E_{Th} :

$$I = \frac{V_{CC} + V_{EE}}{R_1 + R_2} = \frac{20 \text{ V} + 20 \text{ V}}{8.2 \text{ k}\Omega + 2.2 \text{ k}\Omega} = \frac{40 \text{ V}}{10.4 \text{ k}\Omega}$$

$$= 3.85 \text{ mA}$$

$$E_{Th} = IR_2 - V_{EE}$$

$$= (3.85 \text{ mA})(2.2 \text{ k}\Omega) - 20 \text{ V}$$

$$= -11.53 \text{ V}$$

The network can then be redrawn as shown in Fig. 4.46, where the application of Kirchhoff's voltage law will result in

$$-E_{Th} - I_B R_{Th} - V_{BE} - I_E R_E + V_{EE} = 0$$

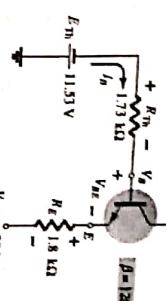


Figure 4.46 Substituting the Thevenin equivalent circuit.

Substituting $I_E = (\beta + 1)V_B$ gives

$$V_{EE} - E_{Th} - V_{BE} - (\beta + 1)V_B R_E - I_B R_{Th} = 0$$

$$I_B = \frac{V_{EE} - E_{Th} - V_{BE}}{R_{Th} + (\beta + 1)R_E}$$

$$= \frac{20 \text{ V} - 11.53 \text{ V} - 0.7 \text{ V}}{1.73 \text{ k}\Omega + (120)(1.8 \text{ k}\Omega)}$$

$$= \frac{7.77 \text{ V}}{219.53 \text{ k}\Omega}$$

$$= 35.39 \mu\text{A}$$

$$I_C = \beta I_B$$

$$= (120)(35.39 \mu\text{A})$$

$$= 4.25 \text{ mA}$$

$$V_C = V_{CC} - I_C R_C$$

$$= 20 \text{ V} - (4.25 \text{ mA})(2.7 \text{ k}\Omega)$$

$$= 8.53 \text{ V}$$

$$V_B = -E_{Th} - I_B R_{Th}$$

$$= -(11.53 \text{ V}) - (35.39 \mu\text{A})(1.73 \text{ k}\Omega)$$

$$= -11.59 \text{ V}$$

4.8 DESIGN OPERATIONS

Discussions thus far have focused on the analysis of existing networks. All the elements are in place and it is simply a matter of solving for the current and voltage levels of the configuration. The design process is one where a current and/or voltage may be specified and the elements required to establish the designated levels must be determined. This synthesis process requires a clear understanding of the characteristics of the device, the basic equations for the network, and a firm understanding of the basic laws of circuit analysis, such as Ohm's law, Kirchhoff's voltage law, and so on. In most situations the thinking process is challenged to a higher degree in the design process than in the analysis sequence. The path toward a solution is less defined and in fact may require a number of basic assumptions that do not have to be made when simply analyzing a network.

The design sequence is obviously sensitive to the components that are already specified and the components to be determined. If the transistor and supplies are specified, the design process will simply determine the required resistors for a particular design. Once the operational values of the resistors are determined, the nearest standard commercial values are normally chosen and any variations due to not using the exact resistance values are accepted as part of the design. This is certainly a valid approximation considering the tolerances normally associated with resistive elements and the transistor parameters.

If resistor values are to be determined, one of the most powerful equations is simply Ohm's law in the following form:

$$R_{\text{load}} = \frac{V_R}{I_R} \quad (4.44)$$

In a particular design the voltage across a resistor can often be determined from specified levels. If additional specifications define the current level, Eq. (4.44) can then be used to calculate the required resistance level. The first few examples will demonstrate how particular elements can be determined from specified levels. A complete design procedure will then be introduced for two popular configurations.

EXAMPLE 4.19

Given the device characteristics of Fig. 4.47a, determine V_{CE} , R_S , and R_C for the fixed-bias configuration of Fig. 4.47b.

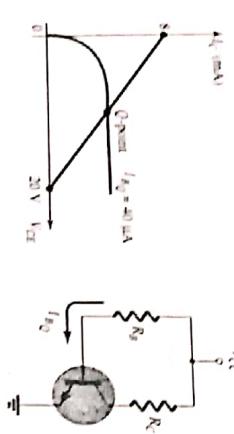


Figure 4.47 Example 4.19

Solution

$$V_{CE} = 20 \text{ V}$$

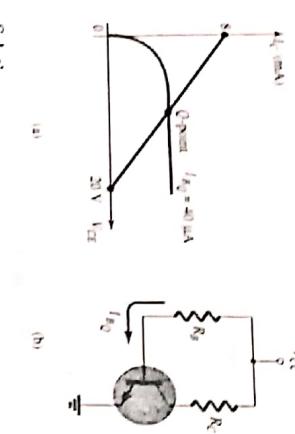


Figure 4.47 Example 4.19

Standard resistor values:
 $R_C = 2.4 \text{ k}\Omega$
 $R_S = 470 \text{ }\mu\Omega$

Using standard resistor values gives
 $I_B = 41.1 \mu\text{A}$

which is well within 5% of the value specified.

Given that $I_{C_E} = 2 \text{ mA}$ and $V_{CE_E} = 10 \text{ V}$, determine R_1 and R_C for the network of Fig. 4.48.

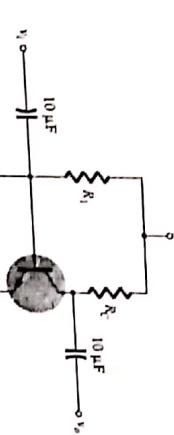


Figure 4.48 Example 4.20

Solution

$$V_E = I_E R_E \approx I_C R_E \\ = (2 \text{ mA})(1.2 \text{ k}\Omega) = 2.4 \text{ V}$$

$$V_B = V_{BE} + V_E = 0.7 \text{ V} + 2.4 \text{ V} = 3.1 \text{ V}$$

$$V_B = \frac{R_1 V_{CE}}{R_1 + R_2} = 3.1 \text{ V}$$

$$\frac{(18 \text{ k}\Omega)(18 \text{ V})}{18 \text{ k}\Omega + 18 \text{ k}\Omega} = 3.1 \text{ V}$$

$$3.1 R_1 = 3.1 R_2 + 55.8 \text{ k}\Omega$$

$$3.1 R_1 = 268.2 \text{ k}\Omega$$

$$R_1 = \frac{268.2 \text{ k}\Omega}{3.1} = 86.52 \text{ k}\Omega$$

$$\text{Eq. (4.44): } R_C = \frac{V_{CE}}{I_C} = \frac{V_{CE} - V_C}{I_C}$$

$$V_C = V_{CE} + V_E = 10 \text{ V} + 2.4 \text{ V} = 12.4 \text{ V}$$

with
 $R_C = \frac{18 \text{ V} - 12.4 \text{ V}}{2 \text{ mA}}$
and
 $= 2.8 \text{ k}\Omega$

with

$$R_E = \frac{V_{CE} - V_{BE}}{I_E} \\ = \frac{20 \text{ V} - 0.7 \text{ V}}{40 \mu\text{A}} = \frac{19.3 \text{ V}}{40 \mu\text{A}} \\ = 482.5 \text{ k}\Omega$$

The nearest standard commercial values to R_1 are 82 kΩ and 91 kΩ. However, using the series combination of standard values of 82 kΩ and 47 kΩ = 86.7 kΩ would result in a value very close to the design level.

EXAMPLE 4.20

EXAMPLE 4.21

The emitter-bias configuration of Fig. 4.49 has the following specifications: $I_{C_\alpha} = I_{C_\omega} = 8 \text{ mA}$, $V_C = 18 \text{ V}$, and $\beta = 110$. Determine R_C , R_E , and R_B .

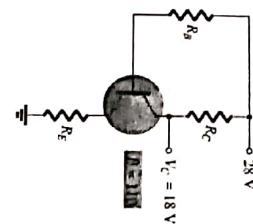


Figure 4.49 Example 4.21

Solution

$$I_{C_\alpha} = \frac{1}{2} I_{C_\omega} = 4 \text{ mA}$$

$$R_C = \frac{V_{CC} - V_C}{I_{C_\alpha}} = \frac{V_{CC} - V_C}{I_{C_\omega}} = \frac{28 \text{ V} - 18 \text{ V}}{4 \text{ mA}} = 2.5 \text{ k}\Omega$$

$$I_{C_\omega} = \frac{V_{CC}}{R_C + R_E}$$

$$R_C + R_E = \frac{V_{CC}}{I_{C_\omega}} = \frac{28 \text{ V}}{8 \text{ mA}} = 3.5 \text{ k}\Omega$$

$$R_E = \frac{V_{CC}}{I_{C_\omega}} - R_C = 3.5 \text{ k}\Omega - 2.5 \text{ k}\Omega = 1 \text{ k}\Omega$$

$$I_{B_\alpha} = \frac{I_{C_\alpha}}{\beta} = \frac{4 \text{ mA}}{110} = 36.36 \mu\text{A}$$

$$I_{B_\omega} = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$

$$R_B + (\beta + 1)R_E = \frac{V_{CC} - V_{BE}}{I_{B_\omega}}$$

and

with

$$R_B = \frac{V_{CC} - V_{BE}}{I_{B_\omega}} - (\beta + 1)R_E = \frac{28 \text{ V} - 0.7 \text{ V}}{36.36 \mu\text{A}} - (111)(1 \text{ k}\Omega)$$

$$= \frac{27.3 \text{ V}}{36.36 \mu\text{A}} - 111 \text{ k}\Omega = 639.8 \text{ k}\Omega$$

For standard values:

$$R_C = 2.4 \text{ k}\Omega$$

$$R_E = 1 \text{ k}\Omega$$

$$R_B = 620 \text{ k}\Omega$$

The discussion to follow will introduce one technique for designing an entire (spec) sheets provide information on a suggested operating point (or operating region) for a particular transistor. In addition, other system components connected to the common supply voltage, and so on, for the design.

In actual practice, many other factors may have to be considered and which may affect the selection of the desired operating point. For the moment we shall concentrate, however, on determining the component values to obtain a specified operating point. The discussion will be limited to the emitter-bias and voltage-divider bias configurations, although the same procedure can be applied to a variety of other transistor circuits.

Design of a Bias Circuit with an Emitter Feedback Resistor

Consider first the design of the dc bias components of an amplifier circuit having emitter-resistor bias stabilization as shown in Fig. 4.50. The supply voltage and operating point were selected from the manufacturer's information on the transistor used in the amplifier.

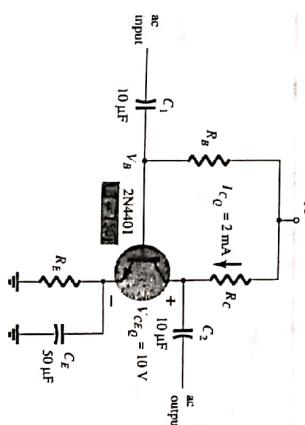


Figure 4.50 Emitter-subbiased bias circuit for design consideration

The selection of collector and emitter resistors cannot proceed directly from the information just specified. The equation that relates the voltages around the collector-emitter loop has two unknown quantities present—the resistors R_C and R_E . At this point some engineering judgment must be made, such as the level of the emitter voltage compared to the applied supply voltage. Recall that the need for including a resistor from emitter to ground was to provide a means of dc bias stabilization so that the change of collector current due to leakage currents in the transistor and the transistor beta would not cause a large shift in the operating point. The emitter resistor cannot be unreasonably large because the voltage across it limits the range of voltage swing of the voltage from collector to emitter (to be noted when the ac response is



Figure 4.54
Using
and the resulting
base
level of the following magnitude:

$$R_{load} = \frac{V_{CC}}{I_{CQ}} = \frac{5\text{ V}}{0\text{ mA}} = \infty \Omega$$

resulting in the open-circuit equivalence. For a typical value of $I_{CQ} = 10\text{ mA}$, the magnitude of the cutoff resistance is

$$R_{load} = \frac{V_{CC}}{I_{CQ}} = \frac{5\text{ V}}{10\text{ mA}} = 500 \text{ k}\Omega$$

which certainly approaches an open-circuit equivalence for many situations.

EXAMPLE 4.14

Determine R_B and R_C for the transistor inverter of Fig. 4.55 if $I_{CQ} = 10\text{ mA}$.

$$V_{CC} = 10\text{ V}$$

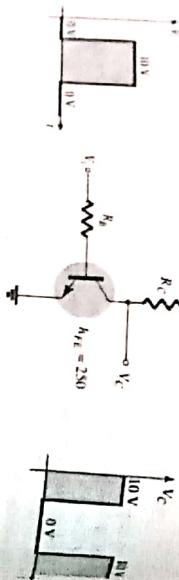


Figure 4.55 Inverter for Example 4.14

Solution

All saturation:

$$I_{CQ} = \frac{V_{CC}}{R_C}$$

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation:

$$I_B = \frac{I_{CQ}}{\beta_{dc}} = \frac{10\text{ mA}}{250} = 40\text{ }\mu\text{A}$$

Choosing $I_B = 60\text{ }\mu\text{A}$ to ensure saturation, and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

$$\text{we obtain } R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\text{ }\mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\text{ k}\Omega$ which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\text{ }\mu\text{A}$$

and

$$I_B = 62\text{ }\mu\text{A} > \frac{I_{CQ}}{\beta_{dc}} = 40\text{ }\mu\text{A}$$

Therefore, use $R_B = 150\text{ k}\Omega$ and $R_C = 1\text{ k}\Omega$.

There are transistors that are referred to as *switching transistors* due to the speed with which they can switch from one voltage level to the other. In Fig. 3.25, the periods of time defined as t_s , t_r , t_d , and t_f are provided versus collector current. Their impact on the speed of response of the collector output is defined by the collector current response of Fig. 4.56. The total time required for the transistor to switch from the "off" to the "on" state is designated as t_{on} and defined by

$$t_{on} = t_r + t_d \quad (4.47)$$

with t_d the delay time between the changing state of the input and the beginning of a response at the output. The time element t_r is the rise time from 10% to 90% of the final value.



Figure 4.56 Defining the time intervals of a pulse waveform

The total time required for a transistor to switch from the "on" to the "off" state is referred to as t_{off} and is defined by

$$t_{off} = t_f + t_d \quad (4.48)$$

where t_f is the storage time and t_d the fall time from 90% to 10% of the initial value.