

## Assignment No. 4

### \* Transistor Biasing :-

- i) Transistor biasing is the process of setting a transistor DC operating voltage or current condition to the correct level so that any AC input signal can be amplified correctly by the transistor.
- ii) The correct biasing of transistors can be achieved by using a process known as base bias.
- iii) Base bias network can be used for common-base, common-collector or common-emitter transistor configuration.

### \* Base Biasing of a common emitter configuration Amplifier :-

- i) For transistor, circuit is with the self bias of emitter base circuit where one or more biasing resistor used to get up the initial DC values of transistor currents  $I_B$ ,  $I_C$  and  $I_E$ .
- ii) The two most common form of transistor biasing are :-
  - a) Beta dependent
  - b) Beta independent

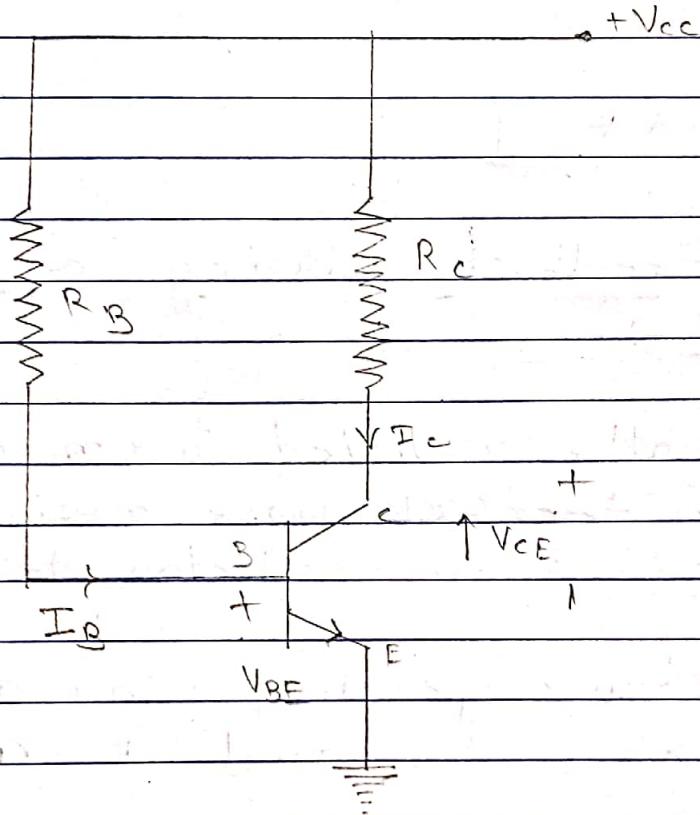
iii) Transistor bias voltages are largely dependent on transistor's Beta ( $\beta$ )

The following are examples of transistor base bias configuration from single supply ( $V_{cc}$ )

#### \* Fixed bias biasing transistor :-

- i) It is a type of bias where base current is maintained constant for given  $V_{cc}$  by using fixed resistor.
- ii) So operating point must remain fixed using this two resistor and fixed current initial operating point has to be found.
- iii) Disadvantage of this circuit is operating point changes with change in temperature (since collector current is varying with temperature).
- iv) Main Advantage of this circuit is simple to shift the operating point anywhere in active region by merely changing the base resistance.

Hence



$$\text{Here } V_{ce} = I_B R_B + V_{BE}$$

$$\therefore I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$\therefore \frac{dI_B}{dI_C} = 0$$

We know that,  
stability factor,

$$S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

$$\text{As } \frac{\delta I_B}{\delta I_C} = 0$$

$$\therefore [s = 1 + \beta]$$

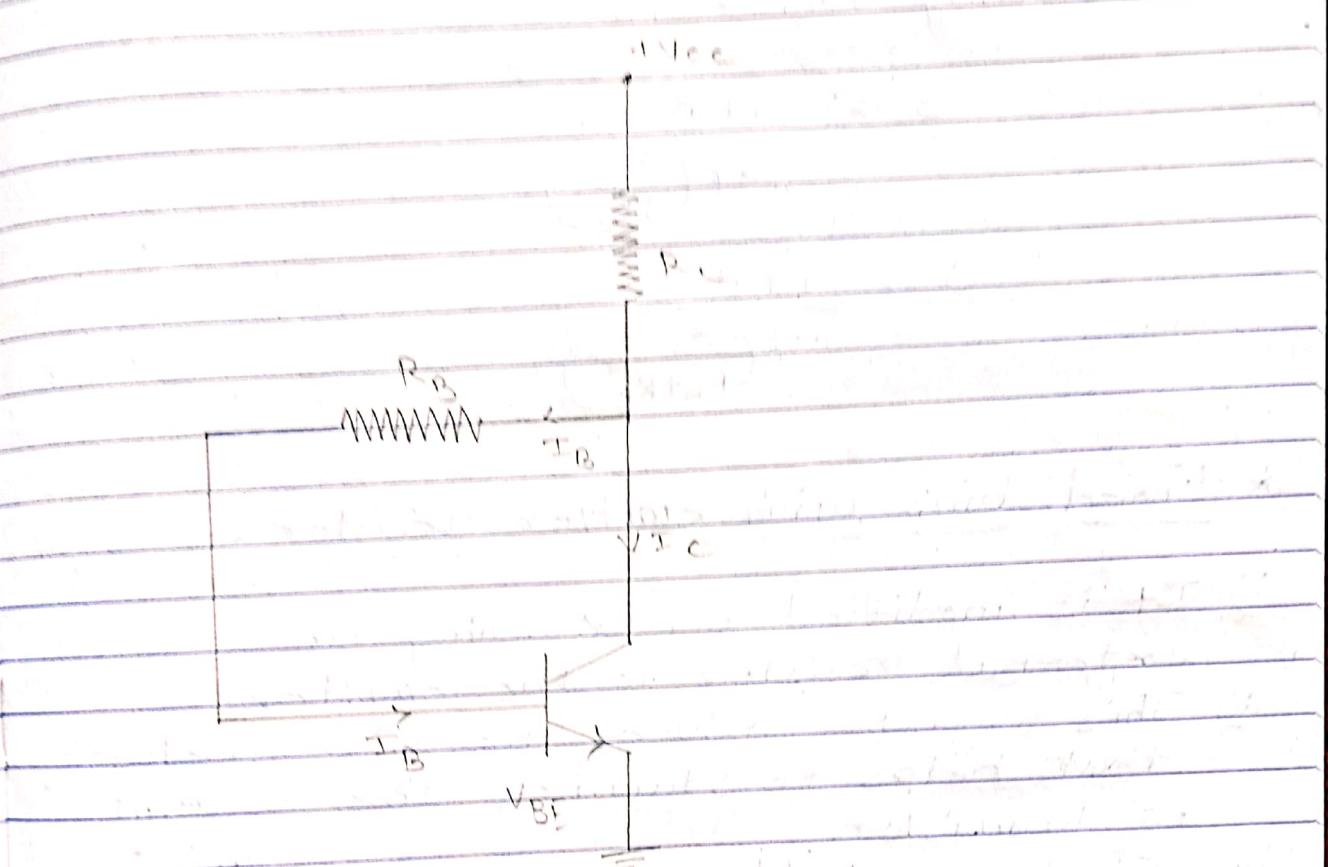
### \* Collector Feedback Biasing of transistor :-

- i) It is slightly modified form of Fixed bias. In feedback base resistor connection is from collector terminal of transistor.
- ii) It has stable operating point against temperature,  $V_{cc}$  and  $\beta$  (current gain).
- iii) This configuration employs negative feedback to prevent the thermal runaway and stabilize the operating point.
- iv) In this form of biasing, if any thermal runaway will induce a voltage drop across the  $R_C$  resistor that will throttle transistor base current.

Here,

$\therefore V_{cc}$

$\therefore I_B$



Here,

$$I_E = I_C + I_B \quad \text{--- (1)}$$

$$\therefore V_{cc} = R_c I_E + I_B R_B + V_{BE}$$

$$= R_c (I_C + I_B) + I_B R_B + V_{BE} \quad \text{--- (From (1))}$$

$$V_{cc} = R_c I_C + R_c I_B + I_B R_B + V_{BE}$$

$$\therefore I_B (R_c + R_B) = V_{cc} - V_{BE} - R_c I_C$$

$$\therefore \frac{\partial I_B}{\partial I_C} = -\frac{R_c}{R_c + R_B}$$

Stability factor is ,

$$S = \frac{1 + \beta}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

$$S = \frac{1 + \beta}{1 - \beta \left( \frac{R_C}{R_C + R_B} \right)}$$

\* Fixed bias with emitter resistor :-

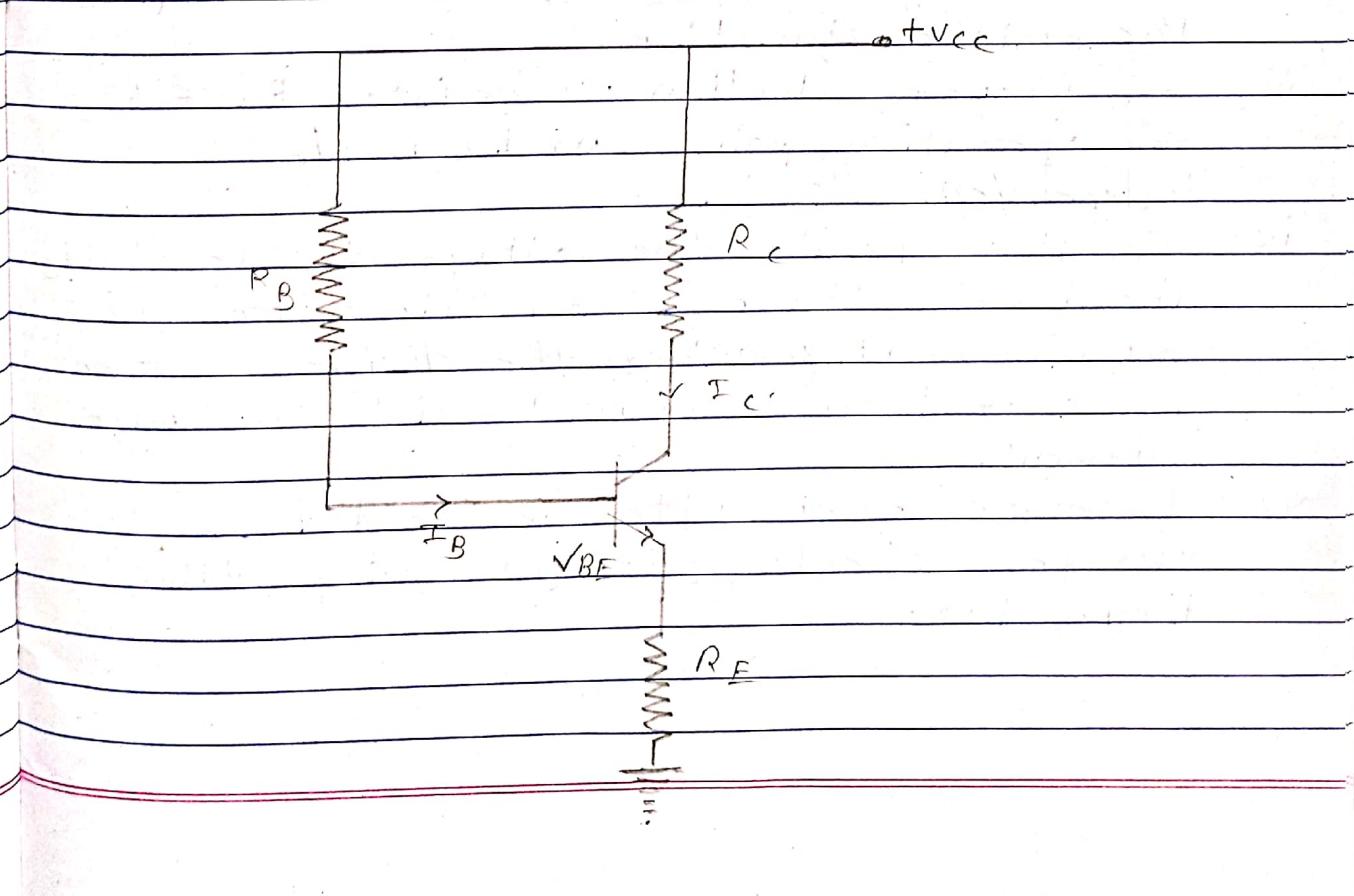
- i) It is modified by attaching an external resistor to the emitter.
- ii) This resistor induces negative feedback that helps to stabilize the Q-point of transistor.
- iii) If  $V_{BE}$  is held constant and temperature increases, emitter current increases.
- iv) However, a large  $I_E$  increases the emitter voltage  $V_E = I_E R_E$ , which in turn reduces the voltage  $V_B$  across the base resistor,
- v) A lower base current, which results in less current, because of  $I_C = \beta I_B$ .

Advantage :-

- i) The circuit has stabilizes the operating point against change in temperature and  $\beta$  value.

Disadvantage :-

- ii)  $R_E$  causes AC feedback which reduces the voltage gain of the amplifier.
- iii) If  $R_E$  is of large value, high  $V_{ce}$  is necessary. This increases cost as well as precautions are necessary while handling.



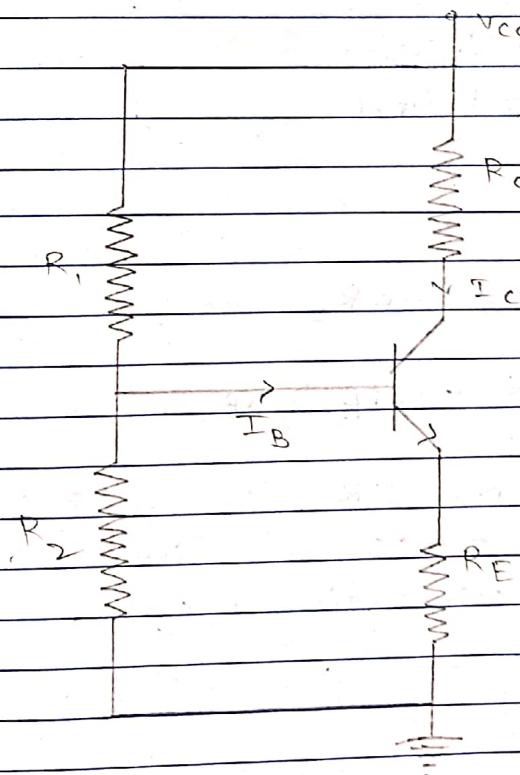
$$\text{stability factor} = \frac{1 + \beta}{1 - \beta \frac{\partial I_B}{\partial I_C}}$$

$$S = \frac{1 + \beta}{1 - \beta \frac{R_E}{R_B + R_E}}$$

\* Voltage divider biasing of emitter bias configuration :-

- i) The voltage divider is formed using external resistors  $R_1$  &  $R_2$ .
- ii) The voltage across  $R_2$  forward biases the emitter junction.
- iii) By proper selection of resistor  $R_1$  &  $R_2$  the operating point can be made independent of  $\beta$ .
- iv) In this circuit the voltage divider hold the base voltage fixed independent of base current provided the divider current is very large compared with the base current.
- v) However, even with the fixed base voltage, collector current varies with temperature.

- vi) So, an emitter resistor is added to stabilize the Q-point similar to above circuits with emitter resistor.
- vii) The voltage divider configuration achieves the current voltages by the use of resistors in certain patterns.



stability Factor is

$$S = \frac{1 + \beta}{1 - \beta \left( \frac{\partial I_B}{\partial I_C} \right)}$$

$$\therefore S = \frac{1 + \beta}{1 + \beta R_E / R_{TH} + R_E}$$

For given circuit

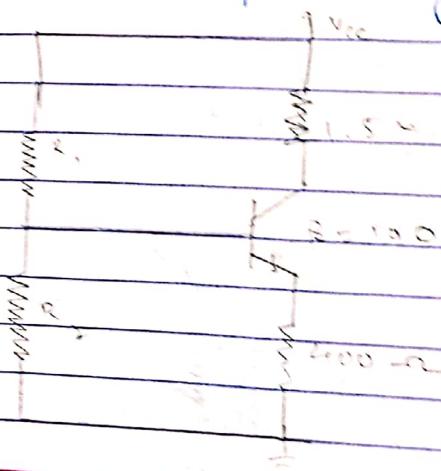
$$\therefore I_B = \frac{V_{TH} - V_{BE}}{(1 + \beta)R_E + R_{TH}}$$

$$I_c = \beta I_B$$

$$\therefore V_{CE} = V_{CC} - I_c R_C - I_E R_E$$

$$V_{CE} = V_{CC} - I_c R_C - (1 + \beta) I_B R_E$$

Q.1] If  $R_1 = 30k$ ,  $R_2 = 5k$ ,  $V_{CC} = 18V$ ,  
 $R_C = 1.5k$ ,  $R_E = 400\Omega$ . Find stability  
 Factor and operating point.



$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

$$= \frac{30 \times 5}{35}$$

$$R_{TH} = 4.28 \text{ k}\Omega$$

$$V_{TH} = \frac{18 \times 5}{35}$$

$$= \frac{18}{7}$$

$$V_{TH} = 2.57 \text{ V}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

$$= \frac{2.57 - 0.7}{4.58 \times 10^3 + 101 \times 400}$$

$$I_B = 42 \text{ nA}$$

$$I_C = \beta I_B = 4.2 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C R_C - (1+\beta) I_B R_E$$

$$= 12 - 4.2 \times 10^{-3} \times 15 \times 10^{-3} - 101 \times 42 \times 10^{-6} \times 400$$

$$V_{CE} = 10.0032 \text{ V}$$

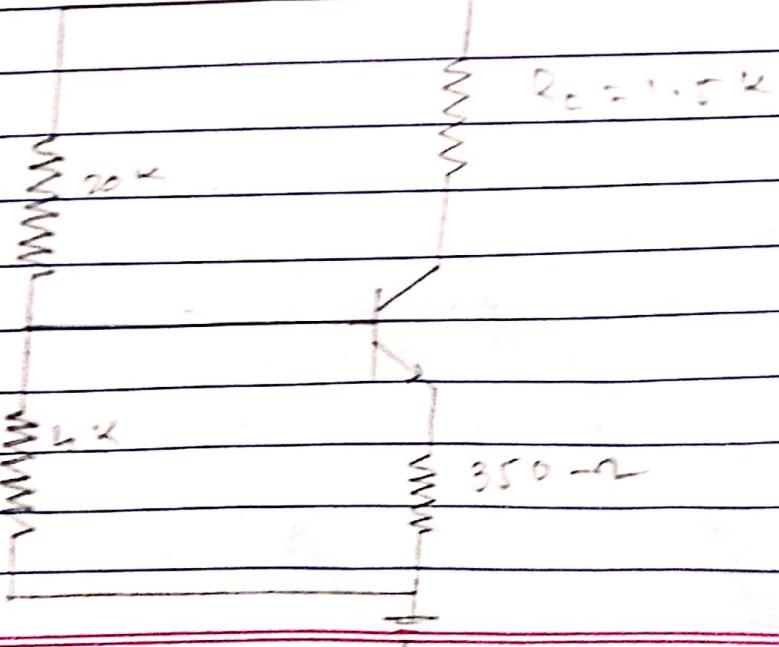
$$\text{Now } s = \frac{1 + \beta}{1 + \beta \frac{R_E}{R_{TH} + R_E}}$$

$$= \frac{101}{1 + \frac{100 \times 400}{2570 + 400}}$$

$$= \frac{101}{9.5365}$$

$$| s = 10.59077 |$$

Q.2] If  $R_1 = 20\text{k}$  and  $R_2 = 4\text{k}$ ,  $R_E = 1.5\text{k}$   
 $R_{TH} = 330\text{-}\Omega$ ,  $\beta = 100$  &  $V_{CC} = 15\text{V}$ .  
 Find stability Factor and operating point.



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$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{20 \times 4}{24} = 3.334 \Omega$$

$$V_{TH} = \frac{15 \times 4}{24}$$

$$V_{TH} = 2.5 \text{ V}$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E}$$

## \* Operational Amplifier (Op-Amp) :-

- An operational amplifier is basically a high gain, direct couple amplifier. It has two inputs and one output.
- Generally, it is operated in single ended input - single ended output mode. The differential amplifier forms the 1st stage of an op-amp.
- Op-amp can perform several arithmetic operations like addition, subtraction, differentiation, integration, comparison, analog to digital conversion, etc.

Inverting input

non-inverting input

Schematic symbol of op-amp.

iv) IC-741 is widely used as op-amp. In this

IC when input is zero, the output can be adjusted to zero by varying the  $10k\Omega$  potentiometer between offset null terminals.

## \* Characteristics of Ideal Op-amp :-

- open loop gain is infinite.
- IP impedance is infinite.
- OP impedance is zero.
- IP bias current is zero.
- IP offset current is zero.
- IP offset voltage is zero.
- Common mode rejection ratio is infinite.
- Frequency response curve extend from zero (dc) to infinite frequency.
- Response time is zero.

## \* Pin diagram of IC-741 :-

+ve

-ve

offset null  
not connected

+ve

Inverting IP

non-inverting IP

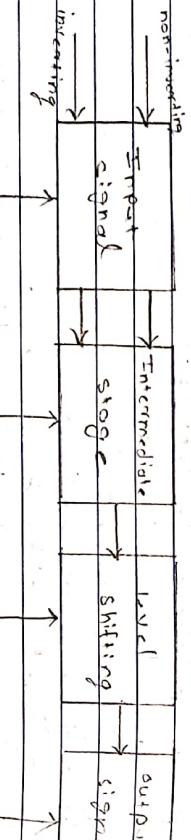
Output

-ve

offset null

PIN 8

\* Internal Block diagram of Op-amp :-



to bias the trans amplifiers stage.

Because direct coupling is used, the dc voltage level at o/p of intermediate stage is well above ground potential. Therefore level shifting circuit is used to shift dc level at o/p downwards to zero with respect to ground. The o/p stage is generally a push-pull complementary amplifier. The o/p stage increases the o/p voltage swing and raise the current supplying capability of op-amp. It also provides low o/p resistance.

Generally, because of slight mismatch of the two input transistor inverting IIP bias current ( $I_{B^-}$ ) is not equal to non-inverting IIP bias current ( $I_{B^+}$ ).  

$$\therefore I_E = |I_B^+ + I_B^-|$$

\* Parameters of op-amp :-

1) Input bias current ( $I_b$ ):-

In an ideal op-amp any current is not drawn from applied input signals. But practically it absorbs small value of DC to bias the transistor in the first differential

Generally, because of slight mismatch of the two input transistors inverting i/p bias current ( $I_{B^-}$ ) is not equal to non inverting  $I_{P}$  bias current ( $I_{B^+}$ ).

$$\therefore I_B = |I_{B^+}| + |I_{B^-}|$$

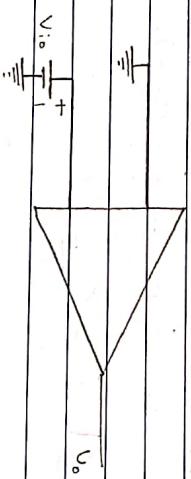
Input offset current :-  
The current gain of JFET transistor in op-amp  
are usually different. Therefore, their  
base current are never equal. The difference  
between the biasing current of inverting

and non-inverting inputs is called input offset current.

$$I_{os} = |I_E^+| - |I_E^-|$$

Typically  $I_{os}$  is less than 25% of input bias current and is a measure of mismatch of input transistors.

3) Input offset voltage :-  
When the inputs of an op-amp are grounded, the o/p must be zero. But there is a small error voltage of the o/p due to the difference in  $V_{BE}$  values of i/p transistors. This is called a i/p offset voltage.



The i/p offset voltage is equal to difference in  $V_{BE}$  values of input transistors.

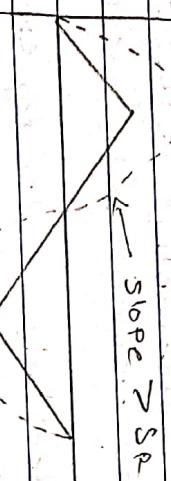
5) Slew rate (SR) :-

SR is most important specification affecting operation of op-amp. It limits the output voltage at higher frequency. SR is defined as maximum rate at which o/p can change.

$$SR = \frac{dV_{out}}{dt} = \frac{I_{max}}{C_C}$$

For IC 741 Slew rate is 0.5 V/μs.

Effect of SR limiting is observed with a sinusoidal signal also. If the slope of the sine wave is less than or equal to SR, there is no SR limiting. But when limiting slope of sine wave is greater than SR, SR distortion is observed.



$$A_{cl} = A_{ol} / (1 + A_{ol} \cdot \beta)$$

where,  $A_{ol}$  = open loop gain  
 $\beta$  = feedback fraction.

SR distortion.

6) open loop gain (A<sub>ol</sub>) :-

The gain of op-amp without negative feedback is called 'open loop gain',  $F_{ol}$ . It is  $7 \times 10^6$  in the midband, this gain is unstable.

$$\text{open loop gain} = \frac{V_{out}}{V_{in}}$$

where,  $V_{in}$  is voltage applied between two input terminals

7) closed loop gain (A<sub>cl</sub>) :-

The closed loop gain of an ideal op-amp is infinite. For use in practical circuit the gain should be limited and stabilized by the negative feedback is used for this purpose. A feedback resistor is connected between output terminals and inverting input terminals of op-amp.

The gain of op-amp with feedback is called 'closed loop gain'.

8) frequency response :-

Frequency response curve shows the change in voltage gain frequency. The gain without feedback is open loop gain. The frequency at which gain is  $70.72 \text{ dB}$  of maximum gain is called 'cut-off' frequency. The open loop cut-off frequency is  $10 \text{ Hz}$  and gain is  $70.712$ .

the voltage gain rolls off at rate of 20dB per decades. The decrease in the gain is due to compensating capacitor. Gain-bandwidth product is called the product of gain and cut off frequency.

$$\text{product} = A_{OL} \times F_{OL} = A_{CL} \times F_{CL}$$

IC 741, gain-bandwidth product is 1 MHz

