Unit 4

Combinational Circuit design

Unit 4: Combinational circuit design

- Combinational circuit design,
- Analysis of CMOS Logic Gates: MOS Device Capacitance, Switching Characteristics,
- Rise Time, Fall Time, Propagation Delay,
- Power Dissipation in CMOS,
- Fan-in, Fan-out,
- Complex Logic Structures,
- static CMOS,
- Ratioed Logic circuits
- Complementary Static CMOS,
- Pseudo NMOS Logic,
- Dynamic CMOS Logic,
- CMOS Domino Logic,
- CMOS Pass Transistor Logic.

Introduction

- Digital logic is divided into
    - combinational and sequential circuits.
- Combinational circuits are those whose outputs depend only on present inputs, while sequential circuits have memory.

- Generally, building blocks for combinational circuits are *logic gates*,while building blocks for sequential circuits are *registers and latches*.

- *Static CMOS* gates uses NMOS and PMOS networks to drive 0 and 1 outputs, respectively.

- Majority of circuits use static CMOS because it is robust, fast,energy-efficient, and easy to design.

- But, certain circuits needs specific speed, power, or density restrictions that force another solution.
- Such alternative CMOS logic configurations are called *circuit families*.
- Most commonly used alternative circuit families:
    - ratioed circuits,
    - dynamic circuits, and
    - pass transistor circuits.

Capacitance Estimation

- Switching speed or dynamic response of MOS systems are strongly dependent on parasitic capacitance associated with MOS device and interconnection capacitance which are formed by metal, polysilicon, and diffusion wires in concert with transistor and conductor resistances.

- Total load capacitance on output of a CMOS gate is sum of

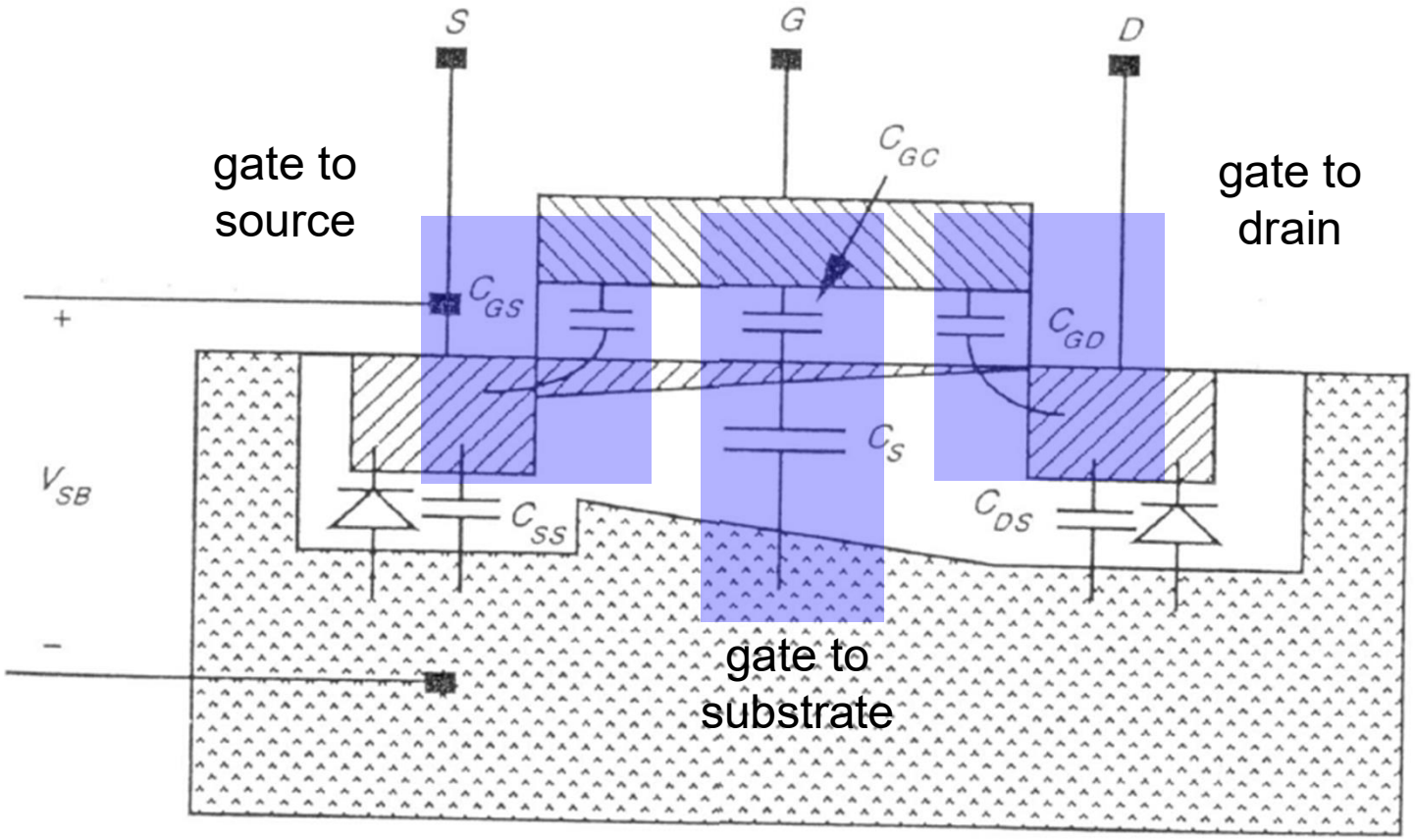
    - Gate capacitance
    - Diffusion capacitance
    - Routing capacitance

- To understand source of parasitic capacitance loads and their variations is necessary in design process of a system when performance in terms of speed is a part of design specifications.

- First understand characteristics of an MOS capacitor.

- Then will see MOS transistor gate capacitance, source or drain capacitance and routing capacitance.

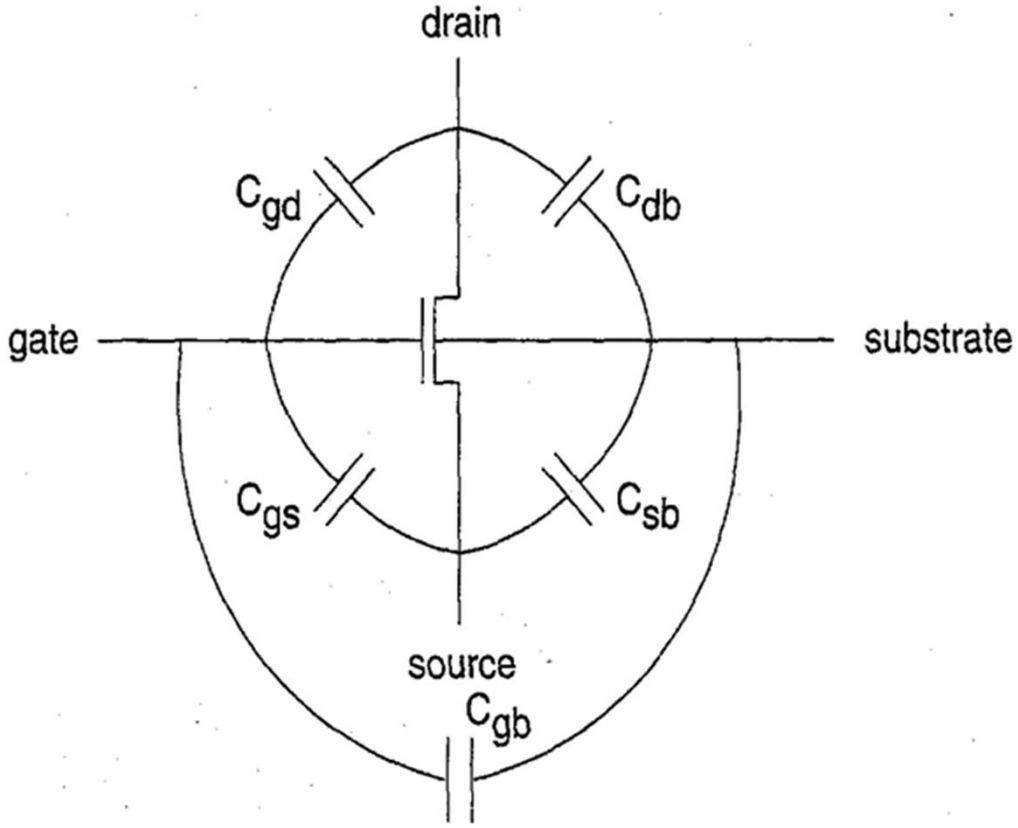
MOSFET Capacitance



- Any two conductors separated by an insulator have capacitance
- Gate to channel capacitor is very important
  - Creates channel charge necessary for operation
- Source and drain have capacitance to body
  - Across reverse-biased diodes
  - Called diffusion capacitance because it is associated with source/drain diffusion

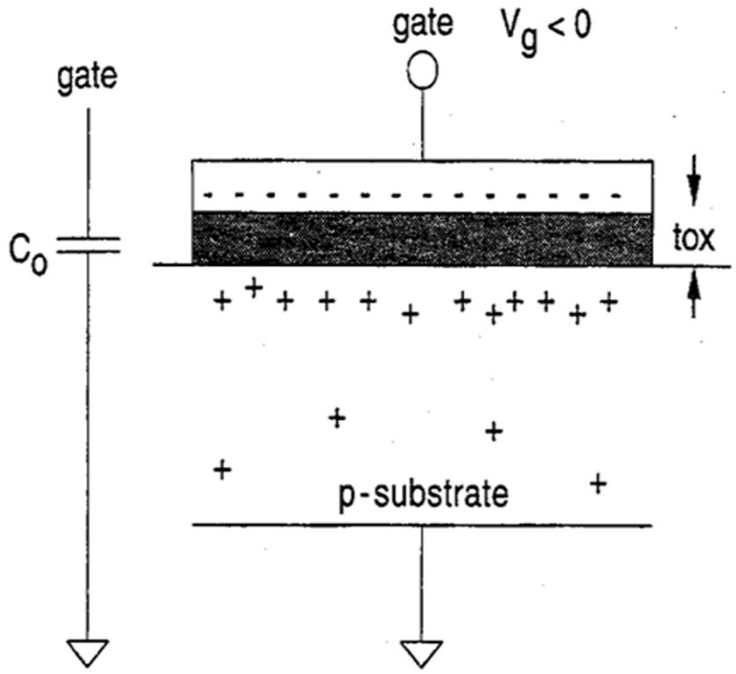
MOS Transistor Gate Capacitance Model

Gate capacitance has different components in different modes, but total remains constant.



- Figure shows diagrammatic representation of parasitic capacitance of an MOS transistor
- Where
    - Cgs is gate to source capacitance
    - Cgd is gate to drain capacitance
    - Csb is source to bulk or substrate diffusion capacitance
    - Cdb is drain to bulk or substrate diffusion capacitance
    - Cgb is gate to bulk capacitance
- Total gate capacitance Cg of MOS transistor is
- $Cg = Cgs + Cgb + Cgd$

- Behaviour of gate capacitance Cg of MOS transistor is explained in three regions of operation as

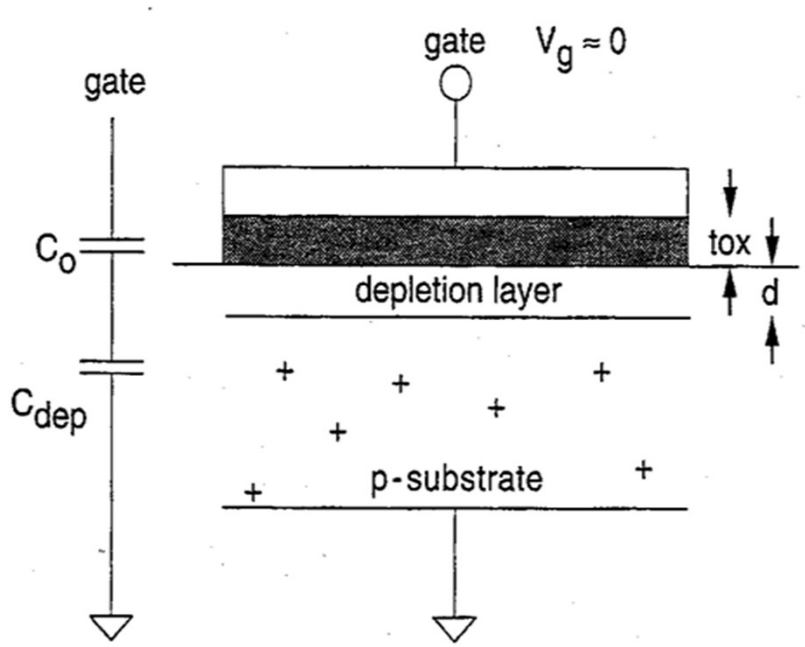


Accumulation occurs when Vg is negative (for P material). Holes are induced under the oxide.

$C_{gate} = C_{ox}A$ where

$$C_{ox} = (\varepsilon_{SiO2}\varepsilon_o/t_{ox})A$$

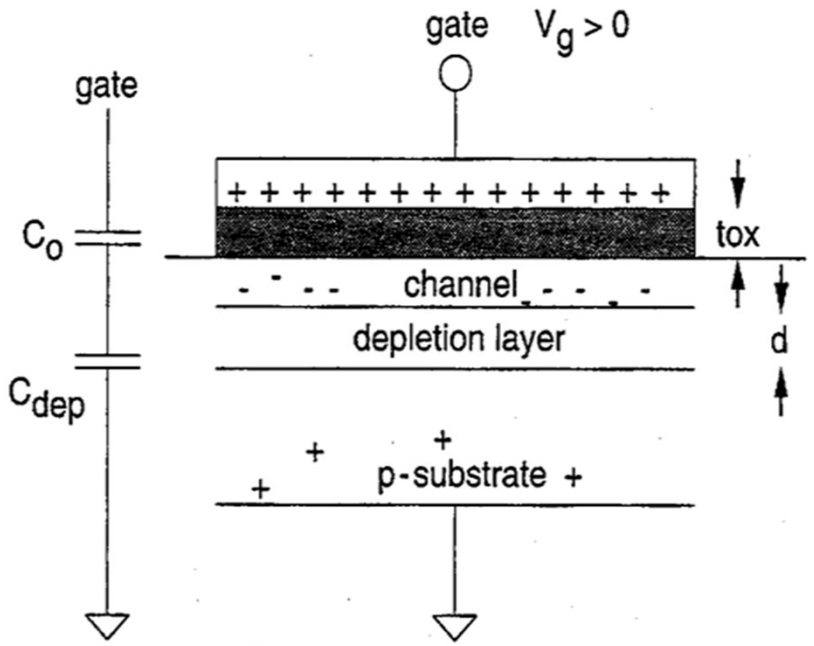
- Where A is area of gate
  - ε_{sio2} is dielectric constant or relative permittivity of SiO_2 (Value is 3.9)
  - ε_0 is permittivity of free space
  - t_{ox}- oxide layer thickness



Depletion occurs when Vg is near zero but < Vtn. Here the Cgate is given by CoxA in series with depletion layer capacitance

$$C_{dep}=(\varepsilon_o\varepsilon_{Si}/d)A$$

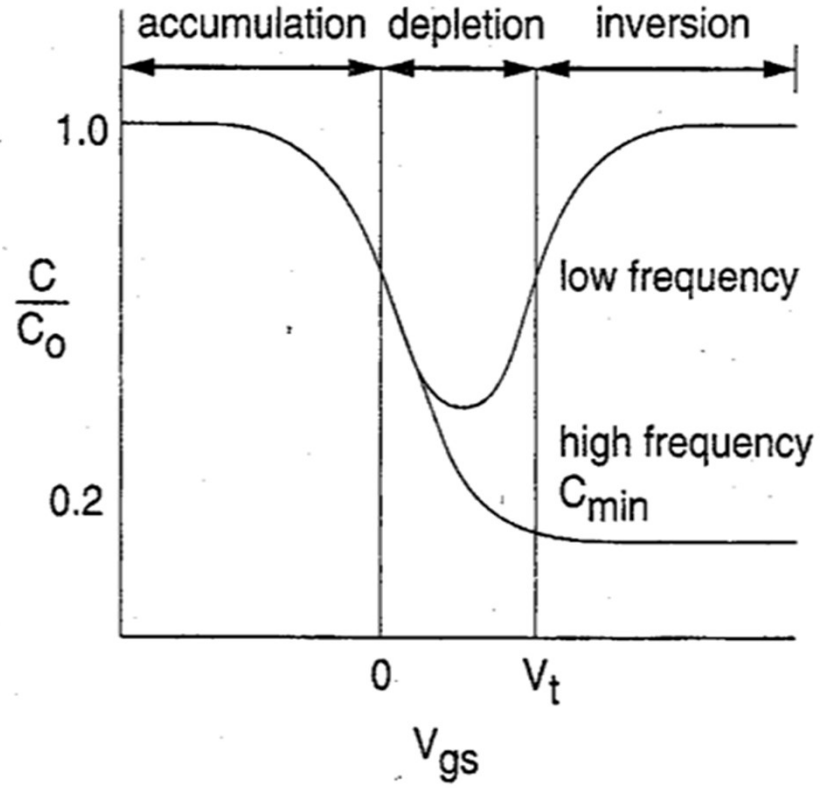
- Where A is area of gate
  - ε_{sio2} is dielectric constant of Si (Value is 12)
  - ε_0 is permittivity of free space
  - d is depletion layer depth



Inversion occurs when Vg is positive and > Vtn (for P material). A model for inversion in comprised of Cox A connecting from gate-to-channel and Cdep connecting from channel-to-substrate.

$$C_{gb}=C_0$$

$$=C_0*C_{dep}/C_0+C_{dep}$$



Normalized gate capacitance versus Gate voltage Vgs.

High freq behavior is due to the distributed resistance of channel

1. Cuf off region where Vgs < Vt.
When MOS device is OFF, no channel so Cgs = Cgd = 0 and
Cgb is modeled as a series combination of two capacitors .e. Co and Cdep.

2. Non-saturation or linear region, where Vgs – Vt > Vds.
Channel is formed so Cgs and Cgd (Gate to channel capacitances) will become significant.
They depend on gate voltage.
And values can be found as

$$C_{gd} = C_{gs} = \frac{1}{2} \quad (\varepsilon_{SiO2}\varepsilon_o/t_{ox})A$$

3. Saturation region, where Vgs – Vt < Vds.
Here Channel is heavily inverted. So drain region of channel is pitched off making Cgd = 0. and Cgs will be

$$C_{gs} = \frac{2}{3} \quad (\varepsilon_{SiO2}\varepsilon_o/t_{ox})A$$

Gate capacitance has different components in different modes, but total remains constant.

TABLE 4.3 Approximation of intrinsic MOS gate capacitance

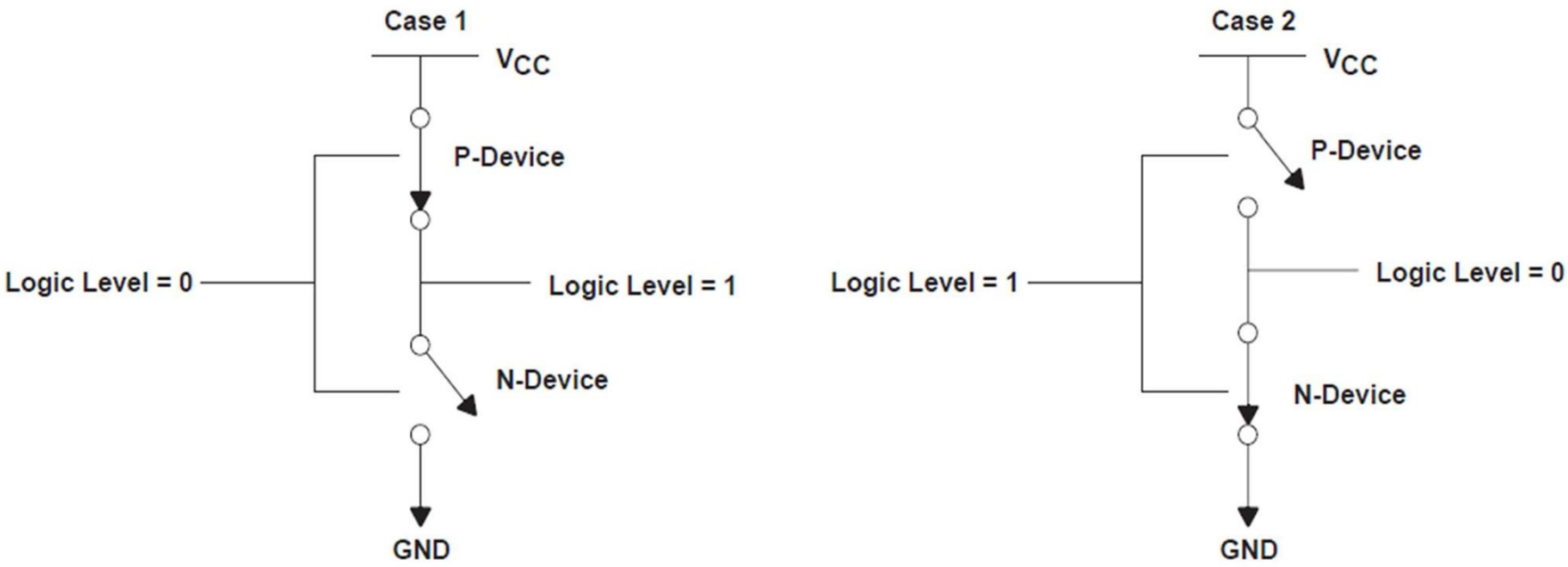
	CAPACITANCE		
Parameter	Off	Non-saturated	Saturated
C_{gb}	$\frac{\varepsilon A}{t_{ox}}$	0	0
C_{gs}	0	$\frac{\varepsilon A}{2t_{ox}}$	$\frac{2\varepsilon A}{3t_{ox}}$
C_{gd}	0	$\frac{\varepsilon A}{2t_{ox}}$	0 (finite for short channel devices)
$C_g = C_{gb} + C_{gs} + C_{gd}$	$\frac{\varepsilon A}{t_{ox}}$	$\frac{\varepsilon A}{t_{ox}}$	$\frac{2\varepsilon A}{3t_{ox}} \rightarrow \frac{.9\,\varepsilon A}{t_{ox}}$ (short channel)

Power Dissipation in CMOS

- There are two component that established the amount of power dissipated in CMOS circuit .These are
- Static dissipation due to leakage current or other current drawn continuously from power supply.
- Dynamic dissipation due to
  - ❑ Switching transient current
  - ❑ Charging and discharging of load capacitance

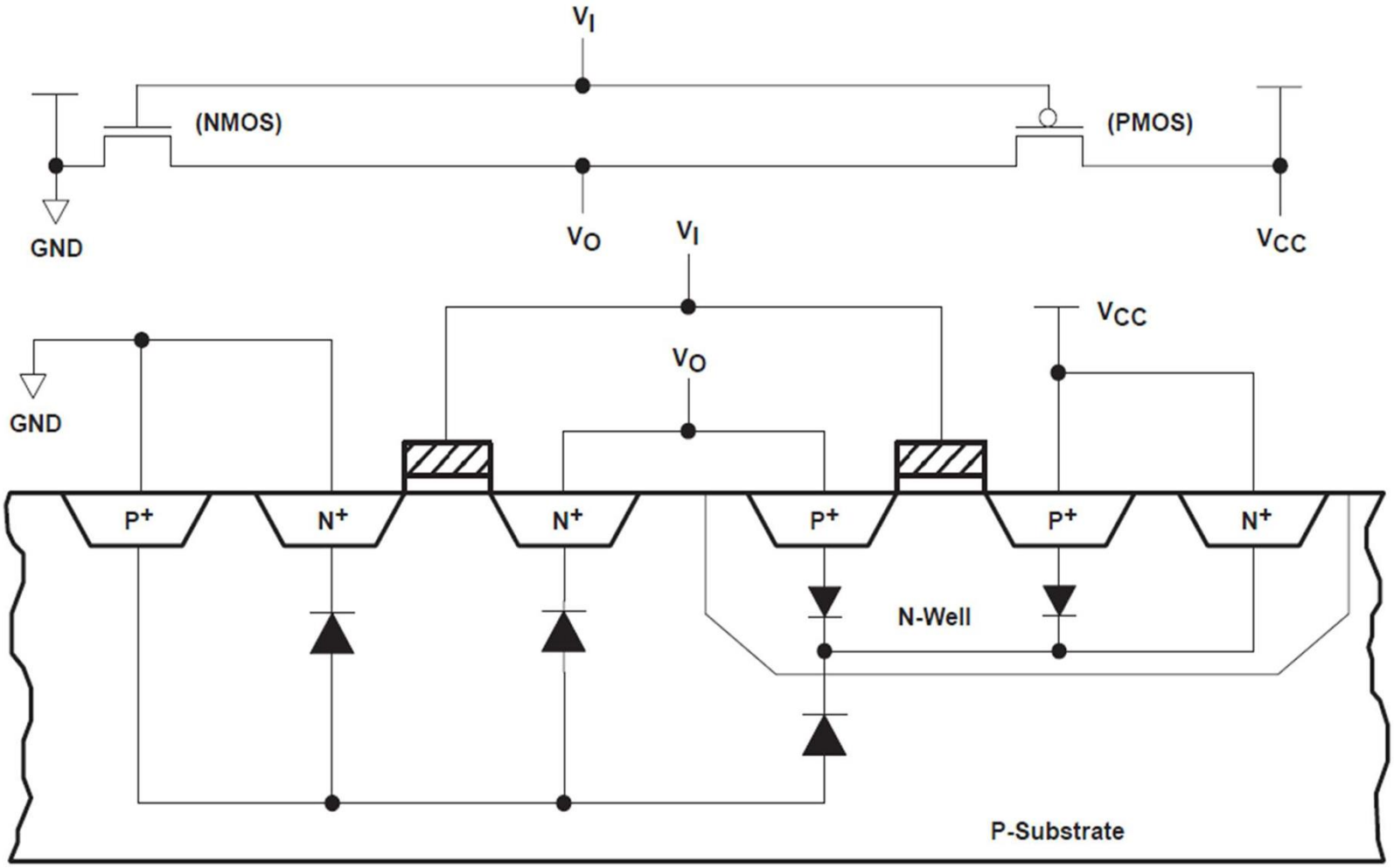
Static dissipation

- As shown in Figure 1, if input is at logic 0, n-MOS device is OFF, and p-MOS device is ON, output voltage is V_{DD}, or logic 1.
- Similarly, when input is at logic 1, n-MOS device is biased ON and p- MOS device is OFF, output voltage is GND, or logic 0.
- Note that one of transistors is always OFF when gate is in either of these logic states.
- Since no current flows into gate terminal, and there is no dc current path from VCC to GND, resultant quiescent (steady-state) current is zero, hence, static power consumption (Ps) is zero.



CMOS Inverter Mode for Static Power Consumption

- But, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and substrate.
- This leakage inside a device can be explained with a simple model that describes parasitic diodes of a CMOS inverter, as shown below



- Source drain diffusion and N-well diffusion form parasitic diodes.
- Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption.
- Leakage current (I_0)of diode is described by equation:
- $I_0 = i_s (e^{qV/kT} - 1)$

- Where:
  - i_s = reverse saturation current
  - V = diode voltage
  - k = Boltzmann's constant (1.38×10^{-23} J/K)
  - q = electronic charge (1.602×10^{-19} C)
  - T = temperature

- Static power consumption is product of device leakage current and supply voltage.
- Total static power consumption, P_S, can be obtained as shown in equation below
- $P_S = \Sigma$ (leakage current) × (supply voltage)

- Leakage current ICC (current into a device), along with voltage, causes static power consumption in CMOS devices.
- This static power consumption is defined as quiescent, or P_S, and can be calculated by equation
- $P_S = V_{CC} \times I_{CC}$
- Where:
  - V_{CC} = supply voltage
  - I_{CC} = current into a device (sum of leakage currents)

Dynamic Power Dissipation

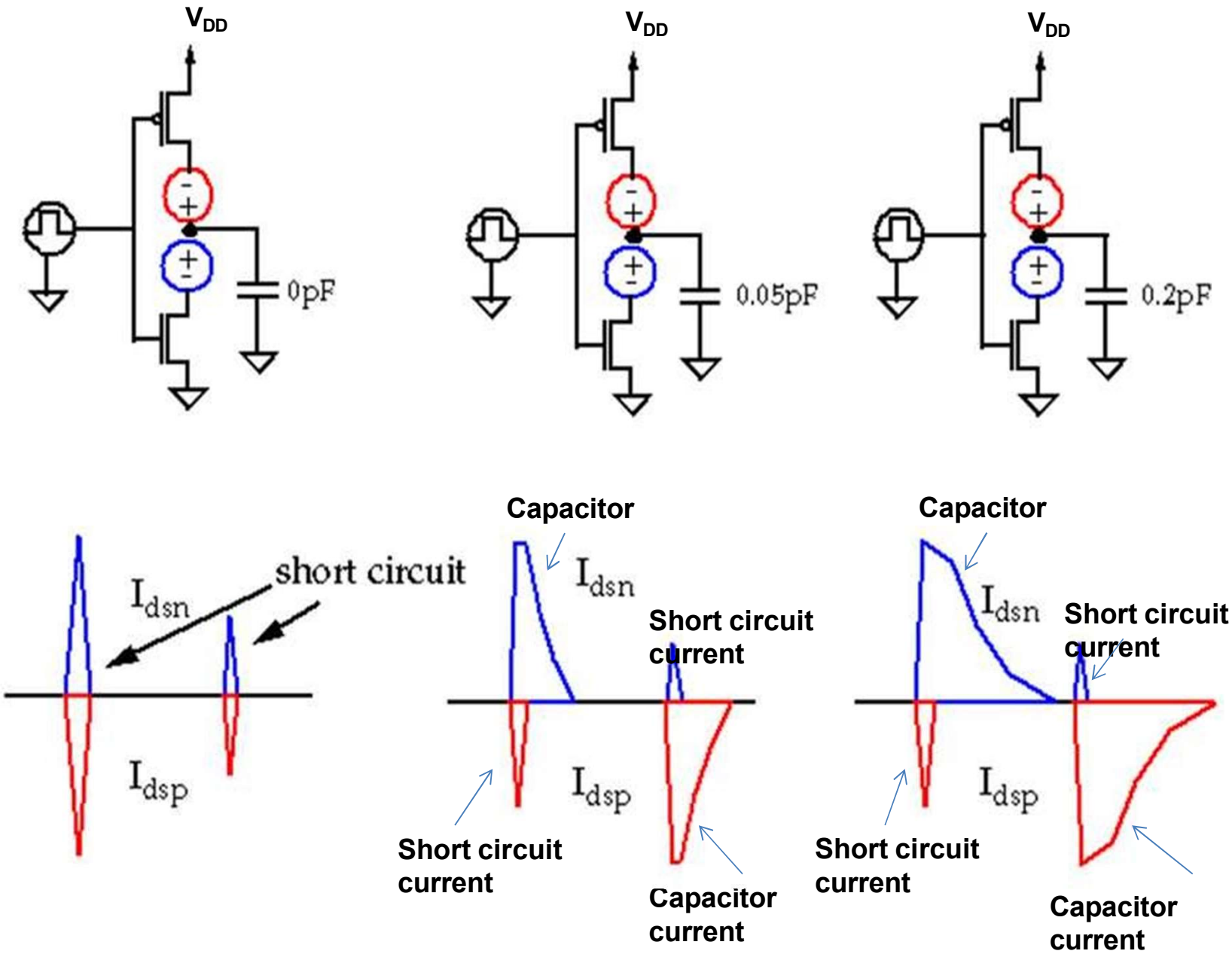
- During transition from 0 to 1 or 1 to 0, both PMOS and NMOS are ON for a short period of time.Which results in a short current pulse from V_{DD} to GND.
- Current is also needed to charge and discharge output load capacitance C_L.

- Current pulse from V_{DD} to GND results in a short circuit dissipation which is dependent on **rise/fall time of input, load capacitance C_L and gate design.**
- Figure shows 3 inverters with varying load from 0pF to 0.2pF with voltage sources to measure currents in SPICE.

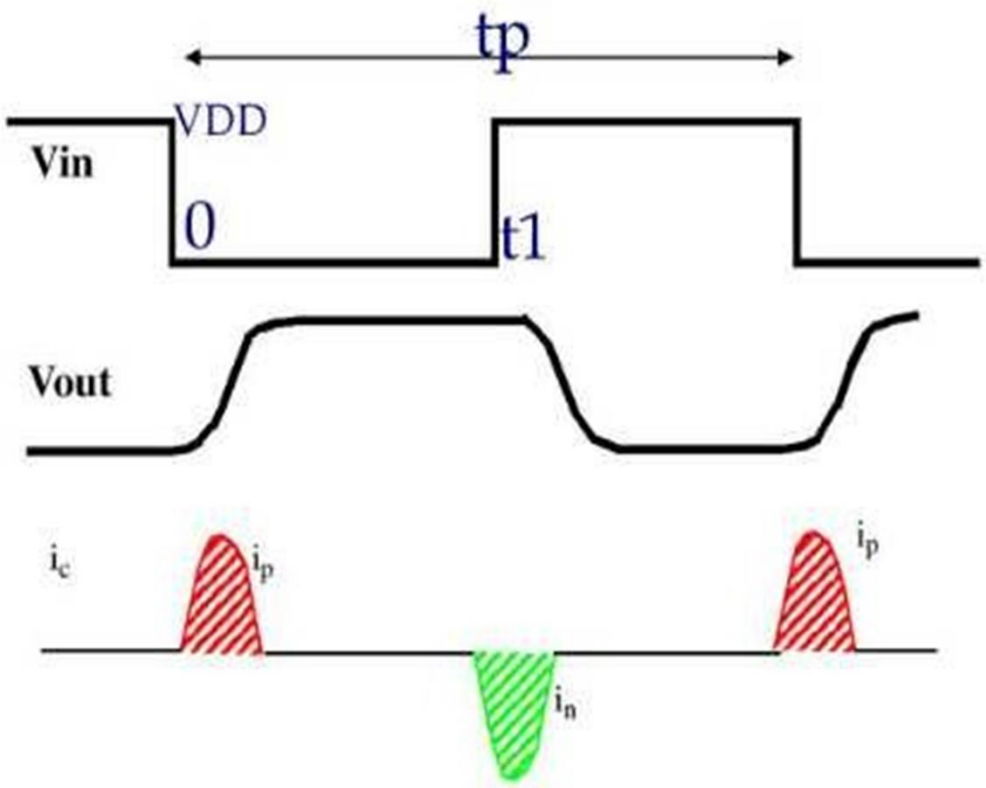
- Current flowing in PMOS and NMOS are shown beside each inverter.

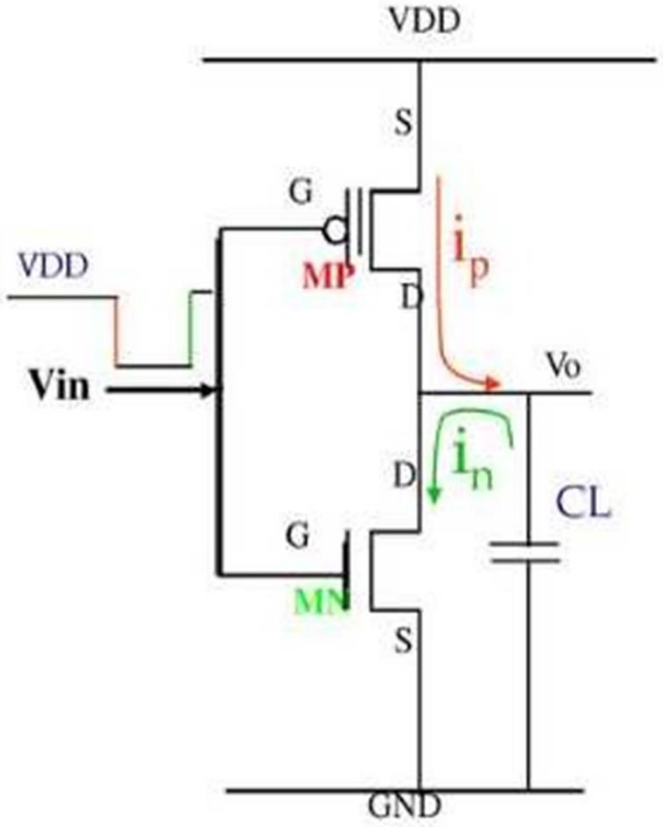
- With no load short circuit current is relatively apparent.

- As load capacitance C_L increases, charge and discharge current starts to dominate current drawn from power supply.


V_{DD}
0pF
V_{DD}
0.05pF
V_{DD}
0.2pF
I_{dsn}
short circuit
I_{dsp}
Capacitor
I_{dsn}
Short circuit current
I_{dsp}
Short circuit current
Capacitor current
Capacitor
I_{dsn}
Short circuit current
I_{dsp}
Short circuit current
Capacitor current

Power Dissipation: Dynamic





Power Dissipation: Dynamic

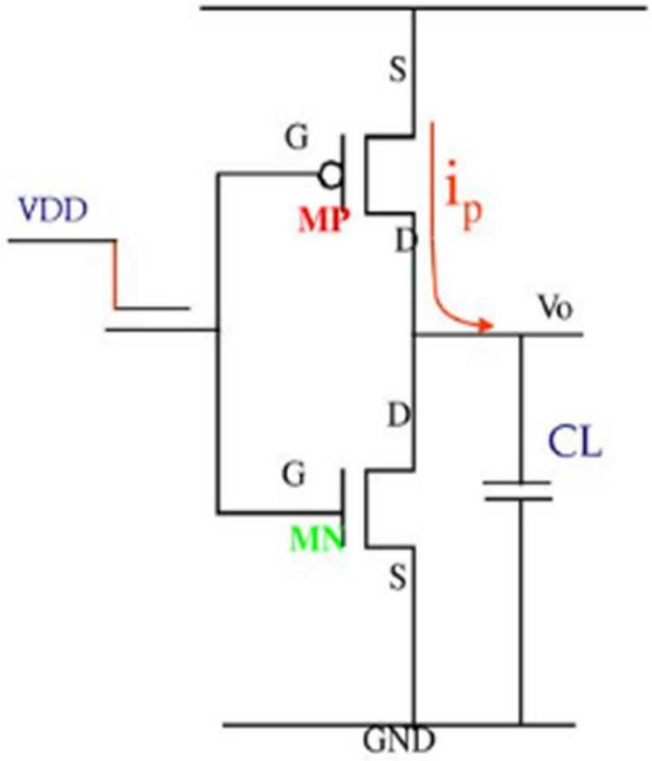
During charging

$$P_{dp} = \frac{1}{tp}\int_0^{t1} ip(t)(VDD - Vo)dt$$

$$ip(t) = C_L \frac{dVo}{dt}$$

$$Pdp = \frac{C_L}{tp}\int_0^{VDD} (VDD - Vo)dVo$$

$$Pdp = \frac{C_L}{2tp}(VDD)^2$$



Power Dissipation: Dynamic

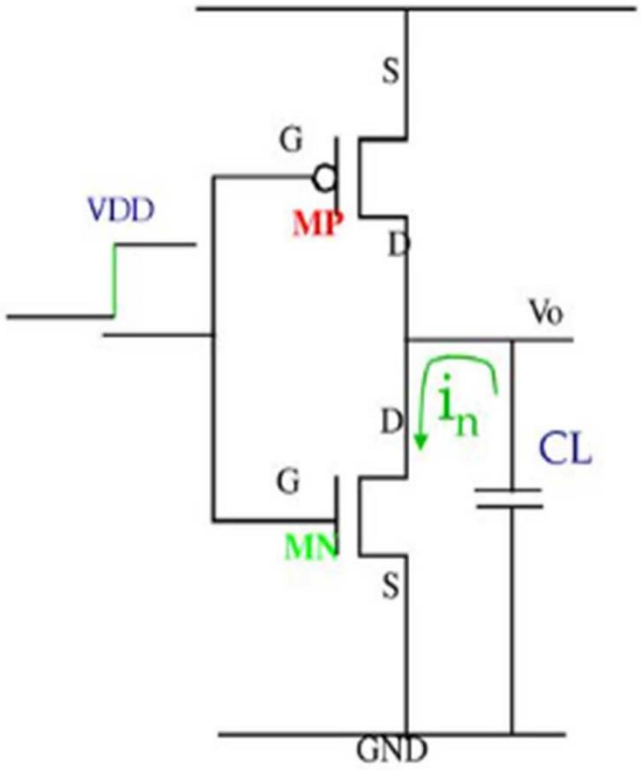
During Discharging

$$Pdn = \frac{1}{tp}\int_{t1}^{tp} in(t)Vodt$$

$$in(t) = -C_L\frac{dVo}{dt}$$

$$Pdn = \frac{C_L}{tp}\int_{VDD}^{0} -VodVo$$

$$= \frac{C_L}{tp}\frac{VDD^2}{2}$$



Power Dissipation: Dynamic

Total Power dissipation

$$Pdp + Pdn = (C_L/tp)\,(V_{DD})^2$$
$$= C_L\, f.\, (V_{DD})^2$$

Taking node activity factor α into consideration:

The power dissipation= $\alpha\, C_L\, f.\, (V_{DD})^2$

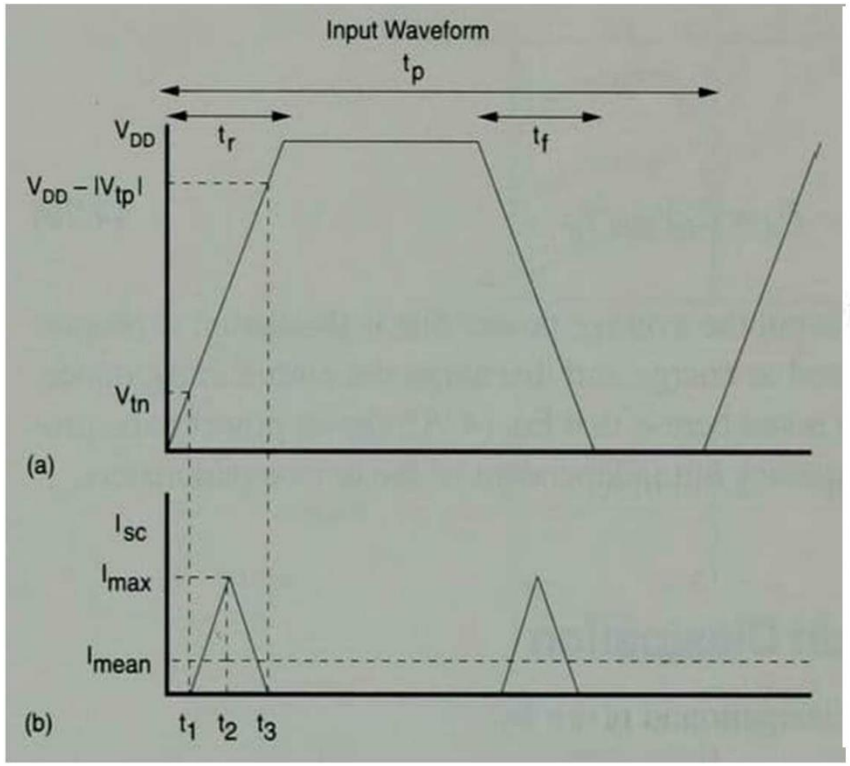
- **Where α is the switching probability or activity factor at the output node (i.e. the average number of output switching events per clock cycle).**

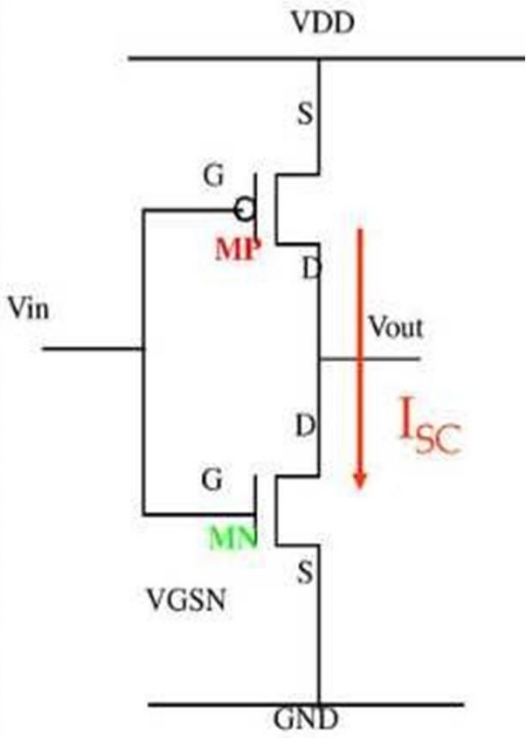
Short circuit Power Dissipation

- Short circuit Power Dissipation is given by
- Psc = Imean*VDD

$$P_{sc} = \frac{\beta}{12}(V_{DD} - 2V_t)^3 \frac{t_{rf}}{t_p}.$$

- Where tp is period of input waveform
- For input waveform as shown which shows short circuit current for an unloaded inverter





- It shows that short circuit current is dependent on $\beta(=\mu\varepsilon/t_{ox})(W/L)$ and input waveform rise and fall times.
- Slow rise time can result in significant short circuit dissipation for loaded inverters.

Total power consumption

- The total power consumption of the CMOS inverter is expressed as sum of its three components

  - $P_{total} = P_s + P_d + P_{sc}$

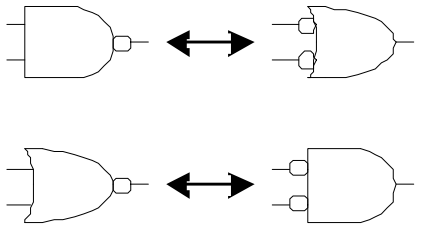
  - Where P_s is Static power consumption
  - P_d is Dynamic power consumption and
  - P_{SC} is short circuit power consumption

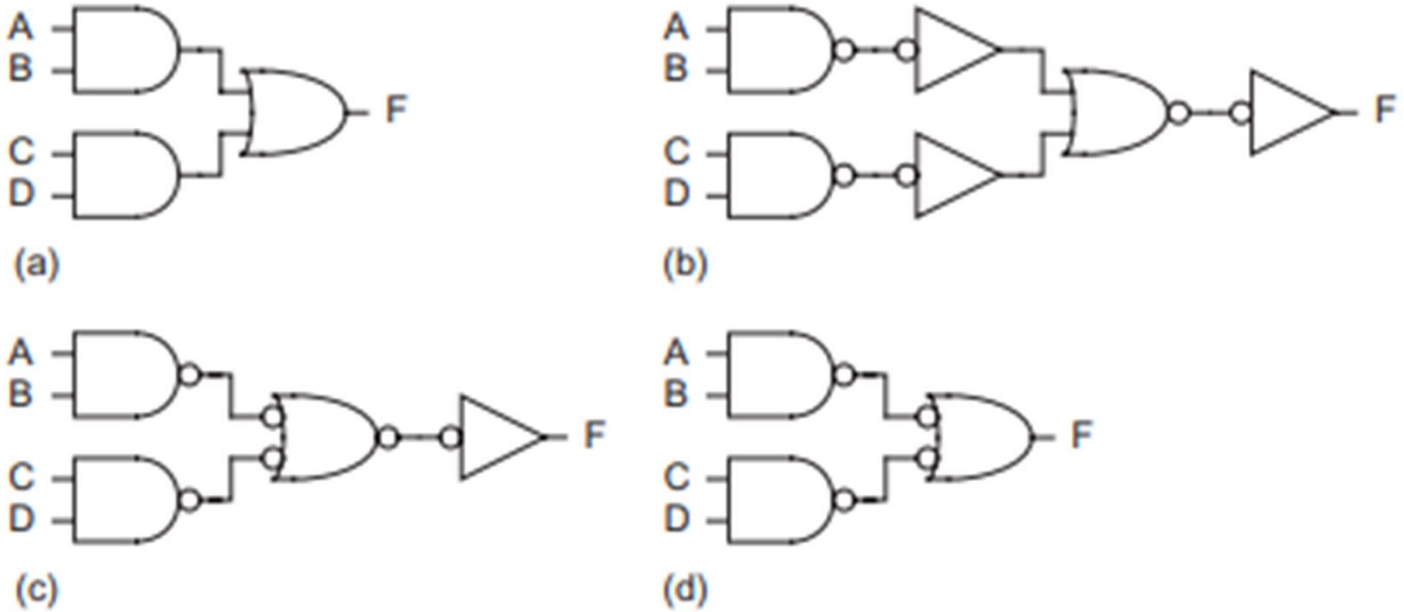
Static CMOS

Start with network of AND / OR gates
Convert to NAND / NOR + inverters
Push bubbles around to simplify logic

Remember DeMorgan's Law

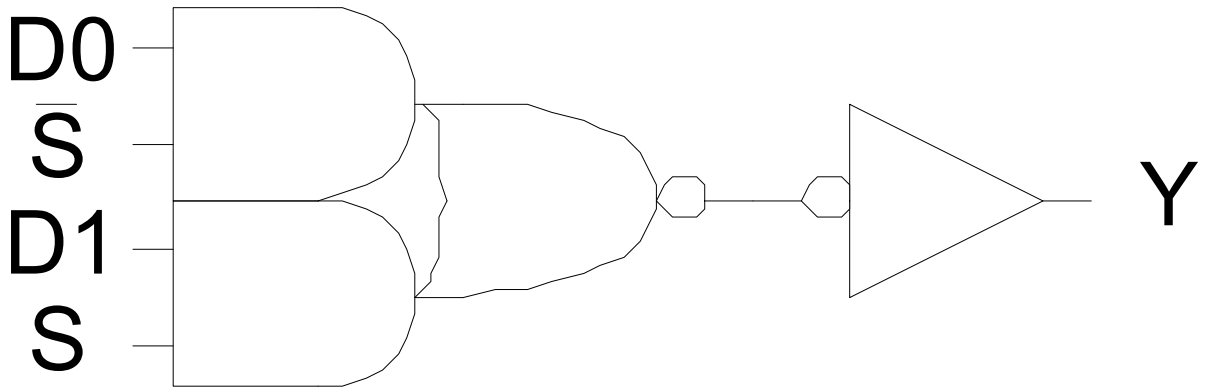
$F=\overline{AB+CD}$





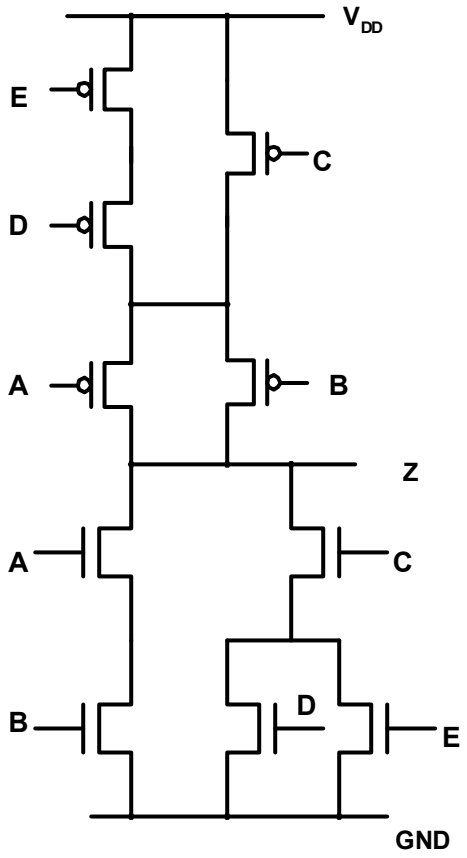
Sketch a design using one compound gate and one NOT gate. Assume ~S is available

$F = D0 \cdot \overline{S} + D1 \cdot S$



CMOS Logic Structures

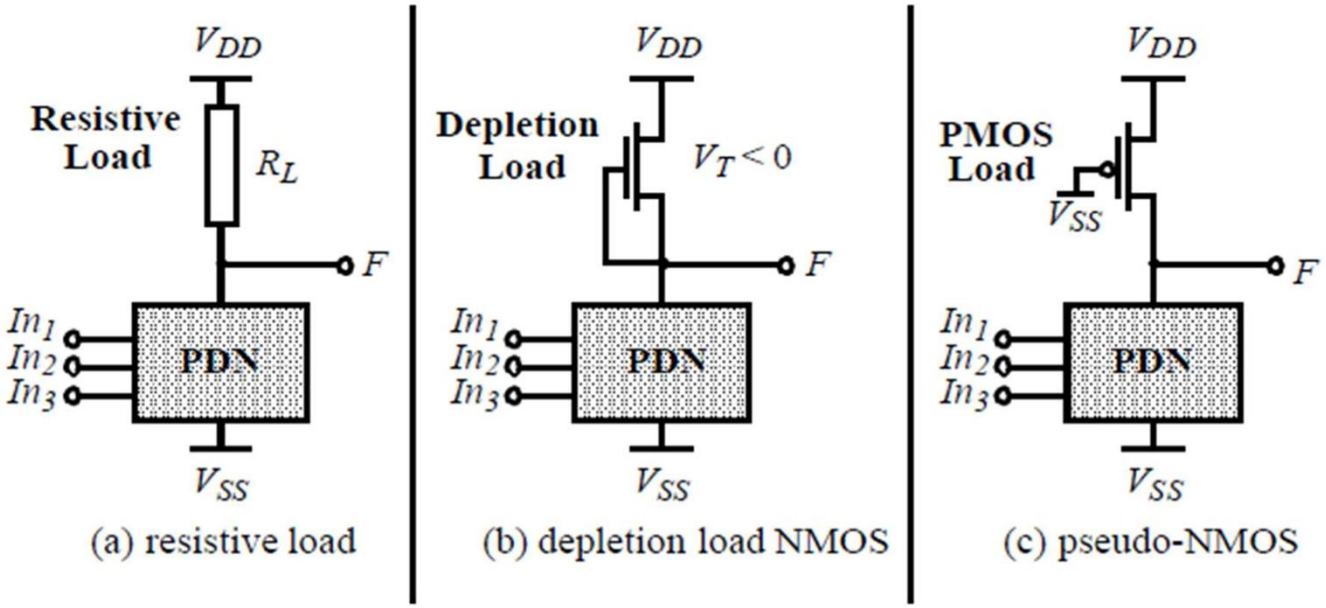
CMOS Complementary Logic



$$Z = \overline{A*B + C(D+E)}$$

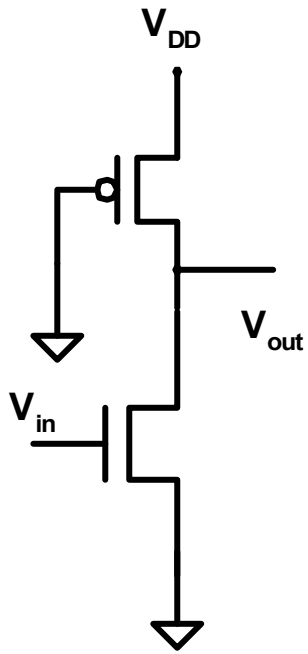
Ratioed Logic:Concept

- Ratioed logic is an attempt to reduce number of transistors required to implement a given logic function, at cost of reduced robustness and extra power dissipation.
- Purpose of PUN in complementary CMOS is to provide a conditional path between VDD and output when PDN is turned off.
- In ratioed logic, entire PUN is replaced with a single unconditional load device that pulls up output for a high output.
- Instead of a combination of active pull-down and pull-up networks, such a gate consists of an NMOS pull-down network that realizes logic function, and a simple load device.

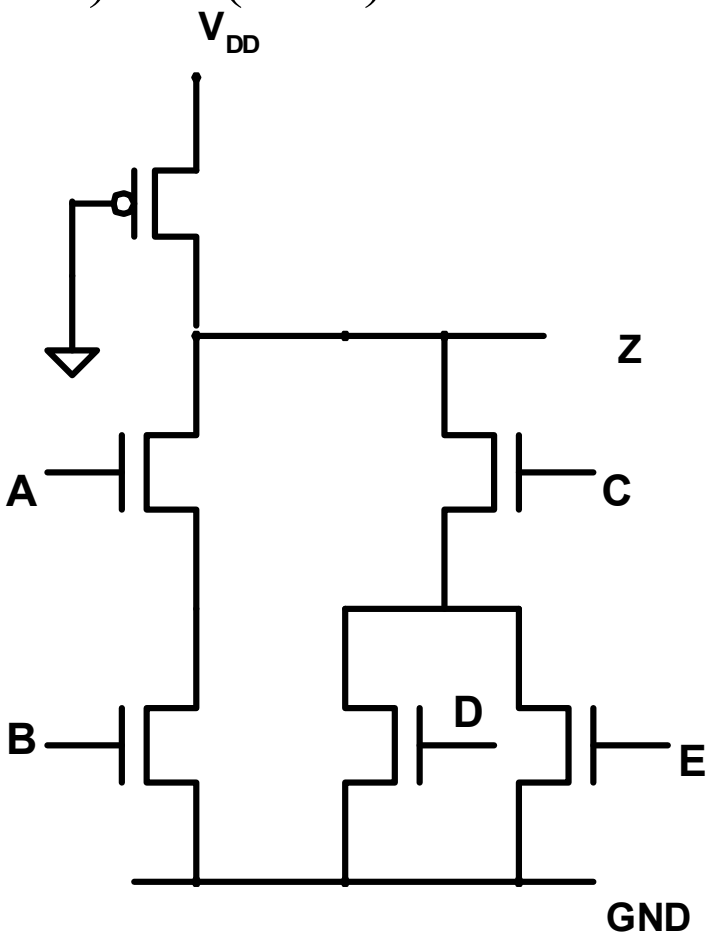


CMOS Logic Structures

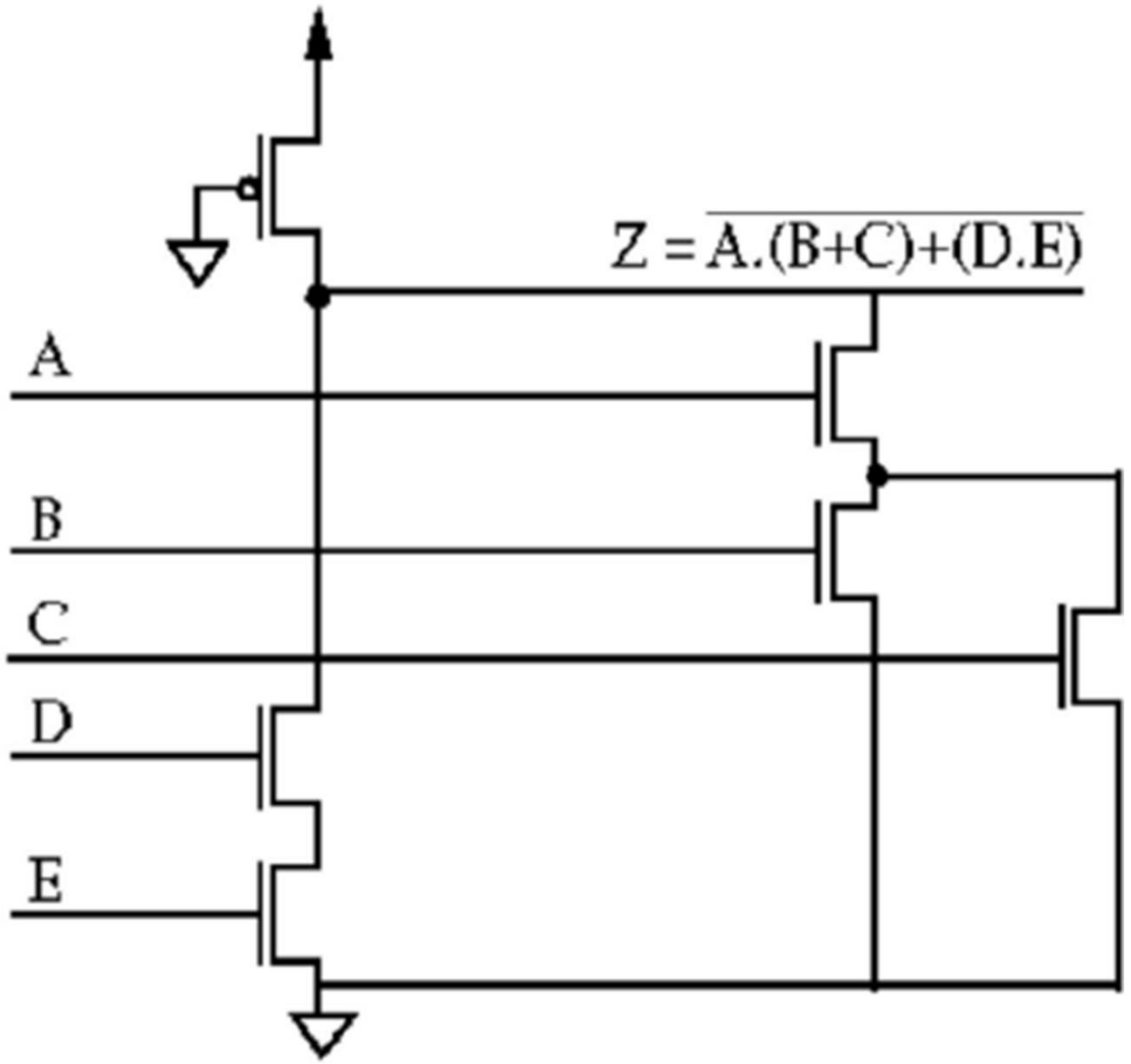
Pseudo-nMOS logic



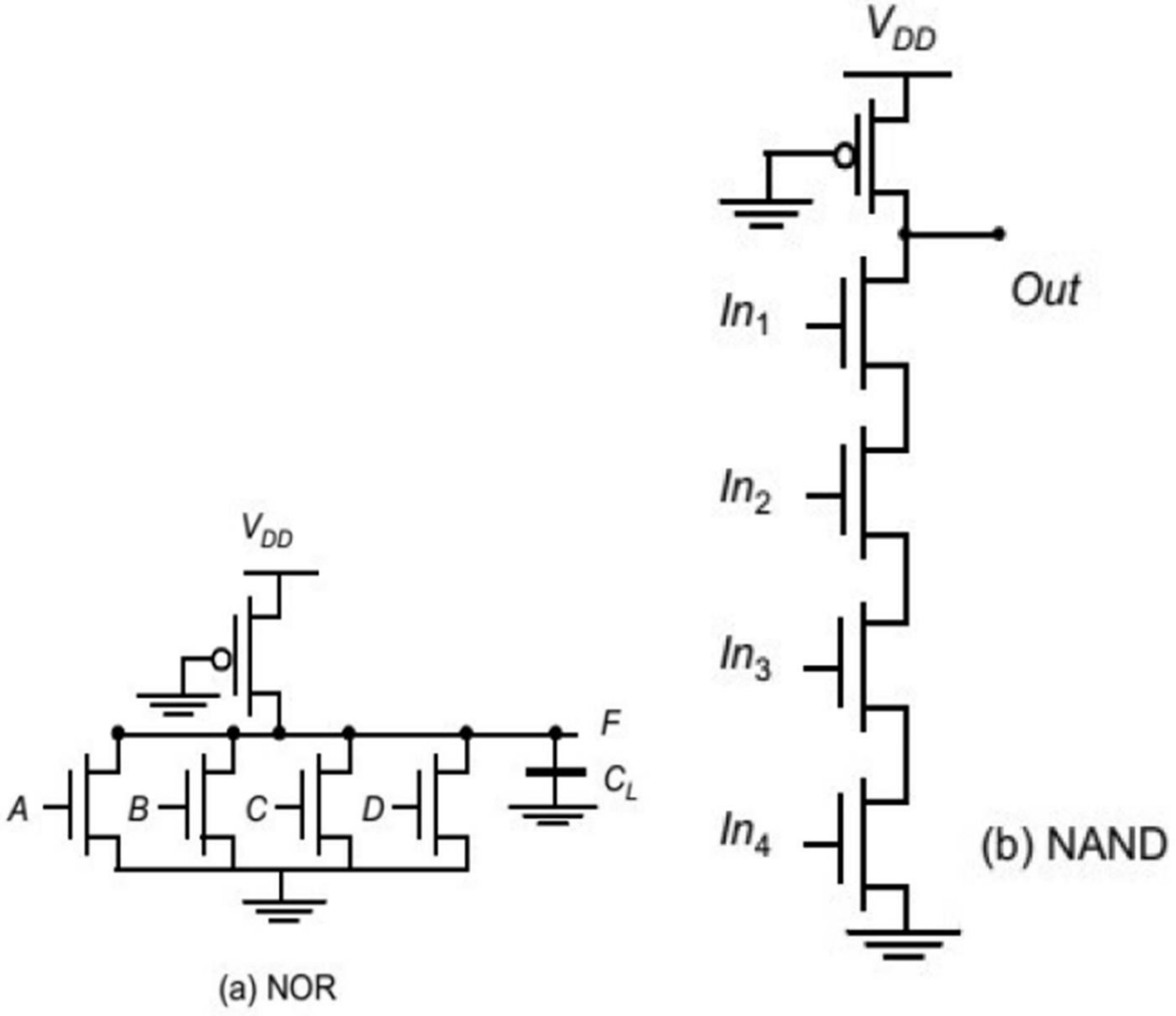
$$F = \overline{(A.B) + C.(D+E)}$$



Implementation of $Z = \overline{A.\ (B + C\ ) + (D.\ E)}$



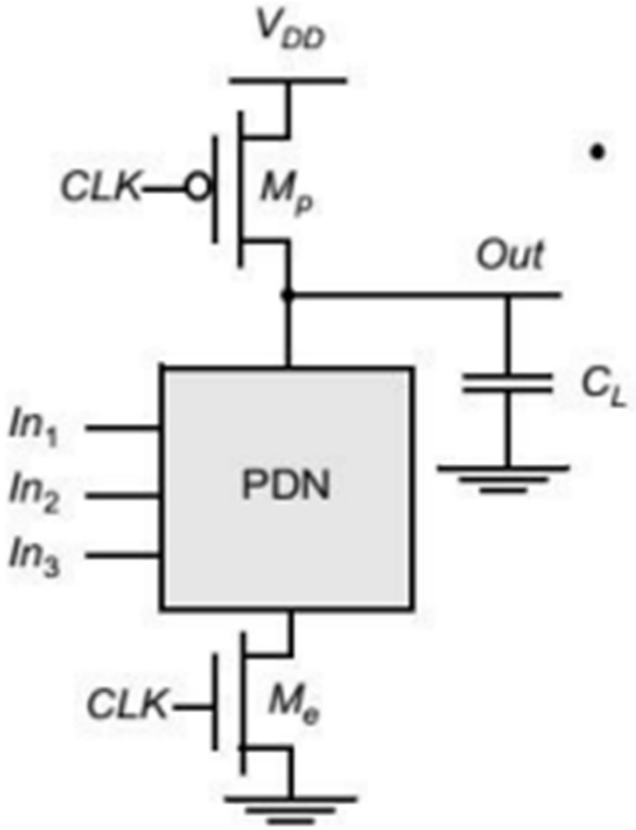
Implementation of 4 input NOR and NAND in pseudo-NMOS logic design style.



Four-input pseudo-NMOS NOR and NAND gates

Dynamic CMOS Logic

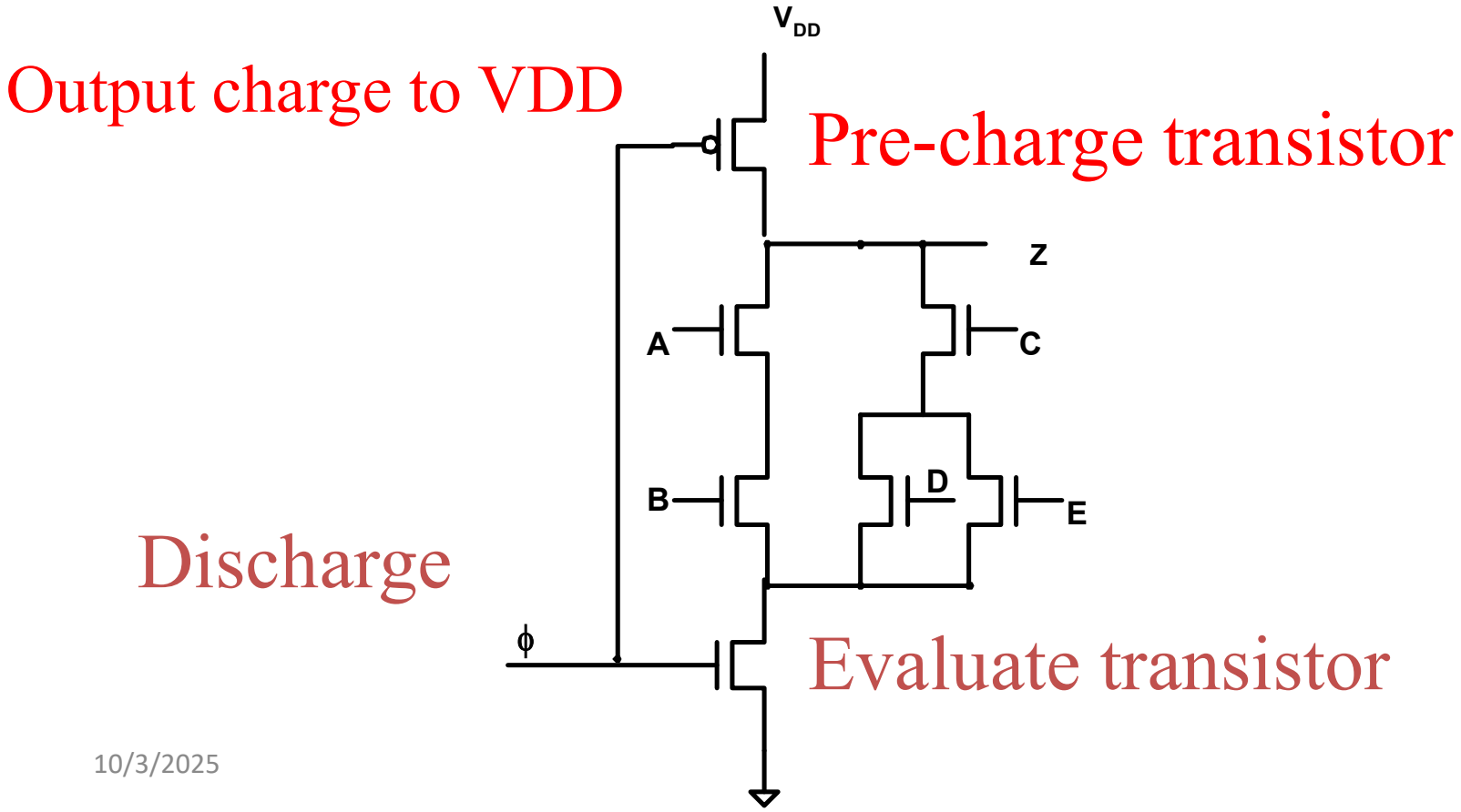
- It is designed to avoid static power dissipation with the addition of a clock input



(a) n-type network

Dynamic CMOS Logic

$$F = \overline{A*B + C(D+E)}$$



Dynamic CMOS Logic

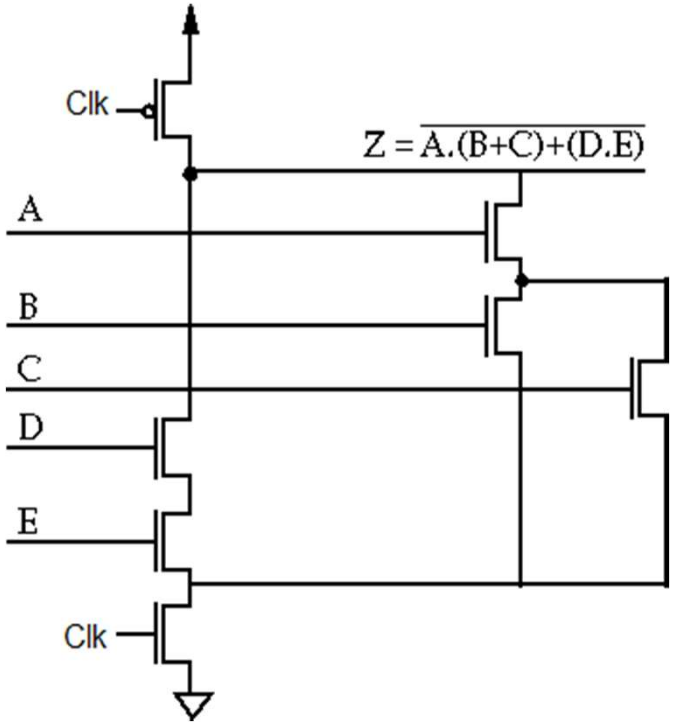
$$Z = \overline{A*B + C(D+E)}$$ When $\phi = 1$

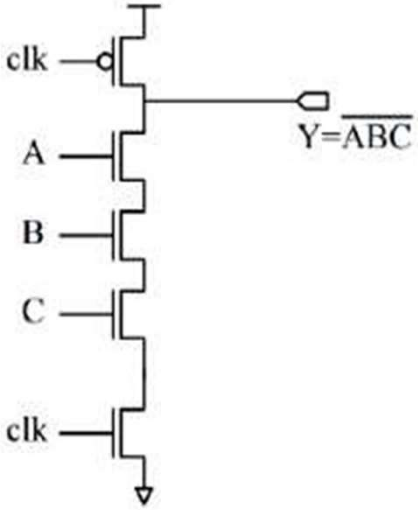
$Z = High$ When $\phi = 0$

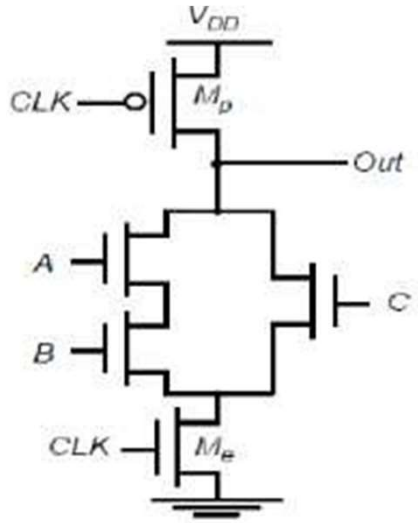
Implementation of
$Z = \overline{A.(B+C)+(D.E)}$ i

Implementation of
$Z = \overline{ABC}$

Implementation of
$Z = \overline{AB+C}$

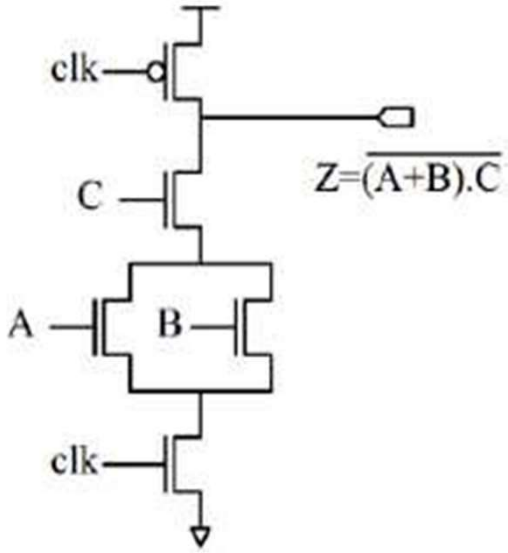






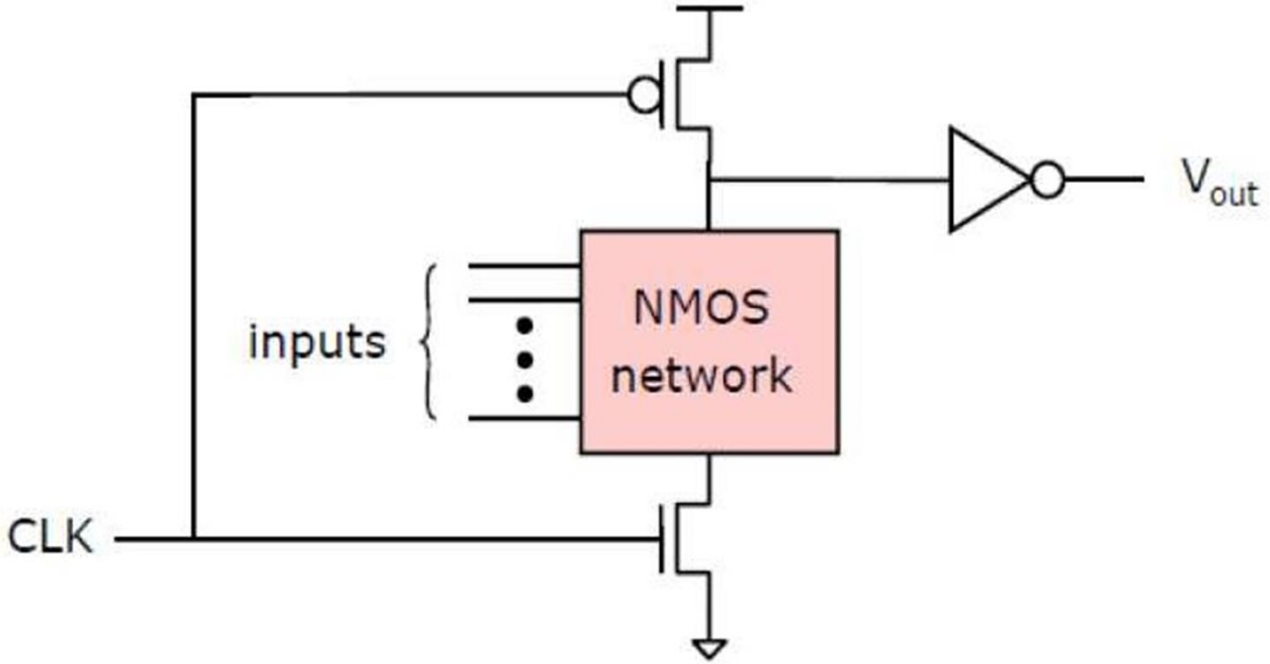
$Z = \overline{A.(B+C)+(D.E)}$ $when\ ClK = 1$
Z = HIGH when Clk = 0

Implementation of
$Z = \overline{(A + B).C}$



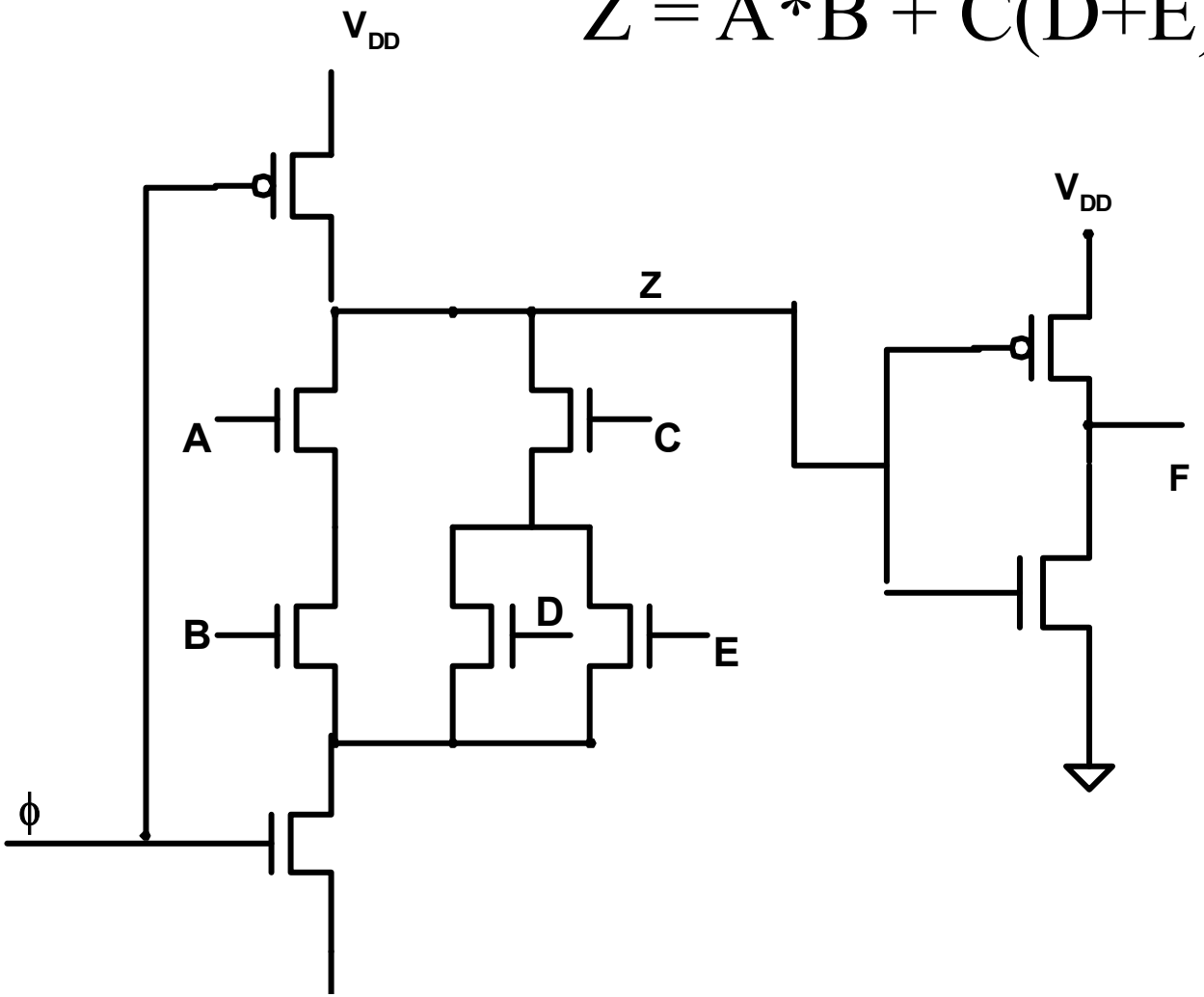
Domino Logic

- A Domino logic module consists of an n-type dynamic logic block followed by a static inverter.



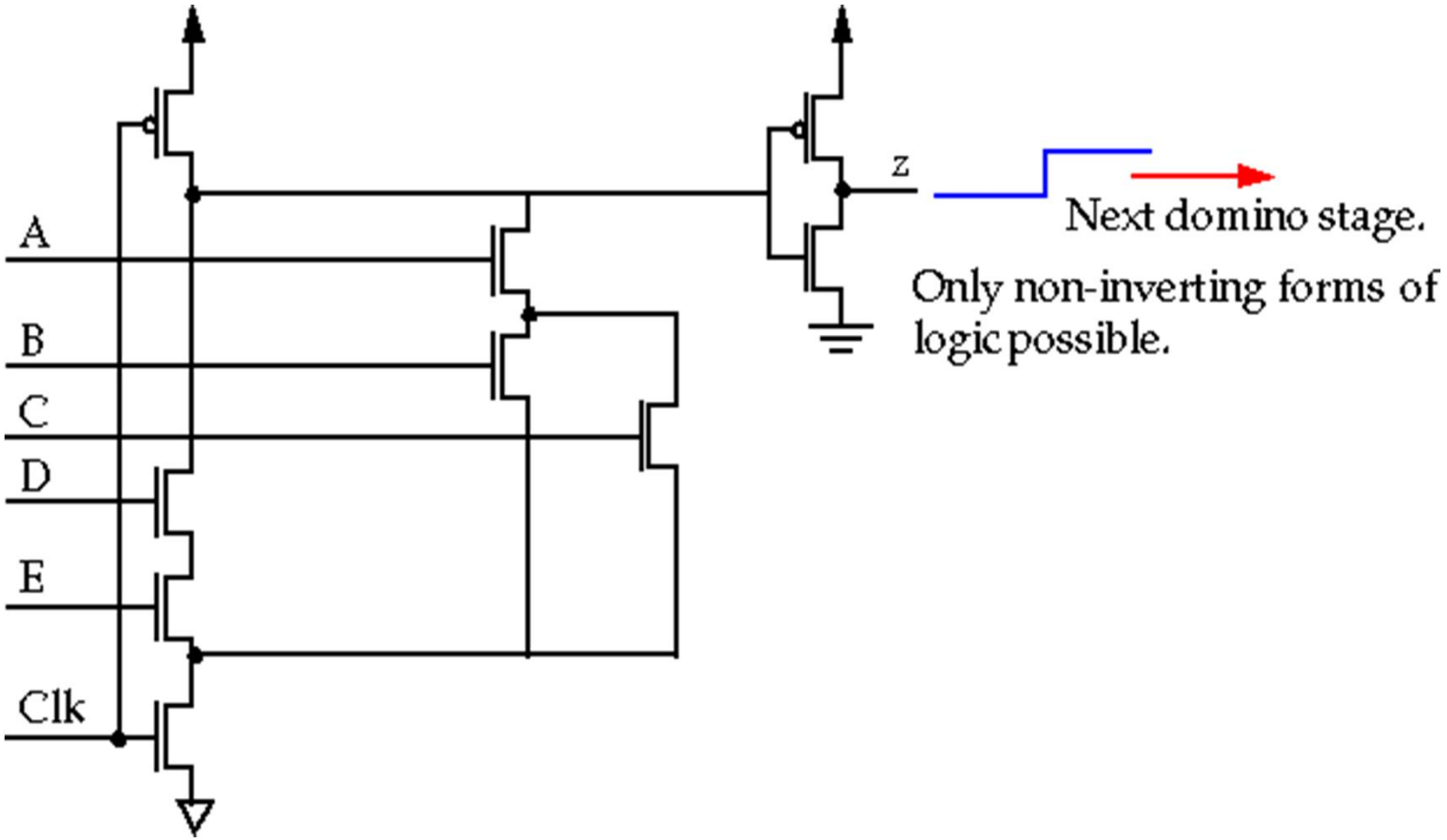
Domino Logic

$$Z = \overline{A*B + C(D+E)}$$



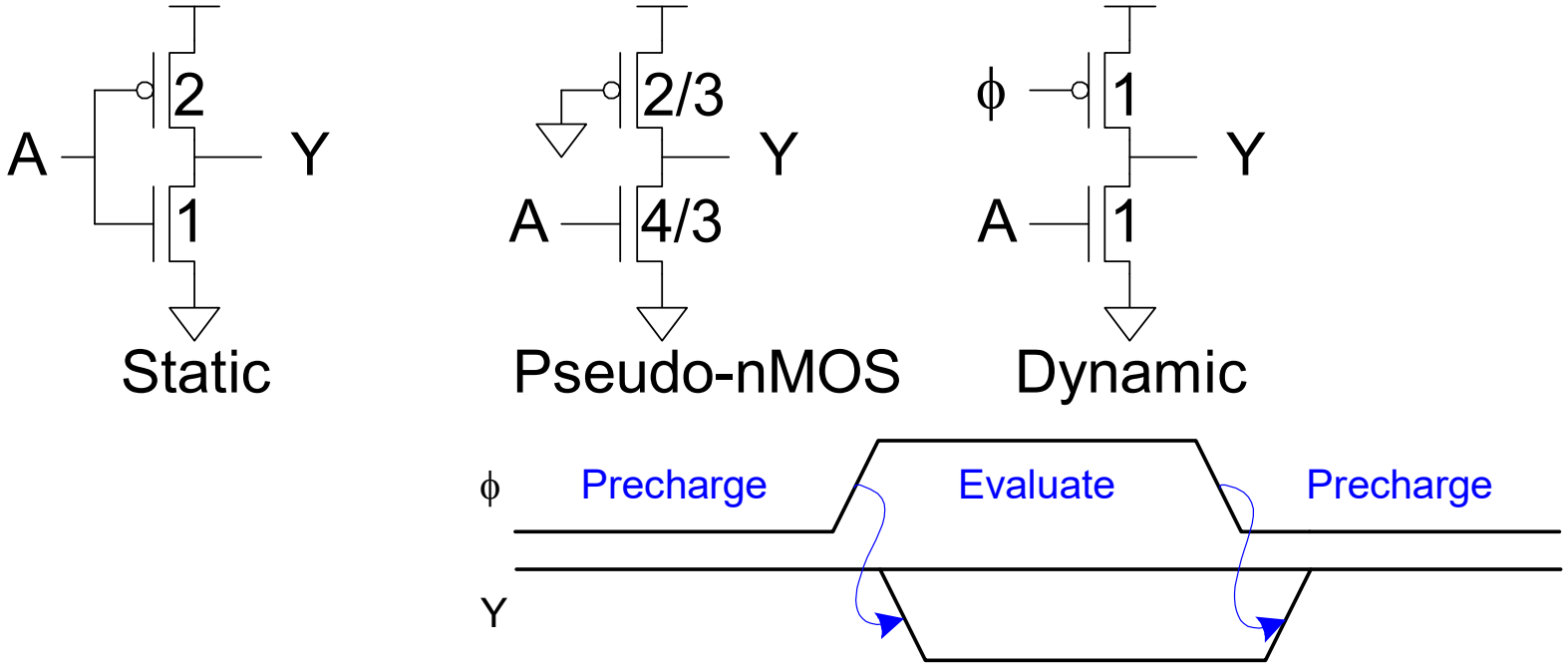
Implementation of

$Z = \overline{A.(B + C) + (D.E)}$



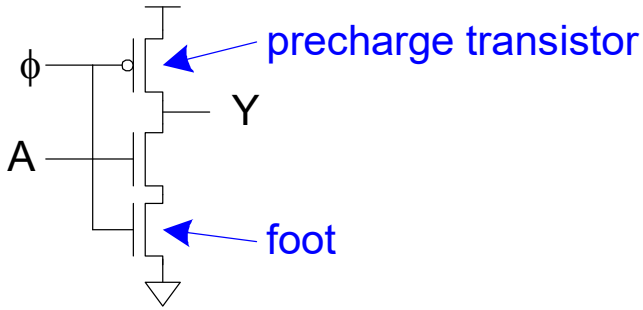
Dynamic Logic

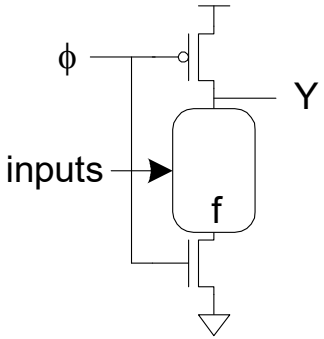
- *Dynamic* gates uses a clocked pMOS pullup
- Two modes: *precharge* and *evaluate*



The Foot

- What if pulldown network is ON during precharge?
- Use series evaluation transistor to prevent fight.





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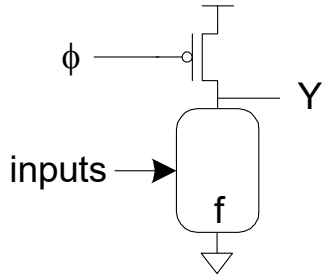
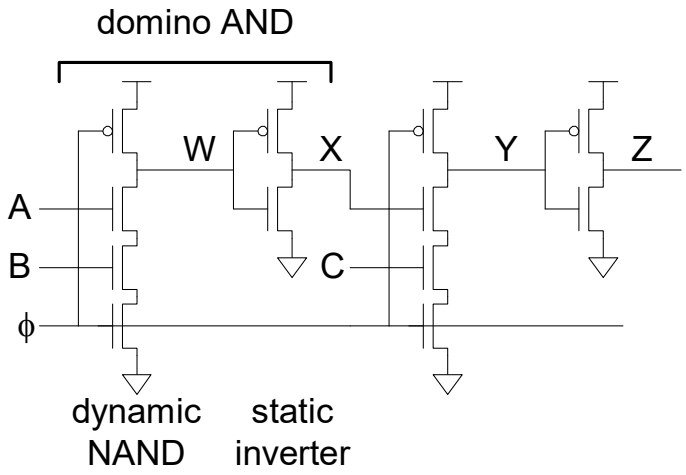
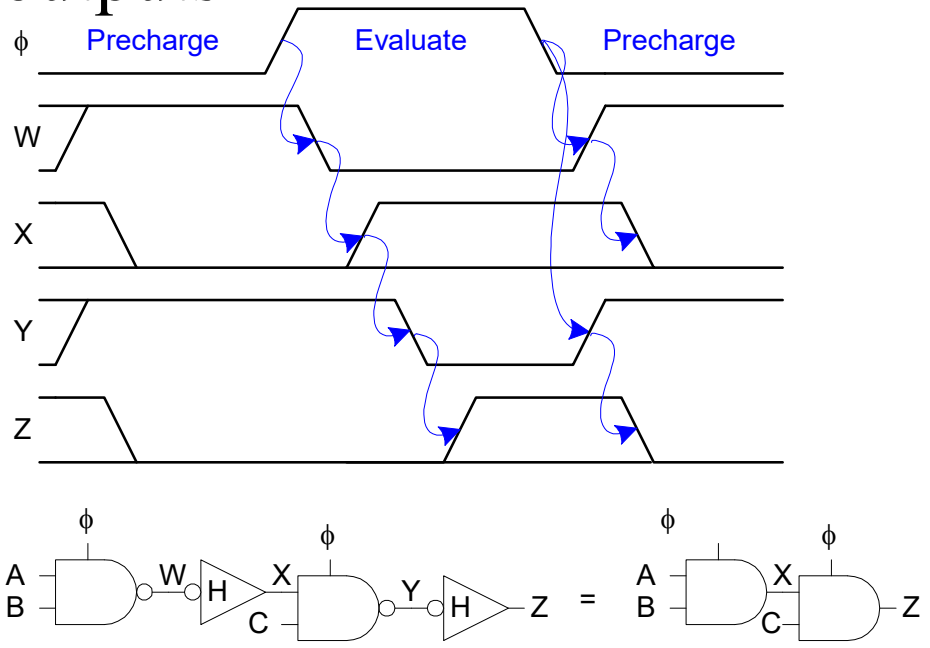


unfooted

Domino Gates

- Follow dynamic stage with inverting static gate
  - Dynamic / static pair is called domino gate
  - Produces monotonic outputs

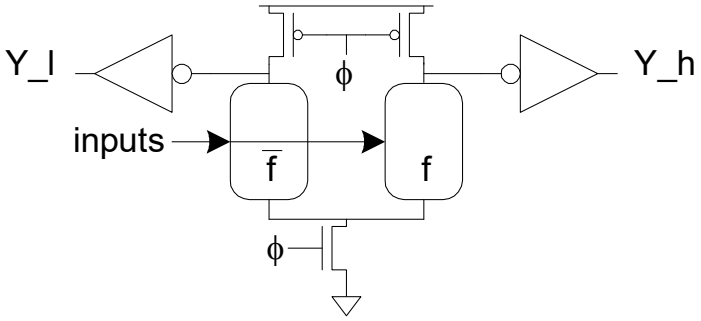




Dual-Rail Domino

- Domino only performs noninverting functions:
  - AND, OR but not NAND, NOR, or XOR
- Dual-rail domino solves this problem
  - Takes true and complementary inputs
  - Produces true and complementary outputs

sig_h	sig_l	Meaning
0	0	Precharged
0	1	‘0’
1	0	‘1’
1	1	invalid

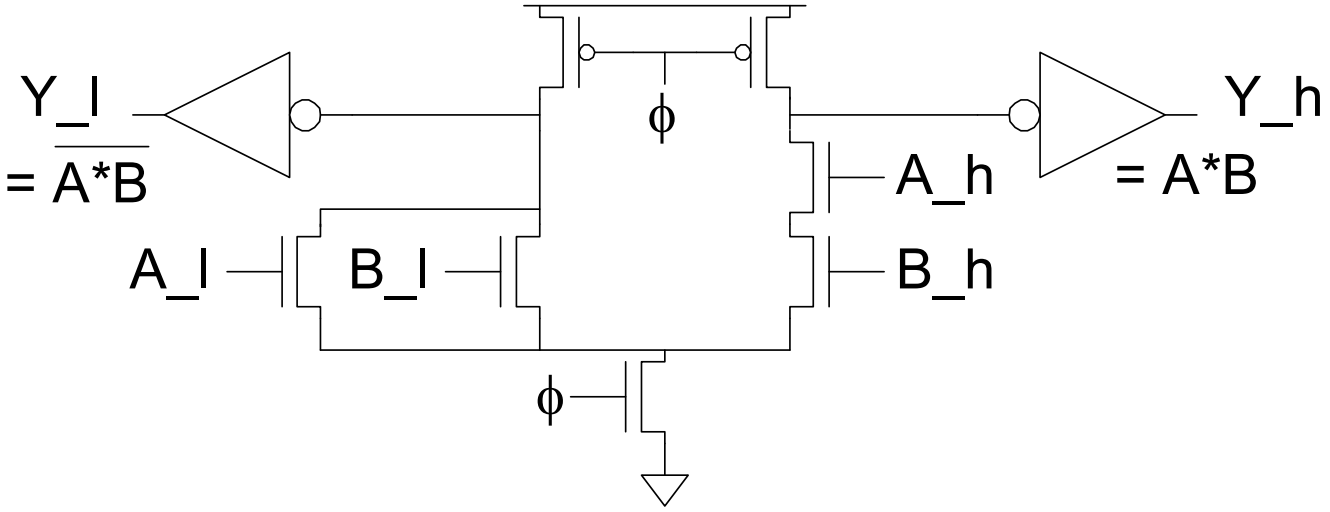


Example: AND/NAND

- Given A_h, A_l, B_h, B_l
- Compute Y_h = A * B, Y_l = ~(A * B)

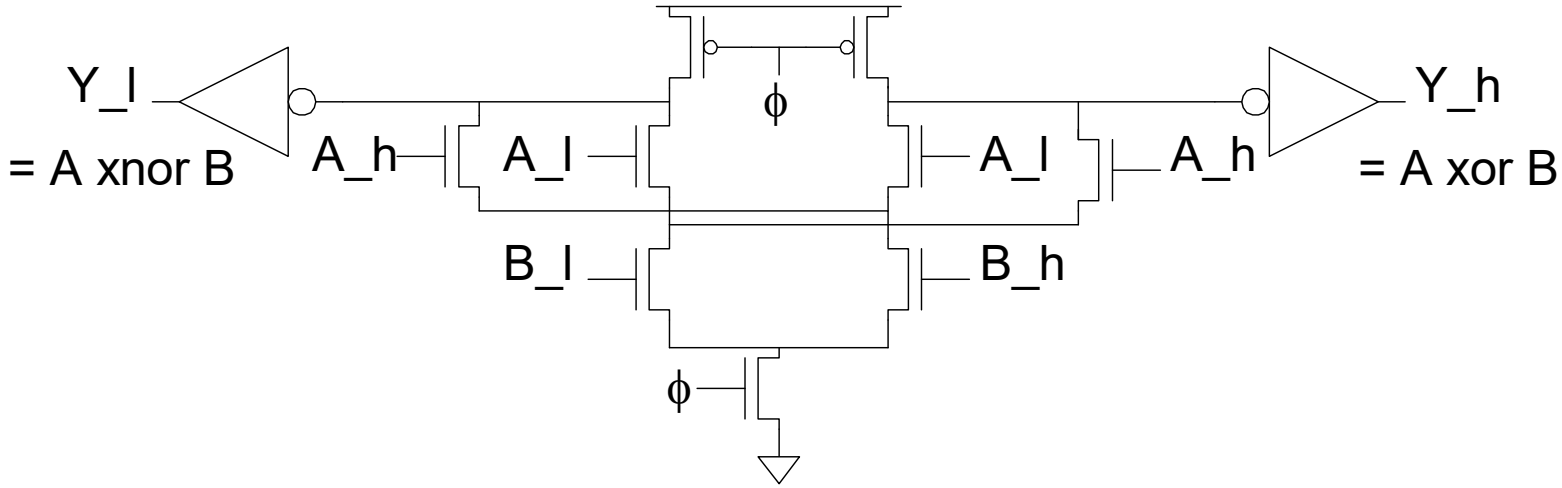
Example: AND/NAND

- Given A_h, A_l, B_h, B_l
- Compute Y_h = A * B, Y_l = ~(A * B)
- Pulldown networks are conduction complements



Example: XOR/XNOR

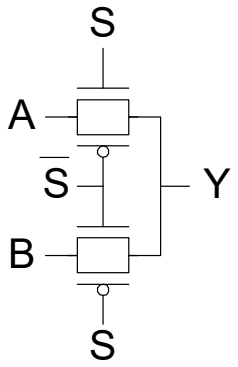
- Sometimes possible to share transistors

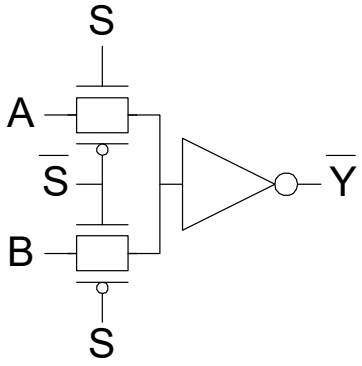


Pass Transistor Circuits

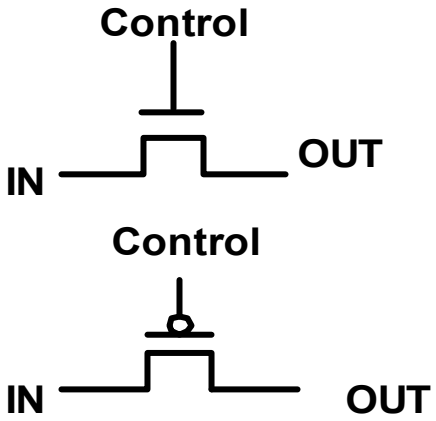
- Use pass transistors like switches to do logic
- Inputs drive diffusion terminals as well as gates

- CMOS + Transmission Gates:
  - 2-input multiplexer
  - Gates should be restoring





Pass Transistor Logic



XOR Truth Table

A	B	A xor B	Pass function
0	0	0	/A + /B
0	1	1	/A + B
1	0	1	A + /B
1	1	0	/A + /B

P

	0	1
0	A B	A /B
1	/A B	/A /B