Microcontroller and Computer architecture

Lecture 2

Microprocessorr 8085: Architecture

A presentation by

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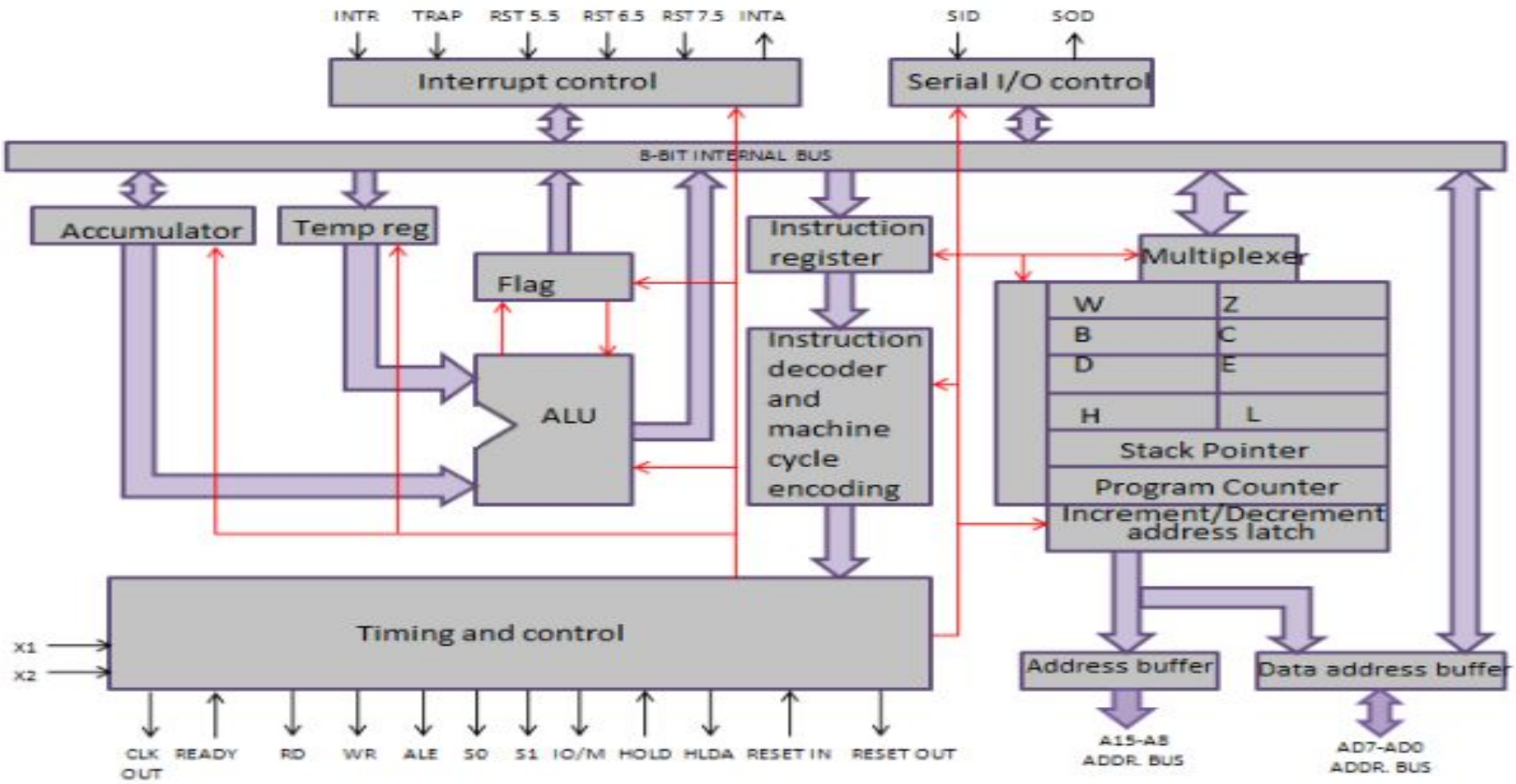
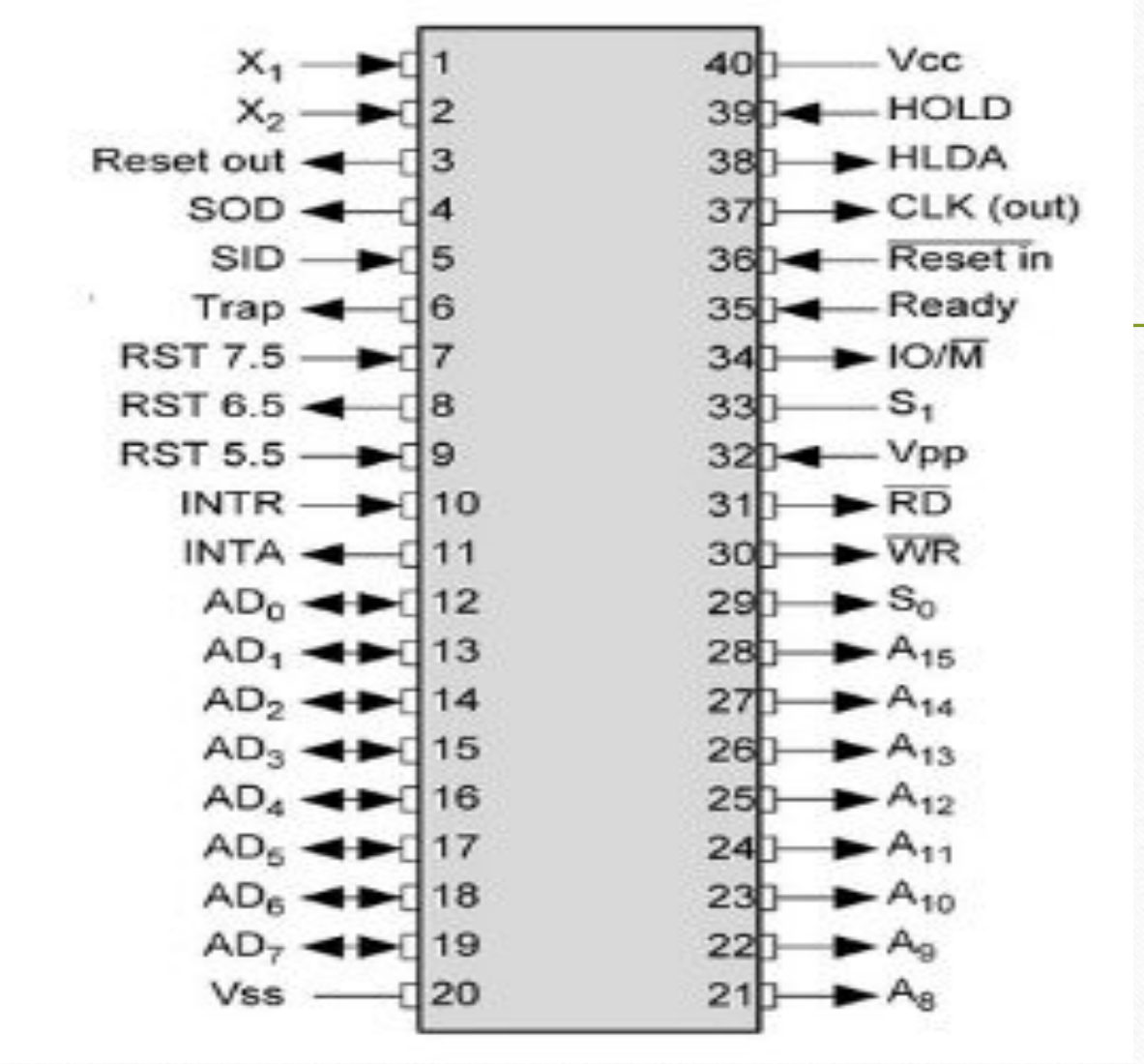

INTR
TRAP
RST 5.5
RST 6.5
RST 7.5
INTA
SID
SOD
Interrupt control
Serial I/O control
8-BIT INTERNAL BUS
Accumulator
Temp reg
Flag
ALU
Instruction register
Instruction decoder and machine cycle encoding
Multiplexer
W
Z
B
C
D
E
H
L
Stack Pointer
Program Counter
Increment/Decrement address latch
Timing and control
X1
X2
Address buffer
Data address buffer
CLK OUT
READY
RD
WR
ALE
S0
S1
IO/M
HOLD
HLDA
RESET IN
RESET OUT
A15-A8 ADDR. BUS
AD7-AD0 ADDR. BUS


X1 1
X2 2
Reset out 3
SOD 4
SID 5
Trap 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
Vss 20
40 Vcc
39 HOLD
38 HLDA
37 CLK (out)
36 Reset in
35 Ready
34 IO/M
33 S1
32 Vpp
31 RD
30 WR
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8