23VLS1401: Microcontroller and Computer architecture

Lecture 4 (U3)

Programmable Timer Counter PTC 8253
Programmable Interval Timers (PTIs)

A presentation by

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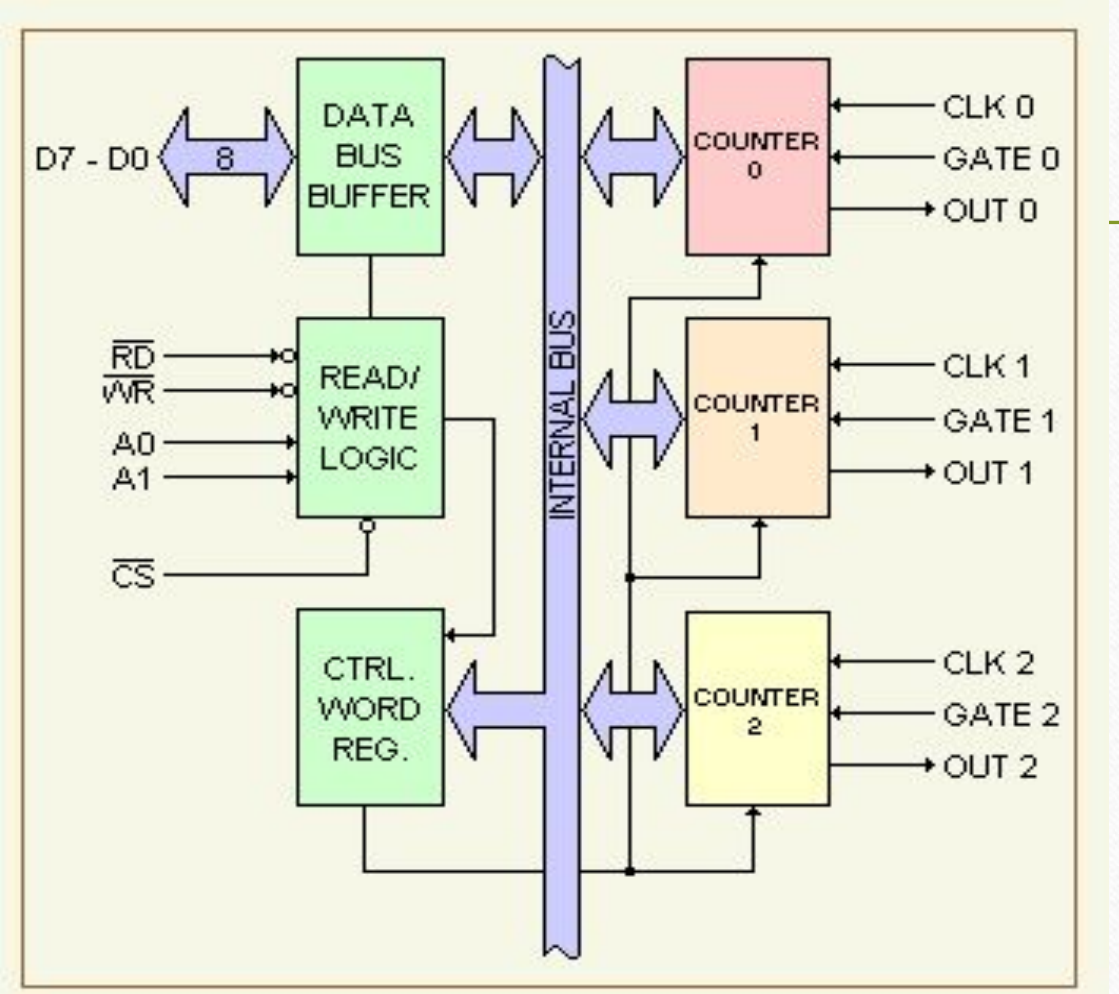
Session objectives

- To learn the architecture of Programmable Timer Counter PTC 8253
- To learn the control words for PTC
- To learn the steps required for Interfacing PTC with 8085
- To develop the interfacing diagram for PTC with 8085

Block Diagram of 8253 PTC



Functions of various blocks of 8253

- **Data Bus Buffer:** It is a tri-state, bi-directional, 8-bit buffer, which is used to interface the 8253 to the system data bus. It has three basic functions −

  - Programming the modes of 8253.
  - Loading the count registers.
  - Reading the count values.

Functions of various blocks of 8253

- **Counters**

Each counter consists of a single, 16 bit-down counter, which can be operated in either binary or BCD. Its input and output is configured by the selection of modes stored in the control word register. The programmer can read the contents of any of the three counters without disturbing the actual count in process.

Functions of various blocks of 8253

Read/Write Logic

- It includes 5 signals, i.e. $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, and the address lines A_0 & A_1. In the peripheral I/O mode, the . $\overline{RD}$, and $\overline{WR}$ signals are connected to $\overline{IOR}$ and $\overline{IOW}$, respectively. In the memory mapped I/O mode, these are connected to MEMR and MEMW.
- Address lines A_0 & A_1 of the CPU are connected to lines A_0 and A_1 of the 8253, and $\overline{CS}$ is tied to a decoded address. The control word register and counters are selected according to the signals on lines A_0 & A_1.

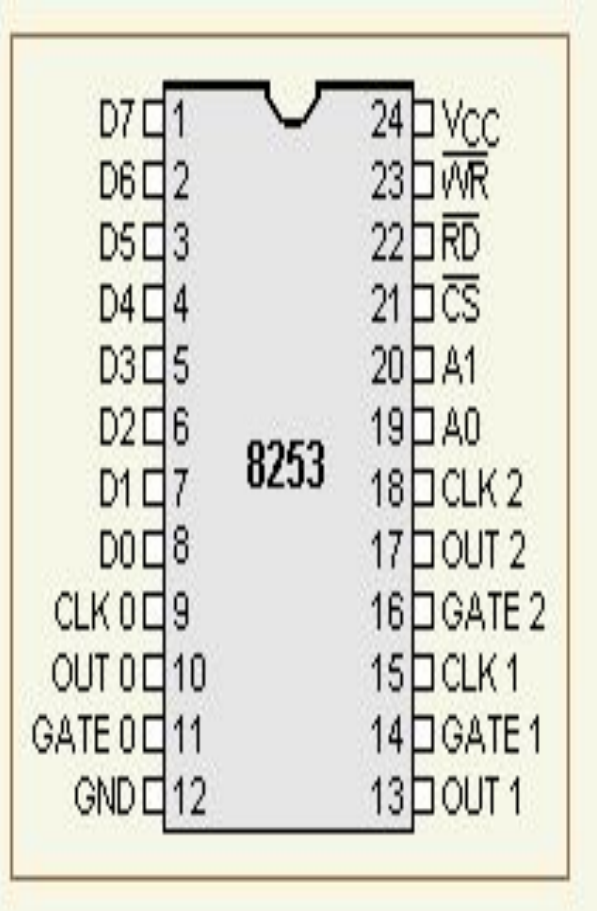
A_1	A_0	
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Control Word Register

Functions of various blocks of 8253

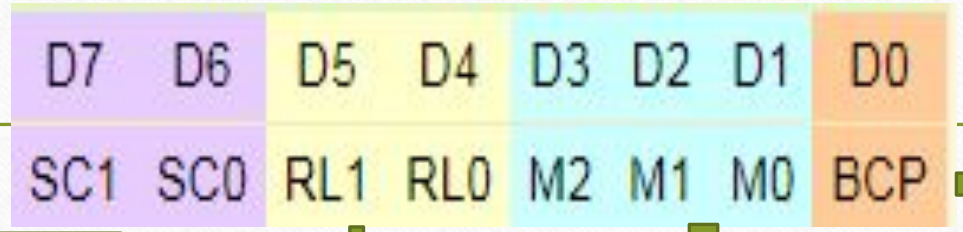
- **Control Word Register:** This register is accessed when lines A_0 & A_1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation.

A_1	A_0	RD	WR	CS	Result
0	0	1	0	0	Write Counter 0
0	1	1	0	0	Write Counter 1
1	0	1	0	0	Write Counter 2
1	1	1	0	0	Write Control Word
0	0	0	1	0	Read Counter 0
0	1	0	1	0	Read Counter 1
1	0	0	1	0	Read Counter 2
1	1	0	1	0	No operation
X	X	1	1	0	No operation
X	X	X	X	1	No operation

Pin diagram of 8255 PPI



Control word register of 8253



D7 SC1	D6 SC0	Counter Select
0	0	counter 0
0	1	counter 1
1	0	counter 2
1	1	illegal value

D0	counts down in
0	binary
1	BCD

D5 RL1	D4 RL0	R / L Definition
0	0	Counter value is latched. This means that the selected counter has its contents transferred into a temporary latch, which can then be read by the CPU.
0	1	Read / load least-significant byte only.
1	0	Read / load most-significant byte only.
1	1	Read / load least-significant byte first, then most-significant byte.

D3 M2	D2 M1	D1 M0	Mode value
0	0	0	mode 0: interrupt on terminal count
0	0	1	mode 1: programmable one-shot
x	1	0	mode 2: rate generator
x	1	1	mode 3: square wave generator
1	0	0	mode 4: software triggered strobe
1	0	1	mode 5: hardware triggered strobe

Modes of operation for 8253 PTC

- Mode 0 - Interrupt on Terminal Count
- Mode 1 – Programmable One Shot
- Mode 2 – Rate Generator
- Mode 3 – Square Wave Generator
- Mode 4 – Software Triggered Mode
- Mode 5 – Hardware Triggered Mode

D3 M2	D2 M1	D1 M0	Mode value
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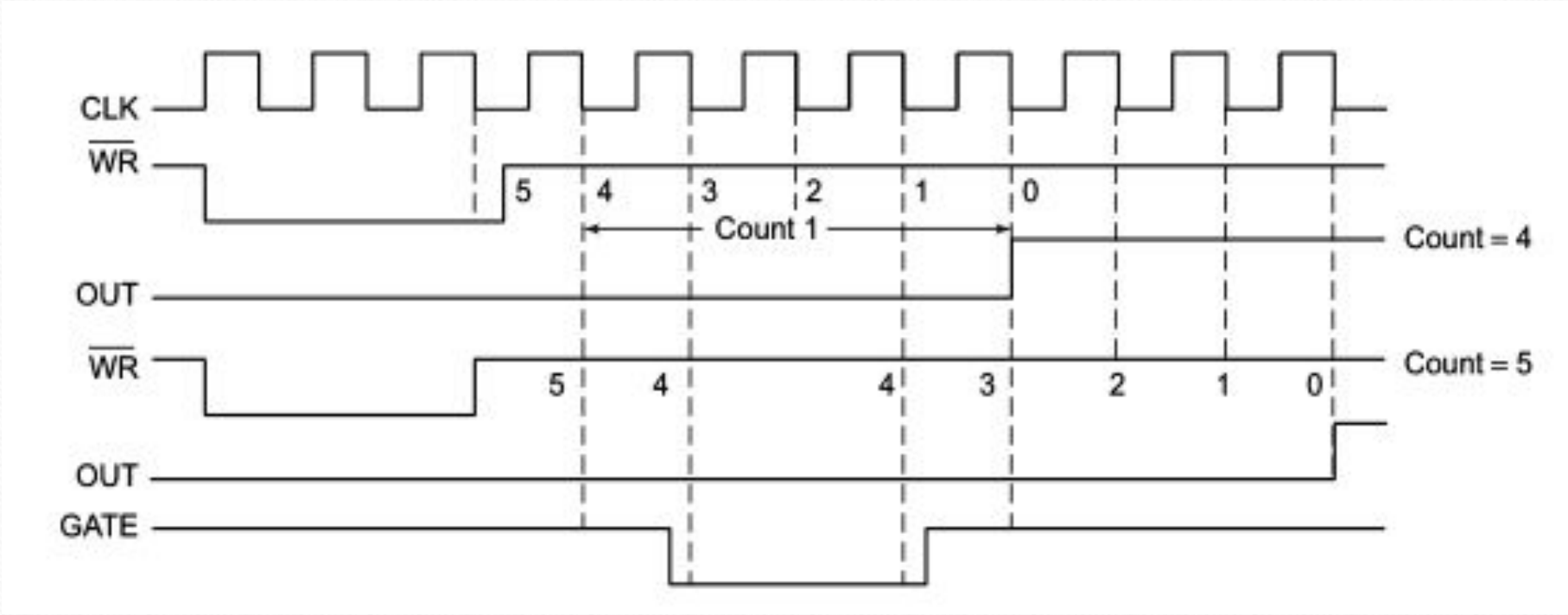
Mode 0: Interrupt on Terminal Count

- It is used to generate an interrupt to the microprocessor after a certain interval.
- Initially the output is low after the mode is set. The output remains LOW after the count value is loaded into the counter.
- The process of decrementing the counter continues till the terminal count is reached, i.e., the count become zero and the output goes HIGH and will remain high until it reloads a new count.
- The GATE signal is high for normal counting. When GATE goes low, counting is terminated and the current count is latched till the GATE goes high again.

Mode 0: Interrupt on Terminal Count

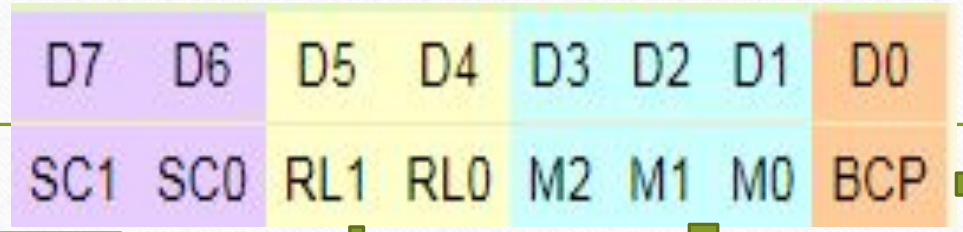


Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to interrupt the microprocessor after 1 ms through OUT terminal of Counter-0

Address Map

	A7	A6	A5	A4	A3	A2	A1	A0	
C0	0	1	0	0	0	0	0	0	40H
C1	0	1	0	0	0	0	0	1	41H
C2	0	1	0	0	0	0	1	0	42H
C3	0	1	0	0	0	0	1	1	43H

Control word register of 8253



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Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to interrupt the microprocessor after 1 ms through OUT terminal of Counter-0

Calculations for count value:

Frequency of Counter 0: **1.5MHz**

$$T = 1/f = \frac{1}{1.5\ X\ 10^6}$$

$$\text{No. of T states required for 1ms} = \frac{1\ X\ 10^{-3}}{T} = 1\ X\ 10^{-3}\ \text{x f}$$

$$= 1\ X\ 10^{-3}\ \text{X}\ 1.5\ X\ 10^6 = 1500\ (Decimal)$$

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to interrupt the microprocessor after 1 ms through OUT terminal of Counter-0

Control word: 31H

SC1	SC0	RL1	RL0	M2	M1	M0	HEX/ BCD
0	0	1	1	0	0	0	1

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to interrupt the microprocessor after 1ms through OUT terminal of Counter-0

ALP

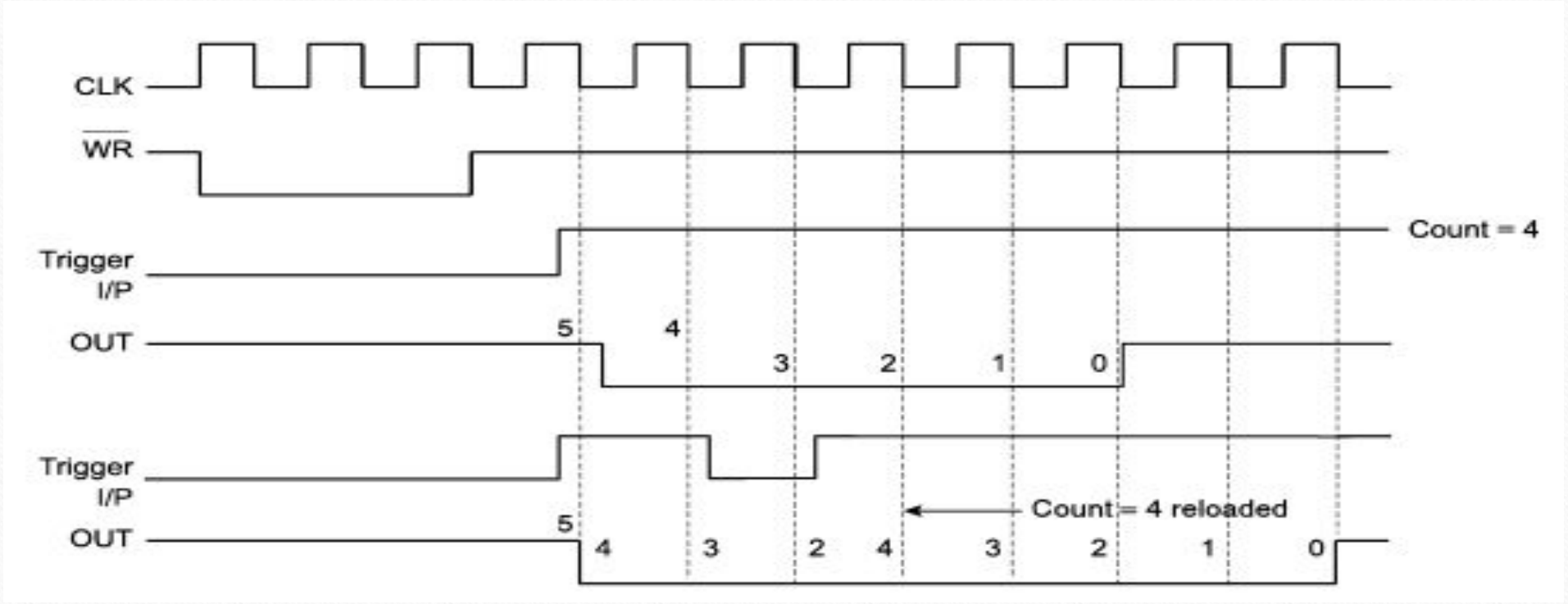
```
MVI A, 31H
OUT 43H
MVI A,00H
OUT 40H
MVI A,15H
OUT 40H
HLT
```

Interfacing diagram

Mode 1: Programmable One Shot

- It can be used as a mono stable multi-vibrator.
- The gate input is used as a trigger input in this mode.
- The output remains high until the count is loaded and a trigger is applied.

Mode 1: Programmable One Shot



Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive a monoshot pulse of duration 10 ms through OUT terminal of Counter-1

Address Map

	A7	A6	A5	A4	A3	A2	A1	A0	
C0	0	1	0	0	0	0	0	0	40H
C1	0	1	0	0	0	0	0	1	41H
C2	0	1	0	0	0	0	1	0	42H
C3	0	1	0	0	0	0	1	1	43H

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive a monoshot pulse of duration 10 ms through OUT terminal of Counter-1

Calculations for count value:

Frequency of Counter 1: **1.5MHz**

$$T = 1/f = \frac{1}{1.5\ X\ 10^{6}}$$

$$\text{No. of T states required for 10 ms} = \frac{5\ X\ 10^{-3}}{T} = 10\ X\ 10^{-3}\ \text{x f}$$

$$= 10\ X\ 10^{-3}\ \text{X}\ 1.5\ X\ 10^{6} = 15000\ (Decimal) = 3A98H$$

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive a monoshot pulse of duration 10 ms through OUT terminal of Counter-1

Control word: 72H

SC1	SC0	RL1	RL0	M2	M1	M0	HEX/ BCD
0	1	1	1	0	0	1	0

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive a monoshot pulse of duration 10 ms through OUT terminal of Counter-1

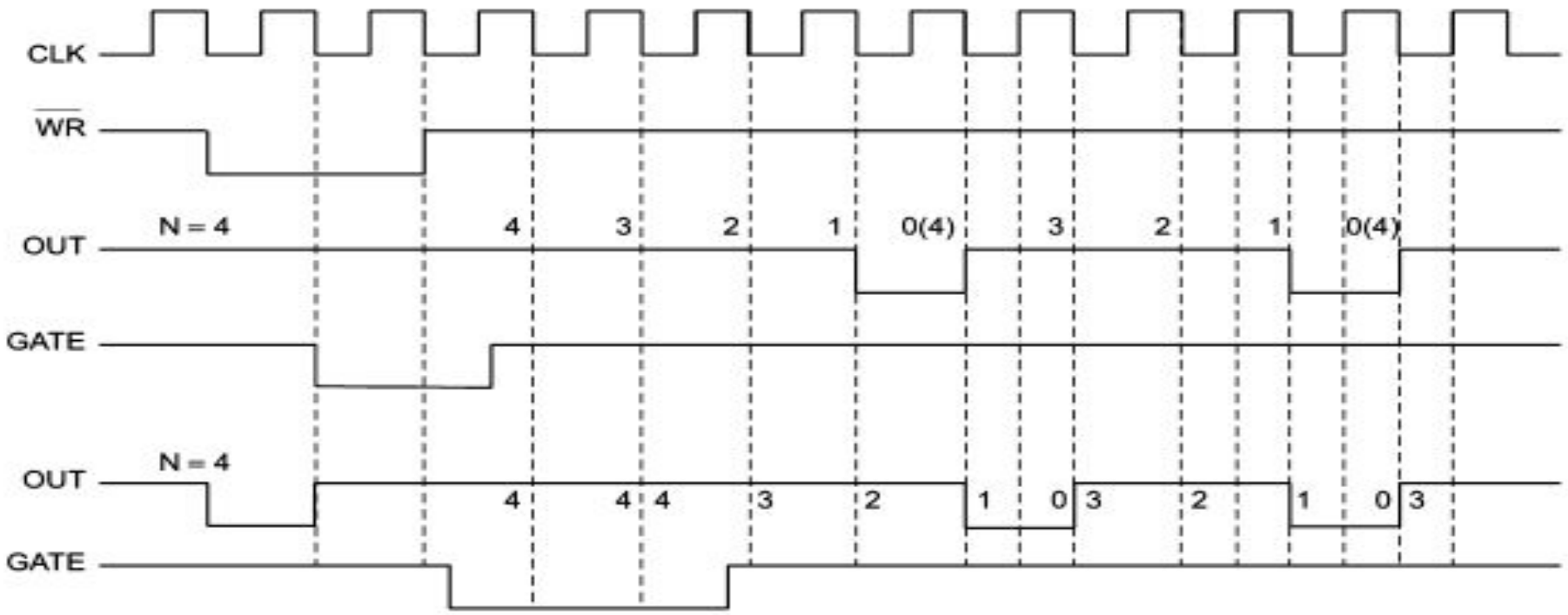
ALP

```
MVI A, 72H
OUT 43H
MVI A,98H
OUT 41H
MVI A,3AH
OUT 41H
HLT
```

Mode 2 : Rate Generator

- The output is normally high after initialization.
- Whenever the count becomes zero, another low pulse is generated at the output and the counter will be reloaded.

Mode 2 : Rate Generator



Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive pulses after every 5 ms through OUT terminal of Counter-2

Address Map

	A7	A6	A5	A4	A3	A2	A1	A0	
C0	0	1	0	0	0	0	0	0	40H
C1	0	1	0	0	0	0	0	1	41H
C2	0	1	0	0	0	0	1	0	42H
C3	0	1	0	0	0	0	1	1	43H

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive pulses after every 5 ms through OUT terminal of Counter-2

Calculations for count value:

Frequency of Counter 2: **1.5MHz**

$$T = 1/f = \frac{1}{1.5\,X\,10^{6}}$$

$$\text{No. of T states required for 5 ms} = \frac{1\,X\,10^{-3}}{T} = 5\,X\,10^{-3} \text{ x f}$$

$$= 5\,X\,10^{-3}\,\text{X}\,1.5\,X\,10^{6} = 7500(Decimal) = 1D4CH$$

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive pulses after every 5 ms through OUT terminal of Counter-2

Control word: B4H

SC1	SC0	RL1	RL0	M2	M1	M0	HEX/ BCD
1	0	1	1	0	1	0	0

Problem Statement: Interface 8085 with 8253 at an address 40H (Counter-0). Operating speeds of the processor and Timer Counter IC 8253 are 3MHz and 1.5MHz respectively. Write a program to derive pulses after every 5 ms through OUT terminal of Counter-2

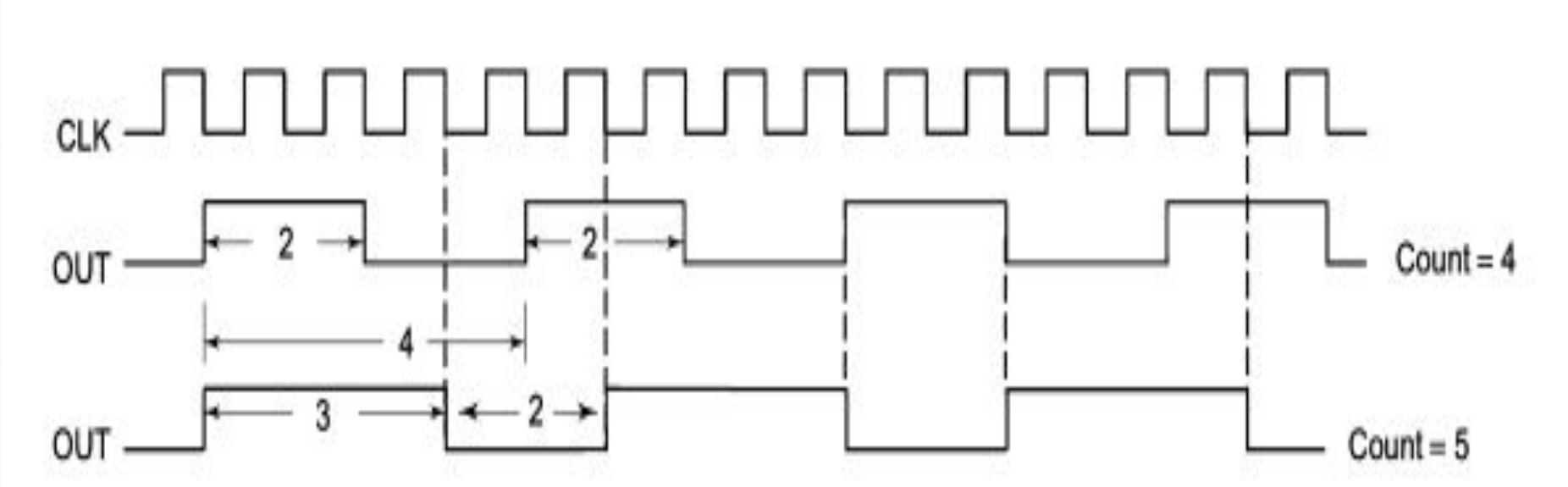
ALP

```
MVI A, B4H
OUT 43H
MVI A,4CH
OUT 42H
MVI A,1DH
OUT 42H
HLT
```

Mode 3 : Square Wave Generator

- This mode is similar to Mode 2 except the output remains low for half of the timer period and high for the other half of the period.

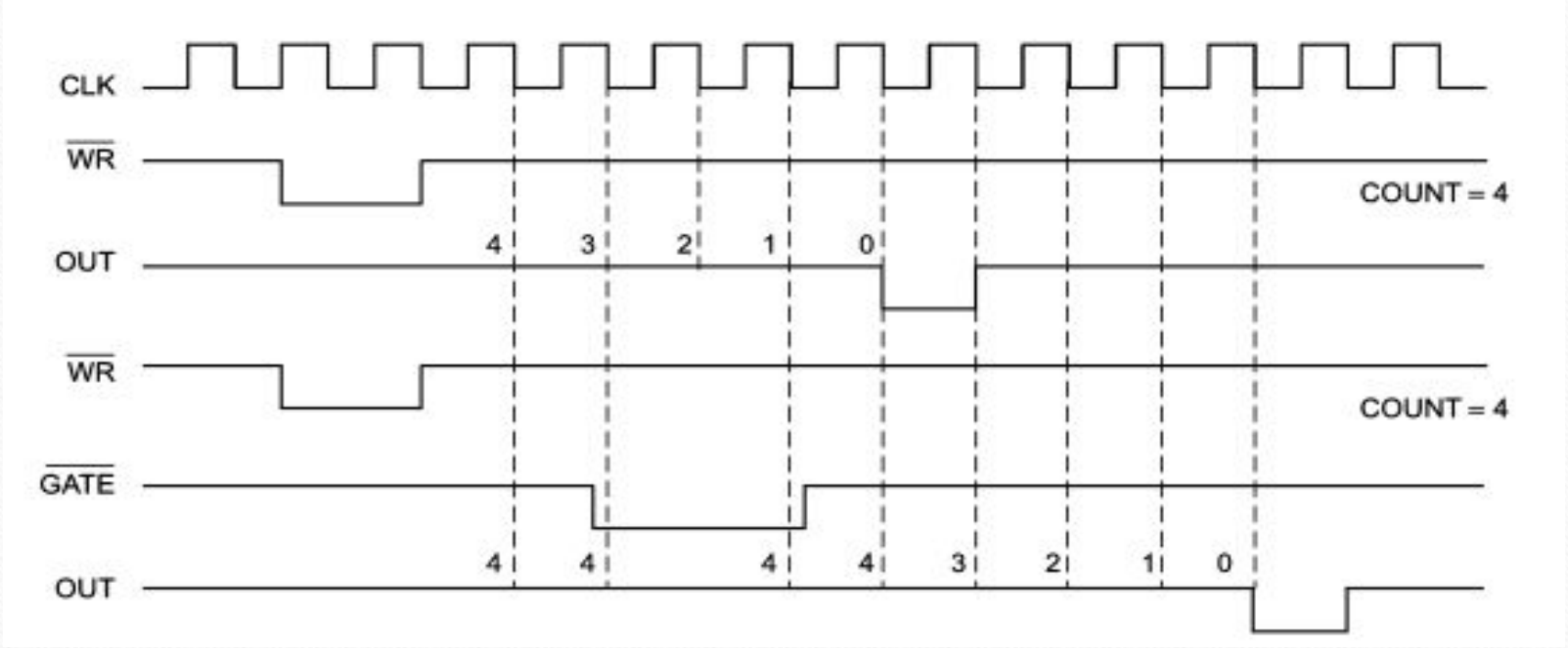
Mode 3 : Square Wave Generator



Mode 4 : Software Triggered Mode

- In this mode, the output will remain high until the timer has counted to zero, at which point the output will pulse low and then go high again.
- The count is latched when the GATE signal goes LOW.
- On the terminal count, the output goes low for one clock cycle then goes HIGH. This low pulse can be used as a strobe.

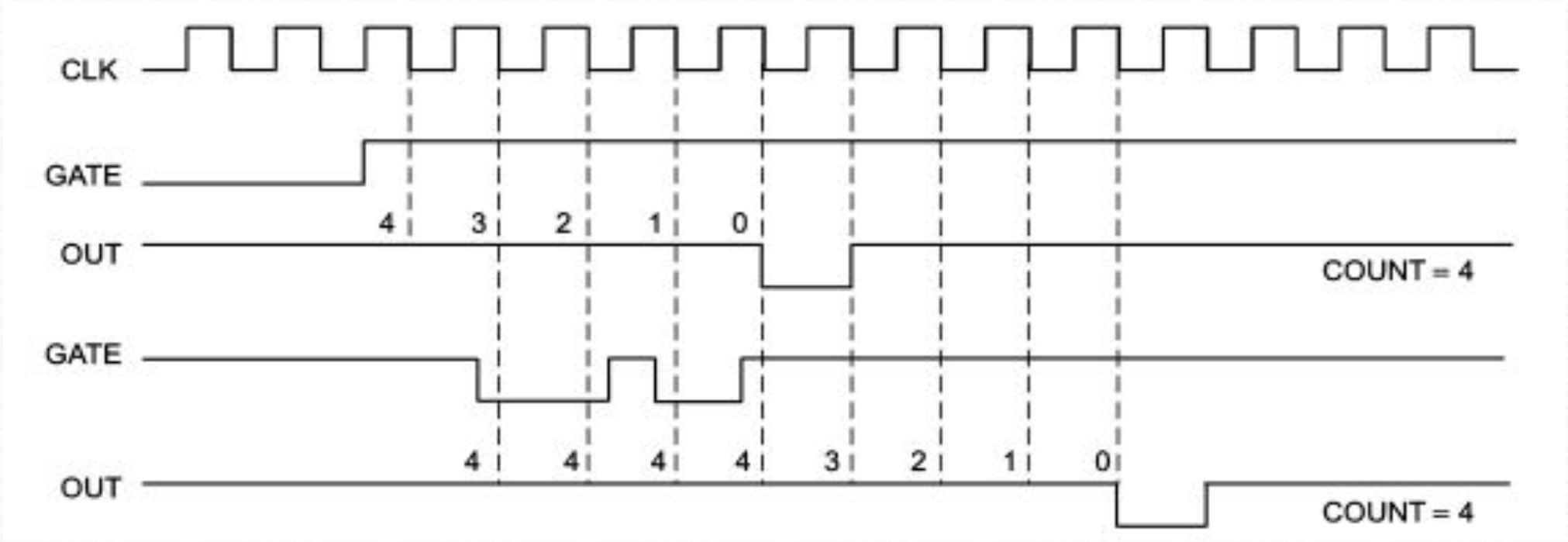
Mode 4 : Software Triggered Mode



Mode 5 : Hardware Triggered Mode

- This mode generates a strobe in response to an externally generated signal.
- This mode is similar to mode 4 except that the counting is initiated by a signal at the gate input, which means it is hardware triggered instead of software triggered.
- After it is initialized, the output goes high.
- When the terminal count is reached, the output goes low for one clock cycle.

Mode 5 : Hardware Triggered Mode




Thank
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