# PWM in ARM LPC2148

# Introduction

**Pulse Width Modulation (PWM)** is a technique by which width of a pulse is varied while keeping the frequency constant.

A period of a pulse consists of an **ON** cycle (HIGH) and an **OFF** cycle (LOW). The fraction for which the signal is ON over a period is known as **duty cycle**.

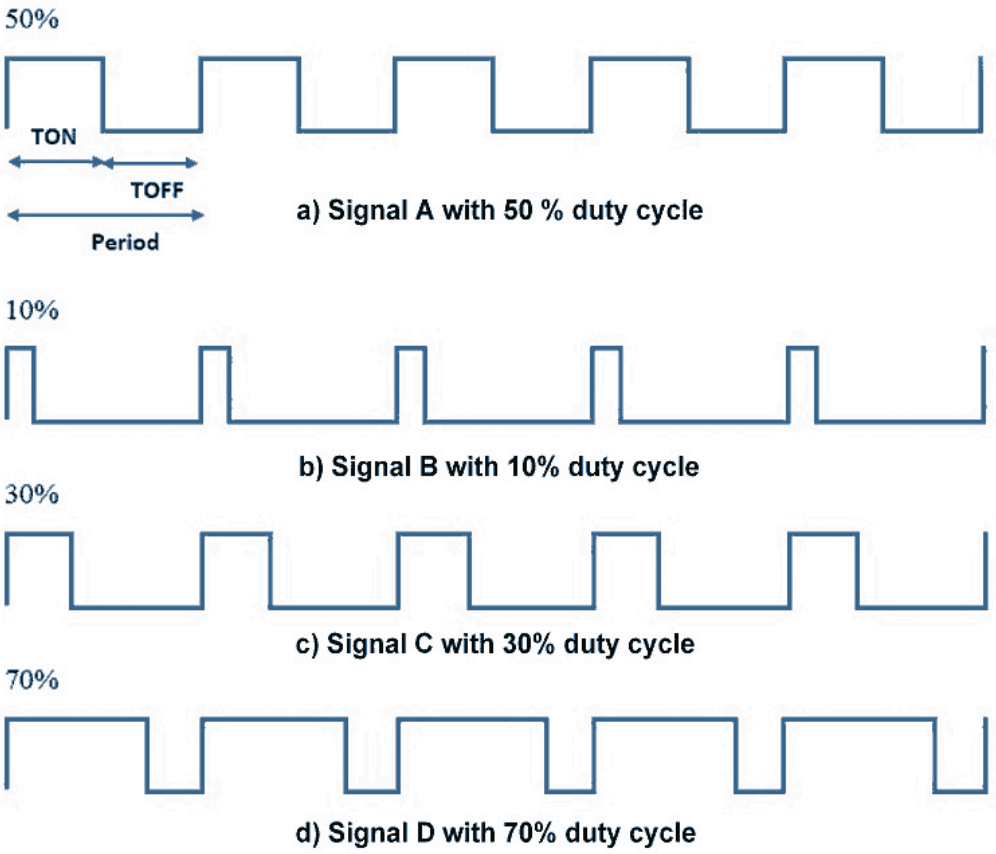
$$\text{Duty Cycle (In \%)} = \frac{Ton}{Ton + Toff} \times 100$$

E.g. Consider a pulse with a period of 10ms which remains ON (high) for 2ms.The duty cycle of this pulse will be

$$D = (2ms / 10ms) \times 100 = 20\%$$

Through PWM technique, we can control the power delivered to the load by using ON-OFF signal.

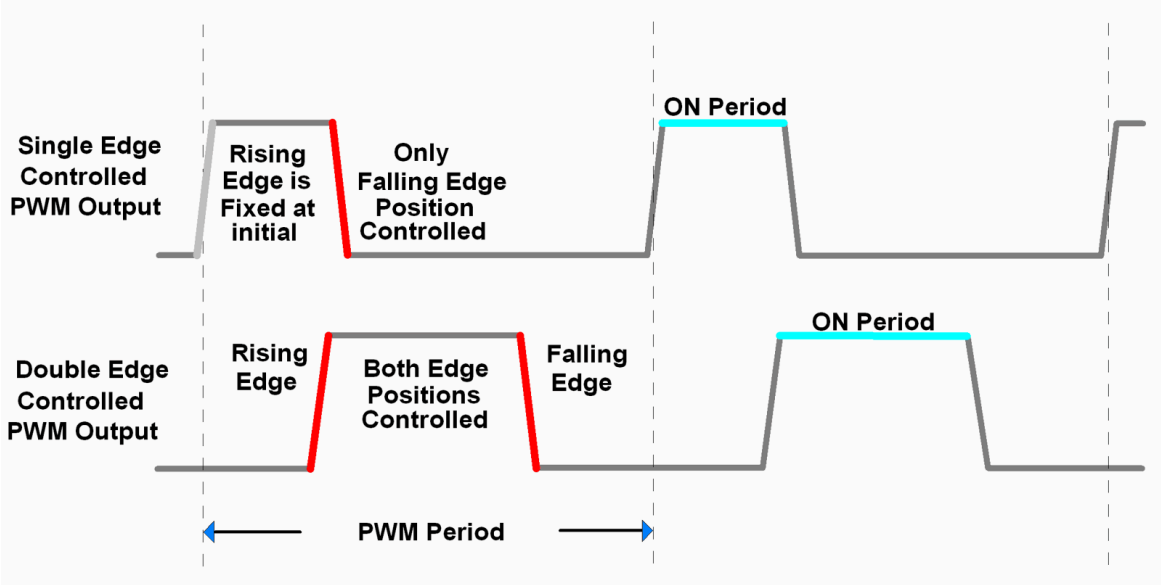
Duty cycle in pwm are shown below.




PWM Duty Cycle Waveforms

LPC2148 has PWM peripheral through which we can generate multiple PWM signals on PWM pins. Also, LPC2148 supports two types of controlled PWM outputs as,

- **Single Edge Controlled PWM Output**
  Only falling edge position can be controlled.
- **Double Edge Controlled PWM Output**
  Both Rising and Falling edge positions can be controlled.



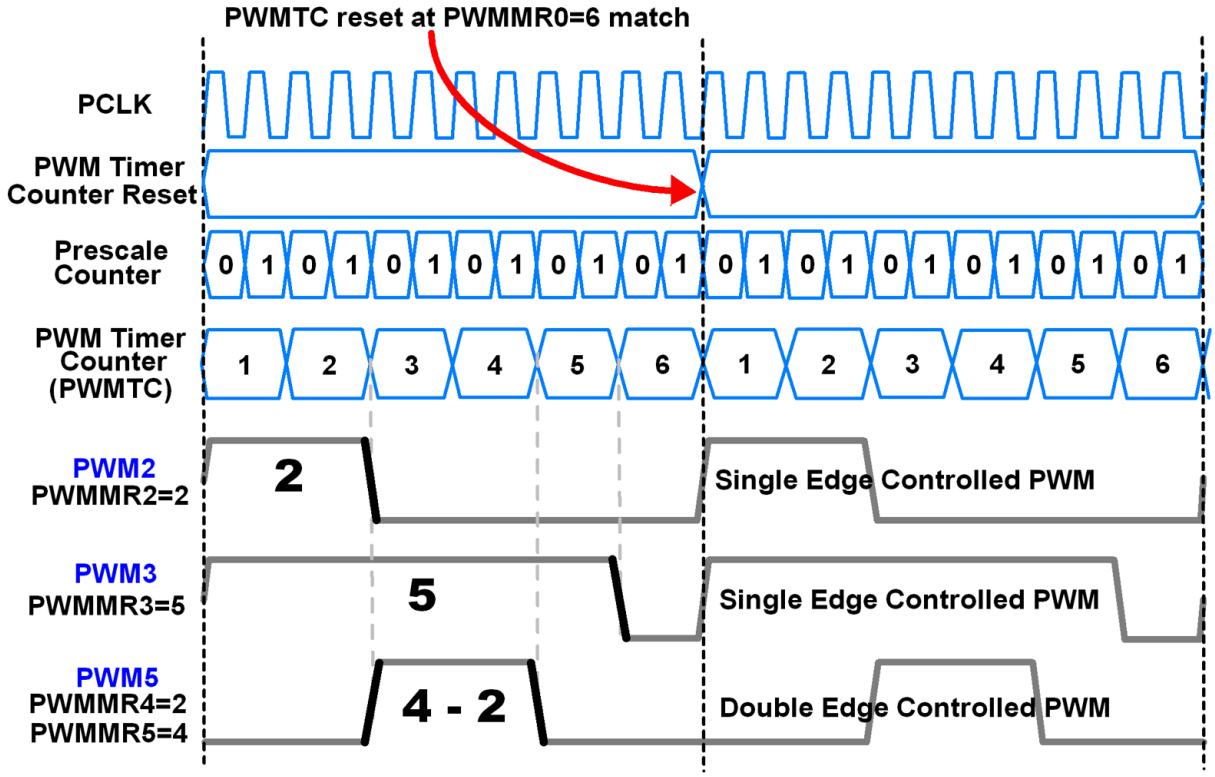

**Single Edge Controlled PWM :** All the rising (positive going) edges of the output waveform are positioned/fixed at the beginning of the PWM period. Only falling (negative going) edge position can be controlled to vary the pulse width of PWM.

**Double Edge Controlled PWM :** All the rising (positive going) and falling (negative going) edge positions can be controlled to vary the pulse width of PWM. Both the rising as well as the falling edges can be positioned anywhere in the PWM period.

# LPC2148 PWM

- The PWM in LPC2148 is based on standard 32-bit Timer Counter, i.e. PWMTC (PWM Timer Counter). This Timer Counter counts the cycles of peripheral clock (PCLK).
- Also, we can scale this timer clock counts using 32-bit PWM Prescale Register (PWMPR).
- LPC2148 has 7 PWM match registers (PWMMR0 – PWMMR06).
- One match register (PWMMR0) is used to set PWM frequency.
- Remaining 6 match registers are used to set PWM width for 6 different PWM signals in Single Edge Controlled PWM or 3 different PWM signals in Double Edge Controlled PWM.

- Whenever PWM Timer Counter (PWMTC) matches with these Match Registers then, PWM Timer Counter resets, or stops, or generates match interrupt, depending upon settings in PWM Match Control Register(PWMMCR).




As shown in above figure, PWMMR0 = 6 i.e. PWM period is 6 counts, after which PWM Timer Counter resets.

PWM2 & PWM3 are configured as Single Edge Controlled PWM and PWM5 is configured as Double Edge Controlled PWM.

Prescaler is set to increment PWM Timer Counter after every two Peripheral clocks (PCLK).

Match registers (PWMMR2 & PWMMR3) are used to set falling edge position for PWM2 & PWM3.

PWMMR4 & PWMMR5 are used to set rising & falling edge positions respectively for PWM5.

Let's see the different PWM that can be generated using LPC2148

The table given below shows when the PWM is Set (Rising Edge) and Reset (Falling Edge) for different PWM channels using 7 Match Register.

| PWM Channel | Single Edge Controlled | | Double Edge Controlled | |
|---|---|---|---|---|
| | **Set by** | **Reset by** | **Set by** | **Reset by** |
| 1 | Match 0 | Match 1 | Match 0 | Match 1 |
| 2 | Match 0 | Match 2 | Match 1 | Match 2 |
| 3 | Match 0 | Match 3 | Match 2 | Match 3 |
| 4 | Match 0 | Match 4 | Match 3 | Match 4 |
| 5 | Match 0 | Match 5 | Match 4 | Match 5 |
| 6 | Match 0 | Match 6 | Match 5 | Match 6 |