M Yashwanth
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Education:

PhD Student in Computational and Data Sciences (CDS) (2021- present)
Indian Institute of Science (IISc), Bangalore (India)
(GPA – 9/10)

Master of Engineering in Signal Processing (2009-2011**)**
Indian Institute of Science (IISc), Bangalore (India)
(GPA - 6.2/8)

Bachelor of Technology in Electronics and Communications (2005-2009)
Mahatma Gandhi Institute of Technology, Hyderabad (India)
(Percentage – 75%)

Publications:

- M Yashwanth, K.V.S. Hari, "Delay Optimized Zero-Forcing Channel Shortening Algorithm for Wireless Communication," in Proceedings of International Conference on Signal Processing and Communication (SPCOM 2012), July 2012, Bangalore, India.

Patents (under publication):

- Null-Space-Projection-Based Channel Decomposition for Beam forming
  https://patents.justia.com/patent/20200274592

Achievements:

- Secured All India 9th rank in ECE in Graduate Aptitude Test for Engineering GATE-2009.

Professional Summary:

Cadence Design Systems (Principal Product Engineer) (May 2019- July 2021):

- Prediction of delays using Neural networks, Random Forest etc.
- Modelling Mathematical equations with LSTM based encoder-decoder model and using the learned representation to predict delays.

Qualcomm (PHY Modelling/Systems Engineer) (Feb 2014- May 2019)

- Involved in the Algorithm development and modelling of 802.11ax standard.
- Worked on Radar detection LLR tuning in the presence of DC and CFO, transmit beam forming.
- Worked on Rx decoding algorithms.

IKANOS (DSP Firmware Engineer) (Jan 2012 -Feb 2014)

- Worked on Notch filter canceller for minimizing the RFI interference.
- Worked on adaptive hybrid to minimize the Tx echo into the Rx.
- Enhancing the symbol boundary detection algorithm.

REDPINE SIGNALS (Baseband Design Engineer from July 2011 to Dec 2011)

- Implementing the 11ac transmitter in the MATLAB.