**Chapter # 7 Exercise**

**7.11**

Suppose that the instruction format for a modified Little Man Computer requires two consecutive locations for each instruction. The high-order digits of the instruction are located in the first mail slot, followed by the low –order digits. The IR is large enough to hold the entire instruction and can be addressed as IR [high] and [IR] low to load it. You may assume that the op code part of the instruction uses IR [high] and that the address is found in IR [low]. Write the fetch-execute cycle for an ADD instruction on this machine.

**Answer-**

the F-E cycle for an ADD instruction in this machine can be displayed as

PC  MAR

MDR  IR [high]

PC + 1  PC\_\_\_\_ fetch

PC MAR

MDR  IR [low]

IR [low]  MAR

A + MDR A

PC + 1  PC

the PC is incremented twice by this instruction.

**7.12**

The Little Prince Computer (LPC) is a mutant variation on the LMC. The LPC is so named because the differences are a royal plan). The LPC has one additional instruction. The extra instruction requires two consecutive words:

0XX

0YY

This instruction, known as move, moves data directly from location XX to location YY without affecting the value in the accumulator. To execute this instruction, the Little Prince would need to store the XX data temporarily. He can do this by writing the value on a piece of paper and holding it until he retrieves the second address. The equivalent in a real CPU might be called the intermediate address register, or IAR. Write the fetch-execute cycle for the LPC *MOVE* instruction.

**Answer-**

There are five basic steps involved in the process;

a. Fetch instruction

b. Retrieve data from memory location XX

c. Save the retrieved data in IAR

d. Fetch the next location to get address YY

e. Store the data from IAR to address YY

PC  MAR

Step 1- MDR  IR

Step 2- IR [add]  MAR

Step 3- MDR  IAR

PC + 1  PC

PC  MAR

Step4- MDR  IR

IR [add]  MAR

Step 5- IAR MDR

PC + 1  PC