मोतीलालनेहरूराष्ट्रीयप्रौद्योगिकीसंस्थानइलाहाबाद
प्रयागराज-211004 (भारत)
Motilal Nehru National Institute of Technology Allahabad
Prayagraj - 211 004 (India)

Department of Computer Science & Engineering
Mid Semester Examination, Session 2024-25 (Even)

Programme: B.Tech. Minor (CSE) **Branch:** Other than CSE **Semester:** VI
Course Name: Computer Organization
Course Code: CSN11102 **Max. Marks:** 25
Time: 1.5 Hours **Registration No.:** □□□□□□□□□

Instructions:
Attempt all questions. All parts of a question should be answered in one attempt SEQUENTIALLY.

Marks

Q1 **(a)** Consider the following assembly language program for a hypothetical processor. A, B, and C are 8 bit registers. The meanings of various instructions are shown as comments. **2+3 [CO1, CO2]**

```
        MOV B, # 0      ;  B ← 0                B-0
        MOV C, # 8      ;  C ← 8                C=8        1000
Z :     CMP C, # 0      ;  compare C with 0                0111
        JZX             ;  jump to X if zero flag is set
        SUB C, # 1      ;  C ← C - 1            C-7
        RRC A, # 1      ;  right rotate A through carry by one bit. Thus:
                        ;  if the initial values of A and the carry flag are a7...a0 and
                        ;  c0 respectively, their values after the execution of this      right shift
                        ;  instruction will be c0a7...a1 and a0 respectively.
        JC Y            ;  jump to Y if carry flag is set
        JMP Z           ;  jump to Z
Y :     ADD B, # 1      ;  B ← B + 1
        JMP Z           ;  jump to Z
X :
```

If initial value of register A is A_0, the value of register B after the program execution:

i. the number of 0 bits in A_0
ii.✓ the number of 1 bits in A_0
iii. A_0
iv. 8

(b) Consider two 8085 memory locations 2000H and 2001H which contain two 8-bit numbers. Write an assembly language program using 8085 instruction set to multiply these numbers and store the product at the subsequent memory locations. Also analyse the case where either any or both the multiplicand and multipliers are zero. In such case store 0000H at the respective locations.

Q2 **(a)** Draw the hardware implementation of Partial Sum approach for multiplying binary integers in signed magnitude representation. **2+3 [CO2**

(b) Using Booth algorithm write down the step-by-step multiplication of the following: (−5)×(−3)= +15

Q3 **(a)** Trace the digital circuit for 4-bit binary adder–subtractor. Write under what condition it will be an adder and in what condition it will work as a subtractor circuit.

(b) Draw and explain the block diagram of a 4-bit carry look ahead adder.

2+3 [CO2]

Q4 **(a)** Convert $(4D3C)_{H}$ into equivalent binary number in 32 bit (single precision) IEEE-754 format.

(B) Consider the following code segment where B1 and B2 are branch instructions.

```
     a = 0;
     while (a < 1000) {
B1       if (a % 2 == 0) { ... }
         a++;

         ...
B2       if (b == 0) { ... }
     }
```

Assume that variable b is initialized to a non-zero value and there is no instruction in the while loop that modifies the value of b. Write down actual outcome sequence (10 sequences) for both branch instructions B1 and B2, respectively using symbols **T:** *branch taken* and **N:** *branch not taken.* Also determine the accuracy percentage of branch prediction with the help of a two- bit branch predictor for both B1 and B2, respectively.

2+3 [CO3, CO4]

Q5 **(a)** Consider a pipeline processor with 4 stages S1 to S4 to execute the following loop:

```
for (i = 1; i <= 1000; i++) { I1, I2, I3, I4 }
```

Time taken (nanoseconds) by instructions I1 to I4 for stages S1 to S4 are given below:

	S1	S2	S3	S4
I1	1	2	1	2
I2	2	1	2	1
I3	1	1	2	1
I4	2	1	2	1

The output of I1 for i = 3 will be available after how many nanoseconds?

(b) An instruction pipeline has 5 stages and each stage takes 2 nanoseconds and all instructions use all 5 stages. Branch instructions are not overlapped, i.e., the instruction after the branch is not fetched till the branch instruction is completed. Under ideal conditions:

(i) Calculate the average instruction execution time assuming that 20% of all instructions executed are branch instructions. Ignore the fact that some branch instructions may be conditional.

(ii) If a branch instruction is a conditional branch instruction, the branch need not be taken. If the branch is not taken, the following instructions can be overlapped. When 80% of all branch instructions are conditional branch instructions, and 50% of the conditional branch instructions are such that the branch is taken, calculate the average instruction execution time.

2+3 [CO4]

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Department of Computer Science & Engineering
End Semester, Session 2024-25 (Even)

Programme: B.Tech. Minor (CSE) **Branch:** Other than CSE **Semester:** VI
Course Name: Computer Organization
Course Code: CSN14001 **Max. Marks:** 50
Time: 2.5 hours **Registration No.:** 2 0 2 2 2 0 6 8

Instructions:

1. Attempt all questions. All parts of a question should be answered in one attempt SEQUENTIALLY.

Marks

Q1 **(a)** Convert $(14.125)_d$ into 32 bit (single precision) IEEE-754 format where suffix **d** denotes decimal number format. 3+1+4+2

(b) Write down the extreme case of NaN and DeNormal Number, respectively.

(c) Consider the following instruction sequence where registers R1,R2, and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.

Instruction	**Semantics**	**Instruction Size** (bytes)
MOV R1, (5000)	R1 ← MEMORY[5000]	4
MOV R2, (R3)	R2 ← MEMORY[R3]	4
ADDR2, R1	R2 ← R1 + R2	2
MOV (R3), R2	MEMORY[R3] ← R2	4
INC R3	R3 ← R3 + 1	2
DEC R1	R1 ← R1 − 1	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 30, and the content of the register R3 is 4000. The content of each of the memory locations from 4000 to 4010 is 45. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable. After the execution of the program, the content of memory location 4010 is ________ **(explain the logic).**

(d) Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 150 instructions, the amount of memory (in bytes) consumed by the program text is ________ **(show the calculation).**

Q2 **(a)** Consider a pipelined processor with 5 stages, Instruction Fetch(IF), Instruction Decode(ID), Execute (EX), Memory Access (MEM), and Write Back (WB). Each stage of the pipeline, except the EX stage, takes one cycle. Assume that the ID stage merely decodes the instruction and the register read is performed in the EX stage. The EX stage takes one cycle for ADD instruction and the register read is performed in the EX stage, The EX stage takes one cycle for ADD instruction and two cycles for MUL instruction. Ignore pipeline register latencies. Consider the following sequence of 8 instructions: 4+4+2

Please Turn Over

ADD, MUL, ADD, MUL, ADD, MUL, ADD, MUL

Assume that every MUL instruction is data-dependent on the ADD instruction just before it and every ADD instruction (except the first ADD) is data-dependent on the MUL instruction just before it. The speedup defined as follows.

$$Speedup = \frac{\text{Execution time without operand forwarding}}{\text{Execution time with operand forearding}}$$

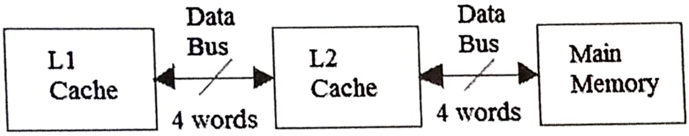
The Speedup achieved in executing the given instruction sequence on the pipelined processor (rounded to 2 decimal places) is ____________

(b) A five−stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 3 clock cycles for MUL instruction and 6 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?

Instruction	Meaning of instruction
t_0: MUL R_2, R_0, R_1	$R_2 \leftarrow R_0 * R_1$
t_1: DIV R_5, R_3, R_4	$R_5 \leftarrow R_3 / R_4$
t_2: ADD R_2, R_5, R_2	$R_2 \leftarrow R_5 + R_2$
t_3 : SUB R_5, R_2, R_6	$R_5 \leftarrow R_2 - R_6$

(c) Explain how the prediction accuracy of a single-bit dynamic branch predictor can be improved with the help of double-bit predictor?

Q3 A computer system has an L1 cache and an L2 cache, and a main memory unit connected as shown below. The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1cache, L2 cache and the main memory unit, respectively. 3+3+4



(a) When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. What is the time taken (in nanoseconds) for this transfer?

(b) When there is a miss in both L1 cache and L2 cache, first a block is transferred from main memory to L2 cache, and then a block is transferred from L2 cache to L1 cache. What is the total time taken (in nanoseconds) for these transfers? [**Note:** *Questions 3(a) and 3(b) are linked.*]

(c) Consider the following table where direct mapping is used.

Main memory size	Cache memory size	Block size	Tag bits (in physical address)	Tag directory size (bits)
	512 KB	1 KB	7	
16GB		4KB	10	
32GB	32KB	1KB		
128KB	16KB	256B		

Fill up the missing values. [**Note:** *assume that memory is byte addressable*]

Q4 (a) Briefly describe the working and addressing modes of the following 8085 instructions **4+6**

load HL pair directly

(i) LHLD 16-bit address, (ii) LDAX (B/D) reg. pair, (iii) LXI, 16-bit value,
(iv) JMP 16-bit address

load accumulator value direct to register

load register pair immediate

jump

(b) Consider the following figure before the execution of an assembly program in an 8085 processor as shown below. The figure depicts the memory locations 3080H and 3081H containing the values 05 and 06, respectively. It also exhibits the initial contents of the general purpose registers along with flag register, program counter (PC) and stack pointer (SP). [**hint:** all the contents are in hexadecimal]

A	F7	43	FLAG
B	32	59	C
D	XX	XX	E
H	XX	XX	L
PC	1000		
SP	XXXX		

location	contents
3080H	05
3081H	06

```
INITIAL     EQU    0000H
STKTOP      EQU    4FFFH
            ORG    1000H
            LXI    SP, STKTOP
            PUSH   PSW
            LXI    H, INITIAL
            LXI    D, INITIAL
            LDA    3080H
            ADI    00H
            JZ     STORE
            MOV    E, A
            LDA    3081H
            ANI    FFH
            JZ     STORE
            MOV    C, A
BACK:       DAD    D
            DCR    C
            JNZ    BACK
STORE:      SHLD   3082H
            XTHL
            POP    PSW
            PCHL
            SPHL
            HLT
```

Write down the contents of the aforesaid registers (if modified by the program). Also determine the contents of the memory locations **3082H** and **3083H**. [**hint:** *MEMORY[X] denotes the content at the memory location X*]

A = ________, F = ________, B = ________, C = ________, D = ________,

E = ________, H = ________, L = ________, PC = ________, SP = ________,

MEMORY[3082H] = ________, and MEMORY[3083H] = ________

Please Turn Over

Q5 (a) Draw the hardware implementation of direct mapped cache where no. of tag bits = 2.
[**Note:** *Use multiplexer(s) and comparator(s)*].

(b) What is conflict miss in direct mapped cache?

(c) Fill the missing values in the following table. Assume that memory is byte addressable and associative mapping is used.

Main memory size	Cache memory size	Block size	Tag bits (in physical address)	Tag directory size (bits)	No. of comparators required
128KB	16 KB	256B			
32GB	32KB	1KB			
	512KB	1KB	17		
16GB		4KB	22		
64MB			10		
	512KB		7		

****************All the Best****************