

# Using history and stride for TLB prefetching

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Gitlab Link: [https://gitlab.com/yash42patel/tlb\\_prefetching.git](https://gitlab.com/yash42patel/tlb_prefetching.git)

## Summary

A large amount of execution time is spent in page table access as we have to access page table only in case of tlb miss, so if we reduce tlb miss we are going to improve execution time by a significant amount. So a lot of work has been done on tlb's and prefetching is one of those areas but there is not much that has been done in tlb prefetching as compared to cache prefetching so we are working on history based tlb prefetching which is not done and as from caches and branch prediction we get an intuition that history is repeated in that same order a large number of times.

So we have tried to analyze the same for SPEC 2006 benchmarks in gem5 and get results related to availability of patterns and how we can implement it feasibly by modifications.

## 1. Introduction

We have analysed address patterns and how our proposed scheme could be designed, so for that we analysed patterns based on history and got result which could be used in implementation and comparing with other prefetching techniques. We have analysed on last few bits and observed that how much false +ve or aliasing we are going to get but as there are design constraints so we have to choose tradeoff between wrong prefetching vs size of prediction table and register used.

So we have analysed on:

1. How much constant stride based patterns we are getting.
2. How much frequency of  $n$  consecutive accesses we get, means how much association of history is there in benchmarks.

Report is organized further as, In section 2. we have shown background and related work and how they have done. then we explained in section 3. that what are motivations behind our design and then in further remaining sections we have explained what we have done and what else can be done in future and what we are going to get out of it.

## 2. Background and Related Work

Address translation, done with virtualization and on larger application working sets is a major source of performance degradation. Many aspects of TLB, namely its structure, lookup etc have gone through rigorous studies but most of the sophisticated techniques to boost TLB performance use TLB prefetching, focuses on pre-fetching the next page in TLB before it is actually called for on the basis of certain patterns or strides. This section gives brief overview of different TLB pre-fetching studies to provide deeper insight into TLB prefetching.

**2.1. Recency based TLB pre-fetching:-** [1] This technique exploits the temporal locality of TLB access such that a single LRU stack is maintained to store the temporal ordering of page accesses. This LRU stack, made up of doubly linked list, which stores a translation table entry consisting of two extra pointers, namely prev and next is used to predict the next pre-fetched entry.

**2.2. Going the distance for TLB pre-fetching:-** [2] an application driven study:- Distance prefetching works on the fact that markov and recency based prefetching takes more space for recording the pattern in reference behaviour and give a solution which does the same thing in a smaller space. It keeps tracks of the strides between successive references to make predictions which is helpful in case of spatial locality.

**2.3. Inter core co-operative TLB pre-fetchers for chip multi-processors :-** [3] Inter-core cooperative pre-fetchers are developed to exploit commonality in TLB miss patterns across multiple cores. This method can collectively improve 19% to 90% data TLB misses across the workloads.

**2.4. Data cache prefetching using global history:-** [4]prefetching with global history buffer improves performance of cache and increases correlation prefetching performance by almost 20% and improves performance of stride prefetcher by 6%.

### 3. Motivation

As specified earlier also tlb is a major part of memory system of cpu as inclusion of tlb's save lot of page translation time on which on average 40% of execution time is spent [2]. So even a small improvement in tlb hit rate is going to improve performance of system a lot.

And second thing is why we are trying to do history based prefetching is as few techniques using history are implemented in the data caches like [4] and have provided significant improvement in tlb and overall performance. So we are trying to use this history type or a pattern which is likely to occur together every time.

### 4. Project Work :-

#### 4.1. System specifications :

We have used gem5 simulator to get a simulation environment to run our workloads and to make changes in tlb configuration to analyse behavior of tlb on various changes. We worked on x86 64 bit in gem5. And our analysis was on **SPEC 2006 benchmark suite**, in SPEC 2006 suite we ran a few benchmarks like bzip, MCF, sjeng, spec\_rand 998 and 999. and other than those specified above we have ran few other but either they are not giving enough data in significant time or they seemed not correct to us so we have done our whole analysis on these 5.

#### 4.2. Methodology :

Our approach is to record and analyse the patterns in the reference behavior.

Reference behavior can also be viewed broadly under one of these categories:

- (a) showing regular/strided accesses to several data items that are touched only once
- (b) showing regular/strided accesses to several data items that are touched several times
- (c) showing regular/strided accesses to several data items, but the stride itself can change over time for the same data item

Not having constant strided accesses (either keeps changing constantly or there is no regularity in the stride at all), but repeating the same irregularity from one access to another for the same data item over time.

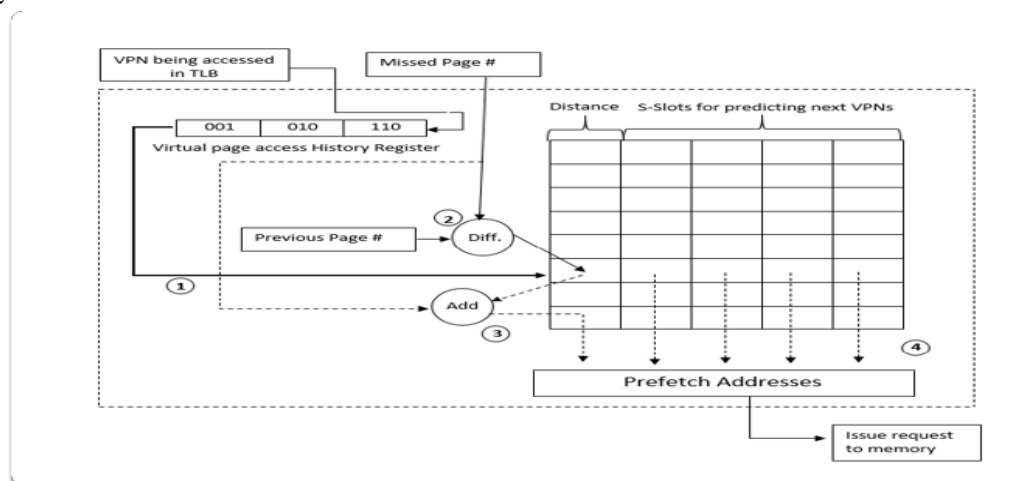


Figure: 4.1 Design of proposed TLB prefetch logic

In this design we exploit temporal locality along with the previous-stride to pre-fetch TLB entries. For this, a pre-fetch logic (Figure. 4.1) is designed consisting of a 'virtual page access history register' in which the history of previous k-addresses, accessed in TLB is stored (as a few bits of the virtual page number (VPN)). This register indexes the entry of the prediction table. Prediction table contains two parts, first one takes the distance between the missed VPN in TLB and the previously accessed VPN (first of the s+1 slots), whereas the other part contains 's' slots with the VPNs that will be prefetched. Pre-fetching would include, the page numbers from these s-slots and one VPN that is calculated by adding the stride (stored in first slot) with the missed page number. Thus, this technique makes use of both the temporal and spatial locality of the TLB references for better TLB prefetching. In addition to it the Page Access History Register is updated at every new TLB reference by working analogously to a shift register with new entry being stored and oldest entry being discarded. In this we keep four prediction to be prefetched on a miss and they are going to be kept in buffer based on frequency of occurrence means if that particular sequence occurs frequently or not otherwise it's going to affect frequency of prediction a lot.

### 4.3 Approach :

Above specified is overview of how our implementation is going to work. for that we need to do profiling of patterns observed on various benchmarks

On basis of stride and history.

We have plotted results for various benchmark bzip , mcf , sjeng , spec\_rand\_998 , spec\_rand\_99

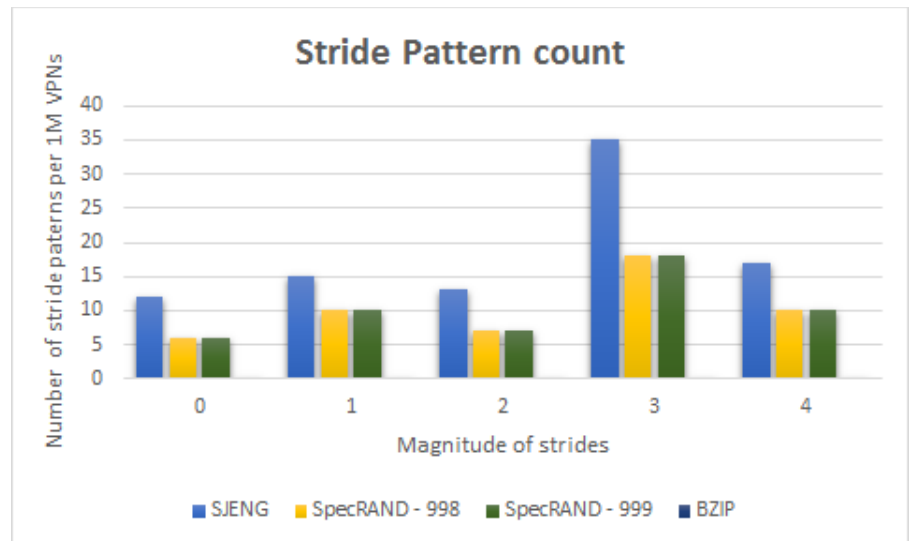
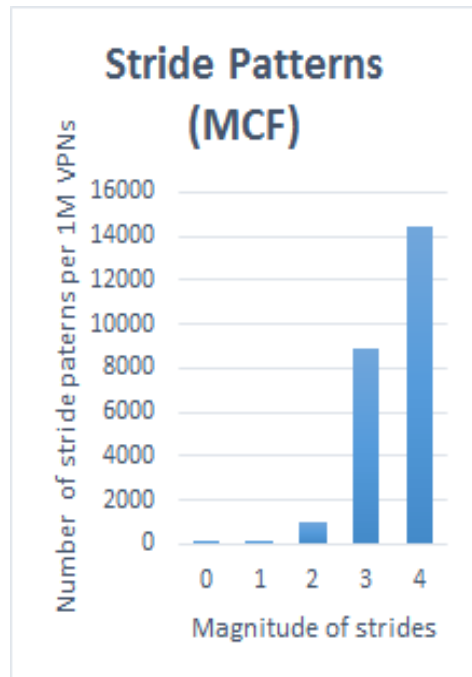
### 4.4 Experimental procedure:

- **for patterns based on strides :** we are calculating total number of constant stride based pattern of different strides like length of stride and what stride is like 0,1,2,3. We have done all of this for 10 crore instructions in every benchmark if there are  $\geq 10$  crore among our selected benchmarks. As this is simple technique so we are trying to analyse that could it be useful if used along with history in our design.
- **for patterns based on history of page access:-** to find repetition of history or say same set of VPN in particular sequence we are trying to find repetition of history locally, means in set of 20K instruction and we are analysing for 1 million tlb access as algorithm used by us has an  $n^2$  complexity and it takes lot of time for even this 1 million instructions.

Initially we are calculating actual repetition of sequence of VPN means using full page numbers but this is not feasible in designing as prediction table would be going to be very large than then again issue of size and latency of access of prediction table is going to affect performance so we are using few last bits of VPN to predict and prefetch. Because of this aliasing is going to be introduced so we select a trade off between size and false prediction on how many bits to be used for prediction so we have done how much wrong prediction increases as less no of bits are used.

### 4.5 Experimental results and evaluation :

**In case of stride based patterns** we do not have significant +ve results as we are using simple constant stride based prefetcher so that might be the reason. In this case we are only getting a lot of constant strides in MCF about 14000 strides of only length 4 so that's significant but in rest of benchmark we have got very few strides means in 10 crores of access we have got only 10's of strides. So this seems like it would not be going to add anything to performance when used along with history based prefetching.

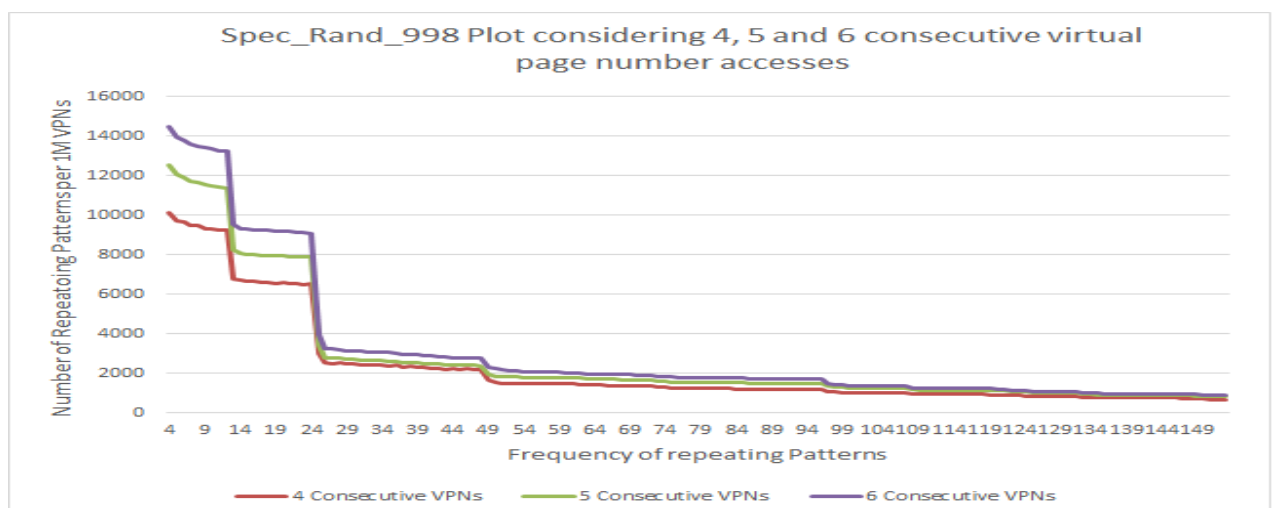


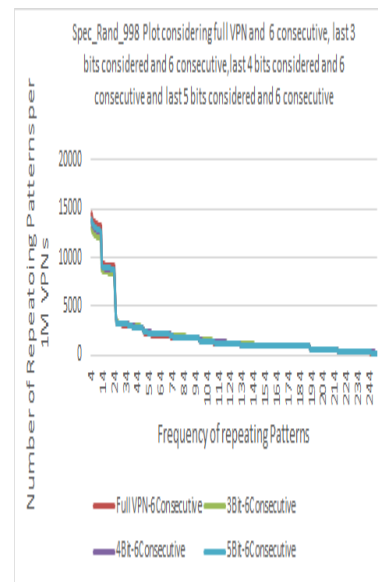
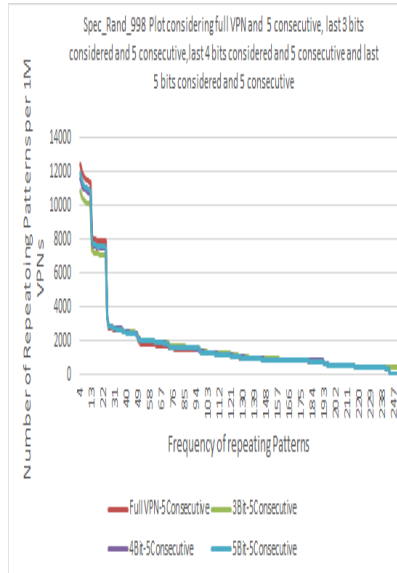
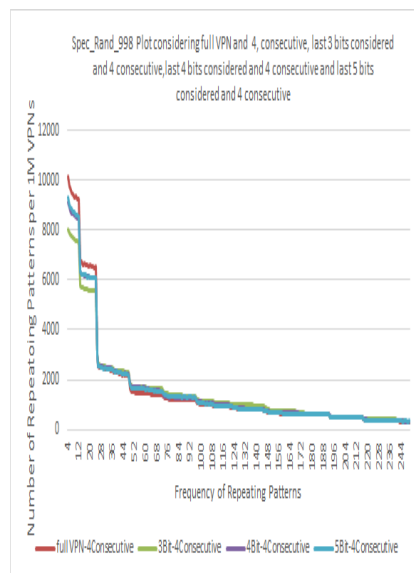
Graph for stride based analysis

#### OBSERVATIONS:-

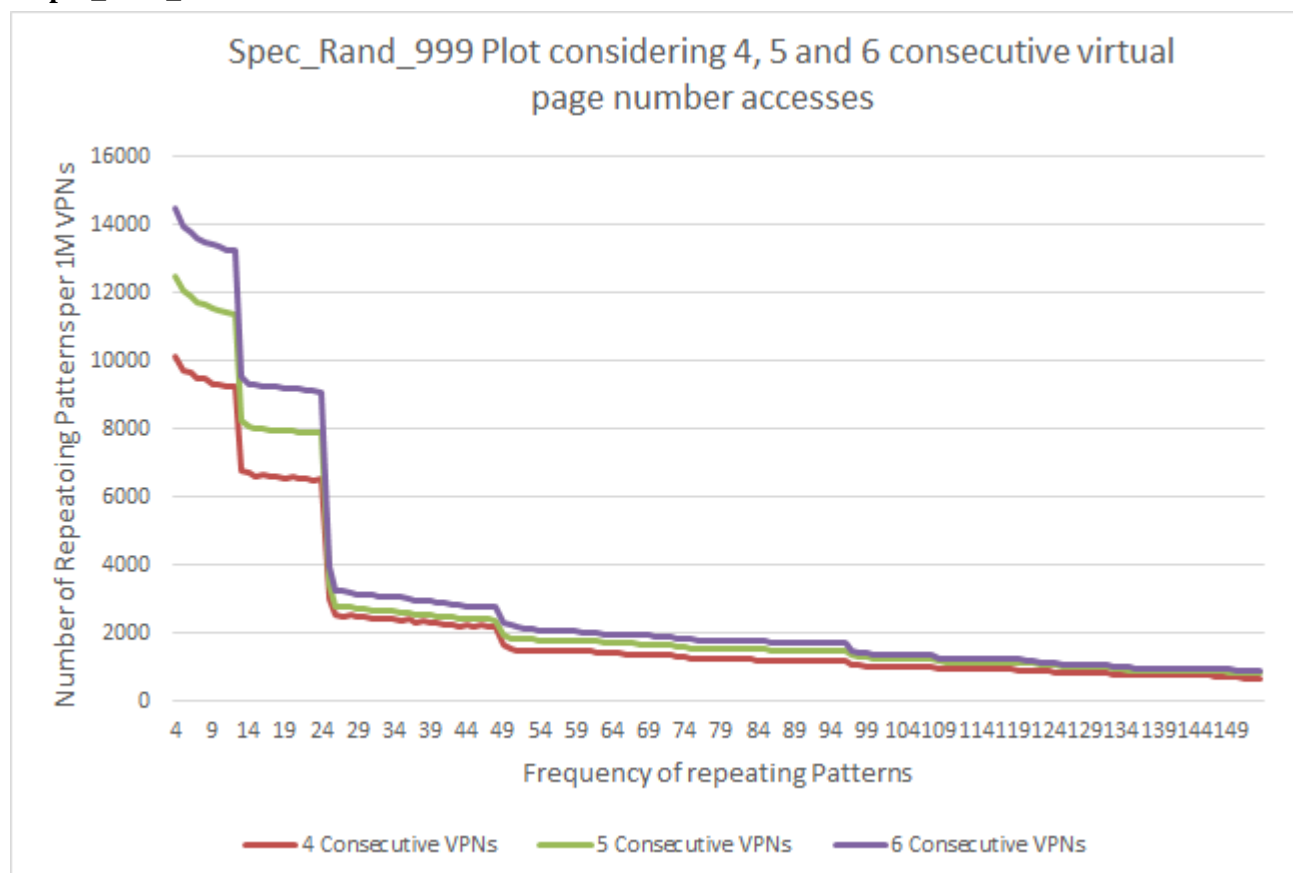
**In case of history based pattern analysis** we are observing that a very high no of wrong prefetches we would have to make if we are using last three bits for prediction and prefetching so it's something we just do not want because this is going to remove actual history based entry from buffer and going to do lot of wrong history prediction that's not there. So we are also analyzing for last 4 and 5 bits that is what we are doing for checking history of length 4, 5, 6 as if we increase length of history we are getting assurance that they are more likely to occur in same order in future also, as from data we are getting that for example spec\_rand 998 or 999 both shows better history frequency as compared to mcf. Same as in sjeng also we have not got that much total difference in higher frequency as compared to other but still means there is more no of sequence with higher frequency means in range of 100-250 in sjeng as compared to others.

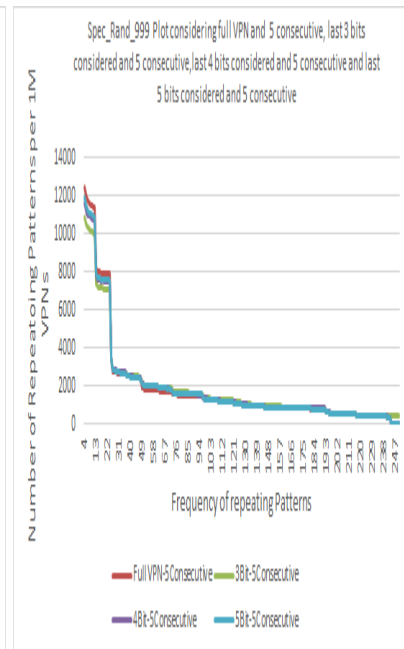
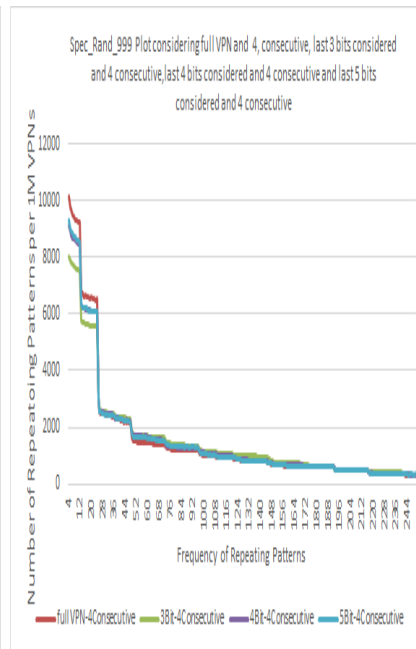
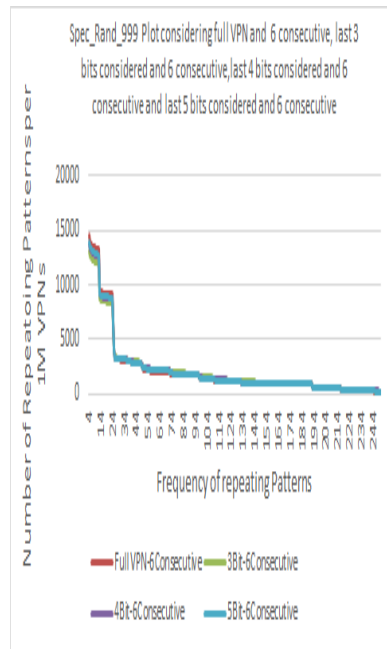
#### 1. Spec\_rand\_998



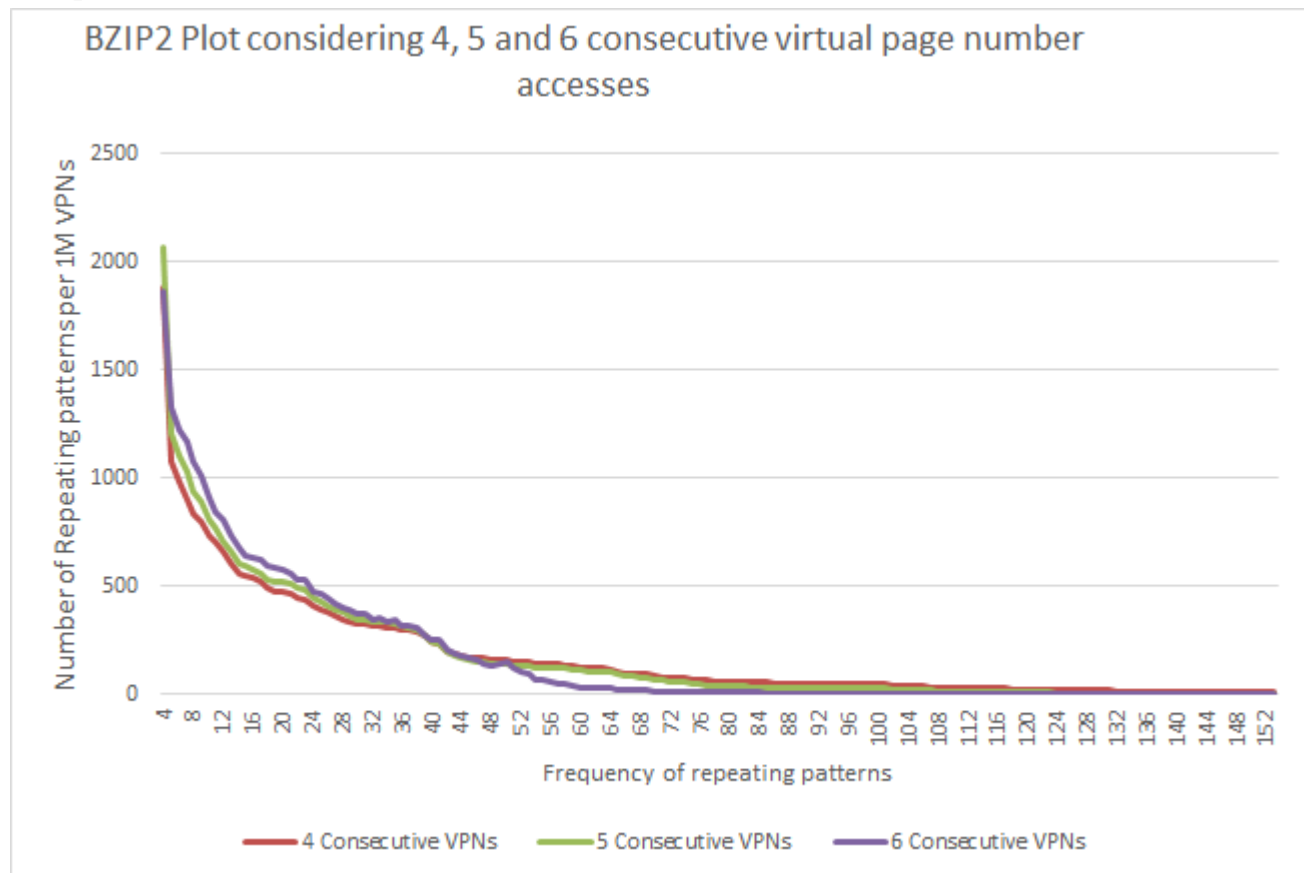


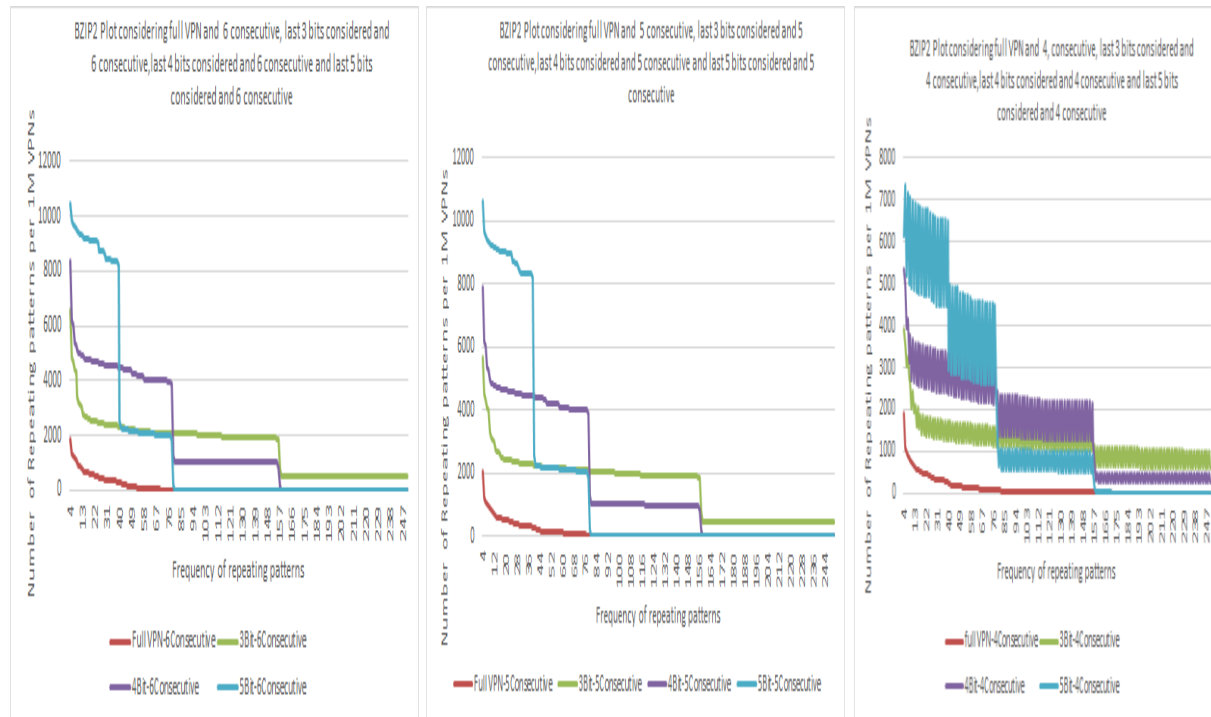
## 2.Spec\_rand\_999



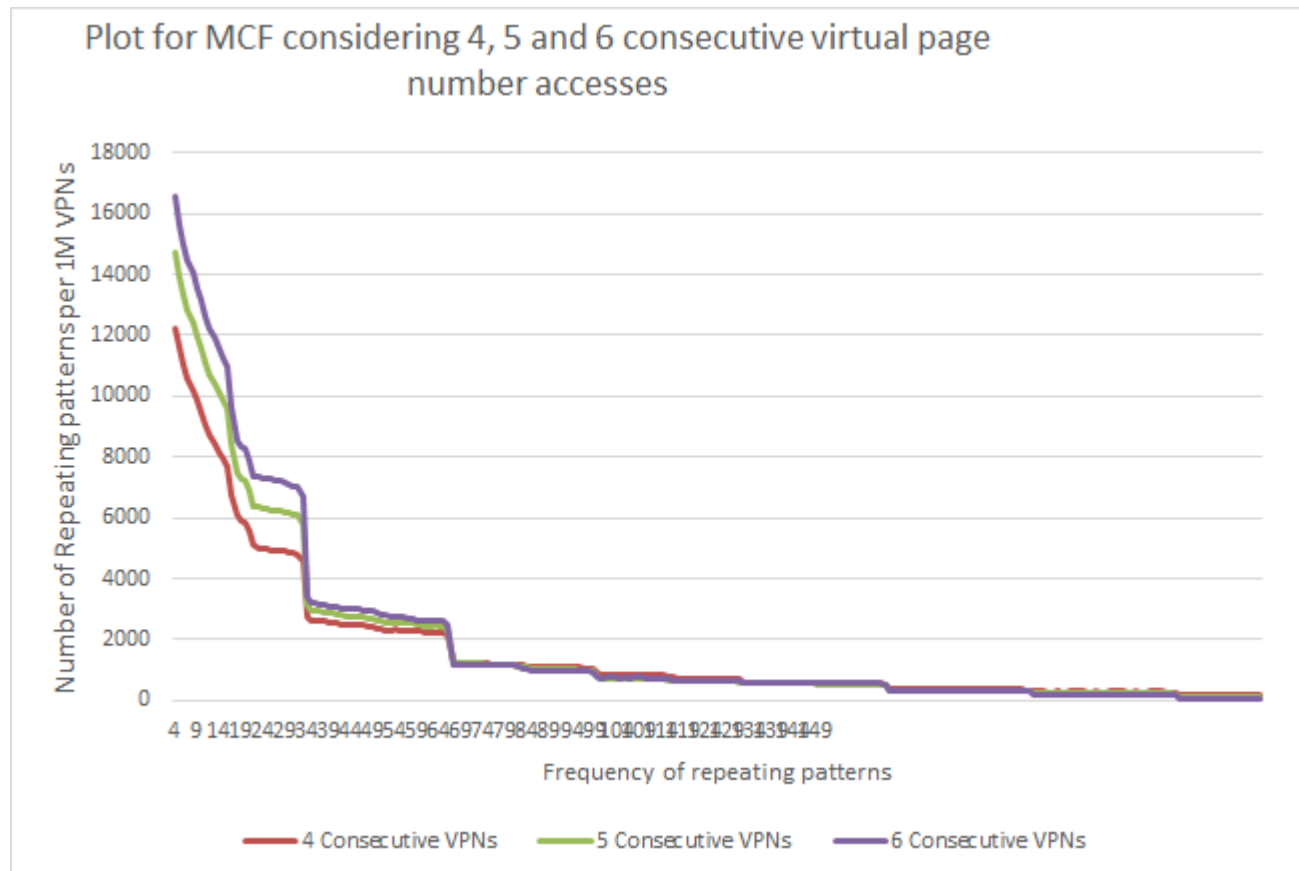


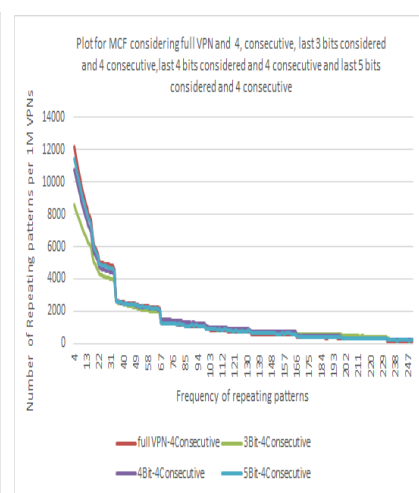
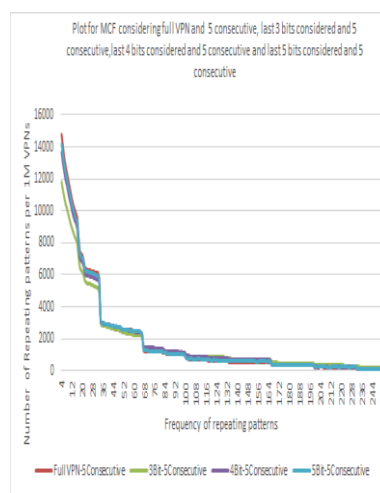
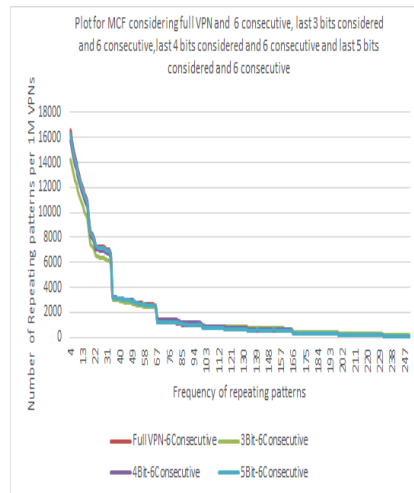
### 3.Bzip2



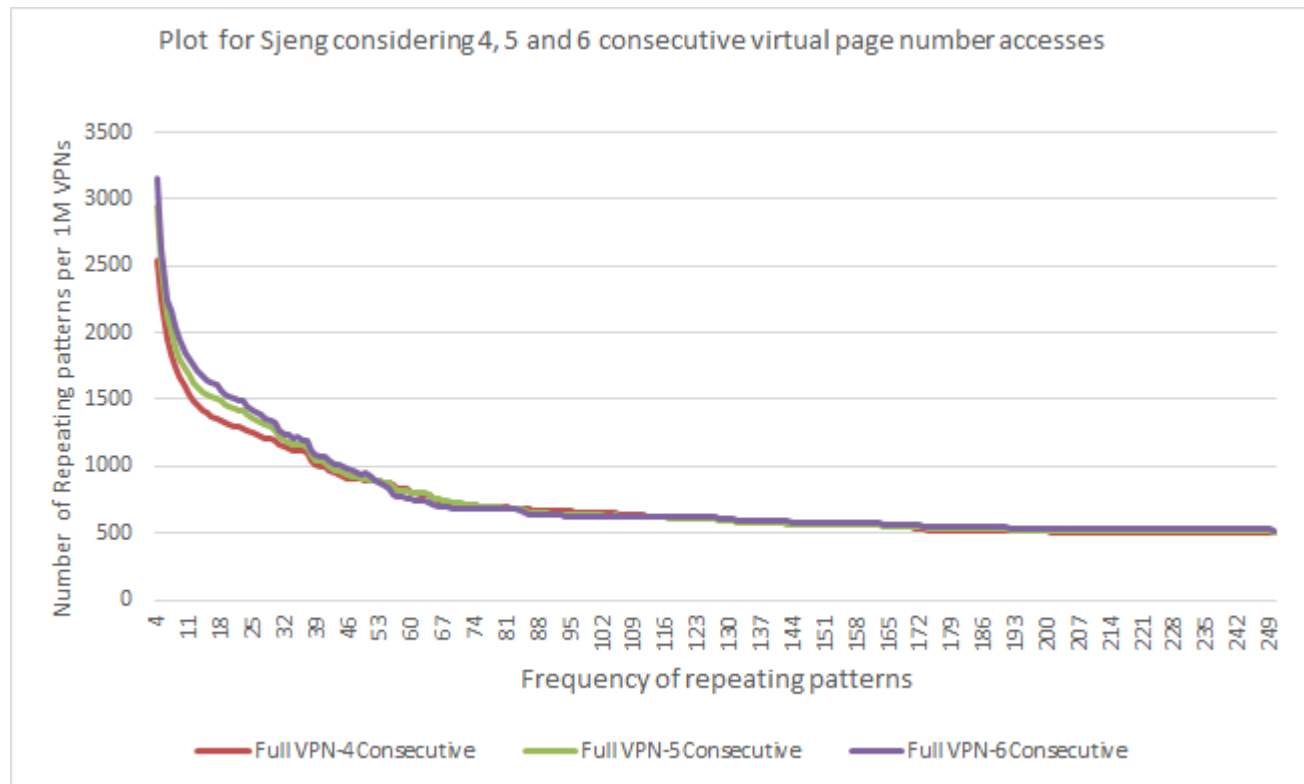


#### 4.Mcf

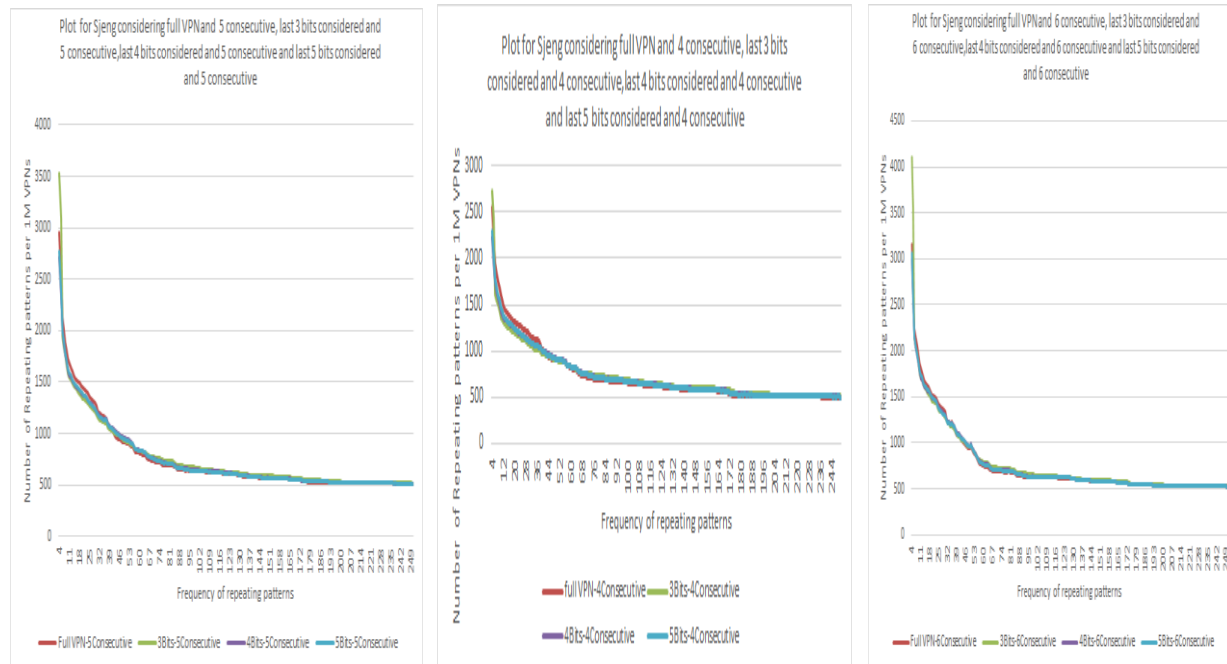




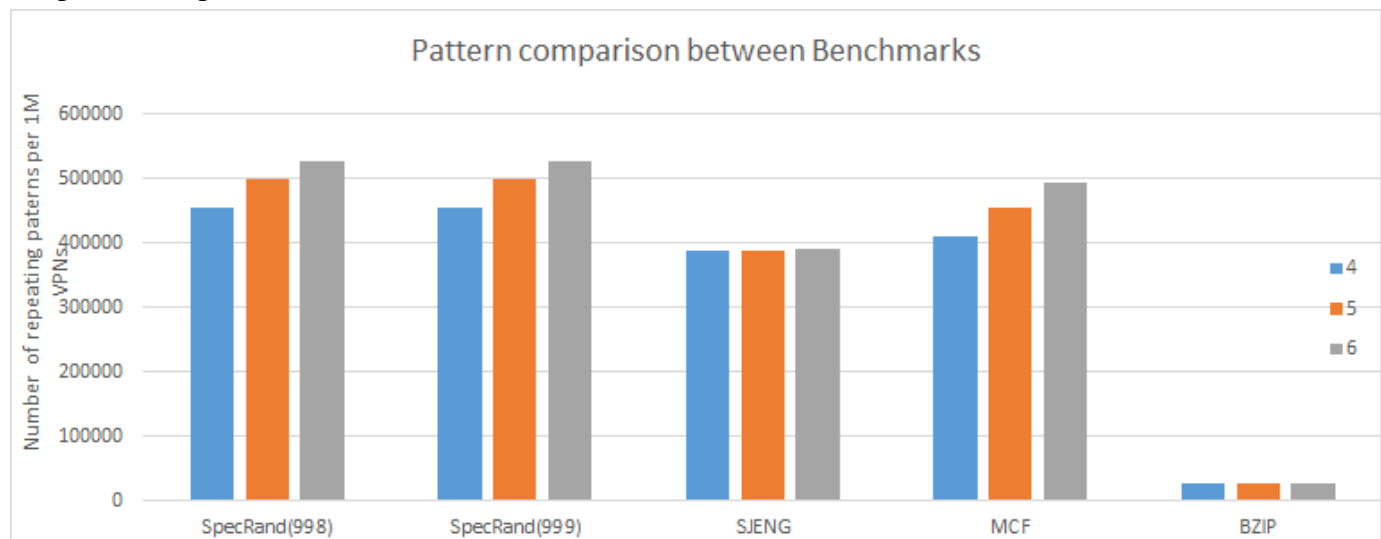
## 4.sjeng







### Graph for comparison between various benchmarks



### OBSERVATIONS :-

Here as we can see that bzip has very low amount of repetitive history whereas other 4 have good repetition but in them to sjeng has very high repetition of history as frequency is high in case of sjeng .Spec 998 and 999 have good amount of history repetition but frequency is not that high as compared to sjeng

### 4.6 Future work :-

As because of time constraints and lot of time getting spent on understanding gem5, it's working and setting up benchmark and amount of time simulator takes for a benchmark we are not able to implement design based on our analyses, so future work would be to implement scheme and see how it improves simple tlb performance or not, so we have to implement given design on various parameters mentioned above for history based analyses and see how energy and cost increases and how much performance gain we are going to get we are getting any.

Then second would be to compare our schemes with other tlb prefetching techniques and how would our design going to work as compared to these prefetching techniques and how much misses our implementaion resolved which are not resolved in these implementations.

## **5. Acknowledgements**

We would like to acknowledge Prof. Arkaprava Basu for his support and guidance for doing the project .We also like to thank few of our fellow colleagues and system lab members who have provided us lot of help in resolving few problems and We also like to acknowledge course e0-243 so that we were able to work on real problem.

## **6. References:-**

- [1] Ashley Saulsbury, fredrik.dahlgren,Per Stenström. Recency based tlb prefetching
- [2] [G.B. Kandiraju](#) , [A. Sivasubramaniam](#) .Going the distance for TLB prefetching: an application- driven study.Proceedings 29th Annual International Symposium on Computer Architecture
- [3] Abhishek Bhattacharjee and Margaret Martonosi .Inter-Core Cooperative TLB Prefetchers for Chip Multiprocessors .
- [4] Kyles J Nesbit , James E Smith .Data cache prefetching using global history buffer.

