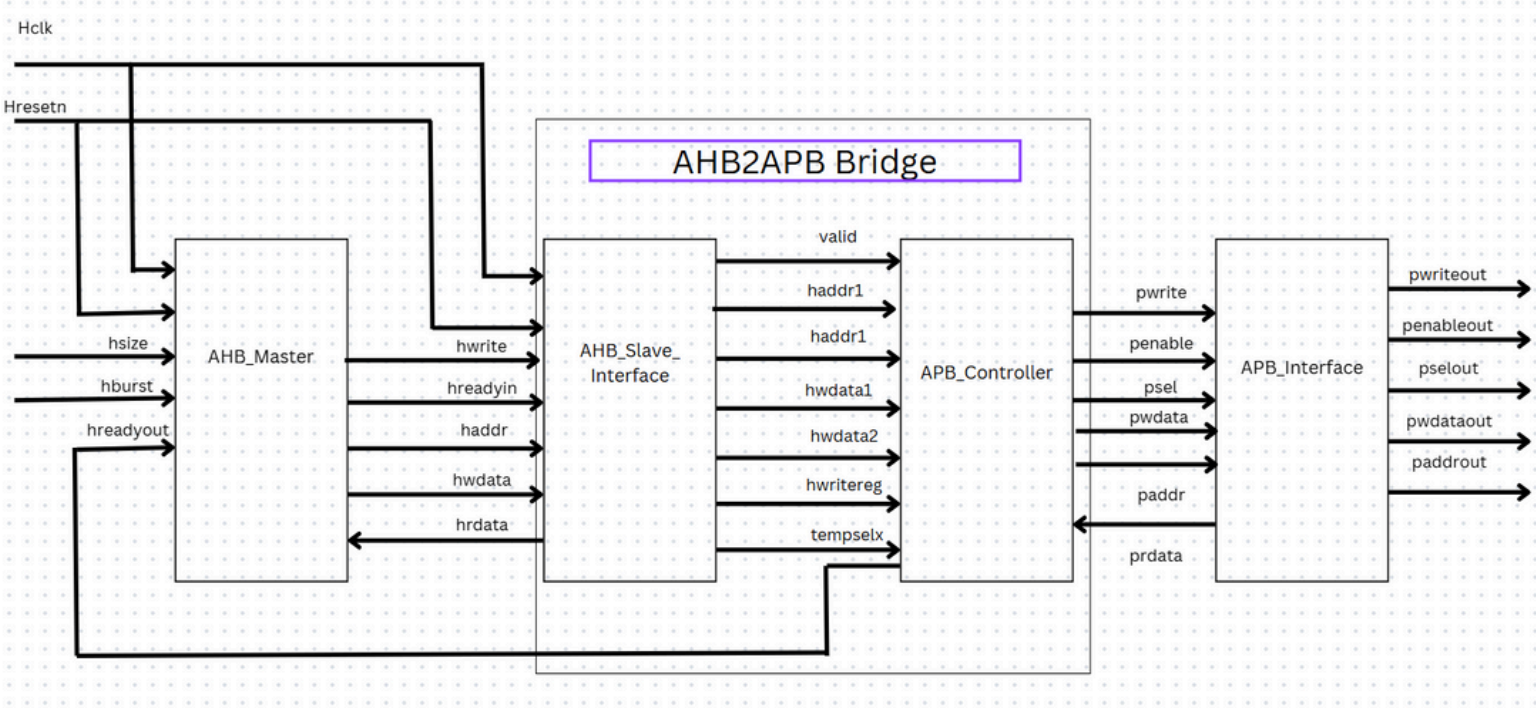
AHB to APB Bridge Design

Block Diagram



1) AHB Slave Interface

```
module AHB_slave_interface(input hclk, hresetn, hwrite, hreadyin,
                           input [31:0] hwdata, haddr, prdata,
                           input [1:0] htrans, hresp,
                           output reg  valid, hwrite_reg,
                           output reg[31:0] haddr1, haddr2, hwdata1, hwdata2,
                           output reg[2:0] temp_selx,
                           output [31:0] hrdata);

//pipelining the address and the data

always@(posedge hclk)
  begin
   if(!hresetn)
     begin
       haddr1<=0;
       haddr2<=0;
     end
   else
     begin
       haddr1<=haddr;
       haddr2<=haddr1;
     end
  end
```

```
always@(posedge hclk)
  begin
   if(!hresetn)
     begin
       hwdata1<=0;
       hwdata2<=0;
     end
   else
     begin
       hwdata1<=hwdata;
       hwdata2<=hwdata1;
     end
  end

always@(posedge hclk)
  begin
   if(!hresetn)
     begin
       hwrite_reg<=0;
     end
   else
     begin
       hwrite_reg<=hwrite;
     end
  end
```

```
//checking if the conditions are valid are or not

always@(*)
 begin
  valid=1'b0;
  if(hreadyin && haddr>=32'h8000_0000 && haddr<=32'h8c00_0000 && htrans==2'b10 || htrans==2'b11)
   begin
    valid=1;
   end
  else
   begin
    valid=0;
   end
 end
```

```
//assigning the value to temp_selx

always@(*)
 begin
  temp_selx=3'b000;
  if(haddr>=32'h8000_0000 && haddr<=32'h8400_0000)
   begin
    temp_selx=3'b001;
   end
  else if(haddr>=32'h8400_0000 && haddr<=32'h8800_0000)
   begin
    temp_selx=3'b010;
   end
  else if(haddr>=32'h8800_0000 && haddr<=32'h8c00_0000)
   begin
    temp_selx=3'b100;
   end
  else
   begin
    temp_selx=3'b000;
   end
 end


  assign hrdata=prdata;
  //assign hresp=2'b0;

 endmodule
```


2) APB Contoller

```
module APB_Controller(
input valid, hwrite_reg, hwrite, hresetn, hreadyin, hclk,
input [31:0] haddr, haddr1, haddr2, hwdata, hwdata1, hwdata2, prdata,
input [2:0] temp_selx,
output reg pwrite, penable, hr_readyout,
output reg[31:0] paddr, pwdata,
output reg[2:0] psel);

reg penable_temp, pwrite_temp, hr_readyout_temp;
reg[2:0] psel_temp;
reg[31:0] pwdata_temp, paddr_temp;

parameter ST_IDLE=3'b000,
    ST_WWAIT=3'b001,
    ST_WRITEP=3'b010,
    ST_WRITE=3'b011,
    ST_WENABLE=3'b100,
    ST_WENABLEP=3'b101,
    ST_READ=3'b110,
    ST_RENABLE=3'b111;

reg[2:0] present, next;
```

```
//present state logic

always@(posedge hclk)
 begin
  if(!hresetn)
   begin
    present <= ST_IDLE;
   end
  else
   begin
     present <= next;
   end
 end
```

```
//next state logic

always@(*)

 begin
  next = ST_IDLE;
  case(present)
     ST_IDLE: begin
                if(valid==1 && hwrite==1)
                 next = ST_WWAIT;
                else if(valid==1 && hwrite==0)
                 next = ST_READ;
                else
                 next = ST_IDLE;
                end
     ST_WWAIT: begin
                 if(valid==1)
                  next=ST_WRITEP;
                 else
                  next=ST_WRITE;
                end
     ST_WRITEP: begin
                  next=ST_WENABLEP;
                 end
```

```
    ST_WRITE: begin
               if(valid==1)
                next=ST_WENABLEP;
               else
                next=ST_WENABLE;
              end
    ST_WENABLE: begin
                  if(valid==1 && hwrite==0)
                   next=ST_READ;
                  else if(valid==1 && hwrite==1)
                   next=ST_WWAIT;
                  else
                   next=ST_IDLE;
                 end
    ST_WENABLEP: begin
                  if(valid==1 && hwrite_reg==1)
                   next=ST_WRITEP;
                  else if(valid==0 && hwrite_reg==1)
                   next=ST_WRITE;
                  else
                   next=ST_READ;
                 end
    ST_READ:  begin
             next=ST_RENABLE;
             end
```

```
     ST_RENABLE:
                begin
                  if(valid && !hwrite)
                   next=ST_READ;
                  else if(valid && hwrite)
                   next=ST_WWAIT;
                  else if(!valid)
                   next=ST_IDLE;
                 end
                endcase
   end

//temporary logic

always@(*)

    begin
     case(present)
      ST_IDLE:
                if(valid && !hwrite)
                 begin
                   paddr_temp=haddr;
                   pwrite_temp=hwrite;
                   psel_temp=temp_selx;
                   penable_temp=0;
                   hr_readyout_temp=0;
                 end
```



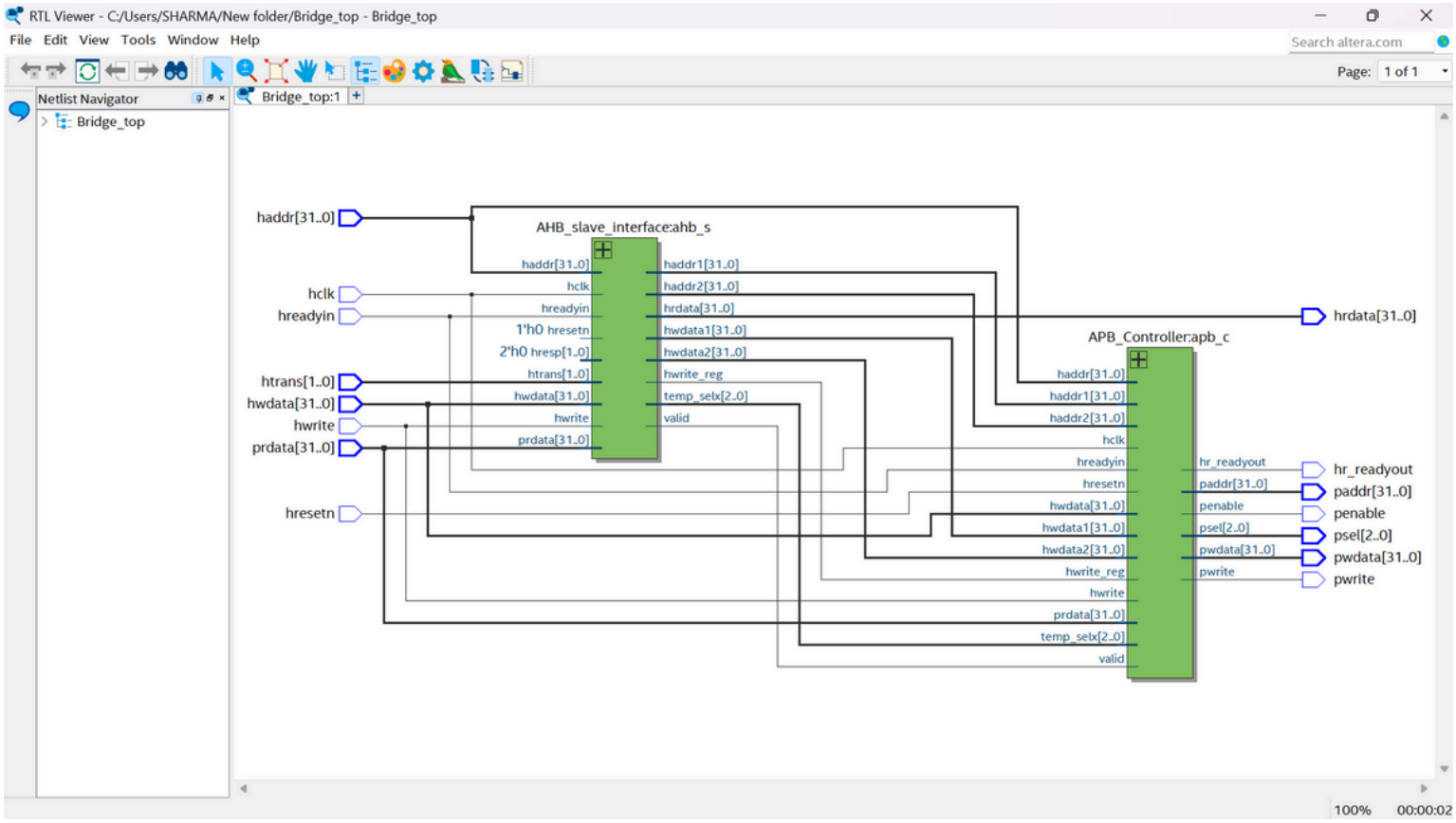
```
                else if(valid && hwrite)
                 begin
                   psel_temp=0;
                   penable_temp=0;
                   hr_readyout_temp=1;
                 end

                else
                 begin
                   psel_temp=0;
                   penable_temp=0;
                   hr_readyout_temp=1;
                 end

      ST_READ:
             begin
              penable_temp=1;
              hr_readyout_temp=1;
             end

      ST_RENABLE: if(valid && !hwrite)
                 begin
                   paddr_temp=haddr;
                   pwrite_temp=hwrite;
                   psel_temp=temp_selx;
                  hr_readyout_temp=0;
                  penable_temp=0;
                 end
```

```
                else if(valid && hwrite)
                 begin
                   psel_temp=0;
                   penable_temp=0;
                   hr_readyout_temp=1;
                 end

     ST_WWAIT:
             if(valid)
              begin
               hr_readyout_temp=0;
               penable_temp=0;
               paddr_temp=haddr1;
               pwdata_temp=hwdata;
               pwrite_temp=hwrite;
               psel_temp=temp_selx;
              end

             else
              begin
               paddr_temp=haddr;
               pwdata_temp=hwdata;
               pwrite_temp=hwrite;
               hr_readyout_temp=1'b0;
              end
```

```
     ST_WRITEP:
             begin
               paddr_temp=haddr1;
               pwdata_temp=hwdata;
               penable_temp=1;
               hr_readyout_temp=0;
             end


     ST_WENABLEP:
              begin
               paddr_temp=haddr1;
               pwdata_temp=hwdata;
               pwrite_temp=hwrite;
               psel_temp=temp_selx;
               penable_temp=0;
               hr_readyout_temp=0;
              end
    endcase
   end
```

```
//output logic

always@(posedge hclk)
 begin
  if(!hresetn)
   begin
    paddr<=0;
    pwdata<=0;
    pwrite<=0;
    penable<=0;
    psel<=0;
    hr_readyout<=0;
   end

  else
   begin
    paddr<=paddr_temp;
    pwdata<=pwdata_temp;
    pwrite<=pwrite_temp;
    penable<=penable_temp;
    psel<=psel_temp;
    hr_readyout<=hr_readyout_temp;
   end
 end

endmodule
```


Synthesis for AHB-slave and APB-controller



3) Testbench for AHB-slave

```
module AHB_slave_interface_tb();
  reg hclk, hresetn, hwrite, hreadyin;
  reg [31:0] haddr, hwdata, prdata;
  reg [1:0] htrans, hresp;
  wire valid, hwrite_reg;
  wire [2:0] temp_selx;
  wire [31:0] haddr1, haddr2, hwdata1, hwdata2, hrdata;

  AHB_slave_interface DUT(hclk, hresetn, hwrite, hreadyin, hwdata, haddr, prdata, htrans, hresp,
                          valid, hwrite_reg, haddr1, haddr2, hwdata1, hwdata2, temp_selx, hrdata);

    initial
     begin
      hclk=1'b0;
      forever #10 hclk=~hclk;
     end

    task reset();
     begin
      @(negedge hclk)
       hresetn=1'b0;
      @(negedge hclk)
       hresetn=1'b1;
     end
    endtask
```

```
    task inputs(input i, j,input [1:0]k);
     begin
      @(negedge hclk);
      hwrite=i;
      hreadyin=j;
      htrans=k;
     end
    endtask

    task in(input[31:0]d, e);
     begin
      hwdata=d;
      haddr=e;
     end
    endtask
```

```
    initial
     begin
      reset;
      inputs(1,1,2'b10);
      in(32'h28, 32'h8000_0002);
      inputs(1,1,2'b11);
      in(32'h73, 32'h8000_0003);
      inputs(1,1,2'b10);
      in(32'h89, 32'h8000_0004);
      inputs(1,1,2'b00);
      in(32'h105, 32'h8000_0005);
      inputs(0,1,2'b10);
      in(32'h0, 32'h0);
      prdata=32'h73;
     end
endmodule
```

4) Testbench for APB-controller

```
module APB_Contoller_tb();
          reg hclk, hresetn, hwrite, valid, hwrite_reg;
          reg [31:0] haddr, hwdata, haddr1, haddr2, hwdata1, hwdata2, prdata;
          reg[2:0] temp_selx;
          wire pwrite, penable, hr_readyout;
          wire[2:0] psel;
          wire[31:0]pwdata, paddr;


        APB_Controller DUT(valid, hwrite_reg, hwrite, hresetn, hreadyin, hclk,
                           haddr, haddr1, haddr2, hwdata, hwdata1, hwdata2, prdata, temp_selx,
                           pwrite, penable, hr_readyout, paddr, pwdata, psel);

        initial
         begin
          hclk=1'b0;
          forever #10 hclk=~hclk;
         end

        task reset();
         begin
          @(negedge hclk)
           hresetn=1'b0;
          @(negedge hclk)
           hresetn=1'b1;
         end
        endtask
```

```
        initial
         begin
          reset;
          hwrite=1'b1;
          valid=1'b1;
          haddr=32'h8100_0000;
          haddr1=32'h8200_0000;
          haddr2=32'h8300_0000;
          hwdata='d32;
          hwdata1='d45;
          hwdata2='d52;
          prdata='d543;
          hwrite_reg=1'b1;
          temp_selx=3'b001;

          #100;

          hwrite=1'b0;
          valid=1'b0;
         end
endmodule
```

5) AHB Master

```
module AHB_Master(input hclk, hresetn, hr_readyout,
                  input [31:0] hrdata,
                  output reg hwrite,hreadyin,
                  output reg [31:0] haddr, hwdata,
                  output reg [1:0]htrans);
                  reg [2:0] hburst;  //single,4,8,16,...
                  reg [2:0] hsize;   //size 8,16,...

integer i,j;

task single_write();
  begin
  @(posedge hclk)
     #1;
     begin
        hwrite=1;
        hreadyin=1;
        htrans=2'd2;
        hsize=0;
        hburst=0;
        haddr=32'h8000_0001;
    end
```

```
  @(posedge hclk)
        #1;
    begin
        htrans=2'd0;
        hwdata=8'h80;
    end
  end
endtask

task single_read();
 begin
  @(posedge hclk)
    begin
     hwrite=0;
     htrans=2'd2;
     hreadyin=1;
     hburst=0;
     hsize=0;
     haddr=32'h8000_0001;
    end
  @(posedge hclk)
   #1;
    begin
     htrans=2'd0;
    end
 end
endtask
```

```
task burst_write();
 begin
  @(posedge hclk)
   #1;
   begin
    hwrite=1'b1;
    htrans=2'd2;
    hburst=3'd3;
    hsize=0;
    hreadyin=1;
    haddr=32'h8000_0001;
   end

  @(posedge hclk)
   #1;
   begin
    haddr=haddr+1'b1;
    hwdata={$random}%256;
    htrans=2'd3;
   end

 for(i=0;i<2;i=i+1)
  begin
  @(posedge hclk);
    #1
    haddr=haddr+1;
    hwdata={$random}%256;
    htrans=2'd3;
  end
```



```
   @(posedge hclk);
    #1;
    begin
     htrans=2'd0;
     hwdata={$random}%256;
    end
 end
endtask
endmodule
```

6) APB Interface

```
module APB_Interface(input penable, pwrite,
                     input [2:0]psel,
                     input [31:0]pwdata, paddr,
                     output pwrite_out, penable_out,
                     output [2:0]psel_out,
                     output [31:0]pwdata_out, paddr_out,
                     output reg[31:0]prdata);

    assign penable_out=penable;
    assign pwrite_out=pwrite;
    assign pwdata_out=pwdata;
    assign paddr_out=paddr;
    assign psel_out=psel;

always@(*)
 begin
  if(!pwrite && penable)
  begin
  prdata=8'd37;
  end
 end
endmodule
```

7) Bridge Top

```
module Bridge_top(input hclk, hresetn, hwrite, hreadyin,
                  input [1:0]htrans,
                  input [31:0]haddr, hwdata, prdata,
                  output pwrite, penable, hr_readyout,
                  output [2:0]psel,
                  output [31:0]pwdata, paddr, hrdata);
                  wire [1:0]hresp;
                  wire valid, hwrite_reg;
                  wire [31:0]haddr1, haddr2, hwdata1, hwdata2;
                  wire [2:0]temp_selx;

       AHB_slave_interface ahb_s(hclk, hrestn, hwrite, hreadyin, hwdata, haddr, prdata, htrans, hresp,
                                 valid, hwrite_reg, haddr1, haddr2, hwdata1, hwdata2, temp_selx, hrdata);

       APB_Controller apb_c(valid, hwrite_reg, hwrite, hresetn, hreadyin, hclk,
                            haddr, haddr1, haddr2, hwdata, hwdata1, hwdata2, prdata, temp_selx,
                            pwrite, penable, hr_readyout, paddr, pwdata, psel);

endmodule
```

8) TOP Testbench

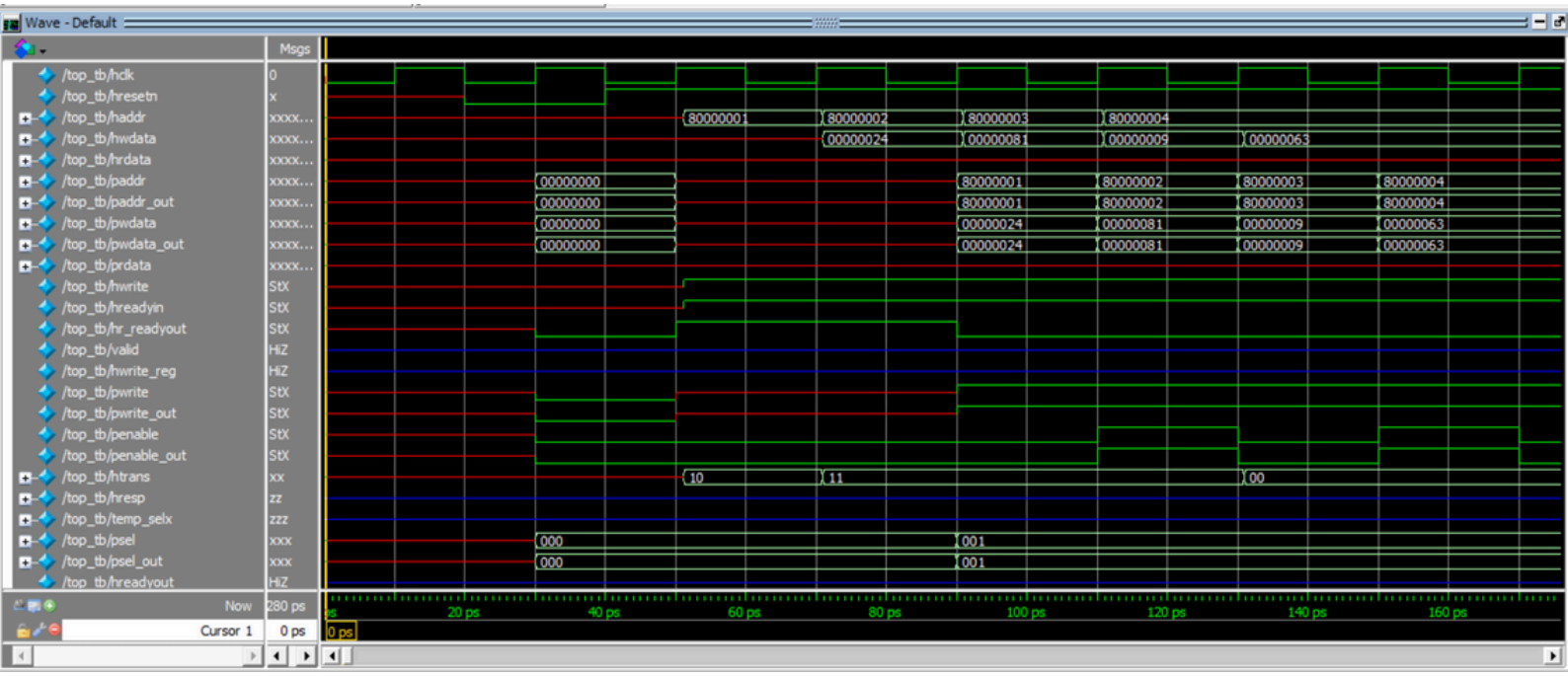
```
module top_tb();
     reg hclk, hresetn;
     wire [31:0] haddr, hwdata, hrdata, paddr, paddr_out, pwdata, pwdata_out, prdata;
     wire hwrite, hreadyin, hr_readyout, valid, hwrite_reg, pwrite, pwrite_out, penable, penable_out;
     wire [1:0] htrans, hresp;
     wire [2:0] temp_selx, psel, psel_out;

     AHB_Master ahb(hclk, hresetn, hreadyout, hrdata, hwrite,hreadyin, haddr, hwdata, htrans);

     APB_Interface apb(penable, pwrite, psel, pwdata, paddr, pwrite_out, penable_out, psel_out,
                       pwdata_out, paddr_out, prdata);

     Bridge_top bridge(hclk, hresetn, hwrite, hreadyin, htrans, haddr, hwdata, prdata, pwrite,
                       penable, hr_readyout, psel, pwdata, paddr, hrdata);
   initial
   begin
   hclk=1'b0;
   forever #10 hclk=~hclk;
   end

   task reset();
    begin
     @(negedge hclk)
      hresetn=1'b0;
     @(negedge hclk)
      hresetn=1'b1;
    end
   endtask
```

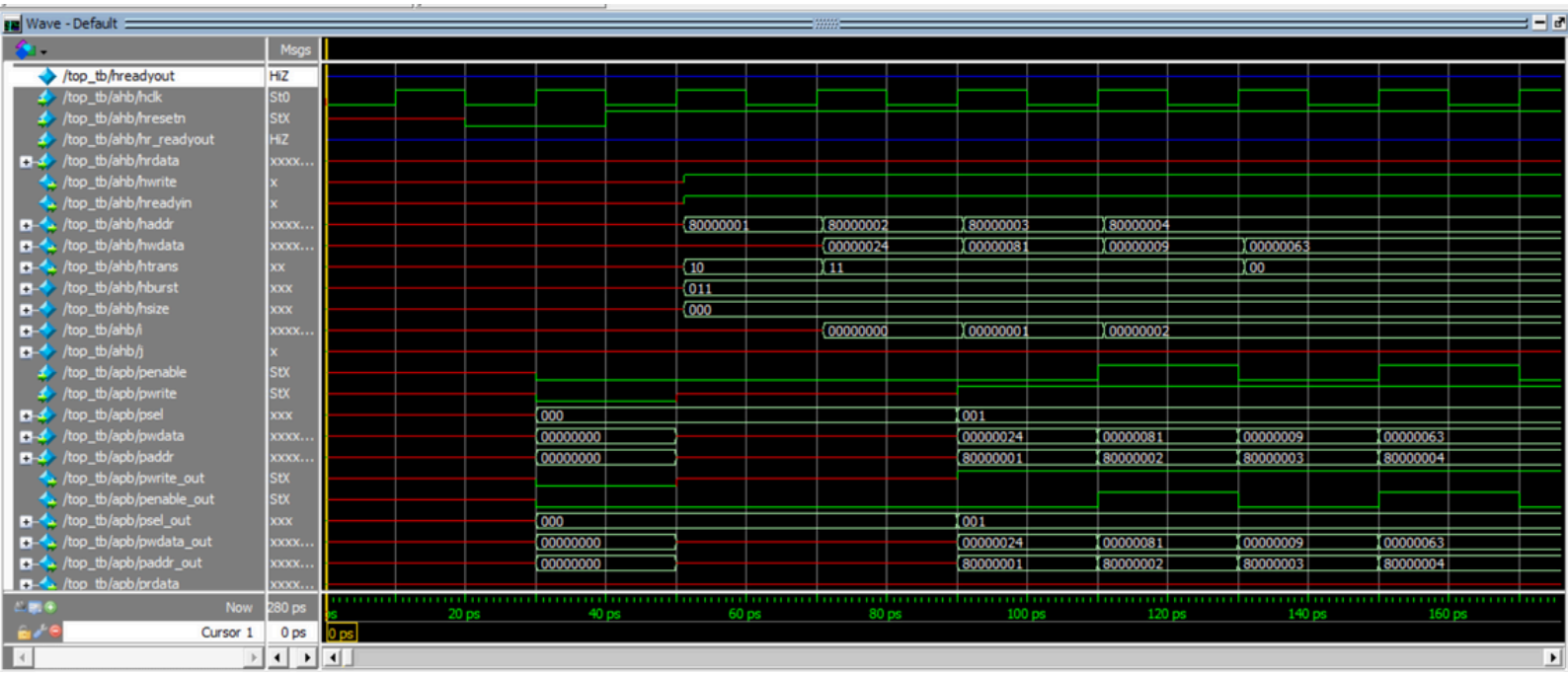


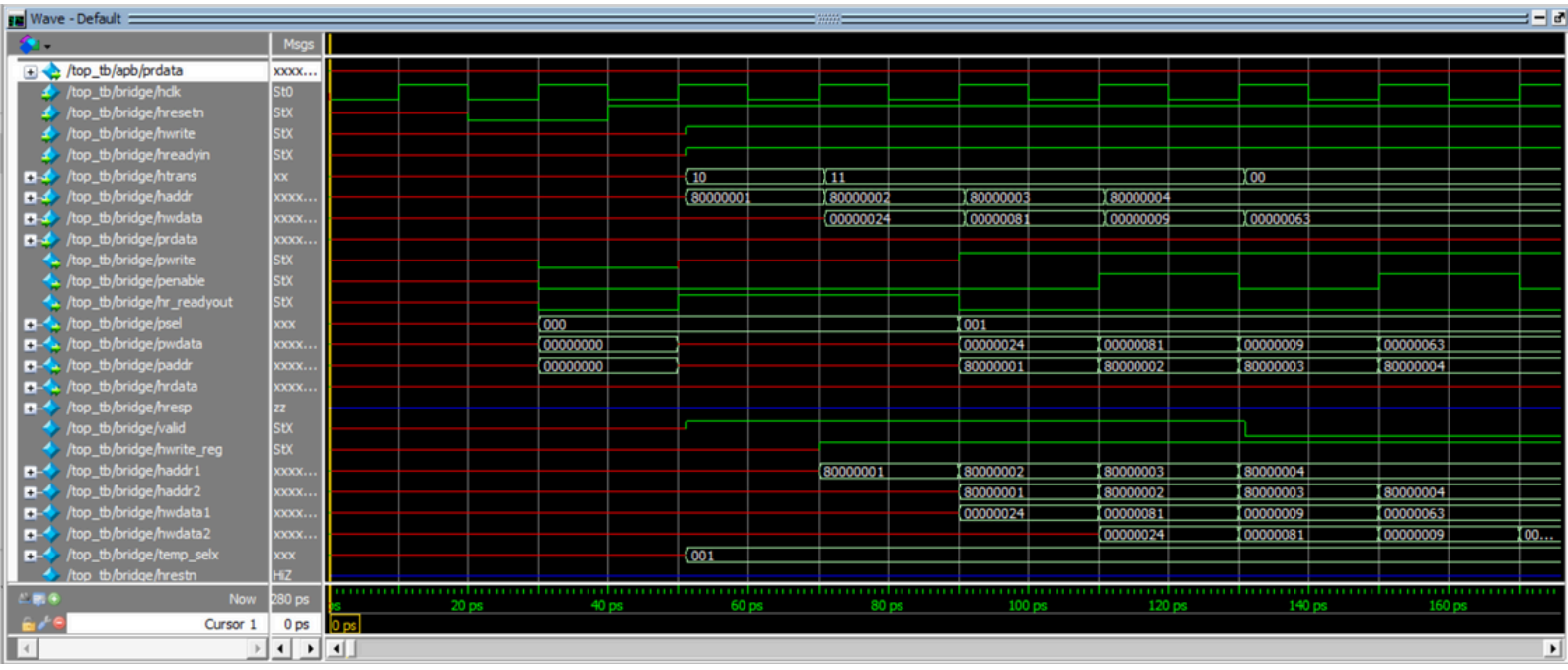
```
  initial
   begin
    reset;
    //ahb.single_write();
    ahb.burst_write();
    //ahb.single_read();
   end
endmodule
```

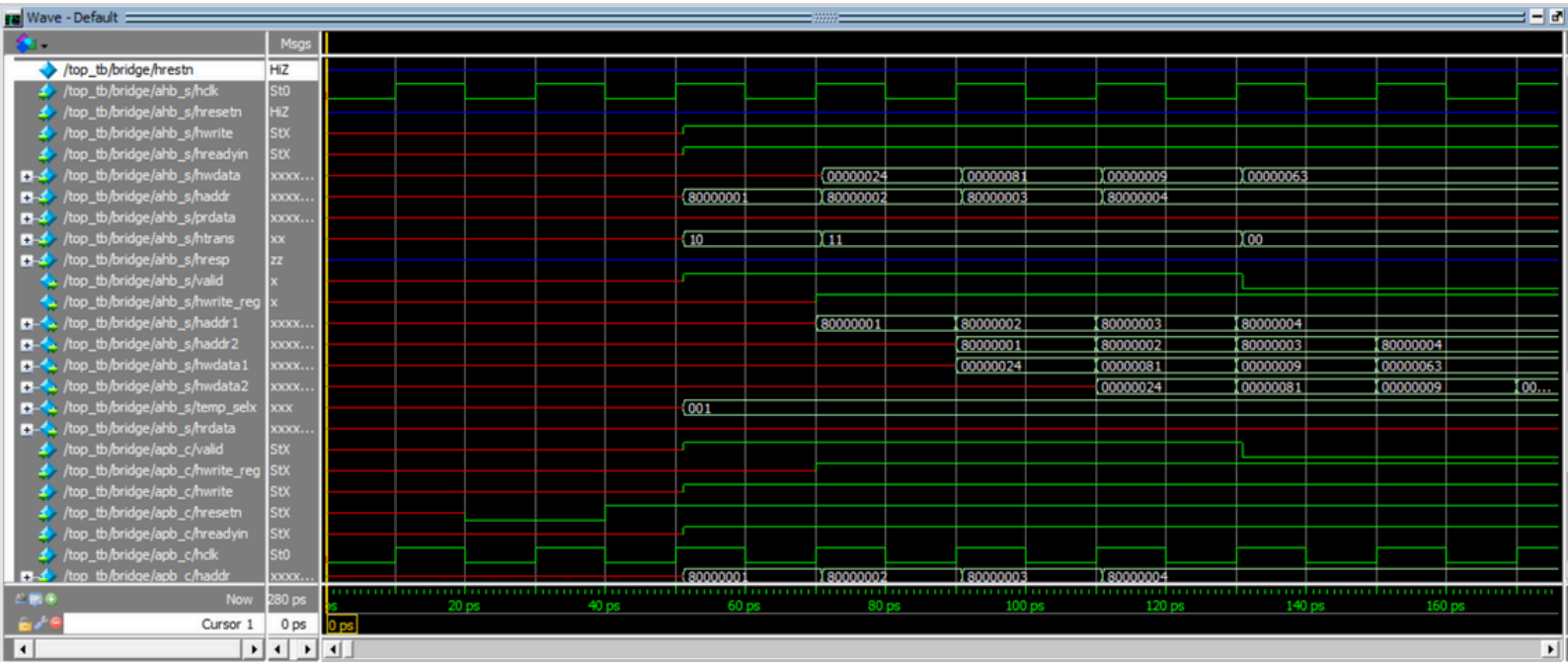
Simulation Waveforms

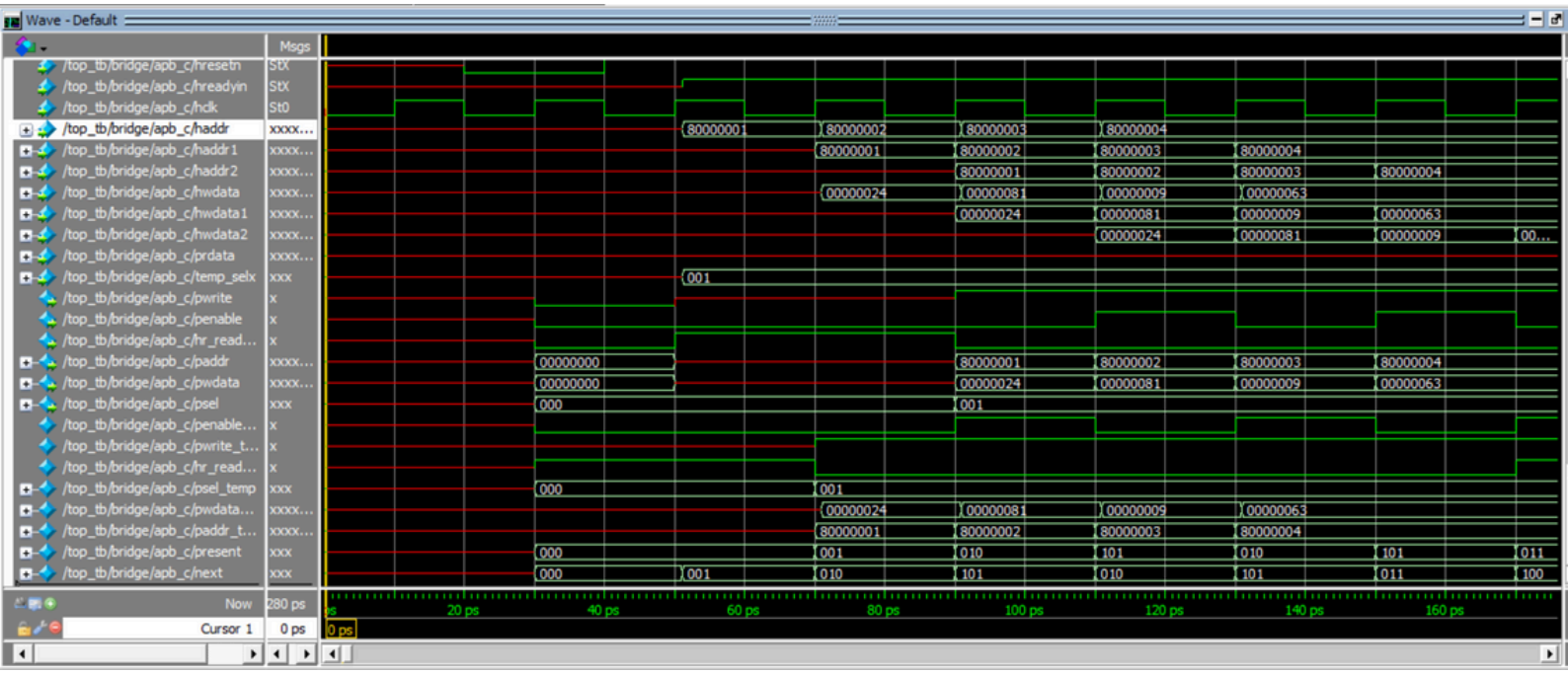
1) Burst_Write


Wave - Default
Msgs
/top_tb/hclk
/top_tb/hresetn
/top_tb/haddr
/top_tb/hwdata
/top_tb/hrdata
/top_tb/paddr
/top_tb/paddr_out
/top_tb/pwdata
/top_tb/pwdata_out
/top_tb/prdata
/top_tb/hwrite
/top_tb/hreadyin
/top_tb/hr_readyout
/top_tb/valid
/top_tb/hwrite_reg
/top_tb/pwrite
/top_tb/pwrite_out
/top_tb/penable
/top_tb/penable_out
/top_tb/htrans
/top_tb/hresp
/top_tb/temp_selx
/top_tb/psel
/top_tb/psel_out
/top_tb/hreadyout
Now
Cursor 1
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps

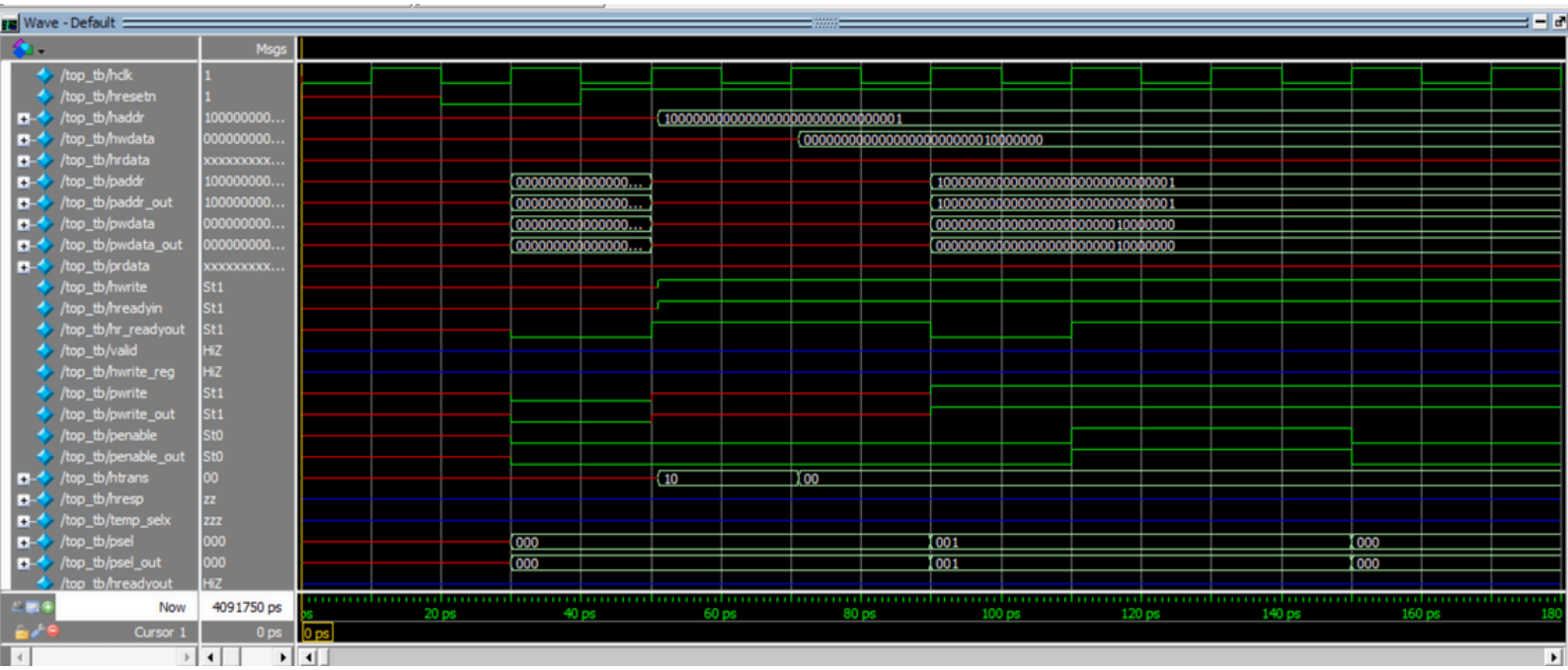

Wave - Default
Msgs
/top_tb/hreadyout
/top_tb/ahb/hclk
/top_tb/ahb/hresetn
/top_tb/ahb/hr_readyout
/top_tb/ahb/hrdata
/top_tb/ahb/hwrite
/top_tb/ahb/hreadyin
/top_tb/ahb/haddr
/top_tb/ahb/hwdata
/top_tb/ahb/htrans
/top_tb/ahb/hburst
/top_tb/ahb/hsize
/top_tb/ahb/i
/top_tb/ahb/j
/top_tb/apb/penable
/top_tb/apb/pwrite
/top_tb/apb/psel
/top_tb/apb/pwdata
/top_tb/apb/paddr
/top_tb/apb/pwrite_out
/top_tb/apb/penable_out
/top_tb/apb/psel_out
/top_tb/apb/pwdata_out
/top_tb/apb/paddr_out
/top_tb/apb/prdata
Now
Cursor 1
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps

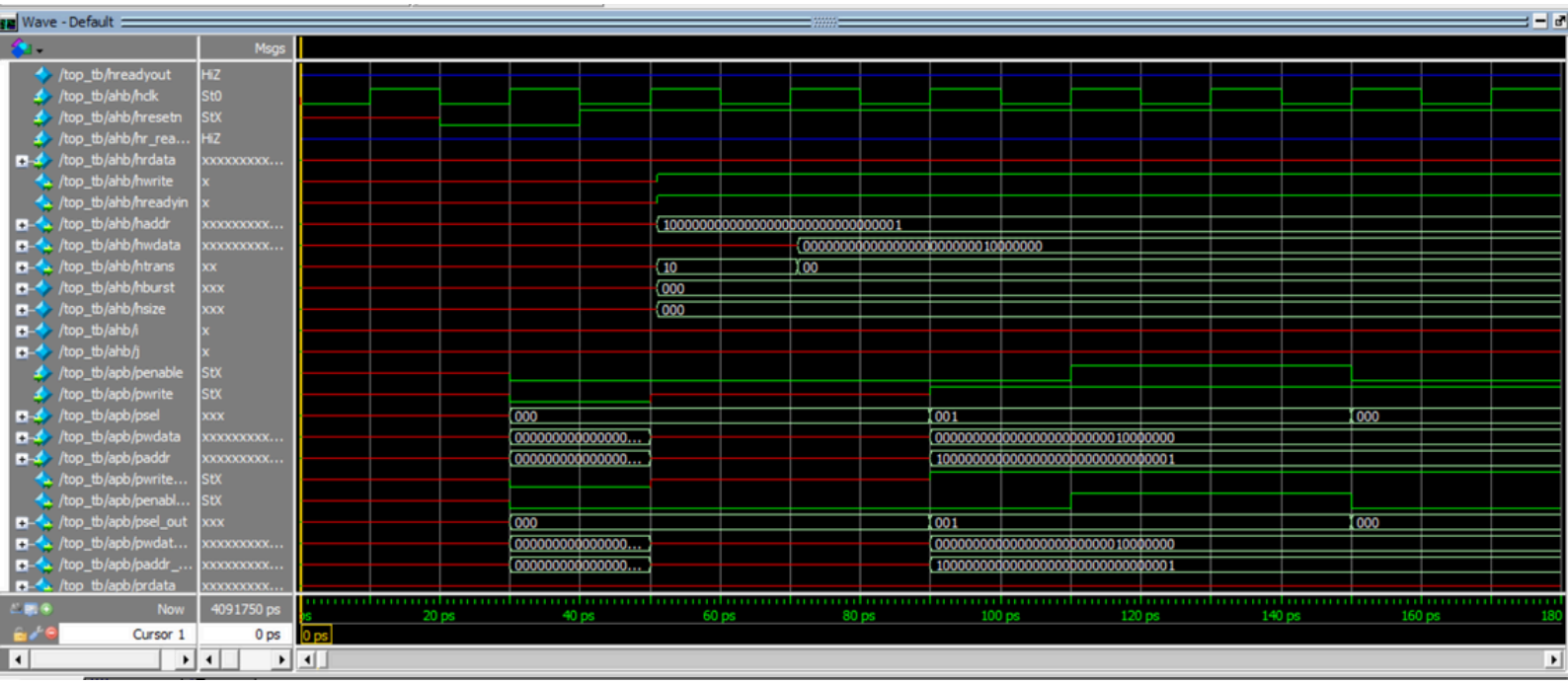

Wave - Default
Msgs
/top_tb/apb/prdata
/top_tb/bridge/hclk
/top_tb/bridge/hresetn
/top_tb/bridge/hwrite
/top_tb/bridge/hreadyin
/top_tb/bridge/htrans
/top_tb/bridge/haddr
/top_tb/bridge/hwdata
/top_tb/bridge/prdata
/top_tb/bridge/pwrite
/top_tb/bridge/penable
/top_tb/bridge/hr_readyout
/top_tb/bridge/psel
/top_tb/bridge/pwdata
/top_tb/bridge/paddr
/top_tb/bridge/hrdata
/top_tb/bridge/hresp
/top_tb/bridge/valid
/top_tb/bridge/hwrite_reg
/top_tb/bridge/haddr1
/top_tb/bridge/haddr2
/top_tb/bridge/hwdata1
/top_tb/bridge/hwdata2
/top_tb/bridge/temp_selx
/top_tb/bridge/hresetn
Now
Cursor 1
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps

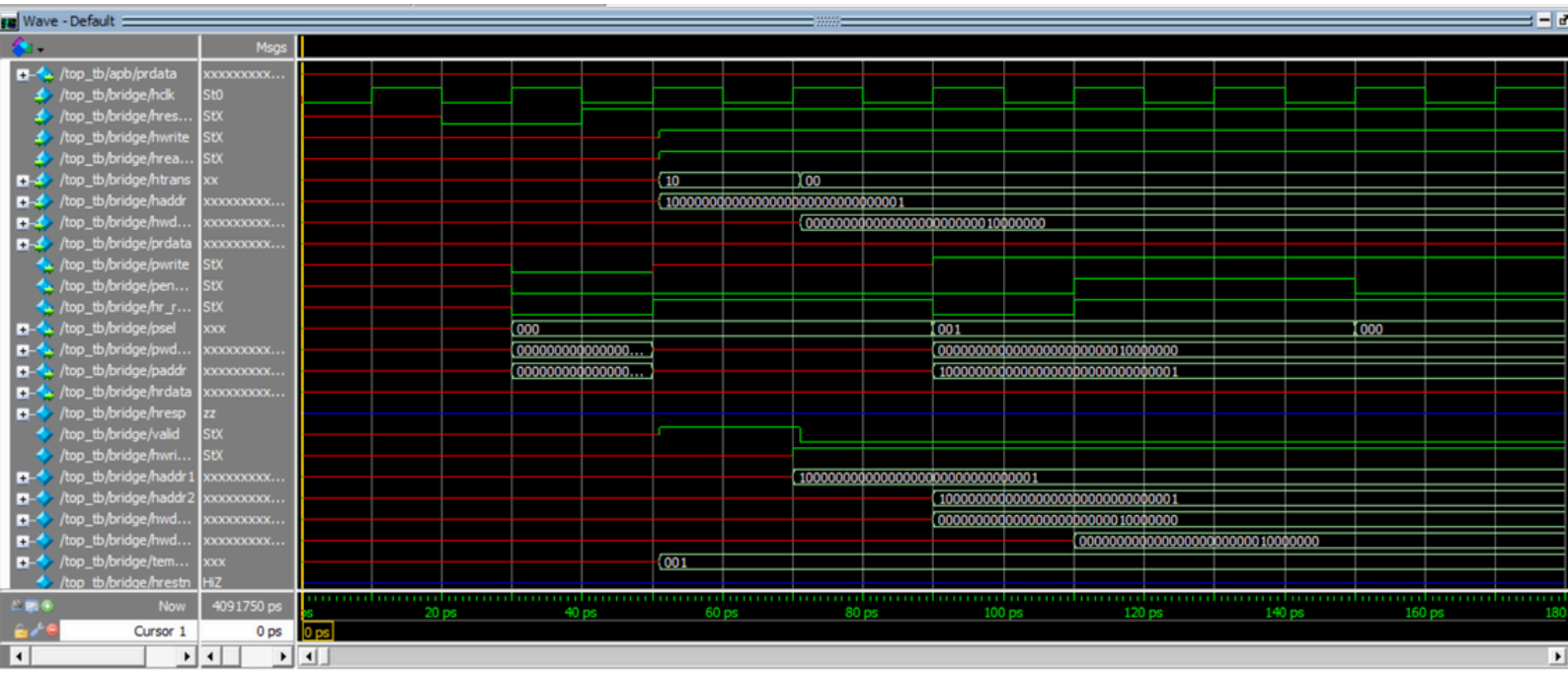




2) Single_Write


Wave - Default
Msgs
/top_tb/hclk
/top_tb/hresetn
/top_tb/haddr
/top_tb/hwdata
/top_tb/hrdata
/top_tb/paddr
/top_tb/paddr_out
/top_tb/pwdata
/top_tb/pwdata_out
/top_tb/prdata
/top_tb/hwrite
/top_tb/hreadyin
/top_tb/hr_readyout
/top_tb/valid
/top_tb/hwrite_reg
/top_tb/pwrite
/top_tb/pwrite_out
/top_tb/penable
/top_tb/penable_out
/top_tb/htrans
/top_tb/hresp
/top_tb/temp_selx
/top_tb/psel
/top_tb/psel_out
/top_tb/hreadyout
Now
4091750 ps
Cursor 1
0 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps
180
0 ps


Wave - Default
Msgs
/top_tb/hreadyout
/top_tb/ahb/hclk
/top_tb/ahb/hresetn
/top_tb/ahb/hr_rea...
/top_tb/ahb/hrdata
/top_tb/ahb/hwrite
/top_tb/ahb/hreadyin
/top_tb/ahb/haddr
/top_tb/ahb/hwdata
/top_tb/ahb/htrans
/top_tb/ahb/hburst
/top_tb/ahb/hsize
/top_tb/ahb/i
/top_tb/ahb/j
/top_tb/apb/penable
/top_tb/apb/pwrite
/top_tb/apb/psel
/top_tb/apb/pwdata
/top_tb/apb/paddr
/top_tb/apb/pwrite...
/top_tb/apb/penabl...
/top_tb/apb/psel_out
/top_tb/apb/pwdat...
/top_tb/apb/paddr_...
/top_tb/apb/prdata
Now
4091750 ps
Cursor 1
0 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps
180
0 ps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/top_tb/bridge/hrea...
/top_tb/bridge/htrans
/top_tb/bridge/haddr
/top_tb/bridge/hwd...
/top_tb/bridge/prdata
/top_tb/bridge/pwrite
/top_tb/bridge/pen...
/top_tb/bridge/hr_r...
/top_tb/bridge/psel
/top_tb/bridge/pwd...
/top_tb/bridge/paddr
/top_tb/bridge/hrdata
/top_tb/bridge/hresp
/top_tb/bridge/valid
/top_tb/bridge/hwri...
/top_tb/bridge/haddr1
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/top_tb/bridge/hwd...
/top_tb/bridge/hwd...
/top_tb/bridge/tem...
/top_tb/bridge/hresetn
Now
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Cursor 1
0 ps
20 ps
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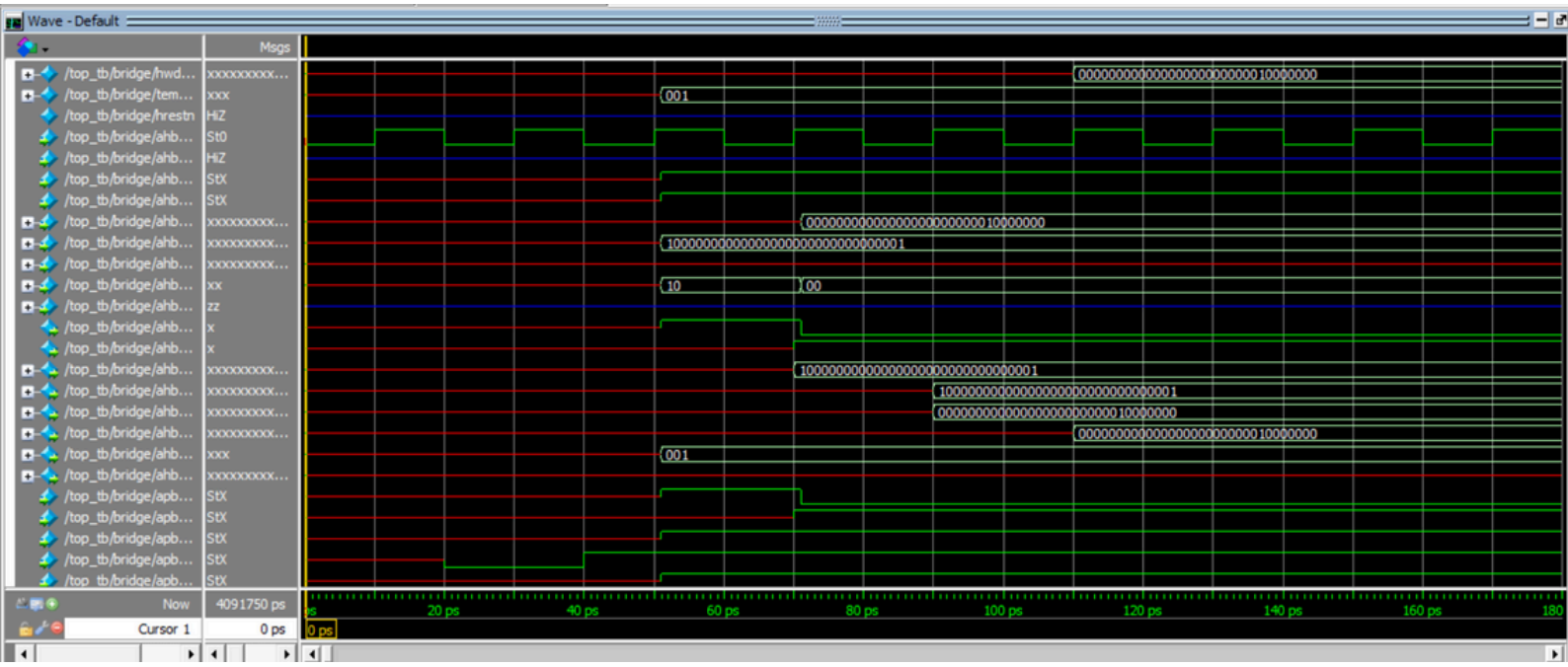
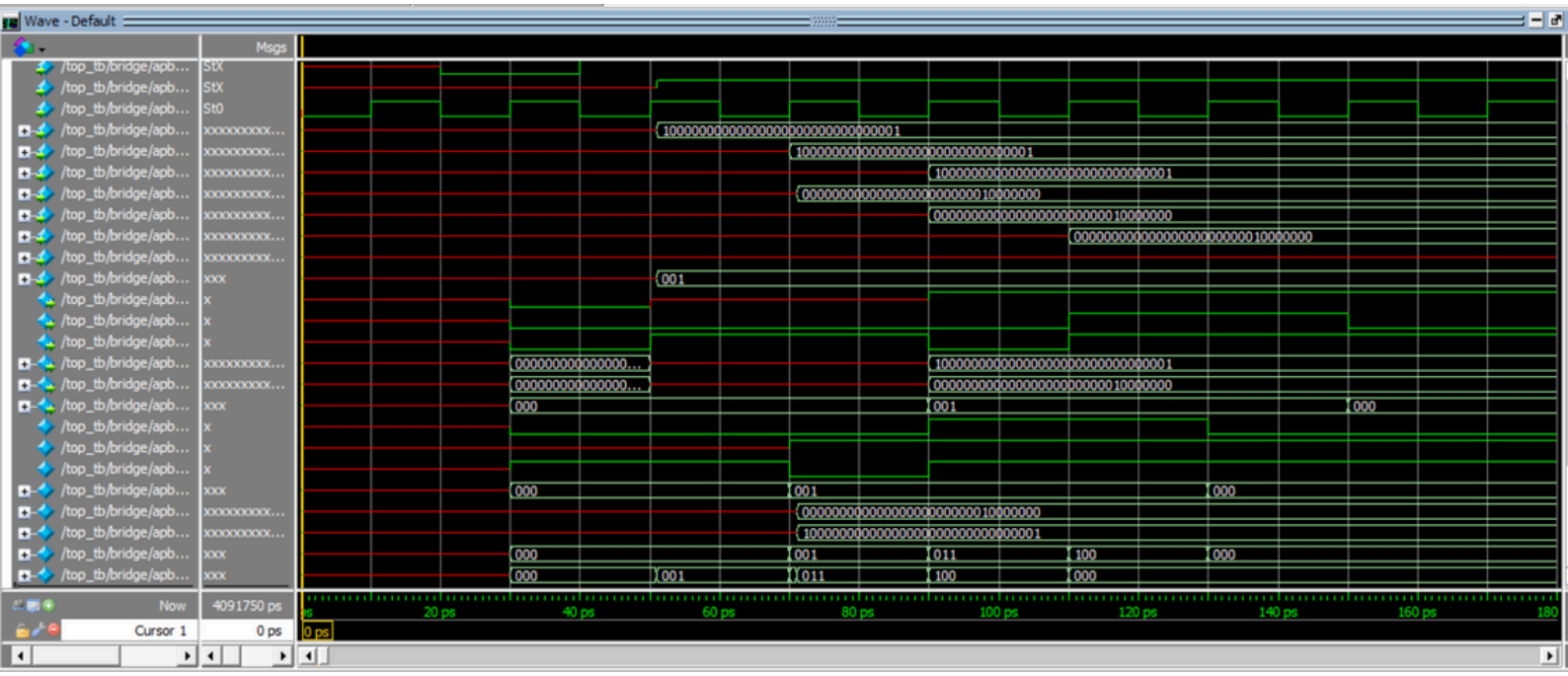
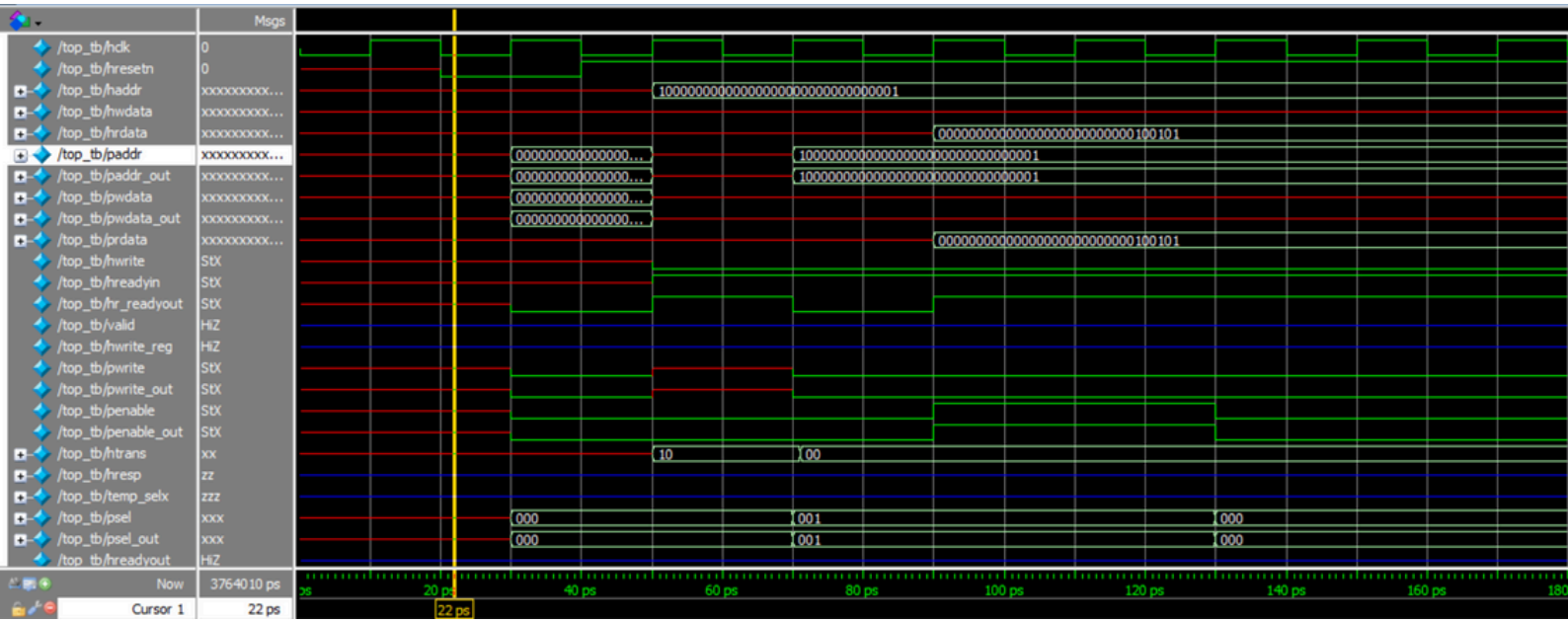
80 ps
100 ps
120 ps
140 ps
160 ps
180
0 ps





3) Single_Read


Msgs
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/top_tb/hresetn
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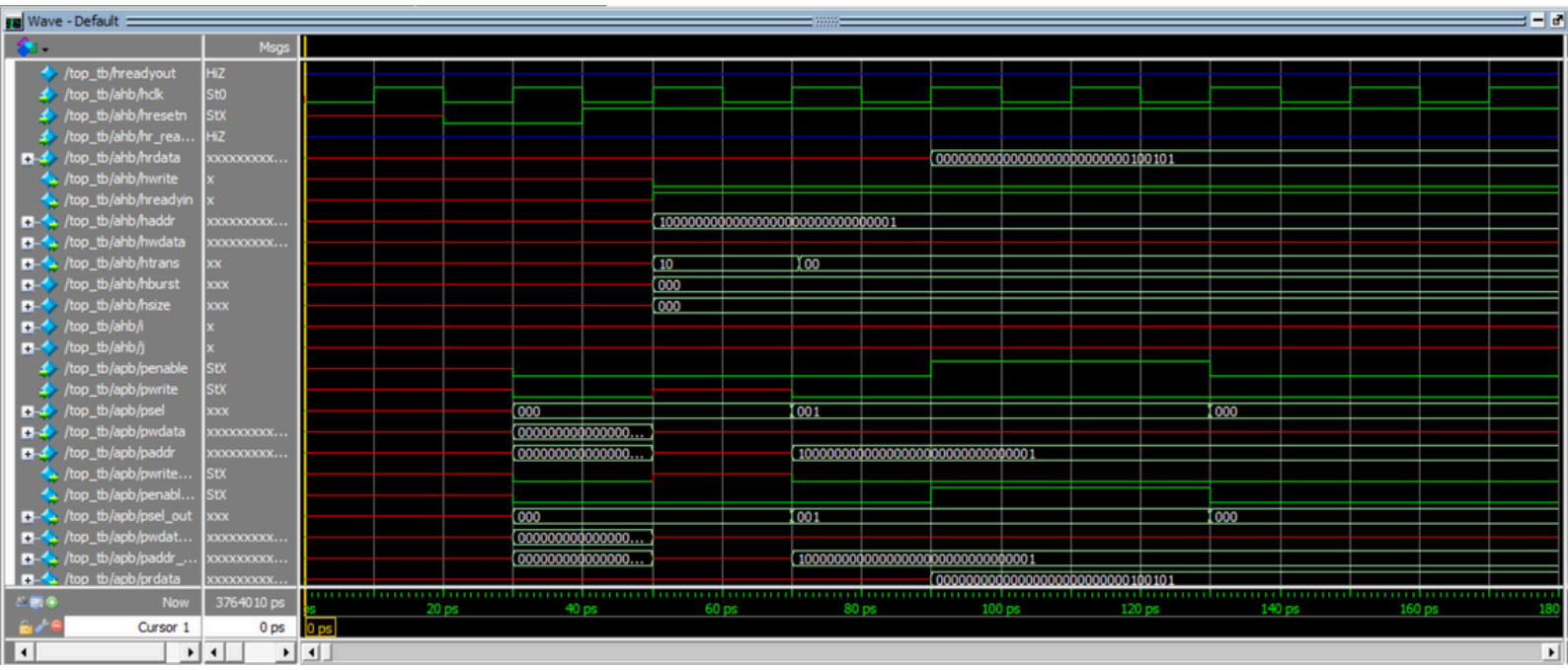
/top_tb/hrdata
/top_tb/paddr
/top_tb/paddr_out
/top_tb/pwdata
/top_tb/pwdata_out
/top_tb/prdata
/top_tb/hwrite
/top_tb/hreadyin
/top_tb/hr_readyout
/top_tb/valid
/top_tb/hwrite_reg
/top_tb/pwrite
/top_tb/pwrite_out
/top_tb/penable
/top_tb/penable_out
/top_tb/htrans
/top_tb/hresp
/top_tb/temp_selx
/top_tb/psel
/top_tb/psel_out
/top_tb/hreadyout
Now
3764010 ps
Cursor 1
22 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps


Wave - Default
Msgs
/top_tb/hreadyout
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/top_tb/ahb/hresetn
/top_tb/ahb/hr_rea...
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/top_tb/ahb/hreadyin
/top_tb/ahb/haddr
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/top_tb/apb/penable
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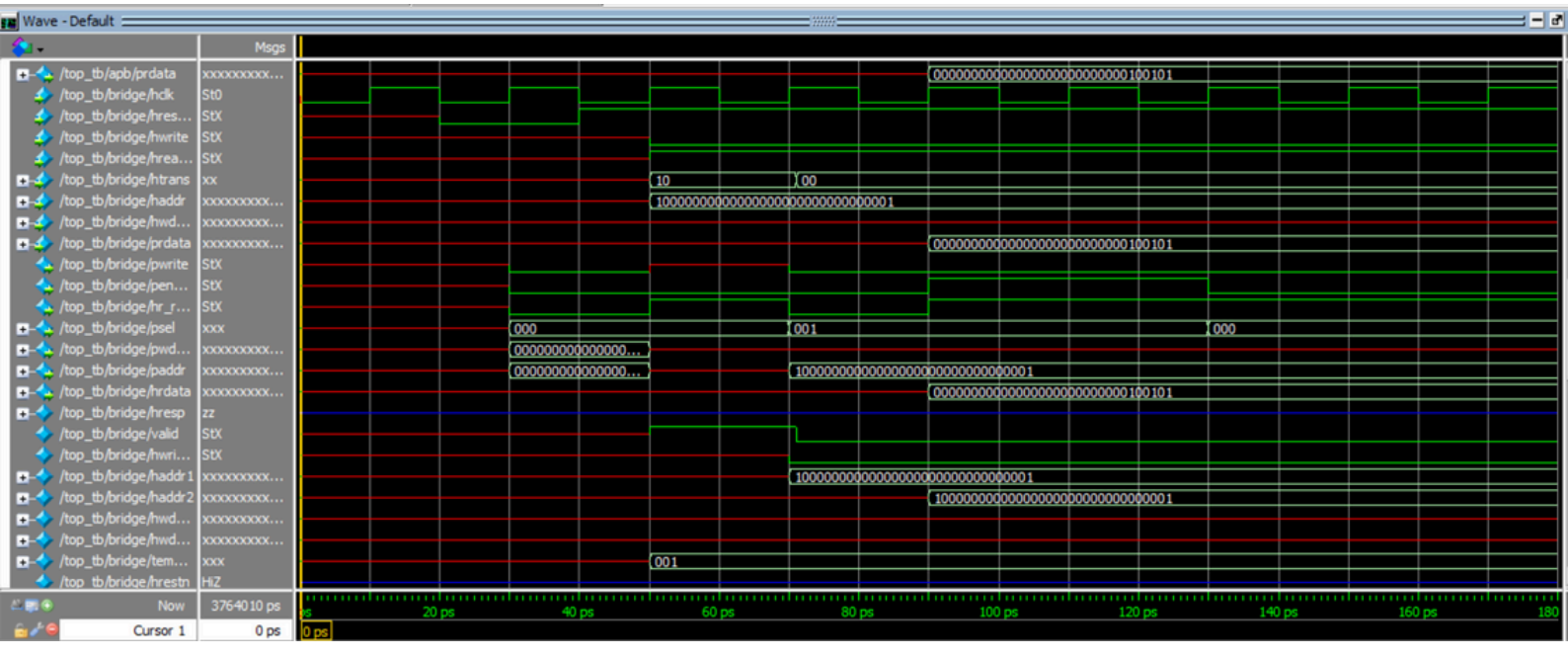
/top_tb/apb/pwrite...
/top_tb/apb/penabl...
/top_tb/apb/psel_out
/top_tb/apb/pwdat...
/top_tb/apb/paddr_...
/top_tb/apb/prdata
Now
3764010 ps
Cursor 1
0 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps


Wave - Default
Msgs
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/top_tb/bridge/hwrite
/top_tb/bridge/hrea...
/top_tb/bridge/htrans
/top_tb/bridge/haddr
/top_tb/bridge/hwd...
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/top_tb/bridge/pwrite
/top_tb/bridge/pen...
/top_tb/bridge/hr_r...
/top_tb/bridge/psel
/top_tb/bridge/pwd...
/top_tb/bridge/paddr
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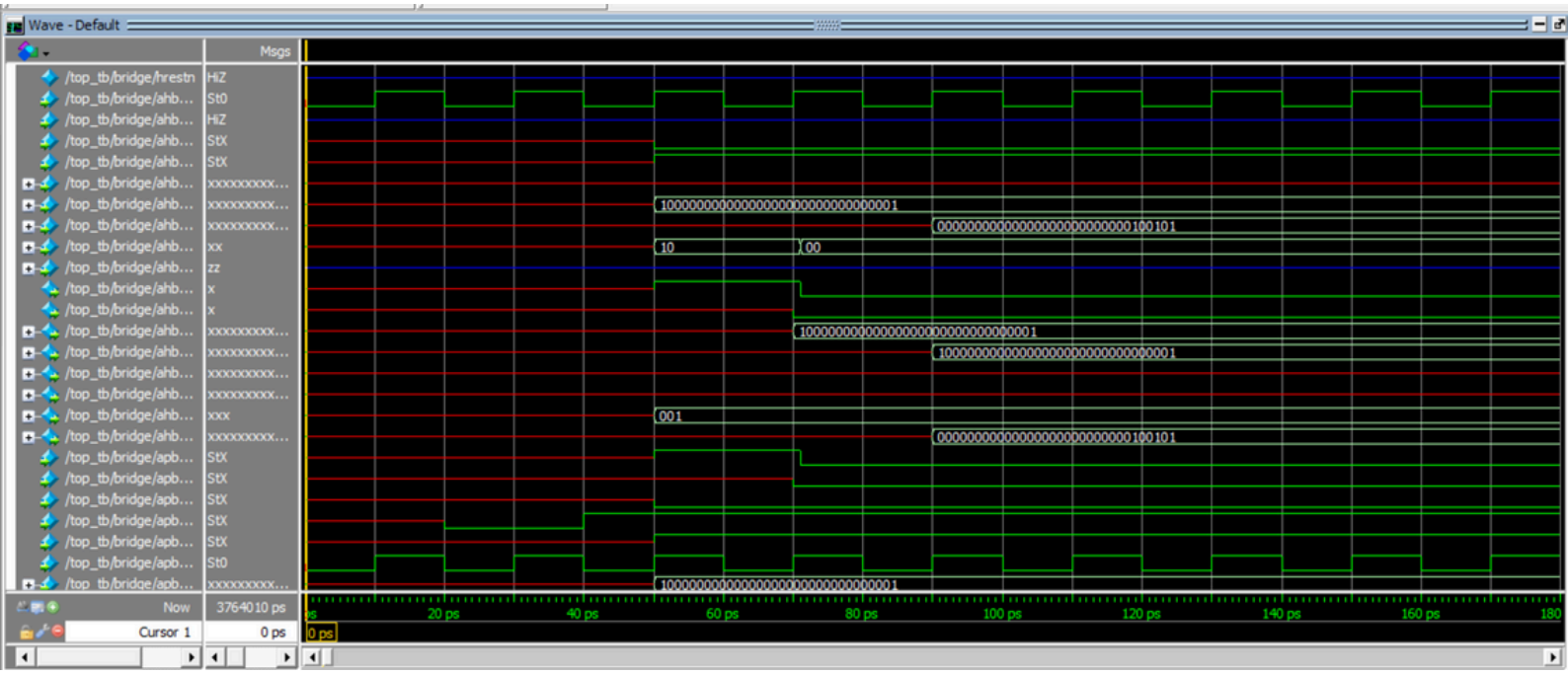
/top_tb/bridge/hwri...
/top_tb/bridge/haddr1
/top_tb/bridge/haddr2
/top_tb/bridge/hwd...
/top_tb/bridge/hwd...
/top_tb/bridge/tem...
/top_tb/bridge/hrestn
Now
3764010 ps
Cursor 1
0 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps


Wave - Default
Msgs
/top_tb/bridge/hrestn
/top_tb/bridge/ahb...
/top_tb/bridge/apb...
HiZ
St0
StX
xxxxxxxxx...
xx
zz
x
xxx
10000000000000000000000000001
00000000000000000000000100101
10
00
001
Now
3764010 ps
Cursor 1
0 ps
20 ps
40 ps
60 ps
80 ps
100 ps
120 ps
140 ps
160 ps
180