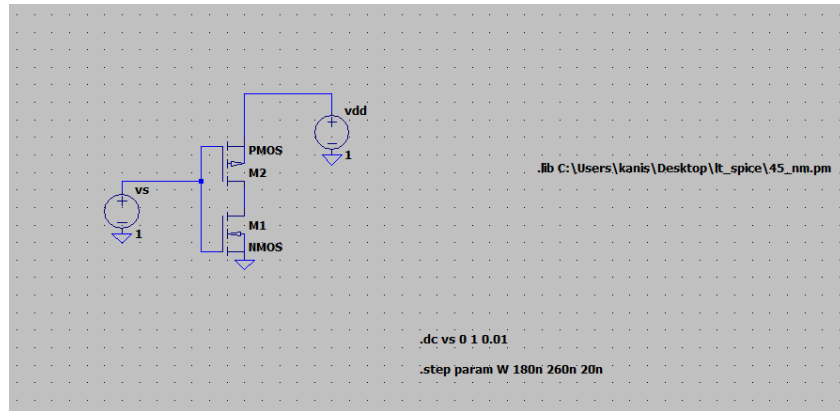


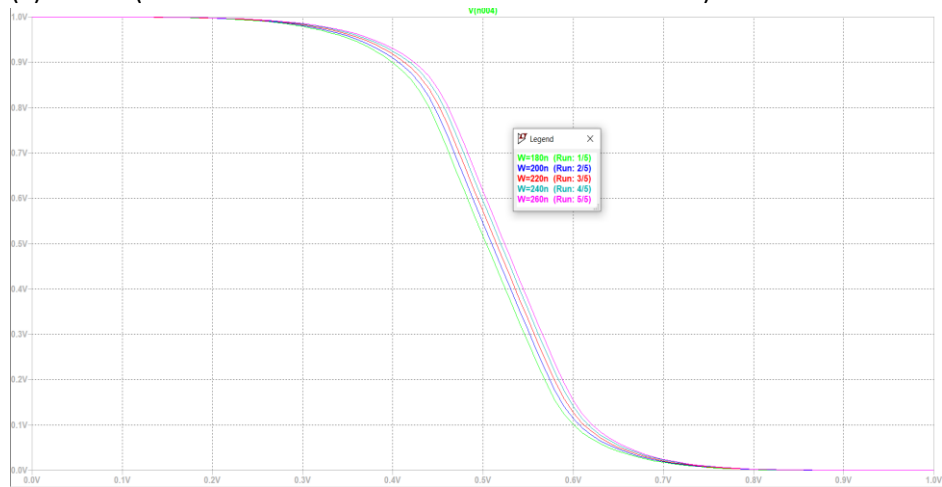
1) INVERTER gate using Static CMOS logic



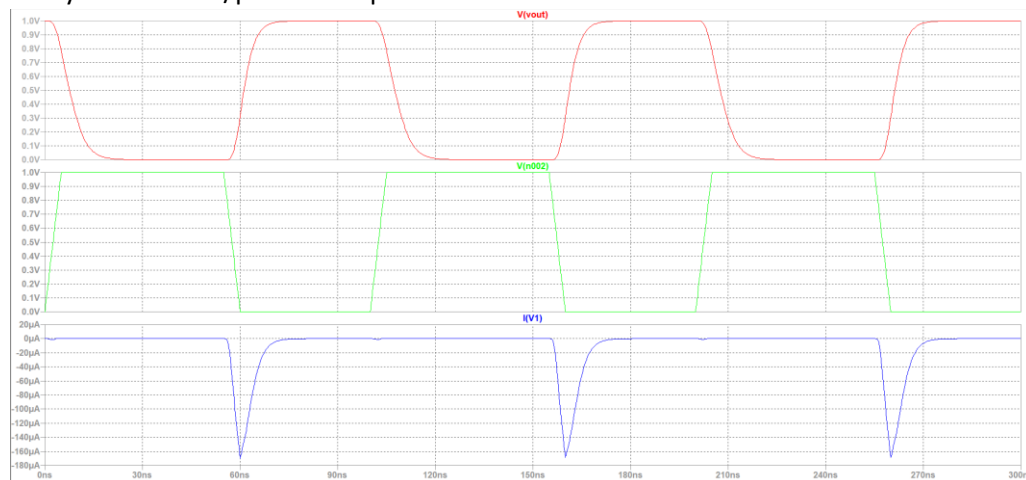
Schematics

(1) VTC

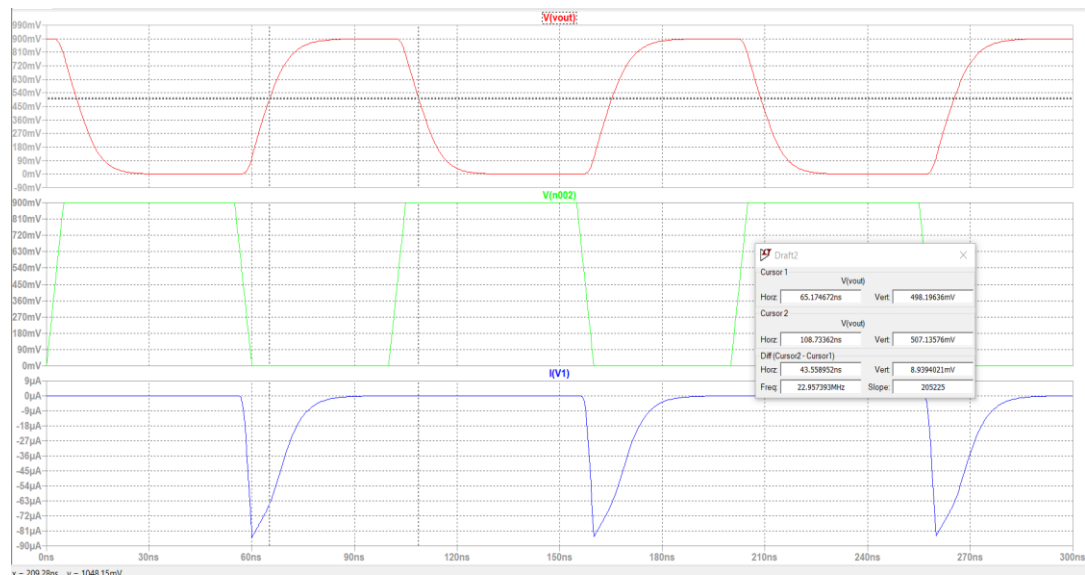
(a) 45nm (width of PMOS is varied from 180nm to 260nm)



(2) Delay calculations/power dissipation



45nm



32nm

(a) Observation and Calculation

$C_{load}=1pF$

Output Delay= $(T_{lh} + T_{hl}) / 2$

Power Dissipation= $V_{dd} * I_{D(avg)}$

- 45nm Technology

$T_{lh}=3.9445ns$

$T_{hl}=1.38ns$

$T_{avg}=2.66ns$

$I_{avg}=10.078\mu A$

- 32nm Technology

$T_{lh}=5.705ns$

$T_{hl}=5.402ns$

$T_{avg}=5.553ns$

$I_{avg}=8.992\mu A$

Node	$T_{pHL}(ns)$	$T_{pLH}(ns)$	$T_{delay}(ns)$	$P=V_{dd} * I_{avg}(\mu W)$
45	1.38	3.9445	2.66	10.0178
32	5.402	5.705	5.55	8.0928

NAND and NOR gate using Static CMOS logic

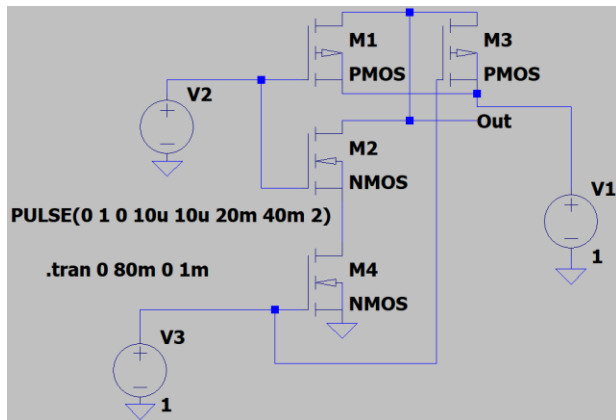
Schematic:

NAND
R

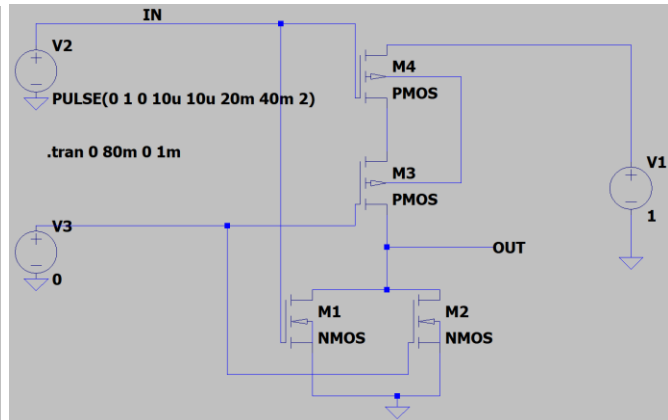
NO

2) NAND and NOR gate using Static CMOS logic

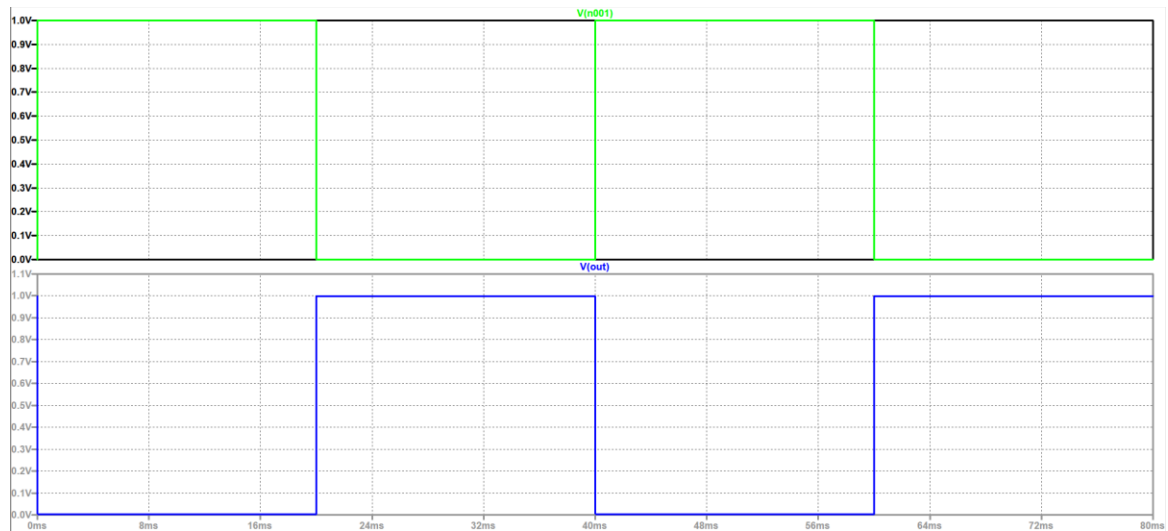
NAND GATE



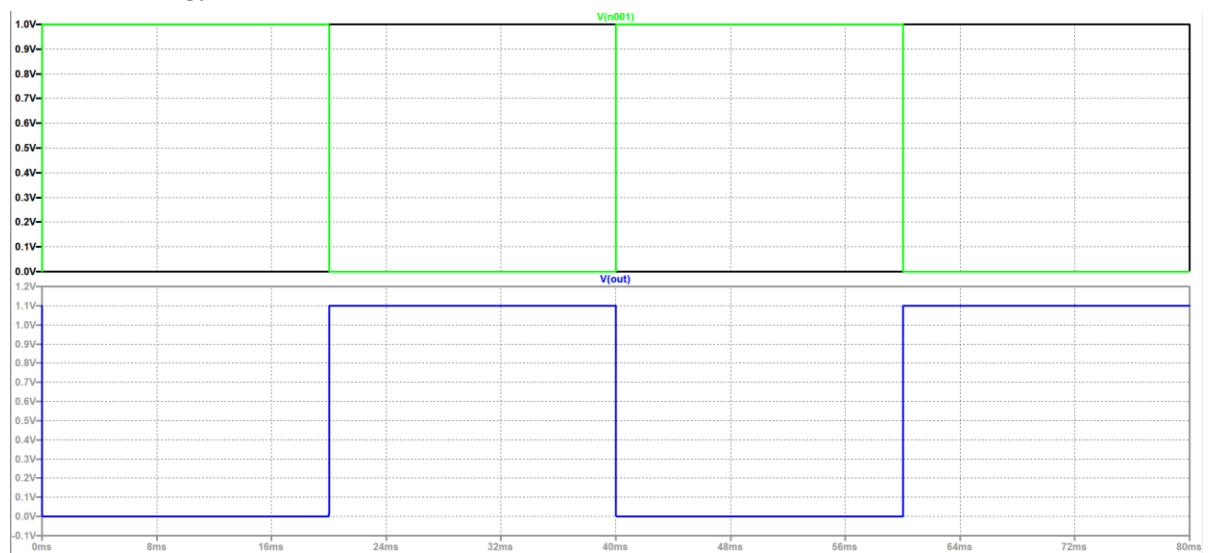
NOR GATE



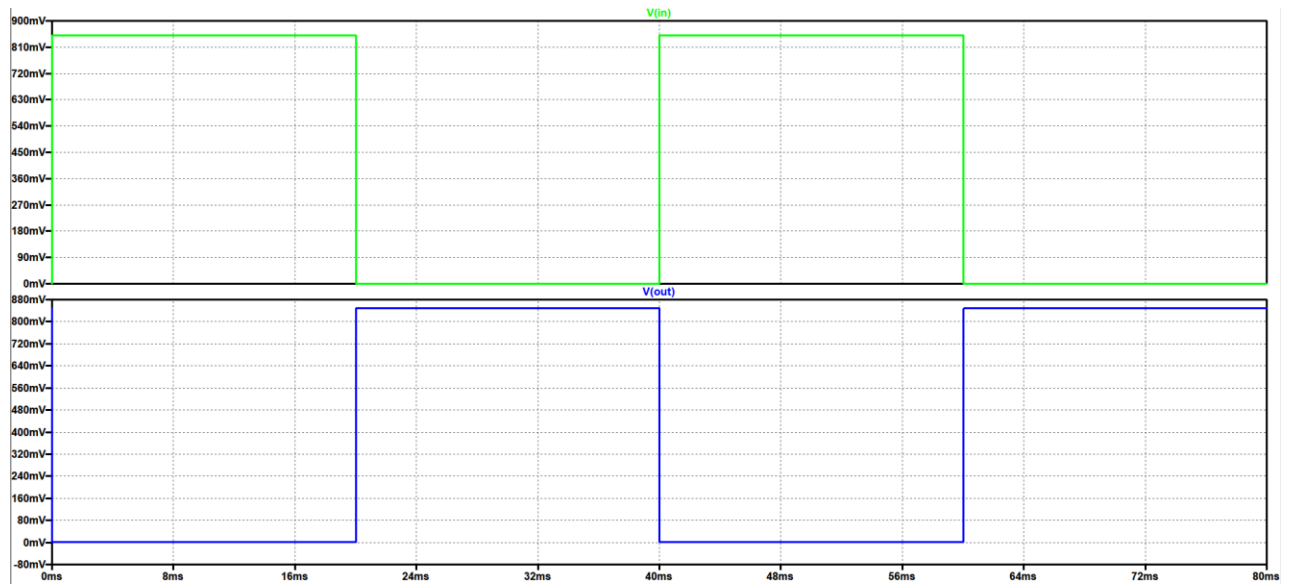
- 32nm Technology



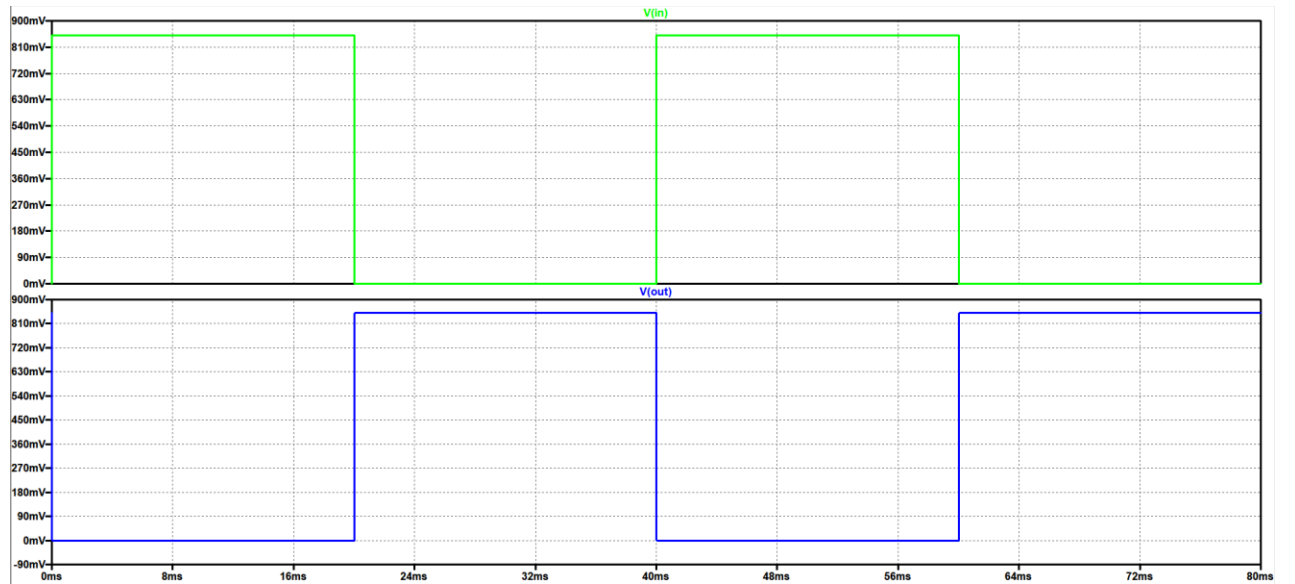
- 45nm Technology



- 32nm Technology



- 45nm Technology



Observations and Calculations:

Formulas Used:

- Output Delay= (T_{lh} + T_{hl}) / 2
- Power Dissipation= $V_{dd} * I_{D(avg)}$

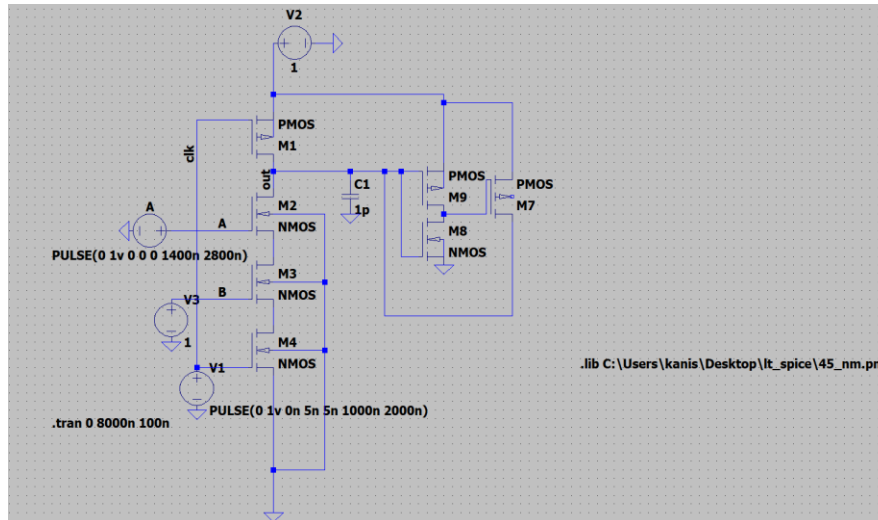
NAND

Technology	T _{lh}	T _{hl}	Output Delay	I _{D(avg)}	Power Dissipation
45 nm	54.649123ns	1.5113573ns	28.08024015ns	48.031nA	48.031nW
32 nm	6.2516376ns	3.65781ns	4.9547238ns	297.19pA	297.19pW

NOR

Technology	T _{lh}	T _{hl}	Output Delay	I _{D(avg)}	Power Dissipation
45 nm	82.2584 ns	29.9875 ns	56.12295 ns	147.96nA	147.96nW
32 nm	33.41985 ns	17.568 ns	25.493925 ns	27.047nA	27.047nW

3) NAND and NOR gate using Dynamic logic (45nm)



NAND gate

Observations and calculations

Formulas Used:

- Output Delay= (T_{lh} + T_{hl}) / 2
- Power Dissipation= V_{dd} * I_{D(avg)}

- 45nm

$I_{D(avg)} = 5.6215\mu A$

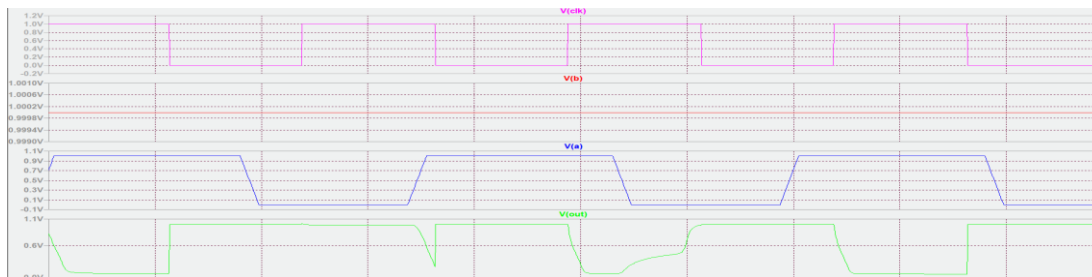
Power Dissipation = $5.6215\mu W$

$T_{lh} = 0ns$

$T_{hl} = 5.9301 - 5.90250\mu s = 27.6ns$

$T_{avg} = 13.8ns$

45nm



- 32nm

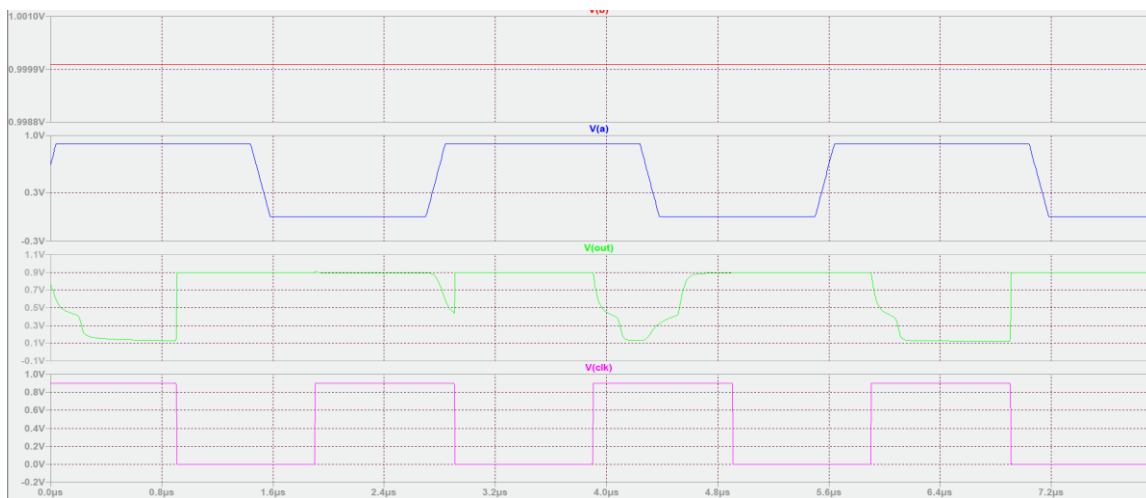
$I_{D(avg)} = 8.694\mu A$

Power Dissipation = $7.8246\mu W$

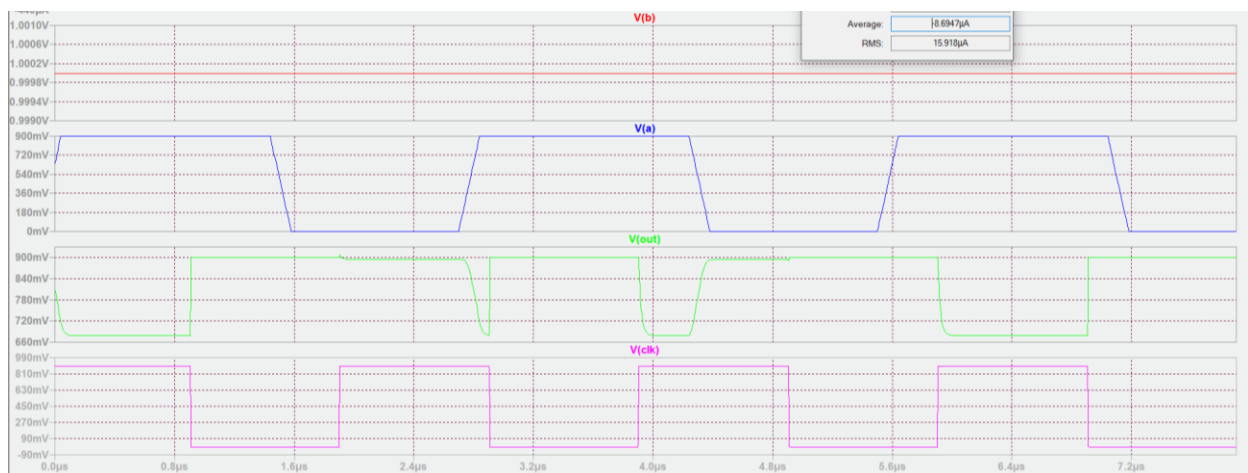
$T_{lh} = 0ns$

$T_{hl} = 4.9602637\mu s - 4.9077753\mu s = 52.5ns$

$T_{avg} = 26.25ns$

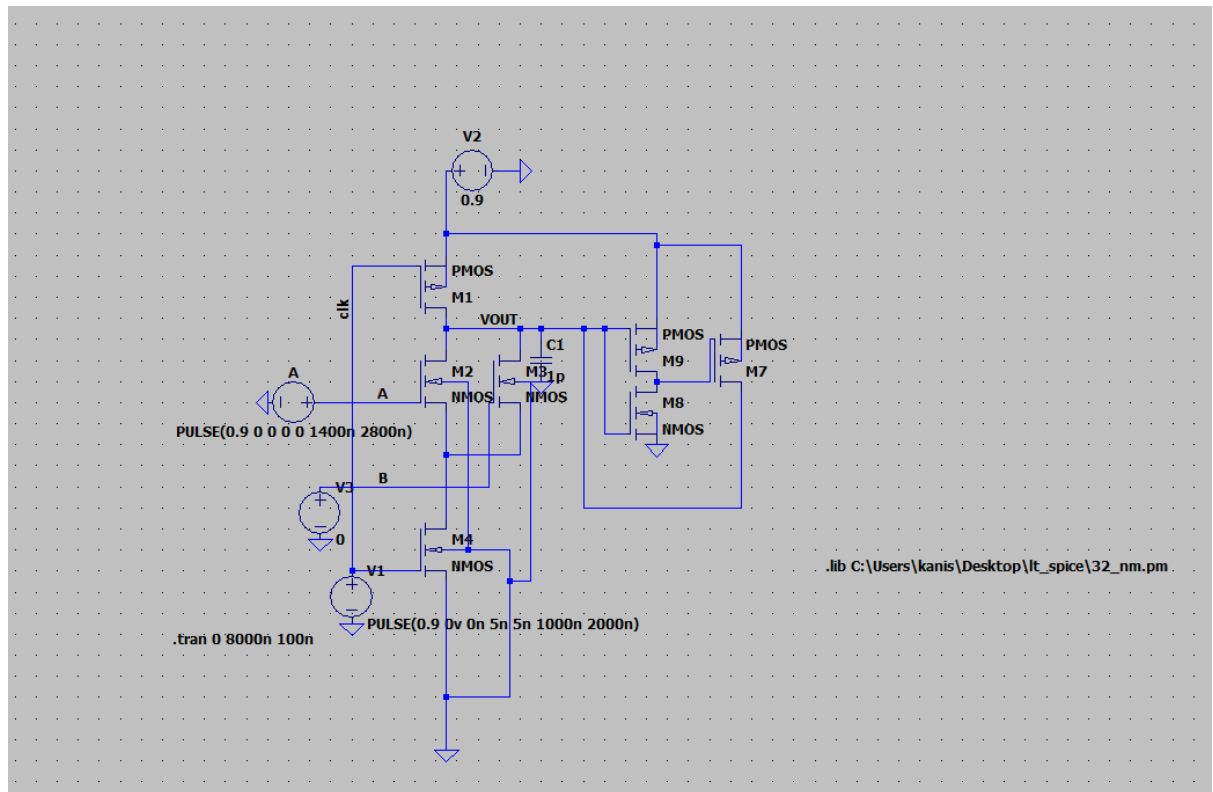


Bleeder circuit week

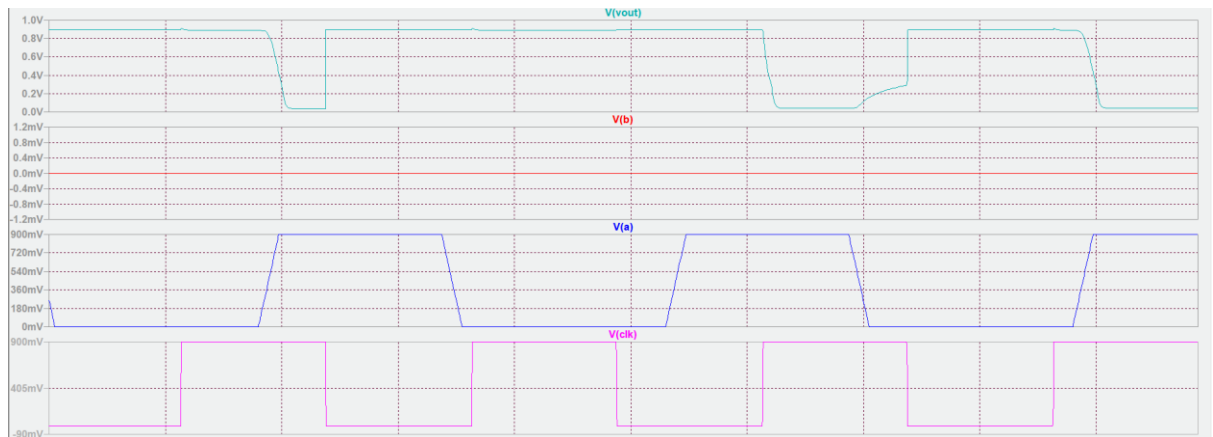


Bleeder circuit strong

NOR GATE



• 32nm



$$I_D(\text{avg}) = 2.4823 \mu\text{A}$$

$$\text{Power Dissipation} = 2.234 \mu\text{W}$$

$$T_{lh} = 0\text{ns}$$

$$T_{hl} = 4.9602637 \mu\text{s} - 4.9077753 \mu\text{s} = 32.5\text{ns}$$

$$T_{avg} = 16.25\text{ns}$$