Yashash Jain

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EDUCATION

IISc Bangalore
MTech in Microelectronics And VLSI Design
Aug 2021-Present | Bangalore, India
GPA: 8.5 / 10.0 (3 semesters)

IIIT Kota
BTech in Electronics and Communication
2017-2021 | Jaipur, India
CGPA: 9.41 / 10.0

COURSEWORK

Academic
Digital VLSI Circuits
Analog VLSI Circuits
Digital System Design with FPGAs
Efficient and Secure Digital System

Online
Digital IC Design
Hardware Modeling using Verilog

SKILLS

Programming:
C, Verilog, VHDL, LaTeX

Tools:
Vivado (Xilinx), Virtuoso (Cadence), MATLAB, LTspice, Sentaurus

Hardware:
Basys 3 FPGA Board, Arduino

CERTIFICATIONS

Cloud Based Analog IC Design Hackathon [link] [report]
Feb'22 – Mar'22 | IIT Hyderabad

Virtual Summer Internship at CPDM, IISc [link] [report]
Jun'21 – July'21 | IISc Bangalore

HOBBIES

Teaching
Sketching
Swimming
Playing Table Tennis

PROJECTS

Hardware Accelerator for Probabilistic Computing | Verilog | FPGA
Jun 2022 - Jun 2023 | M.Tech Project
Under the guidance of Prof. Utsav Banerjee, We designed and implemented of a configurable hardware accelerator for probabilistic computing to solve optimization and factorization-related problems. [Slides]

ASIC Implementation of Neural Network | Verilog | Cadence
Oct 2021 - Dec 2021 | Course Project
Implemented an ASIC (using cadence tools) for classification of hand-written digits using extreme learning machine (ELM) based neural network architecture written in verilog. Doing full RTL to GDSII flow. [Slides]

RTL Design for 32-bit RISC-V Processor | Verilog | FPGA
Aug 2022 - Nov 2022 | Course Project
Designed a single-cycle risc-v cpu with fixed instruction length. Further extended single-cycle path to design a multi-cycle path and five stage pipeline that supports the same instructions at a higher frequency. [Slides]

Sine Waveform Generator using CORDIC Algorithm | VHDL | FPGA
Feb 2022 - Apr 2022 | Course Project
FPGA implementation of sine waveform generator (for variable frequency) based on 12 stages pipelined CORDIC (COordinate Rotation DIgital Computer) algorithm. [Slides]

Smart Soldier Strap - A Helping Hand | Arduino | IoT
Feb 2020 - Jan 2021 | B.Tech Project
A Compact smart embedded device was developed, which senses vital body parameters and real-time tracking of soldiers using IoT. All information is wirelessly communicated through low power LoRa module. [Slides]

PUBLICATIONS

[1] Jain, Yashash, et al. "Novel wearable device for health monitoring and tracking of soldiers based on LoRa module." 2020 IEEE 4th Conference on Information Communication Technology (CICT). IEEE, 2020. [Paper]

ACCOLADES AND RECOGNITIONS

2021	GATE AIR 46	Electronics & Communication Stream
2021	Institute Gold Medal	College topper in BTech (ECE)
2020	Publication	Published paper in IEEE conference
2020	5^{th} position	Hacksagon competition, IIIT Gwalior
2019	Completed all tasks	e-Yantra robotics competition, IIT Bombay
2019	First runner up	Lawn Tennis sports tournament, IIIT Kota

POSITION OF RESPONSIBILITIES

1. Teaching Assistant in the course "Digital VLSI Circuits", IISc Bangalore.
2. Organise career guidance sessions in government schools.
3. Student Representative of IIIT Kota.
4. Captain of Table Tennis Sports Team, IIIT Kota.
5. Team Leader in e-Yantra Robotics and HACKSAGON Competition.