PERGAMON

Microelectronics Reliability 42 (2002) 1617–1622

MICROELECTRONICS RELIABILITY

www.elsevier.com/locate/microrel

Fast thermal fatigue on top metal layer of power devices

Sebastiano Russo, Romeo Letor, Orazio Viscuso, Lucia Torrisi, Gianluigi Vitali

STMicroelectronics, DSG Group, Stradale Primosole 50, 95121 Catania, Italy

Abstract

The paper deals with the analysis and the study of rapid temperature variation effects on metal surface of Vipower devices. These Nmos-Dmos smart power mosfets are substituting relays on automotive applications.

Their particular characteristics of thermal/max current protection, in overload and/or short circuit condition produce temperature variation/gradients (measured by computer aided radiometric techniques), which, if repeated periodically, generate some fatigue effects on surface metallization. Scaling technologies and consequently increasing specific power level arise these phenomena (included in Failure Mode category predictable by COFFIN-MANSON model) as a new failure mechanism that needs a life time prediction and assurance criteria .

1. Introduction

The increasing demand of smart Power MOSFET in automotive applications as a replacement of electro mechanical relays, have highlighted the need to specify the reliability of these devices in terms of switching cycles with well defined working conditions.

1.1 Smart Power MOSFET and application related thermal transients.

The interaction of IPS (intelligent Power Switch) electrical characteristic with the load determines the entity of the power dissipation.

The IPS shown in Fig. 1 is made using the M0 technology that integrates a power MOSFET with vertical current flow and its control part in a monolithic chip solution (see Fig. 2). To comply with automotive requirements this class of devices includes several protections.

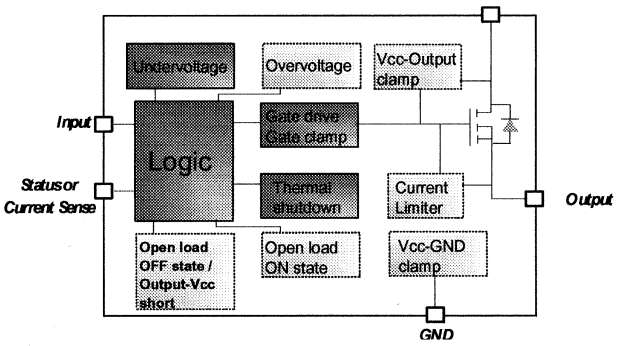


Fig. 1. Functional block diagram of an IPS

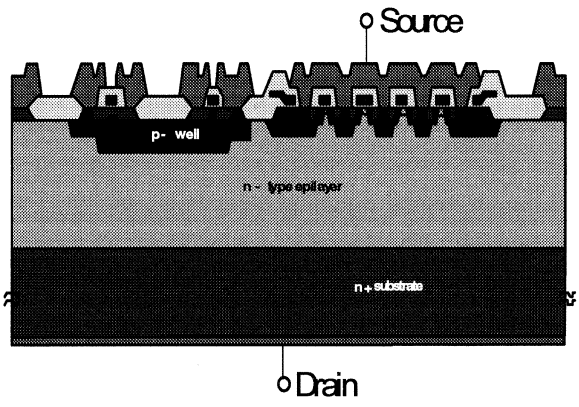


Fig. 2. Structure of a monolithic IPS made with M0 technology

0026-2714/02/$ - see front matter
PII: S0026-2714(02)00200-7

1.2 Short circuit protection

A current clamp combined with thermal shut down intervention avoids device failure during a short circuit operation. The integrated current feedback fixes the working point in the active area of the IV characteristics of the Power stage. The power dissipation equal to battery voltage multiplied by Drain current leads to a fast increase of the temperature detected by the thermal sensor and consequently to the intervention of thermal shut down block. In this condition the thermal sensor temperature variation rate is higher than 50°C/ms. The short circuit operation shown in Fig. 3 puts in

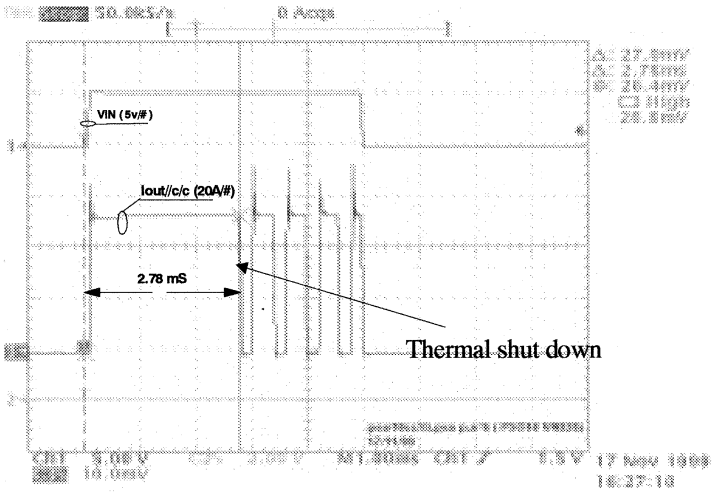


Fig. 3 Short circuit operation of an IPS

evidence that the temperature of the thermal sensor reaches thermal shut down temperature in few ms, which is the intervention time of the short circuit protection.

1.4 Thermal characteristics

The above-described power is dissipated inside the DMOS channel. As a consequence the heat propagates instantaneously inside the source aluminum surface. This concept is reinforced with the thermal model showed in Fig. 4. In fact the thermal capacitance and the thermal resistances of the layer, where the major power dissipation occurs, are one order of magnitude smaller respect to the lower values included in the model.

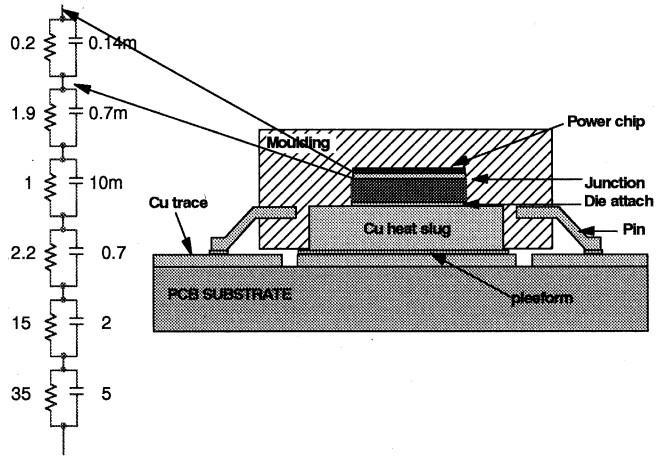


Fig. 4. Device schematic structure and equivalent thermal model

This is also demonstrated with direct measurement of the thermal transient on the device surface using the equipment described in the next paragraph (Fig. 5).

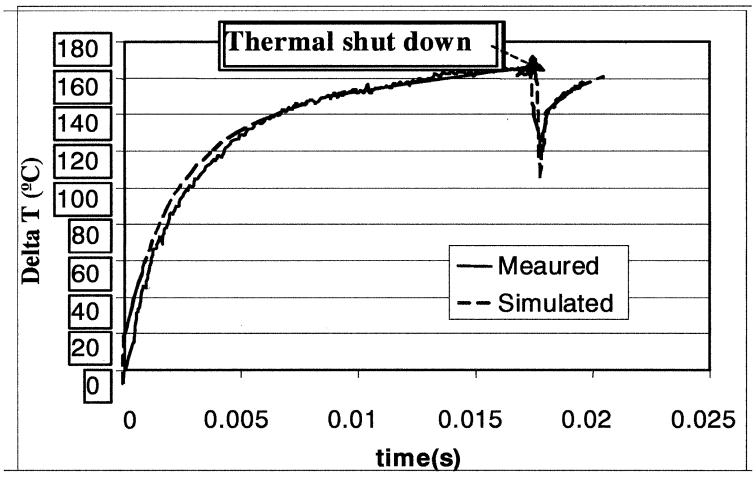


Fig. 5. Temperature measured on the device surface compared with a simulation obtained using the thermal model of figure 4.

1.5 Driving automotive incandescent lamp.

The inrush current of an incandescent lamp is around 10 time its nominal value. The selection criterion of the IPS must take in account the extra power dissipation due to the inrush current. For example, if the IPS limits the current below the inrush current, the device will work in the active area during each cold lamp turn on. The resulting power dissipation on the Power MOSFET can induce a relevant thermal transient and impact of the reliability of the switch Fig. 6 shows the behaviour of the IPS VND810SP when the device turns on a 21W

lamp. This device limits the current at 5A while the inrush current of the lamp is around 18A.

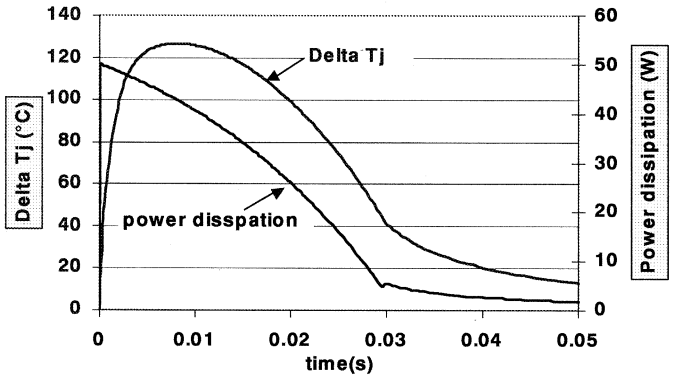


Fig. 6. Behaviour of power dissipation and of junction temperature on the IPS VND810SP driving a 21W lamp.

2. Computer aided radiometric measurement

The thermal mapping system consists of a "Barnes" radiometric microscope cooled by liquid nitrogen, a micromanipulator with thermostatic holder plate (using Peltier cells) driven by a computer where a mapping software was installed, a power supply and a signal generator. The device (VND810SP) under mapping has been mounted on a FR4 substrate (4x4cm) and subsequently decapsulated (epoxy resin removal) up to the surface of the chip.

2.1 Measurement

The D.U.T. on the above conditions has been positioned on the thermostatic holder of the equipment (set at 20.5°C). Measurement cycle consists of a sequence of stimuli on the device set in short circuit condition (T=1 sec , Duty cycle=2%, Vin=4.5V, Vdd=10.1V). In particular, a matrix of 18x13 metal elements (MEXEL) has been defined on a part of the chip surface including bonding area. Each element had dimension 100x100μm. For each MEXEL the device has been stimulated 5 times and the relevant radiometric waveforms (see Fig. 5) stored in computer. In these conditions, at the end of the test the device has been submitted at 13x18x5=1170 cycles of short circuit. This high number of stress cycles generates fatigue effect on the metal surface (see Fig. 10).Thermal map obtained after computing of all stored data shows a very high radiance gradient between pad area and edge of the power region (see Fig. 7, Fig. 8).

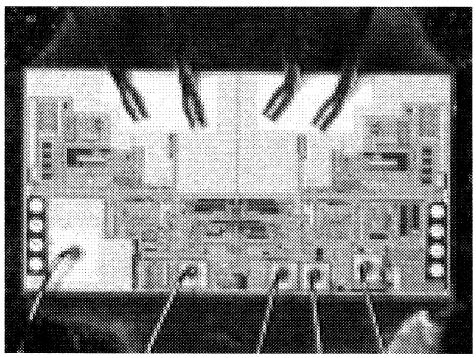


Fig. 7 Top side Dmos area, low side control area

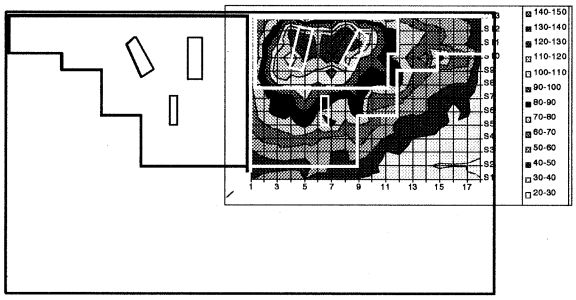


Fig. 8 Isoradiance map on stressed device after 15 msec

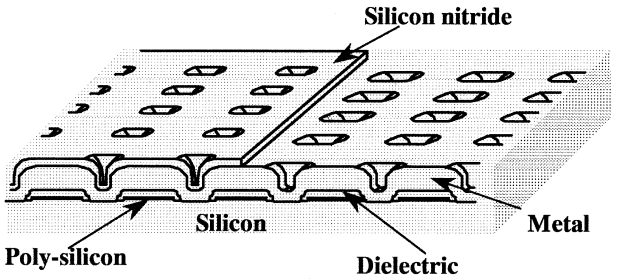


Fig. 9 – Schematic draw of the P-MOS structure, object of the present study. On the left side of the picture the metal layer is protected by PECVD silicon nitride, on the right side no passivation protects the metal because on this area the bonding wires have to be placed.

3. Morphological and failure analysis

The tools used to analyze the Al top metal structure are Optical Microscope, S.E.M. (Scanning Electron Microscopy) and F.I.B. (Focused Ion Beam).

In Fig. 9 we schematically introduce the structure of the object under study in the present work.
On the above structure, from the morphological point of view, we can consider three different cases; the difference consists in three situations of the metal layer of the channel undergoing the electrical pulsed stress. The different situations can be described as following:

a) metal layer electrically stressed without any "constriction" on top (this is the case of the device used for radiometric measurements);

b) metal layer underlying the bonding wires and close to them, electrically stressed inside the package;

c) metal layer electrically stressed inside the package in the regions far from the bonding wires, with passivation layer on top (in this case a PECVD silicon nitride layer is interposed between metal surface and epoxy resin).

For each one of the situations described above we report our comment and experimental observations.

a) In this case we can observe (see Fig. 10) some burning effects close to the bonding wires, which can be considered the simple effect of the flowing current and the consequent thermal effects produced by it. The rapidity of the heat generation (described by the radiance map) produces local fatigue effects which are visible on the Al structure modification.

b) In this case the fatigue effects are distributed on the whole interfacial surface. A variation of the Al crystallographic structure is strongly suspected; unfortunately it hasn't been yet demonstrated (by XRD analysis) due to the very small region to be investigated. We observed – roughly – two phases of the phenomenon:

1) during the former one (which starts when the stress starts, and it's always present) there is only a morphological alteration of the metal layer which shows a marked roughness, visible clearly by optical microscope as a dark metal surface and visible by S.E.M. as micro-cracking in the metal layer (see Fig. 11);

2) during the latter one (which not ever occurs) the phenomenon, generated by a rapid and strongly energetic transient (quasi adiabatic eating) degenerates arising spikes between Aluminum and Silicon; such spikes have been detected, first of all, by leakage current and, in some case, they have been physically individuated by Liquid Crystal, FIB and SEM techniques (see Fig. 12). The evolution from the initial roughness of the metal layer forward to the next spiking can be easily imaged looking at the "cracks" of the Al inside the contact (see Fig. 13).

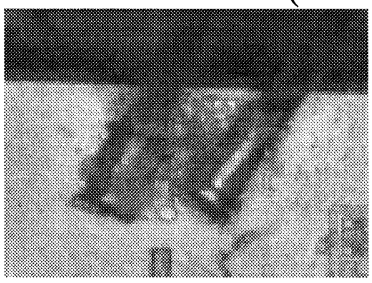
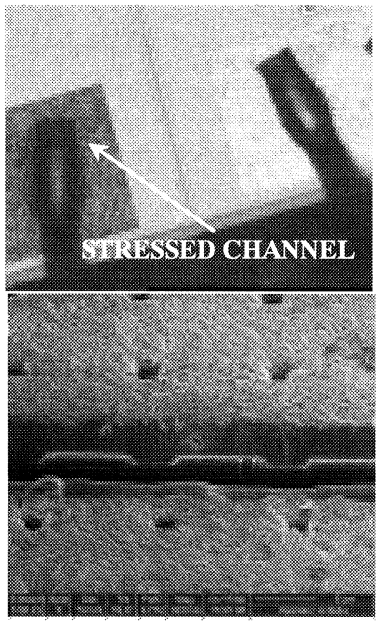


Fig. 10 - Aluminum burning effect, close to the bonding wires, caused by electrical pulsed stress on open die.



(a)

(b)

Fig. 11 - Die stressed inside the package: **(a)** dark metal surface visible by optical microscope on the stressed channel; **(b)** micro-cracking in the metal layer visible by F.I.B./S.E.M.

c) This is the case of a PECVD silicon nitride layer interposed between metal surface and epoxy resin. Despite of the fact the Al layer is a continuous one (because on the Power-MOS

structure – see Fig. 9 – all the sources are contacted only by a big metal plate) the thermal effect, produced by the electrical pulsed stress, doesn't cause either surface roughness or cracking in the bulk of the metal. In Fig. 14 we can see the border (after silicon nitride removal) between metal protected and not protected by *passivation*: the difference in the Al aspect is very clear, both on top and inside the contact.

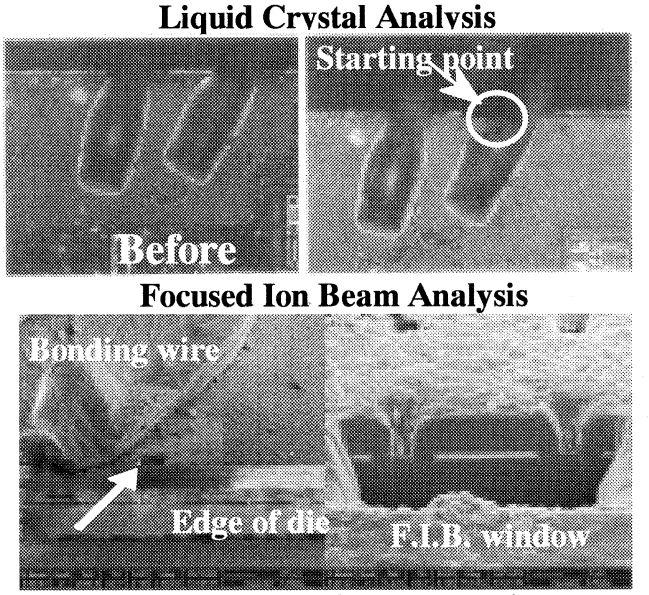


Fig. 12 - Failure analysis (performed by Liquid Crystal, F.I.B. and S.E.M.) on a die stressed on one channel inside the package and affected by high leakage.

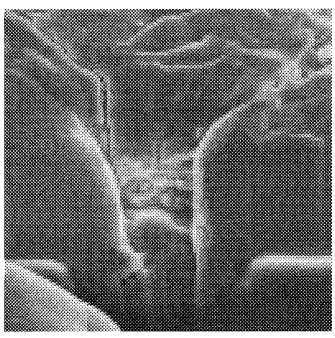


Fig. 13 – Al cracks clearly visible inside a contact close to the bonding wire of a die electrically stressed.

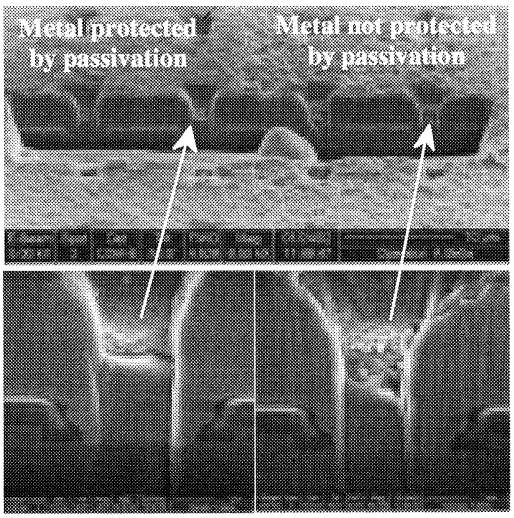


Fig. 14 – F.I.B. section made (after silicon nitride removal) on the border of the "passivated" metal: it's clearly visible the difference, both on the surface roughness and on the cracking inside the contact, of the two regions.

4. Failure mechanism model

A big amount of experimental test data has allowed to fit a life time model and estimate the failure probability in terms of number of cycles at different Delta Temperature relative to a given device technology. The adopted failure criteria have been $\Delta Ron \geq 100\%$ and $\Delta Idss \geq 5\mu A$. The evaluation has been performed by stress a significant number of devices (typically 50 parts for each trial) with different Delta Temperature. The stress test circuit is obtained by connecting a 21W bulb on each output of the VND810SP device (see Fig. 1 for a single channel).
Applying Log-Norm model (90% Confidence Level) we can obtain the estimated Failure Rate related to this level of stress in terms of Delta Temperature (see Fig. 15).

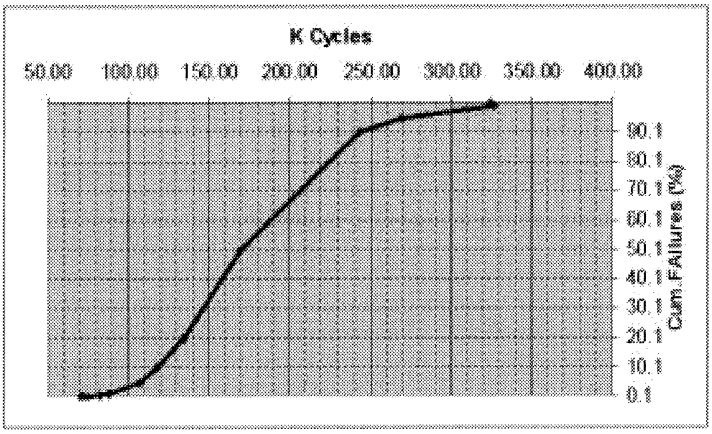


Fig. 15 Estimated failure rate 90% c.l. (log-norm model $\Delta Ron \geq 100\%$ and $\Delta Idss \geq 5\mu A$).

Repeating similar trials by forcing the device with test conditions able to obtain different Delta Temperature, we can correlate the predictable number of cycles to fail at a given Delta Temperature.
As expected, the better model fitting the experimental results is the Coffin-Manson that well predicts the failure due to cracks and material fatigue or deformation relating to cycles of stress or changes in temperature. It is used for solder cracking under the stress of repeated temperature cycling, as an electronic component is powered and not powered.
This model takes the form:
$Nf = A(\Delta T^{-\beta})$ Where
Nf = the number of cycles to a given failure percentage
ΔT = the temperature range
The best fit for A and β are 158.9 and 0.117 respectively.
Starting from the experimental results and applying the Coffin-Manson model, the device initial degradation in terms of number of cycles at the different Delta Temperature can be predicted according to the following curve (see Fig 16).

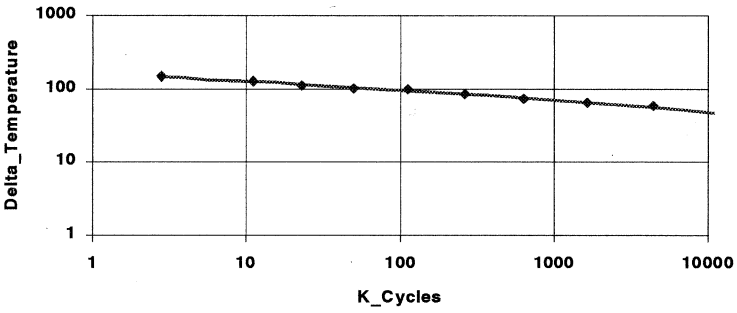


Fig. 16 Lifetime (In-rush cycles vs Delta Temperature)

Observing the fitting model, it is possible to see that the level of Delta Temperature can affect dramatically the number of cycles the device can withstand from some millions to some thousands.
In particular, looking at the curve it's possible distinguish two regions. In fact when the Delta Temperature is less than about 50÷60°C the stress supplied is not able to degrade significantly the device, that does not maintain any memory of the previous stresses it was submitted. Vice versa when Delta Temperature is greater than the a.m. threshold value we can observe a progressive device degradation which is more and more rapid depends on the level of the stress applied.
In fact, depending on Delta Temperature, the degradation can be insignificant or very slow or dramatically rapid. The energy dissipated during repeated switch-on/switch-off can cause progressive changes in materials, especially at interfaces, till to evolve to a crack, in the wire bonding region, that is the final responsible for the failure of the device.

5. Conclusions

An useful model to determine lifetime of the metal layer of a D.U.T. under repetitive high Delta Temperature swing was developed. The empirical analysis of the failure mechanism and the relevant deep structural analysis on stressed devices allowed us to detect the treshold level of safety device operations. This model can be applicable to overall cellular power devices submitted to conditions similar to the above described ones.

Acknowledgements

The radiometric measurements have been performed at "Federico II" Naples University-Electronic department. The used equipment has been developed by a researcher group driven by Prof. P. Spirito.
We would like to thank Mauro Ciappa for his precious suggestion in this paper issuing.
Further thanks to Stefania Gemelli for editing.

References

[1] Paul A. Tobias, David C. Trindade. Applied reliability 2nd edition.Van Nostrand Reinhold.
[2] Landzberg A.H., Norris K.C. Reliability of controlled collapse interconnections. IBM journal of research and development.