Review of SiC MOSFET Based Three-Phase Inverter Lifetime Prediction

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***Abstract*—This paper presents a review on SiC MOSFET based 3-phase inverter lifetime prediction. The inverter-level lifetime prediction flowchart is first illustrated with the system failure rate and system Mean Time to Failure derived which integrate five in-series stresses. An overview of SiC MOSFET power module Physics-of-Failure is then presented. Following it are the step-by-step lifetime modeling comparison and summarization, including power loss analysis, thermal modeling, thermal-mechanical modeling, and damage accumulation modeling. Furthermore, cycle counting algorithms and active power cycling tests specific to SiC MOSFET are discussed. Finally, a detailed system-level thermal profile extraction from SiC MOSFET based 3-phased inverter in the hybrid electrical vehicle application is conducted. The simulation result is consistent with theoretical power loss and thermal equivalent circuit based junction temperature evaluation. Thus it can be used for further system lifetime modeling and the reference for 3-phase inverter based power cycling tests in SPWM mode.**

Keywords—SiC MOSFET; three-phase inverter; lifetime prediction; reliability

I. INTRODUCTION

3-phase inverter systems, applied in wind energy, PV generation and hybrid electric vehicles face randomly fluctuating mission profiles [1]-[4]. Accordingly, due to irregular thermal profiles, the mismatch of the Coefficient of Temperature Expansion causes mechanical stress to bond wire and solder joints, inducing 3-phase inverter systems to malfunction unexpectedly. Thermally induced failure takes a significant percentage of 55% among all sources of failures [5]. Besides, the maintenance cost in high power inverter systems is high, which makes the lifetime prediction important in their continuous, long-term operation. Nowadays with the improvement of gate-oxide lifetime, SiC MOSFET power modules have shown better performance in high power applications compared with traditional Si counterparts [7]-[10]. Besides, with achievable high-temperature tolerance, high efficiency and compact system volume [8], SiC MOSFETs save power loss largely compared with Si IGBTs [11] [12], making them more reliable with longer expected lifetime.

Although many research has been done in the lifetime modeling in high power electronic applications, most of them are concerned with component-level modeling with regard to Si based devices. Some papers have studied the system-level lifetime prediction to decrease the MTTF of the inverters. From topological view, [13]-[15] propose different topologies to increase the system lifetime. Others use Markov reliability model to analyze the lifetime of paralleled devices [16] or paralleled topologies [17] [18]. From the perspective of PWM control, [19] tries to control the switching frequency dynamically with junction temperature swing. [20] compares the impact of power factor dependent DPWM and continuous PWM control on junction temperature to extend the system lifetime. Nevertheless, all the above improvements are rested on qualitative analysis without systematic quantitative lifetime modeling and step-by-step direction of system-level lifetime prediction. [21] gives a quantitative lifetime analysis of a 3-phase inverter. However, only IGBT failures are considered. Besides, not enough comparisons have been made to validate the adopted modeling methods, which weakens the preciseness of the proposed lifetime modeling method. Therefore, this paper serves to give a state-of-the-art review on the lifetime prediction of the SiC MOSFET based 3-phase inverters.

In this paper, a step-by-step flowchart of SiC MOSFET based 3-phase inverter lifetime prediction is first shown in Part II. An overview of SiC MOSEFT module Physics-of-Failure is summarized in Part III. Modeling analysis, cycle counting method comparison and active power cycling tests specific to SiC MOSFET modules are thoroughly presented in Part IV. Finally, a thermal profile extraction based on a hybrid vehicle 3-phase inverter is conducted, which lays a necessary foundation for further system-level lifetime modeling.

II. FLOWCHART OF SIC MOSFET BASED THREE-PHASE INVERTER LIFETIME PREDICTION

Fig. 1 shows the state-of-art flowchart of SiC MOSFET based 3-phase inverter lifetime prediction. There are two ways to get the lifetime curve N_f - ΔT_j, i.e. by modeling and simulation (marked as black solid arrows), or by power cycling verification (marked as red dashed arrows). Here, N_f and ΔT_j are cycles to failure and junction temperature swing respectively. In the flowchart, the yellow square boxes indicate models and profiles related to thermal, mechanical and electrical parameters. While the green diamond shapes indicate the intermediate modeling, analysis, feedback and test procedures. The blue solid arrows indicate the feedback routes.

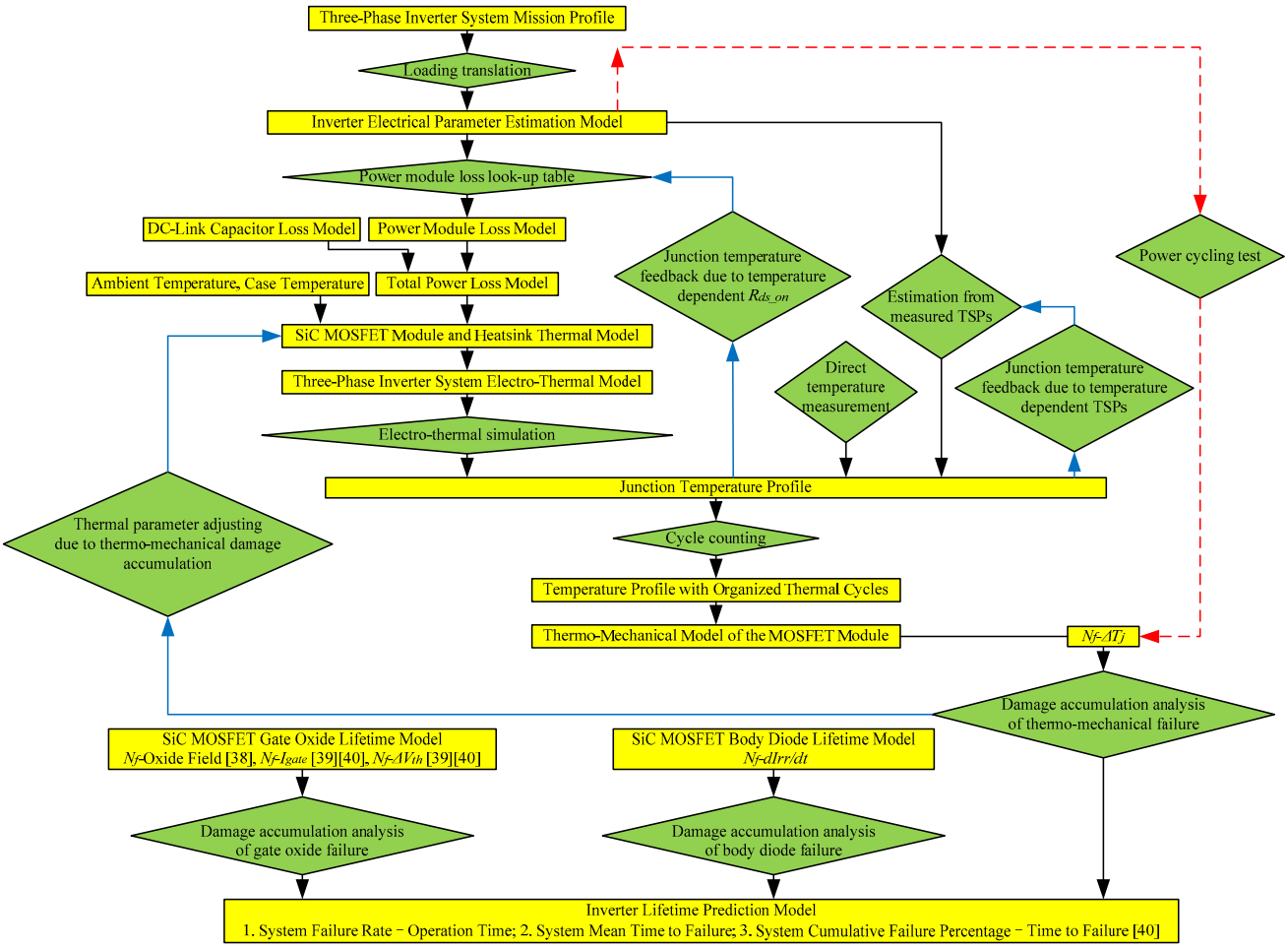

Fig.1 Flowchart of SiC MOSFET based three-phase inverter lifetime prediction

Considering the impact of V_{gs} (gate-source voltage), R_g (gate resistance) on the device power loss [1], gate driver parameters should be included in the Inverter Electrical Parameter Estimation Model. Based on different failure mechanisms, three types of stresses are considered for the system lifetime prediction model, which are junction temperature swing, gate oxide breakdown related and body diode degradation related electrical parameters. In the flowchart, I_{gate}, ΔV_{th}, dI_{rr}/dt are gate leakage current, threshold voltage shift, reverse recovery current change rate, respectively. The reliability function $R_i(t)$ of each individual stress can be approximately characterized by the failure rate $\lambda_i(t)$ with the unit of Failures in Time (FIT) or Failures per billion hours.

Most popular lifetime models for power devices are based on the Exponential or Weibull distribution [6]. Considering the time-dependent failure rate of SiC MOSFET failure modes, Weibull distribution is used here. We define the failure rate of oxide field, I_{gate}, ΔV_{th} induced gate oxide breakdown as $\lambda_1(t)$, $\lambda_2(t)$, $\lambda_3(t)$, respectively, the body diode failure rate as $\lambda_4(t)$ and the thermo-mechanical failure rate as $\lambda_5(t)$. If any of these stress leads to corresponding degradation, the whole system reliability would be affected, which means the stresses can be regarded as in-series. Furthermore, different stresses have unequal contributions to the whole inverter system reliability. For example, junction temperature swing induced thermal degradation takes the largest proportion in the system failure [5]. Thus we define the weight of each of the five stresses as α_1, α_2, α_3, α_4, α_5. According to the statistics of Weibull distribution, the system failure rate $\lambda_{sys}(t)$ is shown in (1).

$$\lambda_{sys}(t) = \sum_{i=1}^{5} \alpha_i \lambda_i(t) \tag{1}$$

The reliability $R_i(t)$ of each stress can be got from (2).

$$\lambda_i(t) = \frac{f_i(t)}{R_i(t)} = \frac{-dR_i(t)/dt}{R_i(t)} \tag{2}$$

Where $f_i(t)$ is the probability density function. Then, the system reliability function $R_{sys}(t)$ is shown in (3):

$$R_{sys}(t) = \prod_{i=1}^{5} R_i(t) \tag{3}$$

System Mean Time to Failure ($MTTF_{sys}$) is shown in (4):

$$MTTF_{sys} = \int_0^{\infty} R_{sys}(t)dt \tag{4}$$

III. SUMMARIZATION OF SiC MOSFET POWER MODULE PHYSICS OF FAILURE

The Physics-of-Failure reliability summarization of SiC MOSFET power modules is shown in Table I. The most frequently encountered failure locations of SiC MOSEFT power modules are gate oxide, body diode, wire bond, chip solder layer and substrate-baseplate solder joint. Although the failure precursors are shown independently, different failure precursors can be the cause and result of each other. For example, the negative bias-temperature stress can result in negative shift of threshold voltage, which induces the increase of leakage current [26]. Besides, when solder fatigue happens, the thermal impedance increases, which causes junction temperature to go up. This in turn results in an increase of drain-source on-state voltage, which indicates another failure mode – wire bond lift-off. Likewise, wire bond lift-off induces uneven current distribution, which generates higher power loss and corresponding higher junction temperature. Hence more thermal stress is put onto the solder interconnections [65].

TABLE I. PHYSICS-OF-FAILURE RELIABILITY SUMMARIZATION OF SiC MOSFET POWER MODULES

PRECURSORS	CAUSE	MECHANISM	CRITERIA	MODE/LOCATION
Gate leakage current I_{gate} [22]-[24]	Thinner gate oxide → higher electric field across oxide under High Temperature Reverse Bias (HTRB) stress	Gate oxide breakdown → gate leakage current	Larger than five times the initial value [22] [30]	Gate failure/ Gate oxide
Gate threshold voltage shift ΔV_{th} [25]-[29]	High Temperature Gate Bias (HTGB) stress	Charge trapping and de-trapping at SiC/SiO_2 interface	Above 20% Maximum of the initial voltage [30] [92]	
Body diode reverse recovery current variation rate dI_{rr}/dt [31]-[33]	1. Low carrier lifetime 2. Thin Epitaxial drift layer 3. Basal-plane dislocations	High dV/dt of body diode coupled with parasitic drain-to-body capacitance → body current I_{rr}	No specific failure criteria can be found	Body diode failure/ Body diode
Drain-source on-state voltage V_{ds_on} [34]-[37]	Stress level much higher than wire bond's strain level	High junction temperature → increase of V_{ds_on}	V_{ds_on} increases by 5% ~ 20% [34]	Wire bond lift-off/ Wire bond
Junction-case thermal resistance R_{th_jc} [34]	Uneven current distributions at solder joints	Crack propagation → increase of thermal impedance	R_{th_jc} increases by 10% ~ 20% [34]	Solder fatigue/ Chip solder layer, substrate-baseplate solder joint

TABLE II. COMPARISON AMONG POWER MODULE AND HEATSINK THERMAL MODELING METHODS

THERMAL MODELING METHODS	ADVANTAGES	DISADVANTAGES	SOURCES
Time-domain Thermal RC Network	Instantaneous junction temperature can be estimated by circuit simulators	1. No consideration about the heat convection from the clod plate to the coolant 2. No consideration about thermal coupling effect	[44] [45] [46] [47]
Frequency-domain Thermal RC Network	1. High-sensitivity and low-noise temperature measurement 2. Device internal temperature and heat flowing outside devices are predicted	Four temperatures (junction temperature, case temperature, heat-sink temperature, and ambient temperature) need to be measured	[48] [49]
Numerical Analysis Method of Thermal Conduction	1. Model dynamic electro-thermal behavior 2. Effective in initial system thermal design 3. Fast calculation and simulation speed	No accurate estimation about the heat spreading effect in the material	[50][51][52]

IV. MODELING ANALYSIS, CYCLE COUNTING AND POWER CYCLING VERIFICATION

A. Modeling Analysis

1) Power Loss Analysis

The temperature dependent characteristics [42] of R_{ds_on} should be reflected in SiC MOSFET conduction loss evaluation, as the junction temperature feedback shows in Fig.1. As to switching loss, owing to high switching frequency of SiC MOSFET, the influence of parasitic elements cannot be ignored. Besides, for the DC-link capacitor, from the analysis in [43], we can find the lifetime model is connected to the temperature variation, which can be related to power loss. Thus, the DC-link capacitance power loss model is integrated into the total system power loss model as shown in Fig. 1.

2) Thermal Modeling

Three power module and heatsink thermal modeling methods are shown in Table II. The thermal impedance of the inverter contains the junction to case impedance, case to heatsink impedance and heatsink to ambient impedance.

There are two ways to derive the junction to case impedance. One is to directly reference the datasheet. The other method measures case and junction temperature respectively and then uses thermal equivalent circuit models to calculate junction-to-case impedance. Case temperature is usually measured by thermal couplers, Infra-Red cameras or optical fibers [21]. But these methods have limited temperature range and relatively low response speed [53]. Due to the physical junction location, most widely used junction temperature sensing method is to indirectly measure the

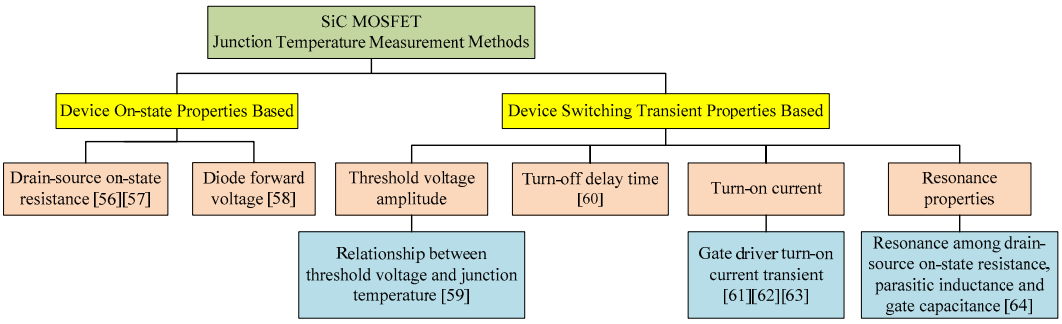

Fig.2 Summarization of TSP based SiC MOSFET junction temperature measurement methods [56]-[64]

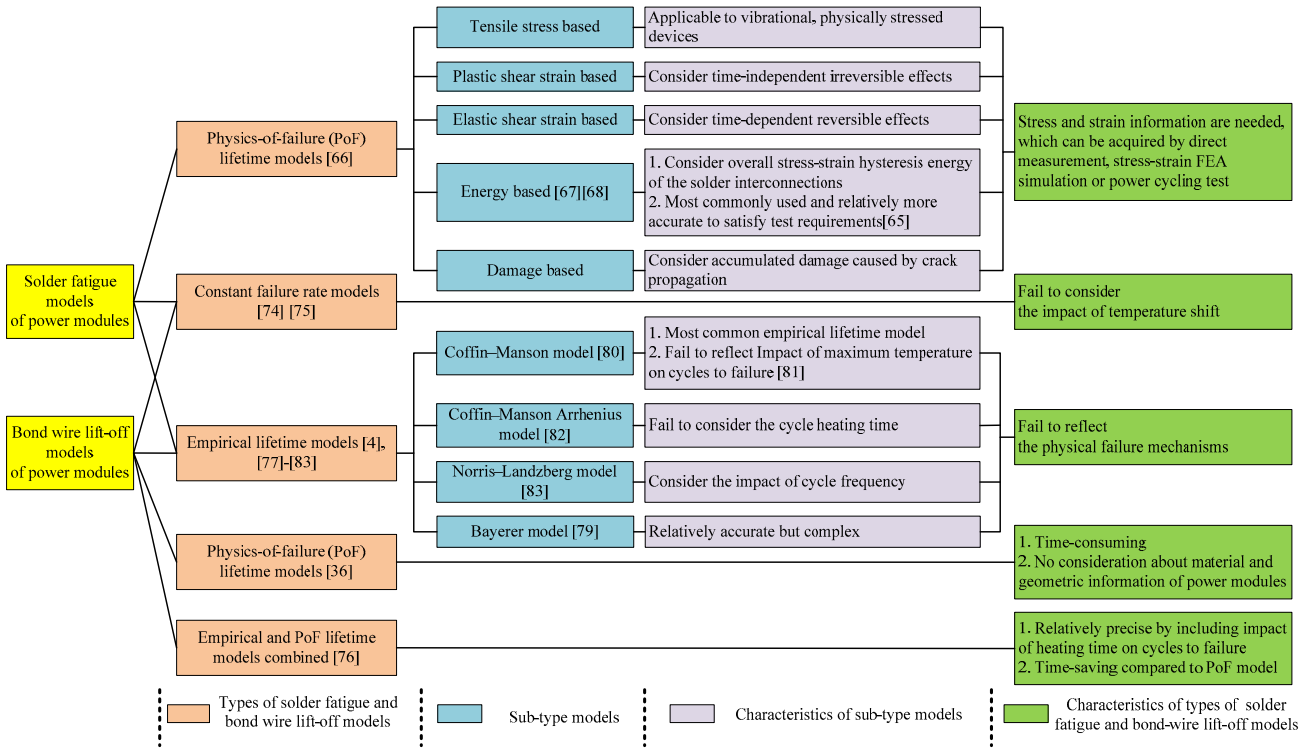

Fig.3 Comparison among solder fatigue and bond-wire lift-off models [4], [36], [65]-[68], [74]-[83]

Temperature Sensitive Parameters (TSP). Fig.2 summarizes the junction temperature measurement methods of SiC MOSFETs, which are generally divided into two types based on the on-state properties or switching transient properties.

As to case to ambient impedance, because of the heat convection effect, thermal coupling between different MOSFETs of different locations on the heat sink is evaluated in 2D thermal model [42] [54], and 3D thermal model [55].

3) Thermo-mechanical Model of the SiC MOSFET Module

Among different thermo-mechanical mechanisms, solder fatigue and wire bond lift-off are two most critical failure modes caused by the mismatch of the Coefficient of Temperature Expansion [65]. Due to similar temperature cycling induced stress-strain interaction mechanisms, either can be modeled by temperature cycle related empirical Coffin-Manson model[80] or by Physics-of-Failure based models. These two types of failure models are summarized in Fig. 3.

4) Inverter Fatigue Damage Accumulation

a) Linear Damage Accumulation Method

Based on the Palmgren-Miner's Law [69], the linear damage accumulation method is the most widely accepted in damage evaluations. However, it is independent of the loading levels [70], which affects the lifetime prediction accuracy.

b) Nonlinear Damage Accumulation Method

The nonlinear damage accumulation method can reflect the accumulation rate change in different stress levels. Commonly used nonlinear damage accumulation methods consider the sequence of stresses. For instance, the method based on the Double Linear Damage Law [71] allows each phase of the loading to be analyzed by the Palmgren-Miner linear damage

rule. However, it ignores the mutual effect among different stresses. In [72], both stress sequences and stress interaction are considered by modifying the exponent parameter in the Manson Halford Model.

c) Comparison

In linear accumulation methods, the damage accumulation rate is considered constant all through the device lifetime. However, actually as damage is accumulated, corresponding stresses could cause additional physical mechanisms, which would change the rate of damage increase. Take the thermo-mechanical stress for example. As the crack propagates, the junction-to-case resistance increases due to the increase of power loss and junction temperature, which accelerates the damage accumulation rate in the wire bond and solder interconnection. Therefore, lifetime predicted by linear methods is impractically longer. While nonlinear methods consider the damage accumulation rate change by putting proper weights onto the affected physical parameters. In order to determine these weights, detailed experimental data are needed [21], which makes these methods not generally applied. As a result, linear accumulation methods are considered in the flowchart in Fig.1. A feedback loop is applied in the thermo-mechanical stress related lifetime modeling to reflect the thermal resistance increase with the damage accumulation [84].

B. Cycle Counting

To efficiently count the randomly distributed thermal cycles, many counting algorithms have been proposed, such as level-crossing counting, peak counting, simple-range counting, and rainflow counting [85]. Among them, the rainflow counting algorithm is the most well-known [4] [86]. It counts only the extreme points to extract the amplitude [87] [88], mean value [89] and cycling period [3]. Traditional rainflow methods output half cycles that are difficult to be integrated into reliability algorithms, so [4] counts small cycles within larger ones to avoid this problem. Plus, contrary to traditional off-line rainflow methods, [90] processes real-time minimum or maximum temperature by using stack-based recursive programming, which overcomes the inefficient data storage.

C. Power Cycling Verification

1) Selection of Ageing Indicators

From the existing test comparisons in [22], widely used reliability test standards are not applicable to the SiC MOSFET due to the specific characteristics such as significant threshold voltage shift. The three Si device based reliability standards are summarized in Table III together with their shortcomings when used as the criteria of SiC MOSFET related tests.

TABLE III. RELIABILITY STANDARDS BASED ON SI DEVICES

Reliability Standards/Year	Shortcomings for SiC MOSFET
U.S. Department of Defense MIL-STD-750-3 / 2012 [73]	Not applicable to high temperature reverse bias stress
JEDEC JESD22-A108C / 2005 [91]	96-hour window is inappropriate after removal of bias
AEC-Q101-Rev-C / 2005 [92]	No consideration about characteristic change at high temperature

As a result, the selection of ageing indicators should be paid special attention to. For example, the frequently used R_{ds_on} in Si device ageing tests experiences a conspicuous increase resulted from positive gate bias and temperature stress. Therefore, it is not proper to be an ageing indicator of SiC MOSFET devices. Besides, drain-source on-state voltage is not suitable for ageing indicator either because of its high sensitivity with oxide trapping [41].

2) Power Cycling Test methods for SiC MOSFET Modules

Among the four active power cycling control methods, the strategy with constant junction temperature swing can achieve the longest lifetime since it compensates most degradation effects [93]. Hence, from the perspective of non-destructive test, temperature variation should be constant in the power cycling test. But in SiC MOSFET, there is charging and discharging of near-interfacial oxide traps [26], which causes the shift of threshold voltage, on-resistance, drain-source voltage. Thus, the injected DC power is unexpectedly changed. As a result, the junction temperature swing would also experience a shift due to the change in the applied thermal stress. Therefore, there exist come intrinsic issues in the SiC MOSFET based active power cycling tests in DC mode.

On the other hand, power cycling test in PWM mode can actively compensate the temperature swing caused by the trapping effect. Furthermore, in reality the degradation mechanism in the PWM controlled power cycling tests [34] is much more similar to the ageing process.

In terms of the above two considerations, power cycling tests in PWM mode rather than DC mode are more reasonable for the SiC MOSFET devices.

V. THERMAL PROFILE EXTRACTION

To verify the proposed inverter-level electro-thermal modeling procedures, a PLECS simulation based on the hybrid electric vehicle (HEV) application has been conducted. The topology is shown in Fig.4. The 3-phase electric motor is

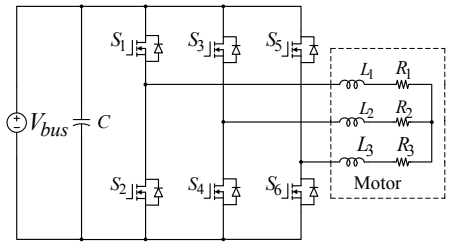

Fig.4 SiC MOSFET based two-level three-phase inverter

modeled by 3-phase in-series resistor and inductor loads. The studied HEV inverter parameters are: Active power – 58.52kW, Phase current RMS – 180A, Power factor – 0.85. The input DC bus voltage and input average current are 600V and 97.53A, respectively. The simulation parameters are: Switching frequency – 20kHz, Modulation index – 0.6. SPWM control method is adopted in this simulation.

BSM300D12P2E001 Full SiC MOSFET power module by Rohm is chosen. The switching turn-on, turn-off, and

conduction loss look-up tables are presented in Fig.5-7, respectively. The switching loss curve extraction is based on the turn-on gate-source voltage V_{gs_on} of 18V, turn-off gate-source voltage V_{gs_off} of 0V, gate resistance R_g of 0.2Ω and drain-source voltage V_{ds} of 600V. The conduction loss curve extraction is based on the relationship between the on-resistance and the junction temperature with the drain current I_d of 300A. The thermal impedance parameters provided by the corresponding datasheet from Rohm are used.

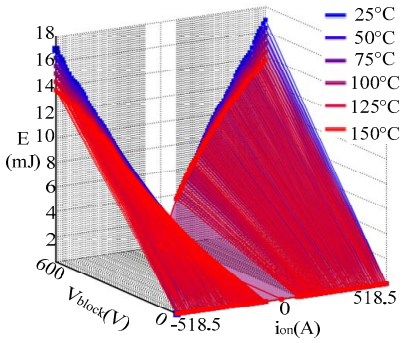

Fig.5 Turn-on Loss Look-up Table

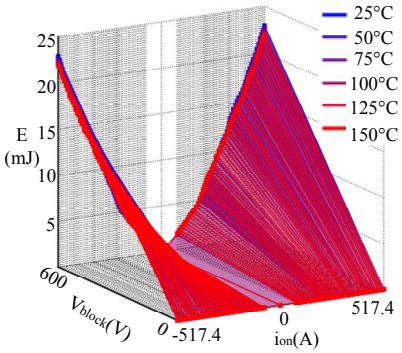

Fig.6 Turn-off Loss Look-up Table

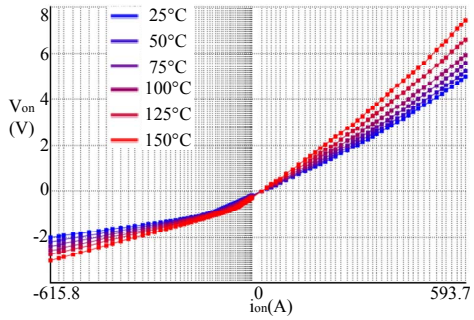

Fig.7 Conduction Loss Look-up Table

Fig. 8 shows the simulated thermal profile and average losses. The average conduction and switching losses of each SiC MOSFET are about 130W, 215W respectively. The junction temperature in the steady state is between 102°C and 104°C. The electro-thermal simulation results are consistent with the thermal equivalent circuit based temperature calculation. Therefore, it can be used for further system

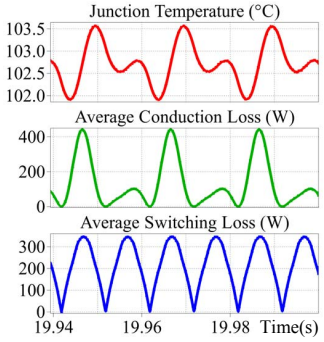

Fig.8. Thermal simulation results

lifetime modeling and the reference for SPWM controlled, SiC MOSFET based 3-phase inverter power cycling tests.

VI. Conclusions

This paper gives a review on a step-by-step lifetime prediction of the SiC MOSFET based 3-phase inverter systems. Based on the Weibull distribution statistical characteristics of five stress variables, the system failure rate and system MTTF integrating three groups of failure modes are first derived. An overview of the SiC MOSFET Physics-of-Failure is summarized. The power loss, thermal analysis, thermo-mechanical modeling, and inverter failure damage accumulation modeling are carefully compared. Besides, cycle counting methods are discussed and the power cycling method applicable to the SiC MOSFET power modules is analyzed. Finally, an electro-thermal simulation is conducted to verify the proposed inverter-level temperature profile extraction. The simulation result is consistent with the theoretical calculation. It can be used for further inverter-level lifetime modeling as well as the theoretical thermal reference of SiC MOSFET based 3-phase inverter power cycling tests in SPWM mode.

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