ECPE Guideline AQG 324

Qualification of Power Modules for Use in Power Electronics Converter Units (PCUs) in Motor Vehicles

Version no.: V01.05

Release date: 12.04.2018

Contact: ECPE European Center for Power Electronics e.V.
Dipl.-Phys. Thomas Harder
Landgrabenstrasse 94
90443 Nuremberg, Germany
Email thomas.harder@ecpe.org
Phone (+49) 911 8102 880

Preface

This Guideline was prepared by the ECPE Working Group ´Automotive Power Module Qualification´ comprising ECPE member companies active in the automotive market. The original version is based on the supply specification LV 324 which has been developed by German automotive OEMs together with representatives from the power electronics supplier industry in a joint working group of ECPE and the German ZVEI association.

The industrial standards referenced in this document have consciously been selected in the specific versions or release years. This means they represent the technical state of the art of the industry, which was not prepared for automotive applications, but has been deemed suitable with regard to automotive applications. In particular, this avoids automotive-relevant details being omitted during revisions with a focus on non-automotive applications.

The official version of the Guideline released by the ECPE Working Group is a public document available on the ECPE web site (www.ecpe.org).

Legal disclaimer

No liability shall attach to ECPE e.V. or its directors, employees, member organizations or members of the responsible ECPE working group for any personal injury, property damage or other damage of any nature whatsoever, whether direct or indirect, or for costs (including legal fees) and expenses arising out of the publication of, use of, or reliance upon, this ECPE Guideline or any other ECPE publications.

ECPE guidelines and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action ECPE does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the ECPE guidelines or publications.

Contents

1 Scope

This document defines requirements, test conditions and tests for validating properties, including the lifetime of power electronics modules and equivalent special designs based on discrete devices, for use in power electronics converter units (PCUs) of motor vehicles up to 3.5 t gross vehicle weight

The described tests concern the module design as well as the qualification of devices on module level (i.e. the assembly), but not the qualification of semiconductor chips or manufacturing processes.

These tests do not replace the tests for complete vehicle PCUs.

The qualification requirements shall be extended or adapted, as necessary, on use of technologically novel designs.

The requirements, test conditions and tests listed in this document essentially refer to power modules based on Si power semiconductors. Future releases of this guideline will address alternative semiconductor technologies e.g. SiC or GaN, and novel assembly and interconnection technologies where other failure mechanisms become important compared to the todays technologies.

The tests listed in this document also apply for validating power module properties when using a thermal interface between the power module and the cooling system on PCU-level, if this interface is not a part of the module structure as a result of the design. Corresponding tests must be conducted on a reference test setup recommended and documented by the module manufacturer, and any equivalent/generic test setups must be specified and documented.

Note:
If the thermal interface to the cooling system is implemented in the PCU and not in the power module, the module manufacturer cannot validate this interface. However, the module manufacturer must demonstrate that his module passes the module qualification in case of a connection as per the specification (recommended reference test setups). The PCU manufacturer must ensure that the thermal interface selected by it complies with the specifications from the module manufacturer.

Example:
Validation of the thermal interface of power electronics modules, which are applied to a heat sink using a thermal interface material (TIM), is considered through specified reference test setups (including materials) in this document.
Validation of the thermal interface of power electronics modules with a pin-fin base plate located directly in the cooling medium is considered in this document.

2 Overview

The tests described in the following serve to validate the properties and the lifetime of power electronics modules for use in the automotive industry.
The defined tests are based on the currently known failure mechanisms and the motor-vehicle specific usage profiles of power modules.

The validation takes place in the following steps:

- **QM – Module test**
  (Determines the electrical and mechanical parameters after the individual qualification tests)
  - Gate parameters
  - Rated and leakage currents
  - Forward voltages
  - X-ray, scanning acoustic microscopy/tomography (SAM/SAT)
  - Internal physical inspection/visual inspection (IPI/VI), optical microscope assessment (OMA)
- **Characterizing module testing**
  - QC-01 Determining parasitic stray inductance (L_p)
  - QC-02 Determining thermal resistance (R_{th} value)
  - QC-03 Determining short-circuit capability
  - QC-04 Insulation test
  - QC-05 Determining mechanical data
- **Environmental testing**
  - QE-01 Thermal shock test (TST)
  - QE-02 Contactability (CO)
  - QE-03 Vibration (V)
  - QE-04 Mechanical shock (MS)
- **Lifetime testing**
  - QL-01 Power cycling (PC_{sec})
  - QL-02 Power cycling (PC_{min})
  - QL-03 High-temperature storage (HTS)
  - QL-04 Low-temperature storage (LTS)
  - QL-05 High-temperature reverse bias (HTRB)
  - QL-06 High-temperature gate bias (HTGB)
  - QL-07 High-humidity high-temperature reverse bias (H3TRB)
- **Final testing for recording the electrical parameters of all DUTs**
- **Converting the test results into reliability data**

Characterizing module tests serve to validate the fundamental electrical-functional properties and mechanical data of power modules. Among other things, these tests can provide early detection and evaluation of degradation-independent weak points in the design (geometric arrangement, assembly and interconnection technology, semicon-

ductor quality) which may gain further significance under degradation influence with regard to reliability and performance.

The environmental tests serve to verify the suitability of power electronics modules for use in motor vehicles. Physical analyses, verification of electrical and mechanical parameters, and insulation properties are used for the validation.

Lifetime testing has the objective of triggering the typical degradation mechanisms of power electronics modules. This process primarily differentiates between two failure mechanisms – fatigue of close-to-chip interconnections (chip-near) and fatigue of interconnections with a wider distance to the chip (chip-remote). Both failure mechanisms are triggered by thermomechanical stress between the different materials (with different thermal expansion coefficients) in each case (see Figure 2.1b).

The reliability of both, chip-near and chip-remote interconnections, depends on the thermal interface to the cooling system. For this reason, module qualification tests relating to these interconnections can only be tested using an application-based setup for modules without direct connection to the cooling system (connection, e.g. without base plate via TIM).

The number of devices under test (DUTs) for environmental and lifetime testing must be agreed upon between the PCU manufacturer and the module manufacturer in advance, following the test flow chart defined in Annex A. For special designs, this must be agreed upon.

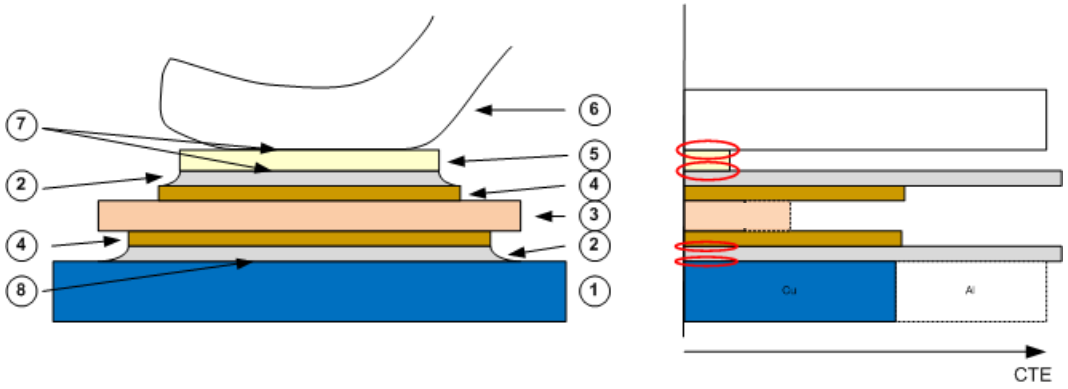

Figure 2.1: **a)** **b)**

a) Sample cross section of a power electronics module
1: Base plate, 2: Solder, 3: Ceramic insulator (DCB, AMB), 4: Copper, 5: Chip, 6: Bonding wire, 7: Chip-near connection, 8: Chip-remote connection

b) Schematic diagram of the thermal expansion coefficient in the individual layers of a power electronics module

3 Referenced standards

The following referenced documents are required for the use of this document. For references with a date, only the referenced issue is valid. For references without a date, the most recent issue of the referenced document (including all changes) is valid.

Standard	Contents
DIN EN ISO/IEC 170 25	General Requirements for the Competence of Testing and Calibration Laboratories
IEC 60747-8:2010	Semiconductor Devices - Discrete Devices Part 8: Field-Effect Transistors (FET)
IEC 60747-9:2007	Semiconductor Devices - Discrete Devices Part 9: Insulated-Gate Bipolar Transistors (IGBTs)
DIN EN 60747-15:2012	Semiconductor Devices - Discrete Devices Part 15: Isolated Power Semiconductor Devices
IEC 60749-5:2003	Semiconductor devices - Mechanical and climatic test methods - Part 5: Steady-state temperature humidity bias life test
IEC 60749-6:2002	Semiconductor Devices – Mechanical and Climatic Test Methods - Part 6: Storage at High Temperature
IEC 60749-34:2011	Semiconductor Devices – Mechanical and Climatic Test Methods - Part 34: Power Cycling
IEC 60749-25:2003	Semiconductor Devices – Mechanical and Climatic Test Methods - Part 25: Temperature Cycling
IEC 60068-2-48:1982	Environmental Testing – Part 2: Tests Guidance on the Application of the Tests of IEC 60068 to Simulate the Effects of Storage
DIN EN 60664-1	Insulation Coordination for Equipment Within Low-Voltage Systems Part 1: Principles, Requirements and Tests
DIN EN ISO 60664-1 Appendix 1	Insulation Coordination for Equipment Within Low-Voltage Systems - Part 2-1: Application Guide - Explanation of the Application of the IEC 60664 Series, Dimensioning Examples and Dielectric Testing (IEC/TR 60664-2-1:2011 + Cor. :2011)
DIN EN 60664-4	Insulation Coordination for Equipment Within Low-Voltage Systems Part 4: Consideration of High-Frequency Voltage Stress
DIN EN 60664-5	Insulation Coordination for Equipment Within Low-Voltage Systems Part 5: Comprehensive Method for Determining Clearances and Creepage Distances Equal To or Less Than 2 mm
DIN EN 60069-2-6	Environmental testing - Part 2-6: Tests - Test Fc: Vibration (sinusoidal)
DIN EN 60069-2-27	Environm. testing - Part 2-27: Tests - Test Ea and guidance: Shock
DIN EN 60069-2-64	Environmental testing - Part 2-64: Tests - Test Fh: Vibration, broadband random and guidance
JESD22-A119:2009	Low Temperature Storage Life

4 Terms and definitions

4.1 Definitions

4.1.1 Power electronics modules

Several active devices, e.g. insulated-gate bipolar transistors (IGBTs), metal-oxide semiconductor field-effect transistors (MOSFETs) or diodes as well as possibly additional passive components (e.g. temperature sensors, capacitors), with one or several current paths integrated using a circuit carrier (e.g. substrate) form a power electronics module.

4.1.2 Topological switch

A single semiconductor switch or several semiconductor switches connected in parallel which are controlled simultaneously to represent the function of a single switch.

Example: A half bridge consists of two topological switches – one high-side switch (HS) and one low-side switch (LS), whereby each topological switch can consist of one or several semiconductor switches/diodes connected in parallel.

4.1.3 Special designs based on discrete components

The control electronics on printed-circuit-boards (PCBs) installed in different PCUs, which contain circuit topologies with at least one topological switch consisting of discrete packaged IGBTs or MOSFETs, are considered power electronics modules as per section 4.1.1. If a driver infrastructure is additionally integrated in the board, the board represents an intelligent power module (IPM).

Note: One example for a special design is a B6 bridge (possibly including a driver) for controlling auxiliary power units on a FR4 PCB.

4.1.4 Current path of a power electronics module

The current path of a power electronics module consists of one or several topological switches which are interconnected in different circuit topologies, depending on the function represented.

Note:
Half bridge, consisting of one high-side switch (HS) and one low-side switch (LS) with center tapping (phase tapping). Any other topologies are also conceivable. For topologies other than bridge circuits, the definition of the current paths has to be agreed advance.

4.1.5 Chip-near interconnection technology

The chip-near interconnection technology describes a design of the chip top side connection as well as the chip backside connection with the substrate.

Examples:
Chip top surface: bond wire, ribbon bond, copper clip, sinter technology, µ-via connect
Chip backside: chip soldering, sinter technology, diffusion soldering

4.1.6 Chip-remote interconnection technology

The chip-remote interconnection technology describes a design of the connections which do not directly include the chip. For this, a differentiation must be made between electrical and thermal interfaces. As a result of the design, chip-remote interconnection technology can be electrical as well as thermal.

Examples:
Electrical interfaces: Design of the contacting for the load and auxiliary contacts.
Thermal interfaces: System soldering between substrate and base plate (modules with base plate) or interface between module and cooling system (modules without base plate).
Note: For modules without base plate, the interface between module and cooling system, which in this case must be considered differently, must be validated with suitable tests during the PCU testing.
Special designs:
Chip-remote interconnection technology related to discrete package types integrated on a PCB (e.g. TO-247 housing): Interface between TO rear side and PCB or heat sink, e.g. with a heat conducting film.

4.1.7 Circuit carrier

A circuit carrier is an unassembled or assembled wiring carrier for electronics.

4.1.8 System

Functionally linked components e.g. a drive consisting of electric machine, power electronics, ECU and sensors form a system.

4.1.9 Substrate

A substrate is a circuit carrier for power electronics components which can consist of different materials e.g. Al_2O_3, AlN, or organic-based materials e.g. in PCBs.

4.1.10 Direct and indirect cooling

In direct cooling the power module is part of the cooling system. Therefore, no thermal interface material (TIM) is used.
In indirect cooling the power module is assembled using TIM.

4.1.11 Signal connections

Signal connections mean the control connections of power electronics modules.

4.1.12 High voltage (HV)

High voltage means voltages > 60 V for DC and voltages > 30 V for AC rms.

4.1.13 Reliability data

Specific to the IGBT, MOSFET, diode, bonds or soldering tests, this is the number of cycles for each DUT until the first end-of-life (EOL) criterion is reached in each case, taking into account identical failure criteria in each case in connection with the test parameters used.

4.2 Abbreviations

Table 4.1: Abbreviations

AIT	Assembly and interconnection technology
AMB	Active metal brazing
CTE	Coefficient of thermal expansion
DCB	Direct copper bonded
DoE	Design of experiments
DUT	Device under test
EOL	End of life
Index "$_N$"	Nominal value – the nominal value of a quantity specified in the data sheet, e.g. voltage, current, resistance. In a module, a value can be different for switches and diodes.
IPI/VI	Internal physical inspection/visual inspection
IPM	Intelligent power electronics module
L_p	Parasitic stray inductance (or leakage inductance)
LSL	Lower specification limit
N_f	Number of cycles N until the first EOL criterion is reached in each case
OMA	Optical microscope assessment
PCB	Printed circuit board
PCU	Power electronics converter unit
PPAP	Production part approval process
PTB	Physikalisch Technische Bundesanstalt (German National Metrology Institute)
R_i	Internal resistance (e.g. of a voltage source in the test setup)
$R_{th,j-c}$	Thermal resistance of junction to case
$R_{th,j-s}$	Thermal resistance of junction to sink
$R_{th,j-a}$	Thermal resistance of junction to ambient
$R_{th,j-f}$	Thermal resistance of junction to fluid
SAM SAT	Scanning acoustic microscopy Scanning acoustic tomography
SOA	Safe operating area
TCAD	Technology computer aided design
TIM	Thermal interface material (e.g. thermal grease, phase change film)
USL	Upper specification limit

4.3 Voltages and currents

Table 4.2: Abbreviations for voltages and currents

V_{CE}	IGBT	Collector-emitter voltage
$V_{CE,sat}$	IGBT	Collector-emitter voltage (forward voltage) in saturation operation
$V_{BR,CES}$	IGBT	Collector-emitter breakdown voltage
$V_{CE,max}$	IGBT	Maximum collector-emitter voltage
V_{GE}	IGBT	Gate-emitter voltage
$V_{GE,max}$	IGBT	Maximum gate-emitter voltage
$V_{GE,th}$	IGBT	Gate-emitter threshold voltage
I_C	IGBT	Collector current
I_{CR}	IGBT	Collector current in reverse operation
I_{CN}	IGBT	Nominal collector current or continuous DC collector current
I_{SC1}		Short-circuit current type 1
I_{SC2}		Short-circuit current type 2
$I_{CE,leak}$	IGBT	Collector-emitter leakage current
$I_{GE,leak}$	IGBT	Gate-emitter leakage current
V_{DS}	MOSFET	Drain-source voltage (forward voltage)
$V_{BR,DS}$	MOSFET	Drain-source breakdown voltage
$V_{DS,max}$	MOSFET	Maximum drain-source voltage
$V_{F,SD}$	MOSFET	Forward voltage of the internal body diode (corresponds to the voltage of the drain-source path in reverse operation)
V_{GS}	MOSFET	Gate-source voltage
$V_{GS,max}$	MOSFET	Maximum gate-source voltage
$V_{GS,th}$	MOSFET	Gate-source threshold voltage
I_D	MOSFET	Drain current
$I_{DS,leak}$	MOSFET	Drain-source leakage current
$I_{GS,leak}$	MOSFET	Gate-source leakage current
V_{gate}		Gate voltage, general, e.g. V_{GE}, V_{GS}
V_S	Diode	Reverse voltage
V_F	Diode	Forward voltage
I_F	Diode:	Forward current
$I_{S,leak}$	Diode	Diode leakage current with reverse voltage applied
V_{test}		Test voltage, general, e.g. for insulation measurement
I_L		Load current, general e.g. on the phase tapping of a current path to load a semiconductor element, to generate the power loss P_V
$V_{int.c}$		Voltage in the intermediate circuit (DC link)
P_V		Power loss (e.g. $P_V = I_C \cdot V_{CE,sat}$ for IGBT, $P_V = I^2 \cdot R_{DSon}$ for MOSFETs or $P_V = I_F \cdot V_F$ for diodes)

All voltages and currents stated refer to the load or signal connections and generally do not include any voltage drops caused by the cables of the test setup.
Deviations from this, particularly for sources with internal resistance R_i or for test setups with series resistors, must be stated for the respective test.

4.4 Temperatures

Table 4.3: Abbreviations for temperatures

T_{RT}	Room temperature
T_{max}	Maximum specified operating temperature (data sheet information for the module)
T_{test}	Test temperature, general
ΔT	Temperature rise or deviation, general
T_{cool}	Coolant temperature
$T_{cool,min}$	Minimum coolant temperature
$T_{cool,max}$	Maximum coolant temperature
$T_{cool,in}$	Temperature of cooling medium, inlet
$T_{cool,out}$	Temperature of cooling medium, outlet
T_h	Temperature of the heat sink attached to the module
ΔT_h	Temperature rise of the heat sink attached to the module
T_c	Temperature of the base plate on modules with base plate
ΔT_c	Temperature rise of the base plate
T_s	Temperature of the sink on modules without base plate
ΔT_s	Temperature rise of the sink on modules without base plate
$T_{c/s}$	Temperature of the generalized contact surface "c" or "s"
$\Delta T_{c/s}$	Temperature rise of the generalized contact surface "c" or "s"
T_{vj}	Virtual junction temperature, general [a]
$T_{vj,min}$	Minimum virtual junction temperature [a]
$T_{vj,avg}$	Average virtual junction temperature [a]
$T_{vj,max}$	Maximum virtual junction temperature [a]
ΔT_{vj}	Temperature rise or deviation of the virtual junction temperature [a]
T_{stg}	Storage temperature
$T_{stg,min}$	Minimum storage temperature
$T_{stg,max}$	Maximum storage temperature
T_a	Ambient temperature

[a] Note: The junction temperature of a power semiconductor usually cannot be measured directly, but is indirectly concluded from a voltage measurement (e.g. $V_{CE,sat}$ for IGBTs, $V_{F,SD}$ of the internal body diode for MOSFETs, and V_F for diodes) (also see section Annex D [2]). Therefore, T_{vj} as the virtual junction temperature is stated instead of the real junction temperature T_j.

4.5 Humidity

Table 4.4: Abbreviations for humidity

RH	Relative humidity

4.6 Times

Table 4.5: Abbreviations for times

t_{on}	On-time of a load (e.g. heating phase)
t_{off}	Off-time of a load (e.g. cooling phase)
t_r	Rise time (e.g. from 10% to 90% gate voltage)
t_f	Fall time (e.g. from 90% to 10% gate voltage)
t_{test}	Test duration
t_{change}	Transfer duration
t_{dwell}	Dwell time

4.7 Standard tolerances

Tolerances refer to the measured value. For this, it must be ensured that the stated tolerances are adhered to independent of the tolerances of the testing system. If no other tolerances are stated in the individual tests, the tolerances from Table 4.6 must be used.
When two tolerance values are stated, the first value indicates the upper tolerance and the second value indicates the lower tolerance of the value range.

Table 4.6: Definitions of standard tolerances

Frequencies	± 1%
Measured temperatures	± 2 °C
Indirectly determined temperatures	± 5 °C
Humidity	± 5%
Times	+ 5%; - 0%
Voltages	± 2%
Currents	± 2%

4.8 Standard values

Unless otherwise specified, the standard values in Table 4.7 apply.

Table 4.7: Definitions of standard values

Room temperature	T_{RT} = 23 °C ± 5 °C
Humidity	RH = 25% to 75% relative humidity
Test temperature	$T_{test} = T_{RT}$

5 General part

5.1 Prerequisites for chip usage in the module

The grade of automotive maturity of the power semiconductor in use within the power module has to be shown for example by means of the ZVEI fact sheet ´Consumer Components in Safe Automotive Applications´ (//www.zvei.org/themen/mobilitaet/consumer-components-in-safe-automotive-applications/).
If additional process steps, which expand the semiconductor stack (e.g. chip post processing for double-sided contacting) are required for the chip assembly in the module, the robustness and suitability for use of this new design must be verified. The verification must be obtained through Design of Experiments (DoE) results, TCAD simulations and a review confirmation by the semiconductor manufacturer. The verification must be documented.

5.2 Technology qualification

Technology qualification refers to the complete execution of all tests described under sections 6 to 9 for a new range of power electronics modules. In the following cases, a technology qualification must always be executed in case of changes to already qualified modules:

Design change:

- Material or geometry change of the base plate
- Material or geometry change of the substrate
- Material or geometry change of the module casing
- Change to at least one contacting surface of the devices
- Use of another material for die-attach (chip bottom side connection) or system soldering
- Change of the interconnection technology for chips for the die-attach (e.g. sintering, soldering, diffusion soldering) or top contacting (e.g. wire bonding, ribbon bonding, Cu clip, sintering)

Chip change:

- Use of other semiconductors or semiconductor materials or other passive components from the same or a different manufacturer

All changes concerning the module and semiconductor design must be reported. Process-related changes must be documented. Appropriate validation measures must be taken and documented based on agreement between the module supplier and the customer. The delta qualification matrix shown in Annex B shall be used as a guideline for the agreement.

5.3 Qualification of special designs (of power electronics modules) based on discrete devices

A reduced test scope must be used for the qualification of special designs. Correspondingly assembled discrete housed semiconductor switches must be qualified as per AEC-Q101, integrated circuits (ICs) (e.g. driver ICs in housings) as per AEC-

Q100, and passive components as per AEC-Q200. For the special designs, only the tests QC-01 (stray inductance), QC-02 (thermal resistance) and QC-03 (short-circuit capability) must be executed. With regard to QC-01, the differences in the different current paths must be marked as well as evaluated and documented with regard to their criticality for reliable operation of the discrete semiconductor switches via simulation and in consultation with the semiconductor manufacturer. Concerning QC-02, a thermal management concept has to be provided which verifies compliance with the semiconductor specifications for each operating point. This also applies to the dynamic case. If necessary, the measuring setup must be adapted accordingly. The requirements for short-circuit capability described in QC-03 must also be tested for the special designs. The tests must be carried out by the manufacturer of the assembly or by the integrator into the PCU.

5.4 Sampling rates and measured value resolutions

The sampling rate and bandwidth of the measuring system must be adapted to the respective test. All measured values must be recorded with all maximum values (peaks).

The resolution of the measured values must be adapted to the respective test. It must be ensured that occurring voltage peaks do not lead to an overflow or that they cannot be measured in the case of an insufficient resolution. Data reductions/abstractions (e.g. limit monitoring) must not suppress irregularities.
When recording the measurement values for lifetime testing, it must be ensured that the measurement values are recorded with sufficient granularity regarding the expected lifetime, in order to ensure meaningful and precise determination of the EOL.

5.5 Design of insulation properties

The design of the air gaps and creepage distances as well as the selection of the solid insulating materials and gels must be indicated as per DIN EN 60664 Parts 1, 4 and 5.

The following must be provided as a minimum:

- Creepage distances including tolerance in the specified temperature range
- Air gaps including tolerance in the specified temperature range
- Solid insulating materials and gels as well as their properties in the specified temperature range and for long-term influence of temperature, humidity and mechanical pressure (e.g. molding compound damage through spring clamp)
- Selected voltage values of the respective design
- Selected test voltages and test periods of the respective design
- Protection against soiling and soiling category with regard to the target application in the vehicle
- Sections and tables from DIN EN 60664 used for the design
- Simulation of the mechanical strength of insulation parts

Note:
For stating the insulation materials and gels, it is sufficient to provide the material

composition. Detailed information about the manufacturer and the type designation is not required.

5.6 Interface description

All interfaces must be described completely with regard to their electrical and mechanical properties.

5.7 Physical analysis

The physical analysis is a detailed analysis which must be conducted after failure of a DUT or after completing all electric testing on an OK part.

The following procedure shall be used:

1. Execution and documentation of all non-destructive tests/analyses
2. Derivation or joint coordination of additional tests/analyses based on the results of the non-destructive tests/analyses
3. Execution and documentation all destructive tests/analyses
4. Archiving of specimen and damaged parts

Examples for test methods are provided in Annex E.
The change in the module compared to the as-new condition must be evaluated.

The results must be documented in the test record.

5.8 Procedure limitations

The test laboratory must be organized and operated as per DIN EN ISO/IEC 17025 or IATF 16949. All test equipment used for measuring must be calibrated as per DIN EN ISO/IEC 17025 (or as specified or recommended by the manufacturer) and it must be possible to trace the equipment back to the PTB or an equivalent national or European standards laboratory. The testing devices, equipment, setups and test methods must not distort the behavior of the DUT. These must be documented in the test report together with the accuracies and the expiration date of the calibration.

6 Module test

6.1 QM – 01 Module test

6.1.1 General information

The module test serves to characterize the electrical and mechanical properties of the DUTs before (to ensure that only flawless DUTs enter into the qualification tests) and after the individual test sequences. Its purpose is to provide insight into the characteristic parameters of the modules, which can vary due to production fluctuations and the stress applied during the individual tests. Unless stated otherwise, the individual test steps of the module tests must be carried out before and after each of the individual test branches as per the test flow chart plan in Annex A and Table 6.1. They must be documented and the deviations outside the specified tolerances must be shown.

The objective of the measurements and tests is:

- To ensure the absence of failures in all DUTs.
- To ensure that all requirements are met.
- To verify the functional behavior and the accuracy of all functions.

The measurements and tests 6.1.2 to 6.1.8 must be conducted as a minimum during the module tests. For all these tests, a defined shutting down/starting up of the DUTs from/into the load condition must be ensured, especially before/after the (intermediate) measurements. The temperature shall only be regulated to the target temperature of the intermediate measurement after shutting off the module. After the intermediate measurement, first the module must be started up and then the temperature must be regulated.

Note on data sheet values: Typical parameter values without range or limit information are not permitted as suitable criteria in the framework of module tests. If the range or limit information is missing in the data sheet, the module manufacturer must supply these later on. The values and the note about a special definition must be documented.

6.1.2 End-of-line test

All DUTs must be tested as per the standard end-of-line test. With regard to 100% traceability, the results of the end-of-line test must be documented.

6.1.3 Testing the interconnection layers

The quality of the interconnection layers (e.g. solder, diffusion solder, sintered interconnection) and possible degradation due to voids, delamination or crack formation must be recorded and documented. For this, an examination using scanning acoustic microscopy (SAM) is recommended.

6.1.4 Nominal collector current or continuous DC-collector current (IGBT – modules)

The nominal collector current I_{CN} must be defined and documented as per one of the following definitions:

a) Nominal collector current = constant direct current with $R_{th,j-c}$ with $T_{vj} \leq T_{vj,max}$ or

b) Nominal collector current = collector current with typ. $V_{CE,sat}$ with maximum $R_{th,j-c}$

Note: Data sheets usually state the implemented nominal chip current (e.g. 800 A). This generally does not correspond to the nominal module current as a function of the thermal resistance and the cooling connection (e.g. 550 A).

6.1.5 Gate-emitter (IGBT)/gate-source (MOSFET) threshold voltage

The gate-emitter or gate-source threshold voltage ($V_{GE,th}$ or $V_{GS,th}$) must be determined at RT and the maximum specified operating temperature, which must be derived from the maximum junction temperature. This threshold voltage must be compared to the data sheet values.

6.1.6 Gate-emitter (IGBT)/gate-source (MOSFET) leakage current

The gate-emitter or gate-source leakage current ($I_{GE,leak}$ or $I_{GS,leak}$) must be determined at RT and the maximum specified operating temperature, which must be derived from the maximum junction temperature. This threshold voltage must be compared to the data sheet values.

6.1.7 Collector-emitter (IGBT)/drain-source (MOSFET) reverse leakage current

The collector-emitter or drain-source leakage current ($I_{CE,leak}$ or $I_{DS,leak}$) must be determined at RT and the maximum specified operating temperature, which must be derived from the maximum junction temperature. This threshold voltage must be compared to the data sheet values.
In case of IGBTs with freewheeling diode connected anti-parallel, the leakage current is the sum of the reverse leakage current of the IGBT and the leakage current of the diode.

6.1.8 Forward voltage $V_{CE,sat}$ (IGBT), V_{DS} (MOSFET), V_F (diodes)

The forward voltage ($V_{CE,sat}$, V_{DS}, V_F) must be determined at RT and the maximum specified operating temperature, which must be derived from the maximum junction temperature. This forward voltage serves as the data basis for the subsequent lifetime testing. For this, the forward voltage must be determined in pulsed operation in order to keep self-heating as low as possible.

6.1.9 IPI/VI, OMA

Damage or changes to the module due to load stress (failure analysis during qualification – see section 5.5) must be recorded with the following analysis methods and documented:

OMA (Optical Microscope Assessment)
IPI/VI (Internal Physical Inspection / Visual Inspection)

The test flow chart as per Annex A must be observed for all tests. If a component-specific adaptation of the test sequence is necessary (e.g. qualification of derivatives), the test flow chart can be adapted in agreement with the component manufacturer, but this must be documented.

	Readouts (1,2,3,4,…)	End Of Line Test [c] (acc. to 6.1.2-6.1.8)	SAM System / Chip solder	Correlation [a] $V_{GE,th}/V_{GS,th}$	Correlation [a] $I_{GE,leak}$ / $I_{GS,leak}$	Correlation [a] $I_{CE,leak}$ / $I_{DS,leak}$	Correlation [a] V_{CE} / V_{DS}	Correlation [a] V_F	Correlation [a] R_{th} (acc. to QC-02)	Short Circuit Test (acc. to QC-03)	Dynamic Test [d] (Double Pulse)	Isolation Test [b]	Optional IPI/VI, OMA
QC-01 .. QC-04	1: Start of test 2: End of test	1,2	1	1,2	1,2	1,2	1,2	1,2				1,2	1,2
QC-05	1: Start of test 2: End of test	1	1,2									1,2	1,2
QE-01 TST	1: 0c 2: 500c (opt.) 3: 1000c	1,2,3	2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
QE-03 V	1: Start of test 2: End of test	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QE-04 MS	1: Start of test 2: End of test	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QL-01 PC_{sec}	1: 0c 2: End of life	1,2 (opt)	2	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2	1,2
QL-02 PC_{min}	1: 0c 2: End of life	1,2 (opt)	2	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2 (opt)	1,2	1,2
QL-03 HTS	1: 0h 2: 1000h	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QL-04 LTS	1: 0h 2: 1000h	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QL-05 HTRB	1: 0h 2: 1000h	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QL-06 HTGB	1: 0h 2: 1000h	1,2		1,2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
QL-07 H^3TRB	1: 0h 2: 1000h	1,2		1-2	1,2	1,2	1,2	1,2		1,2	1,2	1,2	1,2
Master samples	1: 0h	1											

[a] Correlation - for the correlations, the T_{RT} measured values of the characteristic data at the specified measurement time are compared against the values of the initial measurement.
The values used for the correlation shall be documented accordingly and maximum percentages of the anticipated deviations shall be specified.
[b] ISO test - in the ISO test, the insulation capability of the module is tested in accordance with the final series production test specifications.
[c] Defined startup or shutdown before/after exposure to stress shall be ensured according to the specifications in the chapter "Module test".
[d] Should be performed according to IEC 60747-15 2012 chapter 5.3.2.

Table 6.1: Test-dependent module tests

7 Characterizing module testing

The module tests described in sections 7.1 to 7.5 shall be carried out once and supply application-relevant characteristic properties of the module.

Characterizing module tests are the basic prerequisite for conducting subsequent environmental and lifetime testing. The application of generic data for characterizing module tests is not permissible.

7.1 QC-01 Determining parasitic stray inductance (L_p)

7.1.1 Purpose

This test determines the parasitic stray inductance L_p of the main contacts of a single current path of the DUT.

7.1.2 Test

The parasitic stray inductance L_p must be determined as per IEC 60747-15:2012, section 5.3.2 (double pulse testing). If the DUT has several identical current paths, the maximum value of all current paths must be indicated for the parasitic stray inductance.

The scope of random samples for this test must be taken from the test flow chart.

7.1.3 Requirement

The test conditions, the test setup and the test results (measured curves documented by the manufacturer to determine the parasitic stray inductance L_p) must be provided to the purchaser.

Note:
The parasitic stray inductance of the power electronics module installed in the PCU can have a crucial quality-relevant impact on the function or reliability of the PCU, depending on the PCU structure.

7.2 QC-02 Determining thermal resistance (R_{th} value)

7.2.1 Purpose

This test determines the thermal resistance of the individual devices on the power module.

7.2.2 Test

The test must be conducted as per DIN EN 60747-15:2012, section 5.3.6, with the following additions:

DIN EN 60747-15:2012, section 5.3.6.1: thermal resistance $R_{th,j-c}$

- The position and distances of the temperature sensor, which determine the reference point for determining the reference temperature T_c, must be documented.

- The temperature sensor must be guided as closely as possible to the module (as per figure 7.1) to allow optimum determination of the reference point for determining the reference temperature T_c for the case-related thermal resistance:

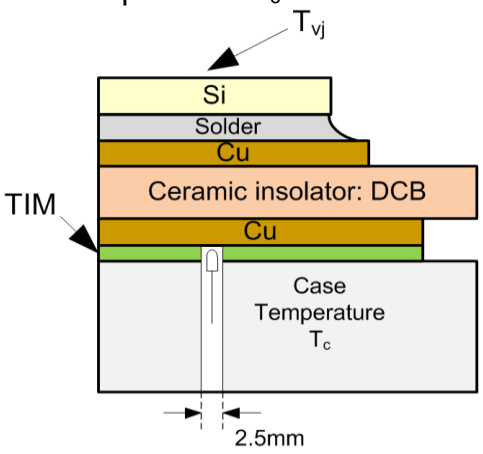

Figure 7.1: Reference point for determining the reference temperature T_c

The thermal resistance $R_{th,j-c}$ must therefore be determined using the following formula:

$$R_{th,j-c} = \frac{T_{vj} - T_c}{P_v}$$

- For measuring T_c, a hole must be made in the heat sink, centrally below the device under test (DUT). The hole must have a diameter of 2.5 mm, see Figure 7.1.

- When determining the thermal resistance $R_{th,j-c}$, the type (manufacturer, designation, thickness, thermal conductance) of the TIM material used during the measurement must also be stated.

DIN EN 60747-15:2012, section 5.3.6.4: thermal resistance $R_{th,j-s}$

- Reference point for determining the reference temperature T_s for the heat-sink-related thermal resistance:

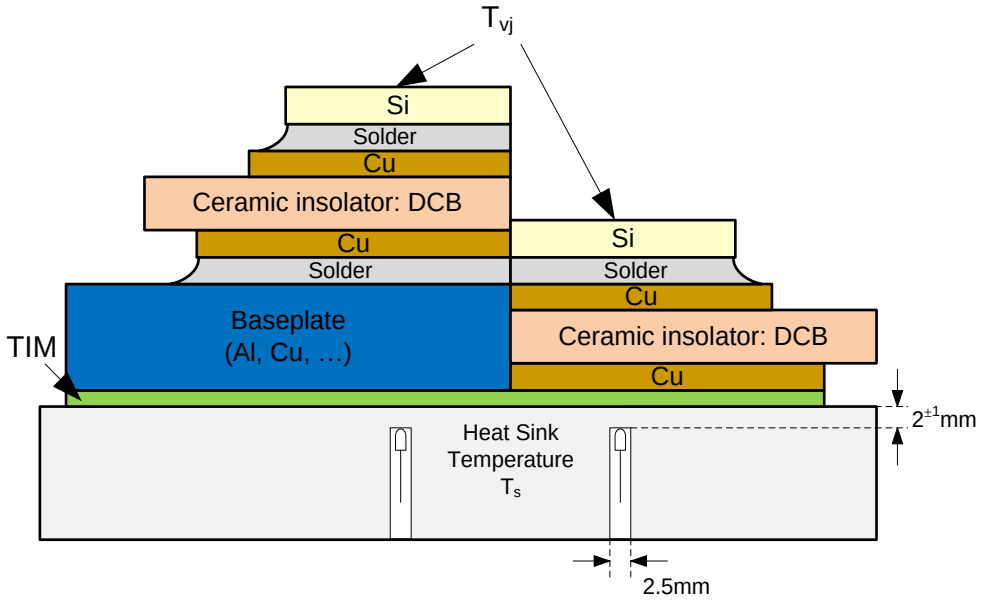

Figure 7.2: Reference point for determining the reference temperature T_S

- The thermal resistance $R_{th,j\text{-}s}$ must therefore be determined using the following formula:

$$R_{th,j-s} = \frac{T_{vj} - T_s}{P_v}$$

- For measuring T_s, a blind hole must be made in the heat sink, centrally below the DUT. The blind hole must have a diameter of 2.5 mm and end 2 ±1 mm below the heat sink surface, see Figure 7.2.

- When determining the thermal resistance $R_{th,j\text{-}s}$, the type (manufacturer, designation, thickness, thermal conductance) of the TIM material used during the measurement must also be stated.

Supplementary tests for DIN EN 60747-15:2012:

- For power modules with direct contact to liquid cooling media, it is necessary to determine the thermal resistance between the junction temperature and the cooling medium ($R_{th,j\text{-}f}$).

  For this, the coolant flow must be adjusted as per common applications and the coolant, (e.g. ethylene glycol water/propylene glycol water), the coolant circuit pressure and the coolant flow must be documented.

  The reference points for determining the temperatures of the cooling medium ($T_{cool,in}$, $T_{cool,out}$) for the thermal resistance related to the coolant according to Figure 7.3:

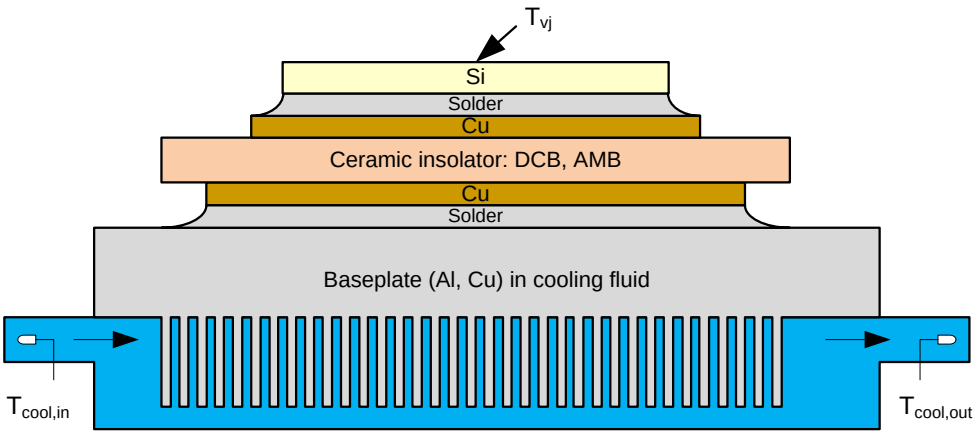

Figure 7.3: Reference point for determining the reference temperature T_{cool}

The thermal resistance $R_{th,j-a}$ must therefore be determined using the following formula:

$$R_{th,j-a} = R_{th,j-f} = \frac{T_{vj} - \left(\frac{T_{cool,in} + T_{cool,out}}{2}\right)}{P_v}$$

The scope of random samples for this test must be taken from the test flow chart.

7.2.3 Requirement

The test conditions (with information about the reference point for the temperature on casing, heat sink or cooling medium) and the test results must be documented.

For power modules with several devices or current paths, it must be indicated how the devices were connected and/or operated for determining the thermal resistance.

7.3 QC-03 Determining short-circuit capability

7.3.1 Purpose

In the frame of this test, the short-circuit capability specified in the data sheet shall be verified. If the module has no short-circuit capability according to the manufacturer's specifications, this test is omitted. Omitting the test must be justified and documented in the test report.

The test is described by the voltages V_{CE} or V_{DS} and V_{GE} or V_{GS}, the short-circuit pulse duration t_p and the junction temperature T_{vj} at the time of the start of the short-circuit pulse duration.

7.3.2 Test

For the short-circuit test it must be ensured that the maximum junction temperature is present in the semiconductor at the start of the test.

A short circuit of type 1 as well as a short circuit of type 2 can be used for the test.

To maintain the voltages within the permissible range during the test, the DUT can be connected with a gate-emitter clamping or with a collector-gate clamping. It must be ensured beforehand that this causes no relevant heating up. If this is the case, the DUT must be adjusted to T_{vj} less than, but close to $T_{vj,max}$ beforehand and it must be documented that $T_{vj,max}$ is not exceeded during the test.

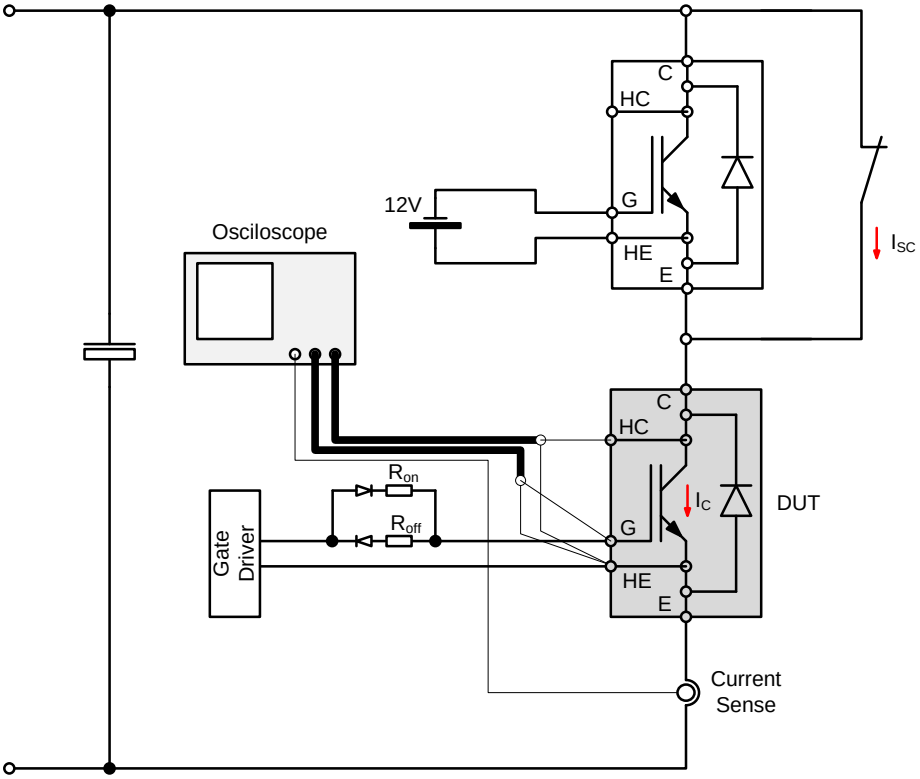

Figure 7.4: Test setup for short-circuit capability

Short circuit type 1 (hard switch failure):

For a short circuit type 1, the inductances in the measuring setup must be kept small enough that the DUT does not reach the saturated range at any time.

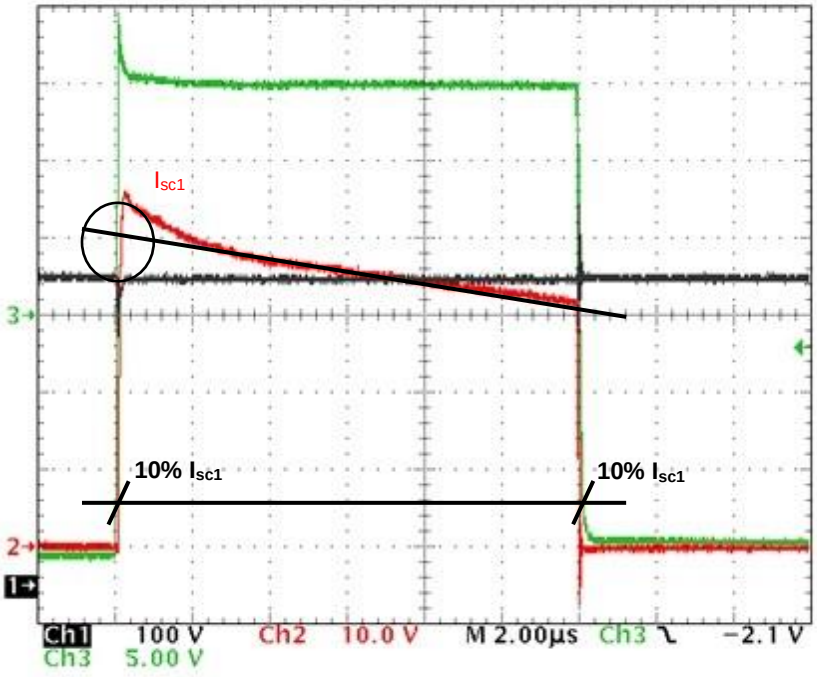

Figure 7.5: Typical short circuit type 1 behavior of an IGBT
Ch1: V_{CE} (100 V/Div), Ch2: IC (10 A/Div), Ch3: V_{GE} (5 V/Div)

For this, the parameter pulse duration t_p and the junction temperature T_{vj} are defined as follows:

t_p: 10% leading edge I_{SC} – 10% trailing edge I_{SC1}
T_{vj}: T_{vj} at the time of 10% leading edge I_{SC1}

The scope of random samples for this test must be taken from the test flow chart.

Short circuit type 2 (failure under load):

For a short circuit type 2, the inductances in the measuring setup must be dimensioned so that the desaturation phase of the DUT is reached after 5 µs at the latest.

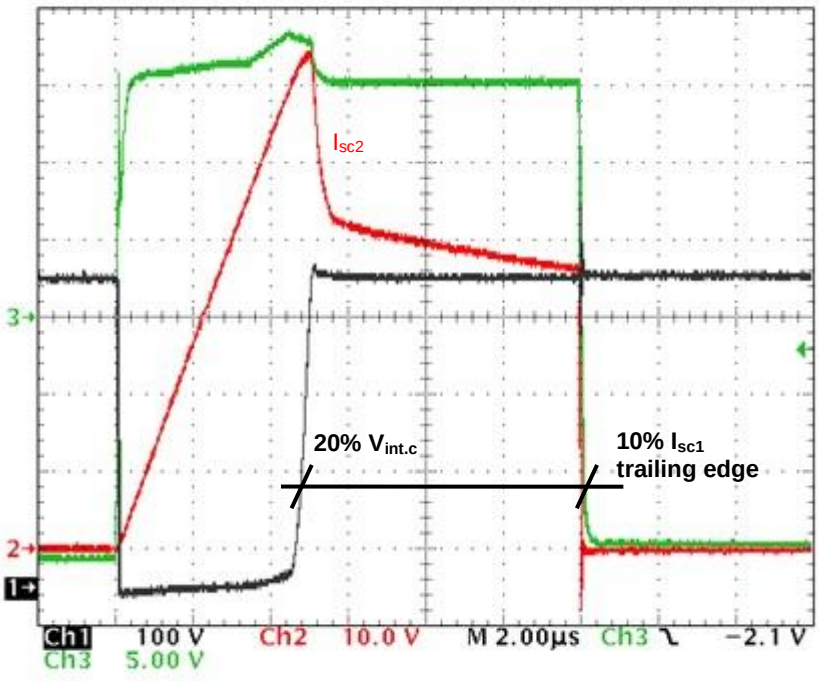

Figure 7.6: Typical short circuit type 2 behavior of an IGBT
Ch1: V_{CE} (100 V/Div), Ch2: IC (10 A/Div), Ch3: V_{GE} (5 V/Div)

For this, the parameter pulse duration t_p and the junction temperature T_{vj} are defined as follows:

t_p: 20% leading edge $V_{int.c}$ – 10% trailing edge I_{SC2}
T_{vj}: T_{vj} at the time of 20% leading edge $V_{int.c}$

The scope of random samples for this test must be taken from the test flow chart.

7.3.3 Requirement

During the test with short circuit type 1 and with short circuit type 2 the test is considered passed if the DUT can keep the intermediate circuit voltage stable 1 s after the pulse.

Beyond this, the specified blocking capacity of the tested module must be tested again after the static test (see sections 6.1.6 and 6.1.7). The test setup, the test parameters ($T_{vj,max}$, I_{SC}, V_{GE}/V_{GS}, V_{CE}/V_{DS}) and the test results (screenshots of the oscilloscope measurements) must be documented.

7.4 QC-04 Insulation test

7.4.1 Purpose

All high voltage DUTs must undergo a dielectric strength test and an insulation resistance test. The insulation between all galvanically insulated connections is tested. For this, all galvanically linked connections in the module should be interconnected conductively.

7.4.2 Test

The tests are conducted on module level.

At the start, the DUTs undergo a pre-conditioning phase, followed by a conditioning phase. The parameters of these phases are different for the insulation resistance test and the dielectric strength test.
The tests must be carried out with standard commercially available insulation test devices. Simple multimeter measurements are not permissible.

The scope of random samples for this test must be taken from the test flow chart.

7.4.3 Insulation resistance measurement

- Pre-conditioning: 8 h at 5 ± 2 °C
- Conditioning: 8 h at 23 ± 5 °C, 90 +10/-5% RH, 86 - 106 kPa
- Cyclic insulation resistance measurement from the start of the conditioning phase
- The test voltage of the insulation resistance measurement must be selected as follows:
    - At least 1.5 times the value of the maximum possible intermediate circuit voltage of the module (e.g., 1.5 x 450 V DC for 650 V-IGBT modules)
    - But at least 500 V DC
- The insulation resistance must not fall below 100 MΩ.

Deviation from the times stated is permissible, but they must not be shorter than twice the time which is required for full heating up of the DUT.

During the conditioning phase, the insulation resistance must be measured and documented cyclically. The measuring rate must be selected so that the lowest occurring value of the insulation resistance is recorded reliably, but at least every 30 min.

To avoid distorting the measured values through contamination, the DUTs must be processed with the cleanliness common to automotive production.

The scope of random samples for this test must be taken from the test flow chart.

Note: The parameters for the pre-conditioning phase and the conditioning phase are selected so that the dew point is passed shortly after the start of the conditioning phase.

7.4.4 Dielectric strength test

The dielectric strength test is conducted after the insulation resistance test from section 7.4.3.

- Pre-conditioning: 30 ± 2 °C until fully heated through
- Conditioning: 48 h at 23 ± 2 °C, 93 ± 5% RH, 86 - 106 kPa
- Measurement of the insulation resistance
- Application of the test voltage
- Measurement of the insulation resistance

Before and after applying the test voltage, the insulation resistance (without additional conditioning) must be measured.

The test voltage must be selected so that the dielectric strength stated in the data sheet of the DUT is ensured.
The scope of random samples for this test must be taken from the test flow chart.

Note 1:
The pre-conditioning phase and the conditioning phase are selected so that the insulation materials of the DUT are subjected to a defined moisture treatment.

Note 2:
As per DIN EN 60664-1, Supplement 1 (Explanation of the Application of the IEC 60664 Series, Dimensioning Examples and Dielectric Testing), the selected test voltage depends on the respective use of the power module:

a) According to the overvoltage categories, if the target applications are operated on the public power grid.
b) On the basis of the actually occurring transient overvoltage in applications isolated from the power grid (e.g. electric system of a pure hybrid electric vehicle) as per DIN EN 60664-1.

7.4.5 Requirement

No sparkovers must occur during the test. The insulation resistance must not fall below 100 MΩ before and after the test. Any drift must be documented and evaluated.

The documentation of the test setup, the test conditions and the test results must be provided to the purchaser.

7.5 QC-05 Determining mechanical data

7.5.1 Purpose

Determination and verification of the mechanical data of a module with regard to the data sheet values are the prerequisites for conducting all tests from test flow chart. Therefore, the following measurements and tests must be conducted before all other characterizing module tests and the corresponding parameters must be provided to the purchaser upon request.

7.5.2 Test

- Determination of the mechanical data of the module and of the seals for confirming the dimensional stability as per the approval drawing.
- Determination of the insulation distances as per the approval drawing.
- Torques of fastenings and electrical contacts:
    - Tightening torques during the initial test as per the manufacturer's instructions.
    - Residual torque during the final test.
- Determination of the setting behavior of the threaded connections during the final test on electric contacts, on fastenings on heat sinks and on parts which are relevant to the insulation properties of the module.

- Application of heat-conducting media:
    - Use or application following the manufacturer's instructions and determination of the distribution of the heat-conducting medium using scanning acoustic microscopy (SAM) on at least one DUT before the start of a test.

7.5.3 Requirement

- Verification of the flow behavior or final distribution after completing a test using scanning acoustic microscopy (SAM), during the physical analysis, if necessary. The size and position of delaminations must be represented using SAM photography.
- The measurement and torque tolerances of the threaded connection points and installation points and of the electric contacts must each be within the module specification.
- Any releasing, tightening, or re-tightening of threaded connections during a test is forbidden.

7.6 Test sequence

The test flow chart as per Annex A shall be adhered to for all tests. If a component-specific adaptation of the test sequence is necessary (e.g. qualification of derivatives), the test flow chart can be adapted.

8 Environmental testing

8.1 Use of generic data

The use of generic data for each test is permissible in the framework of the module qualification, as long as the difference between the module to be qualified and the reference module is documented and as long as proof can be provided that the differences between the reference module and the module to be qualified causes no changes with regard to the module properties.

8.2 QE-01 Thermal shock test (TST)

8.2.1 Purpose

This test validates the resistance to mechanical stress from passive temperature changes. Due to a lack of acceleration factors respectively the long cycle times as a result of the test setup, it is not necessary to conduct this test until EOL.

8.2.2 Test

The test shall be performed in accordance with IEC 60749-25:2003, with the following additions:

IEC 60749-25:2003, section 4: Test fixture

- In the sense of comparability, this test must be conducted exclusively in a two-chamber system (air/air). Testing in a single-chamber or triple-chamber system is not permissible.

IEC 60749-25:2003, section 5.2: Test sequence

- The DUT must be installed as per the manufacturer's installation instructions before it is introduced into the test chamber. If this requires permanent installation of the DUT with a threaded connection or a similar method, this setup must also be implemented in the test chamber and the setup must be documented.

IEC 60749-25:2003, sections 5.3 – 5.8: Cycle frequency, dwell time, test condition, etc.

- This test must focus on the cycle frequency for soldered connections (1 - 2 cycles per hour).
- t_{dwell} > 15 min must be selected for the dwell time for the highest/lowest temperature; this corresponds to stress category 4 from table 2 in IEC 60749-25:2003.
- The following temperatures must be selected for testing the power modules: $T_{stg,min}$ = -40°C, $T_{stg,max}$ = +125°C. This corresponds to test condition G from Table 1.

IEC 60749-25:2003, section 5.9: Transfer duration

- A value of < 30 s must be ensured for the transfer duration t_{change}.

IEC 60749-25:2003, section 5.12: Failure criteria

- In addition to the electric parameters defined in the module data sheet, this test requires a verification of the following parameter:
  - Thermal resistance: $R_{th,j\text{-}c/s}$
    For this, the thermal resistance must be determined depending on the module type as per section 7.2.

  If the measurement of the thermal resistance is not possible within the test setup, then the DUT can be removed at defined times (see 8.2.3) at T_{RT} for determining the thermal resistance and must then be reintroduced into the test setup at T_{RT}.

  In addition to this, it is recommended to also examine the DUT during this test at the times defined above using a suitable non-destructive analysis process (e.g. SAM) and to document the degree of delamination at the junction layers.

- As per the storage temperature parameter T_{stg} described in IEC 60749-25:2003, thermocouples or similar temperature measuring devices must be used to ensure that the entire capacity of the DUT meets the defined temperature limits and the requirements for the dwell time.

  Note:
  The time until complete heating through of the DUT strongly depends on the thermal capacity of the DUT.

- The hold time for the basic temperature values $T_{stg,min}$ and $T_{stg,max}$ must be at least t_{dwell} so the stresses can release and the creeping can begin.

The scope of random samples for this test must be taken from the test flow chart.

This yields the following parameter for the TST test:

Table 8.1: TST test parameters

Lowest value of the storage temperature	$T_{stg,min}$	$-40°C^{0}_{-10}$
Highest value of the storage temperature	$T_{stg,max}$	$+125°C^{+15}_{0}$
Transfer duration	t_{change}	< 30 s
Minimum dwell time for highest/lowest temperature	t_{dwell}	> 15 min
Minimum number of cycles without failures	N_C	> 1000

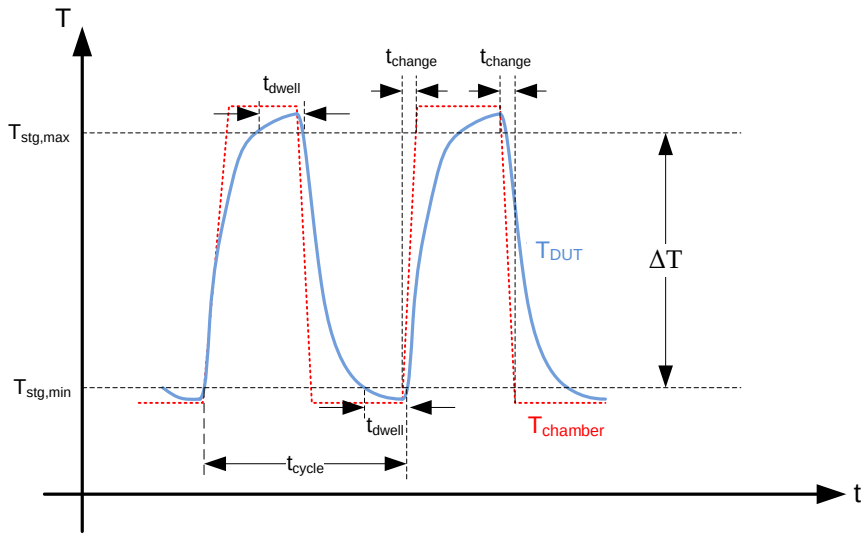

Figure 8.1: Example for TST temperature curve

8.2.3 Requirement

The DUTs must be fully functional before and after the test. All parameters must be within the specification and must not violate the defined failure limits in order for the test to be evaluated as passed.

A rise of the thermal resistance by 20% compared to the initial value before the test must be evaluated as a failure.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

The results and parameters of the test as per the specifications from section 5.1 and Annex C must be documented.

8.3 QE-02 Contactability (CO)

Due to the extremely wide range of technology application possibilities for all module's peripheral contacts and interfaces out of the assembly and interconnection technology field no concrete qualification routines have been specified yet in this present release version. It is pursed to specify suitable and beneficial testing routines in later releases. Therefore, this chapter is inserted already now as a placeholder.

8.4 QE-03 Vibration (V)

8.4.1 Purpose

The purpose of the test is to show the fundamental suitability of the mechanical structure for use in automotive PCUs.
It simulates the vibration load of a module during driving operation and serves to validate the resistance of the module against vibrations with failure patterns, e.g. device detachment and material fatigue.

8.4.2 Test

The test is carried out acc. to DIN EN 60068-2-6 for sinusoidal vibration excitation and DIN EN 60068-2-64 for wide-band vibration excitation with the following parameters:

Table 8.2: Test parameters regardless of point of use

Temperature	T_{RT}
Frequency sweep time for sinusoidal excitation	1 octave/min, logarithmic
Vibration profile A [a] (for combustion engine mounted parts)	Vibration excitation, sinusoidal acc. to Figure 8.2 and Table 8.3 Vibration excitation, wide-band random vibration acc. to Figure 8.3 and Table 8.4
Vibration profile B [a] (for transmission mounted parts)	Vibration excitation, sinusoidal acc. to Figure 8.4 and Table 8.5 Vibration excitation, wide-band random vibration acc. to Figure 8.5 and Table 8.6
Vibration profile D [a] (Detachable body parts for components mounted on sprung masses. Additionally: If the purchaser does not provide any profiles in the case point of use electric machine, vibration profile D must be used.)	Vibration excitation, wide-band random vibration acc. to Figure 8.6 and Table 8.7
Number of DUTs	6
[a] The labelling and order of letters, and their relationship to vibrational profiles are selected acc. to the terms in the German supplier regulation LV 124.	

The test must be performed without bracket or add-on parts in a reference setup. Additional tests with bracket or add-on parts must be coordinated with the purchaser, if required.

For components that are installed on the bracket or vehicle through damping elements, it must be specified in the Component Performance Specifications whether

- all DUTs with damping elements,
- all DUTs without damping elements or
- three DUTs with damping elements and three DUTs without damping elements

must be tested.

The sampling rate must be selected so that interruptions or short circuits can be unambiguously detected by using a sensing current.

The tests must be performed without electrical operation. The electric connection must be implemented as is typical for the application. The test setup must be documented.

The scope of random samples for this test must be taken from the test flow chart.

Vibration profile A (for combustion engine mounted parts)

Table 8.3: Test parameters - vibration, sinusoidal for combustion engine mounted parts

Vibration excitation	Sinusoidal	
Test duration for each spatial axis	22 h	
Vibration profile	Characteristic 1 applies to components mounted on engines with maximum 5 cylinders. Characteristic 2 applies to components mounted on engines with 6 or more cylinders. The characteristics must be combined for components that can be used in both cases.	
Characteristic 1 in Figure 8.2	Frequency in Hz	Amplitude of the acceleration in m/s²
	100	100
	200	200
	240	200
	270	100
	440	100
Characteristic 2 in Figure 8.2	Frequency in Hz	Amplitude of the acceleration in m/s²
	100	100
	150	150
	440	150
Combination	Frequency in Hz	Amplitude of the acceleration in m/s²
	100	100
	150	150
	200	200
	240	200
	255	150
	440	150

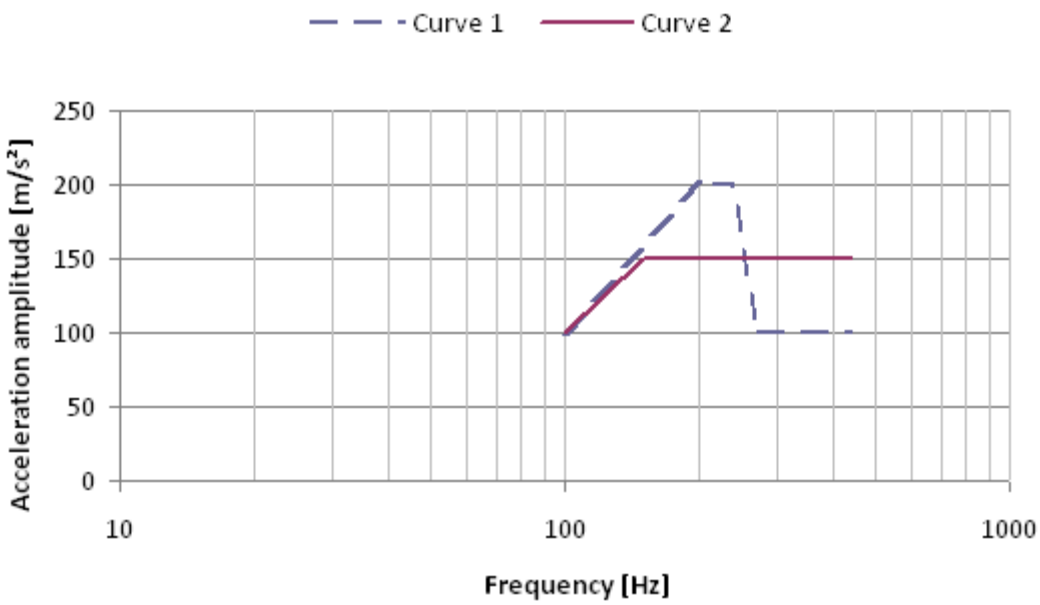

Figure 8.2: Vibration profile, sinusoidal for engine-mounted parts

Table 8.4: Test parameters - vibration, wide-band random vibration for engine-mounted parts

Vibration excitation	Wide-band random vibration	
Test duration for each spatial axis	22 h	
RMS value of acceleration	181 m/s²	
Vibration profile Figure 8.3	Frequency in Hz	Power density spectrum in $(m/s^2)^2/Hz$
	10	10
	100	10
	300	0.51
	500	20
	2 000	20

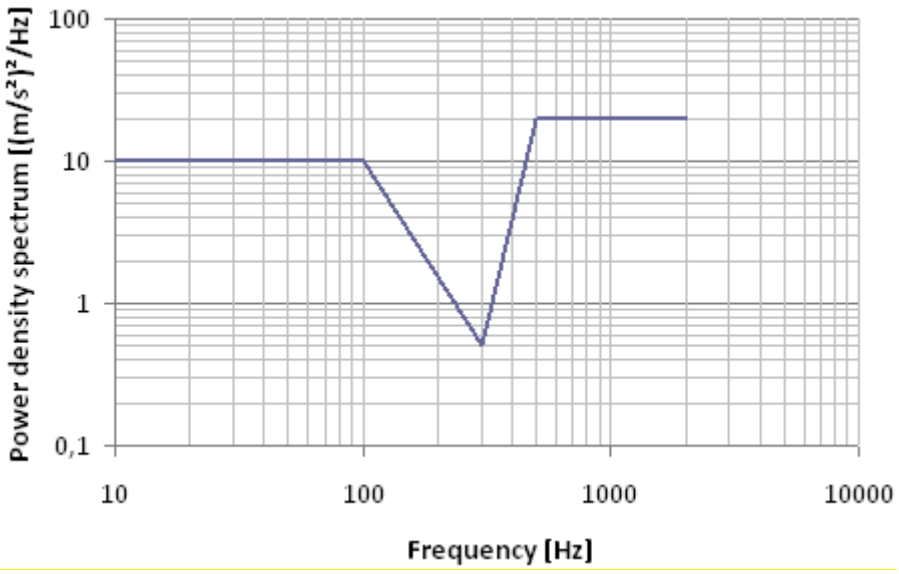

Figure 8.3: Vibration profile, wide-band random vibration for engine-mounted parts

Vibration profile B (for gearbox-mounted parts)

Table 8.5: Test parameters - vibration, sinusoidal for gearbox-mounted parts

Vibration excitation	Sinusoidal	
Test duration for each spatial axis	22 h	
Vibration profile Figure 8.4	Frequency in Hz	Amplitude of the acceleration in m/s²
	100	30
	200	60
	440	60

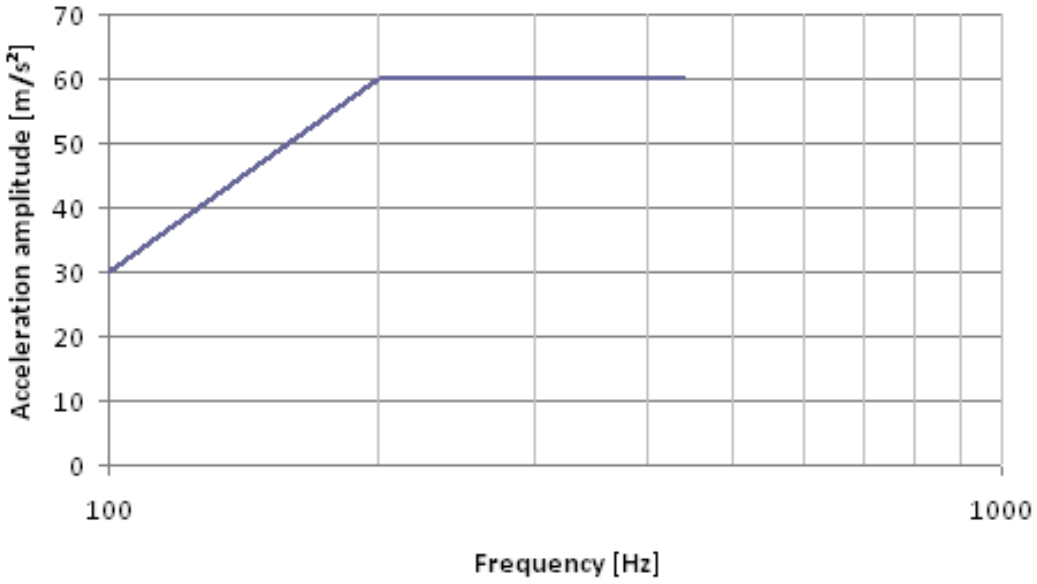

Figure 8.4: Vibration profile, sinusoidal for gearbox-mounted parts

Table 8.6: Test parameters - vibration, wide-band random vibration for gearbox-mounted parts

Vibration excitation	Wide-band random vibration	
Test duration for each spatial axis	22 h	
RMS value of acceleration	96.6 m/s²	
Vibration profile Figure 8.5	Frequency in Hz	Power density spectrum (m/s²)²/Hz
	10	10
	100	10
	300	0.51
	500	5
	2 000	5

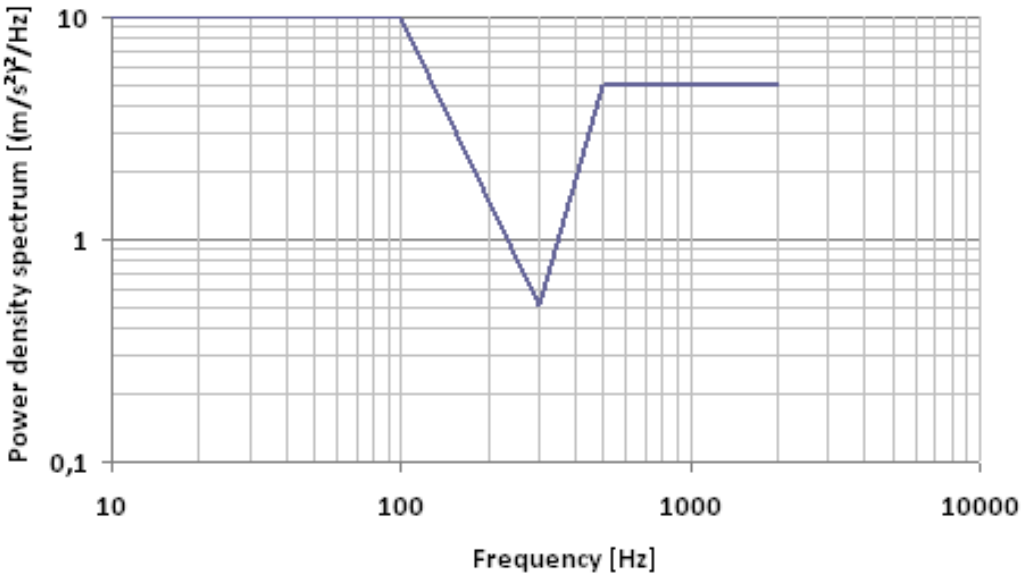

Figure 8.5: Vibration profile, wide-band random vibration for gearbox-mounted parts

Vibration profile D (body-mounted parts (for components installed on sprung masses))

Table 8.7: Test parameters, wide-band random vibration for sprung masses

Vibration excitation	Wide-band random vibration	
Test duration for each spatial axis	8 h	
RMS value of acceleration	30.8 m/s²	
Vibration profile Figure 8.6	Frequency in Hz	Power density spectrum in (m/s²)²/Hz
	5	0.884
	10	20
	55	6.5
	180	0.25
	300	0.25
	360	0.14
	1 000	0.14
	2 000	0.14

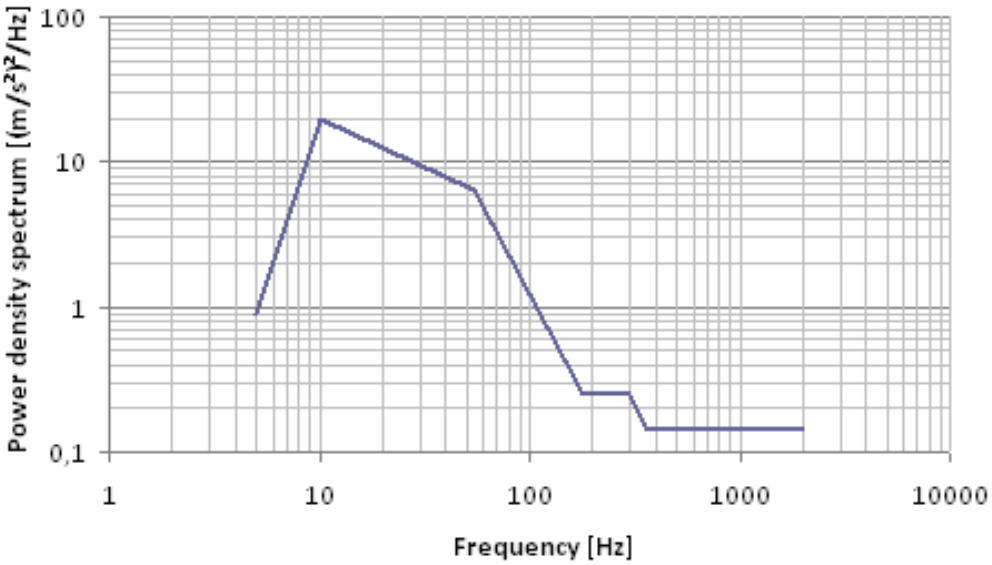

Figure 8.6: Vibration profile, wide-band random vibration for sprung masses

8.4.3 Requirement

The DUT must be fully functional before and after the test, and all parameters must meet the specifications.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

8.5 QE-04 Mechanical shock (MS)

8.5.1 Purpose

This test simulates the mechanical load of the module in the PCU, e.g. when driving over curbs or during an accident. It serves to validate the resistance of the PCU to mechanical shock with failure patterns, such as cracks or device detachment.

8.5.2 Test

The test is carried out acc. to DIN EN 60068-2-27 with the following parameters:

Table 8.8: Test parameters QE-04 Mechanical shock

Peak acceleration	500 m/s^2
Shock duration	6 ms
Shock form	half-sine
Number of shocks per direction (±X, ±Y, ±Z)	10
Number of DUTs	6

The tests must be performed without electrical operation. The electric connection must be implemented as is typical for the application. The test setup must be documented.

The scope of random samples for this test must be taken from the test flow chart.

8.5.3 Requirement

The DUT must be fully functional before and after the test, and all parameters must meet the specifications.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

9 Lifetime testing

9.1 Use of generic data

The use of generic data for each test is permissible in the framework of the module qualification, as long as the difference between the module to be qualified and the reference module is documented and as long as proof can be provided that the differences between the reference module and the module to be qualified causes no changes with regard to the module properties.

9.2 QL-01 Power cycling (PC_{sec})

9.2.1 Purpose

This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model.

The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wear and degradation on the module.

By limiting the key parameter t_{on} (on-time of the load current) to a value range of $t_{on} < 5$ s, the tests exerts targeted stress on the chip-near interconnections (die-attach and top-side contacting).

The results of this test are the reliability data for the module-specific, chip-near interconnection technology as well as the marking of the data in the numerical representation of the lifetime curve $N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$ which must be provided by the manufacturer.

9.2.2 Test

The test must be conducted as per IEC 60749-34:2011 with the following additions:

IEC 60749-34:2011, section 4: Test apparatus

- The control of the switching-on and switching-off duration (cycle duration) must be implemented using permanently set time values (t_{on}, t_{off}). These must be determined before the test in such a way that the temperature rise ΔT_{vj} of the junction temperature necessary for the test is achieved.

- If the temperature rises of the virtual junction temperature ΔT_{vj} as required for the test cannot be achieved through selection of the suitable parameters t_{on}, t_{off}, it is permissible to influence the temperature rise of the virtual junction temperature ΔT_{vj} by varying the gate voltage of the power semiconductor accordingly. For this, a variation of the gate voltage is only permissible within the saturation range of the power semiconductor and must be set once at the start of the test.

- When testing Si-MOSFETs, the virtual junction temperature must not be determined in the channel of the Si-MOSFET but using the body diode, for reasons of device design.

- All other control methods, e.g. controlling the on-time and off-time via the monitoring of the heat sink temperature T_S or the base plate temperature T_C, or controlling using constant power loss P_V, are not permissible.

IEC 60749-34:2011, section 5: Test procedure

- The values set once (t_{on}, t_{off}) must not be adjusted during the entire test (also refer to Annex D reference [1], section 2.4: Control strategy t_{on} = const. and t_{off} = const.).
  Note: A change in the temperature rise of the virtual junction temperature ΔT_{vj} in connection with this during the test duration is therefore accepted, reflecting the aging of the DUT.

- A gate voltage selected at the beginning must not be varied during the test.

- The test must be conducted for at least two different temperature rises ΔT_{vj}. For this, the values for the temperature rises $\Delta T_{vj,1}$ to $\Delta T_{vj,n}$ must be selected such that the maximum temperature rise is at least 40% higher than the minimum temperature rise, so that the results of the tests can be used to validate nodes of the reliability curve $N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$ for chip-near interconnections.

- All relevant current paths in structurally similar DUTs must be tested for each temperature rise $\Delta T_{vj,1}$ to $\Delta T_{vj,n}$ so that all semiconductors and components of a module are tested at least once.

- The scope of random samples for this test is at least six topological switches from three different DUTs. For this, it must be ensured that application-relevant current paths are tested in each case.

- For testing MOSFETs, the inverse body diode of the MOSFET examined in each case can be energized for heating up the device as an alternative. However, it must be ensured that the maximum permissible chip power is not exceeded - if necessary, the current must then be selected to be $< 0.85 \cdot I_{DN}$ and documented.

- The lifetime model of the diodes must be confirmed. If the module manufacturer ensures that the diode has at least the same power cycling capability, e.g. the same chip-near interconnection technology and small single diode dice are used, only a confirmation test has to be performed at minimum one condition with all diodes.

IEC 60749-34:2011, section 6: Test conditions

- The DUT must be fully functional before the test, and all parameters must be within the specifications. The parameters are verified with the use of a module test (see section 6.1).

- The virtual junction temperature T_{vj} of the DUT must be determined using the $V_{CE}(T)$-method (see Annex D, reference [2], section 3: $V_{CE}(T)$-method). Alternatively, chip temperature measurement methods are possible, if the module manufacturer provides a correlation to the method given in reference [2].

- The calculation of the junction temperature T_{vj} using the thermal resistance and the power loss P_V provided in the data sheet is not permissible.

- The test conditions formulated in IEC 60749-34:2011, table 1, must not be taken into account (because these are not suitable for validating a lifetime model).

- The following limits from Table 9.1 for the PC_{sec} test must be observed for verifying the lifetime model provided by the manufacturer:

Table 9.1: Limits for test parameters PC_{sec}

Parameter		Value
On-time of the load current	t_{on}	< 5 s
Value of load current	I_L	> 0.85·I_{CN} [a, b]
Gate voltage	V_{gate}	typically 15 V [c]

[a] The value of the load current > 0.85·I_{CN} must only be used for one node.
[b] A value < 0.85·I_{CN} can be selected for the second node in order to allow a suitable difference of the temperature rises to be set.
[c] The gate voltage for testing IGBT and MOSFET can fall below the 15 V (e.g., when contact currents become too high), if – due to the thermal properties of the module – the desired temperature rise cannot be achieved with on-times of t_{on} < 5 s. For this, however, it must always be ensured that the switch is permanently operated in the saturated range. In these cases, the gate voltage used must only be set once at the start of the tests and documented in each case.

- The module manufacturer must select the remaining parameters for the test as a function of the DUT properties, the test apparatus and the temperature rise of the virtual junction temperature ΔT_{vj} in each case.

- For modules without base plate, a module-dependent and material-dependent settling process of the TIM material between module and cooling system must be taken into account for determining the starting values for forward voltage and temperature rise, and documented accordingly.

- The following parameters must be documented specifically for each module for the test:

Table 9.2: Module-specific test parameters PC_{sec}

Parameter	
Temperature rise of virtual junction temperature (starting value for test after settling process)	$\Delta T_{vj,start}$
Duration of settling process (in cycles)	N_{start}
Load current	I_L
On-time of the load current (heating period)	t_{on}
Off-time of the load current (cooling period)	t_{off}
Minimum virtual junction temperature at the start of the test	$T_{vj,min}$
Maximum virtual junction temperature at the start of the test	$T_{vj,max}$
Coolant feed temperature	T_{cool}
Gate voltage	V_{gate}

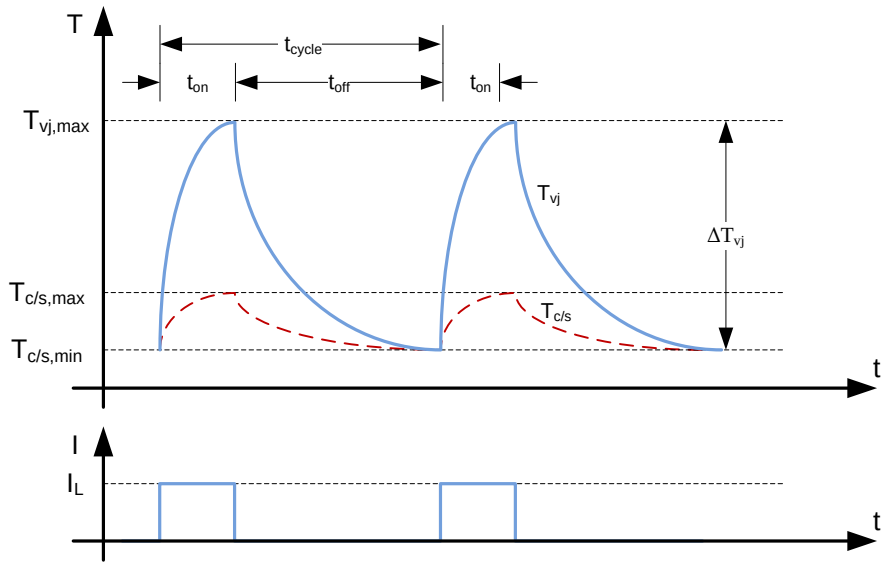

Figure 9.1: Example for current and temperature curve PC_{sec}

- The DUTs must be loaded at least until the first occurring EOL criterion has been reached. It is strongly recommended, however, to continue loading the DUTs after reaching the first EOL criterion in the sense of improved evaluation of the results.

IEC 60749-34:2011, section 8: Measurement and tests

- Monitoring of the failure criteria must be implemented using the two parameters forward voltage (IGBT: $V_{CE,sat}$, MOSFET: V_{DS}, diode: V_F) and temperature rise of the virtual junction temperature ΔT_{vj} and other technology related parameters. These parameters must be monitored for each cycle during the entire test and documented accordingly.
- The EOL criteria must be tested by means of continuous parameter monitoring (see Table 9.3. For this it must be ensured that the measurement values are recorded with sufficient granularity regarding the expected lifetime, in order to ensure meaningful and precise determination of the EOL.

IEC 60749-34:2011, section 9: Failure and evaluation criteria

- The failure criteria are defined as follows:

Table 9.3: EOL criteria PC_{sec}

Parameter		**Change from standard value**
Forward voltage	IGBT: $V_{CE,sat}$ MOSFET: V_{DS} Diode: V_F, V_{FSD}	+5% [a]
Increase of thermal resistance	$R_{th,j-c}$, $R_{th,j-s}$, $R_{th,j-f}$ [b]	+20%

[a] Note: See also the notes on the settling process under test conditions

[b] Note: It has to be ensured that the duration of temperature rise is sufficient for the calculation of static R_{th}, or an additional online R_{th} measurement should be performed without removing the power modules from the test bench, when TIM or a baseplate is part of the DUT.

- It is recommended to examine the DUTs for cracks on the soldering joints, substrates, die parts and the casings after the end of the test using scanning acoustic microscopy. Other relevant thermal and mechanical connections having impact on EOL criteria should be examined.

9.2.3 Requirement

The lifetime data $N_f = f(\Delta T_{vj}, T_{j,max}, t_{on})$ determined for the individual DUTs during the test must be marked in the reliability curve for the power electronics module provided by the manufacturer. A probability of N_f should be specified, e.g. 5%. It must be ensured that only DUTs are used whose failure patterns have identical failure mechanisms. DUTs with deviating failure mechanisms must be removed and the test must be repeated with new DUTs. The failure patterns/mechanisms of these removed DUTs must be documented. Failures of the semiconductor which cannot be clearly attributed to the aging of the assembly and interconnection technology are not permissible.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this test must be taken from Table 6.1.

The results and parameters of the test must be documented. The lifetime data must be created.

9.3 QL-02 Power cycle (PC_{min})

9.3.1 Purpose

This test is the basis for verification of the lifetime model provided by the module manufacturer for the DUTs to be examined. The tests themselves can also be used to support creating the lifetime model.

The objective of this test is to generate targeted stress situations in a power electronics module under strongly accelerated conditions which lead to signs of wearout and degradation on the module.

If the time range of the key parameter value t_{on} (on-time of the load current) is expanded to values from $t_{on} > 15$ s, this test exerts a different stress on the power electronics modules than the test PC_{sec}. The stress can be applied to the chip-remote interconnection (system soldering) as well as to the chip-near interconnection technology (die-attach, top-side contacting).

This test thus enables pro rata simulation of the situation in the module during a cold start.

The results of this test are the reliability data for the module-specific connection technology as well as the marking of the data in the numerical representation of the empirical lifetime curve $N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$ which must be provided by the manufacturer.

9.3.2 Test

The test must be conducted as per IEC 60749-34:2011, with the following additions:

IEC 60749-34:2011, section 4: Test apparatus

- The control of the switching-on and switching-off duration (cycle duration) must be implemented using permanently set time values (t_{on}, t_{off}). These must be

determined before the test in such a way that the temperature rise ΔT_{vj} of the junction temperature necessary for the test is achieved.

- If the temperature rises of the virtual junction temperature ΔT_{vj} as required for the test cannot be achieved through selection of the suitable parameters t_{on}, t_{off}, it is permissible to influence the temperature rise of the virtual junction temperature ΔT_{vj} by varying the gate voltage of the power semiconductor accordingly. For this, a variation of the gate voltage is only permissible within the saturation range of the power semiconductor and must be set once at the start of the test.

  Note: By lowering the gate voltage, higher power loss (greater rise) can be achieved even if excessively high DC currents would violate the limits of the contactings.

- When testing Si-MOSFETs, the virtual junction temperature must not be determined in the channel of the Si-MOSFET but using the body diode, for reasons of device design.

- All other control procedures, e.g. controlling the on-time and off-time with regard to a constant temperature rise ΔT_{vj} or controlling using constant power loss P_V, are not permissible.

IEC 60749-34:2011, section 5: Test procedure

- The values set once (t_{on}, t_{off}) must not be adjusted during the test (also refer to Annex D, reference [1], section 2.4: Control strategy t_{on} = const. and t_{off} = const.).

  Note: A change in the temperature rise of the virtual junction temperature ΔT_{vj} in connection with this during the test duration is therefore accepted, reflecting the aging of the DUT.

- A gate voltage selected at the beginning must not be varied during the test.

- The temperature rises of the base plate temperature or heat sink temperature or fluid temperature $\Delta T_{c/s}$ must be recorded and documented accordingly.

- The reference points for determining the parameters T_c and T_s must be taken from Figure 7.1 and Figure 7.2.

- The test must be conducted for at least two different temperature rises ΔT_{vj}. For this, the temperature rises $\Delta T_{vj,1}$ to $\Delta T_{vj,n}$ must be selected such that the maximum temperature rise is at least 40% higher than the minimum temperature rise, to enable the results of the tests to be validate nodes of the reliability curve $N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$ for the chip-remote interconnections.

- All relevant current paths in structurally similar DUTs must be tested for each temperature rise $\Delta T_{vj,1}$ to $\Delta T_{vj,n}$ so that all semiconductors and components of a module are tested at least once.

- The scope of random samples for this test is at least six topological switches from three different DUTs. For this, it must be ensured that application-relevant current paths are tested in each case.

- For testing MOSFETs, the inverse body diode of the MOSFET examined in each case can be energized for heating up the device as an alternative.

- The lifetime model of the diodes must be confirmed. If the module manufacturer ensures that the diode has at least the same power cycling capability, e.g. the same chip-near interconnection technology and small single diode dice are used, only a confirmation test has to be performed at minimum one condition with all diodes.

IEC 60749-34:2011, section 6: Test conditions

- The DUT must be fully functional before the test, and all parameters must be within the specifications. The parameters are verified with the use of a module test (see section 6.1).

- The virtual junction temperature T_{vj} of the DUT must be determined using the $V_{CE}(T)$-method (see Annex D, reference [2], section 3: $V_{CE}(T)$-method). Alternatively, chip temperature measurement methods are possible, if the module manufacturer provides a correlation to the method given in reference [2].

- The calculation of the junction temperature T_{vj} using the thermal resistance and the power loss P_V provided in the data sheet is not permissible.

- The temperature change $T_{c/s}$ ($\Delta T_{c/s}$) must be determined through the $R_{th,j\text{-}c/s}$ and the power loss P_V as determined during a preliminary measurement.

- The test conditions formulated in IEC 60749-34:2011, table 1, must not be taken into account (because these are not suitable for validating a lifetime model).

- The following limits from Table 9.4 for the PC_{min} test must be observed for verifying the lifetime model provided by the manufacturer:

Table 9.4: Limits for test parameters PC_{min}

Parameter		Value
On-time of the load current	t_{on}	> 15 s
Value of load current	I_L	> 0.85·I_{CN} [a]
Gate voltage	V_{gate}	typically 15 V [b]

[a] A value < 0.85·I_{CN} can be selected for the second sampling point and additional test conditions in order to allow a suitable difference of the temperature rises to be set.

[b] The gate voltage for testing IGBT and MOSFET can fall below the 15 V (e.g. when contact currents become too high), if – due to the thermal properties of the module – the desired temperature rise cannot be achieved with on-times of t_{on} > 15 s. For this, however, it must always be ensured that the switch is permanently operated in the saturated range. In these cases, the gate voltage used must only be set once at the start of the tests and documented in each case.

The module manufacturer must select the remaining parameters for the test as a function of the DUT properties, the test fixture and the temperature rise of the virtual junction temperature ΔT_{vj} in each case.

- For modules without base plate, a module-dependent and material-dependent settling process of the TIM material between module and cooling system must be taken into account for determining the starting values for forward voltage and temperature rise, and documented accordingly.

- The following parameters must be documented specifically for each module for the test:

Table 9.5: Module-specific test parameters PC_{min}

Parameter	
Temperature rise for virtual junction temperature (starting value for test after settling process)	$\Delta T_{vj,start}$
Duration of settling process (in cycles)	N_{start}
Load current	I_L
On-time of the load current (heating period)	t_{on}
Off-time of the load current (cooling period)	t_{off}
Average junction temperature	$T_{vj,avg}$
Maximum junction temperature at the start of the test	$T_{vj,max}$
Heat sink temperature (indirect cooled modules)	T_S
Base plate temperature (modules with base plate)	T_C
Coolant inlet temperature	T_{cool}
Gate voltage	V_{gate}
Thermal resistance (determined in the module test)	R_{th}

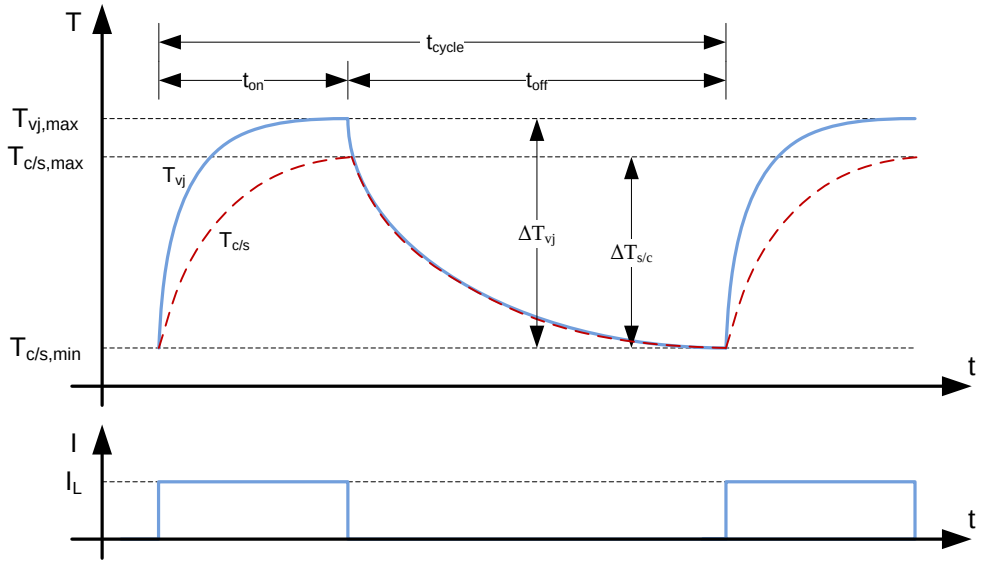

Figure 9.2: Current and temperature curve PC_{min}

- The DUTs shall at least be stressed until the first occurring EOL criterion has been reached. It is strongly recommended, however, to continue stressing the DUTs after reaching the first EOL criterion in the sense of improved evaluation of the results.

IEC 60749-34:2011, section 8: Measurement and tests

- Monitoring of the failure criteria must be implemented using the two parameters forward voltage (IGBT: $V_{CE,sat}$, MOSFET: V_{DS}, diode: V_F) and temperature rise of the virtual junction temperature ΔT_{vj} and other technology related parameters. These parameters must be monitored for each cycle during the entire test and documented accordingly.
- The EOL criteria must be tested by means of continuous parameter monitoring (see Table 9.6). For this it must be ensured that the measurement values are recorded with sufficient granularity regarding the expected lifetime in order to ensure meaningful and precise determination of the EOL.

IEC 60749-34:2011, section 9: Failure and evaluation criteria

- The failure criteria are defined as follows:

Table 9.6: EOL criteria PC_{min}

Parameter		**Change from standard value**
Forward voltage	IGBT: $V_{CE,sat}$ MOSFET: V_{DS} Diode: V_F, V_{FSD}	+5% [a]
Increase of thermal resistance	$R_{th,j-c}$, $R_{th,j-s}$, $R_{th,j-f}$ [b]	+20%

[a] Note: Also refer to the notes on the settling process under test conditions

[b] Note: It has to be ensured that the duration of temperature rise is sufficient for the calculation of static R_{th}, or an additional online R_{th} measurement should be performed without removing the power modules from the test bench, when TIM or a baseplate is part of the DUT.

- It is recommended to examine the DUTs for cracks on the soldering joints, substrates, die parts and the casings after the end of the test using scanning acoustic microscopy. Other relevant thermal and mechanical connections having impact on EOL criteria should be examined.

9.3.3 Requirement

The lifetime data $N_f = f(\Delta T_{vj}, T_{j,max}, t_{on})$ determined for the individual DUTs during the test must be marked in the reliability curve for the power electronics module provided by the manufacturer. A probability of N_f should be specified, e.g. 5%. It must be ensured that only DUTs are used whose failure patterns have identical failure mechanisms. DUTs with deviating failure mechanisms must be removed and the test must be repeated with new DUTs. The failure patterns/mechanisms of these removed DUTs must be documented. Failures of the semiconductor which cannot be clearly attributed to the aging of the assembly and interconnection technology are not permissible.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

The results and parameters of the test as per the specifications (see Annex C.2) must be documented. The lifetime data must be created.

9.4 QL-03 High-temperature storage (HTS)

9.4.1 Purpose

The purpose of this test is to test or determine the effect of storage at increased temperature on the power modules.

9.4.2 Test

The test must be conducted as per IEC 60749-6:2002, with the following additions:

IEC 60749-6:2002, section 4: Test sequence

- If the components to be tested are approved for a temperature higher than 125°C, this higher temperature must be used for the test.

IEC 60749-6:2002, section 4.1: Measurements

- For any intermediate measurements (if agreed with the purchaser), the DUTs must be removed from the test chamber at T_{RT} and also be inserted again at T_{RT}.

IEC 60749-6:2002, section 4.2: Failure criteria

- It is recommended to also examine the DUT during this test at the times defined above using SAM analysis and to document the degree of delamination at the connection points.

- The results and parameters of the test must be documented.

Table 9.7: Test parameters QL-03 High-temperature storage (HTS)

Parameter	Value
Test duration [a]	1 000 h
Ambient temperature $T_a = T_{stg,max}$	≥ 125°C (typ.) [b]
[a] Intermediate measurements as per Table 6.1 [b] If a higher value is defined in the data sheet, this value must be used for the test	

The scope of random samples for this test must be taken from the test flow chart.

9.4.3 Requirement

The DUTs must be fully functional after the test.

All data sheet parameters must be within the specifications.

The scope of the data sheet parameter drift analyses to be documented must be agreed upon with the purchaser.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

9.5 QL-04 Low-temperature storage (LTS)

9.5.1 Purpose

The purpose of this test is to test or determine the effect of aging or transport at a very low temperature on the power modules. A prolonged influence of low temperatures can cause embrittlement, crack formation and fractures on parts made of rubber and plastic as well as on parts made of metal, substrate, or semiconductor material.

9.5.2 Test

The test must be conducted as per JEDEC JESD-22 A119:2009, with the following additions:

JEDEC JESD-22 A119:2009 section 3.1: Low temperature storage conditions

- The test must be conducted at -40°C, which corresponds to condition A.
- If the components to be tested are approved for a temperature lower than -40°C, this lower temperature must be used for the test.

JEDEC JESD-22 A119:2009 section 3.2: Measurements

- For any intermediate measurements (if agreed with the purchaser), the DUTs must be removed from the test chamber at T_{RT} and also be inserted again at T_{RT}.

JEDEC JESD-22 A119:2009 section 3.3: Failure criteria

- It is recommended to also examine the DUT during this test at the times defined above using SAM analysis and to document the degree of delamination on the soldered points.
- The results and parameters of the test must be documented.

Table 9.8: Test parameters QL-04 Low-temperature storage (LTS)

Parameter	Value
Test duration [a]	1 000 h
Ambient temperature $T_a = T_{stg,min}$	≤ -40°C (typ.) [b]
[a] Intermediate measurements as per Table 6.1 [b] If a lower value is defined in the data sheet, this value must be used for the test	

The scope of random samples for this test must be taken from the test flow chart.

9.5.3 Requirement

The DUTs must be fully functional after the test.

All data sheet parameters must be within the specifications.

The scope of the data sheet parameter drift analyses to be documented must be agreed upon with the purchaser.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and during this qualification test must be taken from Table 6.1.

9.6 QL-05 High-temperature reverse bias (HTRB)

9.6.1 Purpose

This test is used to determine weak points in the chip passivation layer structure or the passivation topology and in the chip edge sealing over time.

The test focuses on production-related ionic contaminants which can migrate under the influence of temperature and fields and consequently increase surface charges. This can result in the formation of increased leakage currents. A degradation of the threshold voltage is also possible.

This is particularly important for chips installed without passivation, as in IGBT power modules and MOSFET modules.
The module assembly process and the coefficients of thermal expansion (CTEs) of the materials can also have a significant influence on the passivation integrity and consequently reduced protection against external contaminants.

9.6.2 Test

The test must be conducted as per IEC 60747-9:2007 section 7.1.4.1 (IGBT) and IEC 60747-8:2010 (MOSFET), with the following additions:

Table 9.9: QL-05 High-temperature reverse bias (HTRB)

Parameter	Value
Test duration [a]	≥ 1 000 h
Ambient temperature T_a	$T_{vj,max} - T_{(Pv)}$ [b]
Collector-emitter voltage or Drain-source voltage	$V_{CE} \geq 0.8\ V_{CE,max}$ (IGBT) $V_{DS} \geq 0.8\ V_{DS,max}$ (MOSFET)
Gate voltage	$V_{GE} = 0$ V (IGBT) $V_{GS} = 0$ V (MOSFET)
[a] Intermediate measurements as per Table 6.1 [b] $T_{(Pv)}$ defines the heat input in the semiconductor caused by the leakage losses	

Test parameters:

- During this test, the collector-emitter leakage current $I_{CE,leak}$ and/or the drain-source leakage current $I_{DS,leak}$ must be recorded continuously.
- The threshold voltage of the device $V_{GE,th}$ and $V_{DS,th}$ must be recorded before and after the test.
- The breakdown voltage of the device $V_{BR,CES}$ and $V_{BR,DS}$ must be recorded before and after the test and must be documented.
- The value of the test parameters used T_a, V_{CE} or V_{DS} and V_{GE} or V_{GS} must be documented in the test record.

Failure criterion:

- It must be ensured that the starting behavior or a possible stabilizing process during start up is within the specification (preventing pseudo failures).

- An increase in the collector-emitter leakage current $I_{CE,leak}$, the drain-source leakage current $I_{DS,leak}$ by a factor of 5 based on the initial value above the noise level of the measuring setup including DUT before the test (cold measurements at T_{RT}), or an increase above the value specified in the data sheet must be considered as a failure.

- Usually, an increase in leakage current beyond the failure threshold can be observed during the first hours of the test. This increase represents a displacement current, caused by applying the collector-emitter or drain-source voltage. When this current then drops to a stationary value within the specification again, a) an increase in leakage current by 100% must initially not be assessed as a failure and b) the reference value for evaluation of the subsequent leakage current increase must be set to the new stationary reference value.

- If the threshold voltage $V_{GE,th}$ or $V_{GS,th}$ is no longer in the specified range
  IGBT: $LSL < V_{GE,th} < USL$
  MOSFET: $LSL < V_{GS,th} < USL$
  after completing the test, the test must be considered as failed.

- The deviation of the leakage currents and of the threshold voltage from the initial value must be documented.

The scope of random samples for this test must be taken from the test flow chart.

The leakage current must be permanently monitored throughout the test duration. The test ends either when a defined test time is reached – then a) the increase in leakage current is compared to the start of the test (stationary value) and b) the leakage current values in the cooled state before and after loading are compared. If a) or b) exceed the defined failure thresholds, the test is regarded as failed. This test can also follow a defined failure threshold – then it runs until the maximum permissible leakage current has been reached.

9.6.3 Requirement

All data sheet parameters must be within the specifications.

The scope of the data sheet parameter drift analyses to be documented must be agreed upon with the purchaser.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

9.7 QL-06 High-temperature gate bias (HTGB)

9.7.1 Purpose

This test is not applicable to diodes.

This test is used to determine the combined effect of electrical and thermal load on semiconductor elements with gate connection (MOSFET and IGBT) over time. It simulates operating states under accelerated conditions and is used for device qualification and for reliability monitoring (burn-in screening) of installed gate dielectrics. In the framework of the qualification, the focus is on the validation of the specified lifetime period and the lifetime limit, while the reliability monitoring focuses on production-related premature failures.

The test is designed for evaluating:

a) The integrity of the gate dielectric
b) The condition of the semiconductor/dielectric boundary layer and
c) The contamination of the semiconductor through mobile ions

Note on a) The test accelerates the so-called time-dependent dielectric breakdown (TDDB), which either generates a resistant path between gate and source/emitter or gate and drain, or a low-breakdown diode between gate and source/emitter.

Note on b) Among other things, the thermal-electrical load also leads to the degradation of the boundary layer between semiconductor and gate isolator, which becomes evident through changed threshold voltages $V_{GS,th}$/$V_{GE,th}$ and a changed Miller capacity.

Note on c) The mobile contamination charge effective through increased temperature and electric field influence can degrade threshold voltages $V_{GS,th}$/$V_{GE,th}$, the Miller capacity, and the integrity or control effect of the gate isolator in the long term.

9.7.2 Test

The test must be conducted as per IEC 60747-9:2007 section 7.1.4.1 (IGBT) and IEC 60747-8:2010 (MOSFET), with the following additions:

Table 9.10: Test parameters QL-06 High-temperature gate bias (HTGB)

Parameter	Value	
	Variant 1	Variant 2
Test duration [a]	For each DUT ≥ 500 h, V_{GE} or V_{GS} > 0 ≥ 500 h, V_{GE} or V_{GS} < 0	50% of the DUTs, each with ≥ 1 000 h, V_{GE} or V_{GS} > 0 ≥ 1 000 h, V_{GE} or V_{GS} < 0
Ambient temperature T_a	$T_{vj,max}$	
Collector-emitter voltage or Drain-source voltage	V_{CE} = 0 V (IGBT) V_{DS} = 0 V (MOSFET)	
Gate voltage	V_{GE} = $V_{GE,max}$ (IGBT), DUT switched off V_{GS} = $V_{GS,max}$ (MOSFET), DUT switched off	
[a] Intermediate measurements as per Table 6.1		

Test parameters:

- During this test, the gate-emitter leakage current $I_{GE,leak}$ and/or the gate-source leakage current $I_{GS,leak}$ must be recorded continuously.

- The threshold voltage of the gates $V_{GE,th}$ (IGBT) and $V_{GS,th}$ (MOSFET) must be recorded before and after the test.

- The value of the test parameters used T_a, V_{CE} or V_{DS} and V_{GE} or V_{DS} must be documented in the test record.

Failure criterion:

- An increase in the gate-emitter leakage current $I_{GE,leak}$, the gate-source leakage current $I_{GS,leak}$ by a factor of 5 based on the initial value above the noise level of the measuring setup including DUT before the test (cold measurements at T_{RT}), or an increase above the value specified in the data sheet must be considered as a failure.

- If the threshold voltage $V_{GE,th}$ or $V_{GS,th}$ is no longer in the specified range
  IGBT: $LSL < V_{GE,th} < USL$
  MOSFET: $LSL < V_{GS,th} < USL$
  after completing the test, the test must be considered as failed.

The scope of random samples for this test must be taken from the test flow chart.

9.7.2.1 Test setup

In the path of the gate control, a current-limiting series resistor or an intelligent circuit breaker (may already be implemented in commercial measuring equipment) must be implemented in the test setup to prevent energy discharge in the semiconductor.

9.7.3 Requirement

All data sheet parameters must be within the specifications.

The scope of the data sheet parameter drift analyses to be documented must be agreed upon with the purchaser.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

9.8 QL-07 High-humidity, high-temperature reverse bias (H3TRB)

9.8.1 Purpose

This test determines weak points in the overall module structure, including the power semiconductor itself. Most module designs are not hermetically sealed. Semiconductor chips and bonding wires are embedded in silicone gel which is permeable to humidity. This allows the moisture to also reach the passivation layer over time. Weak points in the chip passivation layer structure or the passivation topology and in the chip edge sealing are affected differently by loads under the influence of humidity. Contaminants can also be transferred to critical areas through moisture transport.

The focus is on production-related ionic contaminants which migrate under the influence of temperature and fields and consequently increase surface charges, as well as on thermomechanical stresses on the housing and the interaction with semiconductor chips. This can result in the formation of increased leakage currents. The focus is also on corrosive substances introduced through the influence of corrosive gas and the interaction of these substances with the assembly and interconnection technology and with the chip.

The module assembly process and the coefficients of thermal expansion (CTEs) of the materials can also have a significant influence on the passivation integrity and consequently reduced protection against external contaminants. Mechanical stress generally leads to a higher sensitivity for (electro-) chemical corrosion.

9.8.2 Test

The test must be conducted as per IEC 60749-5:2003, with the following additions:

IEC 60749-5:2003 section 5.2: Guidelines for electric voltage load

- In contrast to the standard, which permits a selection between constant and intermittent voltage load, the variant as per section 5.2 e)1) "Testing with constant voltage load" must be conducted.

- This test must be conducted with permanently blocked DUTs.

IEC 60749-5:2003 section 5.2.1: Selecting the test loads and test report

- Omitted

Table 9.11: Test parameters QL-07 High-humidity, high-temperature reverse bias (H3TRB)

Parameter	Value
Test duration [a]	≥ 1 000 h (switched off)
Temperature	85°C (constant)
Relative humidity	85%
Collector-emitter voltage[b] or Drain-source voltage	$V_{CE} = 0.8 \cdot V_{CE,max}$ (IGBT), max. 80 V $V_{DS} = 0.8 \cdot V_{DS,max}$ (MOSFET), max. 80 V
Gate voltage	V_{GE} = 0 V (IGBT) V_{GS} = 0 V (MOSFET)
[a] Intermediate measurements as per Table 6.1 [b] To avoid locally reducing the relative humidity influence too strongly through power loss created by leakage currents, the voltage applied to devices must be set to 80% of the specified nominal breakdown voltage.	

Test parameters:

- During this test, the collector-emitter leakage current $I_{CE,leak}$ or the drain-source leakage current $I_{DS,leak}$ must be recorded continuously.

- The threshold voltage of the gates $V_{GE,th}$ and $V_{GS,th}$ must be recorded before and after the test.

- The value of the test parameters used V_{CE} or V_{DS} and V_{GE} or V_{GS} must be documented in the test record.

- Examinations on modules which are exposed to an atmosphere with corrosive gases must be agreed upon with the purchaser.

Note:
Additional examinations with higher collector-emitter or drain-source voltages can accelerate corrosion on the assembly and interconnection technology (e.g. guard ring structure). The risk of failures caused by cosmic rays can increase.

Failure criterion:

- An increase in the collector-emitter leakage current $I_{CE,leak}$ or the drain-source leakage current $I_{DS,leak}$ by a factor of 10 based on the initial value above the noise level of the measuring setup including DUT before the test must be considered as a failure.

- If the threshold voltage $V_{GE,th}$ or $V_{GS,th}$ is no longer in the specified range
  IGBT: $LSL < V_{GE,th} < USL$
  MOSFET: $LSL < V_{GS,th} < USL$
  after completing the test, the test must be considered as failed.

The scope of random samples for this test must be taken from the test flow chart.

9.8.2.1 Test sequence

The DUT must be subjected to a module test (section 6.1) before the load test. This is to ensure that only flawless DUTs enter into the H3TRB.

Over the test duration, the leakage current is measured before and after loading, or, if necessary, with an interruption of the loading. The test ends either when a defined test time is reached – then a) the increase in leakage current is compared to the start of the test (stationary value) and b) the leakage current values in the cooled state before and after loading are compared. If a) or b) exceed the defined failure thresholds, the test is regarded as failed. This test can also follow a defined failure threshold – then it runs until the maximum permissible leakage current has been reached.

The deviation of the collector-emitter leakage current or drain-source leakage current and of the threshold voltage from the initial value must be documented for verifying the validity of the failure criterion.

When measuring the leakage current after loading, it must be ensured through appropriate storage periods and/or suitable heating processes that any residual moisture in the DUT cannot distort the measuring results.

9.8.3 Requirement

All data sheet parameters must be within the specifications.

The scope of the data sheet parameter drift analyses to be documented must be agreed upon with the purchaser.

The parameters are verified with the use of a module test (see section 6.1). The tests to be conducted after and before this qualification test must be taken from Table 6.1.

Annex A: Test flow chart (normative)

The numbers in the test flow chart in following figures indicate the number of topological switches to be tested (compare section 4.1.2).

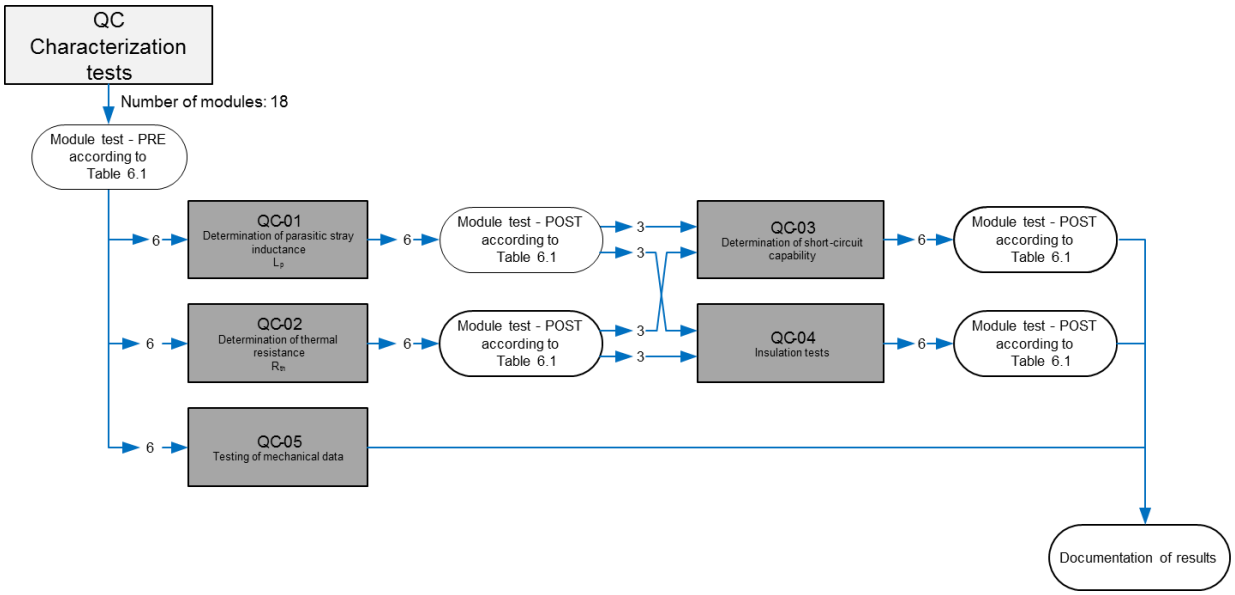

Figure A.1: Test flow chart QC

Note:
The test flow chart QC attempts to minimize the number of DUTs by using DUTs multiple times in case of non-destructive testing. As an alternative, all tests can also be conducted with new modules.

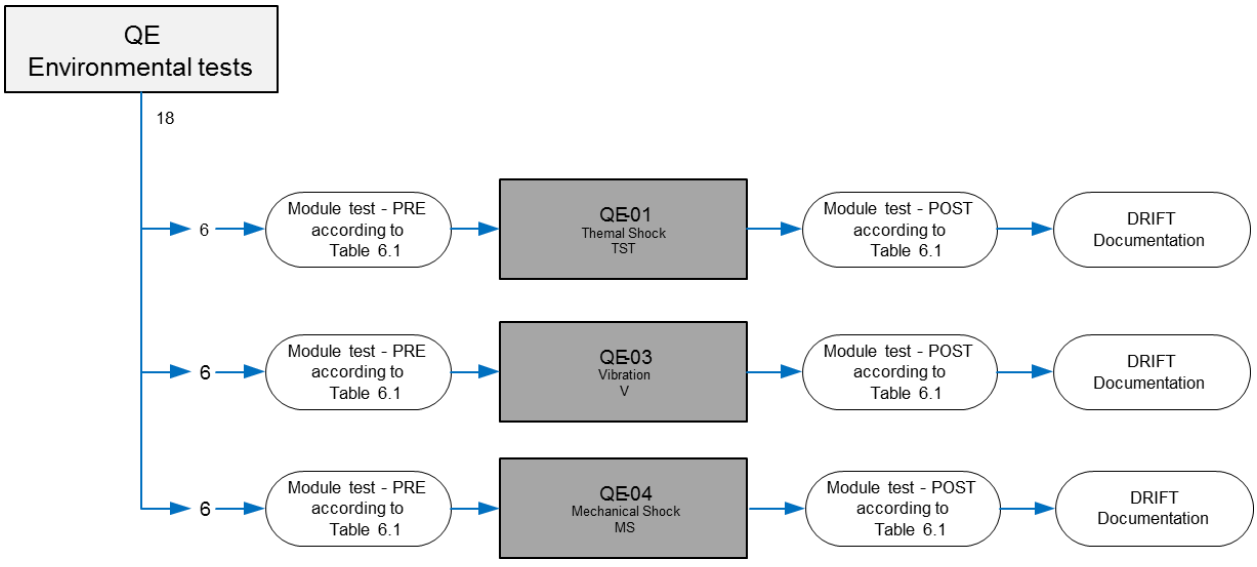

Figure A.2: Test flow chart QE

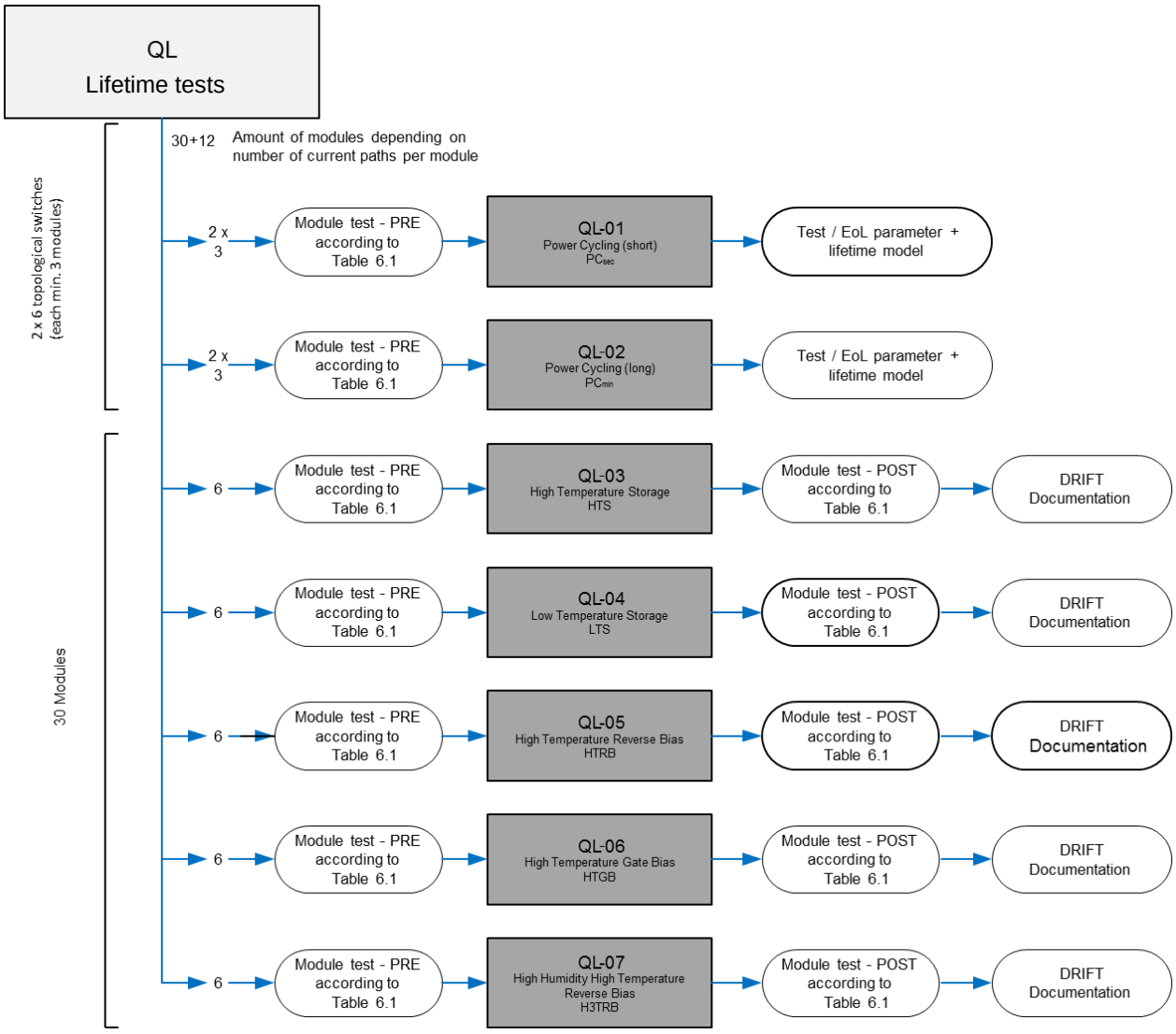

Figure A.3: Test flow chart QL

Annex B: Delta qualification matrix (normative)

Table B.1: Qualification matrix

Qualification matrix		*Characterization entrance tests*						*Environmental tests*					*Lifetime tests*							
		QC-01 Determination L_p	**QC-02** Determination R_{th}	**QC-03** Short Circuit Capability	**QC-04** Insulation Test	**QC-05** Mechanical Data		**QE-01 TST** Thermal Shock	**QE-02 CO** [a] Contactability	**QE-03 V** Vibration	**QE-04 MS** Mechanical Shock		**QL-01 PC(sec)** Power Cycling (short)	**QL-02 PC(min)** Power Cycling (long)	**QL-03 HTS** High Temp. Storage	**QL-04 LTS** Low Temp. Storage	**QL-05 HTRB** High Temp. Rev. Bias	**QL-06 HTGB** High Temp. Gate Bias	**QL-07 H^3TRB** High Humidity, High Temp. Rev. Bias	
Material or geometry change of base plate			x		x	x		x		x	x			x						
Material or geometry change of substrate		x	x	x	x			x						x					x	
Change of material or geometry of package (gel, plastic frame, mold compound)		x			x	x		x		x	x				x	x		x	x	
Change of material or geometry of the terminals (frame bond wire, mold compound etc.)		x		x	x	x		x		x	x				x	x		x	x	
Change of at least one contact area of the semiconductor device		x	x	x	x								x	x					x	
Use of a different or new material for the die attach (solder, sinter material, etc.)			x	x	x					x	x		x	x			x	x	x	
Use of a different or new material for system solder (solder, sinter material, etc.)			x		x			x		x	x		x	x			x	x	x	
Use of different or new semiconductor device or semiconductor material or passive elements of the same or a different manufacturer		x	x	x	x			x					x	x			x	x	x	
Use of a different or new contact technology for die attach of semiconductor devices (soldering, sintering, diffusion soldering, etc.)			x	x	x			x					x	x			x	x	x	
Use of a different or new contact technology for top side connection of semiconductor devices (e.g. wire bond, ribbon bond, copper clip, sinter technology, etc.)		x	x	x	x					x	x		x	x			x	x	x	

Generic data:
The use of generic data per test is permissible (except for characterization tests) as part of module qualification as long as the difference between the module to be qualified and the reference module is documented and it can be verified that the differences between the reference module and the module to be qualified do not cause any changes in the module's properties.

[a] According to chapter 8.3 it is pursued to specify suitable and beneficial testing routines for 'contactability' in later releases. Therefore, this empty column is inserted intendedly already now as a placeholder.

Annex C: Documentation of tests (normative)

The following defines which parameters of the individual tests must be documented as a minimum. Documentation of the tests must be provided in written form as part of the Production Part Approval Process (PPAP) documents.

C.1 Template for PC_{sec} test

Test:		***PC_{sec}***	
Temperature rise	ΔT_{vj}	*Value*	[K]
Maximum junction temperature	$T_{vj,max}$	*Value*	[°C]
Average junction temperature	$T_{vj,avg}$	*Value*	[°C]
Feed temperature	T_{cool}	*Value*	[°C]
Heating duration	t_{on}	*Value*	[s or min]
Cooling time	t_{off}	*Value*	[s or min]
Load current	I_L	*Value*	[A]
Gate voltage	V_{gate}	*Value*	[V]

Reliability data		
DUT no.	Cycles until EOL	Failure pattern failure cause (V_{CE}, ΔT)
1	*Xxxxx*	
2	*Xxxxx*	
3	*Xxxxx*	
4	*Xxxxx*	
5	*xxxxx*	
6	*xxxxx*	
…	*xxxxx*	

Lifetime model	
IGBT	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$
Diode	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$
Solder	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$

The parameters $V_{CE/DS/F} = f(N)$ and $\Delta T_{vj} = f(N)$ must be shown graphically for the individual DUTs for each test and each tested temperature rise $\Delta T_{vj,1}$ … $\Delta T_{vj,n}$. For this, the parameters of all modules in one test series can be included in one diagram. The procedure for creating the reliability diagram must be documented (allocation of the probability of failure to the individual test results, method for the regression to the Weibull density, basis for the lifetime model (e.g. Arrhenius, Coffin-Manson, CIPS2008)).

If the examination was conducted with scanning acoustic microscopy (SAM), the images from the examinations must be documented accordingly.

C.2 Template for PC_{min} test

Test:		***PC_{min}***	
Temperature rise	ΔT_{vj}	*Value*	[K]
Maximum temperature of system soldering/casing	$T_{c/s,max}$	*Value*	[°C]
Maximum temperature of system soldering/casing	$T_{c/s,min}$	*Value*	[°C]
Maximum junction temperature	$T_{vj,max}$	*Value*	[°C]
Feed temperature	T_{cool}	*Value*	[°C]
Heating duration	t_{on}	*Value*	[s or min]
Cooling time	t_{off}	*Value*	[s or min]
Load current	I_L	*Value*	[A]
Gate voltage	V_{gate}	*Value*	[V]
Therm. resistance	R_{th}	*Value*	[K/W]

Reliability data		
DUT no.	Cycles until EOL	Failure pattern failure cause (V_{CE}, ΔT)
1	*xxxxx*	
2	*xxxxx*	
3	*xxxxx*	
4	*xxxxx*	
5	*xxxxx*	
6	*xxxxx*	
…	*xxxxx*	

Lifetime model	
IGBT	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$
Diode	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$
Solder	$N_f = f(\Delta T_{vj}, T_{vj,max}, t_{on})$

The parameters $V_{CE/DS/F} = f(N)$ and $\Delta T_{vj} = f(N)$ must be shown graphically for the individual DUTs for each test and each tested temperature rise $\Delta T_{vj,1}$ … $\Delta T_{vj,n}$. For this, the parameters of all modules in one test series can be included in one diagram. The procedure for creating the reliability diagram must be documented (allocation of the probability of failure to the individual test results, method for the regression to the Weibull density, basis for the lifetime model (e.g. Arrhenius, Coffin-Manson, CIPS2008)).

If the examination was conducted with scanning acoustic microscopy (SAM), the images from the examinations must be documented accordingly.

C.3 Template for TST test

Test:	***TST***		
Temperature rise	ΔT	*Value*	[K]
Minimum temperature	$T_{stg,min}$	*Value*	[°C]
Maximum temperature	$T_{stg,max}$	*Value*	[°C]
Cycle time	t_{cycle}	*Value*	[s/min]
Duration of temperature cycle	t_{change}	*Value*	[s]
Hold time at $T_{min/max}$	t_{dwell}	*Value*	[min]

Test results		
DUT no.	Cycles	Failure pattern failure mechanism
1	*xxxxx*	
2	*xxxxx*	
3	*xxxxx*	
4	*xxxxx*	
5	*xxxxx*	
6	*xxxxx*	
…	*xxxxx*	

Parameter drift			
DUT no.	R_{th} [K/W]		
	0	500	1 000
1			
2			
3			
4			
5			
6			
…			

If the examination was conducted with scanning acoustic microscopy (SAM), the images from the examinations must be documented accordingly.

Annex D: References (informative)

[1] U. Scheuermann, S. Schuler: Power Cycling Results for Different Control Strategies, Microelectronics Reliability 50 (2010), 1203-1209

[2] U. Scheuermann, R. Schmidt: Investigations on the V_{CE}(T)-Method to Determine the Junction Temperature by Using the Chip Itself as Sensor, PCIM 2009, Nuremberg, Germany

Annex E: Typical aspects for physical analysis (informative)

The final analysis can comprise the following scopes, for example (as far as applicable):

- Bolt release torques (e.g. threaded connections on casings, fastening screws on the shaker table)
- Analysis of the soldered or sintered connections of chips and substrates
- Analysis of the remaining bond properties
- Setting behavior of threaded connections
- Residual distribution of heat-conducting media
- Properties of seals
- Creepage under seals
- Failures in soldered connections
- Device/PCB discolorations (especially due to thermal causes)
- Flaws, cracks, deformation of materials (especially for potting and sealing materials). A suitable test method (e.g. x-ray, CT, SAM, micro-sections) must be selected for this in agreement
- Condition of latching mechanisms and clips
- Traces of corrosion and migration
- Evaluation of plastics for resistance to hydrolysis
- Connector pin damage (e.g. due to current, temperature, friction, oxidation)
- Other irregularities