The Superjunction Principle as Enabling Technology for Advanced Power Solutions

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I. INTRODUCTION

Power management and power consumption are gaining more and more importance in recent years. While the battery life time of portable gear may influence directly the buyers decision, it also plays a decisive role in the implementation of additional features in the product, hence influencing the product functionality. In non-mobile power solutions efficiency is a major driving factor, enabling to increase the output power in a given power supply size with little or no changes to the cooling system.
The quality of a power solution is crucially influenced by the power control IC and the power switches. Whereas standby power losses, power factor, safety features in abnormal operation conditions, ripple of the output voltages, system reaction on load jumps are mainly determined by the control IC, the power switches are the major corner stone in optimizing power density, efficiency, system size and weight.
The interaction of control IC, power switch and passive components as the major third party is therefore the decisive factor to step forward on the path to more efficient, more compact and lightweighted power solutions.

The field of applications for power supplies ranges from mobile phone chargers with an output power of 1-5 W up to several kW for telecom or multi-processor server solutions. In the low end of this spectrum cost seems to be the only factor which matters. We see here from a technological perspective a step back towards bipolar power switches and very simple control algorithms, which can be realized without control ICs. Examples for this segment are mobile phone chargers using ringing choke converters (RCC) or cold fluorescent lamps (CFL) with free oscillating control schemes. Above these applications there is a wide range of products where standby power, electromagnetic interfererence and system reaction to load jumps are adding value to the power solution proposed. Typical examples are DVD recorders / players, set-top boxes, printer adapters etc. Technologically we see here several competing approaches encompassing monolithical solutions, which integrate lateral or vertical power switches with the control IC on one piece of silicon, system-in-a-package solutions with two or more dedicated chips in one package, and discrete solutions with separate packages for control IC and power switches. The high power segment is driven mainly by efficiency and a trend towards lower system complexity and hence faster time-to-market. Typical applications are notebook adapters, power supplies for flat panel TVs and server. These applications are dominated by discrete solutions, main focus is laid on the optimization of power architectures and components.

Looking on the power switch the main progress made in the last decade has been due to the introduction of the superjunction principle for power MOSFETs [1-5]. With the latest generation the area specific RDSon has been cut by a factor of 7 in comparison to state-of-the art in the early nineties. The switching speed went up accordingly by a factor of up to 5, wheras the gate charge went down by a factor of 5. The basic principle of superjunction is that the charge required for low conduction losses is counterbalanced by additional charges of the opposite type, being arranged in close packed stripe or column layouts. Consequently the principle allows to reduce the RDSon without sacrificing blocking voltage. The concept is only limited by the precision, with which the net charge – the difference between p- and n-doping – can be controlled.

This article will focus on the benefit and the potential of the superjunction principle for high and mid power solutions. We will discuss the impact on power supply topologies and control ICs in efficiency and system complexity driven applications as well as the potential of superjunction devices in system-in-a-package solutions.

II. MID POWER SOLUTIONS

Once you have access to an optimized vertical power MOS technology, it is the obvious choice to copackage this power switch with a control IC. Using multiple combinations of power MOSFETs with different control ICs facilitates the generation of a broad product portfolio. Chip-on-chip mounting allows to go for nearly the same low RDSon than a discrete solution but by saving additional costs and space for the IC package plus wiring. Furthermore, additional external components like the start-up circuit, which requires at least a 600 V cell can be integrated. Our CoolSET F3 products solve this task by incorporating a depletion MOS cell into the vertical power MOSFET. This cell allows at 0 V gate level to draw a start-up current of several mA when the drain voltage comes up. This current charges the supply cap for

the control IC. At a given upper threshold voltage the control IC starts operating the main switch. As soon as the auxiliary winding on the main transformer takes over to supply the control IC, the depletion cell is turned off with a negative gate voltage relative to its source potential. As this source potential is on the supply level of the control IC zero potential relative to the source of the main switch is sufficient to turn these cells off. A negative voltage with reference to logic ground is therefore not required. The use of an internal start up cell has besides saving costs the advantage that the ESD sensitive cell is not connected to external circuitry. Furthermore the start up current is independent on the input voltage. The starting time for the system is therefore in contrast to an external voltage divider always constant. Fig. 1 shows a basic setup for a 15 W power solution using a CoolSET F3 in flyback configuration.

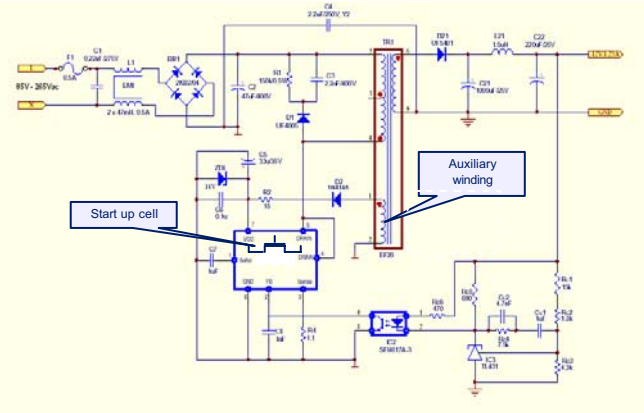

Fig. 1: 15 W SMPS demoboard using CoolSET F3 in flyback topology.

Low standby losses, as being increasingly demanded by customers, are naturally facilitated by the use of a switchable start-up circuit. Additonally active burst mode is used to further lower the standby power losses. Burst mode means that the power switch is only operated from time to time with a set of pulses but inactive in long time intervals in between. When load jumps occur the burst mode is instantly terminated and normal operation mode is entered. This *active* monitoring allows a good system response on load jumps.

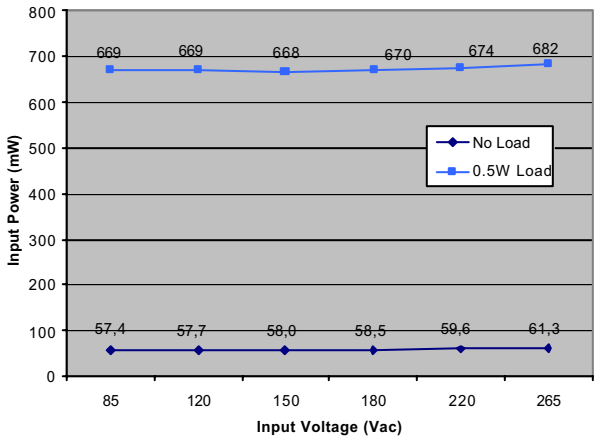

Fig. 2: Standby losses of the board shown above.

With the demonstration board showed in Fig. 1 standby power consumption of less than 60 mW was measured over the entire input voltage range. Fig. 2 shows the results. With further progress in vertical superjunction devices the CoolSET products can naturally expand their power range to higher levels.

What are however the limitations of the combination of a vertical power MOSFET copackaged with a control IC? With decreasing output power the current through the MOSFET will also decrease. Let´s assume wide range input and an output power of 10 W. Typical RDSon for this solution would be in the range of 5 to 10 Ohm. Note that efficiency is not the major driving factor in this application range, the only request is to get out the heat from the power switch. In conventional power MOSFET technology the active area required for 10 Ohm is just above 1 mm², whereas in superjunction technology it is below 0.3 mm². To the active area we have to add inactive areas like chip corners, gate pad, start up circuitry which in sum account to 0.3 mm² typically independent on the RDSon of the switch. Furthermore we have to add inactive areas for the edge termination which linearly increase with 1/RDSon. Consequently we get for a 10 Ohm switch in vertical superjunction technology an active area usage of less than 30% and in conventional technology of less than 50%.

The usage of lateral device concepts [6] seems therefore to be the natural choice, as these concepts allow to surround an inner drain electrode by an outer source electrode. This scheme eliminates the need for a high voltage edge termination and hence significantly reduces the amount of areas not contributing to the current flow.

The lateral concept is however also not free of inactive areas: The contribution of source, gate and drain metallization pads on the surface as well as the less effectively used space in curvatures of the lateral transistor structure are not to be underestimated. Nevertheless a lateral transistor structure can afford a higher area specific on-resistance, if production costs are similar to the vertical power MOSFET. The better the RDSon of the lateral concept is, the wider the range of products will be with better cost structure than the vertical concept. Calculations show a feasible product window for lateral superjunction technologies if the RDSon*A is up to a factor 2 higher.

The main drawback of lateral concepts is its less efficient use of the bulk material for current flow. For a 600 V technology a lateral concept will require a drift length of 50 µm. Adding some space for source, gate and drain wiring will lead to an effective design rule of typically 70 to 80 µm. Choosing similar doping conditions as for a comparable vertical device concept and hence similar electric field profiles and process windows, will require an effective cross section used for lateral current flow of at least 35 µm depth for a superjunction technology and around 50 µm for a conventional technology. These values do not allow to use a lateral MOS channel due to ineffective current spreading into the depth of the lateral transistor structure. This hurdle can be overcome by

trenched source and gate structures, but technology costs will go up.

The motivation for lateral device concepts has therefore not to rely on the one-to-one replacement of vertical power MOSFETs. Cooling in dual-in-line packages may be one of those aspects, as a lateral device may be cooled via source or near source potential, whereas vertical devices require cooling via drain potential. Furthermore isolation is facilitated especially in TO packages. Potential integration of additional system functionality like current and voltage sensors or active zenering are typically easier to integrate with lateral devices. The decision which way to go – lateral or vertical device concepts – is therefore very much determined from the focus application segment and the accessible technologies. With an area specific RDSon advantage of 5 versus conventional power MOSFET technology, no matter which concept to choose, the way will always require superjunction principles.

III. HIGH POWER RANGE

In this segment low RDSon (< 1 Ohm - << 1 Ohm) is a must. Output power ranges from 90 W in notebook adapters to several kW in server or telecom applications. Active power factor correction is standard, in many cases continous current mode is used. The main power stage uses typically half or full bridge topologies in many cases in zero-voltage (ZVS) or zero-current switching (ZCS) architectures.

A power technology which allows to cut the RDSon significantly and offers the best RDSon in a given package outline is the natural choice. This plug-and-play replacement will certainly drive the efficiency of the system up and will save precious time in otherwise detailed optimization of the thermal management.

But looking on the interaction of control IC and power switch what more can be done? The designers of power supplies are today accustomed to resonant topologies like the phase-shift ZVS bridge, because conventional MOSFETs are switching too slow to get the switching losses low enough. They are hence forced to add passive reactive components which store some part of the energy. This energy can then be used to charge the power switch capacitances to achieve zero voltage switching. The obvious drawback of this approach are complex control schemes and system, additional components, usage of the body diode. Furthermore the efficiency can only be optimized at a given load point, which is typically full load condition. At low load condition the energy stored in the reactive components is typically not high enough to recharge the power switches completely. Loss of ZVS operation leading to a substantial loss of efficiency are the consequences.

We went therefore into an investigation whether the best available superjunction technology in a simple hard switching topology can reach the efficiency of a fully optimized phase shift ZVS bridge being equipped with the best conventional state-of-the-art devices. The topology of choice is the two-transistor-forward, being used in an interleaved setup (ITTF) with two identical stages working on the same output cap. Fig. 3 shows the two topologies.

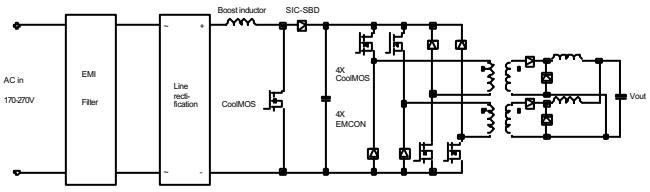

Fig. 3a: Circuit diagram of the interleaved two-transistor-forward topology.

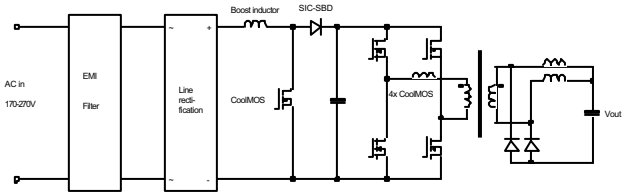

Fig. 3b: Circuit diagram of the phase-shift ZVS full bridge.

An identical design approach was used. Both boards use identical PFC stages and nearly identical output stages. The output power is 1000 W, the output voltage is 48 V, PFC and PWM stage run at 130 kHz.

The phase shift ZVS bridge reaches at full load an efficiency of 90.9 % using the best 500 V devices in TO220 packages with 250 mOhm on-resistance. The ITTF board reaches over the entire load range better results, at full load the efficiency is 91.2% using the latest superjunction technology CoolMOS™ C5 with an RDSon of below 100 mOhm in the TO220 at 600 V blocking voltage.

The same devices boost the efficiency of the phase shift ZVS to 92.4% but only at full load. As shown in Fig. 4 the efficiency of the phase shift ZVS drops substantially at low load condition. As the typical operation condition in servers is due to redundant power supplies at 1/3 to half load, the efficiency at this point of load is of major importance.

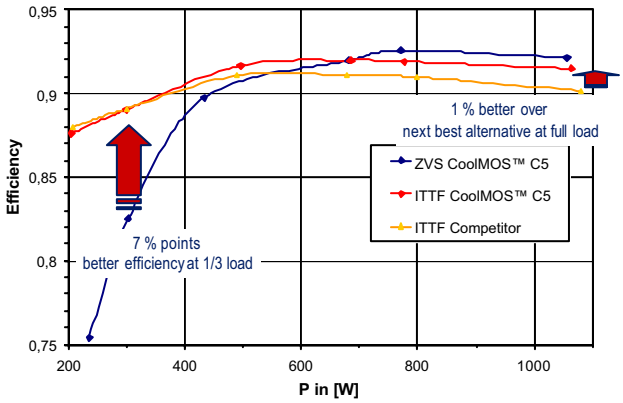

Fig. 4 Efficiency comparison of a hard switching interleaved two transistor forward topology to a resonant phase shift ZVS bridge using TO220 best-in-class devices.

The results above show that the progress in superjunction technology allows to rethink the paradigms of high power architectures. The necessity to go for resonant topologies is no longer existing. The superjunction principle acts as the enabling technology for advanced power solutions.

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