Aging Assessment of Discrete SiC MOSFETs under High Temperature Cycling Tests

Enes Ugur, *Student Member, IEEE,* and Bilal Akin, *Senior Member, IEEE*
Electrical and Computer Science Department, Power Electronics and Drives Laboratory
University of Texas at Dallas
Richardson, TX, USA
enes.ugur@utdallas.edu; bilal.akin@utdallas.edu

***Abstract*— Silicon carbide (SiC) power MOSFETs have been becoming a strong alternative to silicon (Si) technology in high-voltage, high-frequency, and high-temperature applications. Despite their growing market share, limited field information is available regarding the aging facts under thermal stress and long term reliability of discrete SiC MOSFETs. In this paper, discrete SiC devices are thermally aged through a custom designed high temperature power cycling setup controlled by TI 28335 microcontroller. On-state resistance variation of devices is continuously monitored and stored in each cycle, while other electrical parameters are captured at certain intervals by utilizing an automated curve tracer. Variation of electrical parameters throughout the cycles is presented in order to assess their correlation with the aging/degradation state of the switch. The discussions regarding aging precursors are supported by structural changes obtained through scanning acoustic microscopy (SAM) and cross-sectioning.**

Keywords*— *Silicon Carbide (SiC), power MOSFETs, reliability, robustness, aging assessment, accelerated power cycling.

I. INTRODUCTION

SiC power semiconductors have become a strong alternative in a wide spectrum of power electronics systems, particularly in high power and high temperature applications. Compared to their Si counterparts, SiC devices are capable of higher blocking voltage, switching speeds, power handling capacity and thermal conductivity which enables having high efficiency and high power density power converters in automotive industry, grid connected systems, etc. [1]–[5]. As a natural choice of harsh operating environments, SiC MOSFETs are subjected to various mechanical and electrical stresses, wear, and vibration together with extreme temperatures, which contribute to increased equipment failure potential. A failed component can cause catastrophic failures, serious safety issues, or easily result in millions of dollars of repair costs.

Due to high costs of SiC, the size of the chips are usually much smaller compared to Si devices at the same voltage level [6]. Hence, for the same power level, the SiC chips have higher power density and they require better heat dissipation and cooling design in order to handle higher local current densities. Although there are several SiC MOSFETs products in the market, limited information is available on reliability of these devices in comparison to the literature addressing the reliability of Si based power devices. From reliability perspective, short circuit capability [7]–[9], and single pulse avalanche ruggedness of commercial SiC MOSFETs and their aging under repetitive stress conditions [10] have been evaluated. Temperature induced formation of a conductive path through the gate oxide resulting with the inability to block drain–source voltage and thermal generation current induced thermal runaway are identified as failure mechanisms. The SiC/SiO_2 interface charge trapping related gate threshold voltage drift is another reliability concern and the decrease of the conduction band offset at semiconductor crystal - SiO_2 interface is found to be responsible for this effect [5].

Another major reliability issue arises in certain applications where the ambient temperature or coolant temperature require operation above the datasheet required limits (150~175°C), like automotive power train, oil & gas down-hole tractors and military applications. Available power module fatigue models shows that increasing the junction temperature from 150 to 200°C reduces lifetime under thermal cycles by a factor of fifty [6]. Since the trend of SiC applications is increasing the power handling capability in order to decrease cooling system costs, comprehensive reliability and aging evaluation of SiC MOSFETs for high temperature applications is necessary. In the literature, there are several studies dealing with reliability testing at high temperature conditions. High temperature gate bias (HTGB), gate switching and high temperature stress tests at 175 and 200 °C are carried out [11], [12]. On the other hand, a few studies have investigated temperature change induced aging and long term reliability of SiC MOSFETs. Power cycling tests (PCTs) using SiC MOSFETs are carried out in [13], [14], while keeping the junction temperatures within the Safe Operating Area (SOA). In [15], tests are carried out in order to find a reliable protocol for power cycling of SiC-MOSFET devices in high temperature conditions.

Another aspect of reliability is the identification of aging precursors in order to detect device degradation in real-time. Several publications on Si based devices have shown that the degradation of the device causes a gradual variation in the on-state resistance ($R_{ds,on}$) of MOSFETs [16], [17]. The gate threshold voltage and body diode forward voltage (V_{ds}) are also identified as failure precursors for power MOSFETs [18], [19]. On the other hand, a few studies have investigated the failure precursors in SiC MOSFETs. On state resistance is monitored through the voltage drop across the device and an increasing trend in on-state resistance was observed with aging [13], [14]. Yet, the effects of thermal aging on the electrical parameters of SiC MOSFET have not been analyzed in detail.

This work was supported by the National Science Foundation under Grant 1454311.

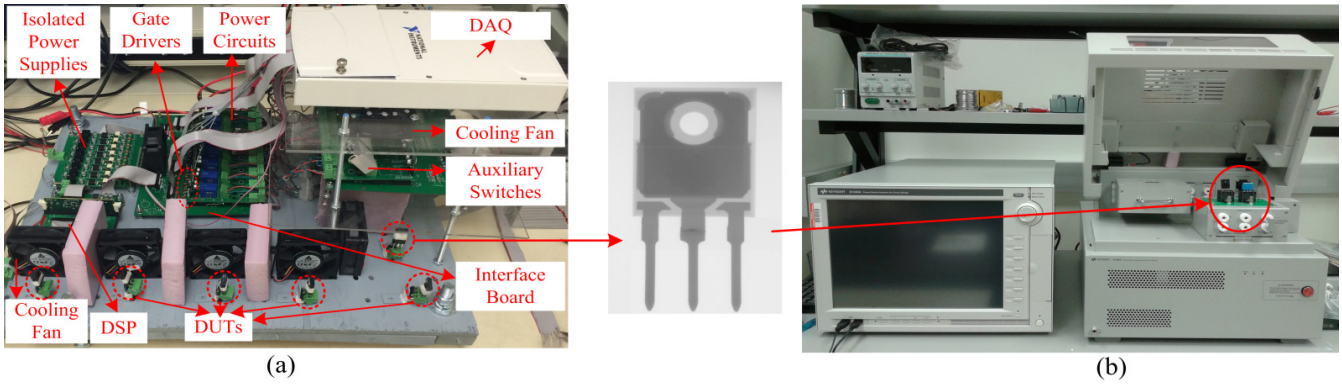

Fig. 1. Illustration of the test-bed; (a) custom designed aging setup, (b) curve tracer [21].

This paper presents comprehensive analyses of thermally aged SiC MOSFETs through high temperature power cycling. An accelerated power cycling test method is performed on a custom-designed test-bed presented in [20]. On-state resistance variation is continuously captured in each cycle throughout the end of device life. In addition, the switches are removed from the test-bed and placed on the Keysight B1506A automated curve tracer periodically, as shown in Fig. 1. Variations in electrical parameters of thermally aged SiC MOSFETs are investigated comprehensively based on the data collected at the curve tracer. The devices are also inspected using the C-Mode Scanning Acoustic Microscopy (C-SAM), the THRU-Scan Acoustic Microscopy (T-SAM) and cross-sectioning to verify the results found by the electrical parameter variations.

II. ACCELERATED POWER CYCLING

In a power converter application, the power semiconductor devices always heat up and cool down due to varying load conditions, switching actions, electrical cycles etc. This temperature cycling leads to thermo-mechanical stresses on the adjacent layers due to coefficient of thermal expansion (CTE) mismatches and eventually wears out the contact points [21]. Temperature cycling and power cycling are two widely acknowledged test methods for investigating the effect of periodical temperature changes on the device packaging. The temperature cycling changes the device temperature by cycling the environmental temperature between the upper and the lower limits. This testing method is more suitable to test large area interfaces and the testing conditions are quite different from the actual operation conditions. On the other hand, power cycling method uses the power losses of the chip to heat up the device (active heating) and cool down the device with the traditional cooling methods. This provides a thermal and stress distribution on the device which is similar to a real application conditions. Although, typically, current or power level is controlled in power cycling, the temperature can also be regulated by controlling the heating and the cooling phases [13].

Since the power devices are designed to operate for millions of cycles under normal operation conditions, it would take very long time to implement a reliability experiment under nominal conditions. To accelerate the aging process, accelerated power cycling tests are introduced and widely used in the literature [20]. In most of the studies DUTs are mounted on cooling system where relatively high load current is injected in order to achieve faster cycling. This increases the thermo-mechanical stress on the bond wires and increases the chance of bond lift or heal crack. In this study, the devices are actively heated without heat sink through controlled current injection and cooled down by forced air cooling through fans. By this way it is possible to increase the junction temperatures up to very high degrees without applying elevated currents. A constant drain current –half of the rated current– is used for all devices.

During the aging tests, having accurate junction temperature information is essential. Various methods are proposed to obtain junction temperature like thermocouple-based solutions, contactless IR setups and estimation through temperature-dependent electric parameters (TSEP). Each of these methods has particular advantages and disadvantages. Using a TSEP is the most popular method for discrete devices since it is non-invasive and do not require de-capsulation. On-state resistance, gate threshold voltage and reverse body diode voltage are the most commonly used TSEP parameters. Recent studies shows that these parameters may change due to charge trapping effects in SiC devices [13], [15] and hence they need to be recalibrated periodically along through the device lifetime. In this study, a simpler solution is adopted by controlling the temperature swing amplitudes with thermocouples attached to the metal tab of each switch. In order to decrease the difference between the measured case temperature and the junction temperature, an additional voltage limit defined for the power sources which normally supply constant drain current to the switches. When the voltage of a switch rises up to its defined limit with the increasing temperature, the drain current and, therefore, the power loss is decreased. Furthermore, the temperature readings calibrated with IR camera measurements for increasing the accuracy of the temperature measurements. The calibration values are updated at certain cycles to eliminate possible errors due to variation of thermal impedances through aging.

III. EXPERIMANTAL RESULTS

The thermal aging tests are performed on the custom-designed test setup which is shown in Fig. 1(a), to power cycle 1.2kV/11A discrete SiC MOSFETs with a junction temperature

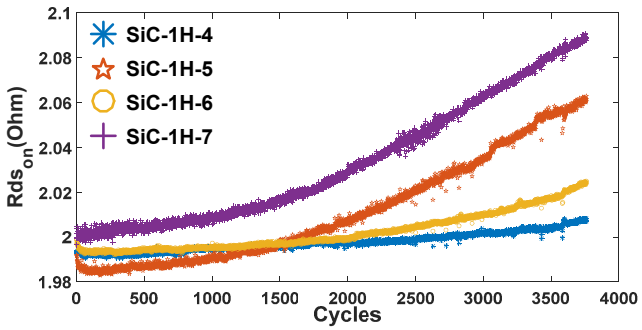

Fig. 2. Online $R_{ds,on}$ measurements versus power cycles.

swing from 30°C to 200°C. The switches are actively heated up to the defined maximum limit with constant current of 4.5A and then cooled with fans till they reach to the minimum temperature limit. The test-bed can test 7 switches at the same time with independent temperature limits and each complete cycle takes around three minutes (60 sec heating and 120 sec cooling). After each cycle, drain to source voltage, case temperature and drain current data of each switch are stored by data acquisition system and utilized for online on-state resistance ($R_{ds,on}$) measurements. The tests are performed on multiple devices and the results from some switches are presented here which represent overall behavior of all DUTs.

The results of online $R_{ds,on}$ measurements are given in Fig. 2. As shown here, on-state resistance of all samples increases gradually throughout the aging cycles. Although the identical thermal swing is applied on all devices, R_{dson} variation characteristics are similar yet the levels are different. This is partially due to manufacturing imperfections. C-SAM pictures of two brand new devices is given in Fig. 3. The topside C-SAM pictures (Fig. 3(a)) shows no anomaly for the switch 1G-2 although it exhibits some delamination of the plastic encapsulant to the heatsink (shown with red arrow) for the switch 1I-5. Fig. 3(b) shows some voids in the die attach interface (white/gray spots) which is different for two given brand new samples.

At every 200 thermal cycles, the devices are removed from the setup and then plugged into the curve tracer (Fig. 1(b)) for parametric analyses. Some of the electrical parameters under the above-mentioned aging conditions are given in Fig. 4. The breakdown voltage is measured with compliance of 1mA, as shown in Fig. 4(a). Throughout the aging cycles, the changes in breakdown voltage do not exhibit a consistent trend. For all switches, the threshold voltage and body diode forward voltage (Fig. 4(b,c)) show very similar increasing trend. Among others, the switch 1G-1 shows very distinct feature and reaches to much higher values than others although it has lower the initial values. The solder degradation is not expected to have an effect on the threshold voltage, as the thermal impedance degradation at the joints does not have any physical interference with SiC chip. One of the anticipated reasons for the threshold voltage change is the charge trapping in the SiC/SiO_2 interface which becomes more severe in high temperature conditions [15]. Especially the distinctive variation of the threshold voltage for switch 1G-1 can be explained with the growing delamination

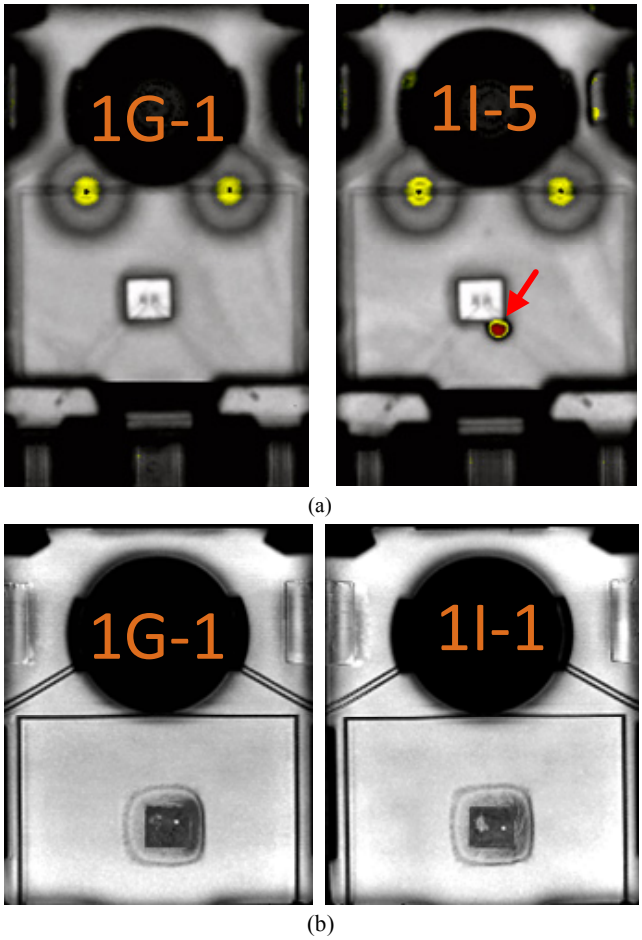

Fig. 3. C-SAM pictures of brand new devices; (a) combined image of the mold compound to heatsink and mold compound to leads interface form topside (b) focused to the die attach interface from back side.

which leads thermal impedance to increase by aging. Due to this ongoing process, temperature level of the chip might get too high after 2000 cycles. The I-V curves of output characteristic (Fig. 4(d)) and on-state resistance (Fig. 4(e)) also supports this assumption. The overall voltage drop and on-state resistance curves start to alter abruptly after 2000 cycles. In Fig. 4(f), parasitic capacitance measurements have been plotted at each aging cycles. The curves suggest very small variation for low voltage values.The switch 1G-1 were inspected using the C-SAM and T-SAM for internal defects such as voids, cracks and delaminations, and overall package integrity through power cycling tests. C-SAM and T-SAM are an effective techniques for non-destructively evaluating the samples for the presence of internal defects.

The first inspection is conducted as a brand new unit before exposure to power cycling tests then the second one assumedly at the middle of the cycling tests -which carried out at 2000 cycles- and last one at the end of 3800 power cycles. The acoustic micrograph pictures are shown in Fig. 5 which reveals the extent and location of defects through aging. The pictures as brand new devices, at the middle and at the end of the cycling tests are indicated as pre-stress, mid-stress and post-stress, respectively.

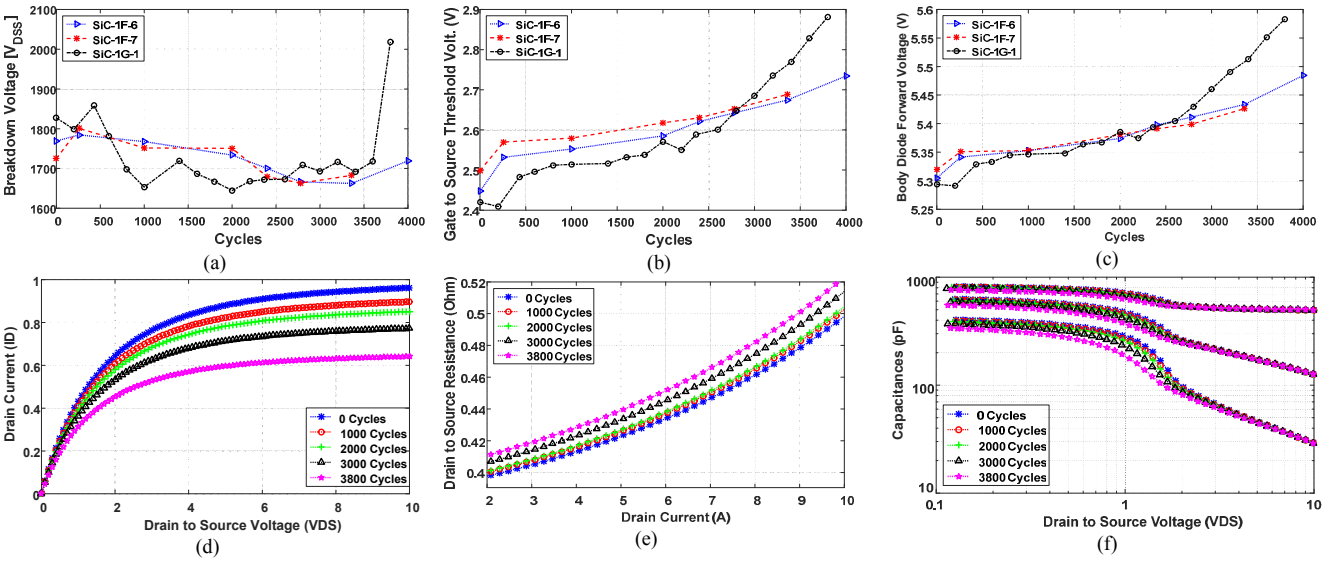

Fig. 4. Electrical parameter variations with respect to aging cycles; (a) Breakdown voltage, (b) Threshold voltage , (c) Body Diode Forward Voltage, (d) Output characteristics , (e) On-state resistance, (f) Parasitic capacitances.

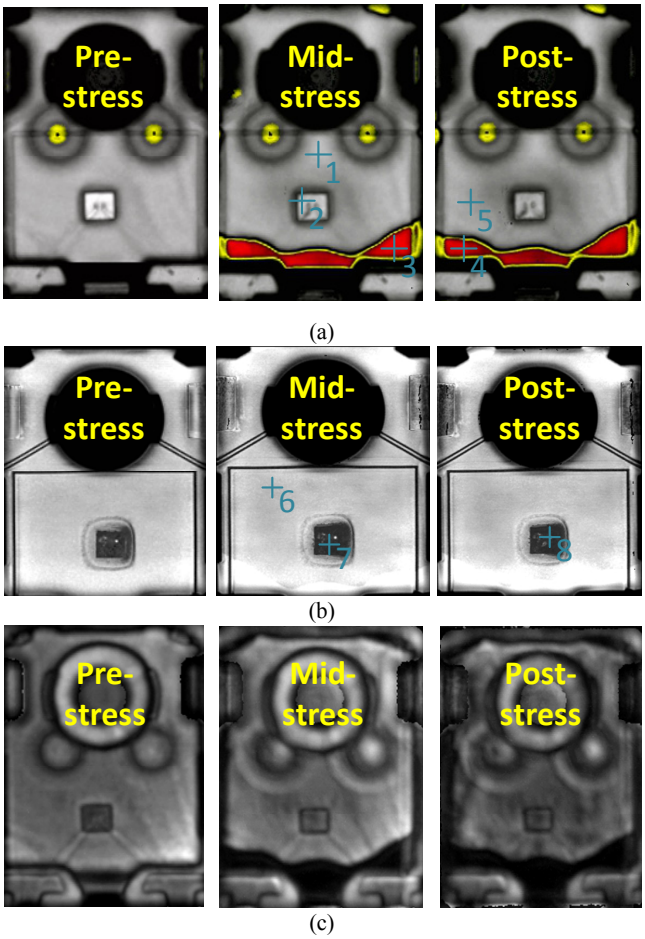

Fig. 5. SAM images of the switch 1G-1 through power cycling (a) combined image of the mold compound to heat sink and mold compound to leads interface form topside, (b) C-SAM image focused to the die attach interface from back side, (c) T-SAM image of the switch.

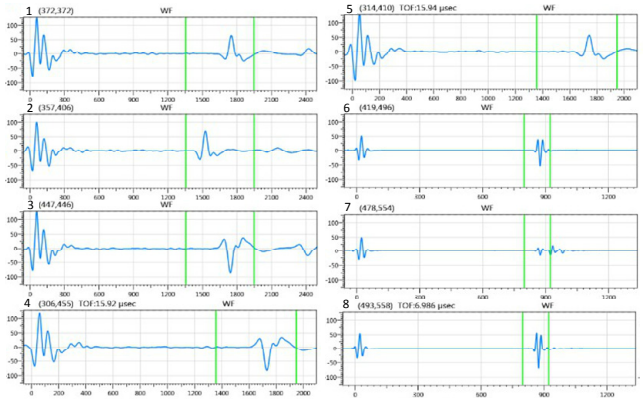

Fig. 6. Example waveforms corresponding to the blue arrows in Fig.5.

The images were generated by focusing the ultrasound through the top (encapsulated) and back (head sink) sides of the components. The topside images are given in Fig. 5(a) and display the encapsulant to die surface, heat sink and lead frame interfaces. The leads are at a different height within the parts than the die/heat sink level, so the images were generated in two scans at two different focus levels, but are displayed in a single image. The color scale displays areas of good adhesion in gray/white and delaminations appears as red/yellow. The backside images are given in Fig. 5(b) and were focused through the heat sink to the die attach level. In these pictures, dark gray indicates good adhesion and light gray/white indicates voiding. The T-SAM images are given in Fig. 5(c) and display the condition of the entire thickness of the parts. It was generated with the top (encapsulant) side up. Light gray indicates good material continuity while black areas indicate a separation at some level within the device.

The pre-stress condition of the switch does not show any significant defect. On the other hand, mid-stress condition images reveal an evident delamination at the mold compound to heat sink interface as red spots in the topside C-SAM and as dark spots in T-SAM. The die surface, die attach and lead

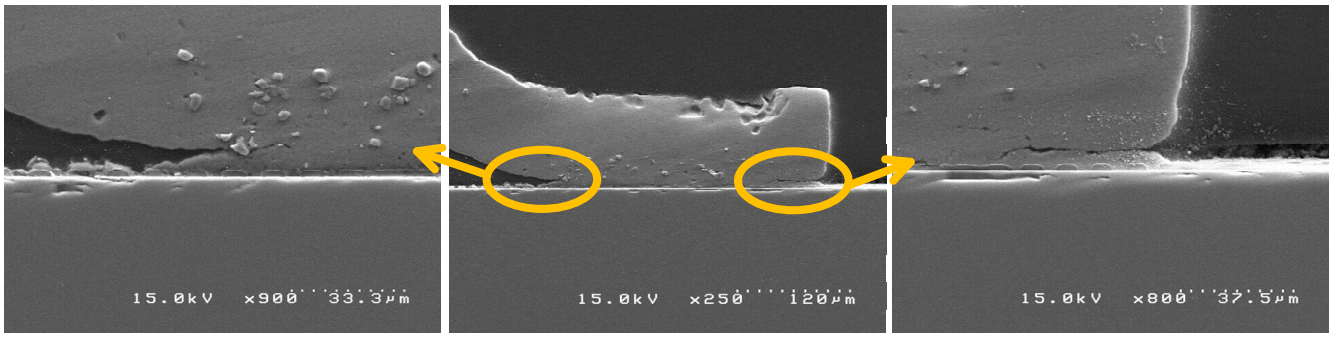

Fig. 7. Cross-sectioned bond wire image.

frame appears to be well bonded. The delaminations on the mold compound to heat sink interface have increased slightly from the mid-stress condition to the post-stress condition. This comparison shows an evidence of thermal stress related degradation. Moreover it also reveals that the main increase in the area of delamination occurred between the pre- and mid-stress conditions.

Example waveforms were captured for a few locations and given in Fig. 6 with the corresponding number of each location. The green bars in the waveforms indicate the gate corresponding to the level of focus. Negative reflections in the graphs indicate delamination on the heat sink while the positive reflections indicate a good adhesion.

The device also cross-sectioned and bond-wire attach has been analyzed as shown in Fig 7. Although a small crack is forming up at the tail of bond wire attach, there is no significant damage on the bond wire. The results show no defect at bond wire and die attach while a huge delamination is detected at the mold compound to heat sink interface. These findings verify the assumption of increased thermal impedance through aging for the device 1G-1.

IV. CONCLUSION

In this paper, a comprehensive reliability and aging evaluation of SiC MOSFETs for high temperature applications is presented. The power switches are exposed to high temperature power cycling, and on-state resistance are measured after each cycle. The other electrical parameters are captured using an automated curve tracer at certain intervals and variations of electrical parameters with respect to aging cycles are presented. It has been shown that on-state resistance, body diode voltage drop and gate threshold voltage are the only electrical parameters that increases consistently with aging and can be used as failure precursors to estimate the remaining useful lifetime of the power devices. The other parameters either do not consistently change or exhibit sudden change before failure, which can be used for instantaneous failure detection. The scanning acoustic microscopy (SAM) and cross-sectioning results are also presented and the root cause of aging is found to be thermal stress related wear out.

ACKNOWLEDGMENT

This work was supported by NSF Grant 1454311. Authors would like to thank Priority Labs for their support regarding C-SAM, T-SAM and X-ray imaging.

REFERENCES

[1] J. Millan, P. Godignon, X. Perpina, A. Perez-Tomas, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[2] J. Rabkowski, D. Peftitsis, and H. P. Nee, "Silicon carbide power transistors: A new era in power electronics is initiated," *IEEE Ind. Electron. Mag.*, vol. 6, no. 2, pp. 17–26, Jun. 2012.

[3] P. G. Neudeck, R. S. Okojie, and L. Y. Chen, "High-temperature electronics - A role for wide bandgap semiconductors?," *Proc. IEEE*, vol. 90, no. 6, pp. 1065–1076, Jun. 2002.

[4] M. Ostling, R. Ghandi, and C.-M. Zetterling, "SiC power devices - Present status, applications and future perspective," in *2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs*, 2011, pp. 10–15.

[5] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic mechanisms of threshold-voltage instability and implications for reliability testing of SiC MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 316–323, Feb. 2015.

[6] J. Schuderer, U. Vemulapati, and F. Traub, "Packaging SiC power semiconductors - Challenges, technologies and strategies," in *2nd IEEE Workshop on Wide Bandgap Power Devices and Applications, WiPDA 2014*, 2014, pp. 18–23.

[7] Z. Wang, X. Shi, L. M. Tolbert, F. Wang, Z. Liang, D. Costinett, and B. J. Blalock, "Temperature-Dependent Short-Circuit Capability of Silicon Carbide Power MOSFETs," *IEEE Trans. Power Electron.*, vol. 31, no. 2, pp. 1555–1566, Feb. 2016.

[8] C. Chen, D. Labrousse, S. Lefebvre, M. Petit, C. Buttay, and H. Morel, "Study of short-circuit robustness of SiC MOSFETs, analysis of the failure modes and comparison with BJTs," *Microelectron. Reliab.*, vol. 55, no. 9–10, pp. 1708–1713, 2015.

[9] G. Kampitsis, S. Papathanassiou, and S. Manias, "Comparative evaluation of the short-circuit withstand capability of 1.2kV silicon carbide (SiC) power transistors in real life applications," *Microelectron. Reliab.*, vol. 55, no. 12, pp. 2640–2646, 2015.

[10] J. A. Schrock, B. N. Pushpakaran, A. V. Bilbao, W. B. Ray, E. A. Hirsch, M. D. Kelley, S. L. Holt, and S. B. Bayne, "Failure analysis of 1200-V/150 - A SiC MOSFET under repetitive pulsed overcurrent conditions," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1816–1821, Mar. 2016.

[11] W. Zhou, X. Zhong, and K. Sheng, "High Temperature Stability and the Performance Degradation of SiC MOSFETs," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2329–2337, May 2014.

[12] Z. Chen, Y. Yao, M. Danilovic, and D. Boroyevich, "Performance evaluation of SiC power MOSFETs for high-temperature applications," in *2012 15th International Power Electronics and Motion Control Conference (EPE/PEMC)*, 2012, p. DS1a.8-1-DS1a.8-9.

[13] Z. Sarkany, Weikun He, and M. Rencz, "Temperature change induced degradation of SiC MOSFET devices," in *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2016, pp. 1572–1579.

[14] N. Baker, S. Munk-Nielsen, and S. Beczkowski, "Test setup for long term reliability investigation of Silicon Carbide MOSFETs," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9.

[15] A. Ibrahim, J. P. Ousten, R. Lallemand, and Z. Khatir, "Power Cycling Tests in High Temperature Conditions of SiC-MOSFET Power Modules and Ageing Assessment," in *CIPS 2016; 9th International Conference on Integrated Power Electronics Systems*, 2016, pp. 1–6.

[16] S. Dusmez, M. Heydarzadeh, M. Nourani, and B. Akin, "Remaining Useful Lifetime Estimation for Power MOSFETs Under Thermal Stress With RANSAC Outlier Removal," *IEEE Trans. Ind. Informatics*, vol. 13, no. 3, pp. 1–1, Jun. 2017.

[17] S. Dusmez, M. Heydarzadeh, M. Nourani, and B. Akin, "A robust remaining useful lifetime estimation method for discrete power MOSFETs," in *ECCE 2016 - IEEE Energy Conversion Congress and Exposition, Proceedings*, 2017, pp. 1–6.

[18] S. Dusmez, H. Duran, and B. Akin, "Remaining Useful Lifetime Estimation for Thermally Stressed Power MOSFETs Based on on-State Resistance Variation," *IEEE Trans. Ind. Appl.*, vol. 52, no. 3, pp. 2554–2563, May 2016.

[19] J. R. Celaya, A. Saxena, P. Wysocki, S. Saha, and K. Goebel, "Towards Prognostics of Power MOSFETs: Accelerated Aging and Precursors of Failure," 2010.

[20] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," in *2015 IEEE International Electric Machines & Drives Conference (IEMDC)*, 2015, pp. 1352–1358.

[21] S. Dusmez and B. Akin, "Comprehensive parametric analyses of thermally aged power MOSFETs for failure precursor identification and lifetime estimation based on gate threshold voltage," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2016, vol. 2016–May, pp. 2108–2113.