99.3% Efficiency of Boost-up Converter for Totem-pole Bridgeless PFC Using GaN Gate Injection Transistors

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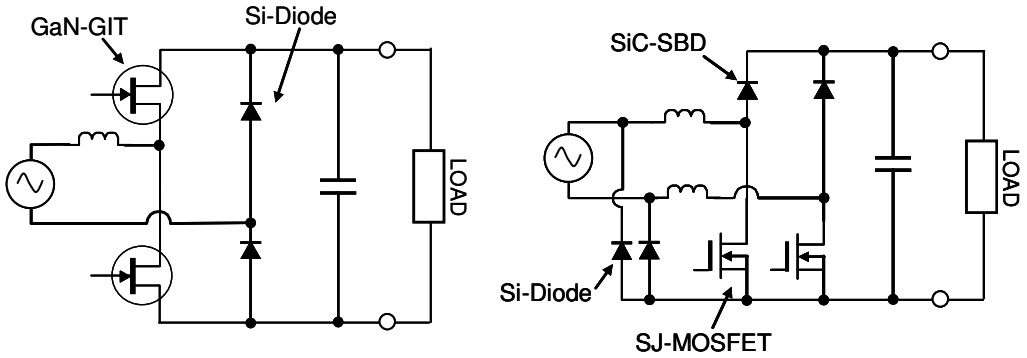
Abstract

In this paper, we present highly efficient operation of a boost-up converter for bridgeless power factor correction (PFC) using normally-off GaN Gate Injection Transistors (GITs) in a novel totem-pole output circuitry. The normally-off device by a single chip enables its flip-chip assembly which effectively reduces the stray loop inductance in the circuit. The fabricated boost-up converter exhibits the peak efficiency of 99.3% and the efficiency of over 99% is maintained in the wide range of the output power from 400W to 2.3kW. The maximum output power of 3kW is the highest ever reported for the efficient synchronous boost-up converter using 600V-class GaN devices.

1. Introduction

Power factor correction (PFC) circuits are mandatorily required for power supplies to enable better management of the total power from the grid. A typical PFC circuit is consisted of the rectifying stage using a diode bridge and a boosting stage using a power transistor and a diode. Since the operating loss in the diode bridges becomes significant after introduction of highly efficient power switching transistors such as super-junction MOS (SJ-MOS) transistors for the boosting stage, bridgeless circuit topologies have emerged as innovative alternatives to further improve the total efficiencies.

In this paper, we present highly efficient operation of a boost-up converter for a bridgeless PFC with a novel totem-pole output configuration using normally-off Gallium Nitride (GaN) transistors. Figure 1 shows a circuit diagram for the totem-pole PFC using the GaN transistors, where conventional one for the bridgeless PFC using Si SJ-MOS transistors is also shown.



(a) Proposed Totem-pole PFC using GaN-GITs

(b) Conventional dual-boost PFC

Fig.1 Representative bridgeless PFC topologies

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Taking advantages of small recovery loss of the reverse diode inherently served by the lateral GaN transistor, the totem-pole PFC can be consisted of two transistors and two diodes. In addition to the small number of the semiconductor components employed, the two diodes do not require good recovery characteristics. Thus, the presented PFC can be more cost effective than the conventional one. The conventional dual-boost PFC is proposed to extract the full potential of SJ-MOS with poor recovery characteristics of the body diode, where two SiC Schottky barrier diodes (SBDs) need to be introduced which would lead to large system size and high cost. The totem-pole PFC configuration is suitable for the application of GaN transistors.

2. GaN Gate Injection Transistor and its gate driving technique

Fig. 2 shows a schematic cross section of normally-off GaN transistor named as Gate Injection Transistor (GIT) [1]. P-type AlGaN gate is placed over an AlGaN/GaN hetero-junction depletes the channel under the gate as well as holes are injected from the gate resulting in increased drain current by the conductivity modulation. Fig. 3 shows Ids-Vds characteristics of the fabricated GIT with the threshold voltage of 1.2V. The on-state resistance and the off-state breakdown voltage are 66mΩ and 650V, respectively. The improved processing and device structure enable the reliable operation free from the current collapse in which the on-state resistances are significantly increased after the off-state stresses. Note that the GITs are free from the collapse up to 650V. In order to extract the full potential of the fast switching of GaN, we introduce a new gate driving circuit for the GIT. The proposed driving circuit has a speed-up capacitor with the gate resistances, while the conventional one is consisted of just a gate resistance as shown in Fig.4. The new driving circuits apparently improve the switching speed as shown in Fig.5.

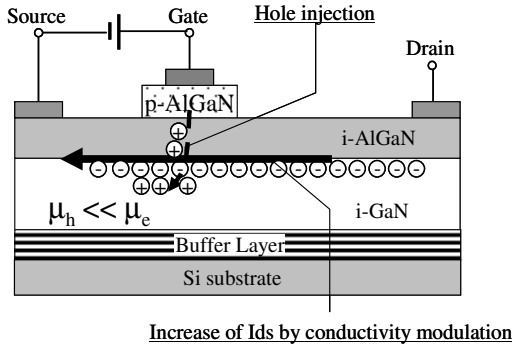


Fig.2 Schematic cross section of AlGaN/ GaN Gate Injection Transistor and its operating principle

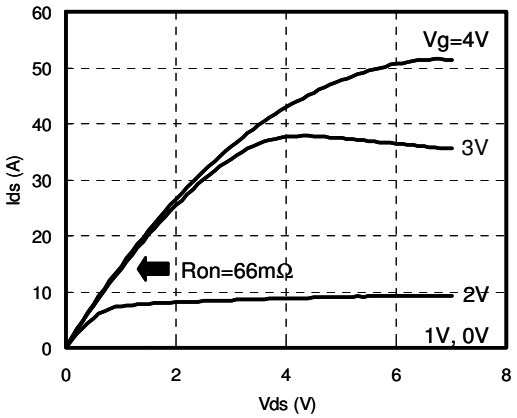
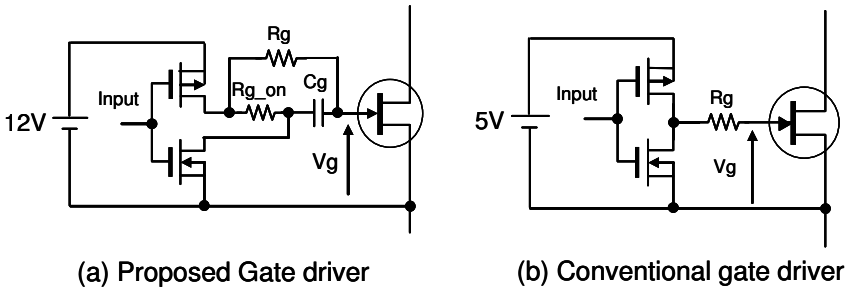


Fig.3 The Ids-Vds characteristics of the GaN-GIT



(a) Proposed Gate driver (b) Conventional gate driver

Fig.4 The circuit diagram of gate drivers

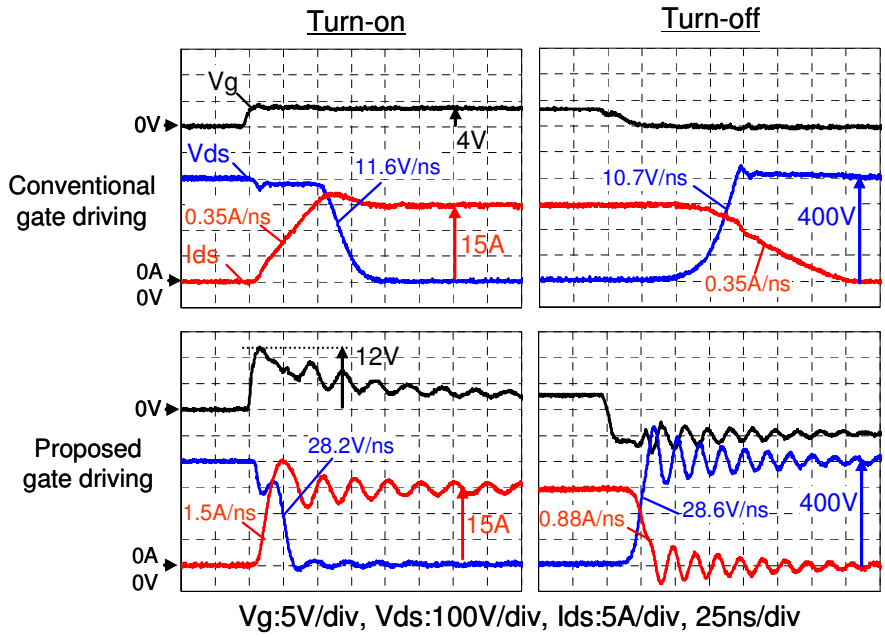


Fig.5 Inductive-load switching characteristics of GaN-GIT with TO-220 package

3. Flip-chip bonding technique

Additional feature presented in the converter is the reduction of the parasitic inductances by the flip-chip bonding of the GaN GITs. The inductance needs to be reduced, since the loop parasitic inductance(L_{LOOP}) on the power line of the boost-up converter affects the switching speed causing the voltage spike between the drain and the source as shown in Fig. 6. Fig. 7 shows the schematic cross section of fabricated half-bridge with GaN-GITs mounted by flip-chip technique. Here the L_{Loop} is reduced down to 2nH as a simulated value, while conventional TO-220 packaged GaN with longer lead exhibits 13nH to 24 nH as the L_{Loop}. The flip chip configuration is only possible by the normally-off GIT by a single chip, while the reported cascaded configuration cannot be assembled in a flip-chip manner. Fig.8 shows the switching waveforms of Vg and Vds of low-side GIT with the flip-chip configuration. The presented flip-chip configuration shows very high turn-on switching speed with the slew rate of 170V/ns which is 1.7 times larger than that by the state-of-the-art SJ-MOS. In addition, no significant voltage spike is observed. Fig. 9 shows the measured recovery characteristics of the GIT operated as a reverse diode, where the recovery loss is small.

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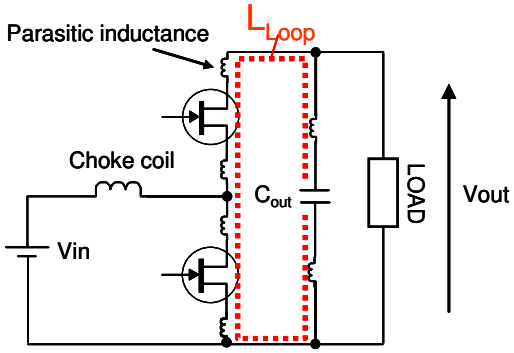

Fig.6 Synchronous boost-up converter with parasitic inductances

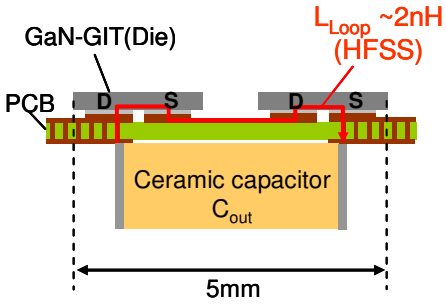

Fig.7 Schematic cross section of fabricated half-bridge circuit with GaN-GITs mounted by flip-chip technique

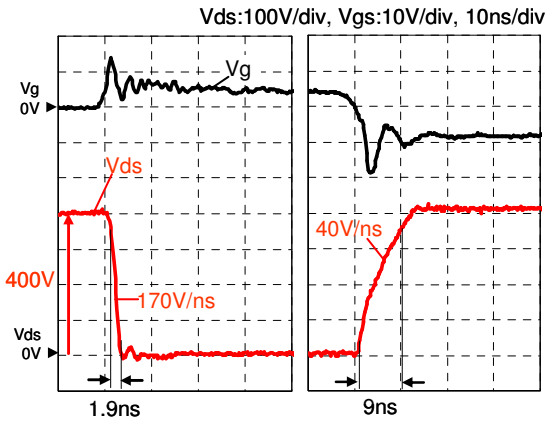

Fig.8 Waveforms of Vds and Vg of low-side GIT mounted by Flip-chip bonding

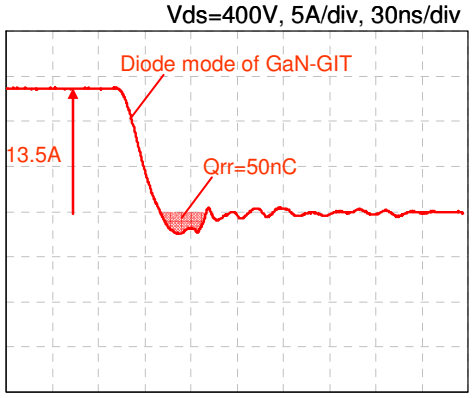

Fig.9 Recovery characteristics of GaN-GIT

4. Perfomances of GaN-based boost-up converter

Fig. 10 shows the photograph of the fabricated GaN-based converter using the flip-chip assembly for the GaN-GITs.

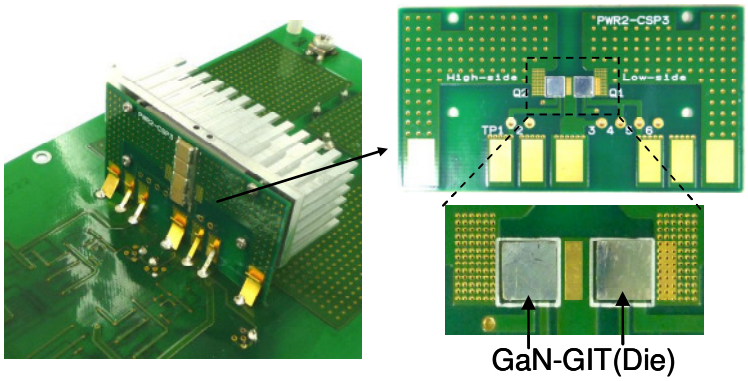

Fig.10 Photograph of the fabricated boost-up converter with GaN-GIT mounted by flip-chip bonding

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Fig.11 summarizes the operating efficiency of the fabricated GaN-based boost-up converter for various output power, in which those by conventional one using SJ-MOSFETs and SiC-SBDs is also shown. The efficiency at the carrier frequency of 50kHz is over 99% from the output power 400W to 2.3kW. The employed synchronous rectifying operation of GaN-GIT also helps the high efficiencies. The peak efficiency of 99.3% at 1kW is the highest ever reported in the single-phase 3kW-outputting boost-up converter to the best of our knowledge.

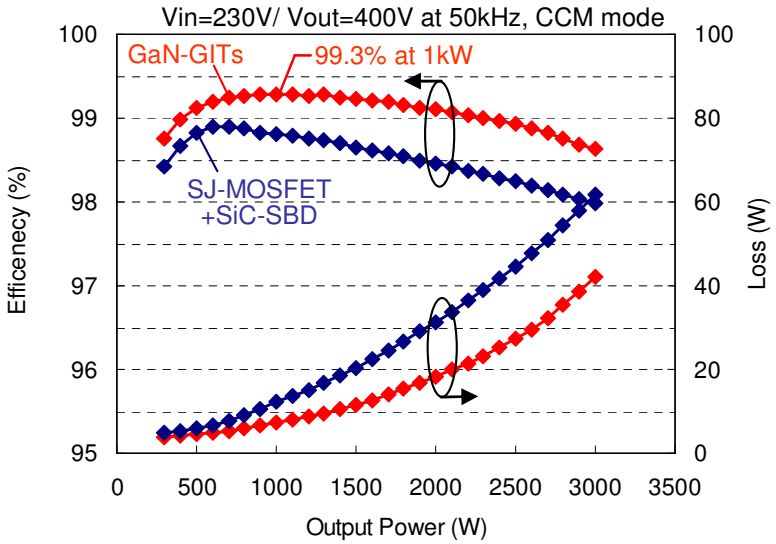

Fig.11 Power conversion efficiency of GaN-based boost-up converter for various output power as compared with those by conventional one using SJ-MOSFET and SiC-SBD.

5. Conclusion

In conclusion, we demonstrate very high operating efficiency of 99.3% of boost-up converter for a novel totem-pole bridgeless PFC configuration using GaN normally-off transistors. The maximum output power of 3kW well exceeds the reported power by the boost converter using the cascaded GaN devices[2]. The presented GaN-based converter is very promising for the highly efficient power supply expected in the future.

Acknowledgement

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Reference

[1] Y. Uemoto et al., IEEE Trans. Electron Device, vol.54 p.3393, 2007

[2] U.Mishra et al., PCIM Europe 2013, Conference Digest, p724-729, Nuremberg, May 14-16, 2013