Reliability Characterization of BEOL Vertical Natural Capacitor Using Copper and Low-k SiCOH Dielectric for 65nm RF and Mixed-Signal Applications

F. Chen[1], F. Ungar[3], A.H. Fischer[3], J. Gill[1], A. Chinthakindi[2], T. Goebel[3], M. Shinosky[1], D. Coolbaugh[2], V. Ramachandran[2], Y. K. Siew[4]; E. Kaltalioglu[3]; S. O. Kim[3]; and K. Park[5]
[1]IBM Microelectronics, Essex Junction, VT 05452; [2]IBM Microelectronics, East Fishkill, NY 12533;
[3]Infineon Technologies AG, Munich, Germany; [4]Chartered Semiconductor Manufacturing Ltd, Singapore
[5] Samsung Electronics Co., Ltd, Kyunggi-Do, Korea
Phone: 802-769-7917; fax: 802-769-4287; e-mail: chenfe@us.ibm.com

ABSTRACT

Integration of low-cost and high performance passive capacitors into existing Silicon CMOS technologies is essential for analog and radio frequency (RF) IC applications. Recently, BEOL vertical natural capacitors (VNCAP) with stacked via-comb structures have emerged as an attractive option due to their low-cost, high density, and highly symmetric configurations. In order to accurately predict low-k VNCAP reliability, in this study, both the time-dependent dielectric breakdown (TDDB) and capacitance stability (C-stability) of Cu/low-k SiCOH VNCAPs at 65nm technology node were thoroughly investigated. The TDDB performance of Cu/SiCOH VNCAP was found to be sensitive to device layouts and process. Capacitance stability was found to be sensitive to the presence of moisture in SiCOH low-*k* film during process. With the optimal device design and process, SiCOH VNCAP was found to exhibit robust TDDB performance, as well as absence of capacitance instability during high temperature stress (HTS). [*Keywords:* time-dependent dielectric breakdown, capacitance stability, moisture impact, Cu interconnect, reliability, low-*k*, ILD, process integration]

INTRODUCTION

Integration of low-cost and high performance passive capacitors into existing Silicon CMOS technologies is essential for analog and radio frequency IC applications. Recently, BEOL vertical natural capacitors with stacked via-comb structures as shown in Figure 1a have emerged as an attractive option for advanced CMOS and BiCMOS RF technologies [1-2]. The motivation for the shift to BEOL vertical capacitor from planar capacitors is due to its low-cost, high density, and highly symmetric configuration. In today's CMOS technology, multi-layer (> 8 metal layers) interconnect structures makes high density VNCAP easily achievable without the extra processing and masks required by conventional planar capacitors such as metal-insulator metal (MIM) capacitors. Based on a symmetric comb-comb with via configuration, the VNCAP is also a truly bidirectional device. Furthermore, the enhancement of quality-factor (Q-factor) of VNCAP with special layout technology has also been reported [3]. However, with the wide spread application of low-*k* dielectrics at the 90nm technology node and beyond, the long-term reliability of VNCAP is rapidly becoming one of the most critical challenges for qualification of such capacitors. Among the VNCAP reliability issues, both VNCAP TDDB and VNCAP C-stability under temperature (bias) stress are of great concerns. TDDB is commonly considered as an important reliability issue because low-*k* materials generally have weaker intrinsic breakdown strength than traditional SiO_2 dielectrics. This problem is further exacerbated by the aggressive shrinking of the interconnect pitch size due to continuous technology scaling and the fact that large area VNCAPs may easily contain tens of millions of vias and several meters of metal lines. For RF analog circuits, the matching properties between individual capacitor elements and the stability of these elements to maintain high precision under different operating condition are critical for the assurance of high circuit performance. Shifts in capacitance after long-term operation can lead to distortion in analog signals [4-5]. Therefore, the stability of capacitance during device operation is another important reliability issue that needs to be evaluated.

In this study, both TDDB wear-out reliability and the stability of capacitance of VNCAP capacitors at 65nm technology node under high temperature and high bias condition were investigated. The TDDB performance of Cu/SiCOH VNCAP was found to be sensitive to device layouts and process. C-stability was found to be sensitive to the presence of moisture in SiCOH low-*k* film. With the optimal device design and process, the SiCOH VNCAP was found to exhibit robust TDDB performance and stable capacitance during bias-temperature stressing.

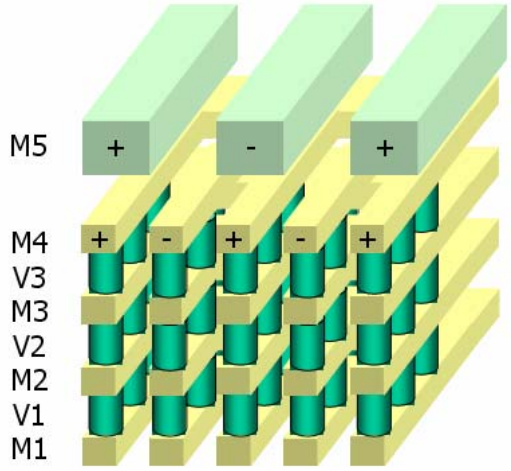

Fig. 1: 3D scheme of VNCAP device containing four thin wire levels (M1-M4) which are interconnected by vias and one fat wire level (M5) without comb-via connection.

EXPERIMENTAL

The VNCAP capacitors investigated in this study were fabricated using a 65nm BEOL process with dual damascene Cu interconnects fabricated in a low-*k* SiCOH dielectric. The capacitors were formed vertically in the BEOL stack using a comb-comb configuration with adjacent vertical wiring linked by multiple vias as show in Figure 1. Via first dual damascene integration scheme was used to fabricate 1x levels in low-k (k=3.0) and 2x levels in FTEOS/TEOS (k=3.5-3.9) dielectric medium. 193nm lithography tools were used for via and lines in 1X levels while DUV, 248nm lithography tools were used for 2X levels. Low down force chemical mechanical planarization (CMP) process was used to planarize the copper over burden for both thin and fat wire levels. VNCAP test structures of this design were fabricated using up to six levels of wiring and used both thin (1X) and fat (2X) wire levels. Capacitors with two finger-to-finger spacing values, 0.1µm and 0.14µm respectively, were evaluated for reliability. In addition to the spacing variation, 2 different via

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configurations were also evaluated. The layout size of the tested VNCAP device is about 150x50 μm^2.

Constant voltage-temperature stresses were performed on wafer level for TDDB evaluation with at least three different biases and three different temperatures for modeling. The method of multiple time-steps to apply low sensing voltages to monitor stress-induced leakage current (SILC) was used during constant voltage stress. For TDDB, the hard breakdown condition was typically defined as a sudden leakage current increase at stress level, and was further confirmed at a sensing level of at least 100X SILC increase. Finally, wafer level, constant temperature aging stresses were performed to study C-stability behavior. The stress temperature for these C-drift studies was kept at 125C and the total stress time was 200hr.

RESULTS AND DISCUSSIONS

A) TDDB PERFORMANCE AND FEM MODELING

The TDDB performance of Cu/SiCOH VNCAP was found to be sensitive to VNCAP device layouts. Figures 2 and 3 illustrate the Weibull distributions of two VNCAP capacitors obtained under the same stress conditions but with two different via configurations labeled as Via-1 and Via-2, respectively. The capacitors with Via-1 configuration exhibited bimodal TDDB distributions showing extrinsic defect tails under all stress biases while the capacitors with Via-2 showed single mode distributions. Coincidently, the process yield degradation of such Via-1 configuration VNCAP was also observed. Therefore, a ground rule for VNCAP capacitors was established to prohibit such Via-1 configuration layout to safeguard reliability as well as yield. By studying three different finger-to-finger spacing, it was determined that SiCOH VNCAP TDDB is driven by field rather than voltage as shown in Fig. 4. The line-to-line spacing values used for field calculation here were nominal values. The field acceleration extracted from exponential law was found to be less variable (<10%) whereas the voltage acceleration factor decreased significantly (~2X) with increasing space. The slight variation of field acceleration factor possibly is due to some CD variations. The TDDB reliability (failure rate at the same usage conditions) of wide spacing VNCAP is significantly better than narrow spacing VNCAP due to reduced field with wide spacing VNCAP and much better Weibull distribution slope of wide spacing VNCAP than that of narrow spacing VNCAP. However, the capacitor's performance such as capacitance and density is balanced with TDDB reliability for better chip operation and narrow spacing VNCAP is of great interest if its reliability could be qualified.

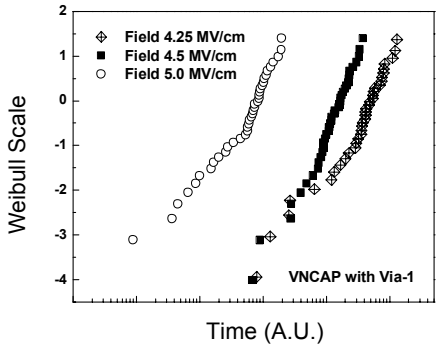


Fig. 2: Weibull plot of VNCAP with Via-1 configuration under three electric fields. Bimodality consisting of intrinsic and extrinsic portions is visible.

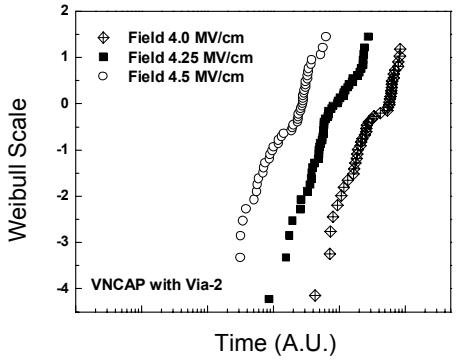


Fig. 3: Weibull plot of VNCAP with Via-2 configuration under three different electric fields with overall single-mode distributions.

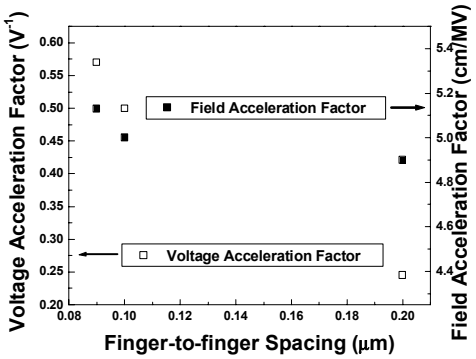


Fig. 4: Field and voltage acceleration factors for various VNCAP with different finger-to-finger spacing.

Post TDDB failure analysis revealed that most failures occurred at the last 1X thin wire level (M4 level in this case) as shown in Figure 5. No process induced abnormalities could be identified at this level comparing to other 1X levels. The obvious differences of M4 from the levels underneath (M1, M2, and M3) are that M4 is not connected by vias to the 2X level above because it is the last 1X level, and it is also coated with a 40% thicker capping layer. In order to investigate the root cause of the preferred dielectric breakdown at the M4 level, finite element modeling (FEM) simulation was performed to examine the electric field distribution inside multi-level VNCAP.

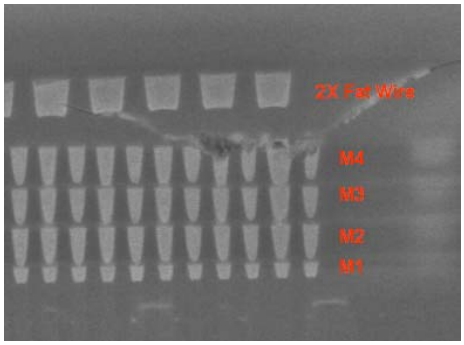


Fig. 5: Cross-section of VNCAP showing a typical dielectric breakdown event preferentially the M4 level

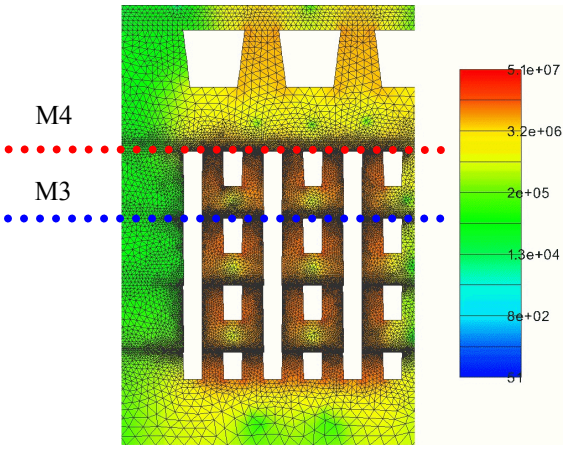


Fig. 6: FEM simulation of the electric field for a VNCAP with staggered via configuration. The field strengths for metal levels M3 and M4 were calculated along the dotted lines at the copper/cap and the low-k/cap interface, respectively.

The simulation grid used for FEM studies reflects metal and via geometries and configurations such as via or metal line taper and the top corner rounding of the copper trenches (Fig. 6), which were identified by physical construction analysis. All field strengths are simulated with respect to a line to line bias of 3.6V. Due to the multi-level configuration, the electric field distribution at each level depends on the surrounding via/metal environment and the actual cap layer thickness. The metal level with higher local electrical field may result faster Cu ion migration and therefore short TDDB. The first obvious effect is the pronounced field enhancement at the copper/low-k/cap layer triple junction point (Fig.7). The magnitude of such field enhancement point is primarily influenced by the corner rounding rather than the metal level. However, the distinct difference between M4 and the layers underneath is that lower metal levels are missing every other field enhancement point due to the presence of the linking vias on those levels, whereas at the same location in M4, a high local field exists. In this way, the density of triple points with high local E-field is two times higher in the top M4 metal level than that in the lower metal levels.

Beside the difference of field enhancement point density, two other systematic E-field distribution differences between M4 and M3 levels were also observed. Based on simulations in Fig.7, it can be seen that the local electric field in M4 is slightly reduced at the low-k/cap interface but enhanced by about 7% at the copper/cap interface inside of the copper line. The main reason of this observation is possibly due to the thicker cap layer on the top of M4. As illustrated in Fig.8, the local field enhancement inside copper line is strongly influenced by the cap layer thickness and it increases with increasing cap thickness. However, the field in the middle of the low-k (outside of copper line) is almost invariable, or even slightly decreases with increasing cap thickness.

Based on our experimental and simulation results, we hypothesis that both the higher density of peak field points and the higher local E-field inside copper line provide an explanation as to why M4 level was more vulnerable to breakdown than the other thin wire levels (M1, M2, and M3) with the same line width and space. The effect of high local E-field inside copper line on low-*k* TDDB could be explained by the field-assisted Cu diffusion theory [8]. Although the electric field at low-*k*/Cap interface is expected to play a major role during copper ion diffusion process, the number of injected copper ions (available copper ions participating in diffusion) is possibly controlled by the field inside copper line. Our experimental results together with the simulations suggest that the higher field at the copper/cap interface inside copper line could generate and push more Cu ions towards the triple points followed by their injection into the dielectric over the barrier. Such inside of line E-field maybe plays an important role during Cu/low-*k* TDDB as well.

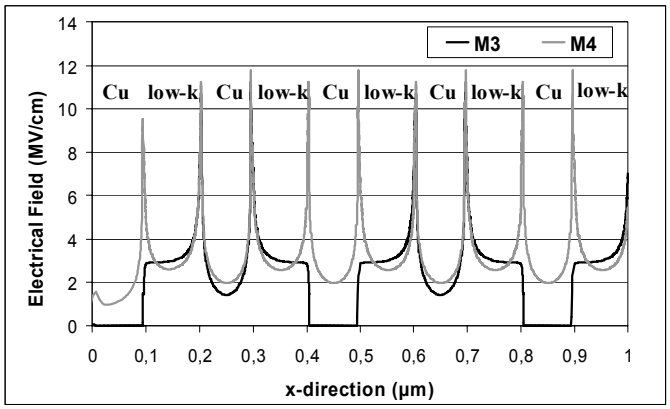
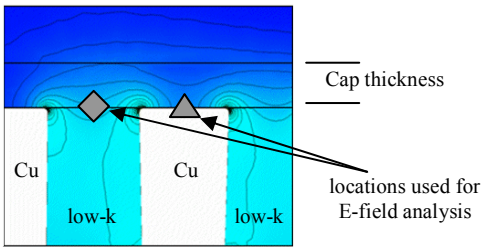


Fig. 7: FEM results of the E-field distribution in the VNCAP with staggered vias for metal level M3 and M4 (Calculation done along the dotted lines in Fig.6).



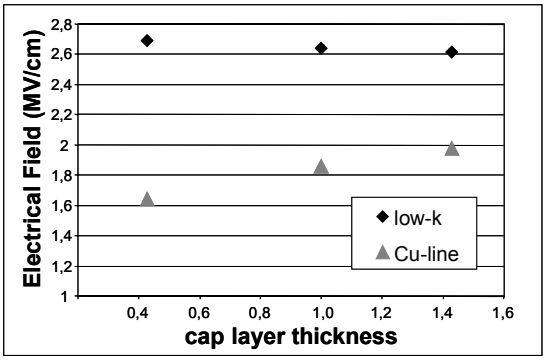


Fig. 8: FEM simulations of the E-field for metal lines with three different cap layer thicknesses. The field strengths are calculated at two locations of the cap interface: 1) at the middle of the copper line; 2) at the middle of the low-k interface between the two metal lines.

B) Moisture Impact And Capacitance Stability

Additionally, during the TDDB study of VNCAP, it was found that the presence of moisture significantly influenced the TDDB kinetics, as well as C-stability. In hardware exposed to moisture due to un-optimized process step, it was found that at high temperature,

the measured capacitance nonlinearly decreased with time over a relatively short period and eventually saturated at a fixed level (Figure 9). Such capacitance reduction was found to be primarily temperature dependent with little to no voltage dependence. In order to verify the role of moisture, several chips were intentionally prepared without any moisture barrier (seal ring). The samples were then exposed to ambient conditions for several days before being stressed at 125 °C. As shown in Figure 10, it was found that the samples expose to moisture showed similar capacitance drop down to -8% during the temperature aging, and that such capacitance drop could be partially recovered at room temperature after removing the heat. Therefore, we conclude that the capacitance drift during temperature aging is mostly due to moisture trapped inside SiCOH. It is known that low-k SiCOH surface layer could be damaged, and therefore absorb moisture during certain process steps [6]. Moisture uptake increases the leakage paths and film polarization, thus resulting in leakage current and film k-value increase (reflected in a capacitance increase). For fully integrated hardware, such trapped moisture will re-distribute within different layers by diffusion at high temperatures to reach a new equilibrium state, and therefore induce the observed temperature-dependent capacitance instability. An empirical formula was developed to model such capacitance drift during temperature aging as following:

$$\frac{\Delta C}{C_0} = A_0 Tanh\left[-\sqrt{\frac{t}{D}}\right], \qquad (1)$$

where C_0 is initial as-received capacitance, ΔC is the total capacitance change, A_0 is a constant representing the final saturation value when time (t) approaches infinity, and $D \sim D_0 \times \exp(-\Delta H/kT)$ is related to the moisture diffusivity. By fitting the experimental data with this empirical formula, values of D and A_0 could be simultaneously obtained. As shown in Figure 9, this empirical formula could fit measured data very well. If the fitted parameter D in equation 1 is in fact related to diffusivity, then an activation energy from the slope of a plot of Ln[D] vs. $1/kT$, as shown in Figure 11 may be extracted. The average D value was found for each of three stress temperatures (125, 150 and 175 °C) and ranged from 199 minutes to 4402 minutes. As shown in Figure 11, the fit to the data points is reasonable, and yields a value for the activation energy of 0.83 eV.

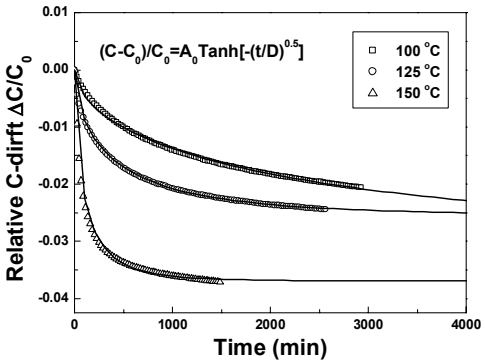


Fig. 9: Capacitance drifts typically obtained at different storage temperatures.

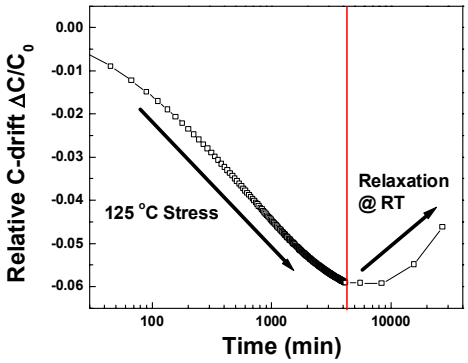


Fig. 10: Nonlinear C-drift at 125 °C and relaxation at room temperature.

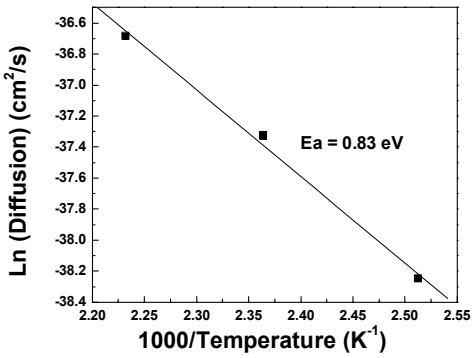


Fig. 11: Plot of LnD vs. 1/kT used to extract an activation energy for the assumed moisture diffusivity.

Moisture not only impacts the stability of VNCAP capacitance, but also influences VNCAP TDDB performance. The TDDB field acceleration factor from fitting the TDDB data to an E-model (Figure 12) and thermal acceleration factor in those "wet" samples were significantly smaller than in "dry" samples, suggesting that the failure kinetics for TDDB may be dramatically different between those two cases. Both sets of VNCAP with difference finger-to-finger spacing exhibited a similar moisture effect. These results are consistent with Lloyd's finding for ultra-low-*k* [7], in which he found that the presence of moisture significantly reduced the TDDB lifetime as well as increased leakage and capacitance. As SiCOH TDDB is attributed to Cu migration during stress from our extensive physical and electric evidence [8], we propose that trapped moisture could diffuse into Cu line, oxidize the Cu, and accelerate Cu diffusion during high temperature and high bias stress. It is well known that when a Cu surface is exposed to moisture, a surface layer containing cuprous oxide (Cu_2O) and cupric oxide (CuO) can be formed [9]. Such oxidation under field and temperature could lead to the ionization of Cu atoms, and ionized Cu could migrate into SiCOH along the SiCOH/Cap interface. A large amount of Cu ions could be generated with the help of moisture at the anode, allowing many Cu ions to inject into SiCOH and form Cu nano-particles and clusters at the interface. Such neutral Cu particles and clusters could further migrate along the interface following a diffusion-limited process with the driving force of concentration gradient. Therefore the actual field and temperature influences on TDDB would be dramatically reduced, and both the voltage acceleration and thermal

acceleration factors are significantly smaller in those "wet" samples than they in "dry" samples.

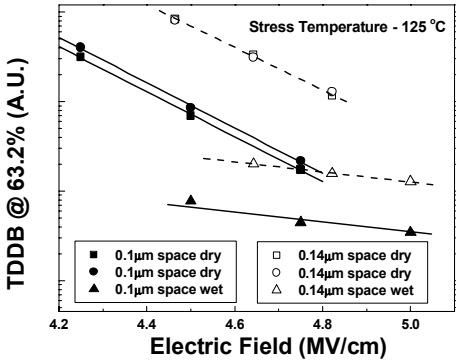


Fig. 12: Field acceleration plot for "dry" and "wet" SiCOH VNCAPs with different comb-comb spacing.

C) VNCAP TDDB AND C-STABILITY QUALIFICATION

A Weibull statistics model was used in the final VNCAP TDDB qualification to predict reliability lifetime of 65nm SiCOH VNCAP. Use of the Weibull distribution usually gives a more conservative projection than Lognormal. The most conservative E-field model was also used for field acceleration and the E-field acceleration factor was determined to be about 5.5 MV/cm at 125 °C, which is the device operation temperature. The temperature acceleration factor was evaluated based on the Arrhenius relation and the thermal activation energy was determined to be about 0.35 eV at nominal 4.5 MV/cm stress field as shown in Fig. 13. Those numbers were used in the final reliability lifetime projection. Furthermore, in order to scale failure probability from test structure to product-like VNCAP size, the Poisson area scaling transformation was used. Strictly speaking, a pure intrinsic fail of a perfect homogeneous material should be area independent and should occur at exactly the same time for all samples. In reality, the material has inhomogenities (even without any defects), which lead to a distribution of failure times. Therefore, such area scaling is required to have a better reliability prediction for real products.

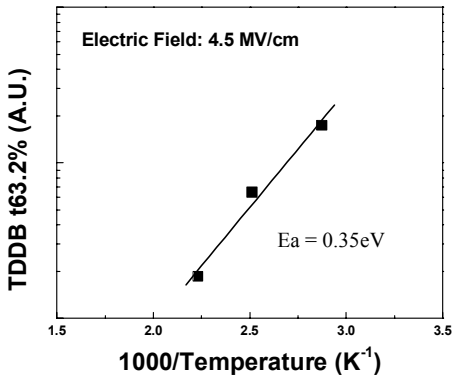


Fig. 13: TDDB @ 63.2% of Weibull scale versus temperature for thermal activation energy determination based on Arrhenius relation.

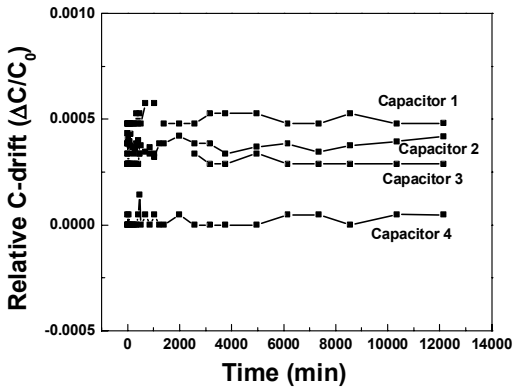


Fig. 14: No detectable C drift at 125C for wafers with optimal BEOL process.

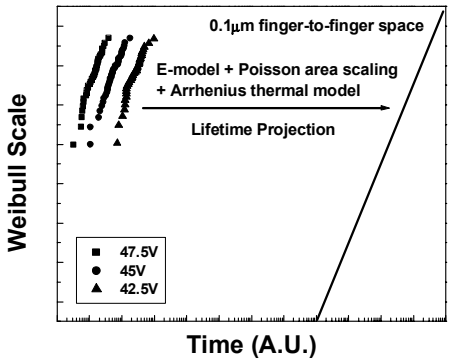


Fig. 15: Weibull reliability lifetime projection plot of SiCOH VNCAP at 65nm technology node.

Finally, with careful device layout design, process control, and process optimization, the capacitance instability of VNCAP could be successfully minimized as shown in Figure 14. The projected SiCOH TDDB lifetime based on conservative Weibull statistics and E-field acceleration model was far beyond the reliability target as shown in Figure 15. Both capacitance and TDDB results assured the successful adoption of this new kind of passive device into the state-of-art RF and mixed signal ICs at 65nm technology node for various high frequency applications.

CONCLUSIONS

In conclusion, both the TDDB and C-stability of Cu/low-k SiCOH VNCAPs at 65nm technology node were thoroughly investigated. The TDDB performance of Cu/SiCOH VNCAP was found to be sensitive to device layouts and process. Capacitance stability was found to be sensitive to the presence of moisture in SiCOH low-*k* film. With the optimal device design and process, SiCOH VNCAP was found to exhibit robust TDDB performance, and a stable capacitance during bias-temperature stress.

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