Reliability Analysis of a High-Efficiency SiC Three-Phase Inverter for Motor Drive Applications

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***Abstract*— Silicon Carbide as an emerging technology offers potential benefits compared to the currently used Silicon. One of these advantages is higher efficiency. If this is targeted, reducing the on-state losses is a possibility to achieve it. Parallel-connecting devices decrease the on-state resistance and therefore reducing the losses. Furthermore, increasing the amount of components introduces an undesired tradeoff between efficiency and reliability. A reliability analysis has been performed on a three-phase inverter for motor drive applications rated at 312 kVA. This analysis has shown that the gate voltage stress determines the reliability of the complete system. Nevertheless, decreasing the positive gate-source voltage could increase the reliability of the system approximately 8 times without affecting the efficiency significantly. Moreover, adding redundancy in the system could also increase the mean time to failure approximately 5 times.**

Keywords*— *Inveter, Markov Chain, Motor Drive Application, Power Modules, Reliability, SiC, Silicon Carbide, Voltage Source Conveter.

I. INTRODUCTION

Silicon Carbide (SiC), as a wide band gap material, offers three main potential benefits compare to the currently used Silicon (Si). These benefits can be listed as higher efficiency, higher switching frequency and higher temperature of operation [1]. SiC technology with its benefits has been shown in many applications, such as, power inverters [2], modular multilevel converters [3], hybrid electric vehicles [4], resonant converters [5], and dc-dc converters [6].

If high efficiency is targeted, the most important parameter that has to be controlled is the power losses. These power losses can be divided into two components, the switching losses and the conduction losses. In order to reduce the switching losses it is important to ensure a low inductive path so as a fast switching performance of the device is achieved. One possibility to reduce the conduction losses is to parallel connect either discrete components or to build power modules with several chips connected in parallel [6]-[9]. Another possibility, which could result in not only reduction of the conduction losses but also in a fast switching performance, is the parallel connection of lower current rated power modules. This will result in low losses and higher power ratings. This has been proposed and tested in [10] [11], where and efficiency higher than 99 % has been reported for a power rating higher than 300 kVA.

Nevertheless, increasing the amount of components has a negative impact on the reliability performance of the system. This will introduce an undesired tradeoff between efficiency and reliability. Several studies have been done regarding the reliability performance of SiC devices. These studies have analyzed different modes of failure of the devices, such as; short-circuit behavior and protection [12]-[14], long term reliability [15]-[23] and gate-oxide stability and threshold voltage instability [24]-[29], as well as high temperature conditions [30]-[32].

However, these studies have been focused on the variation of the electrical internal parameters, such as the threshold voltage, of the devices. Therefore, it is the main proposal of this paper to analyze the reliability aspect of a SiC power electronic system using the information derived from the reliability tests. An estimation of the life expectancy of a three-phase two-level voltage source converter (VSC) for motor drive applications, as well as, deriving important information about what parameters govern the reliability of the system will be done. Section II, will give a description and experimental results of the system analyzed in this paper. In Section III, a reliability analysis is described and the results are discussed in Section IV. Finally, the conclusions are presented in Section V.

II. VOLTAGE SOURCE CONVERTER

The three-phase two-level VSC for motor drive applications analyzed in this paper has a switching frequency of 20 kHz and, an output current of 450 A RMS, a dc-link voltage of 650 V. Assuming a typical line-to-line output voltage of 400 V, the rated output power will be 312 kVA.

It makes use of parallel-connection of power modules. This will reduce the on-state resistance, which will result in a reduction of the conduction losses. This is important when high efficiency is targeted. The power module used in this system is the Cree Inc. CAS100H12AM1 (see Fig. 1(a)). This is an all-SiC power module rated at 1200 V and 168 A. It has an on-state resistance of 16 mΩ at room temperature (RT). Each switch position is built with parallel-connected SiC metal-oxide silicon field-effect transistors (MOSFETs) and antiparallel SiC Schottky diodes. Fig. 2 shows a photograph of the partially built VSC analyzed in this paper.

The requirements for high efficiency and current density are met when ten power modules are connected in parallel. This keeps the switching losses unchanged, while reducing the conduction losses by a factor of ten. Furthermore, the ten parallel-connected power modules for each phase were chosen without any sorting whatsoever. Additionally, a proper current density means that at rated load current, the current flowing through each of the power modules is sufficiently high to increase the junction temperature to the level where the on-state resistance is well within the positive-temperature-coefficient range. Being in this range is an essential condition for the auto-balancing mechanism of the current. This guarantees a uniform sharing of the current among the parallel-connected power modules. Moreover, an even number of power modules reduce the system complexity and is an important factor if a symmetrical placement is targeted [10].

Figure 1: Photograph of the SiC power module.

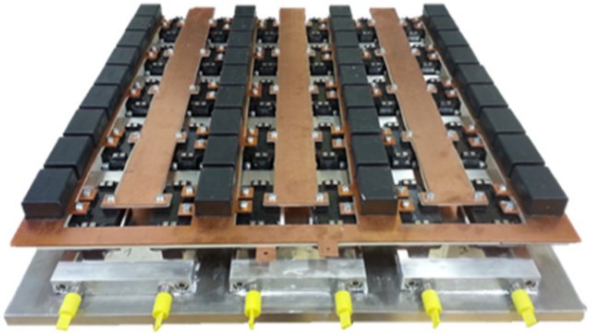


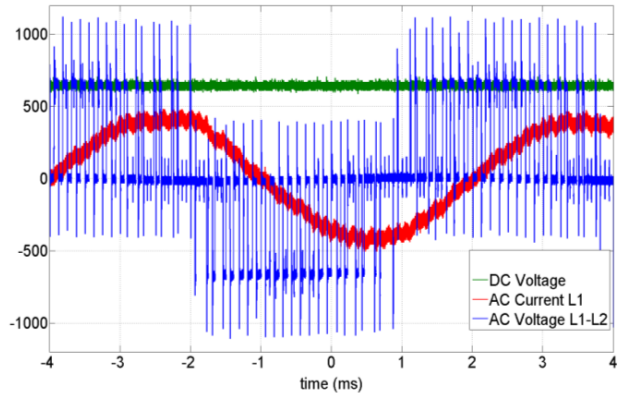
Figure 2: Photograph of the partially built VSC.

In order to reach even higher efficiency it was decided to use the SiC MOSFETs also in the reverse direction. A blanking time of 600 ns was used. Also a switching frequency of 20 kHz was chosen in order to reduce the size of the passive components, such as the dc-link capacitance. For this application it was decided to use MKP capacitors (Metallized Polypropylene Film Capacitors), in particular MKP1848C66012JY5, which meet the requirement of voltage ratings and capacitance. Finally, a total dc capacitance of 720 µF was found for the desired ripple of the dc-link voltage. Additionally, distributed gate-drive units were connected directly to the gate pins of the power modules such that a reduced stray inductance of the gate leads is achieved. This is important for minimizing the Miller effect and achieving a high switching speed, necessary for the high efficiency approach. Table I presents the electrical parameters of the VSC. A more detailed explanation of the methodology and construction process of this converter can be found in [11].

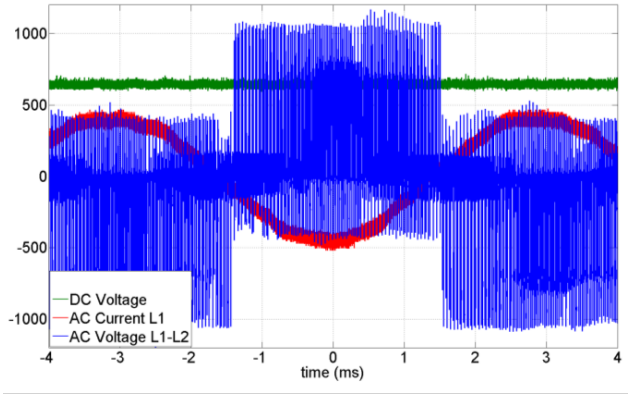
TABLE I. ELECTRICAL PARAMETERS OF THE THREE-PHASE INVERTER

Power Rating, Sn	312 kVA
Input Voltage	650 V DC
Output Line-to-Line Voltage	400 V RMS
Output Phase Current	450 A RMS
Switching Frequency, f_s	20 kHz
DC Capacitance, C	720 µF
Blanking Time, T_D	600 ns

Fig. 3(a) and Fig. 3(b), show the experimental results of the inverter operating at 4 kHz and 20 kHz respectively, supplying a motor drive. These results were obtained at more than 200 kVA. Symmetrical phase current with a motor drive as a load and closed-loop control are shown. The line-to-line voltage is also illustrated showing typical characteristics for pulse-width modulation (PWM) as expected. Table II shows the experimental results driving an electrical machine with efficiency higher than 99% was achieved.



(a)



(b)

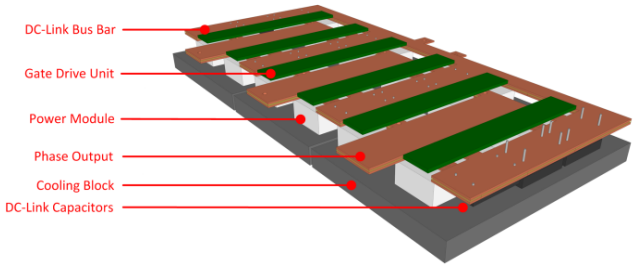
Figure 3: Inverter waveforms during operation at nominal power of 207 kVA and switching frequency of (a) 4 kHz and, (b) 20 kHz.

TABLE II. EXPERIMENTAL RESULTS OF THE THREE-PHASE INVERTER AT 20 KHZ

Output Line-to-Line Voltage	397.88 V RMS
Output Phase Current	293.45 A RMS
Input Voltage	649.83 V DC
Input Current	153.44 A DC
Speed	2000 rpm
Torque	406.07 N/m
Efficiency, η	99.07 %

Furthermore, in order to perform a reliability analysis it is important to extrapolate the mean time to failure (MTTF) from the accelerated tests of each component. It is important to note that the power module used to build the converter consists of parallel connection of single chips from the first generation of Cree devices. These components have evolved into a second generation and even a third where the reliability issues as well as performance have been investigated and improved [18] [19]. Therefore, in this paper, the reliability calculations have been performed using the data from the second generation. A corresponding design, targeting high efficiency using parallel connection of power modules using the Cree Inc. CAS300M12BM2 (see Fig. 4(a)) power module rated at 1200 V and 300 A, with an on-state resistance of 5 mΩ at RT, has been proposed for the calculations, as shown in Fig. 4(b).

(a)



(b)

Figure 4: (a) Photograph of the SiC power module, (b) Layout of the proposed VSC.

Using the information from the manufacturer, available in [15] [16] and considering the values for the rated application of the converter, Fig. 5 for the gate-source voltage (V_{GS}) stress of the MOSFETs, Fig. 6 for the drain-source voltage (V_{DS}) stress of the MOSFETs and, Fig. 7 for the temperature stress of the diodes, were plotted. The MTTF values have been derived for each failure mode in the case of the MOSFETs. Table III summarizes the MTTF and failure rate of the components at the rated condition, including the DC-link capacitors used for the construction of the inverter.

TABLE III. MTTF AND FAILURE RATE OF THE COMPONENTS

Component	Rated Condition	MTTF [hours]	Failure Rate, λ
MOSFETs, V_{GS} Stress	20 V @150 ºC	10^7	$9.03\text{x}10^{-4}$
MOSFETs, V_{DS} Stress	1000 V @150 ºC	$6.5\text{x}10^7$	$1.35\text{x}10^{-4}$
Power Diode	150 ºC	$6\text{x}10^7$	$1.46\text{x}10^{-4}$
DC-Link Capacitor	1000 V	10^8	$8.76\text{x}10^{-5}$

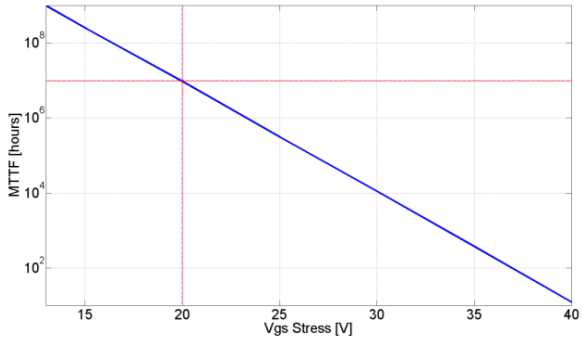


Figure 5: Extrapolated MTTF of 10^7 hours at V_{GS} = 20 V. TDDB of Gate Oxide on 20 A for the Gen2 of SiC MOSFETs [16].

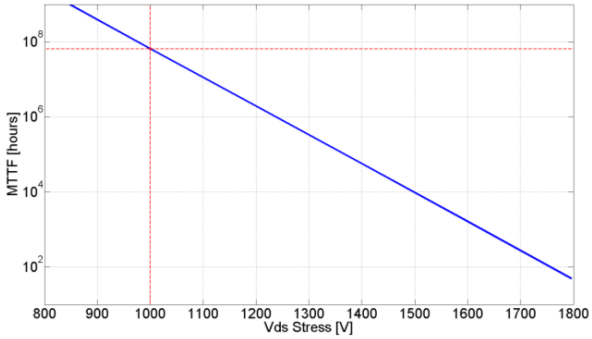


Figure 6: Extrapolated MTTF of $6.5\text{x}10^7$ hours at V_{DS} = 1000 V. Accelerated field testing at 150 °C for the Gen2 of SiC MOSFETs [16].

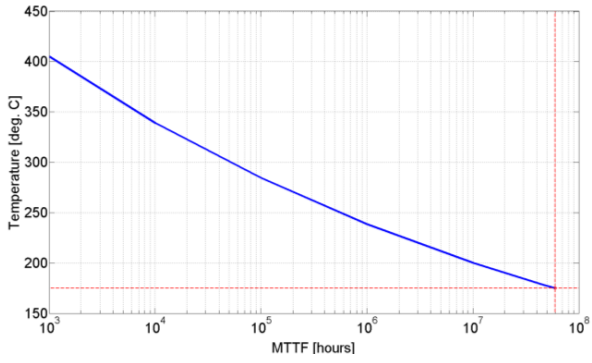


Figure 7: Extrapolated MTTF of $6\text{x}10^7$ hours at 175 °C for the SiC Power Diode [15].

The extrapolated values are related to the single chip. Therefore a reliability calculation must be done in order to obtain the MTTF and failure rate of the power module (see Table IV). This calculation basically consists in the series connection of all the single chips used in order to build the power modules, as shown in Fig. 8. The failure rate for the power module considering both failure modes, the V_{GS} stress and the V_{DS} stress, were calculated using Eq. 1. This is mainly due to the fact that all the chips must be on the safe state so as the module can operate properly.

$$\lambda_{Module} = \sum_{i=1}^{10} \lambda_{Diode_i} + \sum_{i=1}^{10} \lambda_{MOSFET_i} \quad (1)$$

TABLE IV. MTTF AND FAILURE RATE OF THE SIC MOSFET POWER MODULE

Failure Mode	MTTF [years]	Failure Rate, λ
V_{GS} Stress	95.32	0.0105
V_{DS} Stress	356.16	0.0028

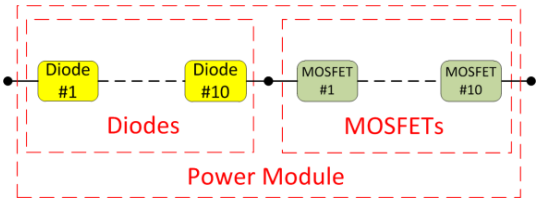


Figure 8: Reliability block diagram for the SiC power module.

III. RELIABILITY ANALYSIS

In this paper, as shown in Table II and Table III, two failure modes have been analyzed. These are: V_{DS} stress and V_{GS} stress. Moreover, two cases of analysis have been performed. The first case, no redundancy, while in the other hand; the second case, takes advantage of the parallel connection of power modules and introduces the so-called, active redundancy.

A. No Redundancy

When no redundancy is considered, all the components of the system are connected in series for the reliability analysis as shown in Fig. 9. This means, that all the components must be working properly to consider that the system is working. Table V shows the calculated MTTF, using Eq. 2, for each failure mode as well as the failure rate for the rated condition shown above in Table I. It is possible to note that the life expectancy is dominated by the gate voltage stress, and it is approximately 8 years.

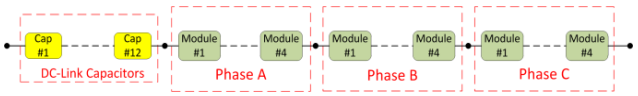


Figure 9: Reliability block diagram for the high-efficiency SiC three-phase inverter without redundancy.

$$\lambda_{Inv} = \sum_{i=1}^{12} \lambda_{Cap_i} + \sum_{i=1}^{12} \lambda_{Module_i} \quad (2)$$

TABLE V. MTTF AND FAILURE RATE OF THE HIGH-EFFICIENCY SIC THREE-PHASE INVERTER WITHOUT REDUNDANCY

Failure Mode	MTTF [years]	Failure Rate, λ
V_{GS} Stress	7.88	0.1269
V_{DS} Stress	28.78	0.0347

B. Active Redundancy

For this case, active redundancy, the VSC required only half of the power modules per phase in order to operate in the safe at the rated conditions (see Fig. 10). Therefore, a certain degree of redundancy could be achieved. In order to do that, additional components should be included in the switching loop, such as disconnectors. These components will add parasitic inductances that modify the switching performance and consequently the efficiency of the system. However, for this paper, all these additional components are considered to be more reliable than the power modules and capacitors.

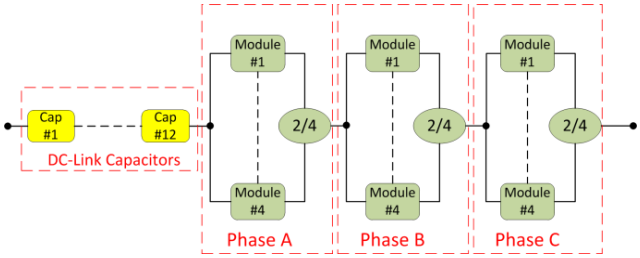


Figure 10: Reliability block diagram for the high-efficiency SiC three-phase inverter with active redundancy.

In order to calculate the MTTF of the system, several calculations must be performed, considering the fact that the failure rate is not constant. For redundant systems, a higher reliability is expected for shorter mission times.

For each phase of the inverter four different states are considered. These states are: (a) fully functional (all power modules working), (b) one failed (one power module failed), (c) two failed (two power modules failed) and, (d) phase failed (more than two power modules failed). Finally, the failure rate for each state must be calculated using the methodology for

series and parallel system. For instance, for the first state (a), Fig. 11 shows the equivalent system of a single phase, and using Eq. 3, the failure rate was calculated. Similarly, calculations were performed for each of the other states.

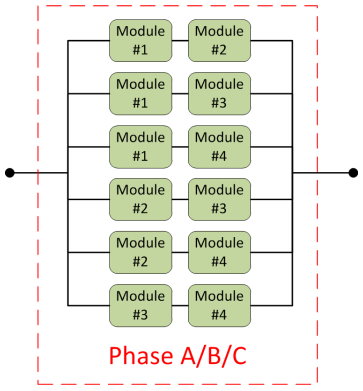


Figure 11: Reliability block diagram for one phase of the high-efficiency SiC three-phase inverter with active redundancy.

$$\lambda_{Phase} = \frac{2\lambda_{Module}}{\sum_{i=1}^{6} \frac{1}{i}} \quad (3)$$

Consequently, Fig. 12 shows the transition between the considered states using the so called Markov Models. The probabilities of failure with respect to the mission time were calculated for each state of the system and for each failure mode as seen in Fig. 13(a) and Fig. 13(b). From these probabilities, the failure rate of the system could be calculated, as well as the probability density function, which contains the MTTF (see Fig. 13(c) and Fig. 13(d)). It must be noted that the plots for V_{DS} stress and V_{GS} stress, are extended to 400 years and 100 years respectively in order to illustrate how the failure rate changes regarding the mission times. Finally, active redundancy increases the MTTF several times, approximately 41 years, as shown in Table VI.

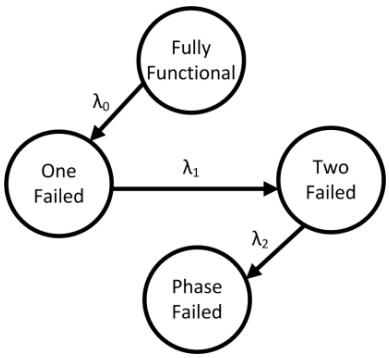
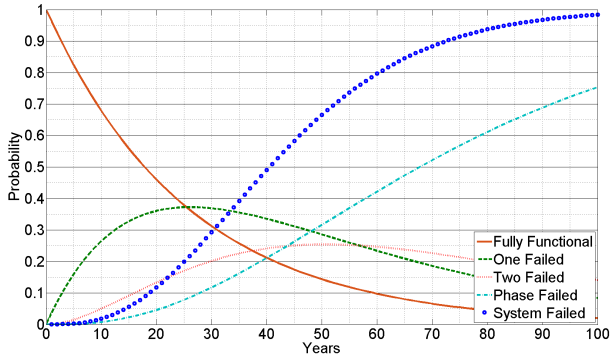
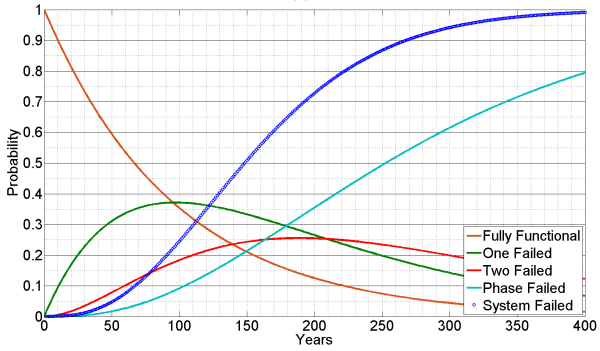


Figure 12: Markov diagram for one phase of the high-efficiency SiC three-phase inverter with active redundancy.



(a)



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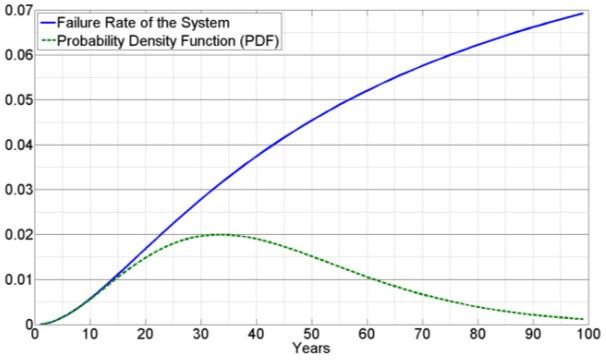
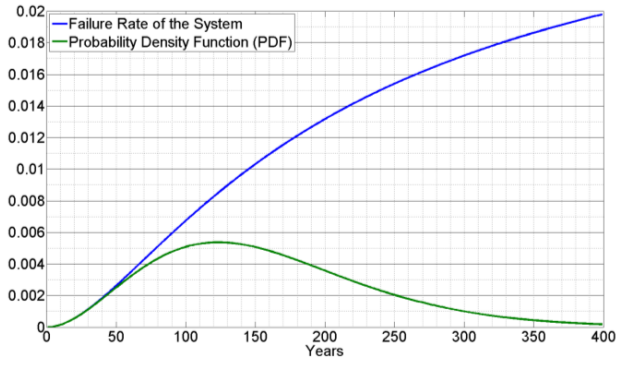


(c)



(d)

Figure 13: Probability of each state of Markov Models and Probability of system failure regarding the mission time for the (a) gate-source voltage stress, (b) drain-source voltage stress. Failure Rate and Probability density function regarding the mission time for the (c) gate-source voltage stress, (d) drain-source voltage stress.

TABLE VI. MTTF AND FAILURE RATE OF THE HIGH-EFFICIENCY SIC THREE-PHASE INVERTER WITH ACTIVE REDUNDANCY

Failure Mode	MTTF [years]
V_{GS} Stress	41.29
V_{DS} Stress	155.34

IV. DISCUSSION

As shown in the previous section, the gate-source voltage stress determines the life expectancy of the system. A more detailed description on how the MTTF varies regarding the gate voltage is shown in Fig. 14. Higher life expectancy is obtained by reducing V_{GS}. However, if active redundancy is included, a similar value of MTTF could be achieved as when the V_{GS} is reduced without reducing it.

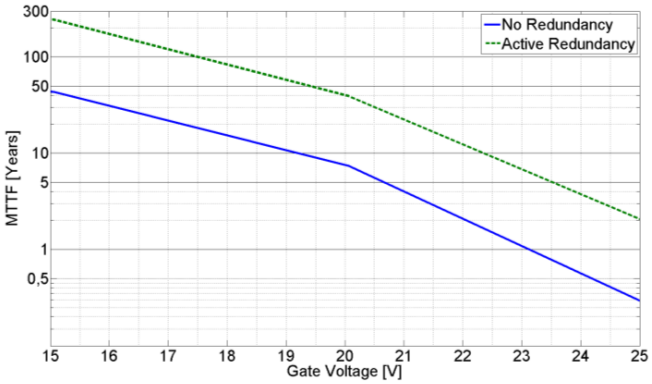


Figure 14: MTTF as function of Gate Voltage. No Redundancy, (blue), Active Redundancy (dash green).

Furthermore, reducing the gate-source voltage, will impact different parameters of the system such as the on-state resistance and the switching speeds, thus, affecting the total losses of the system. Using a simulation model of the power module, it is possible to estimate how these losses depend on the gate voltage. The simulation model of the investigated power module (CAS300M12BM2) was developed using ANSYS Simplorer and Q3D. Finally, the power module was simulated with LTSPICE including the parasitic elements derived from ANSYS. Fig. 15(a) and Fig. 15(b) show the experimental results and the simulation results, respectively, for the turn-ON transitions. Similarly, Fig. 15(c) and Fig. 15(d) show the results for the turn-OFF transition. It can be noted that the simulation results fit the experimental results appropriately. Therefore, an estimation of how the total losses change regarding V_{GS} could be performed.

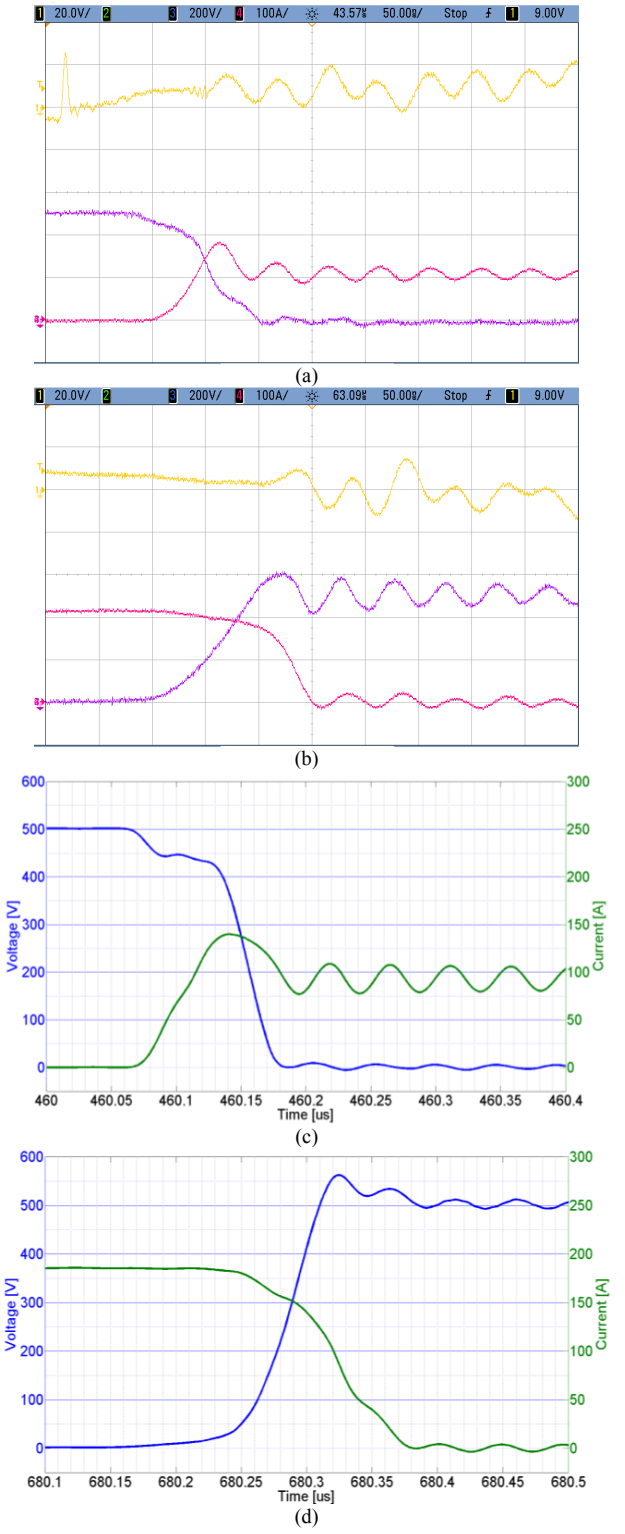


Figure 15: (a) Turn-ON, (b) Turn-OFF switching waveforms of the power module. Measured drain-source voltage of the SiC MOSFET, (purple, 200 V/div), drain-source current of the SiC MOSFET, (pink, 100 A/div), gate-source voltage of the SiC MOSFET, (yellow, 20 V/div), (time-base 50 ns/div), (c) Turn-ON, (d) Turn-OFF transients of the simulated SiC MOSFET power module, drain-source voltage of the SiC MOSFET, (blue, 100 V/div), drain-source current of the SiC MOSFET, (green, 50 A/div).

Using the developed simulation model, the transient performance at different gate voltages were analyzed and plotted in Fig. 16. It is possible to estimate how the switching losses as well as the conduction losses vary depending on the gate voltage. As expected, the lower V_{GS}, the higher the losses.

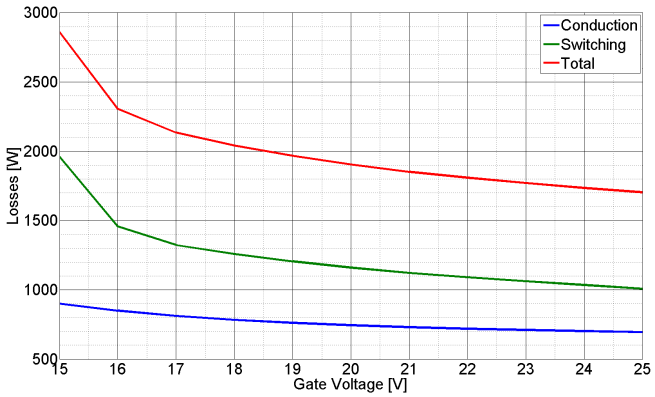


Figure 16: Conduction losses (blue), Switching losses (green), Total losses (red) regarding of the Gate Voltage.

Therefore, reducing the gate voltage will affect the efficiency of the system as shown in Fig. 17. By decreasing the positive gate-source voltage, 5 V, the reliability of the system is increased approximately 8 times and the efficiency is reduced by approximately 0.4 %. Nevertheless, this reduction of the efficiency is not significant compared to the MTTF improvement.

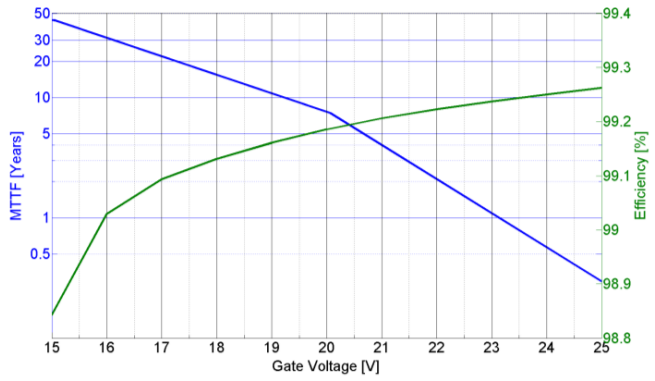


Figure 17: MTTF (blue) and Efficiency (green) regarding of the Gate Voltage.

Several assumptions have been made in order to perform the reliability study. First, when active redundancy is introduced in the study implies that the power modules that fail during operation are disconnected. As soon as this occurs, the remaining power modules will conduct higher current in order to maintain the rated output power. By conducting higher current the device temperatures will increase affecting the reliability of the system. Nevertheless, the reliability calculations have been done with extrapolated values at 150 ºC, i.e. that the study performed is a worst-case analysis.

Also, during the blanking time, part of the current flows through the intrinsic body diodes of the MOSFETs. Several studies have been dealing with the reliability of the body diode [20]-[22]. These studies show a stable body diode performance under a 1000 hour DC body diode stress of 22 A.

Additionally, the negative gate-source voltage, used in many applications, might apply more stress and therefore determine the reliability of the complete system. Several studies have been performed already regarding this aspect [21]-[23]. These studies show a stable threshold voltages for a V_{GS} = -15 V of stress for 1000 hours at 150°C. The average threshold voltage shift for the devices under this stress was approximately -50 mV.

However, it is the hypothesis of the authors that the use of the body diode of the device as well as the negative bias stress might impact the reliability of the system and could determine the life of the inverter. Therefore, this must be investigated in order to determine the failure rate and MTTF in respect to these conditions.

Moreover, the packaging itself could be the factor that determines the reliability of the system. However, for the power module analyzed in this paper, the package is similar to the one used for silicon IGBT power modules, which has been proven for several applications under different reliability standards. This is not considered in this work as a dominant factor of the reliability.

Finally, different strategies could be used so as to increase the reliability of a system, such as reducing the temperature. In order to do this, a lower current must flow through the power modules, i.e. more devices connected in parallel, which will not necessarily increase the reliability of the system. Instead adding additional components might have a negative effect on the operating life of the system. Another possibility is to decrease the voltage level which could also increase the reliability of the system. However, in this case, an additional transformer is needed so as to satisfy the rated conditions of the system. Nevertheless, the drain-source voltage stress does not determine the reliability of the system. Lastly, higher quality components, i.e. better SiC chips will also increase the final reliability.

V. Conclusions

A possible solution for higher efficiencies using SiC has been presented, using parallel connection of power modules. Experimental results of the proposed VSC driving a motor verify an efficiency of 99%. A reliability analysis has been performed on a 312 kVA VSC for motor drive applications. Two different failure modes have been studied, the V_{GS} stress and the V_{DS} stress. Additionally, two possible cases were analyzed: no redundancy and active redundancy. This analysis has shown that the gate-source voltage stress determines the reliability and MTTF of the complete system. Nevertheless,

decreasing the positive gate-source voltage could increase the reliability of the system approximately 8 times without affecting the efficiency significantly. Moreover, adding redundancy in the system could also increase the MTTF approximately 5 times.

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