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Reliability of large periphery GaN-on-Si HFETs

S. Singhal *, T. Li, A. Chaudhari, A.W. Hanson, R. Therrien, J.W. Johnson, W. Nagy, J. Marquart, P. Rajagopal, J.C. Roberts, E.L. Piner, I.C. Kizilyalli, K.J. Linthicum

Nitronex Corporation, 628 Hutton Street, Suite 106, Raleigh, NC 27606, United States

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Abstract

GaN devices exhibit excellent potential for use in many RF applications. However, commercial acceptance of the technology has been hindered by the scarcity and non-statistical nature of reliability results. In this work we present a full device level reliability study of GaN-on-Si HFETs. Reliability results on this technology include three-temperature DC data that show an activation energy of 1.7 eV and an average failure time $>10^7$ h at 150 °C. Additionally, long duration DC lifetest (30 000 device hours) and RF lifetest (4000 device hours) results demonstrate a repeatable low drift process. Environmental tests such as autoclave and ESD demonstrate the ruggedness of the material system and technology. Finally, initial failure analysis is discussed.

1. Introduction

In the past several years GaN has progressed from a lab technology exhibiting high power densities on small periphery devices to a viable commercial technology showing repeatable high total power results on large periphery devices [1–3]. The remaining challenge, before GaN devices can see significant product insertion, is demonstration of good reliability. In this paper we present a complete device level reliability dataset on Nitronex's baseline power transistor technology. The results show GaN-on-Si reliability levels meet or exceed those of many established technologies.

2. Background

Devices reported in this work are based on undoped $Al_{0.26}Ga_{0.74}N$/GaN heterostructures grown on high resistivity Si(1 1 1) substrates by metal organic chemical vapor deposition (MOCVD). The process includes Ni/Au gates and Ti/Al/Ni/Au ohmic contacts. Source and drain fingers are plated with Au and airbridges are used for source connection. Devices are passivated and encapsulated with SiN_x. All devices in this study have a gate length of 0.7 μm, gate-to-source spacing of 1 μm, and gate-to-drain spacing of 3 μm. Detailed descriptions of the process have been provided elsewhere [1,2].

All results reported in this work are taken from 36 mm AlGaN/GaN HFETs with unit gate width of 200 μm and gate pitch of 30 μm. A optical micrograph of this device is shown in Fig. 1. The devices come from Nitronex's baseline manufacturing process, which has demonstrated the ability to produce repeatable devices [1].

* Corresponding author. Tel.: +1 919 807 9100; fax: +1 919 807 9200.
E-mail address: ssinghal@nitronex.com (S. Singhal).

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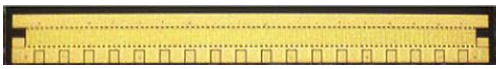

Fig. 1. Optical micrograph of 36 mm die consisting of 180 gate fingers with 200 μm unit gate width and 30 μm gate pitch.

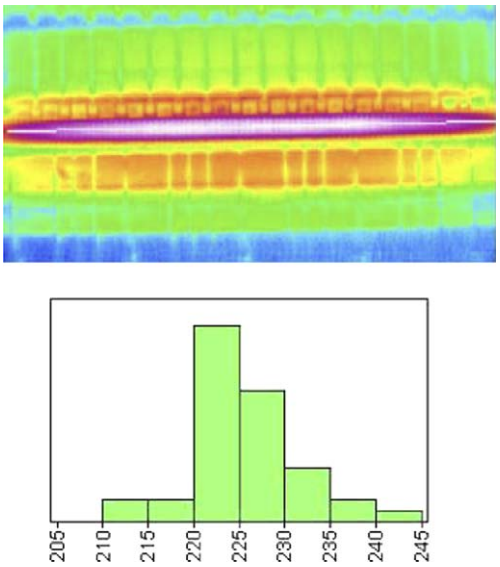

Fig. 2. Thermal image of T_j for typical device (top) and distribution plot of T_j from 42 devices (bottom). All devices biased at 28 V and 2.3 A.

For this reliability study, six wafers were selected randomly out of a 150-wafer baseline distribution and subjected to an extensive battery of tests. Over 400 dic were used to generate the dataset described in this study. The device configuration used in all testing consisted of a transistor die attached to a high thermal conductivity CuW single-ended, ceramic packages using a AuSi eutectic process. The package was lidded with a non-hermetic epoxy sealed lid. The sources were grounded to the package base by way of substrate vias in the 150 μm-thick silicon wafer. Internal matching networks were used to transform both the input and output to higher impedances. These devices typically deliver 60–70 W of CW saturated output power along with 60–65% efficiency at an operating voltage of 28 V and frequency of 2.14 GHz [4]. Prior to life testing, IR imaging of 42 devices was used to characterize junction temperature (T_j). A typical thermal image and the distribution plot of T_j for all devices are shown in Fig. 2. The junction-to-case thermal resistance of 2.3 °C/W or junction-to-heatsink thermal resistance of 2.6 °C/W was used for all lifetests.

3. Results and discussion

The philosophy for this initial round of testing was to focus on reliability of the intrinsic device or process platform in order to gain insight into associated failure mechanisms. The testing can be divided into three major categories: DC, RF, and environmental testing. DC testing consisted of a three-temperature life test to determine activation energy and a 200 °C high temperature operating life (HTOL) test to provide a significant number of device hours under accelerated operating conditions. RF testing focused on determining whether RF operation introduced failure mechanisms different from those observed in the DC testing. Survivability testing was also performed using high VSWR (voltage standing wave ratio) mismatch tests. Environmental testing included humidity resistance and ESD testing. Results in each of these areas are presented below.

3.1. DC testing

In DC-HTOL testing, devices are stressed at the DC operating voltage and maximum junction temperature for extended periods of time. For this study devices were stressed at 28 V and 200 °C using a custom built HTOL test rack capable of simultaneously stressing 100 power devices. This test methodology has been used over the past three years to systematically study several process generations. All test runs have been at the aforementioned 28 V and 200 °C with stress times ranging from 1000 to 2000 h. In total more than 125 devices have been tested and over 150 000 device hours of DC-HTOL testing have been accumulated. In general trends and data from all 5 lifetests have shown similar results. Test runs are described in detail in Table 1.

This work focuses on results of DC-HTOL testing from the most recent generation of baseline devices described in Section 2. Thirty devices were randomly selected from five different wafers and placed under HTOL stress for 1000 h each (30 000 device hours). The stress condition was $V_d = 28$ V, $I_d = 2.3$ A, $T_j = 200$ °C. The HTOL rack uses water-cooling to maintain a baseplate temperature of 30 °C and the current of 2.3 A was chosen (from the thermal imaging data) to produce a T_j of 200 °C. Prior to lifetest all devices went through a biased 24 h DC burn-in. The burn-in is necessary to screen for infant mortality and to stabilize the device. Fig. 3 demonstrates the stabilization of the junction temperature obtained through the

Table 1
Description of historical DC-HTOL tests

Completion date	Device size (mm)	No. wafers	No. devices	Stress time (h)	Device hours (h)
Q2 2003	2	3	18	2000	36 000
Q1 2004	16	5	50	1500	75 000
Q2 2004	16	2	10	1000	10 000
Q4 2004	36	2	20	1000	20 000
Q1 2005	36	5	30	1000	30 000

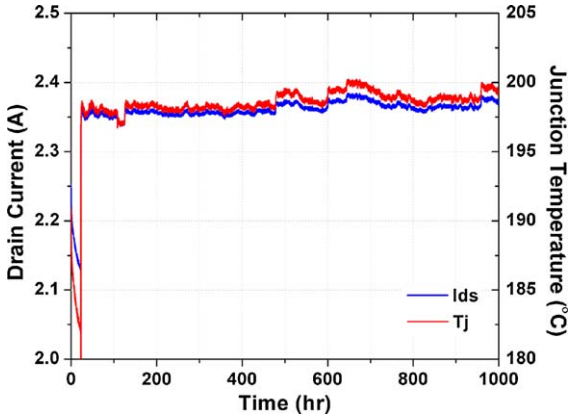

Fig. 3. Plot of I_d and T_j versus time for DC-HTOL test. T_j is readjusted after burn-in and remains relatively constant.

burn-in process. The drain current drop, and hence the associated temperature drop, is compensated for with a readjustment of the drain current. Following the readjustment the junction temperature remains relatively constant throughout the test.

Devices undergo a full battery of DC and RF characterization prior to the lifetest and this characterization is repeated at several intervals throughout the test. In this case devices were removed from the HTOL system after 24, 168, 500, and 1000 h of stress. At each of these downpoints, the full battery of DC and RF testing was repeated. Box plots of the saturated drain current (I_{dss}) versus test interval are shown in Fig. 4 and reveal tight distributions and a logarithmic dependence between drift and time.

A three-temperature DC test was also performed to complement the DC-HTOL test. This test utilizes a smaller sample size, but is designed to determine a temperature acceleration factor. It is generally assumed that semiconductor failures due to parametric drift follow an Arrhenius relationship with temperature and the acceleration factor can be expressed as activation energy, E_a [5]. Once again a custom test setup was used to stress the devices. The setup consisted of an oven with in situ thermocouple feedback loop to control the ambient temperature. Junction temperatures of 260, 285, and 310 °C were used for the test. The bias conditions were identical to the conditions used for the DC-HTOL test, $V_d = 28$ V and $I_d = 2.3$ A. At each condition, 4–8 devices were stressed with the stress times ranging from 500 to 1000 h. The in situ drain current was measured at 2 min intervals to monitor the drift during the stress. Full DC and RF testing was performed at the beginning and end of the test in order to insure integrity of test.

Fig. 5 shows the in situ drain current versus time for a typical device from each of the stress conditions in the three-temperature test. Additionally, the 200 °C stress condition from the DC-HTOL test is shown. The results demonstrate the expected increase in drift with increasing temperature. A failure criterion of 15% drift is used and the data is extrapolated to determine failure time for an average device in each temperature group. The resulting average failure times are plotted on an Arrhenius plot in Fig. 6, revealing an E_a of 1.7 eV. Inclusion of the lower temperature 200 °C results from the DC-HTOL test provides greater confidence that additional low activation energy mechanisms are not present in this process. Assuming a constant E_a, an extrapolation to a more practical operating temperature of 150 °C results in an average failure time $>10^7$ h. These results compare favorably to existing technologies such as Si-LDMOS and GaAs pHEMTs [6–8].

Further analysis can be performed on the DC test results to predict the long-term drift over 20 years. For

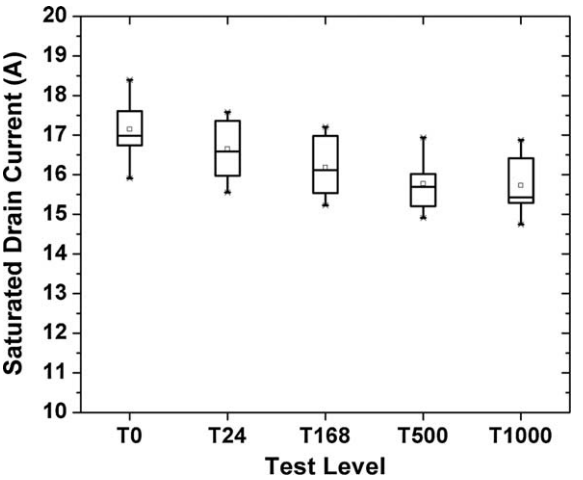

Fig. 4. Box plots showing I_{dss} versus time from DC-HTOL population of 30 devices.

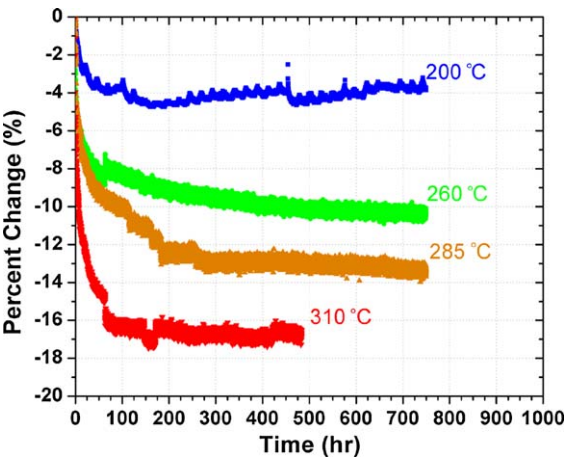

Fig. 5. Drain current percent change versus time for typical devices from 200, 260, 285, and 310 °C DC stress test.

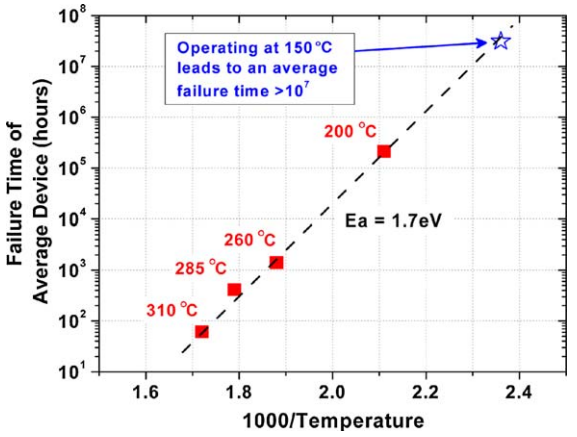

Fig. 6. Arrhenius plot showing $E_a = 1.7$ eV and an average failure time $>10^7$ h at 150 °C.

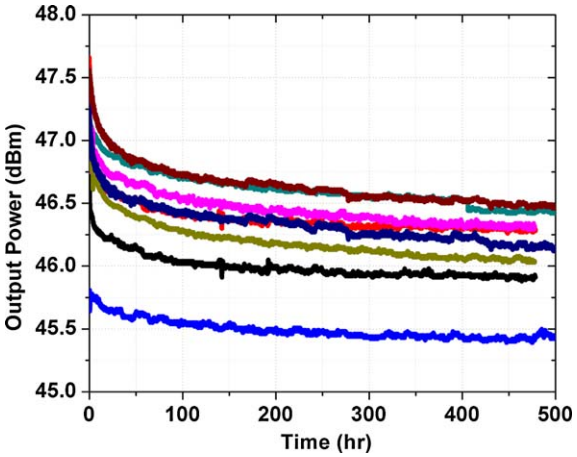

Fig. 8. RF-HTOL results depicting output power versus time.

instance, the DC-HTOL results in Fig. 4 exhibit a logarithmic dependence between drift and time. A logarithmic fit can be extended out to 20 years (175 200 h) and predict the long-term drift at 200 °C. Additionally one can use the E_a previously determined and apply an acceleration factor to predict performance closer to the use temperature of 150 °C. Applying these extrapolations to the DC-HTOL test results in 20-year drift rates for I_{dss} of 14% at 200 °C and 5% at 150 °C, as demonstrated in Fig. 7.

3.2. RF testing

RF life testing was performed by way of a RF-HTOL test. Conditions were chosen to be similar to those used for DC-HTOL ($V_d = 28$ V, $T_j = 200$ °C) with the addition of RF input power sufficient to drive the device into 3 dB compression. Eight devices were stressed for 500 h each. The RF stress was performed at Naval Surface Warfare Center in Crane, IN. The devices were placed in a 50 Ω application board with flange temperature adjusted to provide T_j of 200 °C (flange temperature ~80–100 °C). Once again an adjustment was made in the first 24 h to ensure that the temperature remained ~200 °C throughout the test. In-situ monitoring of the output power was used to track degradation.

Fig. 8 shows that all 8 devices exhibit logarithmic dependence between output power drift and time, similar to DC I_{dss}. Extrapolating the curve to 20 years predicts a long-term drift rate of 0.9 dB at 200 °C. Plotting the output power drift (in Watts), from the RF-HTOL test, and the drain current drift, from the DC-HTOL test, reveals a similar percentage drift versus time, as seen in Fig. 9. The similar logarithmic depen-

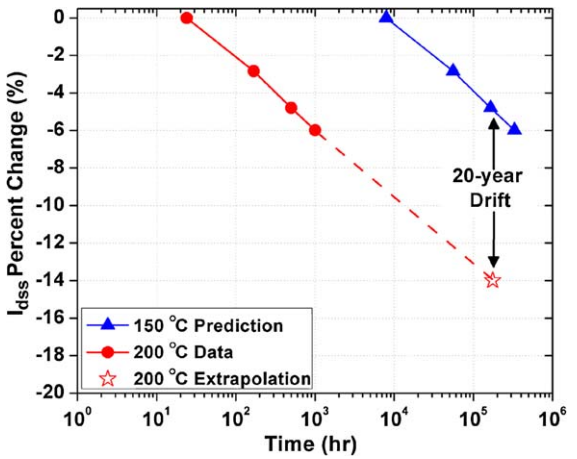

Fig. 7. Extrapolation of 200 °C DC-HTOL data demonstrating 20-year I_{dss} drift of 14% and 150 °C prediction demonstrating 5% drift.

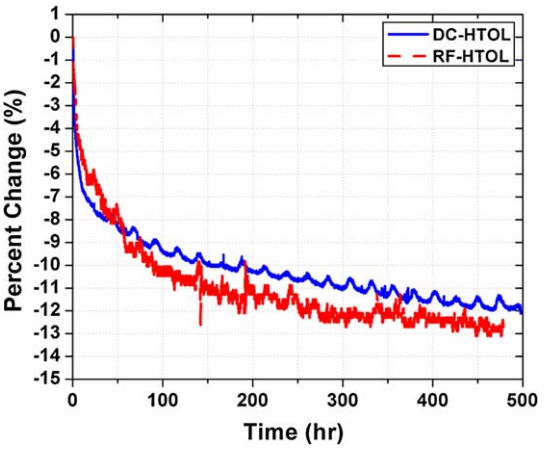

Fig. 9. Comparison of drift from DC-HTOL and RF-HTOL test demonstrating similar performance.

dence and overall drift rates between DC and RF stress testing suggests that the DC stress testing is sufficient for predicting device reliability.

Additionally, ruggedness testing was performed using a VSWR (voltage standing wave ratio) mismatch test. VSWR testing was performed by terminating the output of the application board with attenuation and a short. A 1 dB attenuator and a short were used for 5:1 VSWR, while no attenuation and a short were used for 10:1 VSWR. In each case a line stretcher was used to sweep the impedance through all phases under the mismatch condition. Devices went through full DC and RF characterization before and after VSWR stress. A total of 10 devices were stressed under both VSWR mismatch conditions and all devices survived testing, with minimal changes in parametric performance. Results for 60 V drain leakage ($V_g = -8$ V, $V_d = 60$ V) and output power can be seen in Fig. 10.

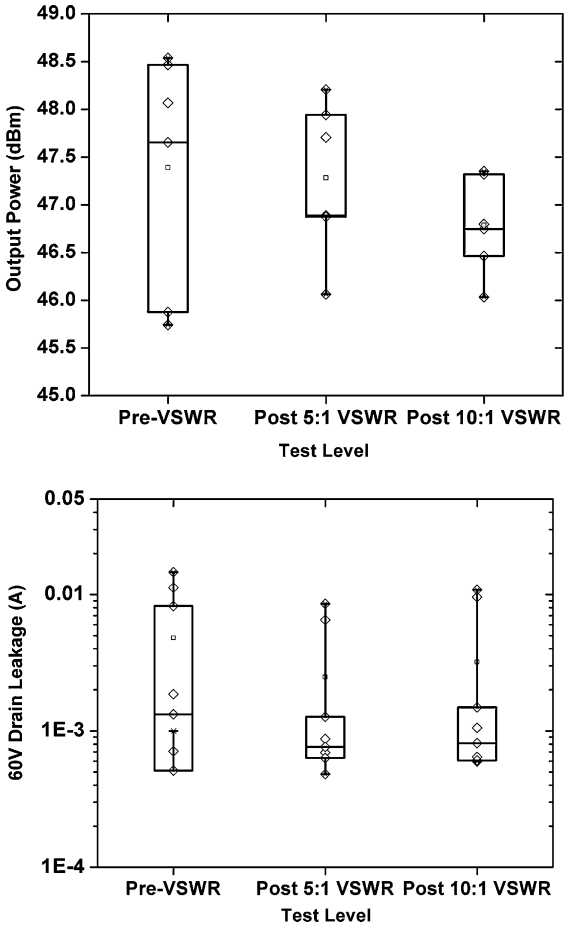

Fig. 10. VSWR results show minimal change in output power (top) and 60 V drain leakage (bottom) after 5:1 and 10:1 VSWR applied.

3.3. Environmental testing

Finally, a battery of environmental tests was carried out on packaged parts. This included autoclave testing, temperature cycling, and ESD testing. The autoclave testing was carried out at 121 °C, 100%RH (relative humidity), 15 psi for 96 h on 20 devices. The results, summarized in Fig. 11, showed no appreciable degradation. Temperature cycling was performed on previous process generations and showed no significant change in parametric performance with similar packaging techniques after 250 cycles at −65 to 150 °C. Visual inspection following the autoclave and temperature cycling test showed no signs of passivation delamination or other physical changes.

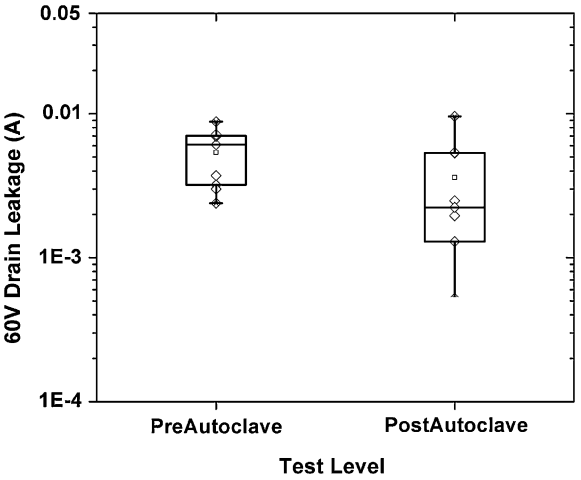

Fig. 11. Results of autoclave test showing minimal change in 60 V drain leakage after 96 h of stress (121 C, 100%RH, 15 psi).

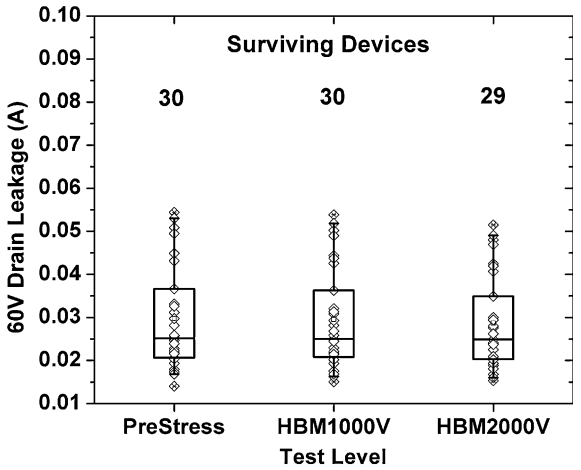

Fig. 12. Results of HBM ESD test demonstrating no failures at 1000 V and 1 failure at 2000 V.

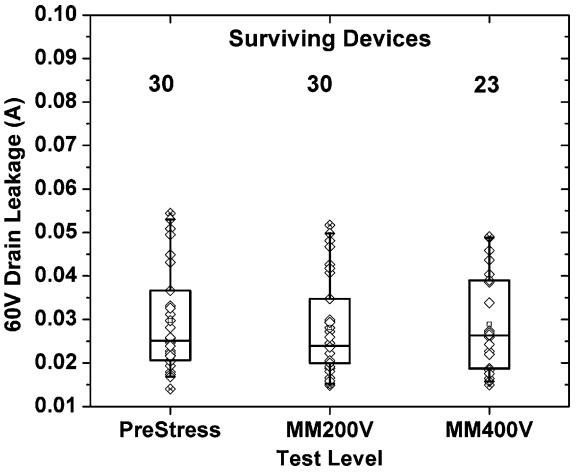

Fig. 13. Results of MM ESD test demonstrating no failures at 200 V and 7 failures at 400 V.

Electrostatic Discharge (ESD) testing was carried out under both human body model (HBM) and machine model (MM) conditions. All pin combinations and polarities were stressed on 30 devices, with failure defined as a 10× increase in 60 V drain leakage current. The results are shown in Figs. 12 and 13. Under HBM conditions all devices survived 1000 V (class 1 C) of stress, with only 1/30 devices failing at 2000 V (class 2). Under MM conditions all devices survived 200 V (class M3), and only 7/30 devices failed at 400 V (class M4).

4. Failure analysis

At the conclusion of reliability testing devices were submitted for failure analysis [9]. Failure analysis efforts were focused on the devices from the DC-HTOL test since this test was closest to actual device operating conditions and also the most statistical. A closer look at the *IV* curves from the DC-HTOL samples revealed an increase (more positive value) in the pinch-off voltage (V_p) with stress time consistent with the observed drop in I_{dss}. This increase in the V_p pointed toward an increase in the Schottky barrier height (SBH). The shift in SBH was confirmed by performing forward diode sweeps on single finger 100 μm transistors before and after stress. In an attempt to discover the cause for the SBH shift, physical analysis was carried out comparing devices from the DC-HTOL test with unstressed parts from corresponding wafers. The physical analysis consisted of FIB (focused ion beam) and STEM (scanning tunneling electron microscopy) images of the source-drain region of each device. Particular attention was paid to gate region of the device and revealed a thin interfacial layer between the gate and semiconductor

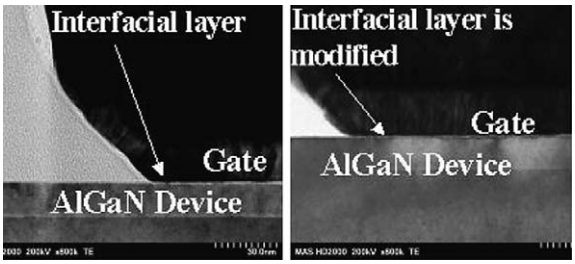

Fig. 14. STEM pictures of unstressed (left) and stressed (right) samples demonstrating modification of interfacial later after stress.

on the unstressed samples, which was unapparent on the devices which had undergone stress. This can be seen in Fig. 14. It was proposed that the modification of the interfacial layer during stress is responsible for the SBH shift and corresponding V_p and I_{dss} shifts.

5. Ongoing work

The reliability dataset presented in this paper is promising and should satisfy most commercial requirements. However, as part of a plan to continuously improve reliability, work has begun in order to confirm the SBH shift theory proposed earlier. An experiment was carried out on wafers where a gate anneal was used to modify the interfacial layer prior to reliability testing. Once again single finger 100 μm transistors were used to measure the SBH before and after stress and showed no change. Based on this encouraging result, a split lot was started where half the wafers were processed with the gate anneal and the other half with no anneal. The lot was processed through the full fabrication flow and

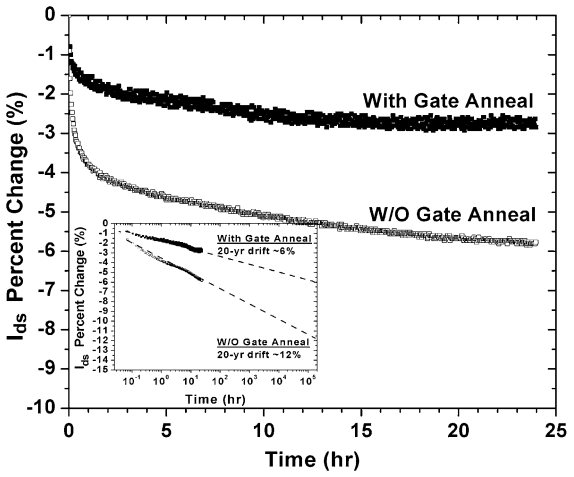

Fig. 15. DC-HTOL results after 24 h of stress on both annealed and unannealed samples showing 50% reduction in drift with gate anneal.

36 mm packaged devices where built from each set of wafers. Fig. 15 shows the dramatic improvement with the gate annealed samples showing half the degradation of the non-annealed samples. Extrapolating this data out to 20-year operating life reveals a reduction in drift at 200 °C from 12% with the unannealed process to 6% with the annealed process. This work is still in preliminary stages and full reports on DC-HTOL and three-temperature testing will be published at a later date.

6. Conclusion

Excellent results have been obtained in terms of DC, RF, and environmental reliability. Accelerated DC life-tests reveal an E_a of 1.7 eV with an average failure time of $>10^7$ h and a predicted 20-year drift rate of $\sim$5% at 150 C. Testing done under RF stress reveal similar drift rates. Initial failure analysis revealed an unwanted interfacial layer under the gate diode and process improvements were made to improve the reliability performance. These results establish Nitronex's baseline GaN-on-Si reliability as being comparable to that of existing technologies and demonstrate the viability of the technology as a manufacturable and reliable platform.

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