Extreme Scaling with Ultra-Thin Si Channel MOSFETs

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Abstract

We examine the scaling limits for planar single gate technology using the ultra-thin Si channel MOSFET. Characteristics for extreme scaled devices with physical gate lengths down to 6nm and SOI channels as thin as 4nm are presented. For the first time, we report ring oscillators with 26nm gate lengths and ultra-thin Si channels.

Introduction

Conventional scaling is becoming very challenging. One promising option for continued scaling without significant departure from standard device structures is the ultra-thin Si channel MOSFET [1-3]. Characteristics for MOSFETs with channel thicknesses of 4nm and gate lengths of 30nm have been demonstrated by others [3]. MOSFETs with gate lengths of 15-40nm on bulk and relatively thick SOI films have also been reported elsewhere [5-10]. In this work we have fabricated ultra-thin Si channel devices with thickness as thin as 4.6nm and with gate-lengths as small as 6nm. For the first time, high-performance ring-oscillators with ultra-thin Si channels and 26nm gate lengths are presented.

Device Fabrication

Ultra-thin Si channel MOSFETs were fabricated on bonded SOI wafers with an initial thickness of 70nm and a 150nm buried oxide layer. The process flow is summarized in Table 1. SOI films were thinned by thermal oxidation and wet etching to achieve the final thickness of 6nm ±2nm. The gate dielectric was formed by thermal oxidation of Si followed by a nitridation process. Gate dielectric thickness splits were carried out on separate wafers with effective-oxide-thicknesses (EOT) of 1.2nm and 2.2nm. A 120nm poly-Si layer was used to fabricate the gate electrode. Conventional 248nm lithography along with aggressive dose conditions and trimming was used to create the sub-lithographic gate dimensions. Gate stack and spacer etch processes were developed specifically to minimize Si consumption in the source-drain region. No channel doping was used with the exception of selected wafers that received halo implants to improve the short channel effect (SCE) and to raise the threshold voltage. In order to reduce external resistance, selective epitaxial Si was grown on SOI layers less than 4-8nm in thickness to form the raised source-drain.

Thick Gate Oxide Ultra-Thin Si Channel CMOS

A TEM cross-section of an ultra-thin Si channel MOSFET is shown in Fig. 1. The EOT in this experiment is 2.2nm and the Si channel thickness is approximately 7nm. The pFET Ids-Vgs and Ids-Vds characteristics with a mild halo implant condition are shown in Fig. 2 and Fig. 3. The saturation current is 366μA/μm, 283μA/μm, and 244μA/μm at Vdd=-1.5V, -1.2V, and -1.0V respectively. The threshold voltage roll-off and sub-threshold slope are shown in Fig. 4 and Fig. 5. The device characteristics clearly indicate that the ultra-thin Si channel is capable of controlling the SCE in pFETs with gate lengths below 50nm even with a mild halo implant condition and a modest gate dielectric thickness. Ids-Vgs and Ids-Vds characteristics for an nFET with a mild halo implant condition are shown in Fig. 6 and Fig. 7. The gate length for this nFET is 38nm, EOT is 2.2nm and T_{Si} is approximately 7nm. The saturation current is 698μA/μm, 567μA/μm, and 466μA/μm at Vdd=1.5V, 1.2V, and 1.0V respectively (Fig. 7). In order to improve the SCE control and provide appropriate threshold voltage, a stronger halo implant condition was used. Fig. 8 shows the Ids-Vgs characteristic of an ultra-thin Si channel nFET with a gate length of 21nm and a stronger halo implant condition. Fig.9 is a plot of the threshold voltage roll-off and clearly shows the effect of the stronger halo implant condition. The increased channel doping concentration for smaller channel lengths causes the threshold voltage roll-up. For channel lengths in the range of about 32-38nm the linear threshold voltage exhibits a steep rise and then begins to roll-off, while the saturated threshold voltage remains fairly flat down to the smallest channel lengths. These results indicate that the ultra-thin Si channel along with the strong halo implant condition is effective in suppressing the threshold voltage roll-off. Sub-threshold slope as a function of gate length is compared for the strong and mild halo implant conditions in Fig. 10. This figure also demonstrates significant improvement in scaling for the strong halo implant condition. The fact that the threshold voltage can be adjusted by the halo implant may have technological significance. If a gate work function solution is not available in time, a more

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conventional approach using halo or channel doping may be used to adjust the threshold voltage. However, the control of threshold voltage variation with channel implant remains a challenging task for ultra-thin Si channel devices.

Ring Oscillators with 26nm Gate Lengths

A similar process as described in the previous section along with optimized implant conditions was used to fabricate high performance ring oscillators with 26nm gate lengths. The delay-per-stage of various ring-oscillators is summarized in Fig. 11. Fig. 12 shows the CMOS inverter delay as a function of Idsat for pFETs and nFETs. Although the saturation current is not particularly high, the delay-per-stage is among the best with respect to the current drive. The small gate dimensions are not only responsible for the good ring oscillator speed but also provide reduction of active power. It is expected that significant performance can be obtained with process optimization. This is the first demonstration of high-performance ring-oscillators with 26nm gate lengths.

Thin Gate Oxide Ultra-Thin Si Channel pFET

In order to evaluate potential performance and SCE control improvements, devices were fabricated using a thinner gate dielectric. A TEM cross-section of an ultra-thin Si channel pFET with a gate length of 14nm and an EOT of 1.2nm is shown in Fig. 13. The channel thickness for this device is 4.6nm. No halo implant was used for this experiment. The Ids-Vgs characteristic of this device is shown in Fig. 14. Saturated sub-threshold slope is 71mV/decade, DIBL is 24mV/V, and Vtsat is –100mV. These results show that even without halo or channel doping, the ultra-thin Si channel is capable of controlling the SCE for very small gate lengths. The reason for the proper threshold voltage is partly due to the threshold voltage shift caused by quantum confinement [11] and fixed-charge in the nitrided gate dielectric. Fig. 15 shows the Ids-Vds characteristic for this device. The saturation current is 439μA/μm, 328μA/μm, and 215μA/μm at Vdd=-1.5V, -1.2V, and -0.9V respectively. Ion-Ioff characteristics for the ultra-thin Si channel pFETs with thin gate dielectric are shown in Fig. 16. For an Ioff of 186nA/μm, an Ion of 328μA/μm is achieved for a supply voltage of -1.2V. For a slightly higher Ioff of 270nA/μm, Ion increases to 398μA/μm for the same supply voltage of -1.2V. The observed variation in Fig.16 is likely related to the sensitivity of threshold voltage, gate capacitance, external resistance, and mobility to variations in T_{Si} [11]. The excellent SCE control and performance are among the best reported for devices with these gate dimensions.

6nm Gate Length Ultra-Thin Channel pFETs

In a separate experiment using different process conditions we have fabricated extremely small gates on ultra-thin Si channels with thin gate dielectric and a strong halo implant condition. SEM cross-sections of devices with gate lengths of 6nm and 12nm and T_{Si}=4-8 nm are shown in Fig. 17. The pFET Ids-Vgs and Ids-Vds characteristics are shown in Fig. 18 and Fig. 19. The device can clearly be turned off even at these extremely small gate dimensions. However, the saturation current at Vdd= –1.5V is only 130μA/μm. The reduced current is likely to be caused by process-induced variations coupled with the ultra-thin Si layer in the channel and the source-drain extension regions. Specifically, mobility degradation in the channel [11] and increased series resistance under the spacer may cause the reduced drive current. Another factor contributing to the low current drive is the high halo concentration in the channel leading to mobility degradation. However, this is the smallest transistor with good MOSFET characteristics ever reported. Fig. 12 compares this result with the 2001 version of International Technology Roadmap for Semiconductors (ITRS) [4] and recent published data [5-10].

Conclusion

We have shown that excellent SCE control can be achieved with ultra-thin Si channel devices. For the first time, high-performance ring-oscillators with gate lengths of 26nm are reported. The ultra-thin Si channel pFET with a gate length of 14nm is among the best reported to date for MOSFETs with these dimensions. In addition, functional transistors with gate-lengths down to 6nm have been demonstrated. These results suggest that aggressive SOI thickness scaling is a promising option to drive CMOS device scaling to its physical limit.

Acknowledgement

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Table 1: Process Flow

Oxidation and wet etch to thin SOI
Shallow Trench Isolation
Gate dielectric, EOT=1.2nm and 2.2nm
Gate stack deposition and patterning
Spacer Module
Extension implants and anneal
Raised source-drain, implant and anneal
$CoSi_2$ formation followed by BEOL

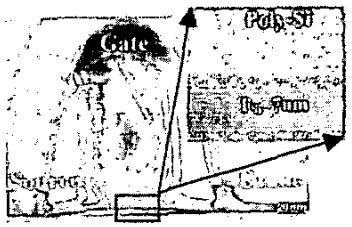

Fig. 1: TEM of an ultra-thin Si channel MOSFET

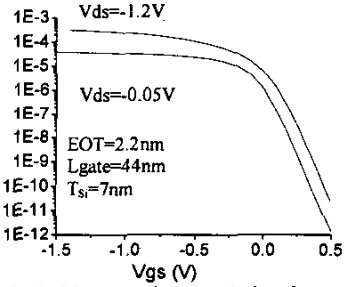

Fig.2: Ids-Vgs characteristic of a pFET with thick gate dielectric

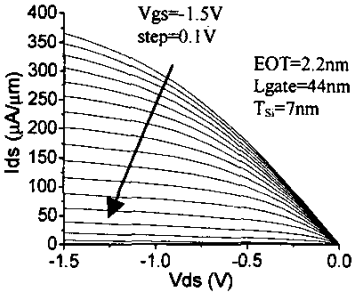

Fig.3: Ids-Vds characteristic of a pFET with thick gate dielectric

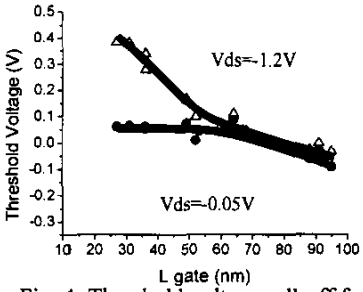

Fig. 4: Threshold voltage roll-off for pFETs with thick gate dielectric

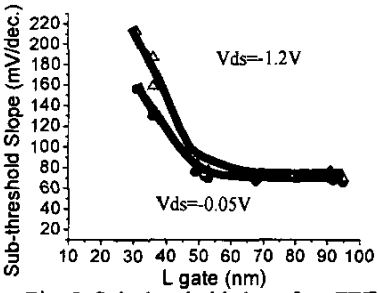

Fig. 5: Sub-threshold slope for pFETs with thick gate dielectric

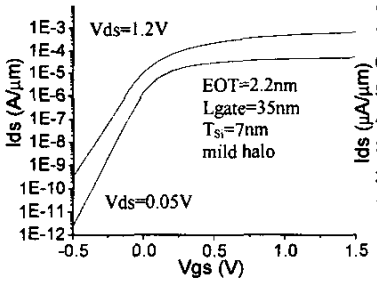

Fig.6: Ids-Vgs characteristic of an nFET with a mild halo

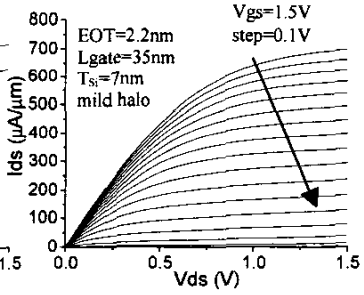

Fig. 7: Id-Vds characteristic of an nFET with a mild halo

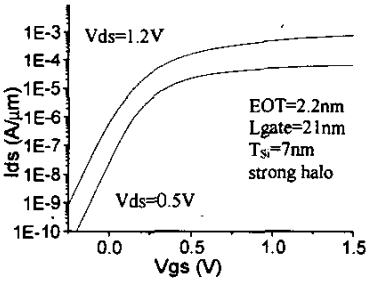

Fig. 8: Ids-Vgs characteristic of an nFET with a strong halo

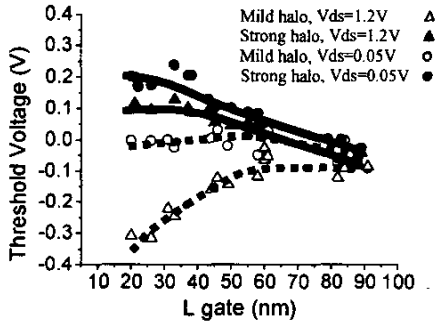

Fig.9: Threshold voltage roll-off for nFETs with thick gate dielectric and different halos

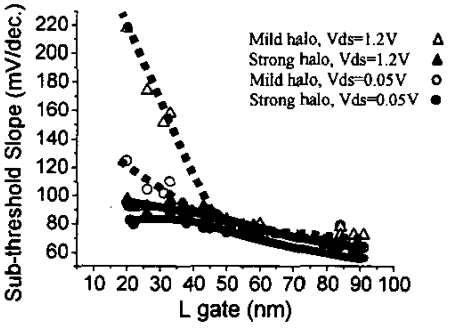

Fig.10: Sub-threshold slope for nFETs with thick gate dielectric and different halos

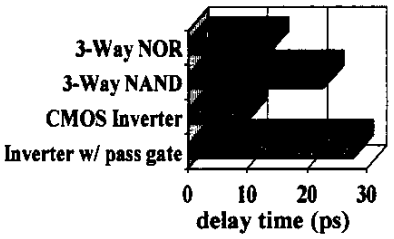

Fig.11: 26nm gate length CMOS ring-oscillator delays

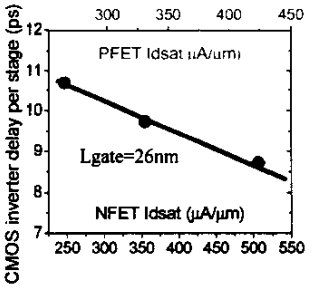

Fig.12: 26nm gate length CMOS inverter delays vs. Idsat

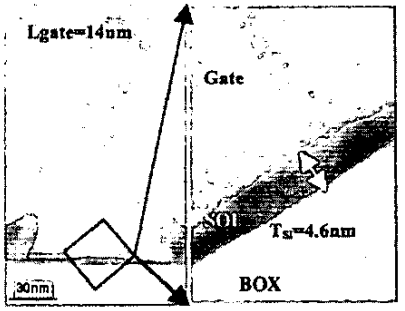

Fig.13: TEM cross section of a pFET with Lgate=14nm and T_{Si}=4.6nm

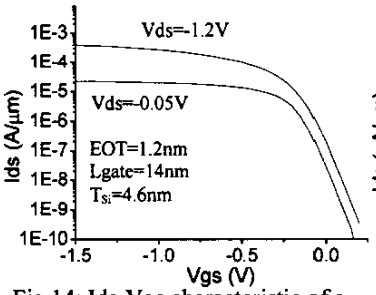

Fig.14: Ids-Vgs characteristic of a pFET with thin gate dielectric

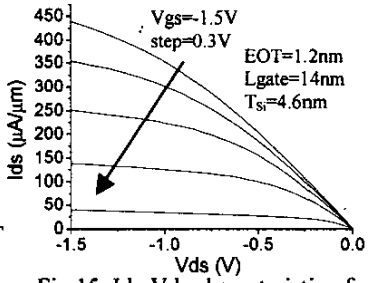

Fig.15: Ids-Vds characteristic of a pFET with thin gate dielectric

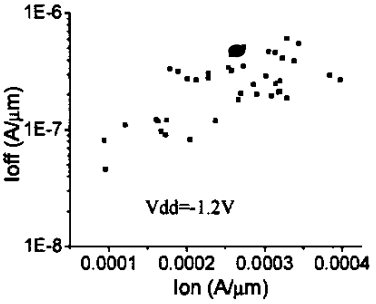

Fig.16: Ion-Ioff characteristic of pFETs with thin gate dielectric

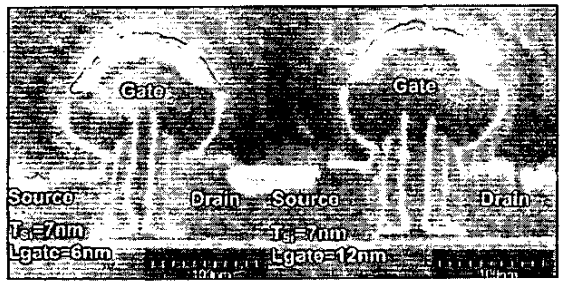

Fig.17: SEM cross-section of ultra-thin silicon channel pFETs with 6nm and 12nm gate lengths

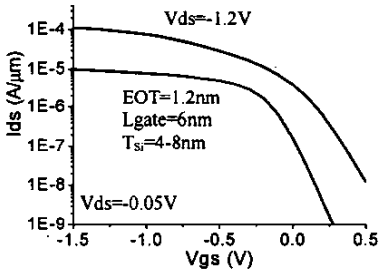

Fig.18: Ids-Vgs characteristic of a 6nm pFET

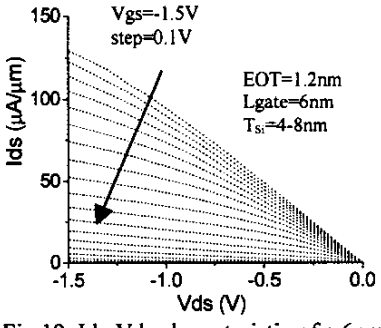

Fig.19: Ids-Vds characteristic of a 6nm pFET

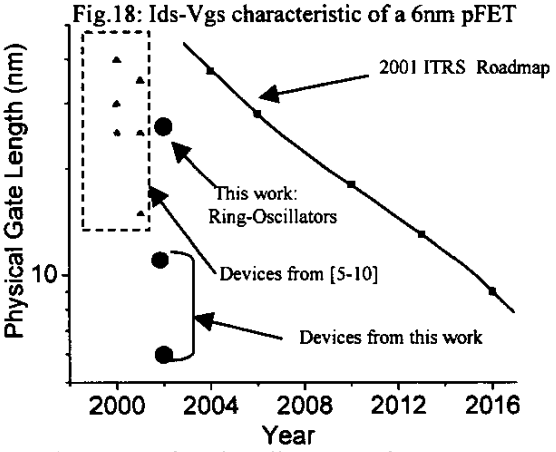

Fig.20: Gate-length scaling comparison