An approach to lifetime estimation of SiC MOSFETs subjected to thermal stress

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Abstract

The ever increasing throughput and demand for faster motion control in the industry require power electronics with higher power densities and increased bandwidths are required to control the mechanical components. The Silicon-Carbide (SiC) MOSFET contains significant improvements over the traditional Silicon (Si) MOSFET and is a promising key component to overcome these challenges. The improved properties of SiC MOSFETs over Si MOSFETs suggest that switching frequencies and load currents can be higher. Also for SiC MOSFETs holds that repetitive load profiles result in cyclic junction temperatures which cause considerable thermal stress inside the MOSFET package. In this paper a thermo-electrical model is developed to determine the limiting repetitive power dissipation profiles. On basis of the simulation results a measurement setup is dimensioned and used to determine the lifetime of SiC MOSFETs at defined thermal cycling profiles. The research is focused on the test method and the strategy to verify the test parameter values such as junction temperature estimation. Initial measurements are performed with a Proof Of Concept (POC) test setup.

1. Introduction

The continuing trend of increasing productivity in several industries often require faster motion of electromechanical systems. The actuators require more electric power to perform faster movements and higher bandwidths for accurate motion control. Power converters with higher output power and higher switching frequencies are required to meet these requirements.
The Silicon-Carbide (SiC) MOSFET is a promising new type of high-voltage power switch which has, in general, a decreased on-resistance $(R_{DS(on)})$ with respect to the traditional high-voltage (HV) Silicon (Si) MOSFETs. The lower gate-capacitance of SiC MOSFETs with respect to Si MOSFETs make the SiC MOSFETs also suitable to operate at higher switching frequencies. Besides higher throughput, reliability of industrial machines is at least as important. Nowadays, in case of failure of a high-voltage power-converter, the main cause is a failure of in the power switches.
The lifetime of HV power MOSFETs is, in general, limited by a Single-Event Burnout (SEB) due to cosmic radiation[1] or degradation of electrical and mechanical interconnects such as solder joints, wire bonds and the die attach. The higher bandgap of SiC results in lower susceptibility to SEB.
Degradation of of MOSFETs is mainly induced by thermomechanical stress occurring at these interfaces due to the mismatch of thermal expansion and the corresponding temperature excursion during operation.
In practice, the failure in power switches is caused by fast power cycling which thermally cycles

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the junction temperature. For this reason this article focuses on fast power cycling tests and the corresponding failure modes which typically are solder fatigue, wire bond lift-off and wire bond heel cracking. Most research literature in this field contains approaches to lifetime estimation by means of tests on IGBT modules [2],[3],[4],[5].
This research paper describes an approach to apply lifetime tests on Silicon-Carbide (SiC) MOSFETs by subjecting these devices to a relatively high-frequent thermal cycling profile induced by load cycling. Lifetime testing methods for IGBTs are used as a basis [2],[3],[4],[5]. The useful-lifetime estimation of SiC MOSFETs is obtained by accelerated power-cycling tests to reduce the testing time to a reasonable level. This is implemented by a Proof Of Concept measurement setup.

2. Test Method

2.1. Junction Temperature Cycling

The lifetime of SiC MOSFETs subjected to thermal stress is determined by means of destructive accelerated lifetime tests. Thermal stress consists of two components: the peak-to-peak junction temperature swing ΔT_j, and the average junction temperature $T_{j,avg}$. Accelerated lifetime tests are performed by heating and cooling of the junction. The junction of the MOSFET is heated by a load current, and cooled by the heatsink on which the MOSFET is mounted. To obtain a condition that is closest to the practical load conditions, the MOSFET is, as in its application, operating in triode operation during the load cycle. The number of load-cycles to failure is indicated by N_f. For example a 5% increase of the initial $R_{DS(on)}$ is defined as a failure ($R_{DS(on)} > 1.05 \cdot R_{DS(on,initial)}$).
The temperature profile is based on previous research projects [4], [5] and [2]. Smaller maximum temperature swings result in longer testing times while much larger temperature swings exceed the specified maximum junction temperature of the MOSFET ($150°C$) in case the test is running at room temperature ($25°$C). This may result in destructive side-effects which have to be avoided. The target for the junction temperature swing ΔT_j is set to $100K$ to obtain relative short testing times to find initial results quickly. Tests with smaller temperature cycles are performed for extrapolation to the value of ΔT_j for which the required 2 billion load cycles are met. ($N_f = 2 \cdot 10^9$).
The research is focused on a commercial available $80m\Omega$ SiC MOSFET with a TO-247 package. The following assumptions are made for this research:

- Lifetime tests are performed on the predefined SiC MOSFET type
- The load cycle frequency of the use case is approximately 13Hz
- Obtained lifetime measurement results are extrapolated

2.2. Thermal Cycling Response

The thermal response of the MOSFET is depicted in Fig. 1(a). The $Z_{th(JC)}$ is a 14^{th} order model which is supplied by the MOSFET manufacturer. The junction temperature is cycled by means of power dissipation in the junction which is applied at a frequency of 13Hz. An estimation of the required power dissipation and duty cycle of the load cycle is obtained by means of a developed simulation.
The power dissipation in the junction is assumed to be a rectangular pulse with a duty-cycle δ. To obtain the steady-state junction temperature cycle, the calculations are performed in the

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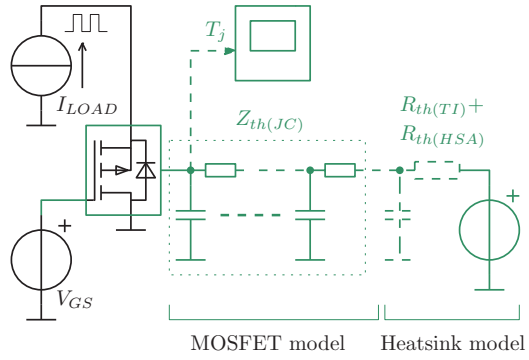
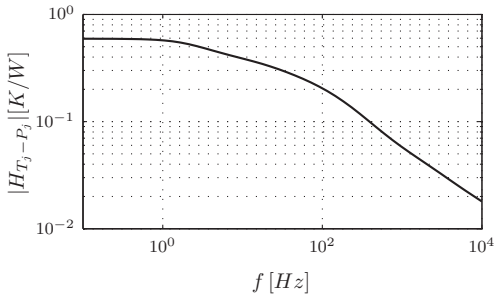
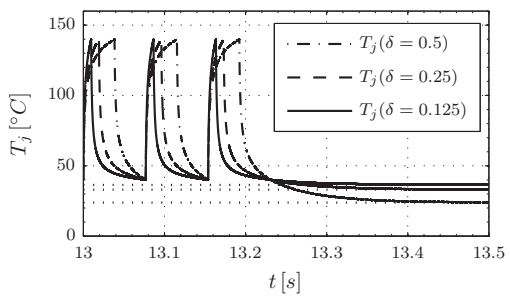


(a) Thermal model of the DUT

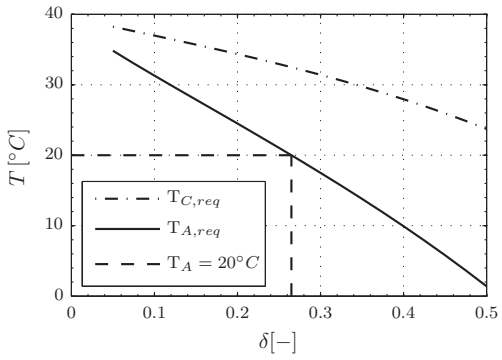


(b) Thermal response of the junction on applied power dissipation

Fig. 1: Thermal behavior of the DUT



(a) Time response of junction temperature at different duty-cycles, $\Delta T_j = 100K$, $T_{j,max} = 140°C$



(b) Required case and ambient temperature $T_{C,req}$ and $T_{A,req}$ to obtain $\Delta T_j = 100K$, $T_{j,max)} = 140°C$ versus δ

Fig. 2: Thermal responses of the DUT

frequency domain, and transformed back to the time domain.
A Cauer based model is converted via a state-space notation to a transfer function. The magnitude of the transfer function is shown in Fig. 1(b).

$$H_{Pj-Tj}(j\omega) = C(j\omega I - A)B + D \tag{1}$$

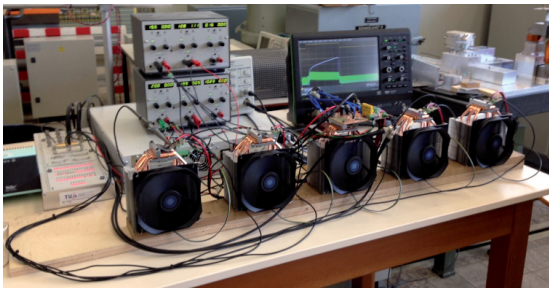
The applied rectangular shaped power pulse $p_j(t)$ can be described by (2).

$$p_j(t) = P_j \sum_{n=-\infty}^{+\infty} \mathrm{rect}\left(\frac{t+nT}{\frac{1}{2}\delta T}\right) \Rightarrow \mathcal{F}\left\{\sum_{n=-\infty}^{+\infty} \mathrm{rect}\left(\frac{t+nT}{\frac{1}{2}\delta T}\right)\right\}_k \text{ where } \mathrm{rect}\,(x) = \begin{cases} 1 & \text{if } |x| \leq \frac{1}{2} \\ 0 & \text{if } |x| > \frac{1}{2} \end{cases} \tag{2}$$

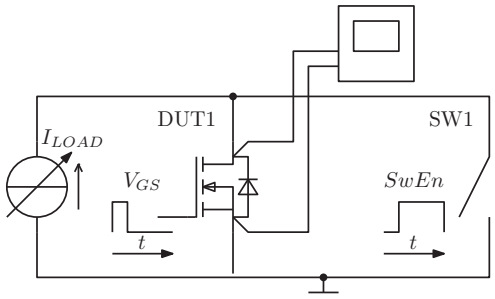
Combining both equations and back-transformation to the time domain results in 3. As described in section 2.1 the target for ΔT_j is set to $100K$. The required power dissipation P_j for a given duty cycle can be obtained by means of (3).

$$P_j(\delta) = \frac{\Delta T_j}{\sum_{k=-\infty}^{+\infty} c_{rect,k} \cdot 2j \cdot \sin(k\pi\delta) \cdot H_{Pj\to Tj}(jk2\pi\frac{1}{T})} \tag{3}$$

The junction temperature over time is plotted in Fig. 2(a) for multiple duty cycles, with corresponding $P_j(\delta)$ to obtain the desired temperature cycle. As described in section 2.1 the



(a) POC measurement setup



(b) POC topology

Fig. 3: Proof Of Concept measurement setup

maximum junction temperature target $T_{j,max,req}$ is set to $140°C$. The first three cycles represent the steady-state time response of the junction temperature. The time response after these cycles indicate the time response of the junction after switching-off the load. The junction cools down to the case temperature T_C. The dotted lines indicate the required value for T_C.
The relation between the case temperature T_C and the ambient temperature T_A is given by (4)

$$T_A = T_C - P_{j,avg} \cdot R_{th,CA}, \tag{4}$$

where $R_{th,CA}$ is equal to the sum of the thermal resistance of the thermal interface material between the MOSFET case and the heatsink $R_{th,TI}$, and the thermal resistance of the heatsink to ambient $R_{th,HSA}$. The parameter $R_{th,CA}$ is assumed to be $0.2K/W$, which is based on an active air-cooled heatsink with manageable dimensions and the use of proper thermal paste. Based on this value for $R_{th,CA}$ the required ambient temperature $T_{A,req}$ is plotted versus the duty-cycle in Fig. 2(b). The required case temperature $T_{C,req}$ is also plotted in this figure as an indication. The dashed line indicates the the practical ambient temperature. It can be concluded that a $\delta = 0.25$ is the highest possible duty-cycle for testing outside a cooled climate chamber which is desired for long term testing. A δ of 0.25 is chosen because a division factor of four is practical for testing multiple MOSFETs at once. Much lower duty-cycles are not representative for the concerning practical application.
The power dissipation P_j of the MOSFET, operating in its on-state with a gate-source voltage V_{GS} of $20.0V$, is equal to

$$P_j = i_D^2 \cdot R_{DS(on)}. \tag{5}$$

In practice $R_{DS(on)}$ depends both on T_j and I_D, so finding the desired setpoint for $T_j(t)$ requires some adjustments of the current source and the cooling. This is described in section 3

3. Proof Of Concept

A Proof Of Concept (POC) is built to verify the simulation results, obtain indicative lifetime measurements and determine which load currents are required to obtain the desired temperature profiles of the junction. The POC measurement setup is shown in Fig. 3(a).

3.1. POC topology

The POC is kept as simple as possible, so only one DUT can be tested and monitored at once. Fig. 3(b) depicts the topology of the POC setup. Fig. 4 shows the load cycle pattern of the DUT and the control signals of SW1.

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The junction temperature T_j of DUT1 is cycled by applying load cycles with $\delta = 0.25$. The load current I_{LOAD} is generated by a high-impedant current source which is configurable by the user. The parameters V_{DS} and I_D are measured to determine $R_{DS(on)}$ which is used to estimate the actual T_j. The parameters V_{DS} and I_D are measured by means of an oscilloscope. Estimation of T_j is defined in section 3.2.

3.2. Junction Temperature Estimation

The main goal of the lifetime tests is to obtain lifetime information in terms of number of cycles to failure (N_f) versus the temperature swing of the junction ΔT_j. To obtain reliable data it is important to perform lifetime tests with a correct junction temperature swing. For this reason it is required to measure the actual junction temperature to verify the thermal swing. Multiple estimation strategies are evaluated on accuracy, practical applicability, and implementation.

Measurement of the junction temperature from outside the MOSFET by means of thermocouples is complex and inaccurate. For this reason Thermo Sensitive Electric Parameters of the MOSFET have been used to determine the actual junction temperature. Junction temperature estimation by the parameters $R_{DS(on)}$, $V_{GS(th)}$, and V_{SD} are evaluated. For the POC the parameter $R_{DS(on)}$ is used to estimate T_j because of its simplicity. T_j estimation by measuring V_{SD} is suitable for future application to obtain redundant measurement results. The TSEP $V_{GS(th)}$ shows time-dependend behavior which makes it unsuitable for a straightforward junction temperature estimation.

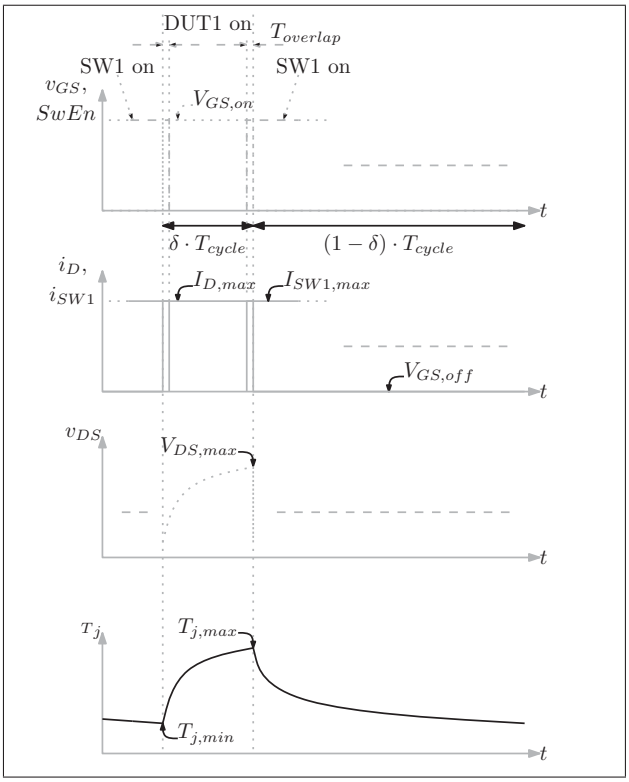

Fig. 4: POC load cycles in time

The $R_{DS(on)}$ depends on two parameters: the drain current I_D and the junction temperature T_j. This property of the MOSFET is used to estimate the junction temperature T_j. To estimate T_j it is required to measure the drain current I_D and determine the $R_{DS(on)}$. The $R_{DS(on)}$ is determined by simultaneously measuring the drain-source voltage V_{DS} and the drain current I_D at a defined gate-source voltage V_{GS}.

The typical values of $R_{DS(on)}$ are provided in the datasheet of the DUT. But verification by measurements has shown that these values are significantly lower in practice. Moreover, there is much spread of the $R_{DS(on)}$ values among different DUT samples. For this reason $R_{DS(on)}$ is characterised at $I_D = \{30.0, 32.5, 35.0, 37.5, 40\}A$, and $T_j = \{25, 50, 75, 100, 125, 140\}^\circ C$. Fig. 5(a) shows the $R_{DS(on)}$ of five different DUT samples at a drain current of $40A$. Interpolation of $R_{DS(on)}$ over the parameters I_D and T_j of a single DUT results in figure 5(b). Each physical DUT is characterised individually. This interpolated data is used to determine the junction temperature.

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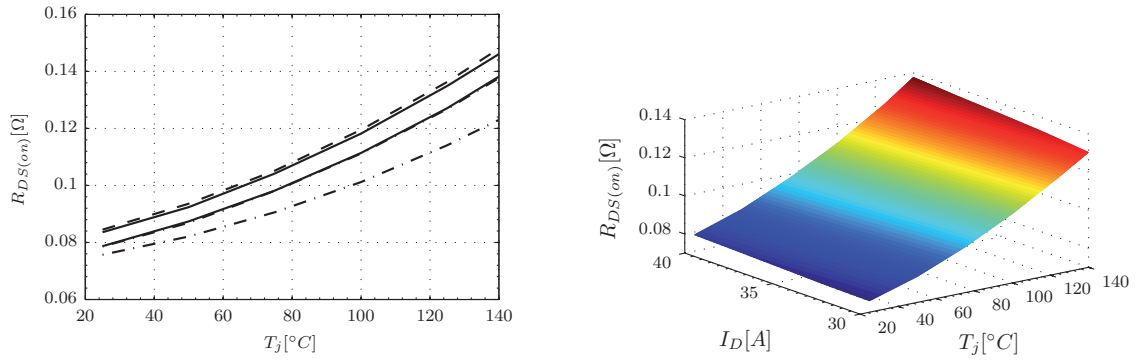

(a) $R_{DS(on)}$ versus T_j @ $I_D = 40A$ (measurements of five samples)

(b) $R_{DS(on)}$ versus I_D and T_j (one sample)

Fig. 5: $R_{DS(on)}$ characterisation results

3.3. POC Test Sequence

The lifetime tests are performed in the following sequence:

1. Adjust I_{LOAD} to obtain $\Delta T_j \approx 100K$
2. Adjust the DUT case temperature T_C by controlling the heatsink temperature T_{HS} to obtain a peak junction temperature $T_{j,max}$ of $140°C$ according to simulations in section 2.2
3. Determine $T_{j,avg}$
4. Keep running the test and count the number of cycles until $R_{DS(on)}$ increased by 5% of its initial value
5. Start a new test with a new DUT, adjust I_{LOAD} to obtain $\Delta T_j = 85K$
6. Adjust T_C of the DUT by controlling T_{HS} to obtain an equal $T_{j,avg}$ as obtained during step 3
7. Count the number of cycles to failure N_f until $R_{DS(on)}$ increased by 5% of its initial value
8. Repeat from step 5, but with $\Delta T_j = 70K$ and lower (in steps of $15K$) until the test time gets too long

3.4. POC Measurement Results

The initial test is performed with at $\Delta T_j = 100K$. After step 1 and 2 of the test sequence, described in section 3.3, the drain-source voltage is measured again. The result of this measurement is shown in figure 6(a). The yellow line indicates the gate-source voltage V_{GS}, the green line indicates the drain/load current of the DUT $I_D = I_{LOAD}$, and the cyan line indicates the drain source voltage V_{DS} during the load cycle. According to the measurement, the measured minimum and maximum drain-source voltages during a load cycle of $39.25A$ are equal to: $V_{DS,min} = 3.59V$ and $V_{DS,max} = 5.82V$. Since this MOSFET is characterized, the junction temperature can be estimated by means of a lookup table. An example of a lookup table is given in Fig. 5(b). The estimation results in a minimum junction temperature of $T_{j,min} = 41.5°C$ and a maximum junction temperature of $T_{j,max} = 141.0°C$. This is close to the targeted junction temperature profile as defined in step 1 of the test sequence.

It took 2 hours and 11 minutes until the $R_{DS(on)}$ increased with 5%. This means that the number of cycles to failure is equal to: $N_f = 102,180$. Fig. 6(b) shows the evolution of the drain-source voltage V_{DS} over the complete test duration. The image shows the parameter V_{DS} in infinite persistence which means that all triggered measurements are superimposed in

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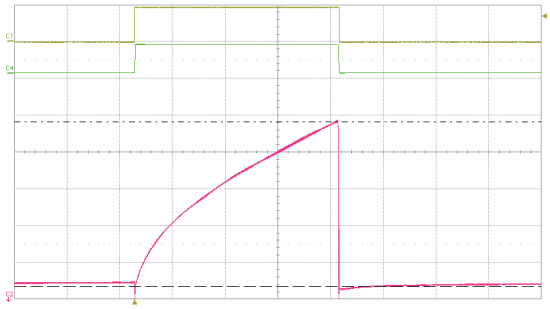
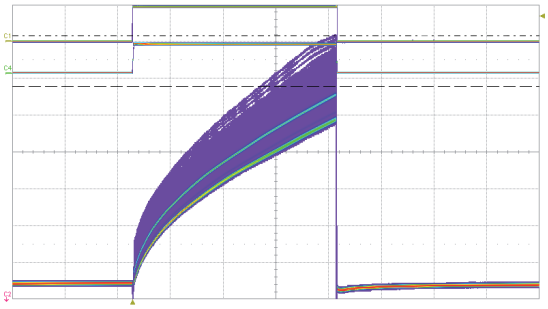


(a) Measured drain-source voltage V_{DS} during a load cycle



(b) Measured drain-source voltage V_{DS} during a load cycle (over entire DUT lifetime)

Fig. 6: Measured drain-source voltage V_{DS} during a load cycle

a single image. The resulted image is thus an average of all measurements where the color represents the number of samples at a certain position. Red colored lines or points represents many superimposed samples, yellow/green slightly less, and purple colored lines or points indicates that only a single or a few samples are superimposed. The trend of the V_{DS} increase and thus increase of $R_{DS(on)}$ during the lifetime test of DUTs show an initial degradation of around 5%, no further degradation for some period and subsequently fast further degradation to above 20%.

3.5. DUT degradation effects and Failure modes

Multiple degraded and defect DUTs are de-capped and analyzed. Images of the inner parts of the DUTs are taken by a Scanning Electron Microsope (SEM). Degraded DUTs contain some broken wire-bonds and cracks in some of the wire-bonds. The analyzed MOSFETs, including one completely broken MOSFET, contained a few wire-bonds without visible cracks. The broken MOSFET contained serious deformation of the metal lines on the junction around the wire-bonds which are not broken. This suggests that the initial degradation starts with wire-bond cracking and further degradation is occurred by the metal lines of the junction.

3.6. POC Lifetime Measurement Results

The results of the lifetime tests with different junction temperature swings are plotted in Fig. 7(a). The number of cycles to 5% increase in $R_{DS(on)}$ are indicated with crosses. The lifetime curve of a Si-based IGBT module [6] is plotted in Fig. 7(a) as an indication. The extrapolated lifetime of the MOSFET is also plotted in Fig. 7(a).
The estimated lifetime, based on this extrapolation, reaches the required $N_f = 2 \cdot 10^9$ cycles for a junction temperature cycle of slightly below $\Delta T_j = 20K$. A hypothesis for the logarithmic-logarithmic relation between the lifetime and temperature swing of the junction is a transition from plastic to elastic deformation of the elements inside the DUT. This hypothesis is supported by [7] and [8]. It has to be noted that the number of measurement points are very limited. Additional lifetime measurements, also at lower values for ΔT_j, have to be performed to prove whether the applied logarithmic-logarithmic extrapolation method is optimistic or realistic.

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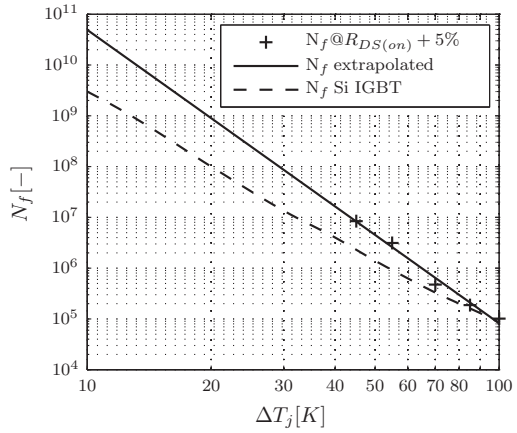
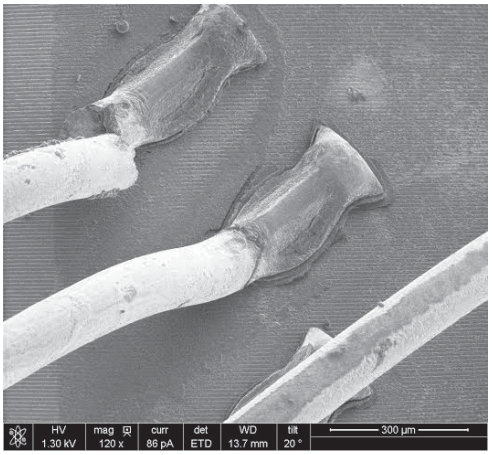


(a) MOSFET lifetime in cycles versus ΔT_j with extrapolations of measurements and an indicative lifetime curve of a Si-based IGBT module on a logarithmic-logarithmic scale



(b) Visualization of degradation effects inside the DUT by means of a Scanning Electron Microscope (SEM)

Fig. 7: POC lifetime measurement results and visualisation of the failure modes

4. Conclusion

Lifetime test methods of MOSFETs subjected to thermal stress are evaluated in this paper. Thermal stress is applied by thermal cycling of the junction temperature. Lifetime tests can be performed by means of a Proof Of Concept (POC) measurement setup with parameters dimensioned by means of a developed electrothermal model.
Lifetime tests require correct junction temperature estimation. Three estimation methods are evaluated. Junction temperature estimation by means of determination of $R_{DS(on)}$ is accurate and easy to implement. The required characterization of each DUT is a time consuming process which requires improvements.
The lifetime of a SiC MOSFET is measured by means of testing these DUTs at multiple levels of ΔT_j. Indicative lifetime figures are obtained and are extrapolated. According to a logarithmic-logarithmic extrapolation, the lifetime of $N_f = 2{\cdot}10^9$ cycles is met at around $\Delta T_j \leq 17K$. But the very limited number of measurements can result in relative large uncertainties for the lifetime estimation at low values for ΔT_j.

5. Future Work

Current measurements do not provide statistical relevance. Tests at defined (lower) levels of ΔT_j and $T_{j,avg}$ have to be performed on a larger number of DUTs to verify the hypothesis of elastic and plastic deformation of MOSFET component layers. A more mature test setup has to be integrated to be able to perform these tests and to perform the tests simultaneously on more than one DUT.
Estimation of T_j by means of determination of $R_{DS(on)}$ requires characterization of $R_{DS(on)}$ versus T_j and I_D which is a time consuming process. This step needs optimization, and automation is desired.
It is recommended to perform the same lifetime tests on Si-based power MOSFETs to be able to compare the lifetime figures of Si and SiC based MOSFETs with each other.

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