Application reliability validation of GaN power devices

Sandeep R. Bahl, Jungwoo Joh, Lixing Fu, Anup Sasikumar, Tathagata Chatterjee, Sameer Pendharkar
Texas Instruments, High Voltage Power Solutions and Analog Technology Development,
Santa Clara, CA, and Dallas TX, U.S.A, email: Sandeep.Bahl@ti.com

***Abstract*—** Standard qualification methodology or "qual" does not specify product-level testing due to the diverse range of products and use conditions, a limited ability for system-level acceleration, and complication from system-level failures. This is a concern for emerging power-management technologies, since the fundamental switching transitions are not covered. We show that hard-switching with the well-known double-pulse tester is predictive of device performance under system-level testing. It simplifies the problem of product reliability testing to one of a device and a tester. It enables us to detect devices that pass qual but perform poorly in application. As a result, our devices pass qual *and* perform well in application.

I. Introduction

The semiconductor industry takes the reliability of silicon transistors for granted. This is a result of mature qualification methodology [1] and longstanding technology experience. The stress tests, however, were developed more than twenty years ago, whereas technology and its uses have changed. For example, power conversion circuitry using hard-switched transistors is now much more widespread.

The qualification of power transistors is typically supplemented by running a smaller number of parts through more extensive validation and robustness tests. These consist of avalanche testing, the running of product, and SOA (Safe Operating Area) testing. Over the years, knowledge has also been gained regarding the robust design of devices, wafer-level reliability validation, and the correlation of device signatures to reliability, e.g. low-leakage and sharp avalanche [2] with fewer field failures of power supplies.

There is now tremendous interest in wide-bandgap semiconductors for power management applications. These materials have different failure modes than silicon power transistors. They also have different requirements, e.g. GaN FET robustness cannot be validated through avalanche testing. In addition, silicon-equivalent wafer-level lifetime tests e.g. HCL (Hot-Carrier Lifetime) are not yet developed. The above does not mean, however, that robust GaN transistors cannot be made; it just means that the validation needs to be done differently and for GaN-specific failures.

II. Background

A question typically asked is "what does "qual" mean?" More details are given in [3]. Briefly, traditional qualification represents about 9 yrs. of lifetime. Passing qual sets statistical confidence levels on FIT (Failure in Time) rate and defectivity. The statistics of zero fails out of 231 parts establish a FIT rate of about 50, and a LTPD (Lot Tolerant Percent Defective) value of one. These calculations, however, assume an activation energy of 0.7 eV, an accelerated-stress temperature of 125C, a use-temperature of 55C, and a stress condition representative of actual use. These assumptions fail for power FETs (including Si), since the typical-use junction temperature is about 100-110°C. If qualification is run at 150°C, then the non-accelerated time for use at 105°C is only 1.1 yrs. This assumes the Si effective activation energy of 0.7 eV, whereas for power GaN FETs the activation energy is different, with a wide range, from 0.1 eV to 1.84 eV [3]. Further, qual does not specify hard-switching, a key use-profile for power management applications.

GaN has shown robust operation under actual-use conditions, e.g. 40V devices in a buck converter [4], 600V devices in a boost converter [5] and 650V devices in a SEPIC (Single-Ended Primary-Inductor) converter [6]. The question arises as to how GaN would be qualified for end-applications. JEDEC does not prescribe conditions, citing the evolving applications and material sets in the semiconductor industry [7]. Application-relevant qualification needs the standard qualification testing extended for the failure modes of GaN with the addition of actual-use conditions. A high-level illustration listing relevant JEDEC literature is shown in Fig 1.

III. Application-relevant Testing

Our approach is to identify an application stress condition for power management applications. As described in [3], *hard-switching* meets this condition, and can be applied using the well-known double-pulse tester. This approach is in accordance with JEDEC guidelines: JESD226 takes such an approach for power amplifier modules (PAMs), and JESD94B recommends a test vehicle, since the actual product complexity may mask intrinsic failure mechanisms.

It is not difficult to see that hard-switching and off-state operation stress the device differently. Consider Fig. 2, which shows simulated hard-switching waveforms of the low-side FET turn-on transition in a 200V:400V boost converter with an inductor current of 5A. The figure illustrates that the peak switching drain current is 15A, about three times the inductor current and that the FET is simultaneously subjected to high currents and voltages. This condition generates both hot carrier and instantaneous thermal stress, for which the SOA needs to be robust for the intended lifetime. Further, large device arrays can experience current crowding due to non-uniform switching. Switching transients can also can introduce capacitive current into unwanted regions of the device. Hard-switching stress-testing ensures that devices are robust both to switching SOA and transients.

The double-pulse tester hard-switching test vehicle schematic is shown in Fig 3. It is widely used for the characterization of switching dynamics, and is essentially a

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boost converter with the output tied to the input. It is also in use by others for the hard-switching robustness testing of GaN [8]. Fig. 4 shows the turn-on I-V loci of the boost-converter of Fig. 2 and the hard-switching test vehicle of Fig. 3, showing not only the relevance of the switching-stress profile, but also the ability to provide both voltage and current acceleration. It can also enable lifetime predictions by device stress at different conditions.

While likely not the only test vehicle, this can readily provide information on the two main GaN failure modes: hard-switching robustness and dynamic Rds-on (dRon) degradation. Poor robustness is easy to detect – the device simply fails catastrophically. dRon degradation is difficult to measure, since it recovers in microseconds [9]. This characteristic makes it necessary to monitor dRon in-situ, e.g. by use of a clamp circuit [10].

We have run accelerated tests on multiple GaN devices in the hard-switching test vehicle. Tests were run at Vds=480V, 10-15A inductor current, and a case temperature of 150°C. The turn-on pulses are short, therefore the stress test is essentially HTRB (High Temperature Reverse Bias) with hard-switching. This is a harsh test condition. The test vehicle detects GaN-specific failures of both dRon degradation and poor robustness, as evidenced by devices from non-optimized processes (Fig. 5). The testing shows that many devices have an increase in dRon followed by a recovery. This phenomena may not be detected by conventional methods. It is important to emphasize that these types of devices pass HTRB qualification testing. In contrast devices from an optimized process are stable, as shown in Fig. 6. The validation of dRon stability with stress is important, since hot-electron stress can cause an increase in the trap density [11].

For broad power management use, GaN must also be robust for soft-switching. Hard-switching is more stressful than soft-switching due to the high I*V overlap. This is shown by both Figs. 7 and 8. Fig. 7 shows that for hard-switching, both dRon degradation and robustness failure modes are accelerated with voltage, and Fig. 8 shows that hard-switching is more stressful than soft-switching. We used devices from a non-optimum process to demonstrate this, since devices from an optimized process are stable. Measurements were done on neighboring devices on the same wafer using an on-wafer pulsing system [12]. We had previously found that soft-switching caused more dRon degration than hard-switching. This is attributed to poor native (off-state bias induced) dRon, with the recovery due to holes generated by hard-switching. A better device is one in which the native dRon is good without relying on holes, as shown by our present results.

The dRon degradation is similar for HTRB and soft-switching, implying that they are both governed by "native" dRon. dRon was monitored during HTRB using the schematic in Fig. 9 and soft-switching conducted using the setup in [12]. The results are shown in Fig. 10. Devices (same non-optimum process) show similar dRon degradation profiles. This is noteworthy, since dRon during HTRB was measured once per minute, whereas the soft-switching rate was 1KHz, an increase of 60,000. From a robustness perspective, it means that passing both HTRB and hard-switching testing addresses the risk of application use (Fig. 11). It also shows that HTRB alone does not capture the impact of hard-switching.

Finally, it is important to know that devices from processes that pass qual but were judged "bad" by hard-switching testing perform poorly in application and vice versa. System-level testing was done using half-bridge EVM cards (Fig. 12). The results are shown in Fig. 13 for devices from three processes: A=bad, B=better, and C=good. "Bad" devices fail by rapidly heating up and over-temperature faulting due to high loss from rapidly increasing dRon. Improved devices have higher power loss as dRon increases with stress, but stabilize as dRon peaks and starts to recover. Good devices are stable. This shows that hard-switching testing while monitoring dRon is a good predictor of system-level reliability and is necessary to ensure good application performance.

IV. CONCLUSION

Hard-switching forms the fundamental switching transition for power management and is not specified by standard qualification testing. By using the familiar double-pulse test vehicle, we are able to administer hard-switching stress to GaN devices and monitor both dynamic Rds-on and robustness failure modes. The test is predictive of performance under system-level testing. It addresses the gap in standard qualification testing because it detects devices that pass qual but perform poorly in application.

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REFERENCES

[1] JEDEC standard JESD47I and AEC standards Q100 and Q101

[2] K. Shenai, M. Dudley, R. F. Davis, "Rugged Electrical Power Switching in Semiconductors: a Systems Approach", *Proceedings of the IEEE*, p.35, 2013.

[3] S. R. Bahl, D. Ruiz, D. S. Lee, "Product-level Reliability of GaN Devices" *IEEE International Reliability Physics Symposium (IRPS)* p.4A-3, 2016 (Invited paper).

[4] B. Rhea, L. Jenkins, F. Werner, W. E. Abell, R. N. Dean, "Two Year Reliability Validation of GaN Power Semiconductors in Low Voltage Power Electronics Applications," *IEEE Wide Bandgap Power Devices and Applications* (WiPDA), p.206, 2015.

[5] Y.-F. Wu, J. Guerrero, J. McKay, K. Smith, "Advances in Reliability and Operation Space of High-voltage GaN Power Devices on Si Substrates", *IEEE Wide Bandgap Power Devices and Applications* (WiPDA), p.30, 2014.

[6] D. C. Sheridan *et. al*., "Ultra-low loss 600V – 1200V GaN Power Transistors for High Efficiency Applications", *PCIM Europe*, p.318, 2014.

[7] JEDEC Standard JESD94B, "Application Specific Qualification Using Knowledge Based Test Methodology," Oct. 2015

[8] S. Kaneko et. al., "Current-collapse-free Operations up to 850 V by GaN-GIT utilizing Hole Injection from Drain", Proceedings of the 27th International Symposium on Power Semiconductor Devices & IC's (ISPSD), p. 41, 2015.

[9] J. Bocker *et. al*., "Experimental Analysis and Modeling of GaN Normally-off HFETs with Trapping Effects," *17th European Conference on Power Electronics and Applications*, 2015

[10] N. Badawi and S. Dieckerhoff, "A new method for dynamic Ron extraction of GaN power HEMTs,", *PCIM Europe*, p1010, 2015

[11] A. Sozza, et al., "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," International Electron Devices Meeting (IEDM), p. 590, 2005.

[12] Current Collapse in GaN Heterojunction Field Effect Transistors for High-voltage Switching Applications, J. Joh, N. Tipirneni, S. Pendharkar, S. Krishnan, "*IEEE International Reliability Physics Symposium (IRPS)* p.6C.5.1, 2014.

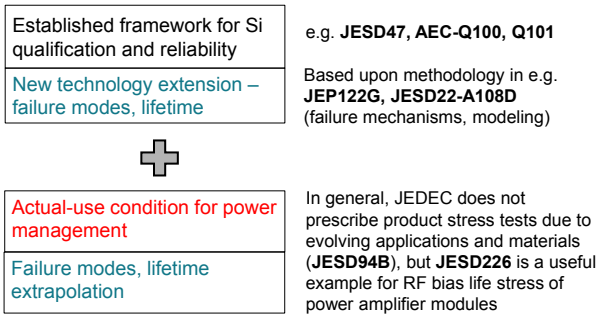

Fig. 1. A qualification framework for new technologies, listing relevant JEDEC literature. New technology qualification needs a knowledge-based approach to discover and model new failure modes, and also stress conditions relevant to use conditions.

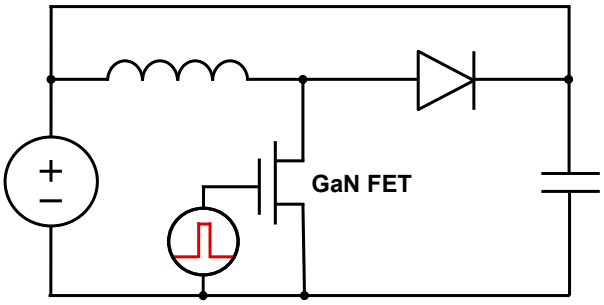

Fig. 3. Schematic of the hard-switching test vehicle. The test is run with short turn-on pulses. The short turn-on pulse adds the hard-switching transition to an HTRB stress without adding excessive self-heating from conduction loss if dRon increases. This allows independent monitoring of both dRon and robustness failure modes.

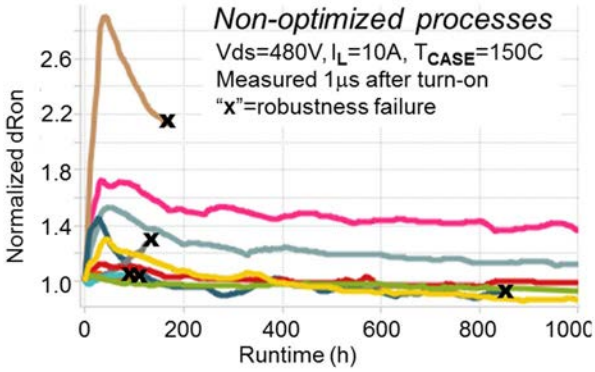

Fig. 5. dRon evolution with accelerated stress for devices from non-optimum processes (including processes "A" and "B" of Fig. 13) showing that the hard-switching vehicle (Fig. 3) can discriminate between good (see Fig. 6) and bad devices for both dRon and device robustness. Devices from these processes pass HTRB qualification testing. Discovery of the dRon peak and recovery was facilitated by minimizing conduction-loss self-heating with short turn-on pulses.

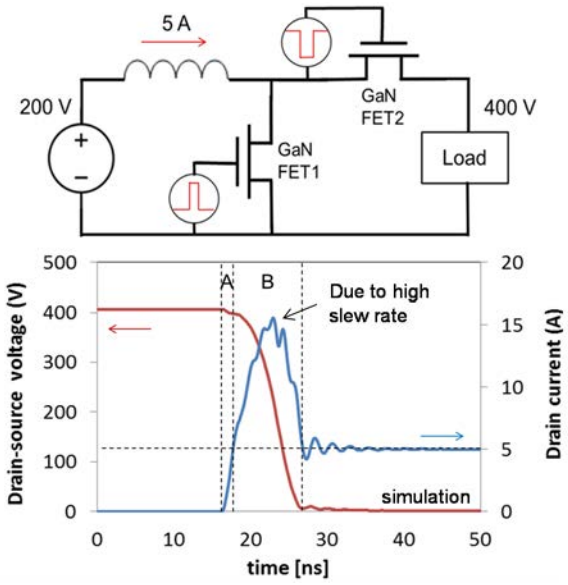

Fig. 2: Boost converter schematic and turn-on waveform for the low-side FET, showing that hard-switching has high I-V overlap. In region *A*, the drain current ramps up to the inductor current at full voltage. In region *B*, it exceeds the inductor current due to the capacitance at the switched node.

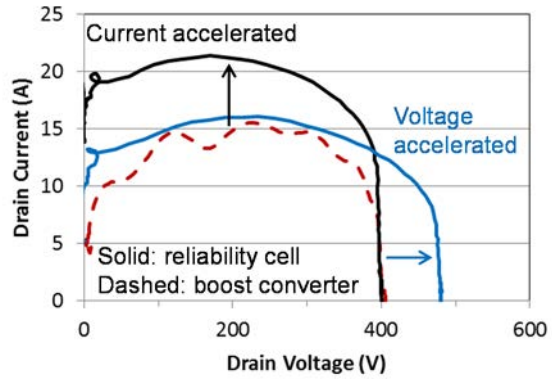

Fig. 4. I-V locus showing voltage and current acceleration capability. The boost converter is simulated and the reliability cell data is measured.

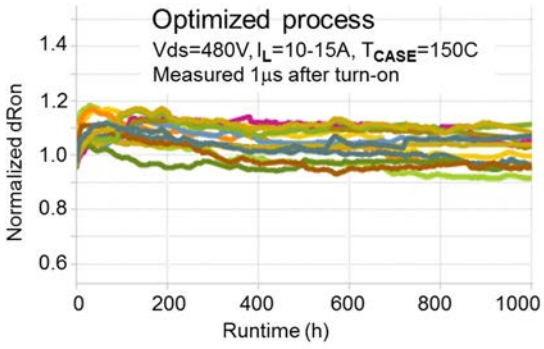

Fig. 6. Dynamic Rds-on measured in-situ at 150°C in the hard-switching test vehicle (Fig. 3) under accelerated stress, showing that devices from an optimized process are stable.

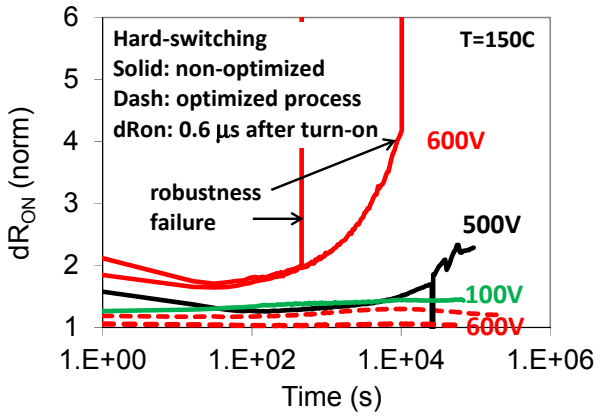

Fig. 7. Hard-switching stress-test on neighboring die using an on-wafer setup. Higher voltage causes more degradation in dRon and quickly results in robustness failure. We used devices from a non-optimized process to show the effect, since devices from an optimized process are stable (dashed line).

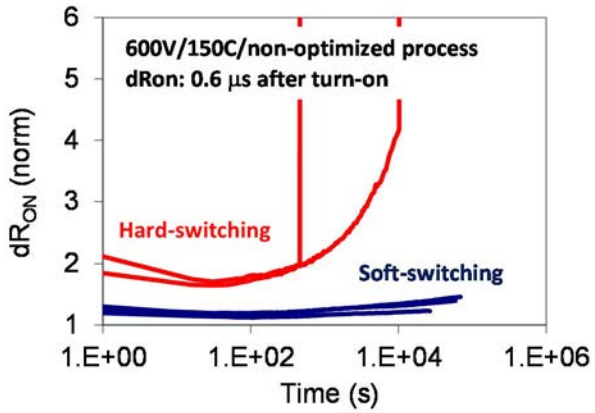

Fig. 8. Comparison of hard and soft-switching using neighboring die on the same wafer using an on-wafer pulsing setup. The data shows that hard-switching is more stressful than soft-switching, causing both higher dRon and catastrophic device failure modes. Device from an optimized process show good hard-switching robustness and stable dynamic Rds-on as shown in Fig. 7.

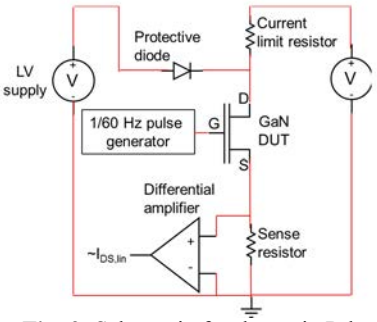

Fig. 9. Schematic for dynamic Rds-on measurements during HTRB.

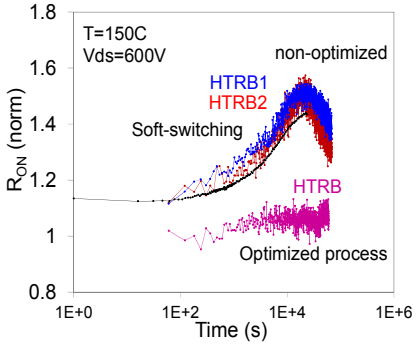

Fig. 10. Comparison of soft-switching (1 kHz) dRon, to that measured using HTRB (1/60 Hz). HTRB and soft-switching provide similar types of stress for dRon degradation. Hard-switching, however, is needed to detect poor robustness

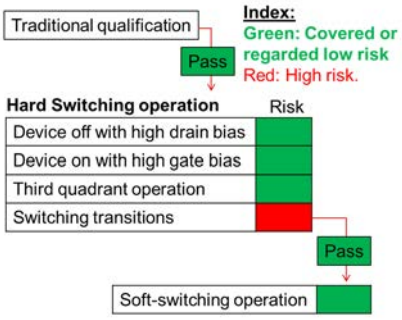

Fig. 11.Ttraditional qualification does not address hard-switching risk. Passing both HTRB and hard-switching testing addresses the risk of application use for both hard and soft-switching.

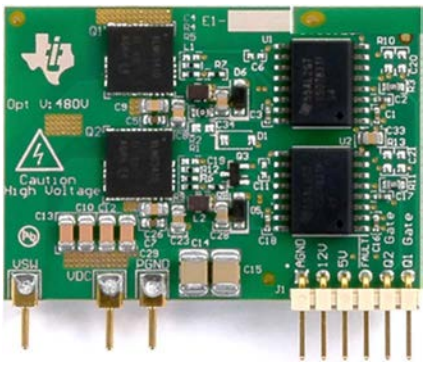

Fig. 12. EVM half-bridge daughtercard. The two TI GaN MCM's (GaN+Si IC) are the 8x8 QFN's towards the left. The parts have overcurrent, over-temperature and UVLO safety protection.

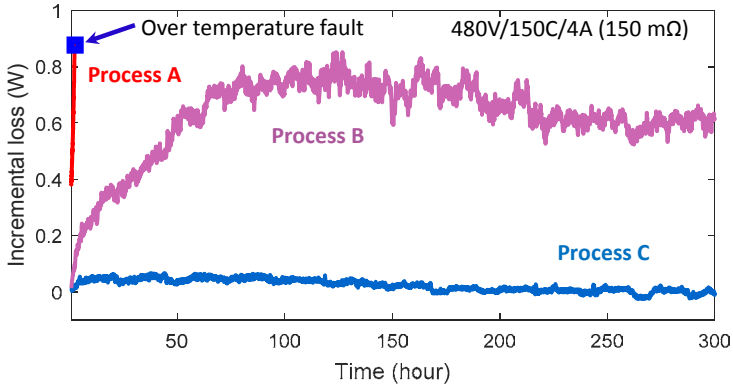

Fig. 13. Half-bridge EVM cards with GaN MCM's run at 480V/150C. Process A showed a high-dRon peak in the hard-switching test vehicle, which causes rapid heating and faulting during system-level testing. Process B was improved, and the device continues past the dRon peak. Process C is stable. This shows that the hard-switching test result is predictive of system-level operation. Since these processes pass qual, hard-switching testing (e.g. Fig. 3) is needed.