Application-relevant Qualification of Emerging Semiconductor Power Devices

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Motivation

- The power electronics industry is conservative, and customers need to be convinced of good reliability with low probability of field-returns
- Customers are not convinced that existing qualification standards for silicon assure the above for emerging technologies
- This presentation outlines and addresses the major gap in the application-relevant qualification of emerging power semiconductor devices
- The goal is to encourage industry collaboration, to develop reliability qualification testing that can predict actual-use lifetime
- Establishing credible methodology will address customer worries of reliability. This is essential for widespread adoption, benefiting all the players

What does JEDEC Qual mean for Si?

1. **Parts were tested for an accelerated 10-years at maximum bias[1]**
   - 1000h at Tj=125C → 8.9 yrs. at Tj=55C (E_A=0.7 eV)
   - Historically biased at 80% of min. BV e.g. 480V for a discrete 600V part[2]. Changing to 100% of max. recommended Vds going forward.
2. **Testing is representative of actual-usage**
   - HTRB/HTGB/HTOL may not represent actual-use conditions, but confidence has been built as a result of extensive experience
3. **There will not be many field-returns.**
   - Zero fails/231 parts (3x77) gives LTPD*=1
   - LTPD=1 means that if you sell a million parts, you can be 90% confident that you will get less than 10,000 part failures in 8.9 yrs.
   - 0/231 also gives a maximum FIT rate of 50.8, which means that less than 4450 fails in 10 yrs from a million parts (60% confidence)
   - In practice, multiple quals have already been run on mature processes, allowing lower statistical FIT rate predictions

*LTPD=Lot Tolerant Percent Defective

1. JEDEC and AEC standards JESD47, AEC-Q100, Q101. The lifetime actually extrapolates to 8.9 yrs.
2. The 80% criteria is traced to a prior revision of AEC-Q101 (Rev C, 2005). The latest version (Rev D1, 2013) specifies qualification at the maximum rated DC reverse voltage

What does JEDEC qual mean for a power technology?

1. **Parts were tested for an accelerated 10-years at maximum bias?**
   - Use temperature is > 55C, typically 100C
   - E_A/acceleration/root causes may not be established
     - 1000h at Tj=150C → 1.5 yrs. at Tj=100C (E_A=0.7 eV)
     - Need E_A of at least 1.18 eV to extrapolate to 8.9 yrs*.
2. **Testing is representative of actual-usage?**
   - HTRB and HTGB are field-equivalent tests. They may not be proxy tests for hard-switching, which is very different
   - When JEDEC qual was established in the early 1990's, the testing was predictive of the use-case then

   → *JEDEC qual does not have a hard-switching test*
3. **There will not be many field-returns?**
   - How would one establish this, since JEDEC testing is not representative of actual usage?

   → *Need to collect large numbers of actual-use device hours*

*the reader will realize that these calculations also apply to power Si devices

Standard qualification tests

e.g. for commercial devices

Type	Test	Description	Condition
Device	HTRB*	High Temperature Reverse Bias	1000h
	HTGB*	High Temperature Gate Bias	1000h
	HTOL	High Temperature Operating Life	1000h
	LU	Latch-up	(per JESD78)
	ED	Electrical Characterization.	Datasheet
Package	IOL*	Intermittent operating life	15k cycles
	AC	Unbiased autoclave 121C/100%RH	96 Hours
	HAST	Biased HAST, 130C/85%RH	96 Hours
	HTS	High Temperature Storage	150C/1000h
	TC	Temperature Cycle, -65/150C	500 Cycles
ESD	HBM	ESD - Human Body Model	1000V
	CDM	ESD - Charged Device Model	250V

Static stress

Dynamic or static stress

***for discrete devices**

Hard-switching is fundamental to power management
HTOL does not cover a hard-switched mission profile

New technology qualification methodology

Established framework for Si qualification
Technology-specific failure criteria, e.g. dynamic Rds-on for GaN, Vt shift for SiC MOS
Activation energies and acceleration factors

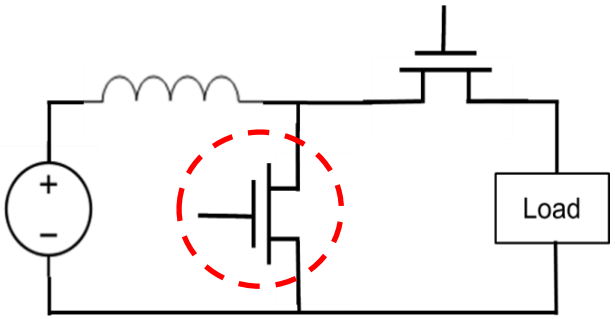
e.g. JESD47, AEC-Q100, Q101

Based upon methodology in e.g. JESD22-A108D and JEP122G

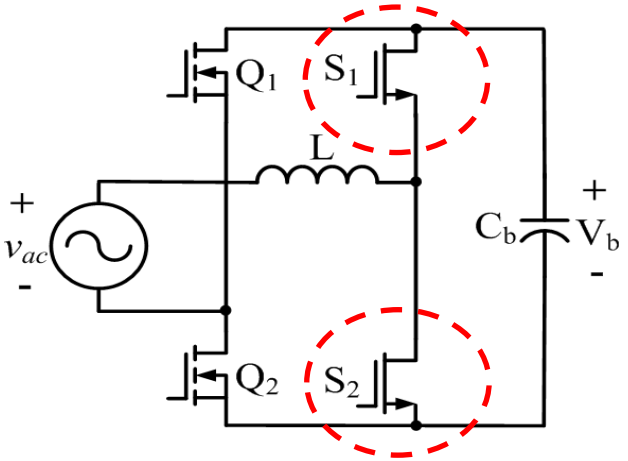
Actual-use mission profile for power management
Technology-specific failure criteria
Activation energies and acceleration factors

JESD94A: Application-specific qualification using knowledge-based test methodology
JESD 226 shows an application relevant example: RF bias life stress (RFBL) for power amplifier modules

Hard-switching is fundamental to power management

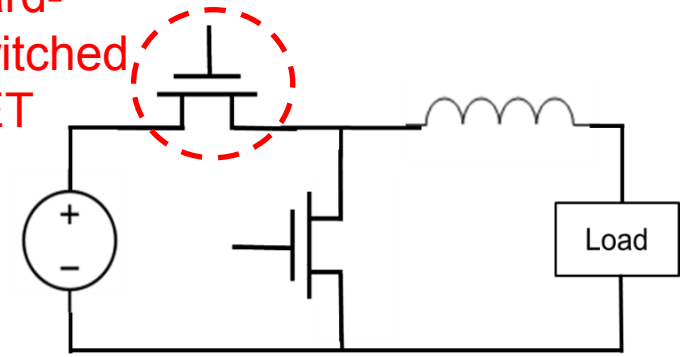


Boost converter

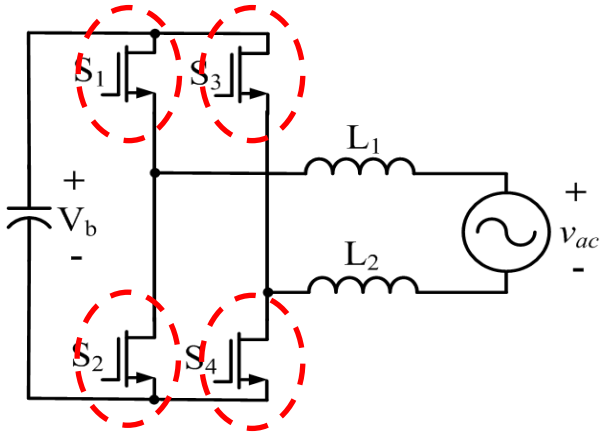


Bridgeless PFC

Hard-switched FET



Buck converter

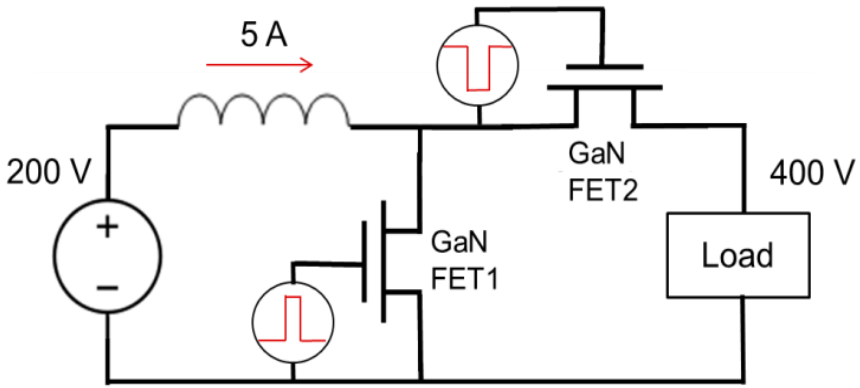


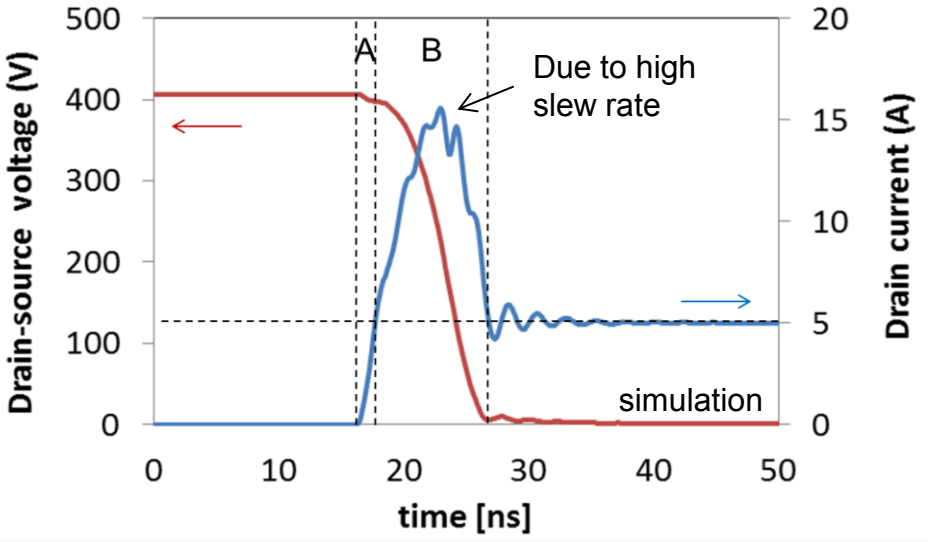
Inverter

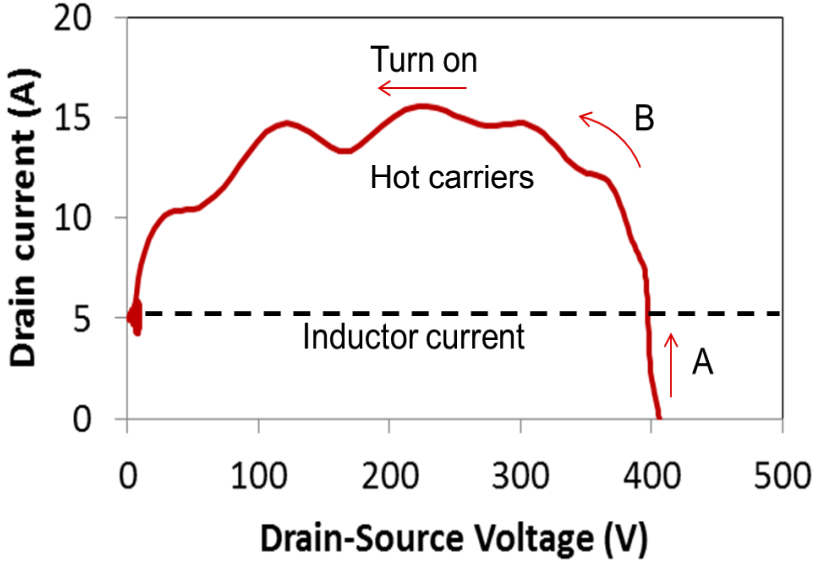
This makes it possible to think in terms of a standard test vehicle

The turn-on transition is hard-switched

e.g. boost converter







The FET is subject to repetitive hot-carrier stress and SOA boundaries

What makes application-relevant qualification feasible

- It is difficult to standardize application-relevant qualification due to the diversity of applications and uses
- Hard-switching is a fundamental transition in power management
- This identification makes it possible to use a test vehicle
- It simplifies the task to qualifying the *intrinsic device* for hard-switching, removing the focus from application diversity
- It is in accordance with JEDEC recommendations, e.g. JESD94A *"A test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms"*
- If it is not too much to ask - can this be a non-proprietary vehicle that runs the test in an energy-efficient manner, and is also well-known?

Double-pulse tester: a well-known circuit

Widely used for the characterization of semiconductor switching dynamics. The list below is from Google search plus a search of major conferences in 2015

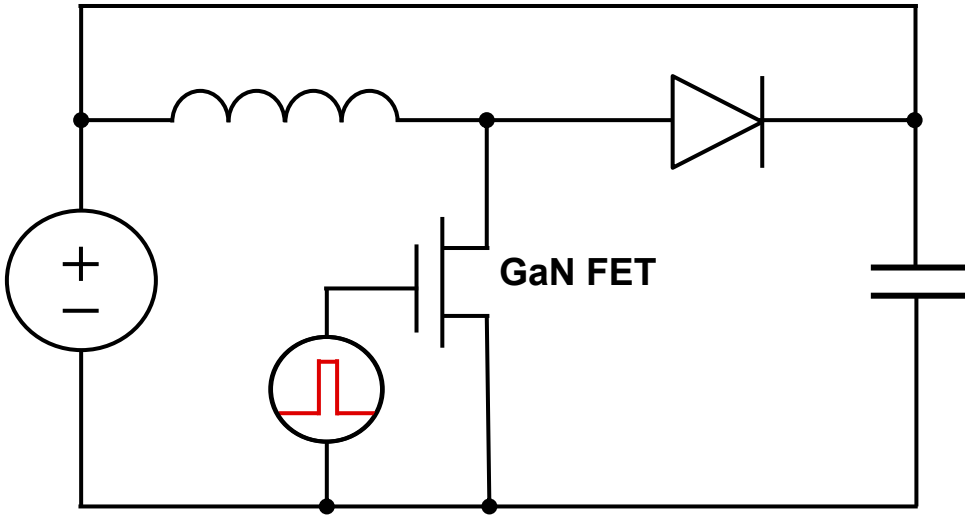
Aalborg University	Panasonic
APEI	Princeton Power Systems
Chinese Academy of Sciences	Robert Bosch LLC
Cree (Wolfspeed)	SmartMotor AS
Danfoss Silicon Power GmbH	South China University of Technology
Fairchild	Technical University of Denmark
Ford Motor Company	Texas Instruments
Fraunhofer Institute	Hong Kong University of Science and Tech.
GaN Systems Inc.	The Ohio State University
General Electric	The University of Alabama
GeneSiC Semiconductor	The University of Manchester
Hella Corporate Center USA Inc.	The University of Tennessee
Infineon	Tsinghua University
Infineon Technologies	United Silicon Carbide, Inc.,
Kettering University	University of Erlangen-Nuremberg
Mitsubishi Electric	University of Nottingham
Nanjing Institute of Technology	University of Parma
National Technical University of Athens	University of Stuttgart
NC State University	University of Warwick
North Carolina State University	Virginia Tech
Norwegian University of Science and Tech.	Zhejiang University

App notes using double-pulse tester:

- Cree CPWR-AN09
- GaN Systems: CN001
- GeneSiC: GA100SBJT12
- Fairchild AN-9020

JEDEC-compliant* hard-switching test-vehicle

Double-pulse tester ≡ Boost converter with output tied to input



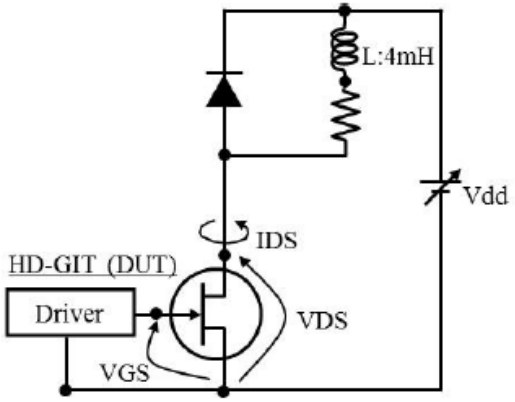
Double pulse mode:
characterize switching dynamics
Continuous pulse mode:
Hard-switching stress

- *Low-side only → no high-side drive complexity and failures
- High-reliability SiC Schottky diode
- short turn-on pulses save power

*From JESD94A – *"A test vehicle may be preferable since the actual product complexity may mask intrinsic failure mechanisms"*

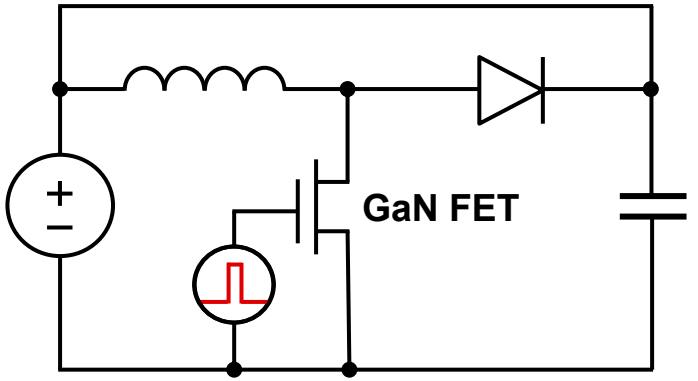
Literature search for reliability cells

Panasonic reliability test circuit
(double-pulse tester)



Kaneko et. al. ISPSD 2015

TI reliability test circuit
(boost converter with output shorted to input)

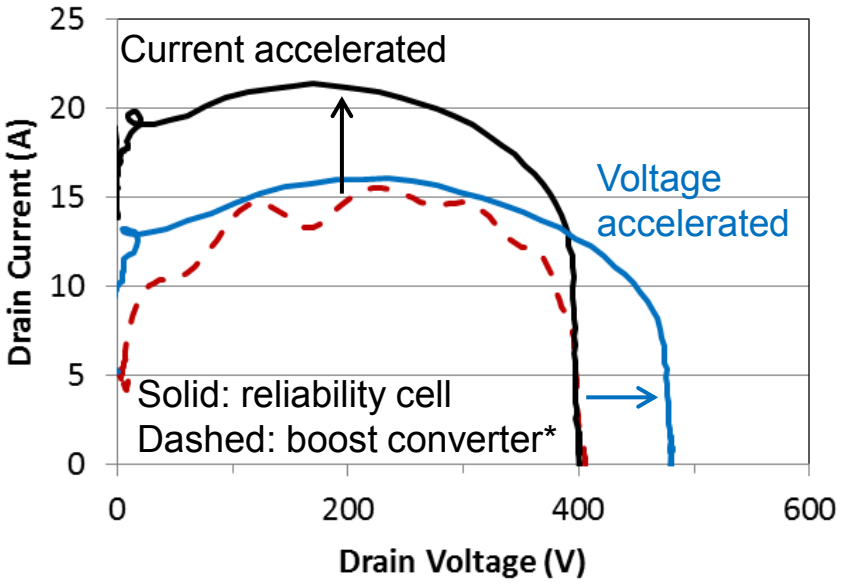


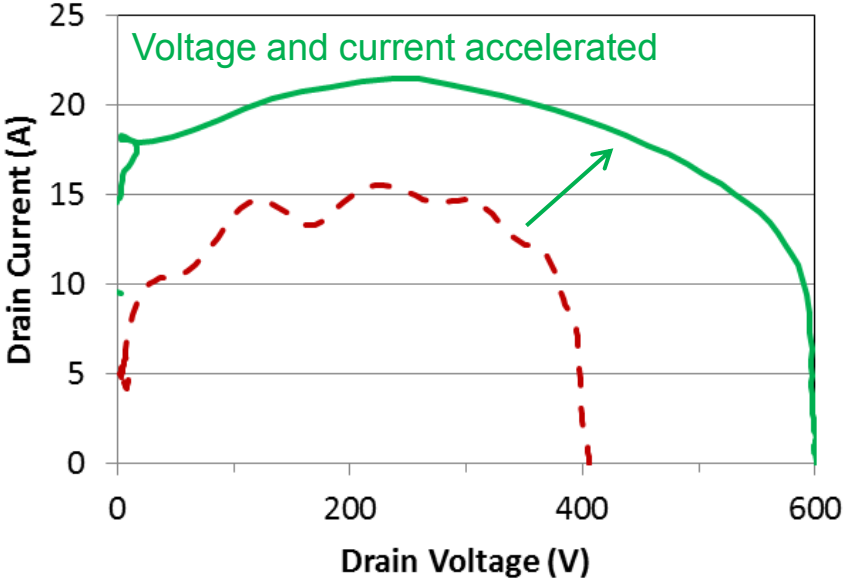
S.R. Bahl, Reliability whitepaper downloadable from www.ti.com/GaN

The cells are equivalent

This means that both companies (Panasonic and TI) independently came up with the same hard-switching reliability vehicle!

Reliability cell can accelerate stress



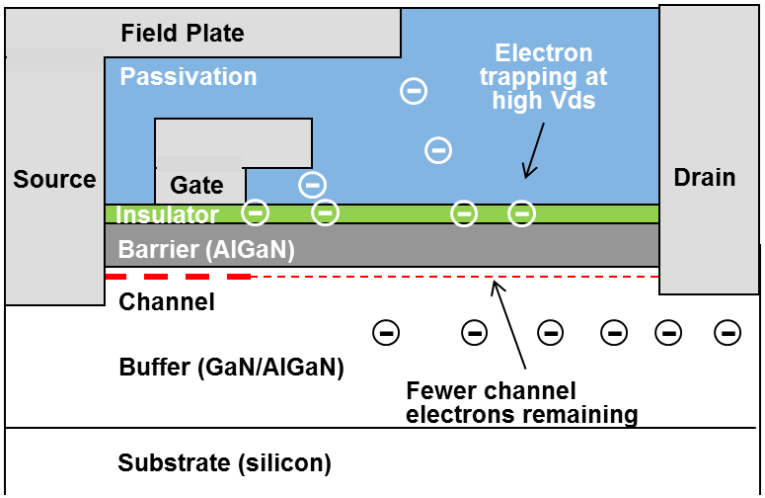


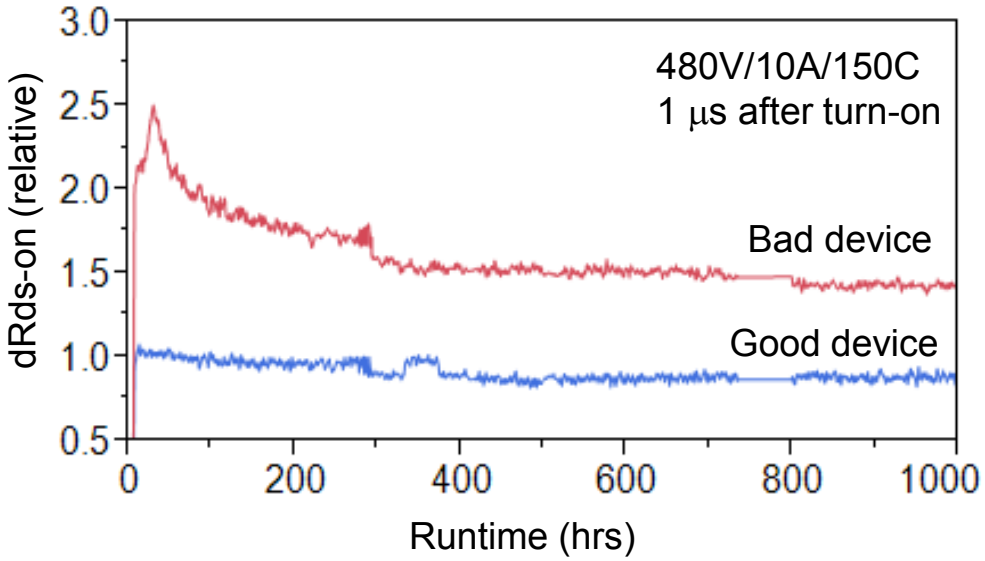
- Reliability cell provides coverage for the application SOA
- Voltage acceleration provided by increasing the supply voltage
- Current acceleration provided by increasing the inductor current
- Other factors can also be accelerated, e.g. temperature, frequency

*boost converter locus is simulated, and reliability-cell locus is measured

Dynamic Rds-on measurement in GaN

- dRon increase is regarded as a key GaN challenge
- Electron trapping during off-pulses causes a memory effect that increases Rds-on at turn-on
- This causes lower efficiency and excessive self-heating
- dRon is difficult to measure due to quick recovery (charges de-trap)





Reliability cell is able to monitor dRon evolution in GaN, and to detect bad devices

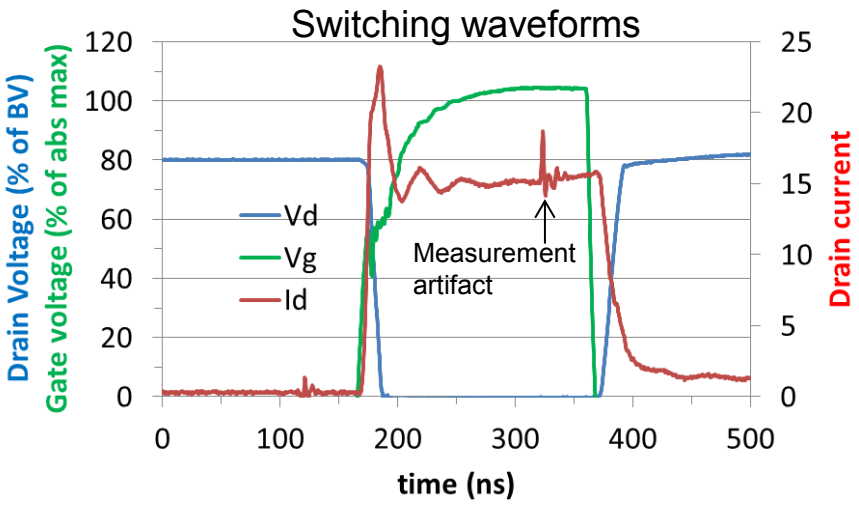
SiC MOSFET gate overstress testing

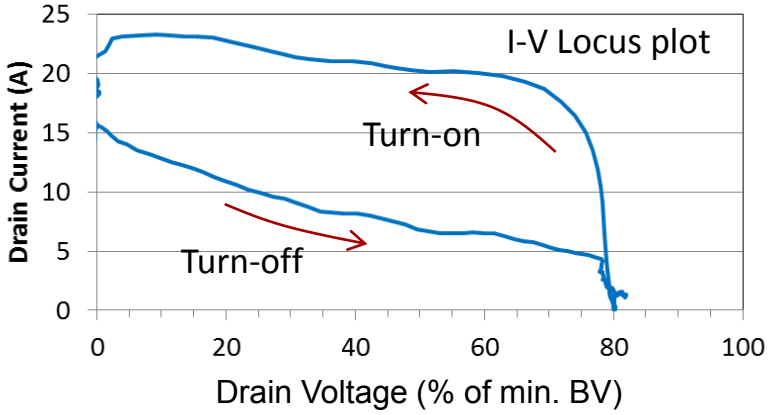
SiC FET tested for 200 h at Inductor current=14 A, T=90C Vds=80% of BV and Vg_max of 5% above *abs-max*.

Parameter	delta
Vt	115 mV
Idss	0.21 uA
Rds-on	0.5 (mΩ)
Igf	17 uA
Igr	1.9 uA
Vsd	40 mV

- Vt was relatively unchanged even above abs-max.
- Main change was in gate current

→ Allows to study degradation modes





Summary

- Customers need to be assured that devices are reliable under actual-use conditions in order to design them into systems
- Hard-switching is an important mission profile for power management, and is not covered by existing qualification (e.g. JEDEC 47). It needs to be done to ensure that there are no unknown failure modes
- The well-known double-pulse tester is a good JEDEC compliant test vehicle for hard-switching. It can accelerate stress conditions, enabling determination of acceleration factors and lifetime extrapolation
- It can excite technology specific degradation modes, e.g. dynamic Rds-on in GaN from hard switching, leakage from gate overstress in SiC
- It is generic to all technologies, and has been used for testing GaN, SiC and Si
- It can resolve the difficulty of application diversity, by shifting the focus from the application to the device