Extraction of Dynamic On-resistance in GaN Transistors

under Soft- and Hard-switching Conditions

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***Abstract*— In this paper we present a new measurement technique for extracting dynamic on-resistance (R_{dson}) of GaN transistors. Dynamic R_{dson} of commercial GaN transistors in soft-switching and hard-switching conditions have been measured. By comparing the dynamic R_{dson} in both switching schemes, it is found that the off-state drain voltage stress is the main cause for the increase of dynamic R_{dson}, while the switching losses in the hard-switching transient could cause additional trapping and degradation, possibly due to channel hot electrons/phonons.**

Keywords-GaN; Dynamic R_{dson}; Soft-switching; Hard-switching; hot-electron-effect;

I. INTRODUCTION

GaN power transistors have attracted great interest for the next generation of power electronics. High voltage AlGaN/GaN transistors have been demonstrated with kilo-volt breakdown voltages and very low specific on-resistance [1-3]. However, electron trapping in AlGaN/GaN HEMTs causes current collapse and increase of on-resistance (R_{dson}) under dynamic conditions [4], which is one of the most challenging problems facing GaN power transistors.

The most commonly used method for characterizing device trapping and current collapse is the pulsed current-voltage (I-V) measurement. However the pulsed I-V measurement does not simulate the condition of real power electronics circuits. For instance, in hard-switching power converters, the switching transistors have lossy switching transitions, during which both the drain voltage and current stresses are present. In soft-switching circuits, the switching loss is minimized and the major stress is from the off-state drain voltage. Therefore, the measurement of the dynamic R_{dson} in real power electronics circuits is highly desirable. However, there are only a few references [5-8] that have extracted the dynamic R_{dson} of GaN transistors and only [7] has clearly illustrated the measurement method and circuit. In this paper, a simple dynamic R_{dson} measurement method is presented. The dynamic R_{dson} of commercial GaN normally-off power transistors in soft-switching and hard-switching circuits is studied.

II. DYNAMIC R_{DSON} MEASUREMENT

A. Dynamic R_{dson} extraction method

In principle, the dynamic R_{dson}, which we describe with the symbol $\tilde{R}_{dson}$, can be calculated by $\tilde{R}_{dson} = \tilde{V}_{dson}/\tilde{I}_{dson}$, where $\tilde{V}_{dson}$ and $\tilde{I}_{dson}$ are the on-state drain-to-source voltage and drain current during dynamic operation. Once $\tilde{V}_{dson}$ and $\tilde{I}_{dson}$ are measured, $\tilde{R}_{dson}$ can be calculated. However, it is challenging to determine $\tilde{V}_{dson}$ in the presence of a large drain voltage swing on the switching device. For example, the drain voltage can swing between hundreds of volts in the off-state and several millivolts in the on-state. Direct measurement of $\tilde{V}_{dson}$ using oscilloscope voltage probes either gives poor accuracy or causes saturation of the oscilloscope channel.

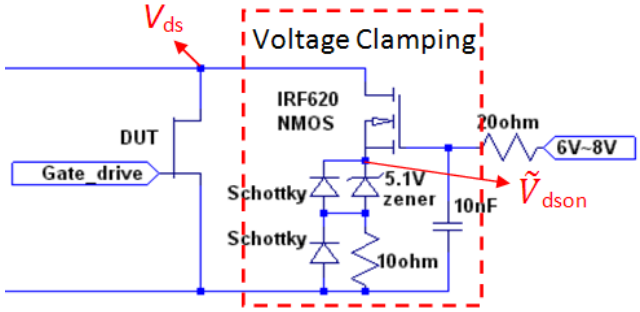

Figure 1. Voltage clamping circuit for V_{dson} measurement

A voltage clamp circuit is needed for $\tilde{V}_{dson}$ measurement to avoid the off-state drain voltage saturating the oscilloscope. Reference [6] used a Wilson current mirror based circuit for $\tilde{V}_{dson}$ measurement. Here we designed a simple voltage clamping circuit as shown in Fig. 1. A 200 V Si power MOSFET IRF620 was used for voltage clamping. The gate of the Si MOSFET is biased at a constant voltage V_g above its threshold voltage V_{th}. When the device-under-test (DUT) is in off-state, the source voltage of the IRF620 is clamped at $V_g - V_{th}$. When the DUT is in on-state, the IRF620 is turned on, providing a low impedance path to measure the $\tilde{V}_{dson}$ of the DUT. In our measurement, V_g was adjusted between 6 V and 8 V to minimize $\tilde{V}_{dson}$ voltage spikes, while ensuring that minimal current is drawn by the clamp FET and therefore

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V_{dsoff} of the DUT is not reduced. The diodes and resistors in the clamping circuit also help to reduce $\tilde{V}_{dson}$ spikes and ringing during the DUT's switching transient. The voltage range of the clamping circuit is 200 V and the $\tilde{V}_{dson}$ can be measured as fast as 1 µs after the DUT is switched on. Transistors with higher breakdown voltage and lower current rating than the IRF620 can be used to increase the voltage range and the speed of the clamping circuit.

Commercial normally-off GaN transistors were used in the measurement. Si MOSFETs IRF620 with similar current and voltage ratings as the GaN transistors were used as a reference. Data sheet ratings are compared in Table 1. The $\tilde{R}_{dson}$ measurement error in our setup is estimated to be between 5 mΩ and 10 mΩ.

TABLE I. DEVICE DATASHEET RATINGS

	Commercial GaN transistor	*Si MOSFET IRF620*
BVdss (V)	200	200
Max Id (A)	3	5
R_{dson} (mΩ)	100	800

B. *Dynamic R_{dson} in soft-switching condition*

A soft-switching circuit has been built to study the off-state V_{ds} stress on the GaN power transistors. The soft switching circuit implementing zero-voltage-switching is shown in Fig. 2. Due to the very high gain of the GaN transistor, a gate drive was built to reduce device ringing. $\tilde{I}_{dson}$ of the DUT is calculated by

$$\tilde{I}_{dson} = I_1 + I_2 - Cd\tilde{V}_{dson}/dt \qquad (1)$$

where the current I_1 and I_2 were measured using Agilent current probe N2893A with Agilent oscilloscope DSO6054A. In on-state, the term $Cd\tilde{V}_{dson}/dt$ in (1) was less than 5 mA, which is small compared to I_1+I_2, therefore,

$$\tilde{I}_{dson} \approx I_1 + I_2 \qquad (2)$$

Before the soft switching test, DC I_d-V_d characteristics were measured on fresh GaN transistors and Si MOSFETs to determine their DC R_{dson}, which are 0.05 Ω and 0.64 Ω respectively, well below the datasheet values. The GaN transistor soft-switching waveforms at peak V_{ds} stress of 150 V are shown in Fig. 3. The device is switched on when the off-state drain voltage drops to zero. The on-state and off-state durations in each switching cycle are 2 µs and 1.3 µs respectively. The switching frequency is 300 kHz.

The dynamic R_{dson}, $\tilde{R}_{dson}$, as a function of the off-state peak V_{ds} stress is plotted in Fig. 4, normalized by the DC R_{dson}. $\tilde{R}_{dson}$ is measured at 2 µs after the peak V_{ds} stress. As shown in Fig. 4, $\tilde{R}_{dson}$ of the GaN transistor increased more than 3 times over its DC R_{dson}, due to the off-state high-electric-field stress induced trapping and possibly degradation in the transistor [9]. On the other hand, the ratio between the dynamic R_{dson} and DC R_{dson} of the Si MOSFET is within 1.1, which is as expected for Si MOSFETs.

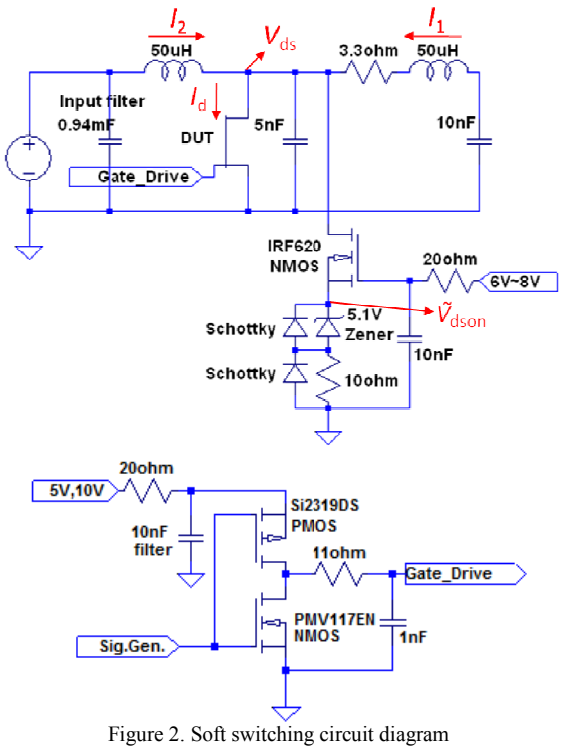

Figure 2. Soft switching circuit diagram

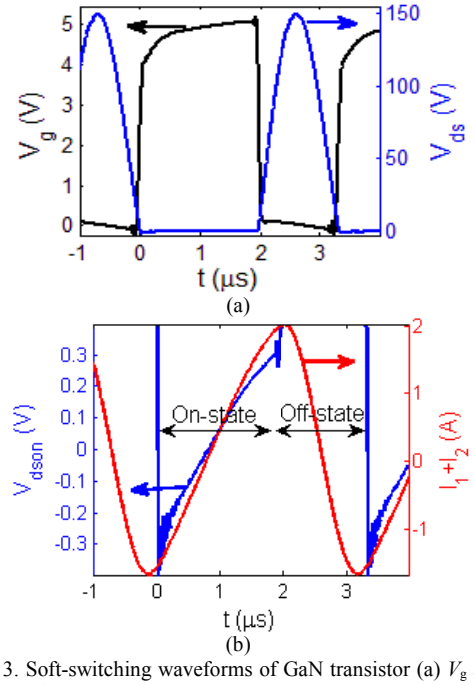

Figure 3. Soft-switching waveforms of GaN transistor (a) V_g and V_{ds} (b) V_{dson} and I_1+I_2 waveforms

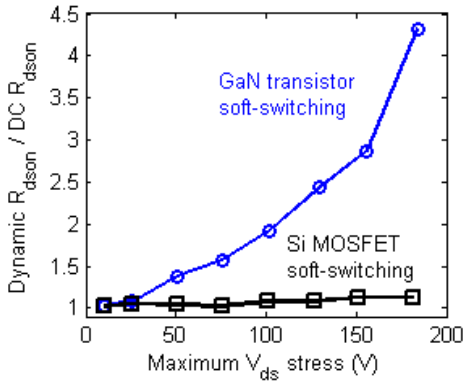

Figure 4. Normalized dynamic R_{dson} of the GaN transistor and Si MOSFET in soft-switching condition at 2 µs after the peak V_{ds} stress.

C. *Dynamic R_{dson} in hard-switching condition*

In contrast to the soft-switching circuit, a hard-switched power transistor has switching losses due to the overlapping of V_{ds} with I_{ds} during the switching transient. Therefore, apart from the off-state V_{ds} stress, the device also experiences an additional pulse of high voltage and high current stress during its switching transient, which could cause additional trapping or degradation due to the channel hot electrons/phonons in GaN transistors [9-11].

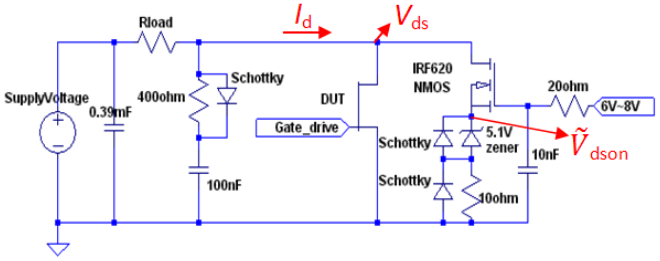

Figure 5. Hard-switching circuit diagram

A hard-switching circuit was built as shown in Fig. 5 to study the effect of switching losses on the GaN transistor dynamic R_{dson}. The load resistor R_{Load} in Fig. 5 was adjusted to maintain the on-state drain current around 1 A. The 100 nF capacitor with the 400 Ω resistor and Schottky diode is the input filter to prevent the overshooting of the drain voltage. Before the hard switching experiment, DC R_{dson} was measured on fresh GaN transistors. The DUT was turned on for 15 µs in a 1 ms period to reduce self-heating. Fig. 6 shows the turn-on and turn-off transient waveforms of the GaN transistor with the off-state V_{ds} of 150 V. Due to the overlapping of I_d with V_{ds}, the switching loss in Fig. 6 is 3.6 µJ per switching cycle with peak power of 20 W and 46 W for the turn-on and turn-off transients respectively.

The dynamic R_{dson}, $\tilde{R}_{dson}$, was measured at 2 µs and 10 µs after the device was switched on. As shown in Fig. 7, $\tilde{R}_{dson}$ increased more than 3 times over its DC R_{dson} value at V_{ds} stress of 180 V. It also decreased with time after the device was turned on, indicating a detrapping transient. On the other hand, the dynamic R_{dson} of the Si MOFETs is within 10 mΩ from its DC R_{dson}.

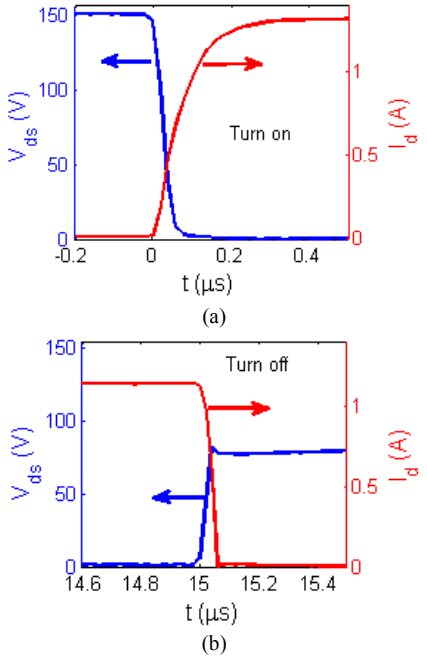

Figure 6. GaN transistor hard switching V_{ds}, I_d waveforms in (a) turn-on transient and (b) turn-off transient at 150 V V_{ds} stress. The V_{ds} rises to 150 V in (b) with a *RC* time constant of 40 µs of the input filter.

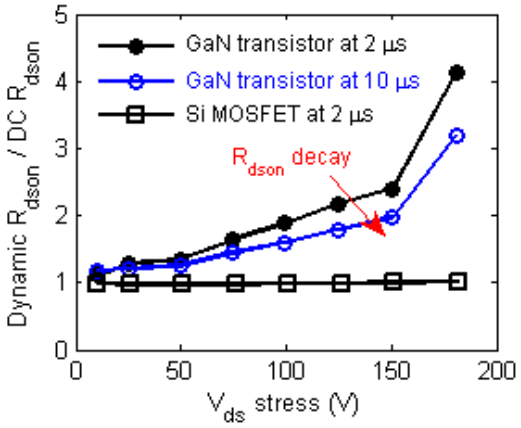

Figure 7. Normalized dynamic R_{dson} of the hard-switched GaN transistor and Si MOSFET at 2 µs and 10 µs after the devices were switched on.

III. DYNAMIC R_{DSON} COMPARISON IN SOFT- AND HARD-SWITCHING CONDITIONS

The increase of the dynamic R_{dson} from the initial DC R_{dson}, $\Delta R_{dson} = \tilde{R}_{dson} - R_{dson}$, can result from trapping in the GaN transistors according to the "virtual gate" concept [4]. Since the devices might also be permanently degraded during the dynamic R_{dson} measurement, ΔR_{dson} represents both the trapping and degradation in the transistors. The effect of the soft switching and hard switching on ΔR_{dson} of the GaN transistors is compared in Fig. 8.

Up to 150 V V_{ds} stress, the difference between the hard switching and soft switching on ΔR_{dson} is small, less than 15 mΩ. At V_{ds} of 180 V and switching loss of 4.7 µJ per switching

cycle, the ΔR_{dson} of the hard-switched GaN transistor is 43 mΩ (24%) more than the soft-switched GaN transistor. Note that hard-switching with 1.7 times higher switching loss (12.5 μJ per switching cycle) at V_{ds} of 50 V causes little effect on ΔR_{dson}, as shown in Fig. 8 for the hard-switched GaN transistor with 10 nF C_{ds} at V_{ds} = 50 V. This suggests that the switching loss by itself is not sufficient to degrade $\tilde{R}_{dson}$. It needs a certain drain voltage to have an impact, which is consistent with the hot electron effects [9, 10].

With the 10 nF C_{ds}, ΔR_{dson} of the hard-switched GaN transistor increased very rapidly even after 75 V V_{ds} stress. The dramatic increase of dynamic R_{dson} could be due to the instantaneous heating from channel hot phonons [11]. At V_{ds} = 100 V, due to the fast discharge of the 10 nF capacitor, the GaN transistor sinks about 15 A of peak current. This is higher than its pulsed current rating of 12 A. While it is necessary to minimize the switching losses of the hard-switched GaN transistors, further investigation is needed to understand the effects of switching losses on GaN power transistors, especially on their the long term reliability.

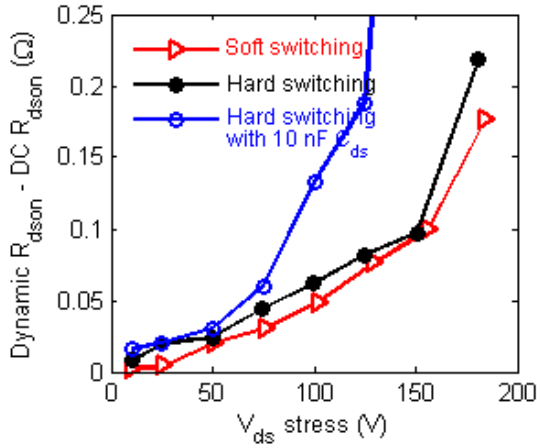

Figure 8. ΔR_{dson} of GaN transistors measured at 2 μs after the peak off-state V_{ds} stress as a function of V_{ds} in hard- and soft- conditions. A 10 nF capacitor was connected to the output of one of the hard-switched transistors to increase its switching loss.

IV. Conclusion

We have presented a method for direct extraction of the dynamic R_{dson} of power switching transistors in switching circuits. The dynamic R_{dson} of GaN transistors in soft-switching and hard-switching conditions has been compared. While the off-state V_{ds} stress is a major contribution to the increase of dynamic R_{dson}, the hard-switching transient can induce additional trapping and degradation in GaN transistors, when the switching loss is coupled with the high drain stresses. Additional, capacitance on the output needs to be minimized to avoid overcurrent conditions. Further investigation of the physical mechanisms, namely the hot electron/phonon effects, is needed to understand the influences of different switching schemes on GaN power transistors.

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