Degradation Assessment in IGBT Modules Using Four-Point Probing Approach

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***Abstract*—Four-point probing of electrical parameters on various components of IGBT modules is suggested as an approach for the estimation of degradation in stressed devices. By comparison of these parameters for stressed and new components one can evaluate an overall degradation of the module and find out the wear state of individual components. This knowledge can be applied for preventing early failures and for optimization of the device design. The method is presented by regarding a standard type power module subjected to power cycling.**

***Index Terms*—Four-point probing, interconnections, physics-of-failure, power modules, thermo-mechanical degradation.**

I. Introduction

POWER devices are currently used in a wide range of applications including the automotive industry, wind and solar power energetics, etc. In these diverse fields of application, the device design and construction do not always match the loads and as a result power modules can fail earlier than expected. Therefore, the interest in understanding and modeling the processes limiting the performance of a component is strong [1], [2].

Obtaining the details regarding a mechanism responsible for a failure of a power electronic component is often problematic. Normally, a component is not investigated until it fails, and at this stage, the information regarding the responsible mechanisms is lost due to catastrophic final stages of the failure leading for instance to burning of some parts, explosions, or similar [3]–[6]. Especially, the evolution and the distribution of the degradation processes causing the failure is difficult to assess afterwards. Therefore, many failure processes have been grouped into the same category even though they are very different with respect to dependence on the load. One of the possible approaches to solve this problem is to monitor on-state properties [7] of the device or its particular component and apply different types of investigation. This could be characterization through microsectioning [8] or focused ion beam (FIB) technique [4], [9]. However, as many failures occur after many years of operation at normal load a typical approach is to use accelerated tests in which high loads are applied. Under these conditions, degradation occurs faster but one needs to be careful about failure mechanisms, which could be not necessarily the same as for normal loads.

Electrical properties of power modules are governed by the quality of used materials and made interfaces or interconnections, and therefore, a subject of their degradation under the load. For example, the partly delamination of a bond wire will change the local current distribution as well as the effective resistance of the given interface. However, an eventual failure might constitute several types of subcomponent failures, which is not necessarily measurable when considering a full module. One example of this is thermal fatigue. A power module is composed of several semiconductor chips, interfaces, and solders. Each of these might be damaged by temperature cycling and contribute to an eventual device failure. However, even if some individual components show significant wear, the full module might still work due to the quite a number of elements constituting it [5], [9]–[11]. One of the ways to evaluate thermal-related degradation is to measure electrical properties of the components or interconnections individually.

Four-point probing or four-terminal sensing provides a high resolution technique for measuring local electrical properties of a given sample [9], [12]. By comparing the parameters measured for stressed and new components or interfaces, one could assess the present quality state. Furthermore, in contrast to microsectioning or FIB, four-point probing is a nondamaging technique, which renders it possible to use the sample after the analysis.

In this paper, a four-point probing technique is developed for electrical measurements on individual semiconductor chips and interconnections: bond wires, solders, and metallizations in insulated gate bipolar transistor (IGBT)-based power modules. This approach allows to assess the degradation type, speed, and distribution through different components as a function of stresses and time. It gives insights into understanding of failure mechanisms, as well as helps to optimize the module design. To illustrate the method, standard IGBT modules subjected to power cycling are studied.

II. Method

A. Wire Geometry

The considered module consists of six identical sections designed as depicted in Fig. 1. Sections are numbered from one to six (S_1–S_6). This is merely a means of keeping an overview of the various sections.

Every section consists of two IGBTs (I_1 and I_2) and two diodes (D_1 and D_2). The IGBTs are connected to a DCB through a solder layer and 12 bond wires (w_1–w_{12}). In the same way, the diodes are connected to the DCB with 16 wires. Sixteen wires

Manuscript received March 21, 2014; accepted July 14, 2014. Date of publication August 6, 2014; date of current version December 23, 2014. This work was a part of the Center of Reliable Power Electronics supported by the Danish Strategic Research Council. Recommended for publication by Associate Editor P. d. P. Rimmen.

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Digital Object Identifier 10.1109/TPEL.2014.2344174

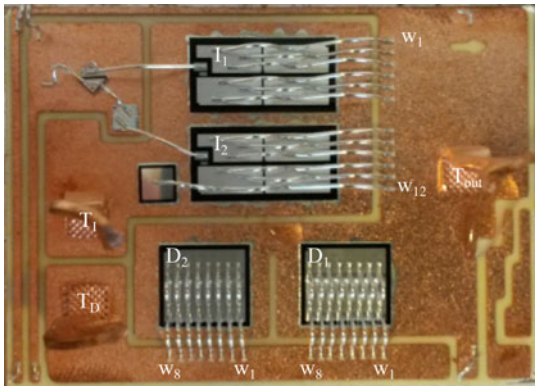

Fig. 1. Image of a single section of the power module under the study.

TABLE I
GROUPING OF IGBT WIRES

Wire #	Description
$w_{1,6,7,12}$	Longest wires placed at the edge of the transistors.
$w_{2,5,8,11}$	Shortest wires.
$w_{3,9}$	Medium length mid chip placed wires.
$w_{4,10}$	Almost same length as the first group and mid chip placed wires.

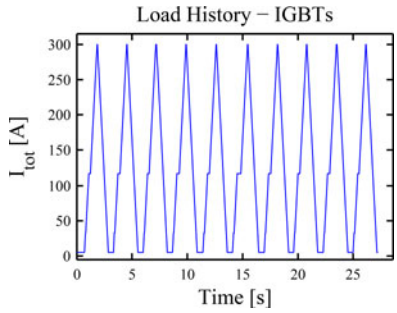

Fig. 2. Current load applied to transistor part of the module for a selected time frame.

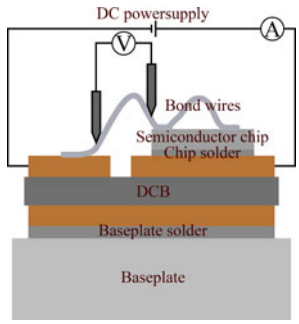

Fig. 3. Illustration of the four-point probing measurement method on a single wire of IGBT module.

on the top of the diodes are placed uniformly and they have equal length, while 12 wires on the top of the IGBTs are placed in varying positions and they are of varying lengths. From this point and forward, we are separating the IGBT wires into four groups based on wire placement and length, which are presented in Table I.

B. Power Cycling

In real-life operation, modules can fail earlier compared to the expected lifetime. The failure is typically catastrophic and any postfailure analysis is complicated due to significant damage (in some cases even explosion) of the module. To investigate the reason for the failure, the module needs to be removed from the load prior to it, which is hardly possible. A widely used alternative way is to run so-called accelerated tests in which the modules are power cycled at some particular conditions and one can easily investigate the module with given number of cycles, i.e., at the beginning, around the middle, or close to the end of lifetime. Presently, three modules are investigated: a new module for referencing, one close to failure (end of lifetime), and one in between (with respect to number of cycles). The samples are denoted modules A, C, and B, respectively. The modules were power cycled with the current periodically ramped from zero to 300A as can be seen in Fig. 2. In power modules subjected to high pulsed currents or high frequency switching, this is a commonly experienced load [2], [7], [13].

In the test setup, the module is mounted on a heatsink, which is water cooled at a temperature below 40°C.

C. Four-point Probing Setup and Procedure

The concept of four-point probing has been widely used for years. Originally, it was mainly applied semiconductor materials to measure the resistivity of, for example, transistors [12]. In the last years, four-point probing became a widely used method for different materials and various purposes. For instance, it was recently applied to estimate fracturing and degradation of materials through the change of resistance [9].

Sketch of our setup is presented in Fig. 3. We developed a system providing positioning of the probes with very high precision on the micrometer scale. This allows us to repeat the measurement geometry on different parts of the device, i.e., to easily compare interfaces or interconnections of the same type. The idea of the method is to separate the probes supplying the current from the voltage measuring probes. This separation limits the current going through the probes measuring voltage, thus, minimizing the influence of the probe and contact resistances. It means that very small changes of resistance due to degradation of material or interfaces caused by thermal fatigue, delamination, lift-off, etc., can be measured.

Depending on the position of the probes, the expected signal varies. If measured across a semiconductor device, a nonlinear relation is to be expected, whereas everywhere else a strictly ohmic behavior should be seen.

Using the above-described setup different configurations for probing are possible. Three approaches utilized in this study are described as follows.

1) *Sections:* Potential difference as a function of applied current from terminal to terminal. As indicated in Fig. 1, three

terminals are present: IGBT side (T_{I}), diode side (T_{D}), and the output terminal (T_{out}). Accordingly, the probing is divided into two measurements: $\mathrm{T_I} \rightarrow T_{\mathrm{out}}$ through the IGBTs and $T_{\mathrm{out}} \rightarrow T_{\mathrm{D}}$ through the diodes. By comparing results with a new module, this gives an overall image of the section state including the semiconductor components, solder, metallization, and wires.

2) *Chips:* Potential difference across the four semiconductor chips as a function of applied current. The potential is measured locally on the chip surfaces meaning $T_I \rightarrow I_{1,2}$ and $T_{\mathrm{out}} \rightarrow D_{1,2}$. This includes the state of the solder and metallization as well. The measurement is carried out at several selected positions on top of the chips.

3) *Wires:* Change in resistance of the wire/chip interfaces compared to a new sample of the same type. Initially, the potential difference is measured on the top of the wire curve, see Fig. 3. This is done with a fixed and known distance between the probes, thus making it possible to derive the local wire current. After obtaining the current distribution between the wires, the potential difference between the probe positioned on the chip surface and one on the wire is measured. The local wire current together with the potential across the wire/chip interfaces yields an effective resistance. This resistance includes the wire itself, the bonded interfaces, and a small fraction of metallization/Cu beside the interfaces.

All measurements are performed using steady-state dc between 0 and 5 A. These are low currents for power modules. The reason for keeping the current low is to limit electrothermal heating. However, even at these currents, a local temperature change is found. Therefore, the temperature is controlled using Peltier elements and a PID concept, i.e., applying a pause in between measurements and requiring a temperature variation below $0.1\,\mathrm{K}$. The pause is also required to take into account the responsivity of the thermocouple, which is attached to the ceramic near the edge of the section.

Standard digital controlled power supplies are used for applying the current to the sample, the Peltier elements and for controlling the IGBT gates. For measuring the sample temperature and potential difference during probing, high resolution multimeters are utilized.

For investigating the standard deviation of the method, measurements are repeated and compared to a reference. It is found that the voltage drop for ohmic measurements is reproducible within the microvolts interval. Furthermore, to continuously ensure the validity of the results, a few selected approaches are utilized. The probing of the semiconductor components is carried out in several selected locations on top of the chip to ensure that the measured values are not local deviations. For wire measurements, the calculated local currents are summed and compared to the total applied current.

D. Scanning Electron Microscopy and Optical Microscopy

To relate the change of electrical properties of the power cycled modules with particular failures or degradation of the components scanning electron microscopy (SEM) equipped by the FIB technique and microsectioning approach based on optical microscopy were used. SEM/FIB is primarily used to investigate the state of the metallization. The SEM/FIB analysis was carried out utilizing a Zeiss 1540 XB instrument. Due to limitations on the FIB milling range, the wire interfaces were analyzed using microsectioning. By combining mechanical cutting and microparticle polishing, cross sections of wire/chip interfaces are obtained and studied by an optical microscope. The method and equipment are described in detail in [8].

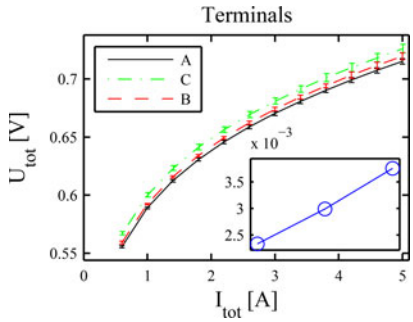

Fig. 4. Mean value of the potential difference between terminals plotted against the applied current with errorbars indicating the spread between the sections. The inset illustrates the voltage spread for three modules at 5 A.

III. Results

A. Four-Point Probing

Measurements across all interfaces of interest (method numbered 1 in Section II-C) were carried out on selected sections of the new module (A) and the most stressed module (C). This study showed that the voltage drop was much more significant on the IGBT chips compared to diodes. Accordingly, the full investigation was limited to the IGBT. Some measurements on diodes were carried out to provide comparison to IGBTs.

1) Sections: In Fig. 4, the electrical potential difference between terminals T_I and T_{out} (across IGBTs) as a function of the applied current is presented. The data are averaged on five sections for every module. In all three curves, deviations obtained on different sections are included as errorbars.

From Fig. 4, the voltage drop is clearly seen to increase with the number of cycles, indicating that the effective resistances of the sections are increased. This shows that the sections degrade over time when power cycled, as would be expected. One can also see that standard deviations are larger for C compared to A and B indicating that degradation is not evenly distributed among the sections. This is illustrated in the inset of Fig. 4, where the voltage spread is plotted for the three modules. The potential differences from T_{out} to T_{D} (across diodes) were all found to be within the errors measured for module A.

2) Terminal to Chip Surface: The measurement presented in Fig. 4 were repeated with the second probe placed on the surface of the chip metallization leaving out the bond wires. To rule out singular effects, the probe was placed on several distinguishable positions on the metallization (corners, wire toes, center). All measurements showed change in voltage within the spread

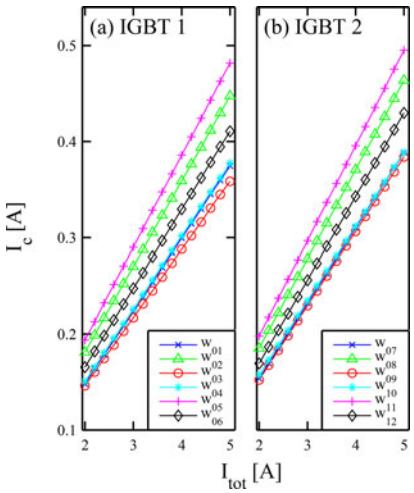

Fig. 5. Local current in each of the wires of a section from module A plotted against the total current.

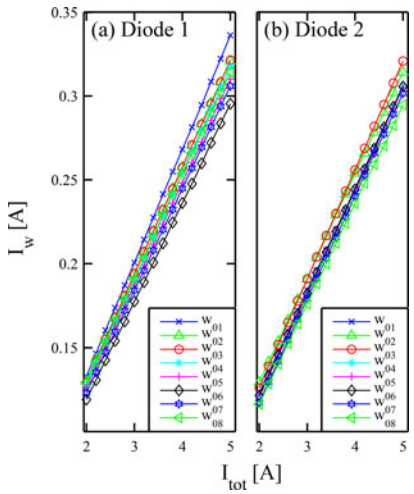

Fig. 6. Local current in each of the wires of a section from module A plotted against the total current.

typical for module A. Therefore, it becomes obvious that the voltage change presented in Fig. 4 is related to the degradation of the bond wire interfaces.

3) Wires—Current Distribution: In Figs. 5 and 6, the local current in the individual wires is presented as a function of the applied total current for two different IGBTs and diodes.

In Fig. 5, a clear difference between the wires can be found. A good correlation between the wires geometry presented in Table I and dependences of Fig. 5 is observed. The shortest wires (namely, 2, 5, 8, and 11) from the second group of Table I carry the highest current. The current in other wires follows well the geometrical placement and length. The deviation of the sum of the local currents in Fig. 5 is less than 5% compared to the applied total current. The results presented in Fig. 5 are for a single section, but qualitatively similar dependences are obtained for other sections of the same module as well as for

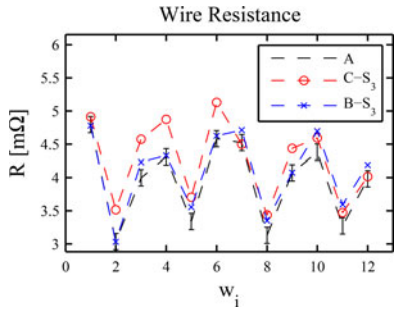

Fig. 7. Resistance of the IGBT bond wires for the selected section of modules B and C and averaged for module A. The lines between the values for different wires are presented only for visual guidance.

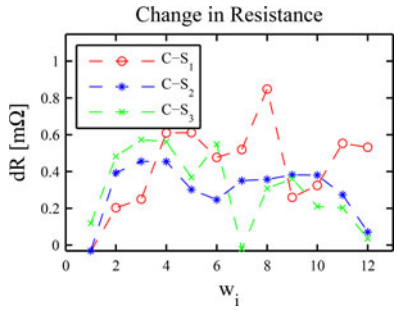

Fig. 8. Difference of resistance of the IGBT bond wires for three sections of module C compared to same wires of module A. The lines between the values for different wires are presented only for visual guidance.

the sections of modules B and C, i.e., those under given number of power cycles.

Compared to the current distribution between the wires on the IGBTs, the current distribution between the wires of the diodes shown in Fig. 6 is much lower. Since all the wires on the diode chips are of the same length and geometry, the small differences between wires are credited to the random production deviations and chip edge effects.

4) Wires—Resistance: By using the calculated local currents and measured potential difference of each wire, an effective wire resistance is obtained. For samples C-S_3 and B-S_3 (where B and C are the modules and S3 is section number 3). these data are presented in Fig. 7 along with the mean values of resistance calculated for five sections of module A.

From Fig. 7, it is clear that the resistances of the wires in samples B-S_3 and C-S_3 are higher than in the new module. The same tendency is found for the majority of the inspected sections.

To better visualize the change in wire resistance between the cycled and new modules, the differences between the values measured on module C and A are presented for every wire and three different sections in Fig. 8. It is clear tendency that the wires at the edges of the sections (w_1 and w_{12}) are less degraded compared to those located in the middle of the section.

To obtain an overall picture of the wire degradation, mean values of resistance measured for each wire on five sections for every module are presented in Figs. 9 and 10. These figures

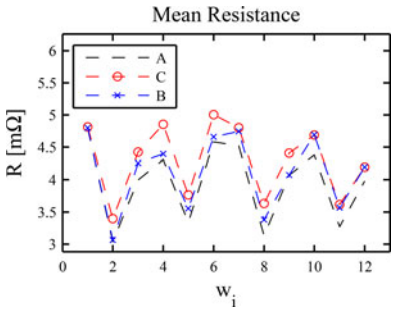

Fig. 9. Mean values of resistance obtained for each wire on five sections for every module A, B, and C. The lines between the values for different wires are presented only for visual guidance.

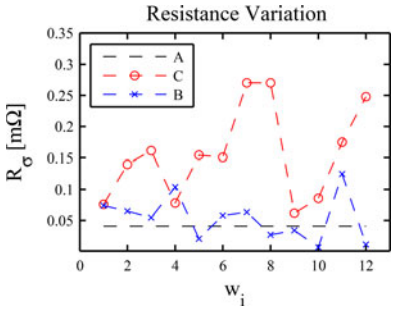

Fig. 10. Values for spread of resistance for every wire on five different sections for modules A, B, and C. Dashed line corresponds to level of standard deviation for new module. The lines between the values for different wires are presented only for visual guidance.

show how the resistance varies for every wire from section to section, i.e., gives the spread of resistance. From the figures, it is obvious that both the resistance and its spread increase with number of cycles. Moreover, certain wires degrade higher than others. In the majority of samples, large resistance changes are observed for the wires having shorter length and located either close to the middle of the chip or at the edge, which neighboring to the next IGBT chip. The very high spread seen for $w_{7,8,11,12}$ is generated by wires partly lifted off in one of the sections (as found by visual observation).

B. Microscopy-Based Failure Mapping

It is found by four-point probing that resistance of wire interfaces increases that probably correspond to degradation under power cycling. However, different types of interfaces (wire bonds, metallization, and solder) contribute to this degradation not in equal manner. To clarify the role of a particular interface, it is important to carry out microanalysis.

1) SEM and FIB: In Figs. 11(a)–(d), SEM surface images of the metallization of IGBTs and diodes for modules A and C are presented. In Fig. 11(a), the ordinary IGBT trench gate structure is clearly seen in the metallization. This is not the case for module C in Fig. 11(b), here the surface is degraded and reconstructed. In contrast, no notable changes are observed for the diode metallizations as one can see in panels (c) and (d). These findings are in good agreement with the four-point

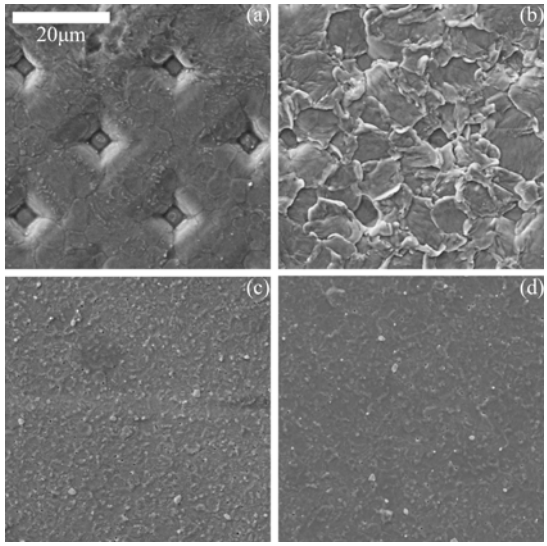

Fig. 11. SEM images of the chip metallization of the IGBT chips in (a) module A, (b) module C, and (c) and (d) the equivalent diode chips.

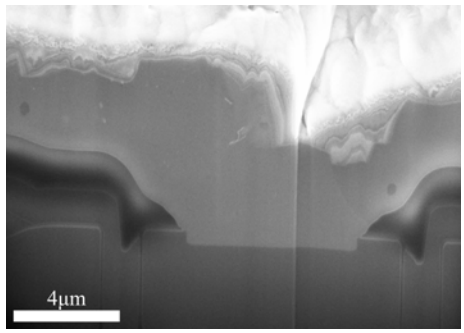

Fig. 12. SEM image of cross section of the IGBT metallization from module C.

probing measurements showing large spreads of local currents on IGBTs compared to the diodes.

The reconstruction observed in the metallization is a well-known degradation process originated by thermal cycling, see [9] and [10]. Reconstruction affects the forward voltage of the section if the metallization is: loosing contact to transistor channels, becoming thinner or causing wire delamination, or lift off. To validate the state of the entire metallization layer (not only surface), FIB milling was applied to obtain cross-sectional views. An example is presented in Fig. 12 . It is found that only the surface layer of the metallization is reconstructed but the rest is in appropriate conditions. Minor diffusion of Si was found using elemental analysis.

2) Microsectioning: In Figs. 13 and 14, cross-sectional views of a bond wire interface are presented. They are obtained using microsectioning combined with optical microscopy. The interface corresponds to the end bond of $C–S_1–w_3$.

In Figs. 13 and 14, fractures propagating from both edges of the bond more than $150\ \mu m$ inwards can be observed. At the heel of the end bond, the fracture reaches ca. $50\ \mu m$ above the chip/metallization interface. From earlier studies, it is know

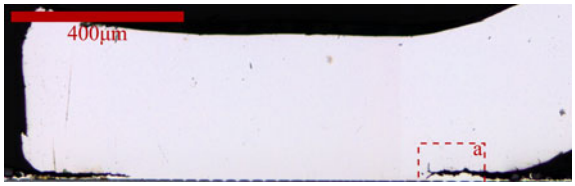

Fig. 13. Optical microscopy image of a wire/IGBT interface on section 3 of module C.

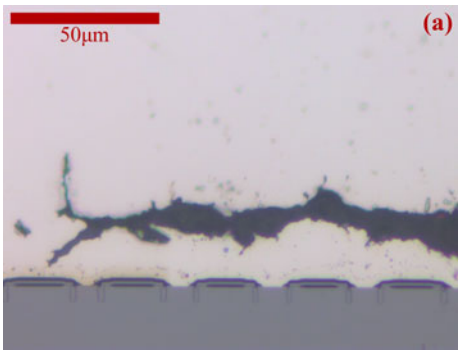

Fig. 14. Magnified part of the image presented in Fig. 13 as dashed rectangle.

that this fracture development goes through the area in the wire, which correspond to gradual interface between the refinement and deformation regions, see [4] and [14].

IV. Discussion

A. Section State

By measuring the electrical potential difference across individual sections of stressed modules, it was possible to establish the type of failure present. As seen in Fig. 4, the *I–V* dependences for IGBTs are nonlinear. However, the increase of voltage from module A to B and further to C has linear dependence, i.e., corresponds to ohmic behavior. The observed ohmic change indicates material fatigue, like mechanical creep of the solder or fracturing of the wire interface. Furthermore, by comparing the change in forward voltage for different sections of the same module, i.e., the spread presented in the inset, one can conclude that the power load is distributed unevenly through the sections because the spread increases. Fatigue is a fundamental occurrence in power cycled modules, however, unevenly distributed fatigue is undesired as the regions stressed additionally can cause early failures. For the diode chips, the change of voltage for B and C modules was found to be within the standard deviations characteristic for the new module. Thus, one can conclude that there is no considerable degradation of diodes and related interfaces that is also confirmed by the microscopy investigations.

B. Diode Bond Wires

Four-point probing study of the diode bond wires showed very small difference in local currents from wire to wire as can be seen in Fig. 6. Assuming that the diode wires are 1) homogeneously placed on the chip surface, 2) same length, and 3) are of the same quality of material, it is very logical to suggest that they degrade in the same manner. From the SEM images of the metallization surface presented in Fig. 11, the state of the diodes reveal almost no restructuring that leads us to the conclusion of a low thermal load, which is the main reason for the degradation of metallization. The combination of the homogeneous current distribution and low load is assumed to be the primary reason for the diode interfaces to remain intact.

C. IGBT Bond Wires

In contrast to the bond wires on the diode chips, the IGBT wires are of unequal length and positioned differently on the chip. The current distributions presented in Fig. 7 show significant deviations from wire to wire. These deviations follow pretty well the geometrical layout of the wires. However, this type of design becomes problematic because local increase of the current leads to additional thermal heating and thereby causes higher mechanical stress. From the data presented in Fig. 8, one can see that wires located at edges, namely, w_1 and w_{12} show the smallest change in resistance, while those close to the central part of the chip demonstrate higher change. Near the outer edges of IGBTs, a smaller change in temperature as well as a lower medium temperature are normally experienced during power cycling [5], [15]. The reason that $w_{6,7}$ do not show the same low damage as $\mathrm{w}_{1,12}$ is the close proximity of the two chips, which create a local heat-up in between the chips as well. The local stress might in the end create the basis for an early failure because lift off of one of the wires place additional load on the surrounding wires.

The change observed in the effective wire resistance is primarily attributed to a change of the bond interfaces. The medium temperature and the current density is not deemed high enough to create significant material changes of the wire itself, e.g., through diffusion or electromigration. However, the power cycling is expected to cause fatigue and fracturing due to mismatch in the expansion coefficients near the interfaces. This is supported by the microsectioning images of a wire interface in Figs. 13 and 14. Here, the dominating degradation is clearly seen to be located around the refinement area of the wire. One can also suggest that the metallization reconstruction on the IGBT chips seen in Fig. 11 can assist the wire lift off.

D. Degradation Evolution and Distribution

By considering the average change in resistance of a given wire interface together with the spread of resistance between various sections, it is possible to map both the evolution and distribution of the damage. In Fig. 9, the mean value of the resistance is clearly seen to increase with number of cycles. The spread between sections plotted in Fig. 10 can give an estimate of the design quality as well as production quality. If the module was ideally designed creating a homogeneously distributed load under operation, then the spread would remain close to that of a new module as the same type of wires would degrade identically. However, the large variation observed for different

wires of module C allows to suggest that the degradation is centered around wires as well as selected sections.

V. Conclusion

The four-point probing method is used for measurements of electrical parameters of power modules. The microvolts resolution of the developed setup enables investigating the condition of the majority of elements, including various interfaces, which are known to be primary origins for most of failures. The originality of the approach is in estimation of correlations between degradation of electrical parameters (for instance, resistance) and development of damages on the microscopic level, which are monitored using optical or electron microscopy.

The method was employed on an IGBT module with a tendency of early failure at certain field loads. Modules at three different stages of lifetime were investigated, namely new module, module close to failure, and one in between. The load applied to the modules causes thermal cycling similar to that experienced by standard power converters in real operation.

The measurements on entire sections demonstrated the nonlinear behavior expected for semiconductor components. Modules B and C show considerable increase in the forward voltage compared to the new module indicating material degradation. The difference between new and worn modules is observed to be of ohmic nature. This is an indication that the ageing and fatigue happens predominantly in interfaces and not in the semiconductor components. It is found that various sections of the same module degrade in different ways most probably due to the fact that the power load is not evenly distributed. Comparing data from different chips, it was observed that IGBT's metallization and bond wires degrade significantly compared to those on diode chips. This degradation was assigned to difference in load and wire geometry on IGBTs. Difference in length and configuration of wires leads to increase of local currents on some of them. Higher local currents cause additional heating and mechanical stresses at the interfaces due to the difference in expansion coefficient for the metallization layer and chip. Moreover, restructuring of metallization is found, which could serve as additional factor for fracturing and wire lift off.

Good agreement between degradation of electrical parameters and formation of structural defects is established. Thus, the four-point probe measurements can be suggested as an independent and a relatively easy method for the estimation of device quality, its ageing and fatigue under operation, as well as for the control of the production quality.

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