Real-Time Aging Monitoring for Power MOSFETs Using Threshold Voltage

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***Abstract*- Power MOSFET is one of the most rapidly aging components in power electronic converters, and some study of the health monitoring of power MOSFETs is made in this paper. This paper proposes a threshold voltage-based real-time aging monitoring method for power MOSFETs in Buck converters. Firstly, the origins of degradation in power MOSFETs are analyzed, and the junction temperature is indicated to be the most promising failure precursor for the health monitoring. Then, threshold voltage is chosen as the thermo-sensitive electrical parameter for junction temperature estimation. For Buck converters, a real-time threshold voltage monitoring method is proposed. Taking advantage of the particular structure of Buck converters, the proposed method only needs to capture the gate-ground voltage, which is costless and easy to realize. Finally, the effectiveness of the proposed method is verified by simulation and experimental results.**

Keywords—power MOSFETs; health monitoring; Buck converters; degradation; failure precursor; threshold voltage

I. INTRODUCTION

The development of power electronic converters has made their widespread use in many fields such as industry, military and aerospace for their low noise, high efficiency and high power density. However, in some cases, the converters may be exposed in severe environments, i.e., electrical overstress, mechanical stress, radiation, or thermal stress during normal operations. In these circumstances, the external forces will lead to degradation or even complete failure of critical internal components. A failure rate distribution of various components in a power converter as shown in Fig.1 illustrates that the electrolytic capacitors and semiconductors are the components most likely to decline [1].

An ageing electrolytic capacitor, which is found to be with distinct failure precursors — the decrease of the capacitance and the increase of the equivalent series resistance (ESR), has attracted much research on the methods to measure its ESR and/or its capacitance [2-6]. However, the precursors of semiconductors are various and the degradation mechanism is still not clear. Several projects have been executed recently to understand and improve power semiconductor device reliability. Most of the work concentrates on insulated gate bipolar transistors (IGBTs) for power electronic converters. In references [7-8], the reliability of IGBT modules,

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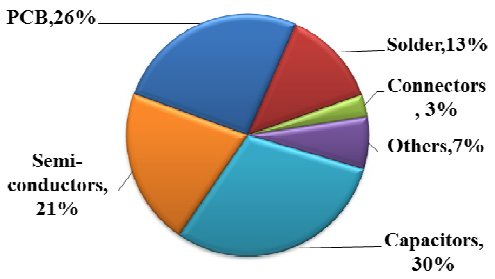


Fig.1. Failure rate districution of different components in power electronic converters [1].

including bond wire liftoff, solder fatigue, and other reliability issues in traction applications, is investigated, and the results are used in later work [9-10]. In reference [11], IGBT technology is optimized by improving the reliability tests and achieving agreement on standardized accelerated tests. There is also investigation into failure precursor parameters for IGBTs [12].The common failure indicators and the drift ratios for failure are listed in Table I [12]. However, failure modes are interdependent. For example, an increase in junction thermal impedance, Z_{th} causes increase in maximum temperature, T_j and this escalates the thermal stress for the bond wires, which will further lead to collector-emitter voltage V_{ce} increasing. Therefore, a careful failure analysis is required.

In conclusion, the recent efforts are mainly for separate devices and focused on IGBTs. But the reality is that power semiconductors are equipped in an active power electronic converter, where conventional monitoring techniques cannot be used with ease. Therefore, two hurdles need to be crossed: 1. Different aging process may present different degradation features and the failure precursors are difficult to unify;

TABLE I
FAILURE INDICATORS AND THE DRIFT RATIOS FOR FAILURE [12]

Failure indicator	Symbol	Drift ratio for failure
Collector-emitter saturation voltage	$V_{ce(sat)}$	5% ↑
Threshold voltage	V_{th}	20% ↑
Collector current	I_{on}	20% ↑
Junction temperature	T_j	20% ↑
Gate saturation current	$I_{g(sat)}$	20% ↑
Thermal impedance	Z_{th}	20% ↑

2. Existing failure precursor monitoring circuits are too complex to apply to active power electronic converters .

This paper is organized as follows. Section II focuses on the origins of power MOSFET failure and analyzes several measurable failure precursors which can quantify the level of aging. On this basis, one common degradation feature is pointed out: causing junction temperature to rise. Given this, the junction temperature is chosen as an overall indicator for health monitoring. According to the temperature sensitivity, the threshold voltage of power MOSFETs is chosen to be thermo-sensitive electrical parameter for the junction temperature estimation. With the regard to threshold voltage measurement, two conventional circuits are explained and discussed to illustrate their disadvantages in Section III. Section IV describes the proposed threshold voltage monitoring method. Then simulation and experimental results are presented to confirm the validity of the proposed method in Section V. Finally, summary is provided in Section VI.

II. Analysis of Degradation in Power MOSFETs

In order to carry on a reliability research of power MOSFETs, the mechanisms of failures and previous research on the failure precursors of power MOSFETs are described and discussed in this section. In general, failure of semiconductor devices can be categorized into two groups: chip-related failure mechanisms and package-related failure mechanisms.

Chip-related failure mechanisms are the root causes for device damage. The reasons for chip-related failures include electrical overstress, electrostatic discharge (ESD), rigger of parasitic transistor, and charge effects [13]. Overheating is a direct result of electrical overstress, which may further lead to secondary breakdown. ESD may partially puncture the gate oxide, and an increase in the threshold voltage V_{th} caused by gate electrical stress is reported in [14]. A large value of dv/dt during turn off will lead to triggering of the parasitic bipolar junction transistor, which may result in a short-circuit failure. Ionic contamination and hot carrier injection are two common degradation causes for power MOSFETs. Ionic contamination is the electric field distortion which is caused by the accumulation of ionic contaminants in the passivation of the high-field region. Hot carrier injection causes defects in the gate oxide. The two charge effects will cause a shift in the performance characteristic of device—such as the threshold voltage (the most common), leakage current, trans-conductance, and saturation current. In general, the threshold voltage will shift from the initial value because of the degradation in the gate oxide region and the shift amount depends on the amount of the interface trapped charge and the oxide trapped charge which are caused by the two charge effects. In an N-channel MOSFET, interface trapped charge makes the threshold voltage negative drift and the effect of oxide trapped charge is converse. However, most researches suggest that oxide trapped charge will be dominant with aging, which means that the threshold voltage will increase with aging [14], [15].

The packaging-related failures are mostly caused by the dissimilarity between the coefficients of thermal expansion (CTE) of the package and chip. The two types of failures are bond failures and die solder layer failure. Bond failure is caused by the difference of CTEs of Si and Al (bond wire), and Die solder layer failures are caused by the difference of CTEs of Si and Cu (substrate). A precursor of wire-bond liftoff is the increase of turn-on resistance $R_{DS(on)}$, while a precursor of solder cracks is the increase of thermal resistance R_{th}.

Therefore, the failure precursors associated with MOSFETs mainly include threshold voltage, on-resistance, and thermal resistance.

It can be found from the failure precursor parameters listed above:

1) The increase of threshold voltage directly results in the increase of switching time and will cause more switching loss.
2) The increased on-state resistance results in more conduction loss.

Usually, ignoring the driving loss, the total loss of a power MOSFET $p_{loss}(t)$ can be expressed as

$$p_{loss}(t) = p_{switching}(t) + p_{conduction}(t) \quad (1)$$

where $p_{switching}(t)$ and $p_{conduction}(t)$ are the transient values of switching loss and conduction loss, respectively. It can be seen that $p_{loss}(t)$ increases with aging. And furthermore, solder cracks lead to increased junction thermal resistance, which together with the total loss causes increasing loss, and the maximum junction temperature will be raised. Therefore, junction temperature is the most promising precursor of failure [16]. A failure is often supposed to happen when the junction temperature is increased by at least 20% of its initial value for the same operating status. For the junction temperature estimation of power semiconductor devices, there are three main methods [17]:

1) Optical methods;
2) Physical contact methods;
3) Electrical methods.

For the reason that the first and the second methods necessitate visual or mechanical access to the device, today device temperature evaluation often uses electrical methods. The thermal dependence of electrical properties of semiconductor devices is used to evaluate the temperature in an electrical method. All the previously presented thermo-sensitive electrical parameters are compared with each other in [17], where the threshold voltage (V_{th}) is proved to be a good choice. However, to eliminate the threshold voltage drift caused by degradation itself, two steps are taken: 1. before each startup, V_{th} is measured as the initial value, which can also be used to evaluate the degradation of the gate oxide; 2. after each shutdown, V_{th} is measured again, and in combination with the initial value, junction temperature can be estimated for the assessment of overall health status.

III. State-of-the-Art Measurements of Threshold Voltage

The threshold voltage is one of the basic parameter of MOSFETs, which has high linearity with the junction temperature (generally in the -2 to -10 mV/°C range) at a small drain current (< 5 mA), and thus it has been widely

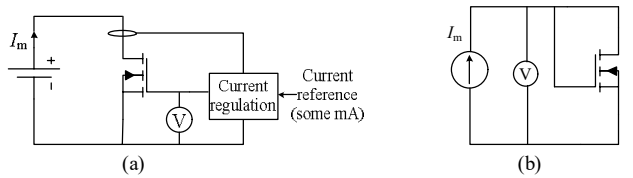


Fig.2. Common threshold voltage measurement circuits: (a) Measuring circuit #1, (b) Measuring circuit #2.

used in the junction temperature estimation of power semiconductor devices [18, 19].

In general, the threshold voltage is measured with a very low current regulation acting on the gate voltage [see Fig. 2(a)] or with a connection of the gate and the drain electrodes [see Fig. 2(b)] [17].The current value is a few milliamps to work as close as possible to the actual threshold voltage. Owing to the complexity of circuit #1(a current regulation circuit is needed) and the particularity of circuit #2(the grid and the drain electrodes are shorted), when it comes to an actual power electronic converter, they are helpless. In actual applications, online threshold voltage measurement is often realized in two ways: at switching transient and at steady state [19].

A. Measurements During Swithing Transient

The measurement circuit at switching transients is shown in Fig.3. S_1 is an optocoupler and it is driven by the output of DSP and it cannot conduct in reverse. The gate resistor R_{g1} is added to slow down the turn-on process. When V_{th} is measured, S_1 is turned off and the gate charging current flows through R_{g1}. Because R_{g1} is very large, the turn-on process of MOSFET is slowed significantly. During this process, the gate-to-source voltage (V_{gs}) and drain current (I_d) are continuously sampled by the DSP until I_d is greater than zero. The gate-to-source voltage at this transient is identified to be the threshold voltage.

However, this circuit has some disadvantages. This measurement method needs to capture the drain-current rise moment accurately during the turn-on process, which is sensitive to interference. In addition, when the drain current waveform is measured, the measurement range on the oscilloscope must be set wide enough to measure both measuring condition and normal operating current levels. If it is not this case, the characteristics of amplifiers inside the oscilloscope will be distorted, resulting in failure to accurately measure the drain current. Furthermore, the measurement of V_{gs} is not common-grounded with the main circuit of Buck converter which will increase the difficulty of the measurement. Last but not least, this method needs to switch the operating states, which means it is not the truly online measurement. Due to these disadvantages, this circuit is not suitable for online threshold voltage measurement of power MOSFETs in Buck converters.

B. Measurements During a Steady State

Fig.4 shows the circuit for the measurement of threshold voltage at a steady state. A power switch (C_1) is added to momentarily disconnect the power MOSFET from the input voltage during the measurement. The optcoupler (S_2) and the power diode (D_1) are used to link the gate electrode to the

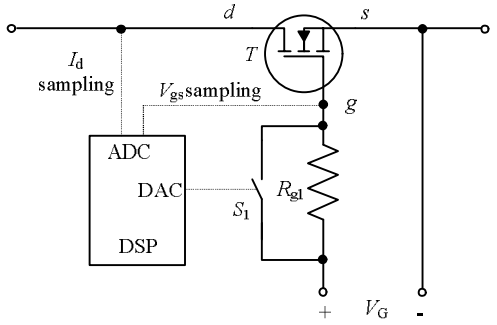


Fig.3. Measurement circuit at switching transients

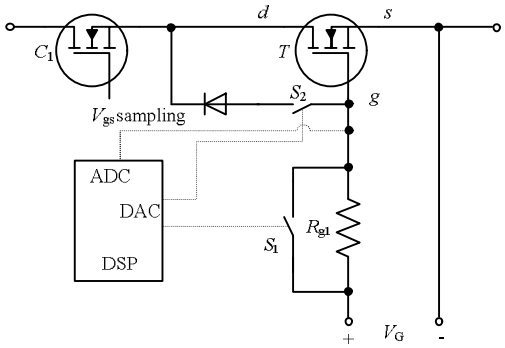


Fig.4. Measurement circuit at a steady state

drain electrode during the measurement of threshold voltage and to disconnect these switches at normal working conditions. During the measurement, the DC link is isolated by controlling C_1 off. With S_1 turned off and S_2 turned on, the small drain current (less than 10 mA) which is determined by R_{g1} is supplied to the MOSFET. The gate-to-source voltage detected under this status is identified as the threshold voltage.

This circuit has a few disadvantages. The introduction of S_2 and D_1 increases the drain-source junction capacitance which will cause additional switching loss. The existence of C_1 in an operating converter will increase the conduction loss. Moreover, too many auxiliary elements (a power switch, an optocoupler, a power diode, etc.) are added, which is no good for improving the reliability or lowering the costs of overall system. Moreover, this method also needs to switch the operating states and thus it is not suitable for Buck converters.

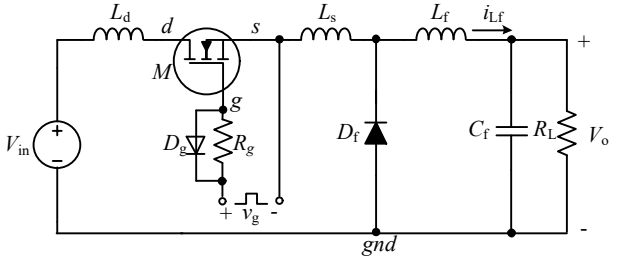


Fig. 5.Buck converter with stray inductances

IV. Proposed Methodology for Threhold Voltage Monitoring

A. Analysis of the turn-on transient

The circuit model of Buck converter considering stray inductances is shown in Fig. 5. All stray inductances in the power loop are lumped and represented by L_d and L_s, which are at the drain and source terminals of the MOSFET. The stray inductances in the branch of the diode D_f is lumped into L_s. The gate inductance is neglected in the analysis because most circuit design guidelines suggest minimizing the potential oscillation introduced by it. The input is a constant voltage source V_{in}, and the output connects to a resistive load R_L. A typical gate drive circuit is constituted of the diode D_g, the gate drive resistance R_g and the drive source v_g that can flip between 0 and V_g. M and D_f are the power MOSFET and the freewheeling diode respectively. L_f is the filter inductor and C_f is the filter capacitor. Fig. 6 illustrates the qualitative turn-on waveforms, which will be thoroughly examined in the following.

Stage 1 [$t_0 - t_1$] turn-on delay time: When the gate signal V_g is applied through R_g, the input capacitance C_{iss} of the MOSFET is charged up. During this stage, the MOSFET works in the cutoff region and the load current still circulates through the diode. Since this stage does not affect the drain current, v_{gs} can be given by

$$v_{gs}(t) = V_g[1 - e^{-(t-t_0)/T_{iss}}] \tag{1}$$

where $T_{iss}=R_gC_{iss}$. The gate-ground voltage v_{g_gnd} can be derived as

$$v_{g\_gnd}(t) = v_{gs}(t) + V_{df(on)} \tag{2}$$

where $V_{df(on)}$ is the voltage drop of the diode D_f.

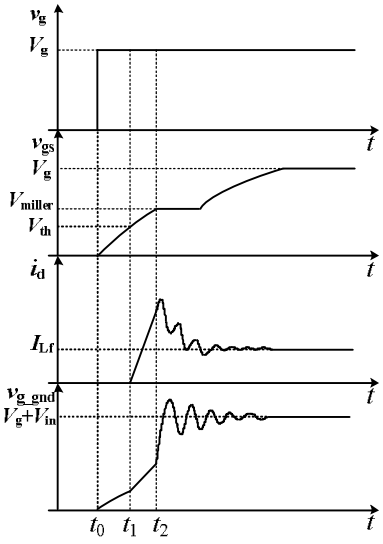


Fig. 6.Qualitative turn-on waveforms

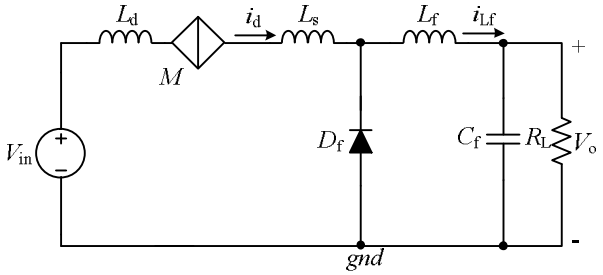


Fig. 7.Equivalent circuit model of state 2

Stage 2 [$t_1 - t_2$] current rise time: In this stage, v_{gs} goes beyond the threshold voltage V_{th} and the drain current i_d starts to increase from zero. As the MOSFET works in the saturation region, where the MOSFET can be equivalent to a controlled current source as shown in Fig. 7, i_d is governed by

$$\begin{aligned} i_d(t) &= \frac{\mu_n C_{ox}}{2}\frac{W}{L}[v_{gs}(t) - V_{th}]^2 \\ &= I_{d0}[\frac{v_{gs}(t)}{V_{th}} - 1]^2 \end{aligned} \tag{3}$$

where μ_n is the electron mobility, C_{ox} is the intrinsic gate oxide capacitance, W/L is the gate width/length ratio, V_{th} is the threshold voltage and I_{d0} is the saturation drain current when $v_{gs}=2\ V_{th}$.

Accordingly, the voltage v_{g_gnd} during this period can be derived as

$$\begin{aligned} v_{g\_gnd}(t) &= v_{gs}(t) + V_{df(on)} + L_s\frac{di_d(t)}{dt} \\ &= v_{gs}(t) + V_{df(on)} + \frac{2I_{d0}L_s[v_{gs}(t) - V_{th}]}{V_{th}^2}\frac{dv_{gs}(t)}{dt} \end{aligned} \tag{4}$$

Furthermore, the voltage slew rate of v_{g_gnd} can be determined

$$\begin{aligned} \frac{dv_{g\_gnd}(t)}{dt} &= \frac{dv_{gs}(t)}{dt} + \frac{2I_{d0}L_s}{V_{th}^2}(\frac{dv_{gs}(t)}{dt})^2 + \\ &\frac{2I_{d0}L_s[v_{gs}(t) - V_{th}]}{V_{th}^2}\frac{d^2v_{gs}(t)}{dt} \end{aligned} \tag{5}$$

It can be seen that an abrupt change in the slew rate of v_{g_gnd} will be observed once v_{gs} reaches V_{th} due to the second item of the equation (5). Therefore, the threshold voltage can be monitored by the capture of this turning point. Though the analysis above is in the case that the converter works in the continuous current mode (CCM), the same conclusion can be drawn in the discontinuous current mode (DCM).

B. Implementation of the turning point extraction strategy

The flowchart of proposed measurement process is illustrated in Fig. 8.

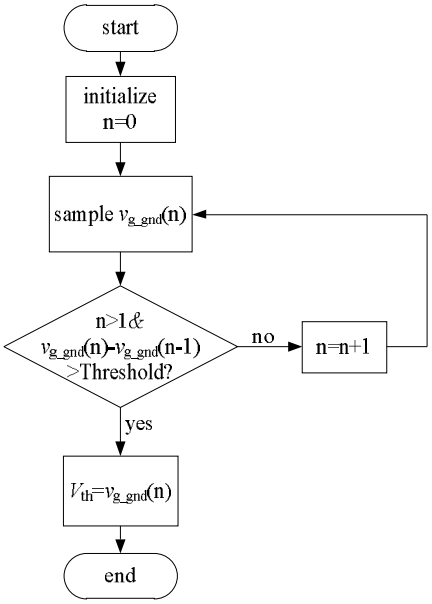


Fig.8. Flowchart of proposed method

The value of "Threshold" can be assigned as

$$\text{Threshold} = A\frac{V_g T_{sam}}{R_g C_{gs}} \tag{6}$$

where T_{sam} is the sample interval, C_{gs} is the gate-source capacitor of measured MOSFET, and A is a constant (greater than 1) determined by the demand of measuring precision. But if C_{gs} cannot be obtained, (6) can also be approximately expressed as

$$\text{Threshold} = Av_{g\_gnd}(t_0) \tag{7}$$

V. Simulation and Experimental Verifiction

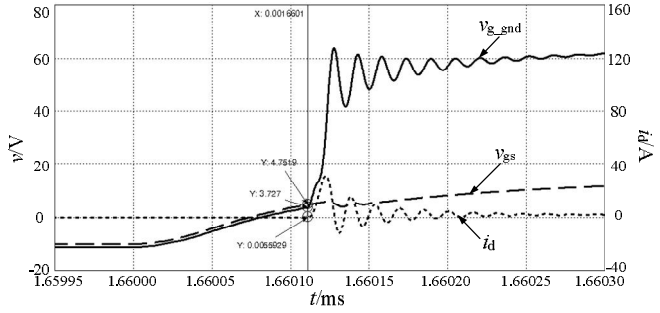
In order to verify the effectiveness of the proposed measurement method, simulation and experimental results are given out in this Section. The parameters used in the simulation and experiment are listed in Table II. The tested MOSFET is IXFK64N50P, and according to the datasheet, its model has been built by the Power MOSFET Tool in SABER. The initial threshold voltage of the created model is 4.35V.

The simulation results are shown in Fig.9. Fig. 9(a) shows the waveforms of v_{g_gnd} ,v_{gs} and i_d, where an abrupt change in slew rate of v_{g_gnd} can be observed clearly when i_d is zero-crossing. Fig. 9(b) shows the waveforms of v_{g_gnd} when the threshold voltage of the MOSFET is set to different values. It can be seen that the shift of the turning point voltage nearly equals the shift the threshold voltage.

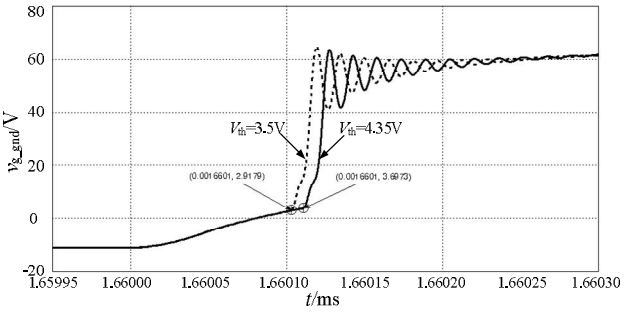
TABLE II
Main Parameters of Circuit

Parameters	Value	Parameters	Value
V_{in}/V	50	L_d/nH	2
V_g/ V	15	C_f / μF	470
R_g/Ω	10	L_f / μH	100
L_d/nH	2	R_L/Ω	10

Fig.10 shows the experimental waveforms of v_{g_gnd}, v_{gs} and i_d, which are consistent with the simulation results. Therefore, shift of the threshold voltage can be monitored by monitoring shift of the turning point voltage.

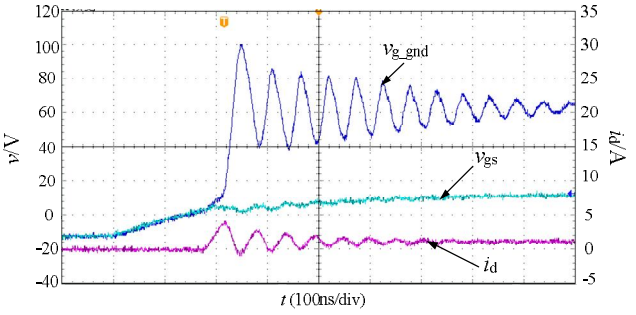


(a)

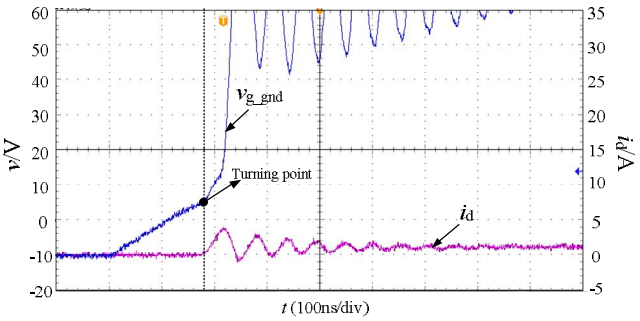


(b)

Fig.9. Simulation results: (a) voltage v_{g_gnd}, voltage v_{gs} and current i_d, (b) voltage v_{g_gnd} of different threshold voltages.



(a)



(b)

Fig.10. Experimental results: (a) voltage v_{g_gnd}, v_{gs} and current i_d, (b) voltage v_{g_gnd} and current i_d with enlarged scale.

VI. Conclusion

The paper has presented a new condition monitoring approach for power semiconductor device reliability in power electronic converters. The novelty lies in the on-line monitoring method of threshold voltage for MOSFETs in Buck converters.

In this paper, the origin of power MOSFET failure and the measurable failure precursors which can quantify the level of aging have been described and one common degradation feature is found: causing the junction temperature to rise. Thus, the junction temperature is chosen as an overall indicator for health monitoring and the threshold voltage is used to be the temperature-sensitive electrical parameter for the condition monitoring of the power MOSFETs. For threshold voltage measurement, two conventional circuits are explained and discussed to illustrate their disadvantages and a new online monitoring method is proposed for Buck converters. The proposed monitoring method utilizes the particular structure of Buck converter, eliminating the need for high-precision current sensor. From the simulation and experimental results, the proposed method is suitable for the real-time temperature estimation of power MOSFETs in Buck converters.

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