Test

Test Actor.lvlib:Test.lvclass:Actor Core.vi C:_work\mops_sam\src\Actors\Test Actor\Test\Actor Core.vi Last modified on 16.10.2019 at 16:44

Printed on 06.12.2019 at 11:19

Test plan							
t Status	Ovenplan						
	Target Name	DUT marking	State	Slot	Load Board	Target FSM	_
	✓ 10.132.112.1	A01	IDLE				
Actions							
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Start Test							
Stop Test							
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