Real-Time Degradation Monitoring of SiC-MOSFETs through Readily Available System Microcontroller

Shi Pu, Enes Ugur and Bilal Akin
Power Electronics and Drives Lab, Electrical and Computer Science Department
The University of Texas at Dallas
Richardson, TX, USA. 75080
Shi.Pu@utdallas.edu

***Abstract*—The goal of this work is to develop a real time degradation monitoring tool for Silicon Carbide (SiC) power MOSFETs. The conventional methods for prognosis and reliability monitoring are mostly based on parametric measurements as on state resistance, threshold voltage, leakage currents etc. The change in switching characteristics of aged devices and the root cause analysis behind this change are also worth exploring for degradation monitoring. In this paper, a real-time monitoring procedure is proposed using readily available system microcontroller. For this purpose, an accelerated aging test bench is utilized to actively swing the junction temperature through power cycles in order to trigger device degradation. A number of parametric measurement results are presented for degradation discussion and turn on time variation are captured by proposed degradation monitoring approach.**

Keywords*—SiC power MOSFET; accelerated aging; switch mechanism; double pulse tester; failure precursor

I. INTRODUCTION

Power converter designs deploying Silicon carbide (SiC) MOSFETs have been undergoing rapidly over the past decade. Compared to conventional Si counterparts, SiC MOSFETs exhibit superior features and enable high temperature operations and high power density applications. Compared to conventional silicon based MOSFETs, SiC MOSFETs can endure high junction temperature and high blocking voltage operation [1]. Although SiC devices exhibit robust features, they are subjected to aging due to electro-thermal stresses, sheer stress and environmental effects. Because of such stress, the remaining lifetime of SiC MOSFET is shortened. Therefore, study of latent failure is crucial for SiC MOSFET operation.

In the literature, there are several studies on Si-MOSFET discussing reliability issues comprehensively. Among the precursors, drain to source resistance ($R_{ds\text{-}on}$) has been commonly studied one which shows a continuously increasing trend during the aging process [2,3]. Also, gate threshold voltage [4], body diode voltage drop [9] and thermal resistance [5] are other proposed precursors which change during thermally triggered aging process. However, since the SiC-MOSFET's substrate is made of SiC material, the difference in thermal expansion coefficients (CTE) between the upper metallization (Al) layer and SiC create sheer stress at different levels. Therefore, $R_{ds\text{-}on}$ shows totally different variation trend during the aging process, so as the other parameters. Hence, it is important to explore aging precursors for SiC MOSFETs to detect device degradation. Different kinds of precursors have been proposed to explore SiC MOSFETs incipient faults [6-9]. Among the proposed precursors, turn off time has been utilized to detect aging for IGBT switches [10]. An advantage of such precursor is that switching waveform is easier to record than electric parameters like $R_{ds\text{-}on}$ and such study is important since switches behavior changing has a direct impact on system efficiency, robust operation and EMI. Thus in this paper, the turn on time variation of SiC MOSFET has been explored and captured by the proposed system.

In Section II, SiC MOSFET switching mechanism is introduced and accelerated aging cycling test is illustrated as background information. Subsequently, proposed turn on time capturing system is elaborated in Section III. Experimental results, parametric measurement and device degradation is discussed. Finally, future work is suggested to enrich the study.

II. BACKGROUND

The SiC MOSFETs switching process is quite similar to Si-based power MOSFETs. A detailed analysis of turn-on process is introduced and corresponding voltage and current values are calculated based on the switch model. Since this study focuses on the turn-on time interval, only the turn-on process is elaborated. However, turn-off behavior can be derived in a similar way.

On the other hand, accelerated power cycling test is a widely used approach to mimic the thermally trigged degradation in practical applications. Therefore, a custom made aging test bench is introduced for SiC MOSFET degradation study.

A. Modeling and analysis for SiC MOSFET turn-on process

A circuit topology of a double pulse tester (DPT) is given in Fig 1. The red part is the commonly used analysis model of SiC MOSFET during operation.

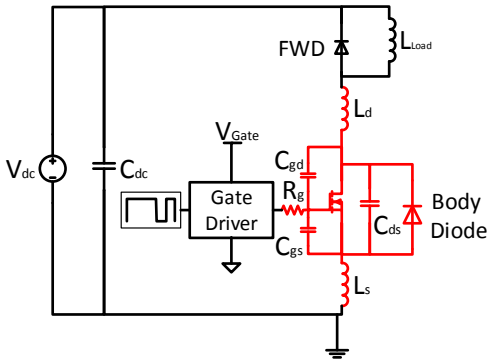


Fig 1. Double Pulse Tester used for hard switching

At high switch speed, stray inductance at drain and source cannot be ignored since high di/dt often generate an unignorable voltage drop on L_d and L_s during switching. Also, parasitic capacitance especially input capacitance (C_{iss}) which include gate to source capacitance (C_{gs}) and gate to drain capacitance (C_{gd}) plays an important role at turn on period.

Four phases are separately defined for the turn on process. Thus, time intervals 1 to 4 are sequentially illustrated. Fig 2 presents the waveform of a typical turn on process of SiC power MOSFETs.

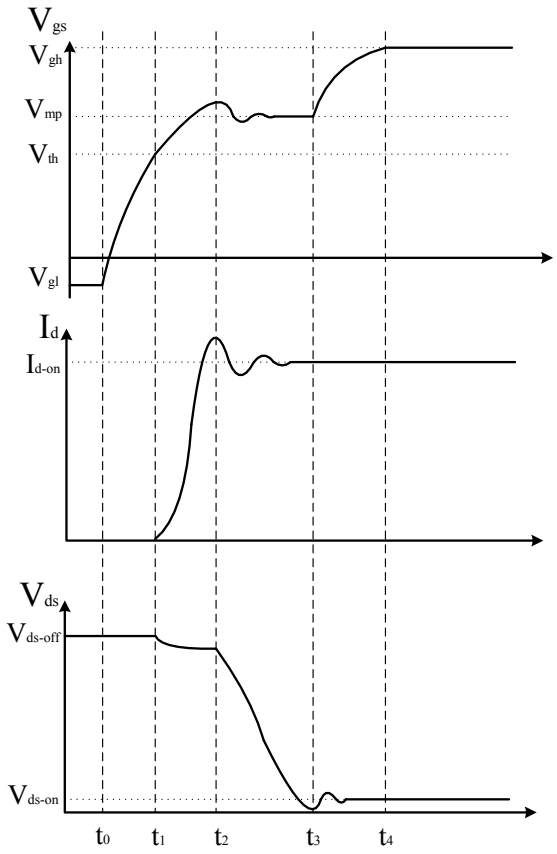


Fig 2. SiC MOSFET switching process waveform

Stage 1(t_0-t_1): In this stage, first of all, gate to source voltage is applied. As well known, during SiC MOSFET gate drive process, a negative voltage is applied to achieve reliable turn off to suppress the dv/dt effect in half bridge configuration [11]. This is mainly because SiC MOSFETs have lower threshold voltage and can easily misconduct due to the switch oscillation and ringing [12]. In this time interval, the input capacitor C_{iss} is gradually charged. V_{gs} has been increased due to the voltage bias at gate. The voltage and current equation of the gate drive loop is given as [13]:

$$I_g = (C_{gs} + C_{gd})\frac{dU_{gs}}{dt} \quad (1)$$

Stage 2(t_1-t_2): At point t_1, gate to source voltage V_{gs} reaches to the threshold voltage V_{th}. Therefore, the drain current starts increasing from 0A. Due to the conducting freewheeling diode, drain to source terminal is still blocked. Therefore, V_{ds} maintains high voltage. The drain current rising in saturation region can be expressed as:

$$I_d = g_m(U_g - U_{th}) \quad (2)$$

The rising slope for the drain current can be obtained by taking the derivative of Eq. (2) as:

$$\frac{dI_d}{dt} = g_m\frac{dV_{gs}}{dt} \quad (3)$$

In this time interval, C_{gs} is charged from V_{th} to V_{mp}. Therefore, the time lenth of stage 2 depends on both charging speed and voltage charging C_{iss}. Considering the gate driver loop:

$$V_{gh} = V_{gs} + R_g I_g + L_s\frac{dI_d}{d_t} \quad (4)$$

Where L_s is the stray inductance of source and C_{iss} is the input capacitance to be charged. Combing equations above, the current rising slope can be deduced as:

$$\frac{dI_d}{dt} = \frac{V_{gh} - \left(\frac{I_d}{g_m} + V_{th}\right)}{R_g\frac{C_{iss}}{g_m} + L_s} \quad (5)$$

According to Eq. (6), variables like threshold voltage, input capacitance and transconductance have direct impact on the charging process, hence needs to be taken into account while considering aging effects. Drain to source voltage also has a slight drop in this stage. Since during the hard switch turn on, high di/dt generate a voltage drop on the stray inductance L_d.

Stage 3(t_2-t_3): The gate voltage reaches to Miller Pleateau region and C_{gd} is positively charged by I_g in the meantime. Due to C_{gd} charging, voltage value across C_{ds} decreases to zero. The value of I_g in stage 3 can be expressed as [14]:

$$I_g = \frac{V_{gh} - V_{mp}}{R_g} = \frac{1}{R_g}\left[V_{gh} - \left(V_{th} + \sqrt{\frac{I_L L_{ch}}{\mu_{ni} C_{ox} Z}}\right)\right] \quad (6)$$

At the end of stage 3, the switch is completely conducts.

Stage 4(t_3-t_4): To guarantee a complete reliable conduction, the gate drive voltage is normally higher than U_{mp}. Therefore, V_{gs} continues to increase and the switch conducts in ohmic region. The turn-on process calls to an end. For partial conclusion, stage 2 is much shorter than stage 3 which means the voltage falling interval occupies most turn on process except stage 4.

B. Accelerated Aging Test Bench

In order to actively swing the junction temperature of DUTs, an accelerated aging bench has been built [15]. The topology of the aging setup is shown in Fig 3.

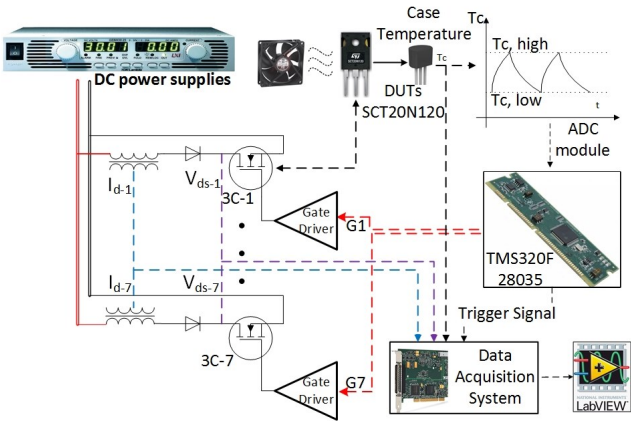


Fig 3. Accelerated aging test bench for DUTs

For each aging channel, DUTs are heated up to 170°C and its temperature is sensed by temperature sensor which is clipped to the surface. Once the case temperature has reached the upper limit, DSP generate an interrupt flag to suspend the conduction of DUTs. In the meantime, a cooling fan is turned on to quickly cool down the switch. After the DUTs' temperature reach below 30°C, the aging cycle restarts and DUTs continue to conduct.

In this study, the measurements are taken at the end of each 250 thermal cycles using curve tracer 1506A – Keysight to observe the changes due to aging.

III. Proposed Degradation Monitoring Approach

According to Eq. (5) and (6), V_{th}, g_m and C_{iss} have an impact on the turn-on period of SiC MOSFET. Therefore, we propose a detection circuit to capture the exact turn on time of SiC MOSFET. The proposed approach is designed based on the topology of DPT and high resolution function of digital signal processor is utilized for measurement.

A. High resolution capture module

Microcontroller Unit (MCU) from Texas Instrument TMS320F28035 provides a high resolution capture module. The capture module can detect rising and falling edge of the input signal at MCU's system clock frequency at 60MHz. This means it can only detect a signal with 16.67ns resolution which is not enough for fast switching edges of SiC MOSFET. High resolution (HR) capture module in C2000 MCU divide each system clock period into 300ps units as shown in Fig 7.

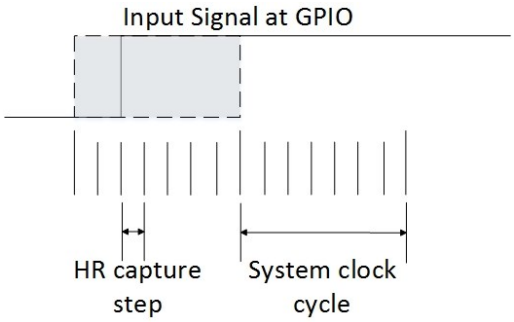


Fig 4. HR capture operation logic

By capture input signal at 300ps precision, the turn on time of DUTs can be more precisely captured. Four functions are provided by HR capture module to measure the time interval length of high pulse width, low pulse width and PWM period. In our approach, high pulse width measurement function is utilized.

B. Proposed real time detection approach

For the double pulse tester we use in this study, two pulses are shoot into the gate of DUT. During the first pulse, DUT is conducted and the input DC voltage is applied fully on the load inductance L_{Load}. The current flowing through L_{Load} rises and its value is equal to the drain current I_d. Thus, the first pulse is a zero current conduction. Subsequently, the second short pulse is applied after a very short time. Since the turn off time is quite short, the current flowing in FWD and L_{Load} nearly remains constant when the first pulse ends. The current value at the second pulse can be calculated by the loading inductor and the time length of the first pulse t_1 as:

$$I_d = I_L = \frac{V_{dc}}{L_{Load}} * t_1 \quad (7)$$

In the test bench, the inductance load is set to be 250μH while t_1, time gap t_g and time interval t_2 equal to 4.85 μs, 0.5μs and 0.5 μs. Thus, what we are focusing on is the turn-on period of the second pulse. The proposed turn-on time detection approach is given in Fig 5.

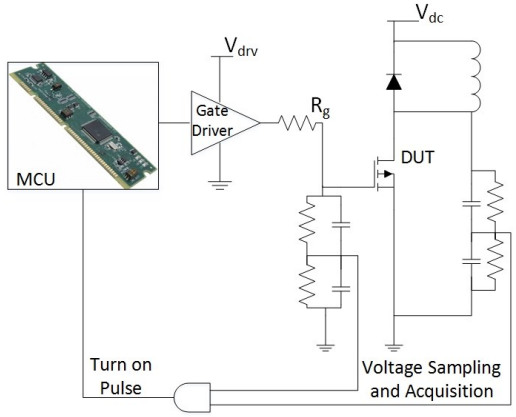


Fig 5. Proposed approach for turn-on time detection

In the proposed circuit, the voltage waveform across C_{ds} is divided by voltage divider circuit and an ultra-high speed AND logic gate is used to obtain the turn-on time pulse. HR capture module is utilized to measure the time interval length of this pulse and for every 400 results captured by MCU, the average value is calculated as the turn-on time of the DUT. This procedure is shown in Fig 6.

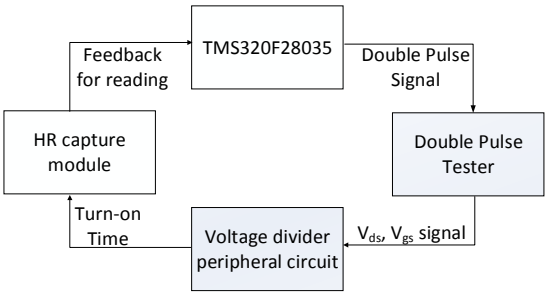


Fig 6. Detection procedure of DUT turn on time

IV. Experimental Results

Parametric measurement result after thermal triggered aging is presented in this section. Subsequently, experimental results of turn on time capturing are obtained. Also the Vds waveform during turn on is plotted for comparison. Subsequently, degradation mechanism is discussed regarding the parameter shift and delay time changing.

A. Parametric measurement results

1506A curve tracer has been used for measuring parameter shifts at room temperature. Fig 7 presents the measuring result of threshold voltage, transconductance and input capacitance.

It can be observed that due to thermal cycling tests, V_{th} increases and transconductance decreases throughout aging. The input capacitance shows slight decrease at low voltage level and at high V_{ds} range.

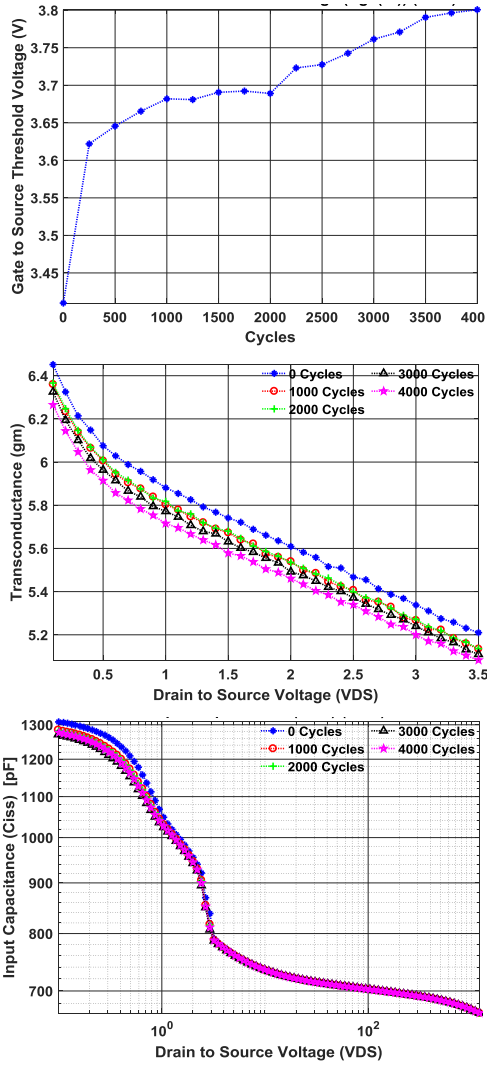
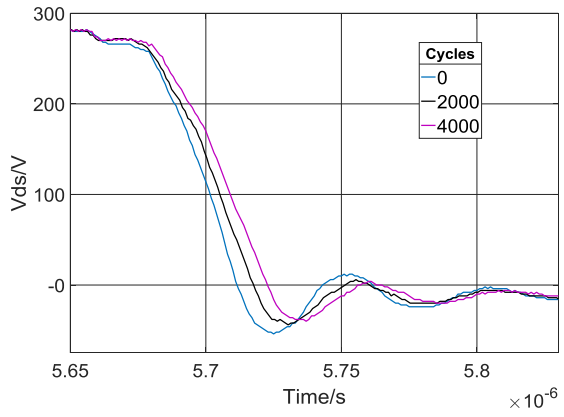


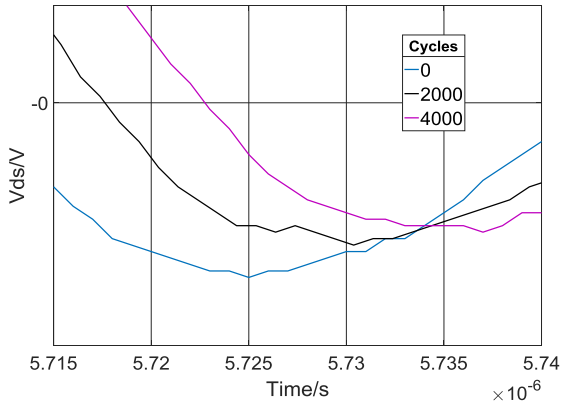
Fig 7. Input capacitance variation throughout aging

B. *Experimental results and turn-on time capture*

V_{ds} falling edge during turn-on is depicted in Fig. 9. Three voltage waveforms at different aging cycles are plotted together to show the V_{ds} time delay during turn on. Fig 9(b) is the zoomed version of Fig 9(a). It can be easily observed that the turn on time of DUT increases after degradation.



(a)



(b)

Fig 9. V_{ds} waveform degradation at turn on

It can be seen that the starting point of voltage fall have a slight time shift. The reason is that due to decreasing transconductance, rising current slope in saturation region decreases. However, it's still a minor difference compared to voltage drop since the rising current time interval only occupies a small portion of the turn on process. A relatively big variation in voltage falling can be observed in the figure. It can be seen that the voltage falling slope increases due to aging and the overshoot and voltage ringing decreases. Fig 10 presents the exact turn on time variation captured by proposed system.

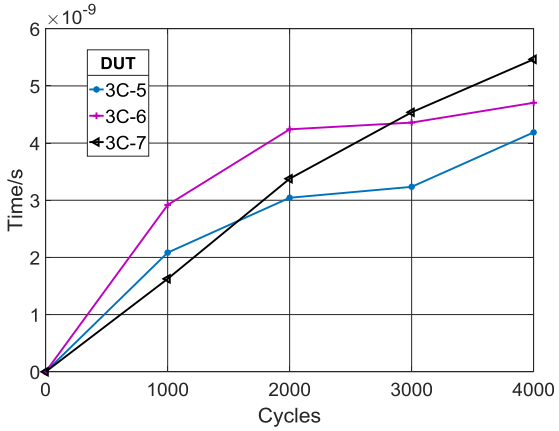


Fig 10. HR capture measurement result

C. *Degradation discussion*

In the falling voltage edge shown in Fig 9, dv/dt increases, means it takes more time for the gate current to fully charge the input capacitor. As discussed in Section II, the turn on process of SiC MOSFET can be modeled as RC charging circuit. Therefore, either the capacitance value increases or the charging current decreases. Fig 7 provides the capacitance value shifts due to aging and it shows that the value of the capacitance doesn't change much at high voltage level and even decreases at low voltage level. This means, the charging current must have been reduced by aging, hence it takes more time to charge the capacitor and the dv/dt is slowed down.

As Eq. (6) implies, with higher threshold voltage, the charging current decreases. Also, the oxide capacitance may also vary by aging. One of the possible reasons in this aging effect thought to be gate oxide degradation. With more traps formed in the gate oxide region, the required voltage to form conduction channel between drain and source may be increased

and since the amount of gate trap increases, the oxide capacitance may also be shifted.

V. Conclusion and Future Work

In this paper we performed a real-time degradation monitoring approach for SiC power MOSFETs. HR capture module in MCU has been utilized to capture the exact turn on time of DUTs. The turn on time of SiC power MOSFETs increases in the order of nanoseconds at room temperature. This degradation can easily be detected by HR capture peripheral which has 150 ps resolution. The double pulse signal is set at ultralow frequency in order to maintain DUTs operating temperature at room temperature so that the temperature dependent variation can be ignored. In the next step, the turn on time variation and parameter shifting at different junction temperatures will be investigated. Also, additional experiment at different voltage and current level needed to ensure the feasibility of this study.

VI. Acknowladgement

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