Analysis on the potential of Silicon Carbide MOSFETs and other innovative semiconductor technologies in the photovoltaic branch

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Keywords

Silicon Carbide, MOSFET, Power semiconductor device, Photovoltaic, Voltage source inverter (VSI).

Abstract

Within the framework of photovoltaic systems connected to the grid, the potential of innovative semiconductor technologies with special focus on SiC devices will be analyzed. The properties of a SiC D-MOSFET will be experimentally examined firstly as a discrete element and then in a laboratory prototype of a highly efficient inverter circuit. The gain on efficiency and possible increase on the switching frequency will be discussed.

Introduction

Innovative semiconductor technologies have found in the photovoltaic branch one of the most favorable market segments, as there can be observed a continuous demand for high performance components mainly justified by the still high price paid per installed system capacity (approximately 4500 €/kWp) [1]. As a consequence, higher efficiency in the energy conversion stage will directly reduce the pay-back time of a system and increase the profitability. An additional characteristic of photovoltaic converters is the fact that 100% of the energy needs to be processed by the power electronics stage, while this value is approximately 33% for double fed induction generators in wind turbines and 10% for variable speed generators in small hydraulic plants [2]. Therefore, investing on the enhancement of the efficiency of photovoltaic power converters will give one of the highest returns among all applications. Of interest are therefore the newest developments regarding semiconductor materials, as operation with reduced losses even at high blocking voltages are becoming more attractive, leading to some changes not only on the choice of topologies by also on the concept of the whole system. Such developments will be discussed in the next items, followed by an evaluation of the possible impact on the referred application. Experimental results will be presented to substantiate the here presented conclusions.

Semiconductor technologies – State-of-the-art

Nowadays, 4H-SiC (along the paper simply referred as SiC) and GaN are the most promising materials in the semiconductors industry, mainly due to some interesting features in relation to Si, as can be observed in Fig. 1.

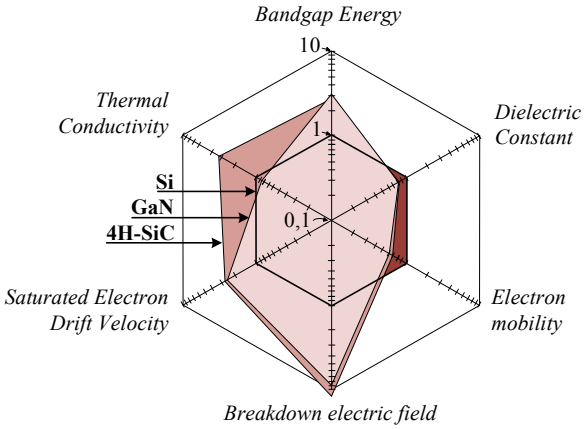

Fig. 1: Key-features of semiconductor materials normalized to the values of Si on a logarithmic scale

One of the most significant features is the very high electric breakdown field that allows thinner and shorter drift layer structures resulting in very low specific on-state resistance values even at higher blocking voltages. Such feature is depicted in Fig. 2 for different switch designs employing the referred technologies.

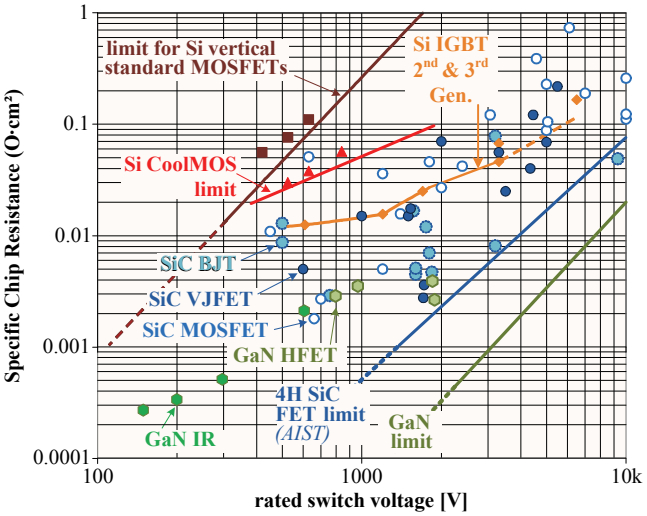

Fig. 2: Key-features of semiconductor materials normalized to the values of Si [2], [3],[4]

For Si IGBTs, it is still possible to achieve reduced conduction losses at high blocking voltages mainly due to the minority carriers' injection, though this comes at the cost of a very inferior dynamic behavior. On the other hand, SiC and GaN devices profit from the superior saturated electron drift velocity that allows an inherently faster dynamic behavior. Though the electron mobility, which is directly related to drift velocity, is inferior for both materials in relation to Si, the non-linear dependence of this value to the electrical field does not allow its use as a benchmarking value regarding the dynamic behavior of the material [5].

A further advantage of the materials is the stable operation at higher temperatures without suffering from intrinsic conduction effects; made possible due to the larger band gap energy value in relation to Si. Still regarding the thermal capability, a significant difference between GaN and SiC is the thermal conductivity, far superior for the last one. In other words, devices made of SiC can dissipate larger amounts of heat even at high temperatures, what is especially attractive in applications oriented to high power density or to harsh ambient conditions like military and space. Finally, another interesting feature of the SiC material is its radiation hardness that is not only advantageous for the applications shortly described, but also for allowing operation nearer the rated blocking voltage without requiring de-rating factors like in normal Si devices.

The presented interesting characteristics come nevertheless at a higher cost per chip area, especially regarding SiC, mainly due to the still low scale of production and the inherent difficulties in obtaining large-area defect-free wafers [6]. On the other hand, approaches with GaN using Si as substrate have the economic advantage, though such hybrid solution loses some of above presented benefits, specially the thermal capability. With this technology, focus has been mainly given to lower blocking voltages [3] with few laboratory investigations with HFET (heterostructure FET) approaching a maximum of 1.8kV [4]. Due to this limitation on the blocking voltage range, this paper will concentrate on SiC devices, as will be discussed on the next item.

Silicon Carbide Switches

The use of the above referred properties of SiC on controllable switches has been pursued in several concepts [7]. Regarding bipolar devices, the Bipolar Junction Transistor (BJT) employing SiC offers an interesting approach, mainly due to the normally-off behavior and low specific on-resistance at blocking voltages up to 10kV. Drawbacks here are the possible bipolar degradation effect that may reduce the current gain of the device, absence of intrinsic diode and the current driven characteristic, demanding a high power driving circuit, what makes its application more interesting at higher voltage and power levels [8].

For the unipolar devices, one first example is the DMOSFET where the MOS channels are constructed through the implanted P-wells, forming a normally-off device. Issues related to such technology are the complex fabrication process and reliability of the gate dielectric material, as the offset of the conduction band between Gate Oxide (SiO_2) and SiC is lower in comparison to the one in Si devices. Improvements on the material technology have nevertheless increased the reliability of the oxide lifetime at temperatures up to 175°C [9], though the maximum junction temperature is still limited by such factor. The last limitation does not apply to lateral channel vertical JFETs (LCVJFET) that avoid the use of Gate Oxide. Such concept rely on epitaxially grown n and p-channels to respectively replace the inversion channel and polysilicon gate of the previous concept, attaining similar or even better values of on-state resistance. A normally-off variant has been demonstrated [10], though more focus has been given to normally-on devices. For all the unipolar devices so far discussed, an intrinsic pn-diode is present on the structure and can be optimized to fulfill either freewheeling or avalanche characteristic, improving robustness and reducing the amount of necessary semiconductors. Simplified design and significant cost reduction can be achieved if a vertical channel is instead applied to the VJFET structure, with the normally-on and -off variants achieving a very low specific on-resistance [ICS7]. Drawbacks now are the absence of the intrinsic diode, the high device sensitivity to process and doping variations making it difficult to obtain reproducible characteristics for normally-off devices. Furthermore, the very low gate threshold voltage on normally-off variants requires special gate circuits to avoid accidental turn-on of the device [11].

Regarding the presented multitude of approaches, one possible way of comparing the concepts is the attained specific on-state resistance as already depicted in Fig. 2, since this value is directly related not only to the chip size and cost of the device but also to the parasitic capacitances. The dynamic behavior can be evaluated by the necessary gate charge, which is directly determines the required gate drive capacity; and the saturation currents, which determine how fast can the parasitic capacitances be charged [7]. One shall nevertheless keep in mind that the comparison may not only rely on these figures of merit (FOM), as it is still necessary to take in consideration the optimum operation range regarding blocking voltage and rated current of each technology and the possible circuit applications regarding specificities like normally-on behavior.

Investigation of the characteristics of a 1200V SiC D-MOSFET

In this paper, the electrical characteristics of a SiC D-MOSFET from the manufacturer CREE rated at 1200V and 20A for a junction temperature of 150°C was examined. The simplified cross-section of the device is depicted below.

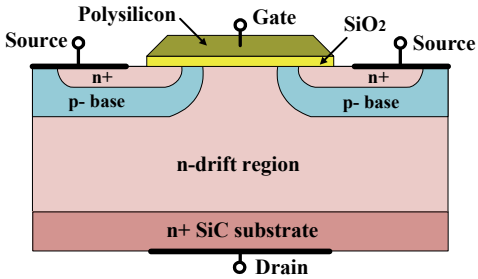

Fig. 3: Structure of the investigated SiC D-MOSFET

Firstly, the dynamic behavior of the device was investigated. For such purpose was employed a commutation cell system with a high measurement bandwidth. This characteristic is important since the transients to be measured take place within tens of nanoseconds. All measurements were performed at 125°C Junction Temperature and with a double pulse procedure. The performance of the MOSFET was compared with a 2nd Generation Trench Gate Field-Stop IGBT rated at 1200V and 25A from the manufacturer Infineon. For the freewheeling of the current, a SiC Diode rated at 20A 1200V was employed so that only the switch characteristics could be evaluated. A gate resistance of 4.1Ω along with a capacitance of 1.5nF were employed for both switches, with a driving voltage of 15V/0V. Below are presented the curves for a blocking voltage of 450V.

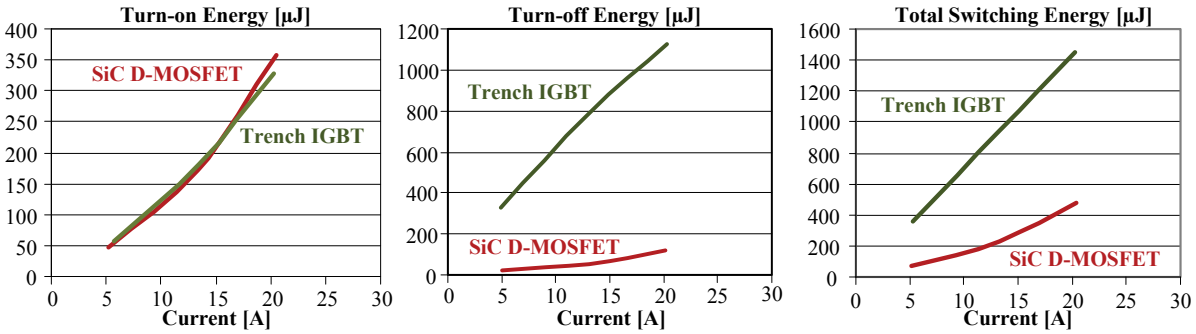

Fig. 4: Turn-on, turn-off and total switching losses at 450V and 125°C for the investigated SiC D-MOSFET and Trench IGBT

The turn-on losses of the devices are practically the same for the given conditions, as reverse recovery losses from the freewheeling diode were not included this time. On the turn-off losses becomes clear the significant advantage of SiC device against the IGBT, as a 90% reduction of the turn-off losses was achieved. The high value for the IGBT can be justified by the tail current that represents the expulsion of the minority carries as the devices blocks. The total switching losses are on the average 75% lower for the MOSFET. Regarding the static behavior, the conduction losses were calculated based on the measured voltage drop during conduction for a junction temperature of 125°C and gate voltage of 15V and are depicted below as an absolute value and normalized to the IGBT values below.

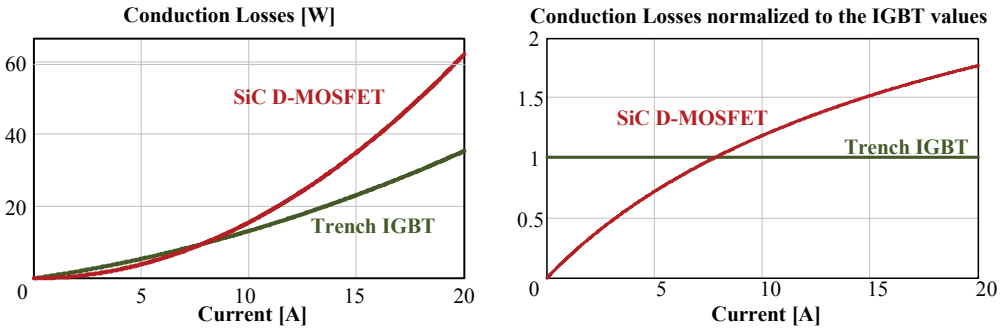

Fig. 5: Calculated conduction losses as a function of the current at 125°C.

The measured value of the on-state resistance of the SiC D-MOSFET was approximately 155mΩ, within the range of COOLMOS® rated at 650V (110 - 160mΩ depending on the generation). This allows the MOSFET to have a competitive behavior regarding conduction losses for almost half of the rated range (at high junction temperature) even when compared with a Trench IGBT.

From the properties of the investigated device one can notice that the focus of this design was not to obtain a better static behavior when compared with a Trench IGBT, since this would increase significantly the cost due to the larger chip area. Instead, it relies on the superior dynamic characteristic to outperform its Si counterpart on the amount of total losses. This nevertheless comes along with high switching speeds, i.e. high values of dV/dt and dI/dt, what may results in problems regarding EMI (electromagnetic interference). As a conclusion, the power board shall be designed with advanced techniques to mitigate the negative effects of such fast transients.

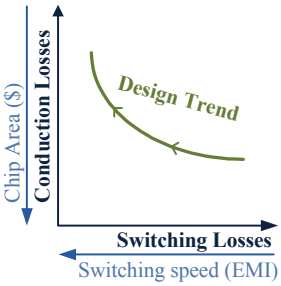

Fig. 6: **T**rend of SiC devices for possible optimizations regarding the conduction and switching losses

Perspectives for SiC devices on power converters for photovoltaic systems

Of interest here is to present some aspects inherent to photovoltaic power converters that may profit from the attractive features of SiC switches. They will be discussed in the following items.

Efficiency

The perspective of increasing the efficiency is especially attractive on the photovoltaic branch due to the still high feed-in tariff values. Taking Germany as an example, an increase of 1% would result in a additional annual revenue of 30 €/kWp (considering an interest rate of 5% for an interval of 10 years), justifying the use of more expensive semiconductor devices. With such increase, commercial inverters that already reach an efficiency of 98% will top 99% within the next few years [12]. Further increase of the efficiency may nevertheless not be cost-effective anymore, so that other features shall also be considered.

Operation at higher switching frequency

To evaluate the potential of the SiC switches for operation at higher switching frequencies, the investigated devices are used as examples. The sum of switching and conduction losses is calculated for a range of frequencies, as depicted in Fig. 7, considering an application of a generic inverter circuit operating with unipolar modulation (H5 or Heric). The switching losses are calculated for the peak currents range (5 – 15A). Meanwhile, conduction losses are calculated by considering a duty cycle of 0,23, which is the average value considering an input voltage of 450V (test conditions) and output at 230V.

From the picture Fig. 7 it is possible to observe that on the lower frequency region where most commercial photovoltaic inverters operate (around 16 kHz), the analyzed SiC D-MOSFET allows a reduction of approximately 42% of the total losses of the referred switch. It is nevertheless possible to observe that the greatest potential for the use of this and other SiC devices lies on the possibility of operating at a higher switching with very little increase on the total amount of losses. This feature allows the reduction of passive elements like output filter by the same order of increase of the frequency, resulting in cost and weight decrease. Operation at very high frequencies may nevertheless be not advantageous for the application, as the complexity of the inductor construction will increase, leading to no further significant cost improvement [13], along with higher losses.

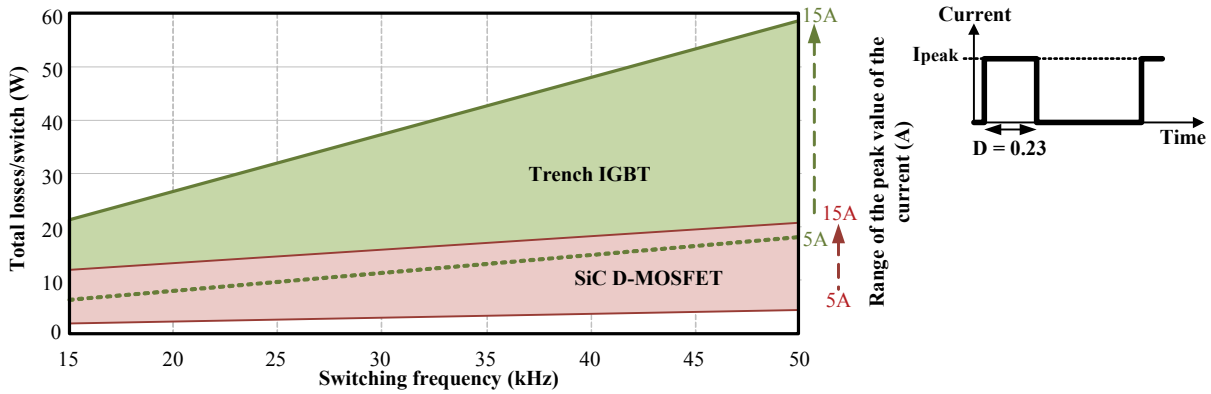

Fig. 7: Total losses per switch for different values of switching frequency and current range

Thermal design

The thermal design can significantly benefit from the features of SiC switches, firstly due to the reduced amount of losses, what results in a lower junction temperature. Also important is the higher thermal conductivity inherent to SiC devices. As an example, the investigated D-MOSFET has a thermal resistance junction to case ($R_{th\text{-}jc}$) equal to 0,4K/W, while this value is equal to 0,65K/W for the Trench IGBT, which has almost the same current rating. For equal case-to-sink thermal resistance values (0,25K/W), this can be translated into a 27% lower heat sink temperature for a certain level of losses. Considering an application with only such switches, the possible reduction of the thermal-resistance of the heat-sink is depicted on the left side of Fig. 8, as a function of the ambient and heat-sink temperatures for the case of the IGBT. The potential of reducing the thermal-resistance of the heat-sink can be directly translated as a reduction on the weight (as illustrated on the right side of Fig. 8) and consequently costs.

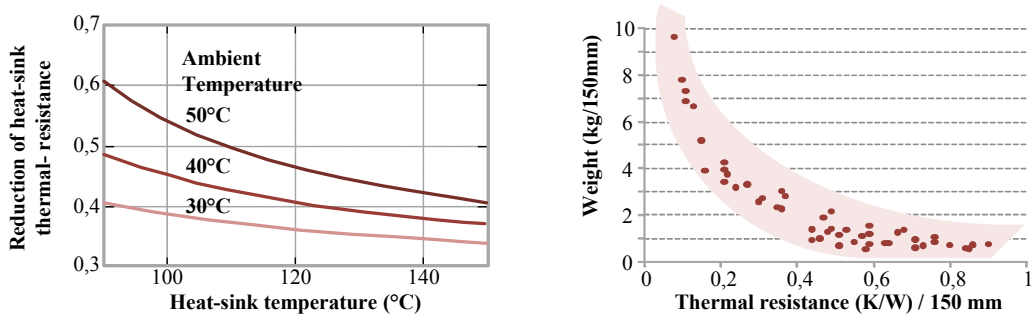

Fig. 8: Possible reduction of the heat-sink thermal resistance and relation between specific weight and thermal resistance for different aluminum heat-sinks (Aavid Thermalloy)

Maximum input voltage level and system concept

Regarding the system concept, one significant step towards higher efficiency was made by eliminating the low frequency transformer on the output that also provided step-up to the low-voltage grid level. As a direct consequence, a higher DC link voltage was required resulting in higher voltage stress across the semiconductors, what is especially critical in three-phase applications in Europe, where a single-stage solution would result in input voltage values higher than 1000V. In this case, one solution is relying on the association of at least three single-phase inverters feeding the three-phase grid forming the so-called mini-central concept [1]. Another possibility is employing a DC-DC converter to regulate the input voltage for an optimal operation of three-phase circuit and to ensure that the PV-array voltage will not exceed 1000V, what is for the time being the maximum allowed value. Discussions are nevertheless being made in Europe to increase this level to 1500V [14] especially for high power applications, as a significant reduction of the conduction losses on the cables and economy of cooper may be possible. In the case of the US where the maximum voltage against the ground is 600V, concepts where the middle point of the array is grounded, allowing a level of 1200V, are also under discussion.

Under such framework, the perspective given by SiC switches of operating with high efficiency even at higher blocking voltages gives at least two possible indicatives for future applications. Concerning the system concept, the possibility of constructing high efficient single-stage circuits for three-phase systems will allow simplification of the design along with reduction of costs and losses. Regarding the suitable topologies, multilevel circuits that have in recent years attracted significant attention due to the possibility of dividing the total voltage stress by associating the switches in series (NPC would be an example) could be substituted by a simple three-phase bridge, what would allow a reduction of costs and complexity.

Input MPP voltage range

Another important characteristic to be considered in photovoltaic systems is the broad input voltage range, normally denominated as MPP (maximum power point) voltage range. The lower limit is commonly related to the maximum by a factor between 0.6 and 0.7. The distribution of energy along this range is mainly influence by the local ambient temperature, installation conditions and cell technology. An example of such distribution is illustrated in Fig. 9 for two crystalline module technologies in Germany. For locations with higher ambient temperature, the curves will move to the left.

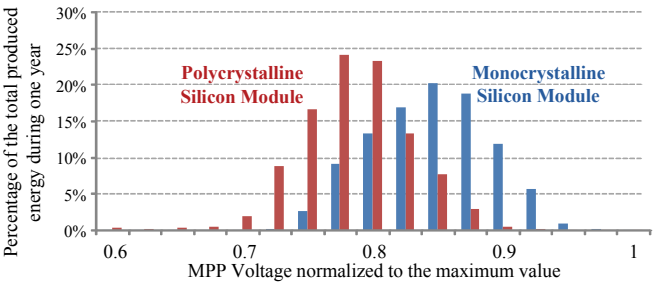

Fig. 9: Distribution of the annual produced energy for modules with different crystalline silicon technologies as a function of the normalized MPP voltage (ISET-LAB)

Of interest is therefore to obtain a high efficiency not on the minimal MPP voltage but rather on a higher range of input voltage. On most inverter circuits, as the input voltage increases, the tendency for the efficiency is to decrease. The first reason for such behavior is the higher difference between input and output voltages, resulting in a higher flux swing on the output filters and consequently increased core losses. Depending on the employed freewheeling diodes (SiC diodes have a slightly higher saturation voltage in comparison to Si variants), conduction losses may increase, as freewheeling will be more frequent. More significant than these factors is the increase on the switching losses, which happens almost directly proportional to the increase of the input voltage. The application of SiC switches with superior switching behavior will therefore reduce the dependency of the efficiency on the value of the input voltage.

Experimental investigation on an inverter circuit

In order to evaluate the potential of not only the SiC D-MOSFET but also other semiconductor devices in a real application, a highly efficient single-phase single-stage inverter circuit was built for such purpose. The basic principle of operation relies on two paralleled step-down converters that modulate a rectified sinusoidal current, with the output connected to the load using opposite polarities. The circuit was obtained by modifying the power flow direction on one of the circuits proposed in [15]. From the two possible variants of the circuits discussed in details in [16], the one presented in Fig. 10 was investigated; where the components of each step-down converter responsible for the positive and negative half waves can be respectively identified as T_1-L_1-D_1-T_3 and T_2-L_2-D_2-T_4. V_{pv} represents a photovoltaic array as the input source and V_g the utility grid in the output. D_3 and D_4 are clamp-diodes to protect the switches located on the grid side against possible transients.

A first advantage of the proposed circuit is the possibility of operating with a single high frequency switch (T_1 or T_2) at a time what significantly reduces the switching losses. The fact that the

freewheeling diodes (D_1 or D_2) are separated from the switches allows the use of optimized technologies. The other switches (T_3 and T_4) are under a voltage stress equal to the grid voltage and operate only at grid frequency, so that they can be further optimized for reduced conduction losses. Since the positive terminal of the PV-array is either directly connected to the phase output during the positive half-wave and to the neutral during the negative half-wave; not only are high frequency oscillations and consequently leakage currents avoided, but also the negative voltage gradient across the cell is well suited for application with back-side contact cells [17]. A laboratory prototype of the circuit presented above was constructed with a nominal power of 4,5kW, input voltage range of 375-600V, output 230V± 10%, switching frequency at 16 kHz and output filter equal to 3mH.

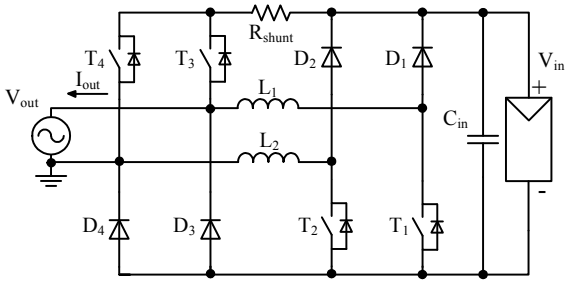

Fig. 10: Investigated inverter circuit

Experimental results with different semiconductor technologies

Tests were performed with the circuit proposed on the previous item with different semiconductor configurations. An important remark at this point is that the objective of the investigation was to evaluate the potential of the different semiconductor configurations under equal conditions. For such purpose, all measurements were done with resistive load rather than directly feeding the grid, so that the influence of the changing grid voltage would not affect the results [18]. In addition, the measured efficiency considers only the power stage, without any external power supply; since these remain practically the same for all configurations. Only the power required by the gate drivers may change depending on the chosen semiconductor (gate charge value), switching frequency and speed; though increases well below 0.15W were observed and hence considered as non-significant on the rated power level.

For each configuration, the efficiency measurement was performed with a wide-band precision power analyzer LEM Norma D-6000, at three-different voltage levels. The first one was the minimum specified MPP voltage, in this case 375V, as with this value the highest level of efficiency is attained. More significant are nevertheless the levels at 435V and 500V, as already discussed in Fig. 9, where most of the produced energy from the PV-array is obtained. On the table below are summarized the tested configurations, as the obtained gain in the European efficiency relative to the previous configuration is depicted in Fig. 11.

Table I: Tested semiconductor configurations

	T1 – T2	T3 – T4	D1 – D2
1	Trench IGBT 1stG 25A/1200V	Trench IGBT 1st G 30A/600V	Stealth Diode 30A/ 1200V
2	Trench IGBT 1stG 25A/1200V	2nd G CoolMOS 38A/650V	Stealth Diode 30A/ 1200V
3	Trench IGBT 1stG 25A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V
4	Trench IGBT 2ndG 25A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V
5	SiC D-MOSFET 20A/1200V	2nd G CoolMOS 38A/650V	SiC Diode 20A/1200V

The configuration 1 was taken as a reference measurement. With the configuration 2 was evaluated the possible optimization of the switches T_3-T_4. For the rated current values, the lowest possible conduction losses were achieved with the CoolMOS, mainly due to the absence of the saturation voltage, as an increase of approximately 0,35% was obtained for the most significant voltage levels. A less expensive alternative would be employing low-frequency IGBTs that are optimized for low voltage drop. The lower increase for $365V_{DC}$ can be justified by the lower ripple content on the current

through the switch. The adoption of SiC diodes in the 3rd configuration provided a gain of approximately 0,275%, mainly justified by the absence of reverse recovery and consequently reduced switching losses. The lower increase for higher input voltages can be justified by the higher conduction losses of the SiC diodes in relation to the Si ones; what is especially critical in higher input voltages, when freewheeling is more frequent. The implementation of a trench-field-stop IGBT of the 2nd generation having an improved dynamic behavior in comparison with the 1st generation resulted in an increase of approximately 0,19% on the European Efficiency.

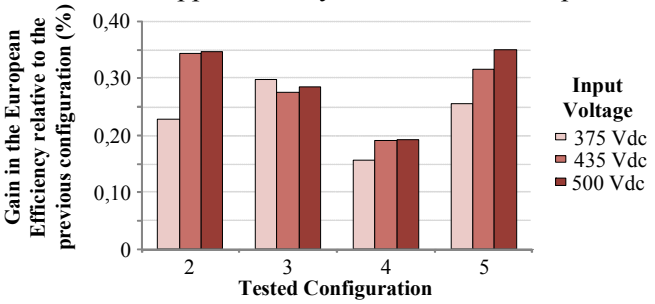

Fig. 11: Gain in the European Efficiency relative to the previous configuration for different input voltage levels

The adoption of the SiC D-MOSFET allowed a further increase of approximately 0,32% over the already high efficient 2nd generation Trench IGBT and 0,5% if compared with the 1st Trench generation. The higher gain for the most superior voltage levels is another interesting feature for the application of the device, mainly justified by the fast dynamic behavior. Still regarding the very low switching losses of the device, the potential of operating with the double of the switching frequency (32 kHz) and using only half of the previous output filters was investigated. On the table below is presented the attained European efficiency values not only for this but also for the other configurations. Here becomes evident the potential of applying SiC devices at higher frequencies for reducing the size and cost of the output filter of an inverter and still maintaining a high level of efficiency.

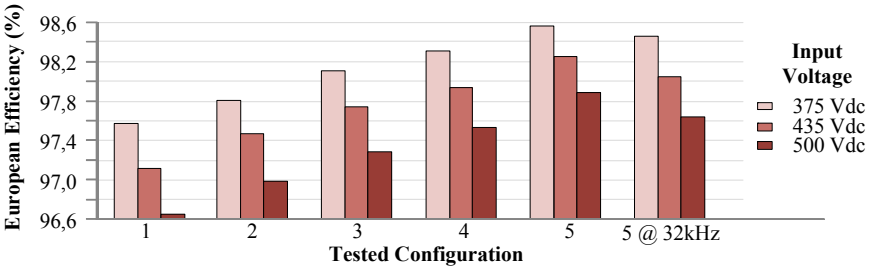

Fig. 12: Measured European efficiency values for the different configurations

To further illustrate the results, the obtained efficiency curves are presented below as a function of the input power.

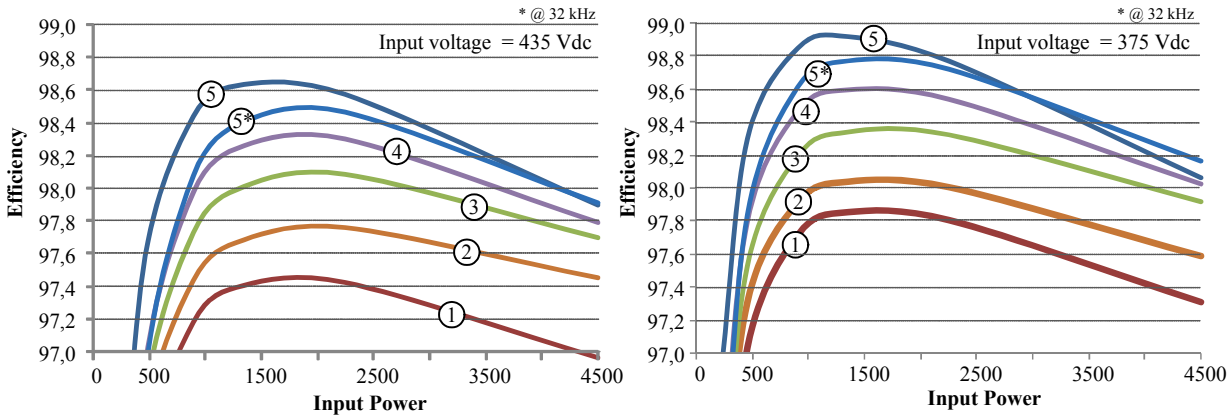

Fig. 13: Measured efficiency as a function of the input power for the different configurations given in Table I

Conclusion

The use of 4H-SiC in semiconductor devices can be seen as one of the most significant developments in power electronics in recent years. Following the commercial introduction of diodes employing such technology, a significant deal of research has been focused on the development of active switches, as the very interesting properties of SiC allow highly efficient operation even at higher blocking voltages. One first clear potential is therefore increasing the efficiency of existing designs, what is especially attractive in photovoltaic systems. But enhancing such value beyond 99% is not cost-effective, so that it becomes necessary to explore the potential offered by SiC to reduce the cost of the periphery of the circuit. One first possibility is operating at higher switching frequency and still attaining a high efficiency; what serves as an indicative of possible decrease of passive elements like output filter. Photovoltaic inverters could therefore leave the low switching frequency of 16 kHz behind and move towards more compact designs. The size of the heat-sink can also be significantly reduced given the superior thermal capabilities of SiC, so that a further decrease of weight and cost could be achieved. All those possible gains need in the end to be weighted in relation to the still high cost of SiC devices so that a breakthrough for the implementation of the technology can be achieved.

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