High Input Impedance ADC Driver with Error Compensation

S. J. Petričević, P. Mihailović, M. Barjaktarović, J. Radunović

Abstract – A novel high impedance JFET high voltage follower combined with ADC driver and a dedicated error compensation feedback is discussed in this paper. Proposed circuit builds around required ADC driver and its transfer curve by adding few low cost components to turn it into a high impedance input ADC driver with high voltage capability and error compensation ability. Such a circuit is applicable in instrumentation dedicated to voltage measurement.

I. Introduction

High input impedance followers are an important class of amplifiers often used in various instrumentation devices. JFETs are seen as a good choice for an active component of a follower stage since they provide excellent bandwidth, minimal noise and very low input (gate) currents. Conventional follower is biased using a current source and loaded with resistive load. Regardless of a type of transistor used for a follower, there remains a problem of linearity (distortion in frequency domain) that originates from non linear current-voltage relationships of transistors. Direct effect of this is a voltage difference between the follower input and output (voltage error) that is a function of input voltage. By using large bias currents and high impedance loads this can be minimized, but only to a limited level. If low power consumption is also required from a follower this option is not available and further solutions must be investigated.

Voltage followers continue to be investigated in contemporary literature for audio or instrumentation purposes [1]-[4]. Instruments dedicated to general voltage measurement require a high impedance buffer in order to impose minimal loading of the test point yet must be able to cover large voltage range (few tens of volts) with low noise and acceptable error (or distortion from audio application perspective).

A promising option is available when follower output voltage must be made compatible with input voltage ranges of AD converters, typically in a volt range. Since most ADC require low impedance drivers to pump charge into sample/hold capacitors, an operational amplifier is used in inverting configuration to attenuate the voltage signal and drive the ADC. This signal can be used to modulate current bias of a follower to provide compensation for the follower voltage error with only a few additional components. Such a solution is presented in the paper and elaborated using LTSpice.

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II. Compensation Method

Basic idea behind error compensation is to modulate the FET source current in such a manner to negate effect of input voltage to v_{GS} voltage. A general scheme is presented in fig. 1 where a JFET follower (transistor J1) is driving an inverting attenuator that drives the input to an analog to digital converter (ADC). This ADC input voltage (v_{ADC}) is taken as an input to an arbitrary current source B1 and is used as an argument of a function that defines the source current.

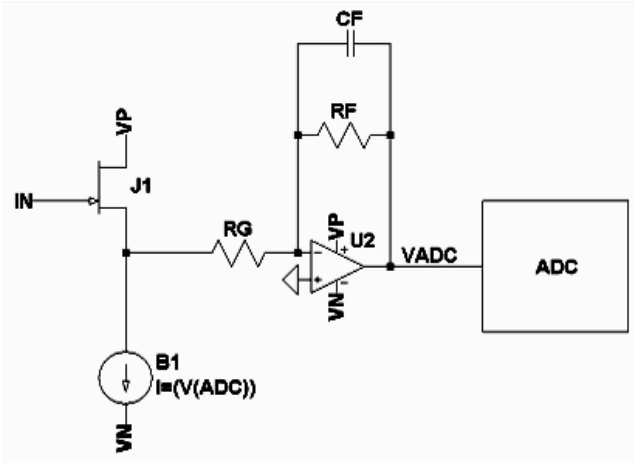

Fig. 1. The proposed topology.

Since the FET is operating in the saturation region the source current can be expressed as

$$i_S = i_{RG} + i_{B1} \simeq i_D = I_{SS}\left(1-\frac{v_{GS}}{V_P}\right)^2\left(1+\lambda v_{DS}\right) \quad (1)$$

One may reason that solving Eq. 1 for v_{GS} might give good insight into required i_{B1} modulation, but it would unfortunately prove to be a fruitless effort. Since Eq. 1 is non linear, so would be the formula expressing i_{B1} (the one controlling the B1 current source) and such functions are difficult to implement in analog electronic circuits. Elements used to implement such a function (current mirrors) would introduce additional non linearity that would cause exact solutions unusable.

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Given previous remarks one approaches the problem form minimal component count perspective to reduce price and complexity of the design. It is reasonable to assume that the current flowing thru resistor R_G should be compensated for in the B1 generator (its current reduced by equal amount) since it flows from JFET source and as a component of i_S causes a change in v_{GS} and thus an error.

What is not immediately obvious from the schematic is the presence of additional loading on the source from small signal model resistance r_{ds} and current source output resistance r_O in parallel with R_G. Thus total loading on the source r_s is expressed as

$$r_s = \left(R_G^{-1} + r_O^{-1} + r_{ds}^{-1} \right)^{-1} \tag{2}$$

It is the change in source current caused by this load that needs to be compensated for in order to reduce v_{GS} changes. This compensation of the first order will prove to reduce the error by sufficient amount. Since the input to the current source is taken from ADC input where signal amplitude is at -20 dB to input, on estimates the B1 current modulation to be

$$i_{cQ1} = \frac{10 v_{adc}}{r_s} = v_{adc} / \frac{r_s}{10} \tag{3}$$

One additional point is worth nothing. Almost all ADCs on the market are of single supply type, requiring input voltage to be of positive polarity. This means that the zero voltage level must be shifted up, typically in a range of one volt or so. The driver must allow for this, in spite of additional complications to the circuit. This best way to accomplish this shift is to make the I_S bias value (dc component) to have a negative V_{GS} (V_S shifted up) by a required amount. This makes it easier to design the op amp stage, since equal amount of voltage applied to op amp plus input (*VCM*) balances the circuit.

III. The Proposed Driver

The proposed ADC driver with error compensation is presented in fig. 2. Component choice is a straight forward business. Since op amp (U1) operates as an attenuator, its performance in ac domain is not critical. Neither is offset voltage important since the error it introduces can be compensated in digital domain by subtracting the value obtained by calibration. If one chooses a n type JFET (J1, type BF256A in the circuit) that requires a small drain current (in the order of milliamps) the circuits both low power operation and also does not place any constraints on the op amp output current limiting. The circuit uses Universal OpAmp2 model from LTSpice, since it provides easy access to major characteristic values, but can be substituted by almost any conventional op amp. In fact, the op amp should be chosen to satisfy ADC driving requirements.

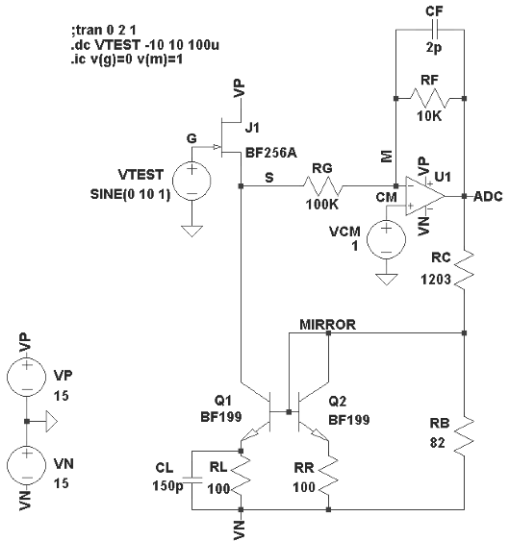

Fig. 2. The proposed driver.

For component and model values in fig. 2 (r_{ds}=37.5 kΩ, r_O=85.3 kΩ) one finds r_s=20 kΩ and from Eq. 3 $_{icQ1}$=0.5 mA. This current is provided by compensation resistance R_C that modulates the current mirror input current. Since v_{adc}=1 V then R_C should be about 2 kΩ but there is also some small signal variation at mirror input (due to RB and finite mirror input resistance) that requires lower value for R_C. After some experimenting an optimal value of 1203 Ω was found to cause minimum error.

Due to large voltage span across R_C, its DC current is found as

$$I_{R_C} = \frac{V_{CM} - V_N - 0.9V}{1200\Omega} = 12.58mA \tag{4}$$

This current, if reflected by mirror, would cause JFET to have a V_{GS} different from projected -1 V required for shifting. Thus a resistor R_B is placed across mirror input to bleed the mirror input current by

$$I_{R_B} = \frac{V_{MIRROR} - V_N}{R_B} = 11mA \tag{5}$$

Thus bringing the mirror output current to the required level of 1.58 mA.

IV. Simulation Results

Fig. 3 present result for v_{GS} obtained by DC sweeping the driver input (gate) from -10 V to +10 V (x axis). Total error is less than 1 mV (about 850 µV) which is better than 1:20000 resolution, or around 14 bits of accuracy from ADC perspective.

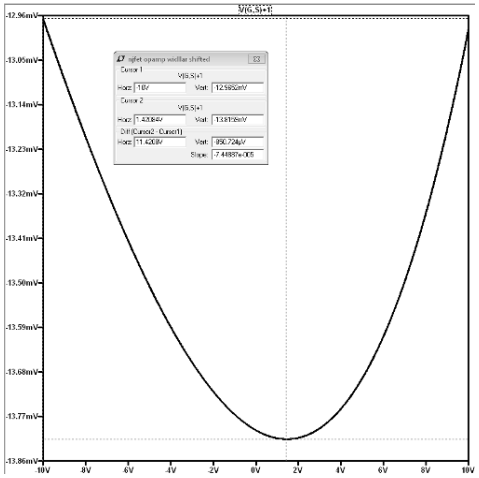

Fig. 3. Voltage v_{GS} obtained by DC sweeping of the driver.

Uncompensated JFET follower loaded with 100 KΩ resistor exhibits an error of some 140 mV, 150 times more than compensated driver.

In the frequency domain the driver behaves well due to inherent large bandwidth of the common drain amplifier (follower) as seen in fig. 4. Bandwidth at the ADC input is dominated by the op amp bandwidth (GBW of the op amp is 10 MHz) with follower showing some peaking.

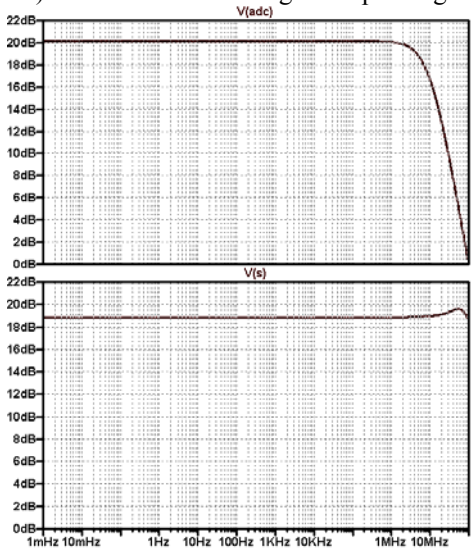

Fig. 4. Driver and follower AC response.

Noise spectral density at the ADC input is also low at some 13.7 nV/√Hz (fig. 5) with total rms noise voltage of 35 µV over the entire bandwidth. This puts the estimated noise pp voltage at 250 µV and SNR at 1:30000 (almost 15 bits of effective resolution).

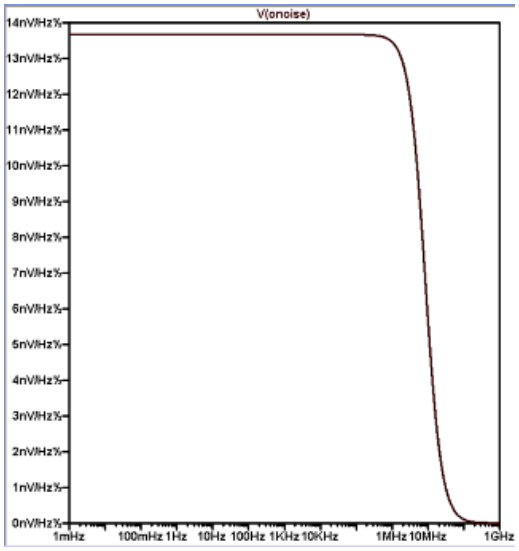

Fig. 5. Driver AC noise spectral density at the ADC input.

V. Conclusion

Simple and low cost extension to an ADC driver has been proposed to turn it into a high impedance, large bandwidth, low noise buffer with large voltage swing. Error caused by JFET non linearity is compensated by a feedback taken from ADC driver output that modulates the JFET polarization current. This compensation reduces the error 150 times to provide 14 bits of error free resolution and SNR of almost 15 bits with no reduction in bandwidth.

Acknowledgement

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