

# *In-situ Prognostic Method of Power MOSFET Based on Miller Effect*

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**Abstract**—Power MOSFET plays an important role in power electronic systems, the failure of which will lead to system losing functions. Thus the degradation failure process and mechanism of MOSFET attract wide attention of scholars. However current research works cannot solve the real time degradation monitoring problem of MOSFET. Normally, MOSFET should be removed from the system for testing or monitoring. This paper presents a new in-situ prognosis method for MOSFET based on miller effect. According to the theory analysis, simulation and experiment results, the miller platform voltage is identified as a new degradation precursor. Then, particle filter algorithm is used for MOSFET remaining useful life (RUL) prediction based on the degradation data of miller platform voltage. Meanwhile, MOSFET samples with different degradation levels are formed by “overstress of gate bias” accelerating life test. The samples are placed into application circuit for the monitoring and extraction of miller platform voltage, so as to verify the method proposed in this paper.

**Keywords**—Power MOSFET; prognostics; miller effect

## I. INTRODUCTION

Power MOSFET has become a crucial component in most power electronic circuits, including the circuits of hybrid electric car, aerospace power equipment, because of its high switching speed and well thermal stability [1]. With the development of microelectronic components manufacture methods, the thickness of the gate oxide and length of channel decrease gradually, which improve the dynamic characteristic and reduce the power loss and cost significantly. While such improvement will make MOSFET more sensitive to hot carrier injection (HCI) and radiation, and the oxide-trapped charge and interface traps will be much heavier. These two types of damage will accumulate and eventually cause MOSFET losing its gate voltage controllability and system losing functions. The statistical data show that power MOSFET has a high failure rate only lower than electrolytic capacitor among all components in power electronic circuits [2]. Thus, the failure problems of power MOSFET attract wide attentions in the past years.

Currently, the researches on MOSFET failure problem can be generally categorized into two types. The first one is physics of failure (POF) based, scanning electron microscopy (SEM), electron spin resonance (ESR), spin-dependent recombination (SDR) et al are used to investigate and analyze

the damage or degradation of inner structure and material of MOSFET [3-6]. The second one concentrates on the analysis of degradation process and failure mechanism by monitoring the electrical or thermal precursor parameters. For power MOSFET, normally, the threshold voltage, channel resistance and transconductance are monitored as precursor parameters [7-10], based on which the remaining useful life (RUL) can be estimated. For the two above researches, the first one is destructive physical analysis, which will destruct the MOSFET. While normally the second one should remove MOSFET from the application circuits and measure with power device analyzer. The above mentioned research can reveal the failure process and mechanism of MOSFET, which is very important for the reliability improvement of MOSFET. However, the real time monitoring of MOSFET degradation is still a problem, namely, the degradation information of MOSFET can't be obtained without removing it from the operating circuit. Therefore, some scholars try to use the testable outputs of the circuit, to study the degradation of MOSFET with parameter identification methods [11]. Parameter identification methods have better testability, however the training process needs enormous amount of data, and the measurement of output parameters will be affected by various stress and noise. So the identification method sometimes is too complicated to be used in real system.

In this paper, a new prognosis method for power MOSFET based on miller effect is presented. The turn-on waveform especially the miller platform is studied and the relationship between miller platform voltage and threshold voltage are revealed. The miller platform voltage is identified as a new precursor. Based on the testing data of miller platform, particle filter algorithm is used to predict the RUL of MOSFET in operation circuit.

## II. THE PLATFORM PHENOMENON OF MOSFET $V_{GS}$

### A. Miller Effect Analysis

For semiconductor components, the equivalent capacitance between input and output terminals will be amplified due to the amplifier, this is called miller effect.  $C_{gd}$  is the so-called miller capacitance of power MOSFET.  $C_{gd}$  will change significantly during the turn-on process, and this kind of change surely will influence the turn-on characteristic of

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MOSFET [12]. Basically the turn-on process of MOSFET can be separated into the 4 phases, as shown in Fig. 1.

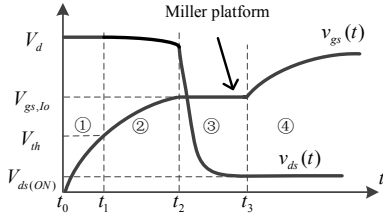


Fig. 1. Turn-on waveforms of the MOSFET.

1) The gate drive voltage steps from zero to  $V_{GG}$  at  $t_0$ . From  $t_0$  to  $t_1$ , gate current (drive current) flows through  $C_{gd}$ ,  $C_{gs}$  and charge them, which will make the gate-source voltage  $V_{gs}$  rise.  $V_{gs}$  will reach  $V_{th}$  at  $t_1$ . In this period, the channel will be closed because  $V_{gs}$  is smaller than  $V_{th}$ . MOSFET works in cutoff region.

2)  $V_{gs}$  keeps rising after  $t_1$ , then the channel opens and the MOSFET comes into the active region<sup>[12]</sup>.  $i_g$  rises rapidly along with the increase of  $V_{gs}$ , and  $V_{ds}$  decreases gradually. The miller capacitance increases due to the change of  $V_{ds}$ . In this period, only few of gate current flows into channel through miller capacitor.

3) From  $t_2$  to  $t_3$ , MOSFET moves its work point from active region to variable resistance region. In this period, most or possibly all  $i_g$  flows into  $C_{gd}$ .  $V_{gs}$  will stay temporarily around  $V_{gs,Lo}$ , or rise slowly.  $I_o$  is the maximum of load current.

4) At  $t_3$ ,  $V_{ds}$  drops to the on-state value which can be estimated as (1). Then  $V_{gs}$  will keep rising until reach  $V_{GG}$ .

$$V_{ds(on)} = I_o \times R_{ds(on)} \quad (1)$$

According to the above analysis, the platform (miller platform in Fig. 1) voltage  $V_{gs,Lo}$  is related with  $V_{th}$  and  $I_o$ , as shown in (2).

$$V_{gs,Lo} = V_{th} + I_o / gm \quad (2)$$

During the degradation process of MOSFET,  $gm$  changes slightly, and can be regarded as a constant.  $I_o$  is also a constant when the application circuit is confirmed. Therefore,  $V_{th}$  can be estimated with  $V_{gs,Lo}$ . When a MOSFET is in the circuit,  $V_{th}$  is unmeasurable, instead  $V_{gs,Lo}$  is testable. So, the degradation of  $V_{th}$  can be monitored indirectly with  $V_{gs,Lo}$ .

#### B. Effect of Load Type on MOSFET Miller Platform

The typical types of load in MOSFET application circuits are resistive load and inductive load. In the test of this paper, MOSFET is connected to resistive load. While in switch mode power supply (SMPS), the equivalent load connecting to MOSFET is inductive. The miller platform will reveal different characteristics in different load conditions. Fig. 2 shows the simulation result of miller platform in inductive condition and resistive condition respectively. Fig. 2b shows that load current is still raising during the miller effect period in resistive condition. It will shorten the duration of miller

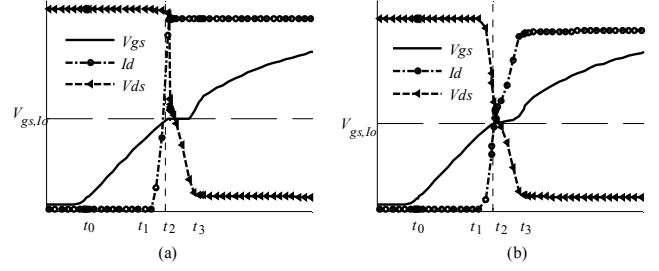


Fig. 2. Turn-on waveforms of the MOSFET: (a) with inductive load and (b) with resistive load.

platform, and slope the platform slightly. Thus it can be seen that the method proposed in this paper will get a better effect when using in inductive load circuits (e.g. SMPS circuit).

It should be noted that in the application of SMPS, constraint by the choosing of inductance, the load current will not be an ideal constant. So the miller platform will not reveal accurately when the maximum load current comes. So (2) should be modified as the following equation:

$$V_{gs,Lo} = V_{th} + \delta I_o / gm \quad (3)$$

### III. THRESHOLD VOLTAGE DEGRADATION AND IN-SITU MONITORING METHOD

#### A. Degradation Simulation

According to the relationship between miller platform voltage and threshold voltage, the miller platform voltage may shift, since the MOSFET degradation can cause the threshold voltage shift. To verify this suppose, PSpice is used to simulate the degradation. MOSFET degradation can be simulated by changing threshold voltage parameter with Model Editor in PSpice. Fig. 3 shows that the degradation process of miller platform voltage is similar to that of threshold voltage. Therefore the miller platform voltage can be used to evaluate the shift level of threshold voltage, and then the degradation level of MOSFET.

#### B. Accelerated Degradation Experiment

The accelerated degradation experiment are carried out on IRF530N. It has an initial threshold voltage of 3V, thus the failure threshold can be set at 4.5V [1]. The literature [7] presented that the oxide-trapped charge and interface traps will appear under the gate bias overstress condition. The oxide-trapped charge will lead the threshold voltage decrease, and the interface traps will lead the threshold voltage increase. During the incipient degradation period, the oxide-trapped charge will firstly appear which will lead the threshold voltage decrease slightly. As the oxide-trapped charge accumulates, the interface traps then appear and gradually dominant the voltage shift. So the threshold voltage will increase eventually.

MOSFET accelerated degradation circuit is shown in Fig. 4. Referring to the literatures [1, 7], the stress condition of  $V_{gs}=50V$  and  $V_{ds}=0V$  is selected to accelerate the MOSFET

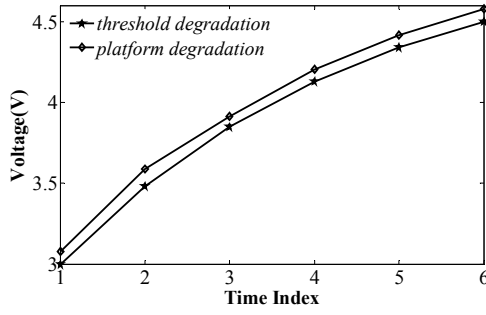


Fig. 3. Threshold voltage and platform voltage degradation curve.

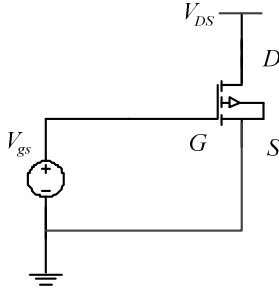


Fig. 4. MOSFET accelerated degradation circuit.

degradation. Each degradation experiment will hold for ten minutes, and parameters will be measured after that. There will be a certain recovery effect on threshold voltage. So the monitored MOSFET parameters should be measured immediately after the end of each degradation period to minimize the recovery time. Parameter measurement includes two parts: threshold voltage measurement and miller platform voltage measurement. The ten minutes' degradation and measurement will cycle until the measurement value of threshold voltage goes beyond its threshold value of 4.5V.

- Threshold voltage measurement.

Threshold voltage can be measured easily by Agilent B1505A power device analyzer. Fig. 5 shows series of transfer curves measured by analyzer during the MOSFET degradation process. The rising parts of each curve are basically parallel, which means the transconductance changes slightly. A set of threshold voltage values extracted from transfer curves are plotted in Fig. 6.

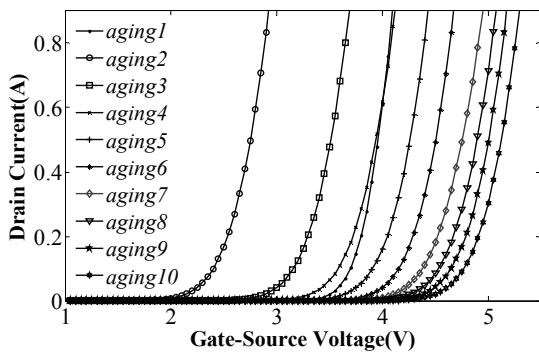


Fig. 5. Degradation of transfer curve.

- Miller platform voltage measurement

An application circuit for power MOSFET shown in Fig. 7 is carried out to demonstrate the measurement and extraction method of miller platform voltage. The circuit driven by an optocoupler works at 10KHz. The load is resistive with a maximum current at 1A and the peak voltage of drive signal is 10V. The in-situ monitor point is set at gate of MOSFET, and the drive waveform in Fig. 8 is captured. After denoising the waveform with MATLAB, the second derivation of waveform is calculated. Then the time  $t$  referring to the maximum value of second deviation of waveform is found. The miller platform voltage is defined as the value of drive signal at time  $t$ . The platform voltage degradation curve shows in Fig. 9.

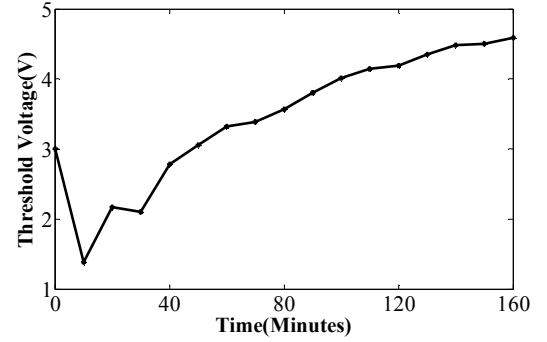


Fig. 6. Threshold voltage degradation curve.

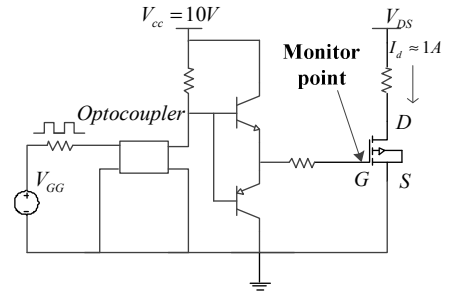


Fig. 7. MOSFET application circuit.

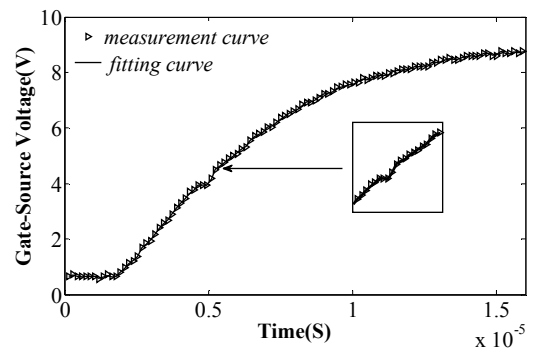


Fig. 8. Turn-on waveforms of MOSFET from real circuit.

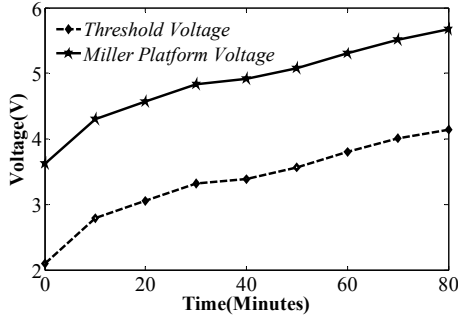


Fig. 9. Waveforms of platforms shift from real circuit.

#### IV. MOSFET RUL PREDICTION BASED ON PARTICLE FILTER

Particle filter algorithm can be used in remaining useful life (RUL) prediction, which has been widely used in maneuvering target tracking and fault diagnosis of complex industrial processes. The algorithm can be presented mathematically as follows:

$$x_k = f(x_{k-1}, w_k) \quad (4)$$

$$y_k = h(x_k, v_k) \quad (5)$$

Where (4) is the state equation, (5) is the observation equation,  $x$  represents the state,  $y$  is the measurement,  $w$  and  $v$  denote the process noise and observation noise respectively. The prognostic method includes two parts.

The first part estimates the miller platform voltage degradation model and the approximate range of initial values of model parameters. Four MOSFET components are monitored in accelerated degradation experiments. The pow-law model, exponential model and logarithmic model are compared in curve fitting part. To get better fitting result, the drop phase at the beginning of degradation is ignored. The residual sum of squares of fitting with each type is shown in Table I.

TABLE I. COMPARISON OF RESIDUALS WITH DIFFERENT DEGRADATION MODELS

Residual Sum of Squares	Degradation Model		
	$a+bx^c$	$a+bx e^{ct}$	$a+\ln(bxt+c)$
#1	0.0056	0.0870	0.0207
#2	0.0062	0.0947	0.0296
#3	0.0386	0.0710	0.0422
#4	0.0354	0.1191	0.2180

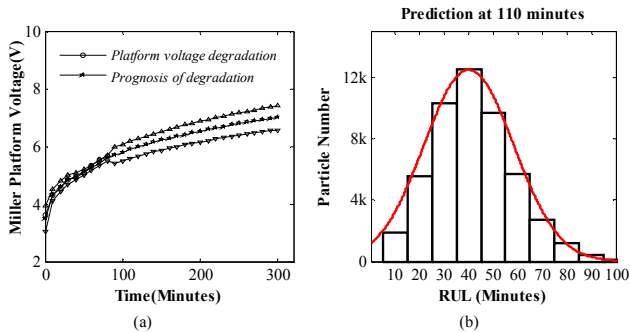


Fig. 10. (a) Prognosis curve based on particle filter and (b) Estimate result of RUL.

#### V. CONCLUSION

This paper presents a degradation monitoring and RUL prediction method of power MOSFET based on miller effect.

- The results of theory analysis, simulation and measurement all reveal that miller platform can reflect the shift of threshold voltage. In the accelerated degradation experiments of power MOSFET IRF530N, the degradation trend of miller platform voltage is coincident with that of threshold voltage.
- The accelerated degradation of power MOSFET can be achieved effectively by magnifying the gate bias voltage. In the experiments of IRF530N, the threshold voltage increases to its failure threshold after 150 minutes' experiment under the degradation condition of  $V_{th}=50V$ ,  $V_{ds}=0V$ . In the accelerated degradation process, threshold voltage decreases for a short time, and then increases gradually. It is coincident with the results from literature [7].
- Particle filter can update the particles importance weights according to the measurement data. It is an effective method for RUL prediction of MOSFET.
- In the future, some other MOSFET application circuits (e.g. SMPS system) will be tested to study the scope of the miller effect based methods. The recovery effect will also be studied further.

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#### REFERENCES

- [1] J. R. Celaya, P. Wysocki, V. Vashchenko, "Accelerated aging system for prognostics of power semiconductor devices," AUTOTESTCON, 2010 IEEE. IEEE, 2010, pp. 1–6, 2010.
- [2] Department of Defense, MIL-HDBK-217F, Military Handbook-Reliability prediction of electronic equipment, USA: Department of Defense, 1995.
- [3] J. P. Campbell, P. M. Lenahan, A. T. Krishnan, "Observations of NBTI-induced atomic-scale defects," Device and Materials reliability, IEEE Transactions on, vol.6, no.2, pp. 117–122, 2006.
- [4] S. Mahapatra, K. P. Bharath, M. A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-MOSFETs," Electron Devices, IEEE Transactions on, vol.51, no.9, pp. 1371–1379, 2004.
- [5] R. Ranjan, K. L. Pey, C. H. Tung, "Failure defects observed in post-breakdown high- $\kappa$ /metal gate stack MOSFET," Reliability Physics Symposium Proceedings, 2006. IEEE, 2006, pp. 590–594, 2006.
- [6] L. J. Tang, K. L. Pey, C. H. Tung, "Gate dielectric-breakdown-induced microstructural damage in MOSFETs," Device and Materials Reliability, IEEE Transactions on, vol.4, no.1, pp. 38–45, 2004.
- [7] N. Stojadinovic, I. Manic, V. Davidovic, "Effects of electrical stressing in power VDMOSFETs," Microelectronics Reliability, vol.45, no.1, pp. 115–122, 2005.
- [8] Celaya, J. R., Saxena, A., Saha, S., "Prognostics of power MOSFET," Power Semiconductor Devices and ICs (ISPSD), 2011 IEEE 23rd International Symposium on. IEEE, 2011, pp. 160–163, 2011.

- [9] Celaya, J. R., Saxena, A., Kulkarni, C. S., "Prognostics approach for power MOSFET under thermal-stress aging," Reliability and Maintainability Symposium (RAMS), 2012 Proceedings-Annual. IEEE, 2012, pp. 1-6, 2012.
- [10] Rodriguez, M. A., Claudio, A., Theilliol, D., "A new fault detection technique for IGBT based on gate voltage monitoring," Power Electronics Specialists Conference, 2007. *PESC 2007*. IEEE, 2007, pp. 1001-1005, 2007.
- [11] Zheng, X. Y., Wu, L. F., Guan, Y., "A research of on-line parameter identification of MOSFET on-resistance based on hybrid system and Kalman filter," Control and Decision Conference (CCDC), 2013 25th Chinese. IEEE, 2013, pp. 1883-1887, 2013.
- [12] Mohan, N., Undeland, T. M., "Power electronics: converters, applications, and design," John Wiley & Sons, 2007.