In-situ condition monitoring system to study the ageing of power semi-conductor devices in photovoltaic inverters

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Summary / Abstract

This paper presents a new method for in-situ condition monitoring of semi-conductor devices, in photovoltaic DC/AC inverters. It consists on measuring the voltage drop across the Collector-Emitter junction, the dynamic resistance and the thermal impedance of each device. Using this method, the monitoring can be done without disconnecting the drivers, neither the DC-link capacitors, nor the DC-link bus. Moreover, the condition monitoring is done under the actual DC-link voltage, hence there is no need for an independent current source. This method was tested in an accelerated ageing test bench, and validated by comparison with classical measurement tests. In addition, examples of condition monitoring implementation in DC/AC photovoltaic inverters are finally proposed.

1 Introduction

In photovoltaic (PV) systems, the DC/AC inverter has the highest failure rate, and the anticipation of its breakdowns is still difficult [1]. Thus, it is crucial to determine the main failure modes of its semi-conductor devices, and particularly, the related electrical indicators. Generally, the condition monitoring of power semiconductors can be partially done by measuring periodically these electrical indicators. The monitoring can be done by measuring the Collector-Emitter voltage V_{ce} in the case of IGBTs, the Drain-Source voltage V_{DS} in the case of MOSFETs, and the forward voltage V_f in the case of diodes. This method is well known in the literature [2] [3] [4] [5] [6], where the ageing monitoring is done periodically in an accelerated ageing test bench, directly after each accelerated ageing phase. Conversely, the monitoring of these electrical parameters can be done online, during the functioning of the inverter, as proposed by Ruiz de Vega et al. [7].

On the other hand, an increase of this voltage under given current and temperature, of between few percent to 20% (mostly 5%), is considered to be an indicator of the power module ageing. Usually, that can indicate wire bonding lift-off, or a reconstruction of the metallization surface.
Moreover, another damage indicator of the power modules is the increase in their thermal impedance Z_{th}. Nowadays, this parameter is calculated especially from the active part temperatures that are estimated conventionally, by injecting a constant current in each semi-conductor device, provided by an external current source. The calculation of the thermal impedance is often carried out during the cooling phase, after switching off the current source.
Usually, an increase of about 20% of this parameter is considered as an indicator of the soldering and/or substrate fatigue. However, this method widely presented in the literature [8] [9] [10] [11] requires a total disconnection of the characterized semi-conductor device from the rest of the inverter, and needs an independent high current source.

Thus, this paper proposes a novel method for measuring the thermal impedance of semi-conductor devices of DC/AC PV inverters, without disconnecting the devices, and without any external high current source. Moreover, this method allows for the measurement of the semi-conductor's dynamic resistance r_d, in the case of IGBTs and diodes. The methodology will be first presented, then the in-situ thermal impedance measurement method will be validated. Finally, several implementation examples in PV inverters will be proposed.

2 General methodology

The method proposed in this paper consists in monitoring the state of health of semi-conductor devices under conditions of use. The monitoring is done periodically between two phases of operative production, in the case of photovoltaic inverters, and between two phases of accelerated ageing in the case of a power cycling test (using the opposition method). Usually, the power cycling using the opposition method, allows the ageing of the devices in conditions close to the application: the semi-conductor devices are used in switching conditions and work under nominal conditions [12] [13].

Now in order to depict the principle of this method, let's consider the case of its implementation in an advanced power cycling test bench using the opposition method, with an accelerated ageing profile representative of the photovoltaic application, as presented in [14].
The electrical diagram of the ageing test bench is based on a single phase inverter feeding a pure inductive load (**Figure 1**). In this first version of the test bench, the pow-

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er switches are IGBT power modules (Semikron - *SKM200GB12E4)*. As shown in **Figure 2** and as proposed by [2] and [7], this inverter is successively used for monitoring the health status of the semi-conductor devices, and for accelerating their ageing. When a damage indicator crosses a damage threshold, the ageing is stopped. A relaxation phase is added between the production/ageing and the monitoring phases, by stopping the inverter during several tens of minutes in order to decrease the temperature of the devices [15] [16].

In this setup, the condition monitoring phase allows for an in-situ measurement of three damage indicators of each semiconductor device. The first ageing indicator is the Collector-Emitter voltage V_{ce} for IGBTs and the forward voltage V_f for diodes. The second indicator is the dynamic resistance r_d, and the third one is the thermal impedance Z_{th}. Actually, the two novelties presented in this paper are the in-situ measurement of both the thermal impedance and the dynamic resistance of the power devices.

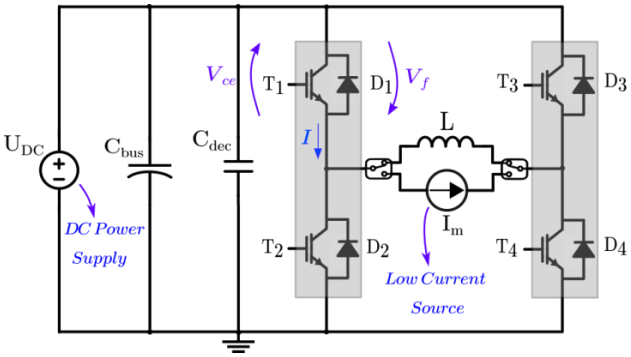

Figure 1 Schematic of the power inverter

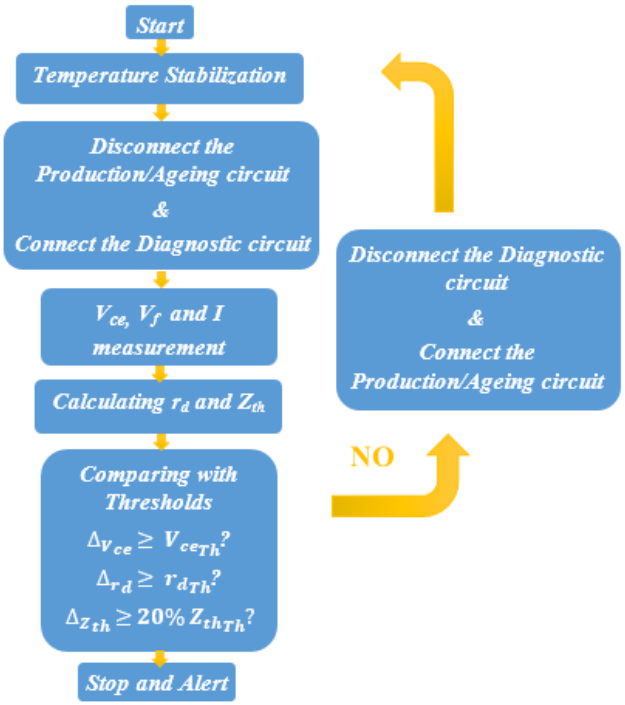

Figure 2 General principle of the proposed condition monitoring method

3 In-situ condition monitoring

3.1 Methodology

During the monitoring phase, four monitoring configurations are successively applied, to characterize the damage indicators of four couples of devices: (T_1, D_3), (T_2, D_4), (T_3, D_1) and (T_4, D_2) (cf **Figure 1**). For example, the monitoring cycle presented in **Figure 3** is used to characterize (T_1, D_3). Now in order to simplify the depiction of the method, only the estimation of IGBT T_1 damage indicators will be presented.

First, the V_{ce} value under a low current of 100 mA is measured to estimate the junction temperature $T_{J_{start}}$ of the IGBT, just before the high current injection. For this measurement, T_1 and T_3 are in on-state and T_2 and T_4 are in off-state. After a while, T_4 is turned-on (and T_3 turned-off), which leads to a rise of the load's current. Then, after several tens of µs, T_4 is turned-off, which results in a slow decrease of the V_{ce} voltage, allowing the measurement of the first damage indicator V_{ce} under high current. **Figure 4** shows that V_{ce} and the current are measured twice successively, which allows for an estimation of the IGBT dynamic resistance r_d as following:

$$r_d = \frac{V_{ce0} - V_{ce1}}{I_0 - I_1} \quad (1)$$

Note that r_d is monitored, since it should be more sensitive to the wire bonding degradation than V_{ce}. After a while, the high current in the transistor is canceled by turning-on T_3 and T_2, and then the voltage V_{ce} can be measured under an injected current of 100 mA. Thus, the junction temperature after the current injection $T_{J_{end}}$ can be estimated, and then used to calculate a thermal impedance value:

$$Z_{th} = \frac{T_{J_{end}} - T_{J_{start}}}{P} \quad (2)$$

where P is the mean power dissipated by the IGBT during the current injection, and can be hence estimated by multiplying $V_{ce\,High\ Current}$ by $I_{High\ Current}$ (**Figure 4**). Note that the power varies with time during the current injection, since V_{ce} is temperature dependent [17]. However, this phenomenon is not considered in this setup, since the objective is not to measure the exact thermal impedance value, but rather its increase with time.

For D_3, the estimation of the power loss is a bit more complicated, since it switches during the monitoring cycle. Switching losses are thus added to conduction losses using current measurements and switching energies from manufacturer datasheets

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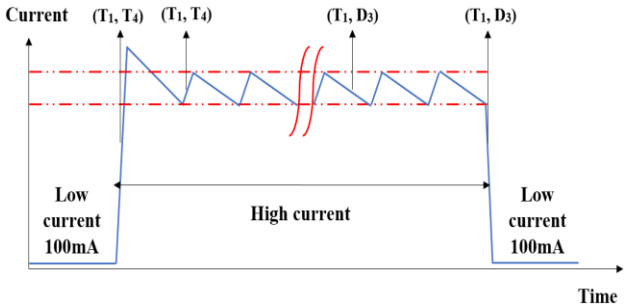

Figure 3 Monitoring cycle for (T1, D3) (typical waveform)

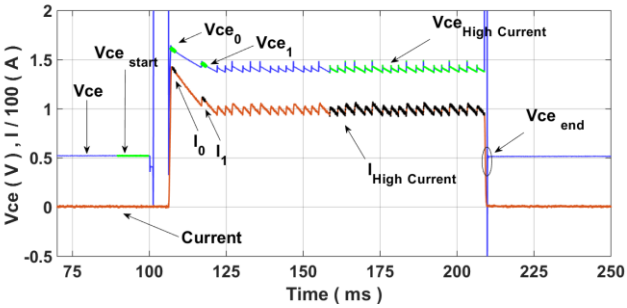

Figure 4 Monitoring cycle for (T1, D3) (real measurements)

3.2 TSEP measurement and calibration

According to Eq. 2, the semi-conductors' junction temperature should be determined, in order to calculate the thermal impedances of the system. However, since the direct measurement of this temperature during semiconductor conduction is still complicated, it was estimated using a thermo-sensitive electrical parameter (TSEP) [9] [18] as it was shown in the previous paragraph. This TSEP is the Collector-Emitter voltage V_{ce} under a low current of 100mA for the IGBTs. Similarly, the TSEP for the diodes is the forward voltage V_f measured under the same current level.

A calibration step is used to determine the relationship between the TSEP and the semi-conductor's junction temperature. During the calibration phase, the system's temperature is fixed by a water-cooled heat sink. At thermal equilibrium, it is assumed that the semi-conductors' junction temperature is equal to the heat sink temperature ($T_J = T_H$), measured with T-type thermocouples. To do the measurements, the cold plate was drilled at different positions, corresponding to the locations of the center of each semi-conductor chips, then thermocouples were inserted in the drilled holes. Finally, after the insertion of the thermocouples, the holes were sealed with an Ag-filled glue [17] [19]. **Figure 5** represents the drilled cold plate, with 16 thermocouples inserted under the center of the chips.

In order to obtain the relationship between the junction temperature and the TSEP, the cooling fluid temperature was fixed respectively at $30°C, 50°C, 70°C, 90°C$ and $100°C$. Once the thermal equilibrium was considered to be achieved (in approximately 30 $mins$), the TSEP was measured for each referenced temperature.
Accordingly, **Figure 6** represents the resulting graph of the Collector-Emitter voltage V_{ce} of T_1 as a function of the junction temperature.

Since the transition between the high current and the low current is not instantaneous, the value of the TSEP measured directly after the current injection, should not be used to estimate the junction temperature. Consequently, an extrapolation is essential to estimate the junction temperature TJ_{end} before the current fall, as that the T_J decreases sharply within the first few μs after the switching [8] [9] [11].

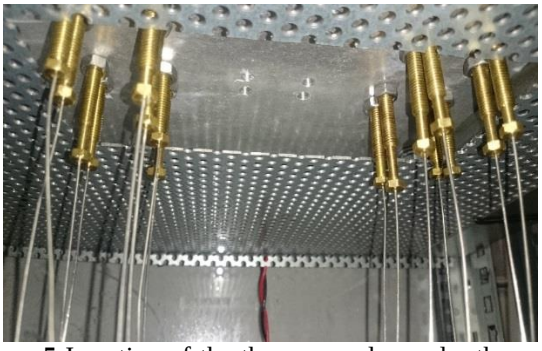

Figure 5 Insertion of the thermocouples under the center of the chips positions

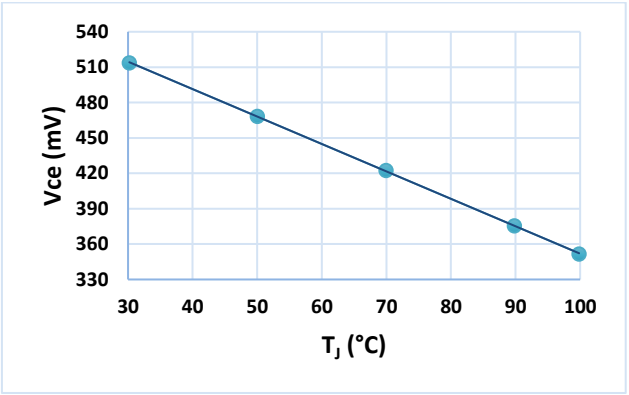

Figure 6 Collector-Emitter voltage V_{ce} of T_1 as a function of the junction temperature T_J.

3.3 The test bench

As mentioned before, this method was tested in an accelerated ageing test bench, with the synoptic of this latter presented in **Figure 7**. One FPGA core of a PXI system (National Instruments) drives the IGBTs and the DC-link power source. It also controls an electronic board, dedicated to supply low current for the temperature measurement by TSEP. Furthermore, the PXI system is used to control the coolant fluid temperature, and it is also used to measure V_{ce}, V_f, and V_{ge} (Gate-Emitter voltage) through ADC converters. **Figure 8** represents the electrical cabinet of the test bench.

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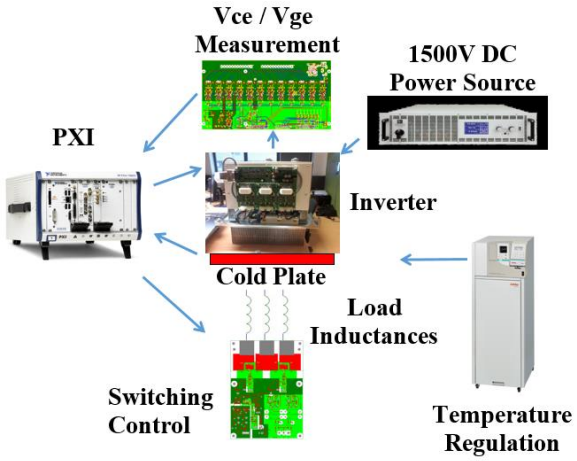


Figure 7 Synoptic of the test bench

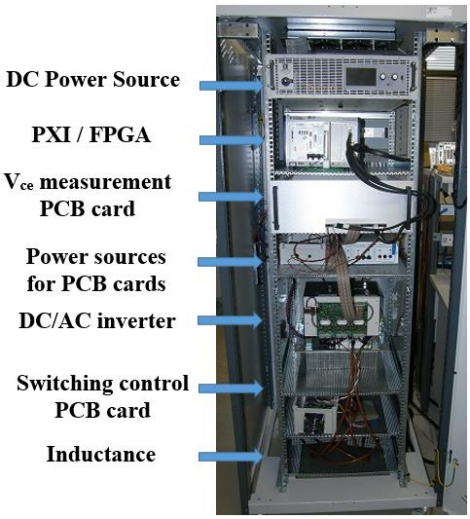


Figure 8 Electrical cabinet of the test bench

4 Validation of the thermal impedance measurement

The validation of the in-situ Z_{th} measurement is crucial for evaluating this test bench. Thus, in this section, Z_{th} measurements obtained with a classical method will be compared with the proposed in-situ measurements setup.

4.1 Classical measurement

For classical Z_{th} measurements, the experimental setup is based on the measurement of the thermal impedance during the cooling of the device. This method widely presented in the literature [8] [9] [10] [11], requires a total disconnection of the characterized semi-conductor device from the rest of the inverter. Moreover, it needs an independent current source to inject a current in the semiconductor device in order to heat it up under constant power dissipation, before the measurement of the TSEP during the cooling phase.

Figure 9 represents the DUT (Device Under Test) mounted on the cold plate, and connected to the current sources. In this figure, only one low current source is connected to the DUT. **Figure 10** represents the full measurement test bench, where the data are recorded using a data logger.

Finally, **Figure 11** represents the variation of the thermal impedances of the power modules as a function of time. These measurements are obtained with the classical method. The "Cat 1" thermal impedances represent the self-heating thermal impedances, whereas the "Cat 2" impedances represent the mutual thermal coupling impedances between the devices.

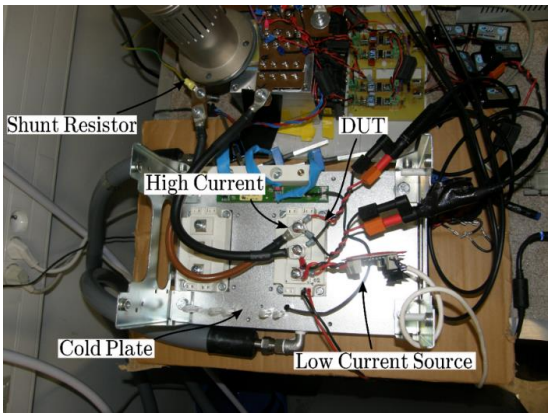


Figure 9 Connection of the current sources to the DUT

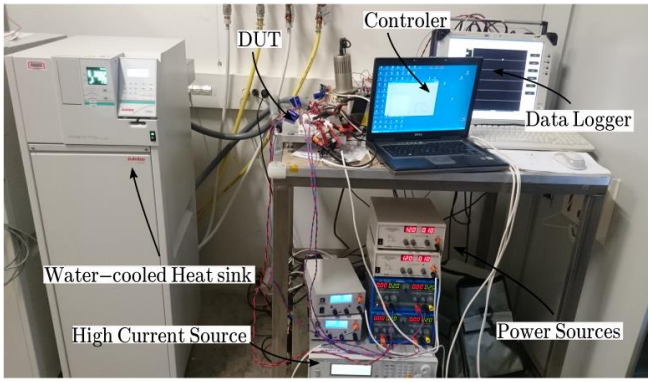


Figure 10 Thermal impedances measurement test bench

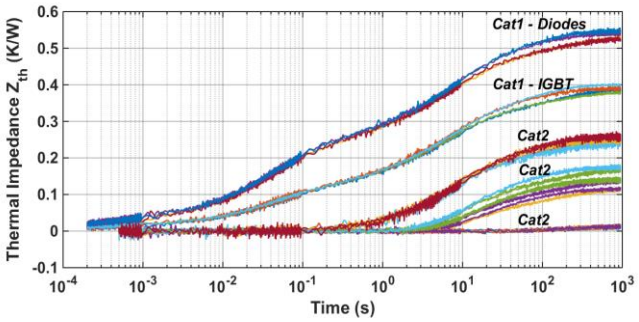


Figure 11 Thermal impedances obtained with the classical measurement method

4.2 Comparison and validation

In order to validate the in-situ method, several measurements of the thermal impedances were done, using the method presented in §3.1 with different current injection durations (between $10^{-2}s$ and 10s). Then, the results were compared with the ones obtained with the classical

method. Accordingly, **Figure 12** represents a comparison between the measured thermal impedances of IGBT T_1, using both the classical method and the in-situ method, while **Figure 13** represents the thermal impedances of diode D_1.

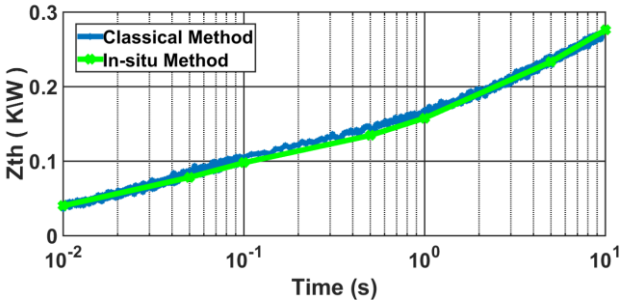


Figure 12 Thermal impedances of IGBT T_1 obtained with both methods.

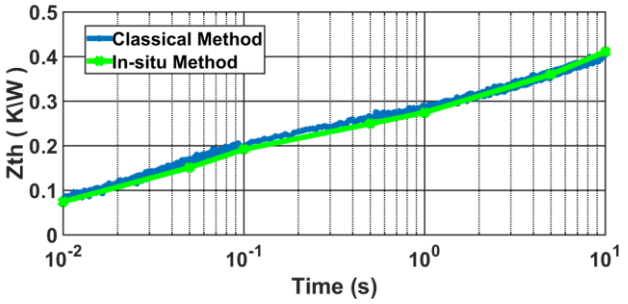


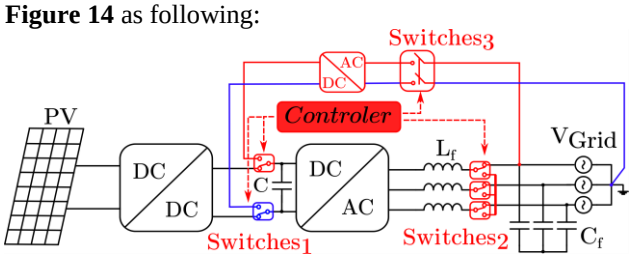
Figure 13 Thermal impedances of diode D_1 obtained with both methods.

It can be noticed that the results obtained with the in-situ method, are very close to the ones obtained with the classical method, which validates the in-situ method. Here, only the results on T_1 and D_1 are presented, however the measurements on the other devices also showed very close results.

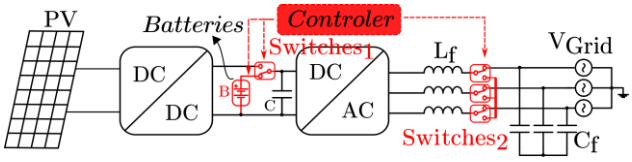
On the other hand, the measurement of the thermal impedance using the in-situ method can be done just by calculating some points, as presented in **Figure 12** and **Figure 13**. Each point corresponds to one current pulse duration. The choice of the pulse duration is important in the final application, as it will determine the type of degradations that could be observed. For very short durations (several ms), it will be possible to observe the degradation of the die attach. However, for duration of several tens of ms to several hundreds of ms, the measurements will be impacted by substrate damages. Nevertheless for longer durations (several s to several hundreds of s), it will be possible to respectively observe the degradation of the thermal interface material or of the cooling device.

5 Implementation in a condition monitoring system of photovoltaic inverters

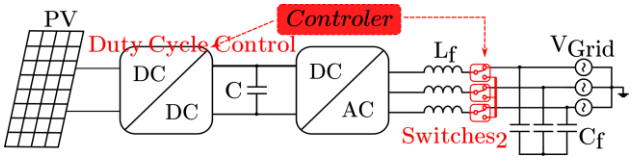
Already validated in an accelerated ageing test bench, the in-situ condition monitoring method needs to be implemented in a condition monitoring system, inside a photovoltaic inverter. However, since the diagnosis phase will be done during the non-operation period of the inverter (eventually at night), it is necessary to find a power source to supply the DC-link bus. It should be noticed that the power needed to apply the method is only equivalent to the power losses of the inverter, during relatively short times (the inverter power losses $\leq 4\%$ of the inverter's input power during operative production). Hence, three possible solutions are proposed in this paper, illustrated in **Figure 14** as following:



a) Using a rectifier



b) Using batteries



c) Using the DC/DC inverter

Figure 14 The different proposed topologies of the photovoltaic inverter's condition monitoring system

Figure 14.a suggests using a rectifier connected to the grid, to supply the DC-link bus of the photovoltaic inverter. The controller connects and disconnects the switches (Switches 1 and 2), in order to apply the diagnosis cycle during the night. Switches_2 are used to disconnect the group of inductances L_f from the grid, and to reconnect them together during the diagnosis phase. According to this solution, the diagnosis phase can be applied every day or every few days.

Figure 14.b suggests using batteries that can be connected to power the DC-link bus during the diagnosis phase (night), and then recharged during the production phase. According to this solution, the diagnosis phase can be applied every day, or every few days.

Similarly to the other solutions, the one illustrated in **Figure 14.c** proposes to wait for the daylight, to produce sufficient energy to power the DC-link bus, using the photovoltaic panels. This can be done, by controlling the duty cycle of the DC/DC inverter.

All these propositions are only preliminary ideas for future implementations of the in-situ condition monitoring in PV inverters. They have to be designed, validated and

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carried out in prototypes. Furthermore the cost of these solutions has to be estimated and compared in order to determine if these solutions could be commercially realistic.

6 Conclusions

This paper presents a method for in-situ condition monitoring of semi-conductor devices in DC/AC PV inverters. This method allows for in-situ measurement of three damage indicators. Particularly, this method allows for in-situ measurement of the semi-conductor's dynamic resistance r_d. This indicator is considered to be more sensitive to the devices degradation than V_{ce} or V_f.
Moreover, the method allows for an in-situ measurement of the thermal impedance of the semi-conductor devices. This method was implemented and tested in a power cycling test bench, and was validated with classical measurement tests. Finally, the paper proposes three solutions for an implementation of the method in a condition monitoring system of DC/AC photovoltaic inverters, which have to be validated in the future.

7 Aknowledgements

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