Power cycling test with power generated by an adjustable part of switching losses

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Keywords

«Component for measurements», «Power cycling», «Reliability», «Silicon Carbide», «Switching losses», «Test bench»

Abstract

In standard power cycling tests, forward conduction generates heat in the die and therefore the thermomechanical stress in the package. In application, however, a significant part of the power losses are switching losses, so that the load current is lower than in standard power cycling test, for an equal temperature swing. A new concept for power cycling tests is presented, which allows the generation of switching losses in addition to conduction losses. This concept closer to the real application. The circuit still uses a low voltage power source, while maintaining an accurate measurement of the virtual junction temperature. First test results of IGBTs in standard module technology and SiC MOSFETs in discrete TO-247 housing indicate no significant difference in results from standard power cycling tests. The new method was successfully applied to low voltage Si MOSFETs, which is for the first time applied to such a power cycling test under conditions where switching losses dominate.

1. Introduction

The methods of standard power cycling tests have been improved over the years, e.g. higher accuracy for measuring the $V_{CE}(T)$ or faster measurement after turn off, does permitting a more accurate determination of the virtual junction temperature, but there are no approaches with application-close loss generation and simultaneously very accurate detection of the virtual junction temperature.
In the standard method for power cycling, a low current is used for the $V_{CE}(T)$ method [1] and a high DC current for heating. In this case the temperature swing ΔT_J directly relates to the load current and the on-time. To adjust ΔT_J, setting the gate voltage at devices under test is an option, but this only helps to adjust a few K as there should be a big distance kept to operating in linear mode.
For devices with very low conduction losses e.g. low voltage MOSFETs the standard approach is to operate the inverse diode [2]. When operated in MOSFET-mode a higher current than feasible in application might be needed to provide the desired losses for high temperature swings. Hence it is possible that some connections close to the chip, such as bond wires, are overstressed. This could lead to wrong results and conclusions. The new concept adds switching losses to the conduction losses in an adjustable part so that the temperature swing is no longer directly related to the current or the on-time.

2. Test bench concept

A simplified schematic is given in Figure 1. The concept was explained in detail in [3].

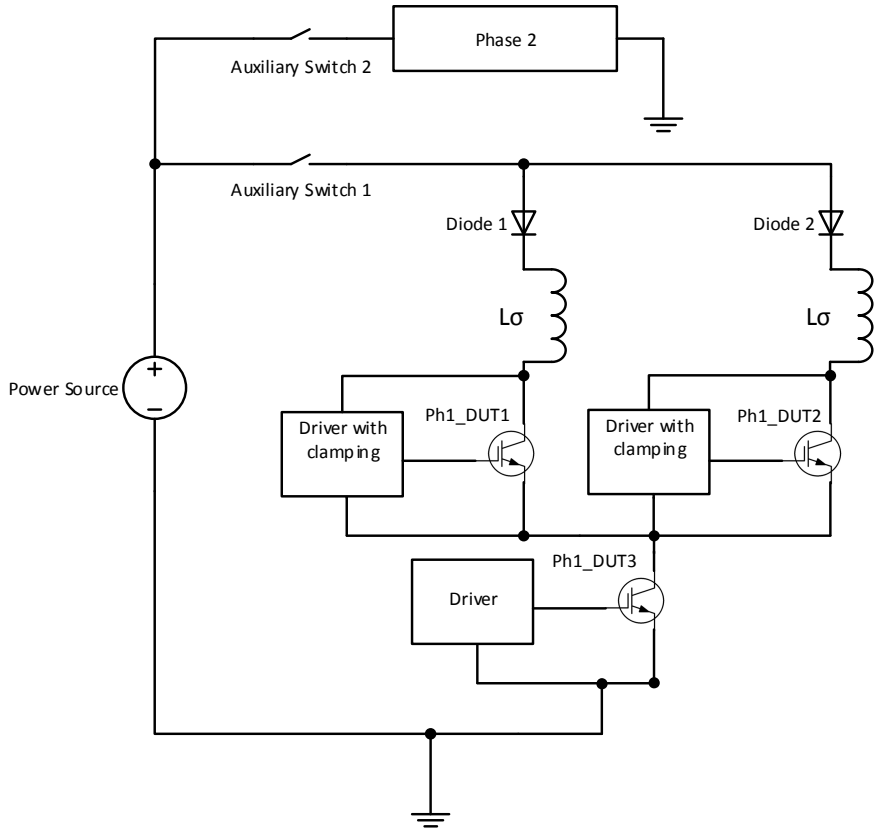

Figure 1: Simplified schematic of the test bench

As in standard power cycling test setups, a low voltage, high DC current power source is used. The test bench has two parallel phases of the same structure. Each phase consists of two parallel legs, containing a blocking diode (D1, D2), a stray inductance (L_σ) and up to three devices under test (DUT). The load current is alternated between the two phases. During the on-time of one phase the load current is switched alternately by the devices under test (DUT1 and DUT2) at a selectable high-frequency. The stray inductance L_σ causes a voltage peak at turn-off and thus gives rise to switching losses. A third device under test which stays in on-state, is optionally connected in series to the paralleled legs. If the ratio of switching to conduction losses is selected to be equal within DUTs 1 and 2, DUT3 should have the same temperature swing ΔT_J as the two alternating devices. A sensing current source is connected to each device under test. The switching voltage at turn-off is projected to maximal 1kV and is designed for a frequency of up to several 10 kHz.

In MOSFET-mode the DUTs will behave the same way with a slightly different pulse pattern.

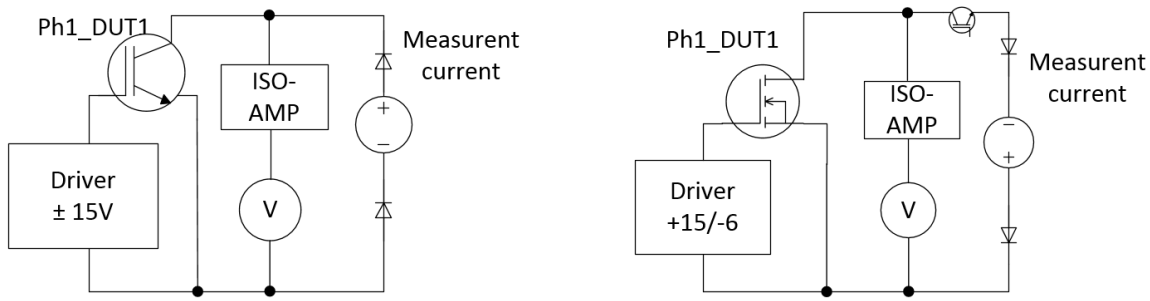

Figure 2: Difference between setups for MOSFET (right side) and IGBT devices (left side)

Figure 2 shows the differences between the two operation modes of the test bench. For T_J measurement the IGBT stays on, while in MOSFET-mode the device is turned off. The measurement current source is connected in reverse and therefore needs to be protected while the high frequency operation is running. This is realized through a small IGBT, which decouples the source. Ph1_DUT3 and Ph2_DUT3 must be turned off as well, so that a driver is necessary. More information for power cycling of MOSFETs and SiC-MOSFETs can be found in [4].

3. Boosted active clamping

At every turn-off the switching voltage must not exceed the breakdown voltage of the DUT. Therefore, for the switching devices, a boosted active clamping circuit is applied which is shown in Figure 3.

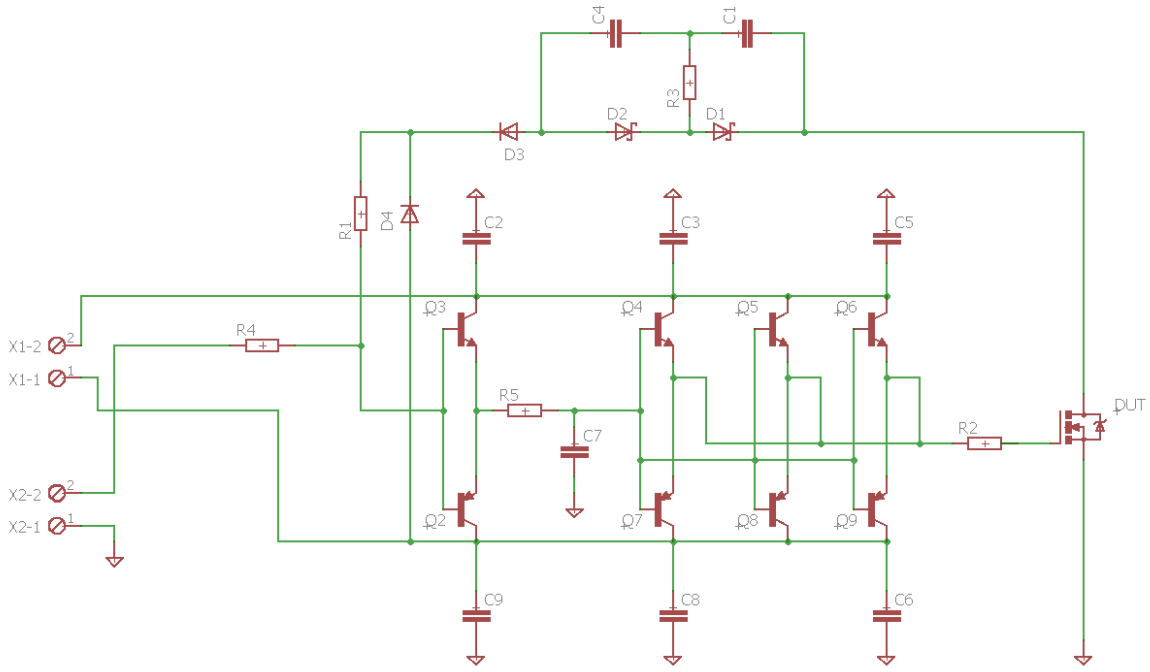

Figure 3: Schematic of the boosted active clamping circuit

In this schematic the device under test is named again as DUT. The connector X1 is used for power supply from the driver, X2 provides the gate signal. The TVS-diodes D1 and D2 are used to set the level of the clamping voltage. The capacitances C1 and C4 give a dv/dt feedback. This is used to reduce the edge steepness at the rising edge and to prevent overshoots of the clamping voltage. Diode D4 does the same for the falling edge. Diode D3 blocks the gate voltage. If the turn off voltage exceeds the blocking voltage of the TVS diodes, a current flows into the first amplifier stage (Q2 and Q3) and is amplified again in the second stage, consisting of the transistors Q4 – Q9. Some of the current from the Diodes D2 and D1 goes through R4 into the driver. The ratio can be set via the resistances R1 and R4. R5 and C7 are used as a low pass to avoid ringing in the clamping voltage.

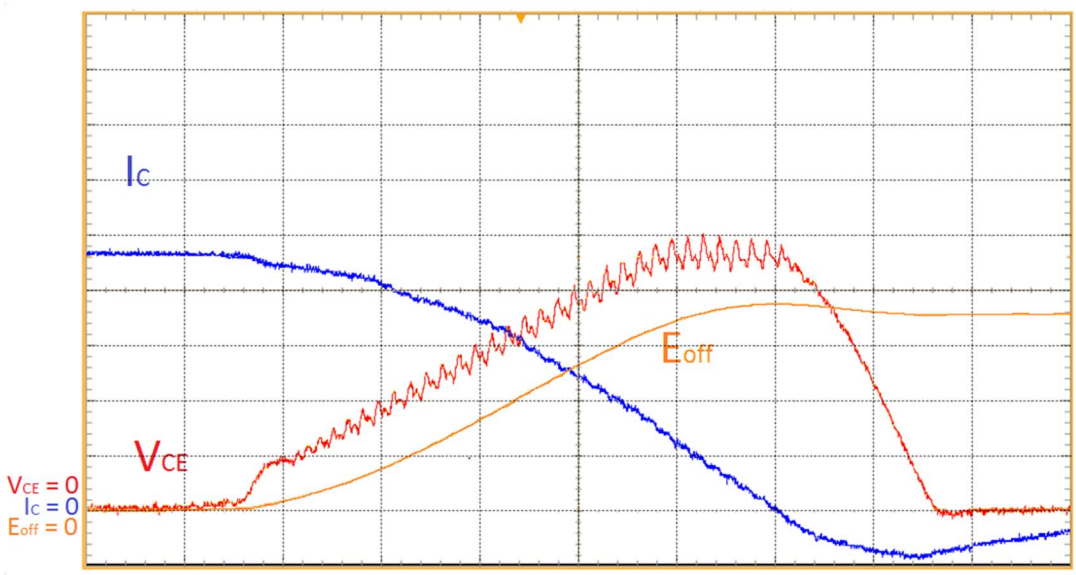

Figure 4: Clamping at I_C=23A, V_{CE}=440V, E_{off} =3.6mJ
Red: 100V/div, Blue: 5A/div, Orange: 1mJ/div, 200ns/div

Figure 4 shows a turn off event. The used devices under test were 25A, 1200V IGBTs (Infineon FS25R12). The oscillations of the collector emitter voltage are caused by the boosted active clamping stage. In an earlier version the RC-filter between the two amplifier stages is missing. The slowly rising V_{CE} shows the effect of dv/dt feedback. The turn-off energy (E_{off}) is stored into the device within roughly 1.4µs. Hence it can be assumed that E_{off} only feeds into the thermal capacitance of the chip. The resulting temperature swing should not exceed a certain value which is roughly 3 – 5 K.

$$\Delta T_j = \frac{dQ}{C_{th} \cdot d \cdot A} = \frac{5\ mJ}{2.34\ \frac{g}{cm^3} \cdot 703\ \frac{J}{kg \cdot K} \cdot (0.115 \cdot 27.2)\ mm^3} = 0{,}97\ K \qquad (1)$$

Equation (1) is shows the resulting temperature swing with the above-mentioned simplification. If the result stays below 3 - 5 K, there is no need to consider it in the lifetime estimation. The used values are taken from the datasheet of the chip and the chip size.

4. Measurement

As mentioned before, a high measurement accuracy is desired, so that the V_{CE}(T) method is used to determine the virtual junction temperature. In this section the applied pulse pattern and the measurement circuit are explained.

4.1. Pulse pattern

A pulse pattern is implemented as shown in Figure 5.

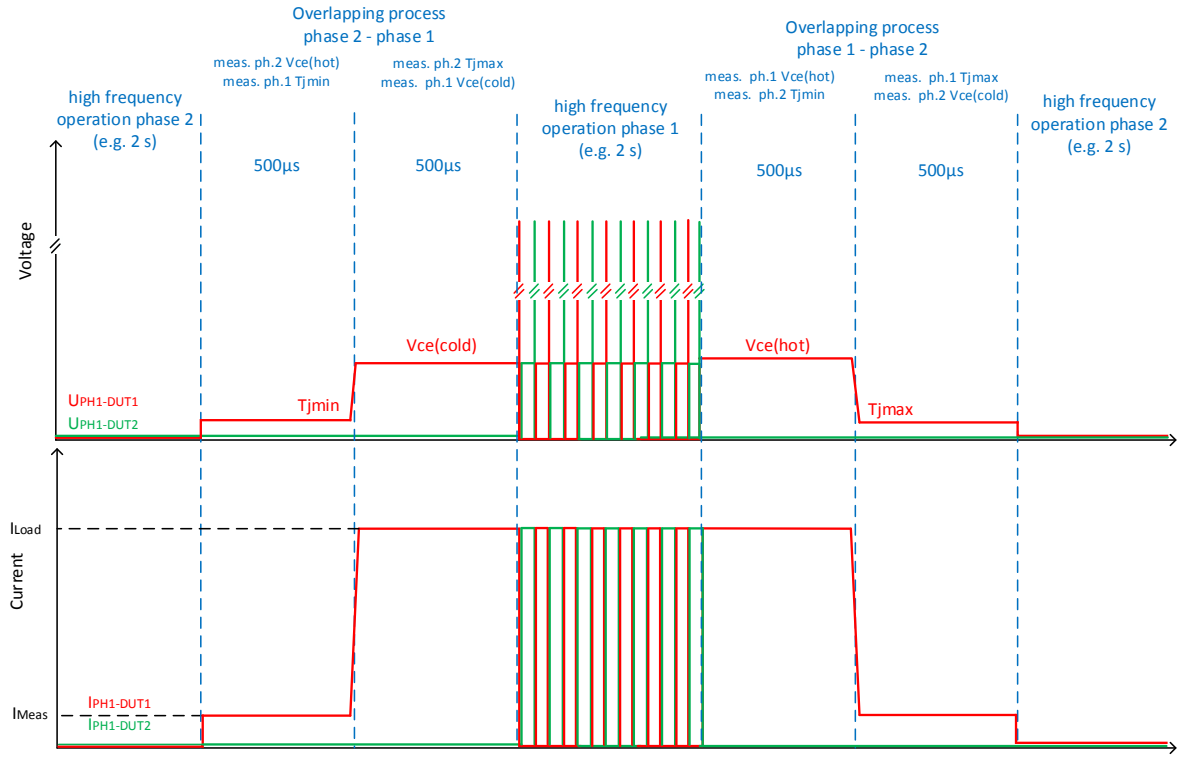

Figure 5: Pulse pattern for high frequency operation

Between the high frequency operation of each phase, a measurement period of 1000µs is implemented. For each phase within one cycle it is possible to measure only one device under test. Therefore the device, which is to be measured, is alternated every cycle. Otherwise the load current at $V_{CE(hot)}$ and $V_{CE(cold)}$ would split uncontrollably within the two devices. For MOSFETs the $V_{CE}(T)$-method is used as well. The used temperature sensitive electrical parameter TSEP is the voltage drop of the inverse diode. The pulse pattern for IGBTs and MOSFETs is slightly different. In IGBTs-mode the measured device stays on while T_{Jmax} is determined. In MOSFET-mode the semiconductor must be turned off and a negative gate voltage must be applied to prevent the current from flowing through the channel.

The AD-converter of the measurement system, which is used for gauging V_{CE}, must not be exposed to voltages above 10V, hence a circuit is necessary for protection and insulation, shown in Figure 2 as ISO-AMP.

4.2. Isolated amplifier

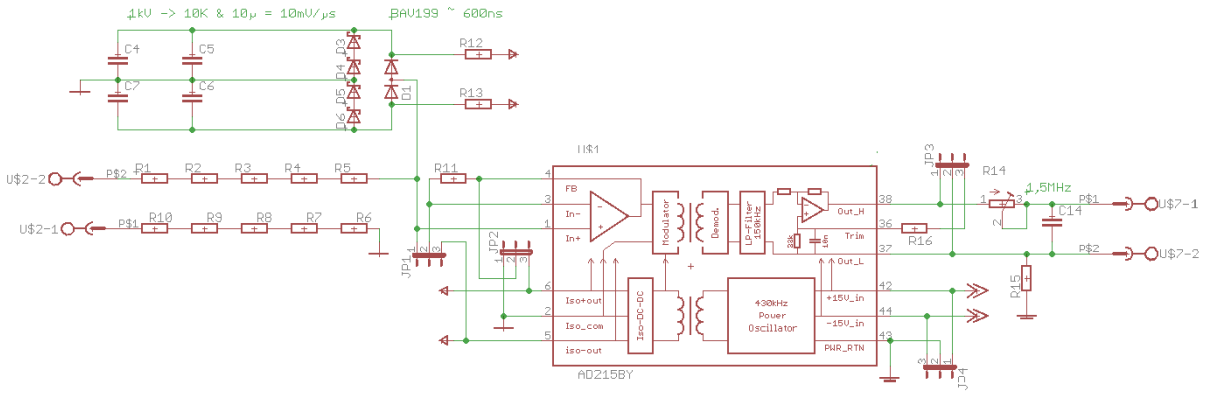

Figure 6: Schematic of the isolation amplifier circuit

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Figure 6 shows the basic schematic of the isolation amplifier stage, which is used for every device under test. It is designed to withstand 1 kV for a duty cycle of ¼. The resistances R1-R10 are used to limit the current while breakdown of the TVS diodes D3-D6. These are high power resistances for up to 100 W, which need to be actively cooled. D1 is a diode with a very small reverse recovery time. If the voltage exceeds 10 V in any direction, the TVS diodes will break down and clamp the voltage to 10V, otherwise the AD215BY measures the actual input voltage at the connector U2. The power supply (±15V) is not shown. The offset error of the AD215 is in the range between 0 and -80mV, but can be adjusted to zero. The gain error is not measureable because the input impedance of the measurement system is 10 GΩ, so that a very low current flows.

5. First Results

For investigating the new method and the power cycling bench, a test on modules with 1200V/25A single chip IGBT 4 (FS25R12) in standard technology from Infineon [5] was carried out. Later some tests on SiC-MOSFETs and low voltages MOSFETs were performed, as Table 1 shows.

Device	Current Rating	t_{on}	Test current	Switching Frequency	Ratio	Test No.	ΔT_J	TJ_{min}	No. of Samples
IGBT	25A	1 s	28 A	12.5kHz	50%	1	80K	30-55°C	10
IGBT	25A	1 s	20 A	20kHz	66%	2	80K	25°C	4
IGBT	25A	1 s	28 A	25kHz	66%	3	100K	30-40°C	4
SiC-MOSFET	55A	2 s	37 A	50kHz	50%	4	75K	25-40°C	11
IRFP 4004	195A	2 s	120 A	12kHz	75%	5	75K	35-40°C	8

Table 1: Overview of the performed tests, device parameters voltage class all 1200V except Si-MOSFETs 40V, switching frequency, ratio of switching to total losses, test number and parameters

Test 1 is used as reference, because this test condition has often been used on other (DC) test benches and the ratio of 50% allowed the connection a third DUT in always on-state. The results agreed well with expectations. A lot of samples were used, because the first results on air cooled heatsinks show a big spread of conditions. For subsequent tests, the cooling was changed to water cooling.

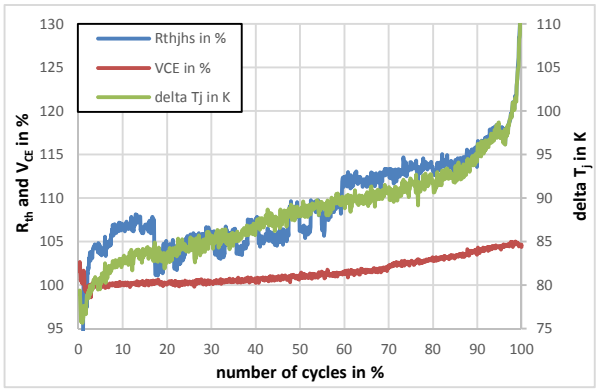

Figure 7: Course of Test 1 Phase 1 DUT 3, steady on, ΔT_J=80K, 28A, T_{Jmax} =105-120°C, t_{on}=1s

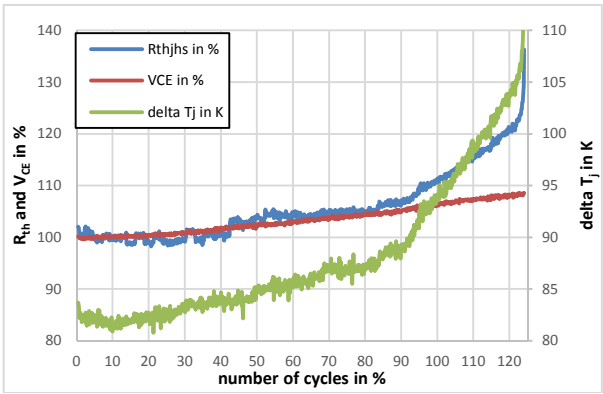

Figure 8: Course of $V_{CE(Cold)}$ of Test 3, 50% switching losses, ΔT_J =80K, 28A, T_{Jmax} =125°C, t_{on}=1s

All tested IGBTs show roughly the same behavior. V_{CE} increases during the whole test and R_{TH} often rises at the very end, as Figure 7 demonstrates. Figure 8 shows a switched device and also, as in Figure 7, there is an increasing V_{CE} during the whole test and R_{TH} rises at the end, so that no different failure mechanism was observed for this test condition between device with and without switching losses. The relative cycle numbers in comparison to CIPS2008 model [6] are the same.

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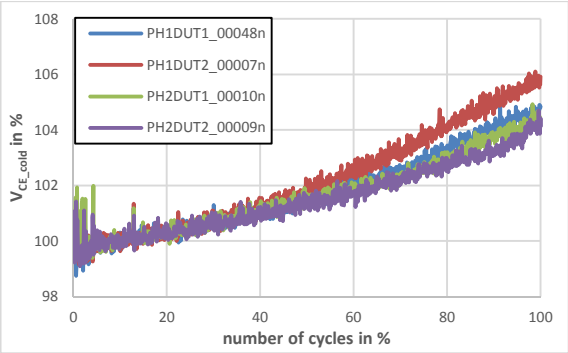

Figure 9: Course of $V_{CE(Cold)}$ of Test 2, 66% switching losses, ΔT_J =80K, 20A, T_{Jmax} =105°C, t_{on}=1s

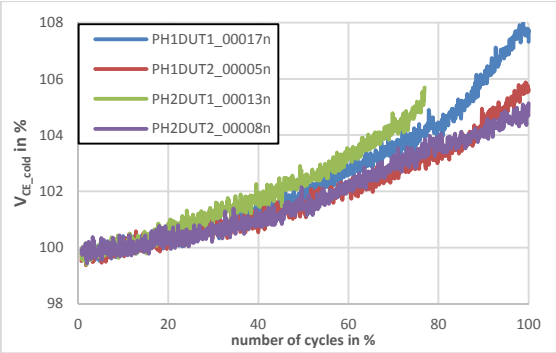

Figure 10: Course of Test 1 Phase 2 DUT 1, 66% switching losses, ΔT_J =100K, 28A, T_{Jmax} =130-140°C, t_{on}=1s, , not the same X-axes as figure 9

Figure 9 and Figure 10 Figure 9show the voltage drop of all devices under test during test 2 and 3. As well as in the first test, a continuously rising V_{CE} is observed. Some devices show an R_{TH} increase. Tests 2 and 3 show that there is no difference in lifetime at all between the switched and the non-switched devices for this IGBT type.

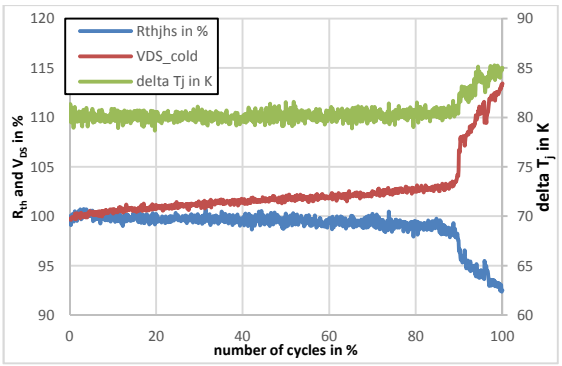

Figure 11: Course of Test 4 Phase 1 DUT 1, 50% switching losses, ΔT_J =80K, 37A, T_{Jmax} =125°C, T_{on}=2s, 100% =56000 cycles

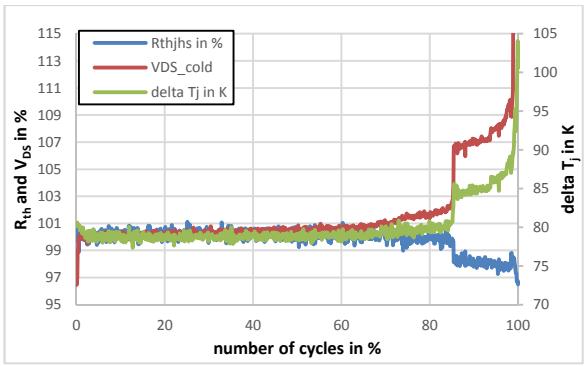

Figure 12: Course of Test 4 Phase 2 DUT 3, steady on, ΔT_J =79,5K, 37A, T_{Jmax} =124°C, T_{on}=2s, 100% =41000 cycles

In Test 4, SiC MOSFETs in discrete housing TO-247 (ROHM) were investigated. Figure 11 and Figure 12 giving the courses of the test. All tested devices show the same behavior, but the number of cycles up to end of life is scattered more than in Tests 1, 2 and 3. The stepwise increase in V_{DS} indicates a bond wire failure at ~90% of the performed cycles. At the same time the R_{TH} decreases, which is very uncommon and caused by an artefact of the measurement setup. The used TIM has a high R_{TH} and the thermocouple was placed far away in an adapter plate with a big thermal capacitance, and the switching losses are not considered in the calculation of R_{th}. A better method for extracting R_{th} is required.
Test 5 with low voltage MOSFETs is still running. Here the new method shows its advantages. Due to the very low $R_{DS,on}$ per area, the common approach is to operate the inverse diode or the gate voltage needs to be set close to the gate threshold voltage to increase conduction losses. If the gate voltage is below a certain value the positive temperature coefficient of conduction losses is changed to a negative temperature coefficient, which means at high temperature the losses are reduced. Therefore such an approach may decelerate the load compared to application, and more cycles until end of life are achieved. The inverse diodes have negative temperature coefficients as well [4].

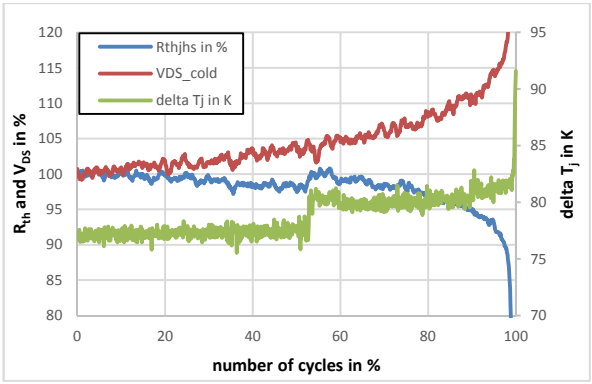

Figure 13: Course of Test 5 Phase 2 DUT 2, 75% switching losses, ΔT_J =77K, 120A, T_{Jmax} =130°C, T_{on}=2s, 100% =395000 cycles

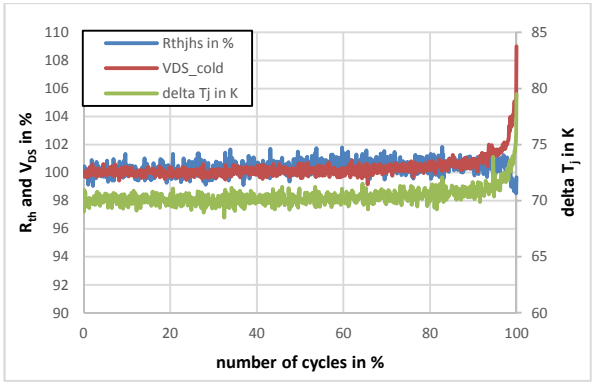

Figure 14: Course of Test 5 Phase 2 DUT 3, inverse diode, ΔT_J =70K, 120A, T_{Jmax} =127°C, T_{on}=2s, 100% =208000 cycles

Compared are a MOSFET in the new switching mode (Figure 13) and a MOSFET at position DUT 3 in Figure 1, used in the in the inverse diode mode (Figure 14). Both tested devices show jumps in V_{DS} which indicate bond wire failures. At ~50% of the performed cycles of the switched DUT, a rise in ΔT_J can be observed. This happens due to a change of another semiconductor within the phase. Possible reasons are that the connection is slightly different or in another position so that the inductivity is changed and hence the temperature swing. Figure 13 shows this behavior, but the change in ΔT_J is very small so that it can be neglected.

Due to the very small voltage drop of the low voltage Si-MOSEFTs the 105% end of life criteria is questionable.

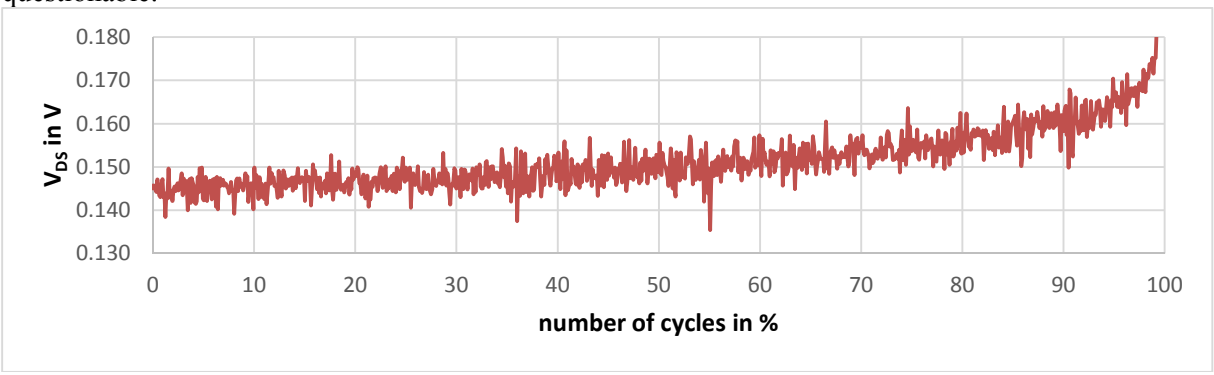

Figure 15: Voltage drop of Phase 2 DUT 2 at load current cold, unfiltered

Figure 15 shows the actual value of the voltage drop during the test (Figure 13) at load current. The initial value is ~145mV, therefore 105% is 152.25mV and the 7.25mV increase can hardly be determent. Due to measurement noise and current inaccuracy the limit for V_{DS} should be set to 110% or 115% for low-voltage MOSFETs in forward conduction mode.

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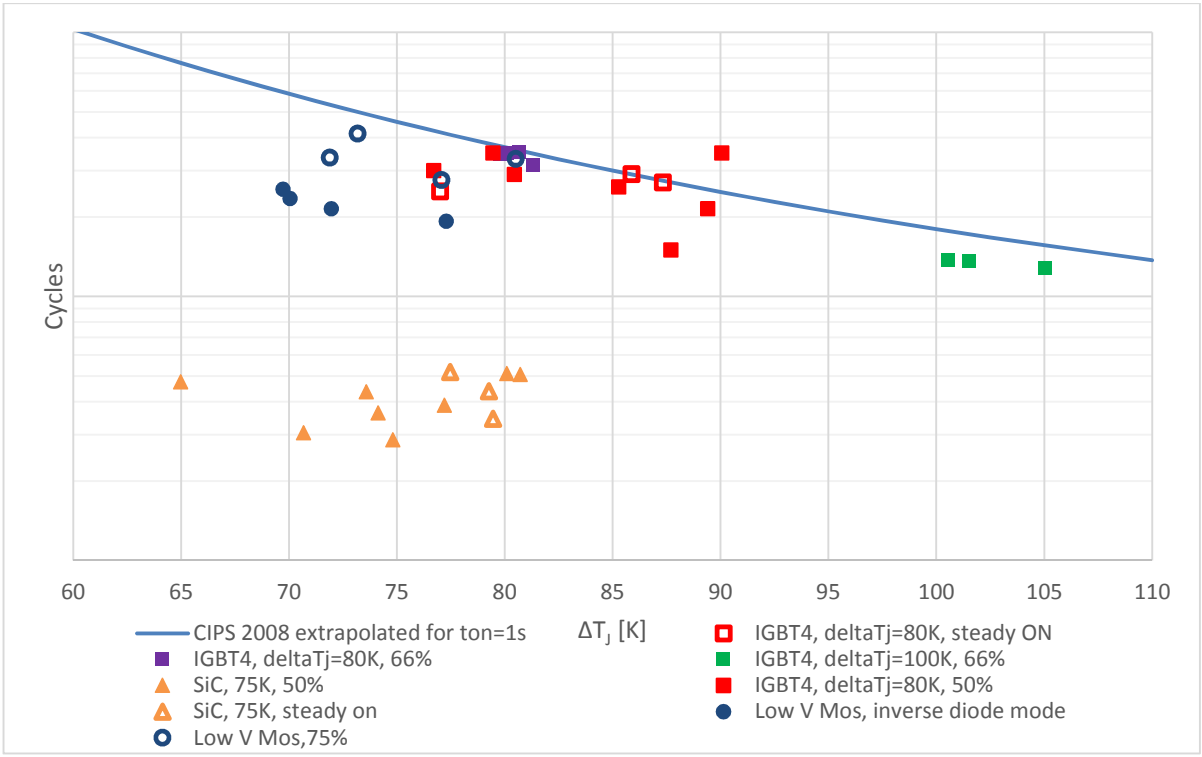

Figure 16: Overview of the performed tests, Failure criteria V_{CE}/V_{SD} 105%, R_{thjh} 120%, IGBT modules: t_{on} 1s, discrete SiC and low V MOSFETs t_{on} 2s

As mentioned before, the results of tests 1, 2 and 3 are very close to each other and slightly above the reference (blue line). The SiC MOSFETs have a lower power cycling capability when standard packaging technology is used, which was already shown in [7]. The blue circles below the reference shown in Figure 16 are tested using inverse diode. In this test, the switched devices achieve a longer lifetime. Regarding evaluation of possible cycles to failure for the LV MOSFET, the results should be considered carefully. A detailed failure analysis and more results are necessary before interpretation.

Conclusion

The new proposed power cycling method is capable of providing thermal electric stress in a different way than the standard power cycling test with conduction losses only. In contrast to the established method the tested semiconductors prove their ability to switch actively, to block voltage and to conduct current. The commonly used $V_{CE}(T)$ method for measuring of the junction temperature was applied successfully under switching conditions with high voltage. With this new test method it is possible to reduce the average current over a very wide range, so that it is possible to prove the given equations for calculating the expected lifetime as given in [6]. The performed tests on IGBTs show a small difference which might be close to the range of measurement errors and production tolerances, between the switched and non-switched devices under test. The investigated discrete SiC MOSFETs seem to behave in the same way, but show a larger spread in the number of cycles reached. A lower N_f was achieved, which is comparable to former results [7].
For the first time, an application close test for low voltage Si MOSFETs is performed with load in the MOSFET mode and with dominating switching losses. The achieved number of cycles up to failure is quite high. More tests and detailed analysis are necessary for evaluation.
For further improvement of the test method, a better procedure for extracting R_{th} and Z_{th} under these conditions will be of used.

References

[1] R. Schmidt und U. Scheuermann, „Using the chip as a temperature sensor - The influence of steep lateral temperature gradients on the Vce(T)-measurement,“ in *Proceedings EPE '09*, Barcelona, 2009.

[2] BMW: GS 95035;VW: VW 82324 Group Standard, *LV324: Qualification of Power Electronics Modules for Use in Motor Vehicle Components, General Requirements, Test Conditions and Tests,* Daimler, 2014.

[3] C. Herold, P. Seidel, J. Lutz und R. Bayerer, „Topologies for inverter like operation of power cacling tests,“ in *Microelectronics Reliability, vol. 64*.

[4] C. Herold, L. Tinschert, P. Seidel, J. Sun und J. Lutz, „Power Cycling Methods for SiC MOSFETs,“ in *Proceedings ISPSD*, Saporo, 2017.

[5] AG, Infineon, „FS25R12W1T4,“ 16 10 2013. [Online]. Available: http://www.infineon.com/dgdl/Infineon-FS25R12W1T4-DS-v02_01-en_de.pdf?fileId=db3a3043139a1bac0113b4c47b490549. [Zugriff am 28 06 2016].

[6] R. Bayerer, T. Herrmann, T. Licht, J. Lutz und M. Feller, „Model for Power Cycling lifetime of IGBT Modules - various factors influencing lifetime,“ in *2008 5th International Conference on Integrated Power Systems (CIPS)*, Nürnberg, 2008.

[7] C. Herold, M. Schäfer, F. Sauerland, T. Poller, J. Lutz und O. Schlling, „Power cycling capability of Modules with SiC-Diodes,“ in *Proceedings CIPS*, Nürnberg, 2014.