Vce-based chip temperature estimation methods for high power IGBT modules during power cycling - A comparison

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<< V_{ce} measurement>>, <<IR thermography>>

Abstract

Temperature estimation is of great importance for performance and reliability of IGBT power modules in converter operation as well as in active power cycling tests. It is common to be estimated through Thermo-Sensitive Electrical Parameters such as the forward voltage drop (V_{ce}) of the chip. This experimental work evaluates the validity and accuracy of two V_{ce} based methods applied on high power IGBT modules during power cycling tests. The first method estimates the chip temperature when low sense current is applied and the second method when normal load current is present. Finally, a correction factor that eliminates the series resistance contribution on the V_{ce} measured at high current, is proposed.

Introduction

The IGBT power modules are one of the main components prone to failures in high power converters [1]. The temperature levels and variations (i.e. thermal-cycling) are considered the major stressors causing degradation of the power device and finally, failures. Therefore, an accurate and reliable measurement of the junction temperature is imperative for monitoring and evaluating the thermal performance of the modules in a converter operation, as well as, in a power cycling (PC). Numerous methods have been introduced for sensing an on-line junction temperature [2] and they can be classified as: direct measurement on chip level using temperature sensors or infrared (IR) thermography and indirect temperature acquisition by means of Thermo-Sensitive Electrical Parameters (TSEPs). TSEPs are preferred, because they do not require modifications of the device package and for some of them, the implementation in real field applications is more straightforward [3].

The concept of using TSEPs is to estimate the temperature of a semiconductor chip by finding the dependency of an electrical parameter on its temperature. For this purpose, various TSEPs have already been used in research and each is characterized by its own sensitivity and linearity to the temperature. For Metal Oxide Semiconductor (MOS) based devices, there are three main TSEPs: the saturation current, the gate-emitter threshold voltage [4] and the forward (on-state) voltage during low current injection [5, 6]. However, these methods require modifying the operation of a converter. Also, they need additional electrical equipment as seen in [7]. Thus, an alternative method has been proposed in [3], in which the forward voltage is measured during rated current levels without any need of additional components. Even though this is a more realistic method to be implemented in real-time operation, certain issues such as self-heating during the measurement process and aging effects should be taken into account. Further, there are temperature estimation methods which are based on the dynamic behavior of the device such as turn-on and turn-off delay time [8], the collector current slope [8] and peak gate current during turn-on [12]. Regardless of which TSEP is used, a calibration procedure is essential at the beginning.

A common practice for calibration is to heat up the power module externally until a homogeneous heat distribution is established from the heat sink up to the chip. Then, at that known temperature, the TSEP is measured. Repeating the measurement over a wide range of temperatures, the relation between temperature and the TSEP is found. It should be considered that during the measurement process, the chip

self-heating remains as low as possible and its temperature remains fairly constant, otherwise compensation is needed. This is an issue especially for high current pulses and thus the pulse duration should be minimized. Another critical issue is the series resistance contribution of the packaging caused by terminal leads and bond wires. Since in functional conditions the temperature is not uniformly distributed, a correction factor should be applied. This is discussed in [13], while in [14] a method which uses multiple current levels to cancel out the series resistance is performed showing also robustness to an aging effect.

This paper presents two temperature estimation methods intended for PC test setup of high power IGBT modules. These methods use the forward voltage drop during low sense and high load current as TSEPs [15]. In order to eliminate the contribution of the series resistance in the latter method, a correction factor is introduced. The accuracy and validity of these methods are tested and the results will be compared with direct measurements conducted at open power device by IR camera. In addition, the experimental test setup is outlined and the methods are tested during its operation.

Junction Temperature Estimation Methods

V_{ce}-T_{vj} at high load current

The on-state voltage drop of an IGBT is a function of virtual junction temperature (T_{vj}), collector current (I_c) and gate-emitter voltage (V_{ge}). It is the sum of the voltage across the semiconductor part and the voltage across the electrical connections.

$$V_{ce(meas)} = V_{ce}(T_{vj}, I_c, V_{ge}) + R_{on}(T_{on}) \cdot I_c \tag{1}$$

Where, $V_{ce(meas)}$ is the measured on-state voltage, I_c is the collector current, V_{ce} is the forward voltage across the semiconductor, V_{ge} is the gate-emitter voltage, R_{on} is the resistance of the electrical connections, T_{vj} is the virtual junction temperature and T_{on} is the temperature of the electrical connections.
Now, at constant I_c and V_{ge}, it is possible to measure $V_{ce(meas)}$ as a function of temperature. Further, it is also assumed that T_{on} is equal to T_{vj} in the calibration process. From the I-V characteristic curves, it can be observed in Figure 5(a) that V_{ce} shows a non-linear relation with respect to T_{vj} and I_c. However, considering only the linear part, according to [16], the on-state voltage drop can be derived from the following equation.

$$V_{ce(meas)}(T_{vj}, I_c) = V_{ce(meas),0} + k_{TS}(I_c) \cdot (T_{vj} - T_{vj,0}) \tag{2}$$

Where, $V_{ce(meas),0}$ is the measured on-state voltage at a reference temperature $T_{vj,0}$, k_{TS} is the voltage sensitivity in respect to temperature [mV/K]. The junction temperature is thus calculated by:

$$T_{vj,est} = \frac{V_{ce(meas)}(T_{vj}, I_c) - V_{ce(meas),0}}{k_{TS}(I_c)} + T_{vj,0} \tag{3}$$

However, as shown in [13] and it will be also noticed later during PC tests, the above equation can outcome substantially different temperatures compared to the actual values. This happens due to the fact that temperature distribution is homogeneous during the characterization of the power module while is mounted on a heat plate, whereas this is not the case during normal operation. In latter case, large temperature gradients can occur on the surface of the chip as well as the terminal interconnects. Thus, a correction factor should be added and it will compensate the deviation of the V_{ce} measured at normal operation from the one measured during calibration process. This factor is defined as:

$$\Delta V' = V_{ce}(T_{vj}, I_c) - V_{ce(meas)} = SF \cdot (T_{vj} - T_{vj,min}) \cdot \alpha \cdot I_c \tag{4}$$

Where, $V_{ce(meas)}$ is the measured on-state voltage at module's terminals while normal operation and $V_{ce}(T_{vj}, I_c)$ is the corresponding voltage drop at given T_{vj} and I_c which is found using the calibration curves. In addition, it is possible to extract the temperature coefficient α[mΩ/K] of the effective resistance of the IGBT switch using a Shockley with a resistor model [15]. With a scaling factor (SF) to exclude the non linear effect of the semiconductor part, it becomes viable to calculate the additional voltage drop by multiplying with the temperature deviation, $T_{vj,est} - T_{vj,min}$, and I_c. Equation (3) in now formulated as in Equation (5) and the corrected estimation of the junction temperature ($T_{vj,corr}$) is found.

$$T_{vj,corr} = \frac{V_{ce(meas)}(T_{vj}, I_c) - V_{ce(meas),0} + \Delta V'}{k_{TS}(I_c)} + T_{vj,0} \tag{5}$$

V_{ce}-T_{vj} at low sense current

The measurement of V_{ce} during low current injection is a very common method in PC tests. It is known from literature [6, 14] that it indicates temperatures close to mean values of the active chip surface. This method is preferred due to its simplicity and adequate sensitivity that is about -2 to -2.5 mV/^{o}C for few hundreds of mA sense current. As also shown in Figure 6, at these low current levels the IGBT has negative temperature coefficient. Such a low current does not produce any noticeable extra heating at the device and it can be applied continuously when the IGBT is in on-state. At a PC setup, low current injection can be used to estimate the temperature immediately after the high load current has removed and the switch off transient has passed. The measurement can provide reliable results after a period of around 300 μsec which is the time that the semiconductor needs to establish an electrical equilibrium to conduct the low current. This time period can be seen later in Figure 4(b). In addition, it is possible to monitor the cooling phase until the switch is on again.

Experimental setup

Power Cycling Test Bench

The temperature estimation methods are applied on a PC test bench, as shown in Figure 1. It has been built to conduct accelerated wear-out tests for high power IGBT modules. Its operation principle is based on an injection of high DC current pulses. The chip is heated up actively during the on-time while is let to cool down during the off-time. Thus, temperature swings appear due to losses on the active area of the IGBT. That induces stresses on the device and triggers failures such as solder fatigue and bond wires lift-off as explained in [9, 10]. Even though only conduction losses are predominant, the DC mode has other advantages. It allows many devices to be tested simultaneously with less considerations regarding noise in the measurements, overvoltages and high DC link-voltage.

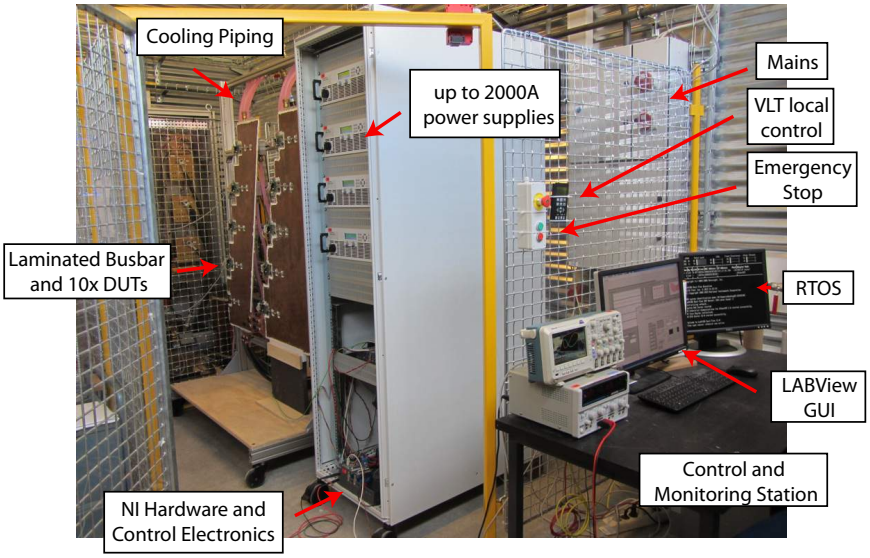


Figure 1: View of the PC test setup.

As seen in the schematic diagram of Figure 2, the setup is able to accommodate up to 10 PrimePack3™ IGBT modules that are placed in 5 strings configuration with 2 devices under test (DUTs) in series on each string. At normal operating condition, one string is active at a time conducting the full current. Then, the current is switched to the next active string with a short overlap time (100 μsec) in order to preserve the current path and avoid high switching overvoltages. The duty cycle of all the strings can be adjusted by setting one string as by-pass that increases the total cooling duration of all strings. The control and measuring system is built using National Instruments (NI) Labview and NI C-series modules. In addition, the DUTs are water-glycol cooled using the ShowerPower® (Danfoss) technology which keeps a homogeneous temperature distribution across the baseplate [11]. An example of a PC test is presented in Figure 3 showing the V_{ce} and V_{ge} voltages of two IGBT switches under test. Also, the overlap time is highlighted. In this case, 2 strings (i.e. 4 DUTs) are tested with a pulsed current of 1000A. The switching on and off times (t_{on},t_{off}) for both the strings are set to 1sec. If a longer cooling time was desired, then the by-pass string could be activated.

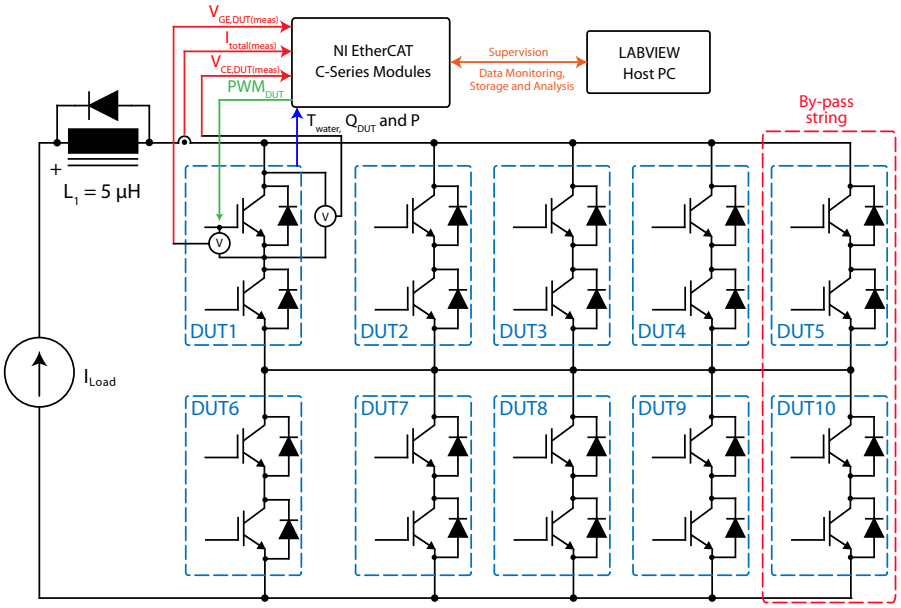


Figure 2: Simplified diagram of the PC accelerated wear-out test setup for IGBT modules.

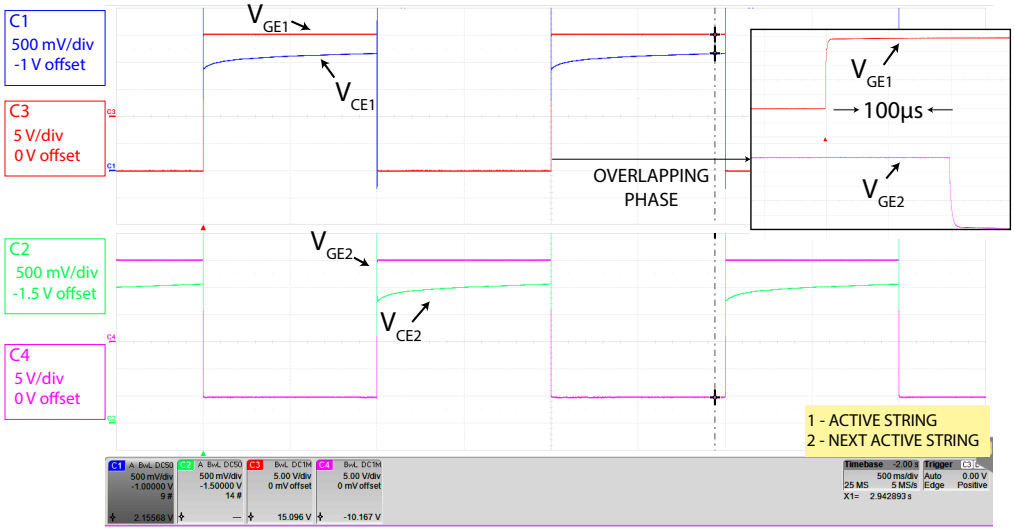
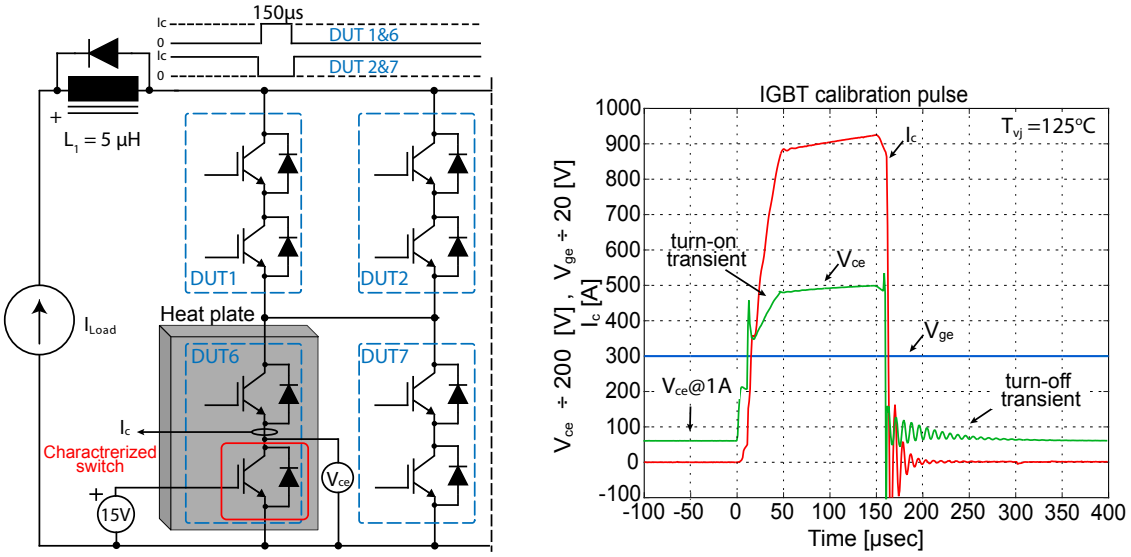


Figure 3: PC test with 2 tested strings, $t_{on} = t_{off} = 1$sec and I_c =1000A.

Vce-Tvj Calibration

For the calibration phase, the power module that is going to be characterized is placed on a controllable heat plate. By heating up the plate at different temperatures, the module is also heated up homogeneously. At each temperature, the values of V_{ce} are measured for the desired Ic. This is accomplished by applying short load pulses of 150 μsec fact that minimizes the self-heating of the chip [15]. The IGBT switch that is characterized is set to be constantly switched on with applied V_{ge}=15V, as indicated in Figure 4(a). According to Figure 4(b), the calibration of V_{ce} and T_{vj} with the low sense current of 1A is done during -100 to 0 μsec time interval. From 0 to 150 μsec, the load pulse is applied and (V_{ce},I_c) pairs are measured during 100 to 150 μsec period in order to ensure that turn-on transient has passed. The sampling period f_s for these electrical measurements is set to 1MHz. In addition, Figure 4(a) explains how part of PC setup is used for the characterization of the modules. In this case, DUTs 2 and 7 are used to preserve the load current in the setup and for the short calibration time the current is switched to DUTs 1 and 6.



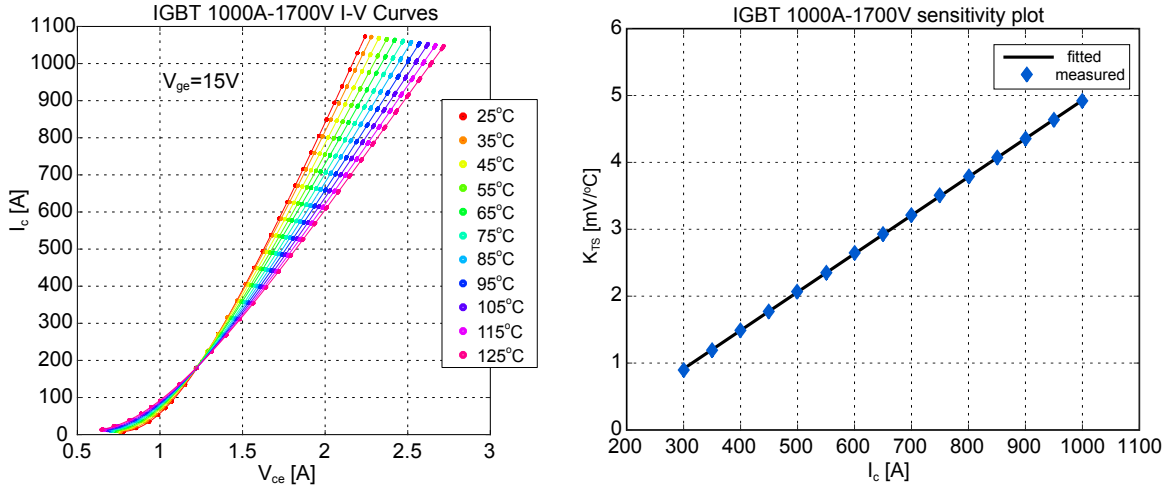
(a) (b)

Figure 4: Figures showing for the calibration of V_{ce}-T_{vj} (a) PC test setup modified for calibration of the low side IGBT of DUT 6 (b) Typical calibration pulse at T_{vj}=125°C, sense current of 1A and load current at around 900A.

Results and Discussion

Characterization of TSEPs

The measurement points of V_{ce} obtained from the calibration process are plotted and the relation of T_{vj} in respect to V_{ce} and I_c can be extracted, while V_{ge} is kept constant at 15V. From now on V_{ce} for high load current is referred as $V_{ce,Ic}$ and for low sense current (I_{low}) is referred as $V_{ce,low}$. The DUT is a P3 IGBT module rated for 1000A-1700V and consisted of six parallel sections of half bridges with two IGBTs and two diodes. Both low and high current TSEPs are calibrated for temperature range from 25°C to 125°C according to the method mentioned above. In Figure 5(a) the characteristic curves are plotted for different temperature levels. Sensitivities (k_{TS}) of approximately 1mV/°C and 5mV/°C occur for 300A and 1000A respectively, as shown in Figure 5(b).



(a) (b)

Figure 5: Figures showing (a) I-V characteristic curves (b) Sensitivity factor k_{TS}.

Similarly for $V_{ce,Iow}$, the relation to T_{vj} for I_{low} equal to 1A is plotted in Figure 6. It can be seen that this TSEP has linear behavior and measured sensitivity of -2.4mV/°C at that specific current.

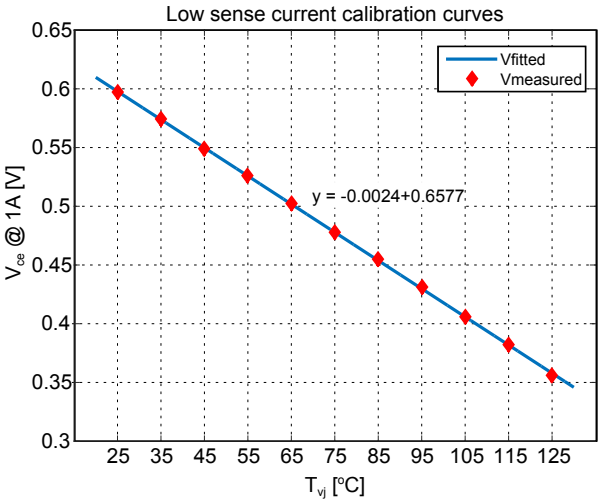
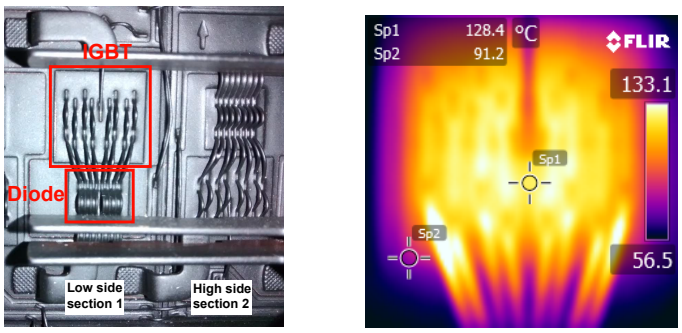


Figure 6: $V_{ce,low} - T_{vj}$ calibration curves.

Temperature Estimation during PC

In order to test and validate the two temperature estimation methods, DC current pulses are applied to the IGBT module under test, in a same way as done during PC. The switching times are $t_{on} = t_{off} = 1$sec and currents from 500A upto 1000A are measured with steps of 100A. The module package has been opened for IR thermography measurements. Thus, the casing has been removed so as a single IGBT chip (out of inner 6 connected in parallel) is viewed directly through the camera. Moreover, the internal structure has been painted black to increase the emissivity of the targeted surface. The actual chip which is measured is shown in Figure 7(a), while in Figure 7(b) measurements from the thermal camera are processed using PC based software.



(a) (b)

Figure 7: Images showing (a) IGBT sections with a black lacquer (b) IR thermography.

The sequence of V_{ce} measurement points are illustrated in Figure 8. The first two measurements, ① and ②, are done to estimate the chip temperature at the time instant when IGBT is turned on, giving the $T_{vj,start}$ and the rest two measurements,③ and ④, estimate the chip temperature exactly when the IGBT is turned off outcoming the $T_{vj,end}$. The ① and ④ belong to $V_{ce,low}$ and the ② and ③ are done for $V_{ce,Ic}$. Cumulative results from both methods are shown in Tables I and II, together with the IR measurements for minimum, maximum and average temperatures of the entire IGBT chip surface.

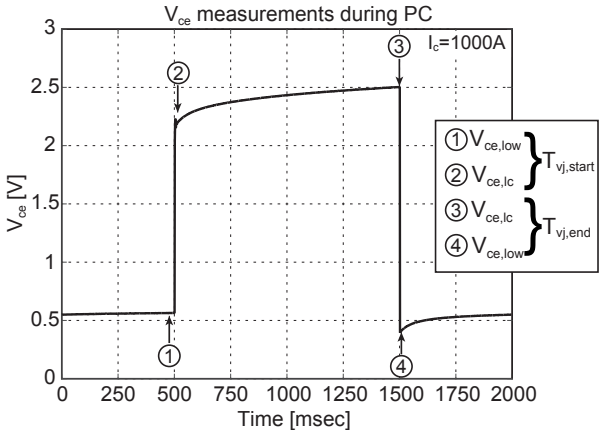


Figure 8: V_{ce} measurement sequence during one PC cycle.

Table I: Evaluation results of $V_{ce,low}$ and $V_{ce,Ic}$ at the start of a pulse

I_c $[A]$	$T_{IR,min}$ $[^oC]$	$T_{IR,mean}$ $[^oC]$	$T_{IR,max}$ $[^oC]$	$T_{vjVce,low}$ $[^oC]$	$T_{vjVce,Ic}$ $[^oC]$	$Error$ $T_{vjVce,low}[\%]$	$Error$ $T_{vjVce,Ic}[\%]$
500	25.0	25.4	25.9	25.3	25.0	-0.4	-0.1
600	24.6	25.1	25.7	24.9	25.0	-0.6	0.1
700	24.7	25.1	25.7	24.9	24.4	-1.0	0.7
800	24.7	25.2	25.7	24.9	23.9	-1.0	1.3
900	24.7	25.1	25.7	24.9	23.7	-1.0	1.4
1000	24.7	25.1	25.6	24.9	23.7	-0.9	1.4

Table II: Evaluation results of $V_{ce,low}$ and $V_{ce,Ic}$ at the end of a pulse

I_c $[A]$	$T_{IR,min}$ $[^oC]$	$T_{IR,mean}$ $[^oC]$	$T_{IR,max}$ $[^oC]$	$T_{vjVce,low}$ $[^oC]$	$T_{vjVce,Ic}$ $[^oC]$	$Error$ $T_{vjVce,low}[\%]$	$Error$ $T_{vjVce,Ic}[\%]$
500	35.5	53.9	60.6	53.2	45.3	-1.3	8.6
600	38.2	62.0	70.7	61.5	51.7	-0.9	10.3
700	41.9	71.8	77.8	71.5	60.0	-0.4	11.8
800	46.3	83.0	96.8	82.8	69.7	-0.2	13.3
900	57.1	97.0	113.0	96.1	80.8	-0.9	16.2
1000	63.8	115.5	132.1	112.0	93.5	0.4	18.0

It can be noticed that $V_{ce,low}$ method estimates T_{vj} very accurately both at the beginning and at the end of the pulse. The relative error of $V_{ce,low}$ when compared with $T_{IR,mean}$ remains lower than 1.3% which indicates that this method estimates values very close to the average temperature across the chip surface rather than the minimum and maximum appeared temperatures. In contrast $V_{ce,Ic}$ method, even though it tracks T_{vj} at the very early start of the pulse with satisfying accuracy, then it deviates from $T_{IR,mean}$ resulting at the end of the pulse the maximum error of 18%. This can be explained from the uneven temperature distribution of the chip that becomes even more significant for high load pulses reaching $\Delta T_{IR,max-min}$=68.3K at I_c=1000A. Moreover, the lead terminals and copper traces and bond wires are at different temperatures than the chip fact that differs from what exists in calibration, as justified earlier.

At this point the correction factor $\Delta V'$ should be introduced and it will cancel out the contribution of the resistance in series inside the module package. The coefficient α extracted from the I-V curves outcomes a value of $5.4476 \cdot 10^{-6}$[mΩ/K]. The value is extracted using a Shockley with resistor model [15]. Then, the scaling factor is tuned at a value of SF=0.23 resulting after the correction in an acceptable convergence of $T_{vj,est}$ to $T_{IR,mean}$ as shown in Figure 9. This SF can be considered as the 23% of the effective resistance which is responsible for the initial error. The same SF is valid for all current levels above 300A which is the linearity area of the I-V curves. However, here only four representative cases are shown. Finally it can be noticed that $T_{vj,corr}$ converges better to the reference values in the higher temperature range than the lower one. This is expected because of the nonlinear thermal dynamics and

transients in the voltage at the beginning that deviates the temperature estimation and it does not converge at the expected value.

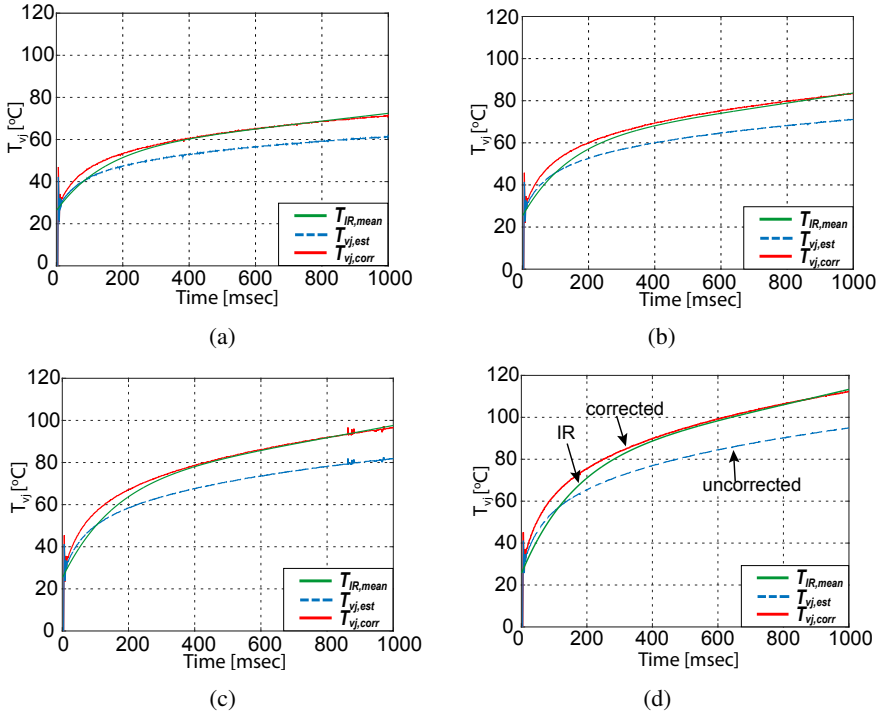


Figure 9: T_{vj} plot during 1sec pulse for (a) I_c=700A (b) I_c=800A (c) I_c=900A and (d) I_c=1000A.

Conclusion

Chip temperature estimation of an IGBT power module becomes imperative when health monitoring and reliability aspects are into consideration in a converter operation. Also when power cycling tests are conducted, chip temperature has to be known as it is the main parameter which stresses the device under test. This experimental work has investigated the validity and accuracy of two methods that are based on forward voltage measurements and its relation to the chip temperature. The one measures the on-state voltage when the IGBT conducts a low sense current while the other measures it at a high load current. The first method is easy and convenient to be applied on power cycling tests where the switch can stay at on-state after the high load is removed and only the sense current is present. In this way the amplitude of the temperature swing is measured. The second method is possible to be used in real field applications too [3]. However, the initial estimation has to be corrected in order to obtain accurate results. The results has shown that the first method estimates the average chip temperature with great accuracy at all current levels, fact that has been proved by infrared thermography. Regarding the second, the initial discrepancies from the real chip temperatures has been corrected by introducing a correction factor. Having the thermography as a reference, a scaling factor has tuned in order to outcome values as close as to the mean chip temperature. The same correction factor used in different current levels and validated the measurement. A number of tests is required to find the variation of factors between the modules and in different packaging of modules.

References

[1] Shaoyong Yang; Bryant, A.; Mawby, P.; Dawei Xiang; Ran, L.; Tavner, P., "An Industry-Based Survey of Reliability in Power Electronic Converters," Industry Applications, IEEE Transactions on , vol.47, no.3, pp.1441,1451, May-June 2011

[2] Baker, N.; Liserre, M.; Dupont, L.; Avenas, Y., "Improved Reliability of Power Modules: A Review of Online Junction Temperature Measurement Methods," Industrial Electronics Magazine, IEEE , vol.8, no.3, pp.17,27, Sept. 2014

[3] Ghimire, Pramod, et al. "A real time measurement of junction temperature variation in high power IGBT modules for wind power converter application." Integrated Power Systems (CIPS), 2014 8th International Conference on. VDE, 2014.

[4] Bahun, Ivan, Neven obanov, and eljko Jakopovi. "Real-Time Measurement of IGBTs Operating Temperature." AUTOMATIKA: asopis za automatiku, mjerenje, elektroniku, raunarstvo i komunikacije 52.4 (2012): 295-305.
[5] Smet, V.; Forest, F.; Huselstein, J.-J.; Richardeau, F.; Khatir, Z.; Lefebvre, S.; Berkani, M., "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling," Industrial Electronics, IEEE Transactions on , vol.58, no.10, pp.4931,4941, Oct. 2011
[6] Scheuermann, Uwe, and Ralf Schmidt. "Investigations on the VCE (T)-Method to Determine the Junction Temperature by Using the Chip Itself as Sensor." PCIM Europe. 2009.
[7] Nowak, Mietek, Jacek Rabkowski, and Roman Barlik. "Measurement of temperature sensitive parameter characteristics of semiconductor silicon and silicon-carbide power devices." Power Electronics and Motion Control Conference, 2008. EPE-PEMC 2008. 13th. IEEE, 2008.
[8] Kuhn, Harald, and Axel Mertens. "On-line junction temperature measurement of IGBTs based on temperature sensitive electrical parameters." Power Electronics and Applications, 2009. EPE'09. 13th European Conference on. IEEE, 2009.
[9] Pedersen, Kristian Bonderup, and Kjeld Pedersen. "Bond wire lift-off in IGBT modules due to thermomechanical induced stress." Power Electronics for Distributed Generation Systems (PEDG), 2012 3rd IEEE International Symposium on. IEEE, 2012.
[10] Busca, Cristian. "Modeling lifetime of high power IGBTs in wind power applications-An overview." Industrial Electronics (ISIE), 2011 IEEE International Symposium on. IEEE, 2011.
[11] Olesen, K., R. Bredtmann, and R. Eisele. "Shower power: new cooling concept for automotive applications." Proceedings of the Automotive Power Electronics Conference, Paris, France, June. 2006.
[12] Baker, N. and Munk-Nielsen, S. and Iannuzzo, F. and Liserre, M. "Online Junction Temperature Measurement Using Peak Gate Current.", APEC, 2015
[13] Perpiñà, X., et al. "Temperature measurement on series resistance and devices in power packs based on on-state voltage drop monitoring at high current." Microelectronics Reliability 46.9 (2006): 1834-1839.
[14] Dupont, Laurent, and Yvan Avenas. "Evaluation of thermo-sensitive electrical parameters based on the forward voltage for on-line chip temperature measurements of IGBT devices." Energy Conversion Congress and Exposition (ECCE), 2014 IEEE. IEEE, 2014.
[15] P. Ghimire, K. B. Pedersen, I. Trintis, B. Rannestad, and S. Munk-Nielsen , "Online Chip Temperature Monitoring Using Vce-Load Current and IR Thermography", accepted in ECCE 2015.
[16] Kim, Yong-Seok, and Seung-Ki Sul. "On-line estimation of IGBT junction temperature using on-state voltage drop." Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE. Vol. 2. IEEE, 1998.