A Power Supply Reaching Titanium Level Efficiency for a Wide Range of Input Voltages

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***Abstract*—To achieve the highest possible grade for server or computer power supplies in terms of efficiency, various solutions for high line input already exist on the market. In this work a new topology is investigated closely in simulation, showing that the titanium grade may also be achievable at low line input and how the control can be done by utilizing low voltage MOSFETs. Currently the control algorithm is already implemented in real hardware and the prototype for one module is under developement.**

I. Introduction

The voluntary certification program for efficient energy use in power supplies, the 80plus [1] initiative introduced the new titanium level efficiency requirements at high line input for switch mode power supplies. Until today, there are no titanium requirements for low line input. Due to higher input currents at low line and accordingly higher conduction losses in the power factor correction stage titanium level is very difficult to achieve at low line. The goal of this work is to achieve the required efficiencies for high line titanium level regardless of low or high line input in all load conditions.

II. Proposed Solution

The new idea is to use a modular approach, which is able to divide the input voltage at high line to utilize low voltage MOSFETs like OptiMOS™ [2], which have have even better switching figure of merits (FOM) compared to higher voltage MOSFETs like CoolMOS™. The power supply consists of two stages with each being able to deliver 500 W of output power. The input AC voltage is capacitively divided. At low line input both stages operate in parallel (see Fig. 1) and at high line both are stacked in series (see Fig. 2) to divide the input voltage. Each module consists of a triangular current mode (TCM) resonant power factor correction (PFC) circuit (which has already been demonstrated by ETH-Zürich) [3], [4] (TCM-PFC) with a complementary controlled zero voltage switching (CC-ZVS) full bridge [5] (CC-ZVS Bridge) as an isolating DC/DC converter afterwards and a current doubler circuit on the secondary side.

For a single module, the circuit comprises of a three phase interleaved TCM PFC, a DC Link capacitor and a ZVS-Bridge for DC/DC conversion (Fig. 3). The input capacitor to divide the input voltage is very small (around 1μF) to minimize the phaseshift between the line voltage and the input current.

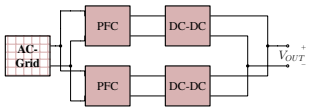

Figure 1. Proposed principle schematic for low line input.

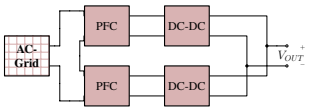

Figure 2. Proposed principle schematic for high line input.

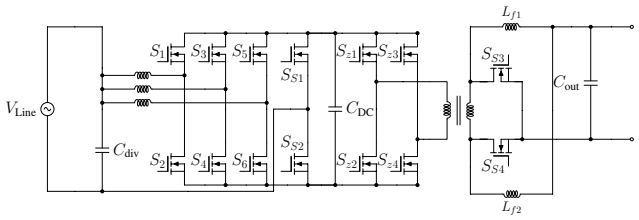

Figure 3. Principal schematic of a single module.

III. Control strategy: Implementation

The PFC stage is implemented with three interleaved fast switching phases (S_1 to S_6) and one slow switching (S_{S1} and S_{S2}) leg for the return path. The small capacitor on the input (C_{div}) divides the input voltage in case of a high line input. The PFC stage boosts the voltage to 200 V. The complementary controlled full bridge (S_{z1} to S_{z4}) converts the DC-link voltage down to 12 V DC with S_{s3} and S_{s4} as synchronous rectification MOSFETs in a current doubler topology [5]. The control has been implemented on a microcontroller and an field programmable gate array (FPGA). The switching timings for the PFC as well as the required duty cycle for the DC/DC stage are calculated by the microntroller and then sent to the FPGA to achieve a higher switching accuracy over quad serial peripheral interface (qSPI). The four pulse width modulation (PWM) signals for the DC/DC converter are generated on the FPGA with the duty cycle received from the microcontroller. Parts of the control for the PFC and zero voltage switching (ZVS) bridge has been implemented in Matlab/Simulink™.

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The main idea is that at startup the stages connect either in parallel or in series depending on the measured line voltage. This connection can be realized with semiconductor assisted relays for nearly no additional loss when operating. Both modules are controlled by the FPGA with identical signals for every corresponding switch (S_1 module 1 receives the identical signal as S_1 module 2).

IV. Control strategy PFC stage

A similar PFC has already been proposed by [3]. The key difference here is the change from high voltage MOSFETs to low voltage MOSFETs like OptiMOS™. This is possible through stacking or paralleling of modules. With this idea it is also possible to divide the input voltage per module to any desired level. The only major drawback with more modules is the reduction in power density, since the current through each module is the same, the magnetic components don't decrease in volume. Due to the triangular current control all fast switching MOSFETs (S_1 to S_6) in the PFC stage turn on under ZVS conditions, which results in zero turn-on losses.

A. Control of a single phase

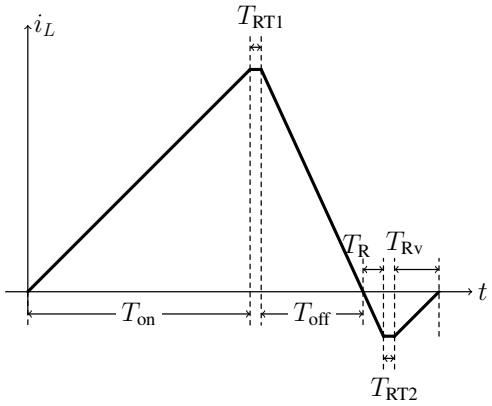


Figure 4. Basic PFC triangular current waveform [3].

Fig. 4 shows the waveform of the TCM PFC for a single phase. The waveform can be decomposed into six different time steps and each time step could be solved with differential equations. In total there would be three separate differential equations necessary, which provide six equations each with different inital conditions to solve. One linear differential equation for the on-times T_{on} and T_{Rv}, one nonlinear for the two resonant transitions T_{RT1} and T_{RT2} and another linear for the off time T_{off} and T_R. First only one phase consisting of the switches S_1 and S_2 of Fig. 3 is investigated closer.

1) At the beginning S_2 is on and the boost inductor is charging.
2) After T_{on} S_2 is switched off and both switches are off for the resonant time T_{RT1}. During the resonant time the inductor current charges both parasitic output capacitors C_{OSS} of the MOSFETs. During T_{RT1}, the voltage across S_2 is increasing in an S-shape and the voltage across S_1 is decreasing to zero.
3) When the voltage reaches zero, S_1 is switched on for the duration of T_{off} and T_R discharging the boost inductor and reversing the current after T_{off}.
4) After this time S_1 is switched off. For input voltages below half the DC-link output voltage no negative current would be required to achieve ZVS and S_1 could be switched off at zero current. For input voltages higher than half the DC-link voltages, S_1 is on for an additional time T_R charging the boost inductor with a negative current in order to achieve ZVS.
5) After switching off S_1, the second resonant transition starts, which increases the voltage across S_1 in an S-shape and decreases the voltage across S_2 in an S-shape.
6) S_2 is turned on again, charging the boost inductor. After T_{Rv} the current in the boost inductor is zero again.

For the control of this PFC the input voltage, the DC-link voltage and the zero current crossings of the inductor have to be measured. The input voltage is the actual input voltage for the module (this means it can be the total line voltage for low line or approximately half the line voltage for high line input), the DC-link voltage is controlled with an outer voltage loop controller and should be around 200 V DC and for each phase a zero current detection for the inductor current is necessary, see Fig. 5. The control algorithm consists of an inner control loop, which calculates the on- and off times depending on the measurements and the output of the other two control loops. The other two control loops are the outer DC-link voltage control loop and the phaseshift control loop. As an outer loop over all these controls a phase shedding control algorithm, which determines, if phases have to be added or removed to stay at a high efficiency, is implemented.

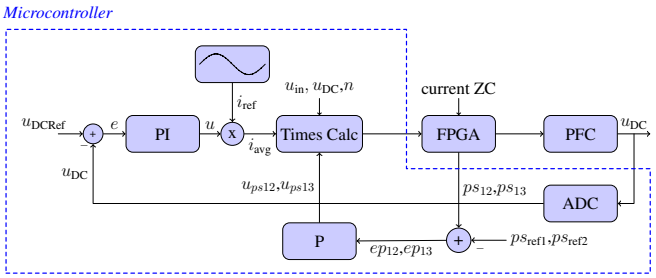


Figure 5. Simplified block diagram of the PFC control.

B. Phaseshift control

In order to minimize the input current ripple and to reduce the input EMI filter size, three phases are interleaved to

each other depending on the actual load. To achieve the best possible sinusoidal input current the phases should be out of phase to each other, with the optimum phaseshift according to eq. (1), where n is the number of currently active phases.

$$\phi = \frac{360}{n} \tag{1}$$

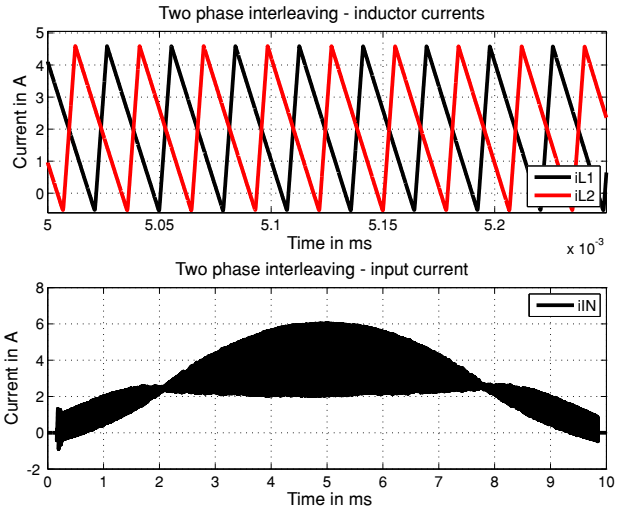
For every phase a statemachine has been implemented on the FPGA. Everytime when the inductor of phase 1 is beginning to charge the actual value of a phaseshift timer is stored (current period) and afterwards reset. If phase 2 or 3 start to charge the inductor the actual phaseshift timer values is stored (phaseshift values). These values are then sent via qSPI to the microcontroller. The phaseshift between the signals can be changed by increasing the peak-current i_{lp} and the negative current by the same amount. If both values are increased by the same amount (higher positive and higher negative current) the average current stays approximately the same. This principle can be applied to all three phases. The phaseshift between the phases is compared with the desired phaseshift from eq. (1) and gives an error e_{ps12} and e_{ps13} for the phaseshift between phase 1 and 2, and phase 1 and 3, see Fig. 5. Respectively these errors are the input of two simple P-controllers which can increase the required positive and negative current with u_{ps12} and u_{ps13}. If the output of one controller becomes negative a decrease of current would be required, which would also mean that this phase would then be delivering less power. In this case the positive and the negative current of the first phase is increased, the total system still delivering equal average power over all phases. Fig. 6 shows how the interleaving control performs for two and three phases.

C. Phase shedding

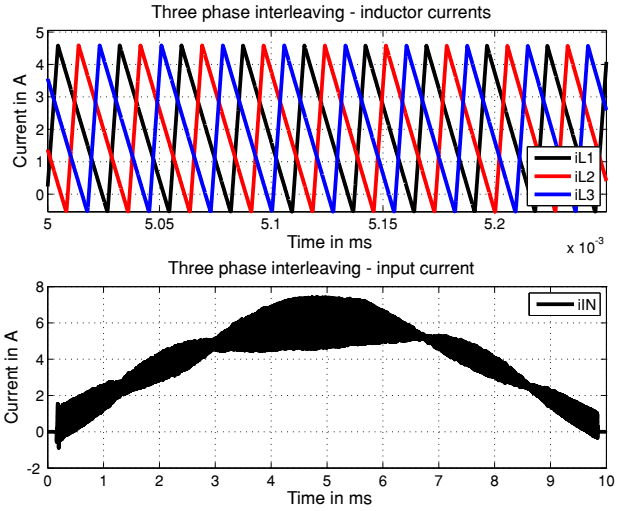
The load is estimated from the information of the currently active phases and the output value u of the voltage loop control. A statemachine is running on the microcontroller estimating the current load and adding or removing phases to stay in a high efficiency region. For a smooth control the number of active phases is only allowed to change during the zero crossings of the line voltage. Fig. 7(a) shows the controller response from a low to high load jump. At the beginning only one phase is active and after 10 ms the state machine goes into the next state enabling the second phase and after 30 ms all three phases are active and stay active. Fig. 7(b) shows the response from a low load to a medium load change. Once the second phase is active it stays active all the time.

D. Voltage control loop

This controller aims to keep the DC-link voltage at the desired voltage of 200 V. For this control a PI-controller was implemented. The output of this controller is then multiplied



(a) Two phase interleaving.



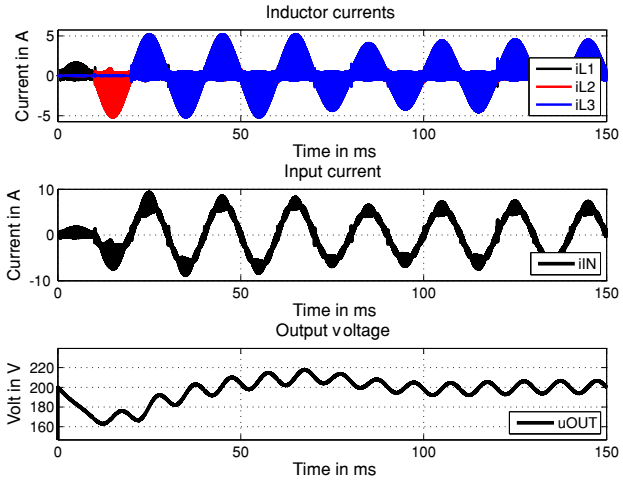
(b) Three phase interleaving.

Figure 6. Phase currents (top) and input current (below) for two and three phase interleaving.

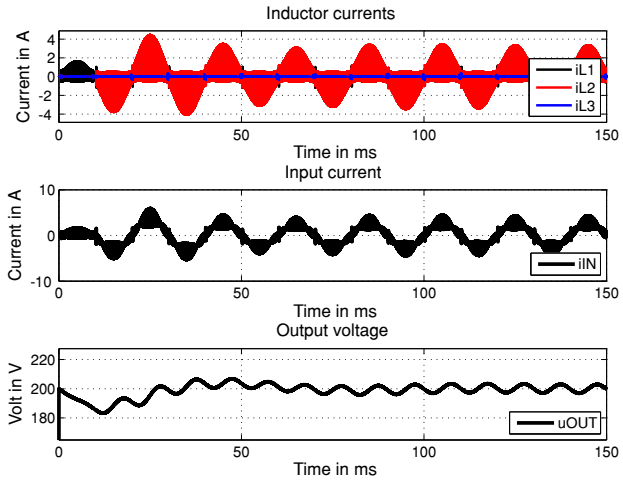
with the line voltage as reference sine i_{ref} and is used for the shape of the input current. For a sinusoidal line input current independent of a change in the control the output of the controller is only allowed to change at the line voltage zero crossings.

E. Timing calculation

With respect to the output values of the above mentioned control loops the timings (T_{on}, T_{off}, and T_R, see Fig. 4) for each phase can be calculated, where T_{delay} is a constant time delay, L is the value of the boost inductors, u_{in} is the line voltage, u_{out} is the DC-link voltage, i_n is the negative current



(a) Load jump from low to high load.



(b) Load jump from low to medium load.

Figure 7. Phase shedding control for different load jumps starting with one phase; (top) phase currents; (middle) input current; (bottom) output voltage.

and i_{Lp} is the peak inductor current.

$$T_{on} = \frac{L \cdot (i_{Lp} + i_n)}{u_{in}}$$
$$T_{off} = \frac{L \cdot i_{Lp}}{u_{out} - u_{in}} \cdot 1.2 \qquad (2)$$
$$T_R = \frac{L \cdot i_n}{u_{out} - u_{in}} - T_{delay}$$

T_{on} is the necessary time which is needed to reach the desired peak inductor current i_{Lp}, but here including the time T_{Rv}. T_{off} is the time which is needed until the inductor current reaches zero again. This value is multiplied in eq. (2) with a safety factor of 1.2, which gives some time to synchronize with the zero current detections. This safety factor is used for the statemachine running on the FPGA. The statemachine enters the next state after detecting a zero current or after the calculated time T_{off} has been reached. This ensures switching even without a zero current condition. For safety reasons a fail counter is implemented inside the FPGA. If T_{off} has been consecutively reached for a certain amount of times all switches are switched off. For T_R the time to reach the negative current i_n is calculated and afterwards a constant delay T_{delay} is substracted. This delay will be evaluated on the prototype and consists of the propagation delays of the ZCD detection and of the logic inside the FPGA.

F. Computation power limitations

For input voltages smaller than half the output voltages no negative current is necessary to achieve ZVS conditions. Also the minimum required negative current for higher input voltages can be calculated. Switching at the minimum required negative current can save losses during high load conditions, but this comes at the cost of computation power. On the contrary, in low load conditions the switching frequency increases producing more gate and switch off losses. To balance these losses, a constant negative current can be used to limit the switching frequency and reduce the switching losses. Also setting the negative current to a constant value over the whole line period saves the necessary computation power for looking up the "optimum negative current value" in a look up table (LUT). To further reduce the required computation power the resonant timings are kept constant. This leads to some higher conduction loss through the body diodes of the MOSFETs, but in simulation this loss turned out to be small (around 400 mW at full load).

V. Control Strategy Complementary Controlled ZVS Bridge

The complementary controlled ZVS bridge [5] is similar to the conventional phase shifted ZVS bridge well known in industry. There is just a slight difference in the control pattern, which is shown in Fig. 8. The current doubler rectifier on the secondary side has only half the current through the output inductors compared with the center tapped rectifier. Fig. 8 also shows V_P as the voltage across the primary transformer winding, I_P as the current trough the primary transformer winding and V_{Sz2}, V_{Sz4} as the voltages across the bottom primary switches from Fig. 3. As mentioned in [5] the advantage of this topology is that it creates the gate signals for the synchronous rectification MOSFETs S_{Ss3} and S_{Ss4} on the secondary side naturally on its own. The voltages across V_{Sz2} and V_{Sz4} are identical to the perfect gate signals. V_{Sz2} controls the MOSFET S_{Ss4} and V_{Sz4} controls S_{Ss3}.

To control the complementary ZVS bridge both the microcontroller and the FPGA are used. Since this part is running on a fixed frequency the control could also be done exclusively

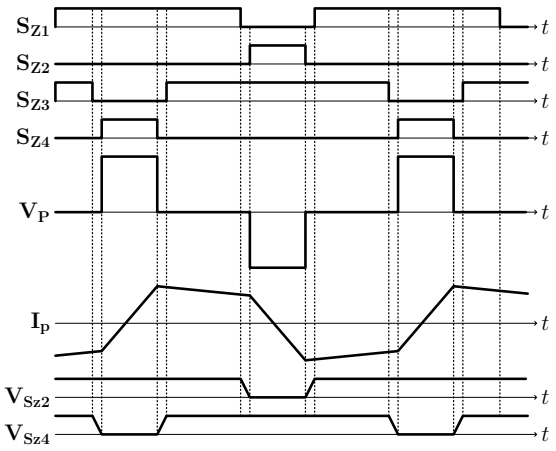


Figure 8. Complementary controlled ZVS bridge signals.

on either the microcontroller or the FPGA. Here the duty cycle is calculated on the microcontroller and then transmitted via qSPI to the FPGA. The four required switching signals for each primary switch are then generated from the FPGA. The secondary switches can be controlled either directly from the FPGA or as implemented in the first prototype directly controlled with the measured voltage V_{Sz2} and V_{Sz4}.

VI. Simulation of the Circuit

A. Implementation

The simulations were carried out with MATLAB/Simulink coupled with Gecko [6]. For the control of the PFC, a method similar to the one shown in [3] or [7] was implemented. For the calculation of the switching times, parasitic values of the components were also considered. These included the equivalent series resistances (ESR) of the boost inductor, the on-resistances of the MOSFETs (R_{DSon}), the parasitic stray inductances of the MOSFET packages, the ESR of the DC-Link capacitors and the output capacitances of the MOSFETs C_{OSS}. Additional losses like the MOSFET off switching and the gate losses were calculated during the simulation. The on switching losses were assumed to be zero, since every MOSFET is turned on under ZVS condition. Also the AC losses (skin and proximity effect) from the inductor and transformer windings have been considered, as well all the core losses have been estimated.

B. Modelling of the MOSFET

Since the simulation software Gecko calculates with ideal switches with a choosable R_{DSon} the MOSFETs are modelled as shown in Fig. 9, where L_d and L_s are the parasitic drain and source inductivities and C_{OSS} is the nonlinear output capacity of the MOSFET, see Fig. 10.

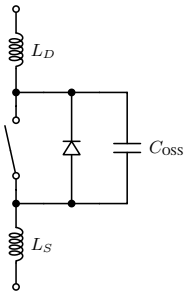


Figure 9. Model of a MOSFET in Gecko.

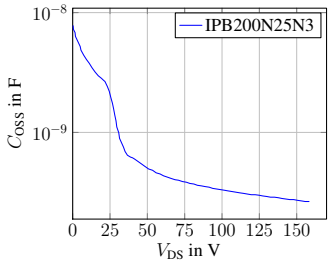


Figure 10. Output capacity over V_{DS} from the MOSFETs on the primary side.

C. Gate drive losse

The gate drive losses were estimated by counting the turn-on events of every switch and are then calculated with eq. (3) with Q_G as the gate charge and V_G as the gate driver supply voltage.

$$P_{Gate} = Q_G \cdot V_G \tag{3}$$

D. Switch off loss

The switch off losses were estimated with the fall time t_F from the datasheet, the actual current at the turn-off event i_{off} and the voltage across the MOSFET after the turn-off event v_{off}. It was assumed that the current decreases linearly to zero and the voltage increases linearly from zero to v_{off} in the time t_F, see eq. (4).

$$\begin{aligned} P_{TurnOff} &= \int_0^{t_F} v_{off}(t) \cdot i_{off}(t) dt \\ &= \frac{v_{off}(t_F) \cdot i_{off}(0) \cdot t_F}{6} \end{aligned} \tag{4}$$

E. Core loss

For the calculation of the core losses of the inductors and the transformer the improved general Steinmetz equations (iGSE) formulas have been used [8], [9], [10], see eq. (5),

$$P_v = \frac{1}{T} \int_0^T k_i \left| \frac{dB}{dt} \right|^{\alpha} (\Delta B)^{\beta - \alpha} dt \,, \tag{5}$$

where α and β can be used directly from the given Steinmetz parameters and k_i can be calculated from the Steinmetz parameters

$$k_i = \frac{k}{(2\pi)^{\alpha-1} \int_0^{2\pi} |cos\theta|^{\alpha} 2^{\beta-\alpha} d\theta} \,. \tag{6}$$

For the PFC stage the sinusoidal input line voltage waveform was split into n parts [11], [12], see Fig. 11. For each part of the sinewave the triangular current shape according to Fig. 4 for the specific DC input voltage is calculated. Then, for this triangular input current the magnetic field strength H and with the material $B - H$ curve the magnetic flux density B is determined. Together with the Steinmetz parameters and eq. (5) the core losses P_{cn} for this specific part of the sine are

calculated. This has been done n times for every part of the first quarter of the line input voltage sinewave. Afterwards the total core loss is equal the average of all P_{cn}.

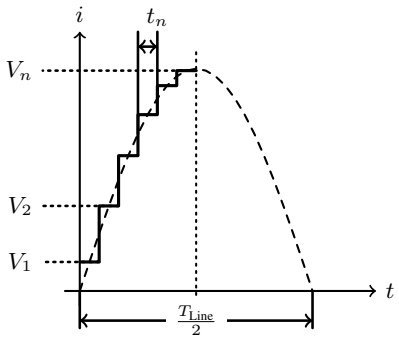


Figure 11. Splitting of the input current sine for the PFC for a fast core loss estimation.

For the calculation of the transformer iron loss the maximum flux density was evaluated with the magnetization current at 10% load. The loss was then evaluated with the help of the loss charts for an operation frequency of 100 kHz.

F. AC Loss

The AC losses in the copper wires of the inductors and transformers have been considered as losses due to the skin effect and the proximity effect for round conductors. The skin effect losses can be described with eq. (7), from [13],

$$P_s = \frac{4}{\sigma\pi d^2}\frac{\xi}{2}\frac{\hat{I}^2}{2}\frac{K_{\text{ber}}(0,\xi)K'_{\text{bei}}(0,\xi) - K_{\text{bei}}(0,\xi)K'_{\text{ber}}(0,\xi)}{K'_{\text{ber}}(0,\xi)^2 + K'_{\text{bei}}(0,\xi)^2} \tag{7}$$

and the proximity effect with eq. (8) also from [13].

$$P_p = \frac{2\pi\xi}{\sigma}\hat{H}^2\frac{K_{\text{ber}}(2,\xi)K'_{\text{ber}}(0,\xi) + K_{\text{bei}}(2,\xi)K'_{\text{bei}}(0,\xi)}{K_{\text{ber}}(0,\xi)^2 + K_{\text{bei}}(0,\xi)^2} \tag{8}$$

with

$$\xi = \frac{d}{\sqrt{2}\delta} \qquad \delta = \frac{1}{\sqrt{\pi f\sigma u_0}}, \tag{9}$$

where d is the diameter of the wire, δ is the skin depth, f the frequency, u_0 is the magnetic constant, σ is the electric conductivity, $\hat{I}$ is the peak current and $\hat{H}$ the peak magnetic field strength in the conductor. K_{ber} and K_{bei} are the Kelvin functions of the first kind for the order zero or two (first index). K'_{ber} and K'_{bei} are the derivatives of the original Kelvin functions. These equations are only valid for sinusoidal currents. To calculate the losses for nonsinusoidal currents a fourier transformation of the current waveform is needed. For each component of the fourier transformation the skin and proximity effect losses are calculated and the sum is taken to obtain the total loss.

G. Efficiency evaluations

For the calculation of the efficiency in Fig. 12 the case with a DC-link input voltage of 200 V for the DC/DC converter was chosen (see Fig. 16). A constant loss of 1 W for the control circuit has also been added to the total losses.

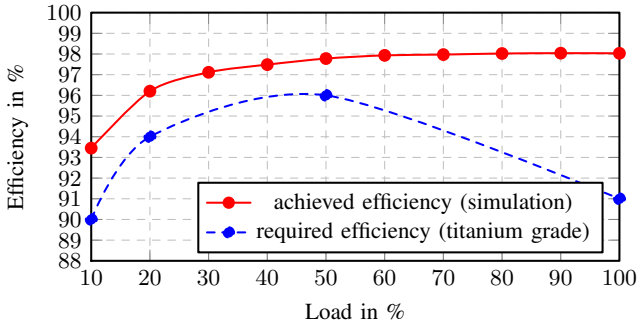


Figure 12. Simulated efficiency of the whole SMPS; achieved efficiency with simulations (red, solid); required efficiency for titanium grade (for high line) (blue, dashed).

Fig. 13 shows a breakdown of the losses of the PFC. The increase of the gate drive losses from 30% to 40% load is due to having two active phases above 33% load. The same effect can be observed between 60% and 70% load. At low load the gate losses are the main losses and at high load the losses of the boost coil (core, conduction, and AC losses) are the main losses. Fig. 14 shows the efficiency curve over the load. It can be seen that the efficiency never decreases below 98%, even at low load. It also shows the advantage between a control with and without phase shedding especially in the low load region.

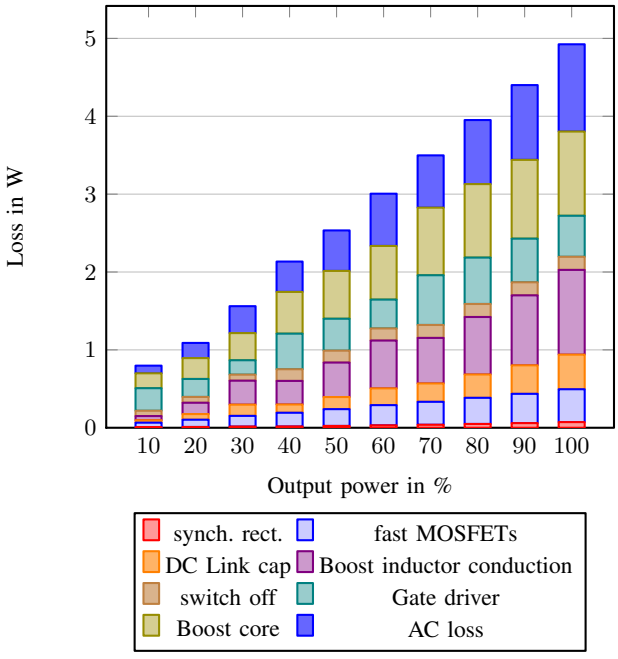


Figure 13. PFC loss breakdown for a single stage with phase shedding over different load points (100% load correspond to 500 W).

Fig. 16 shows the efficiency for the complementary controlled ZVS bridge over the load for different DC-link volt-

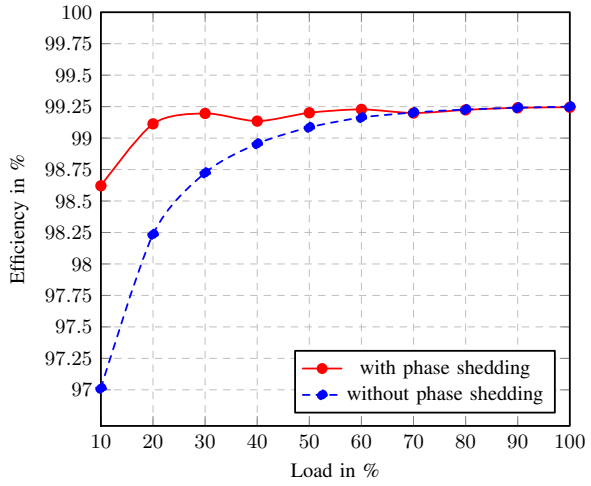


Figure 14. PFC efficiency over the load; (red, solid) with phase shedding; (blue, dashed) no phase shedding.

ages. At high loads the efficiency increases slightly for lower DC-Link voltages due to the increased duty cycle. Fig. 15 shows the corresponding loss breakdown. The high conduction loss of the synchronous rectifiers at high load and the high core loss from the filter inductors at low load compared to the other loss sources is noticeable. To increase the efficiency towards higher loads additional MOSFETs could be paralleled. To increase the efficiency at low load larger filter inductors could be used, to minimize the delta of the magnetic flux density and therefore the core losses.

H. Electronic components

The simulations are based on the electronic components shown in Tab. I. The synchronous rectifier switches S_{S1} and S_{S2} on the primary side each of which are paralleled three times. The synchronous rectifier switches on the secondary S_{S3} and S_{S4} side are single unparalleled switches.

Table I
RELEVANT ELECTRONIC COMPONENTS.

Part	Description	Details
1	primary switches	OptiMOS™, 250 V, 20 mΩ, IPB200N25N3G
2	secondary switches	OptiMOS™ , 60 V, 2.8 mΩ, BSB028N06NN3G
3	boost cores	Magnetics 55550A2, MPP, 180 uH
4	transformer core	Vacuumschmelze, Vitroperm 500F, 10:2, T60004-L2050-W434
5	output filter cores	Magnetics 55547A2, MPP, 13 turns

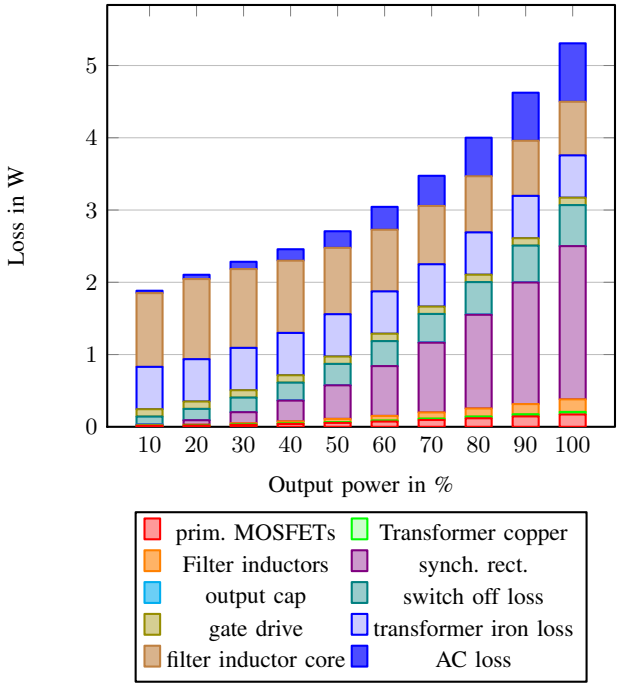


Figure 15. Complementary controlled ZVS bridge loss breakdown for 200 V DC link voltage.

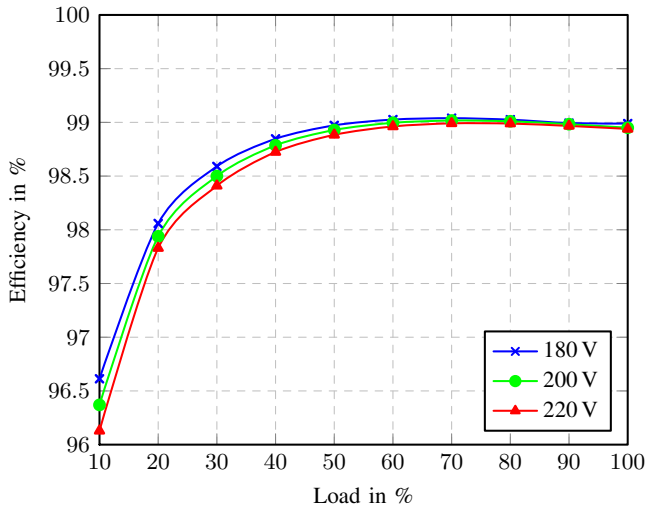


Figure 16. Complementary controlled ZVS bridge efficiency over the load; (blue, crosses) 180 V DC link voltage; (green, dots) 200 V DC link voltage, (red, triangles) 220 V DC link voltage.

VII. Conclusion

The simulated performance of the TCM PFC as well for a complementary controlled ZVS bridge with low voltage MOSFETs was shown and the results look promising. It clearly shows the advantages of using lower voltage MOSFETs with a better FOM like the OptiMOS™ and it shows that the titanium grade which currently exists only for high line may also be achieved for low line input. The prototype for the verification of the simulation results and the new concept is currently in developement.

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