New Electrical Overstress and Energy Loss Mechanisms in GaN Cascodes

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***Abstract*— Depletion-mode Gallium Nitride Field-Effect Transistors (d-mode GaN FETs) need to be cascoded with a low-voltage enhancement-mode (e-mode) Si FET in order to satisfy the safety requirements of the power electronics industry. We find that the standard GaN cascoded structure is susceptible to electrical overstress and additional energy loss mechanisms. This paper provides an understanding of these mechanisms and their effects on both electrical overstress and energy loss. It also provides a method to measure the loss, and presents a benchmarking figure-of-merit. The insights will also be relevant for other wide-bandgap depletion-mode cascoded solutions e.g. SiC JFET, and are important for the successful design of cascoded solutions.**

Keywords—GaN, cascode, avalanche, turn-on loss, turn-off loss, soft switching, overstress, capacitor balance

I. INTRODUCTION

Gallium Nitride FETs are of great interest for power electronics. They are, however, naturally depletion-mode (d-mode) due to the presence of a naturally-occurring Two-Dimensional Electron Gas (2DEG) conducting channel formed by polarization charges [1]. D-mode devices are normally on, raising safety concerns and leading the industry to focus on normally-off e-mode solutions. While there are a few e-mode GaN FETs available [2,3], many GaN FET manufacturers are releasing d-mode devices cascoded with a low-voltage Si FET as a composite e-mode FET [4,5,6,7]. While some of the disadvantages of the regular cascode are known, e.g. lack of slew-rate control, and avalanching of the low-voltage Si FET due to static voltage sharing [8,9], others are not well known or documented, particularly in dynamic operation.

GaN FETs, due to their high switching speed, are of great interest for the miniaturization of power converters, since an increase in the switching rate results in smaller passives. High voltage, high switching rate converters are typically soft-switched, in order to maintain high efficiency, by recovering the energy stored in the output capacitance, Coss. We have found, however, that GaN cascodes can have additional energy-loss mechanisms, both during turn-off and during turn-on. While in hard-switching, this energy is lost anyway, these losses will limit energy recovery during soft switching. Losses due to these mechanisms can be avoided by using the safety-FET cascode architecture as in [10].

To gain an understanding of both the voltage overstress and energy loss mechanisms, we have tapped into the internal "floating" node of a GaN cascode structure. The findings are described in this paper.

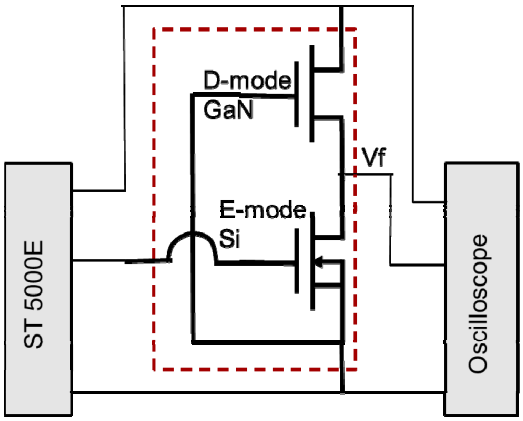

Fig.1: Setup for pulsed measurements. The dashed outline represents the two co-packaged devices

II. VOLTAGE OVERSTRESS

The cascode was dynamically pulsed using a Scientific Test Inc. ST-5000E instrument. The test setup is shown in Fig. 1. Both the GaN and Si FETs are co-packaged. Vds pulses were applied to the drain of the cascode, while keeping the gate off at 0 V. Waveforms are shown in Fig. 2, where Vds is pulsed till 30V and the floating node voltage, Vf, is monitored.

In Fig. 2, the Vds and Vf scales are the same, and the figure clearly shows that Vf follows Vds till about 8 V, and then diverges. This is the point at which the GaN FET shuts off. Interestingly, Vf continues to rise after the GaN FET shuts off until the point where Vds stops rising. Vf then decays until it falls back to a value of about 8 V. The behavior can be explained as follows: as Vds rises, displacement current flows through the GaN drain-to-source capacitance (Cds) and charges up the floating node. The voltage Vf is governed by the capacitor divider between Cds of the GaN FET and output capacitance (Coss) of the Si FET.

At low values of Vds, Cds of GaN FETs can be high, so the effect is enhanced. Once Vds stabilizes, Vf decays due to the Idss0 leakage through the Si FET and falls to a voltage such

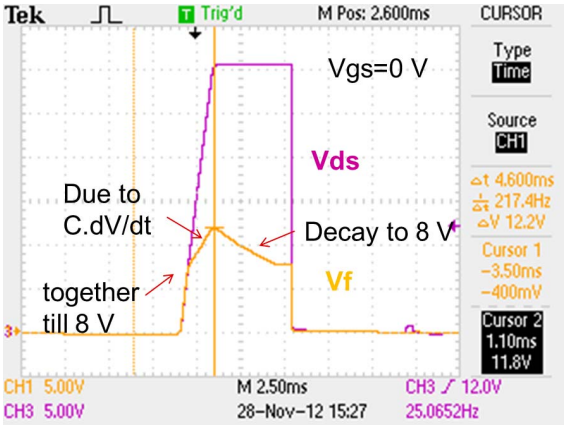

Fig. 2: The drain voltage of the cascode is pulsed till 30V with the Si FET off, and the floating node voltage, Vf, is monitored.

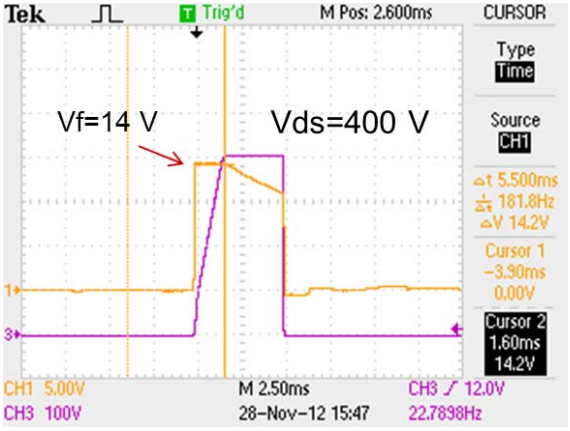

Fig. 3: When Vds is pulsed to 400V, the Si FET avalanches due to the floating node voltage, Vf, reaching BV.

that the leakage current through the GaN FET equals that of the Si FET. A lower Vf increases the leakage through the GaN FET, and the fact that Vf falls means that at 30V, the leakage through the GaN FET is very low.

If the drain is pulsed to higher voltages, it can cause the Si FET to avalanche. Waveforms with Vds=400 V are shown in Fig. 3. As Vds rises to 400V, Vf rises to the breakdown voltage of the Si FET, causing it to avalanche. Vf then decays towards a steady-state static value. As seen from Fig. 3, the peak value of Vf is 14 V. This is the breakdown voltage of the Si FET.

At higher voltages, as shown in Fig. 4 for 500V, the Si FET avalanches during the entire off-state pulse. This is because the leakage current of the GaN FET becomes higher than the Idss0 of the Si FET, thereby driving it into breakdown. As Fig. 4 shows, the avalanching of the Si FET occurs during both dynamic and static conditions. Dynamic avalanching is due to displacement current flowing through the Cds of the GaN FET during the rising edge of Vds. Static avalanching is caused when the leakage current of the GaN FET exceeds that of the Si FET. Regardless of the cause, both Si and GaN FETs are subjected to stressful conditions which may decrease their lifetime.

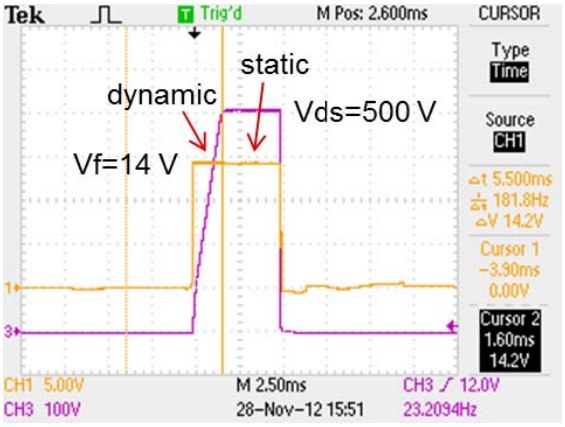

Fig. 4: At higher Vds (500V), the leakage through the GaN FET becomes larger than that of the Si FET. This drives the Si FET into avalanche even when Vds is static.

A higher-voltage Si FET may be chosen to prevent avalanching, but higher voltage FETs have larger specific Rds-on. Additionally, the GaN FET would then need to be reliable for the higher negative gate-source voltage. It is also possible to limit the maximum Vf by using a clamp [4] to protect against overvoltage from switching transients, or from large GaN FET leakage at high Vds.

III. ENERGY LOSS

The goal of soft-switching applications is to recover the energy, Eoss, stored in Coss. It is therefore important to carefully evaluate energy loss effects. One such effect was reported for Si power MOSFETs in ref [11]. Here we report two different mechanisms that cause energy loss in the cascode structure. The loss happens both in hard and soft-switching. In hard switching, however, the energy, Eoss, would be lost anyway, therefore these losses are important for soft-switching. We describe them below, and propose a method of measurement and figure-of-merit to benchmark different cascode devices.

A. Avalanche loss during the turn-off transition

The first mechanism is the *avalanche loss* due to the Si FET being driven into breakdown by the rise of the floating node voltage during turn-off. It will also occur when a clamping element is used to limit the rise of Vf. It can be calculated if C-V curves are available for both GaN and Si FETs. Since the Cds of the GaN FET and the Coss of the Si FET are in series, one may use the conservation of charge as follows:

$$Q(avalanche)=Qds\_GaN(Vdd - BV\_Si) - Qoss\_Si(BV\_Si) + Qoss\_Si(Vt\_GaN) \quad (1)$$

Where the first term represents the charge stored in the GaN Cds, and the remaining terms represent the charge in the Si Coss after the GaN FET turns off. Vds is the drain-source voltage across the cascoded solution. The energy loss per cycle is then calculated by multiplying *Q(avalanche)* by the BV of the Si FET

A useful normalization and figure-of-merit is the power dissipated per ohm of on resistance at 1 MHz operation. For the FET described above, this is 40 mW* Ω /MHz. This means that for a 100 mΩ cascode switching at 500 kHz, this power dissipation would be 0.2W.

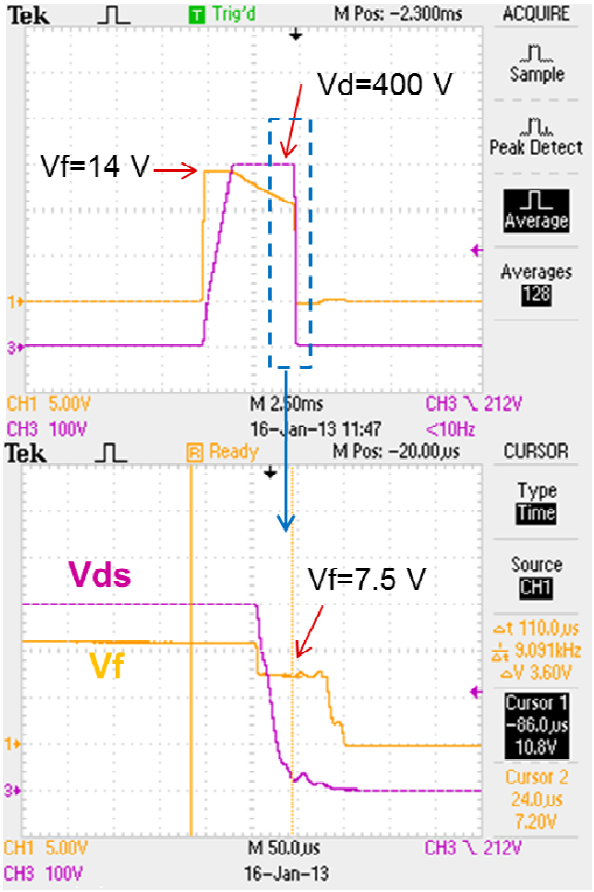

Fig.5: A zoom-in of the turn-on transition, showing that the floating node voltage, Vf, has a plateau at 7.5V while Vds is falling. The GaN FET is weakly conducting during the plateau in order to restore the capacitor charge balance.

B. Early turn-on loss during the turn-on transition

When either the Si FET avalanches during turn-off, or a clamp shunts some charge, an imbalance is created between the charge stored on the Cds of the GaN device and the charge stored on the Coss of the Si FET. This causes Vf to be lower than it would have been without avalanche or clamping. Now consider the example of a soft-switching zero-voltage transition prior to turn-on, when the drain voltage of the cascode drops with the device off. As the GaN drain voltage drops, there is a corresponding drop in Vf. However, since Vf was reduced due to avalanche during turn-off (or due to clamping), Vf drops to the Vt of the GaN device before the Vds of the GaN device is fully lowered. This causes the GaN device to start conducting, which restores the capacitor charge balance. This keeps Vf at approximately Vt during the remaining turn-on transition, as shown in Fig. 5. At the end of the transition, the charge imbalance has been corrected by the same amount of charge flowing through FET conduction as was lost during avalanche. However, the energy loss is higher since the charge flows at a higher voltage. The energy loss equals the energy stored in the drain-source capacitance of the GaN FET at the onset of the GaN FET turn-on, i.e. at the drain voltage (defined as Vdt) at which Vf falls to Vt. At this point, the voltage across the GaN FET is approximately Vdt-Vt, and the following charge balance holds:

$$Qds\_GaN(Vdd\text{-}BV\_Si) - Qds\_GaN(Vdt\text{-}Vt\_GaN) = Qoss\_Si(BV\_Si) - Qoss\_Si(Vt\_GaN) \quad (2)$$

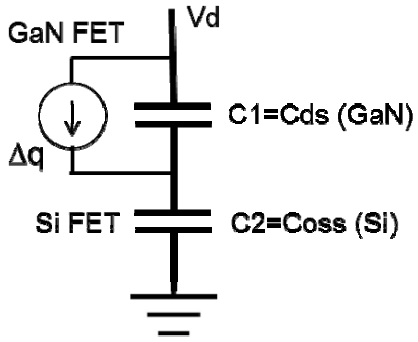

Fig. 6: Equivalent circuit of the cascode for the turn-on loss derivation, showing the capacitor divider between the two FETs. The capacitance C2 is treated as fixed, since the voltage across the Si FET is approximately the Vt of the GaN FET.

An expression for the energy loss may be derived by considering the equivalent circuit in Fig. 6. The figure shows a capacitor divider comprising C1 and C2. It also contains a charge source (the GaN FET turning on) to replace the charge lost from C2 as Vd drops. C2 equals the Coss of the Si FET with its drain at the Vt of the GaN FET. C1 is the voltage dependent drain-to-source capacitance of the GaN FET.

We start with the basic energy equation:

$$dE = V1\, dQ \quad (3)$$

Where E is energy, V1 is the voltage across the GaN FET and dQ is the charge replaced by the GaN FET turning on. dQ is equal to the charge lost from C2 as the drain voltage drops.

$$dQ = \frac{C1(V1)\times C2}{C1(V1)+C2} dVds \quad (3)$$

Vds can be expressed in terms of V1 by using the capacitor divider voltage equation. Expressing Vds in terms of V1 and substituting in (1)

$$dE = (C1(V1) \times V1) dV1 \quad (4)$$

Integrating (5) over the Vds drop gives the the energy loss:

$$E = \int_0^{Vdt-Vt} (C1(V1) \times V1) dV1 \quad (5)$$

This is the energy "Eds" of the GaN Cds at the onset of early turn-on. Therefore, using C-V curves for GaN and Si FETs with the above equations, the energy loss can be calculated.

IV. MEASUREMENT OF THE CASCODE LOSS

To measure the above losses, which we call the *Cascode Charge-sharing Loss*, we developed a simple board, consisting of the schematic shown in Fig. 7. It consists of a half-bridge to generate a high-voltage pulse and an RC filter to slow down the transitions so that they can be accurately captured by an oscilloscope. The cascode is held off by shorting its gate to its source. Two quantities are measured: the voltage, Vds, across the cascode, and the current, Id, by measuring the voltage across a shunt resistor. A measurement result is shown in Fig. 8. An integral of the drain current results in a value of 2.3 nC*Ω/pulse, which is the charge lost to avalanche. The drain energy is calculated by multiplying Id with Vds and integrating with time. The integrated drain energy is also plotted, showing a normalized value of 0.2 uJ*Ω per pulse. This leads to a figure-of-merit of 0.2W*Ω/MHz. Therefore, if a 0.1 Ω device is operated at 500 KHz, the cascode charge-sharing loss will be 1 W.

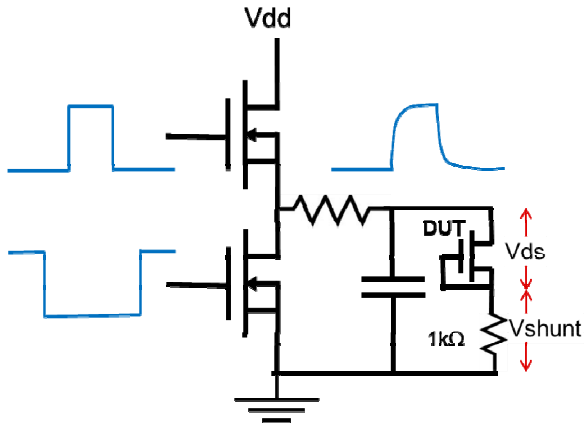

Fig. 7: Schematic of the setup to measure the Cascode charge-sharing loss. The Device Under Test (DUT) is the cascode

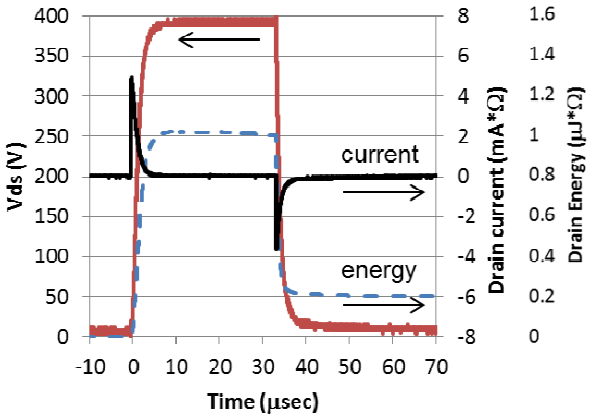

Fig.8: A plot showing the drain voltage, current, and energy as a function of time. The energy at the end of the pulse is the cascode charge-sharing loss per cycle

Using this technique, we have benchmarked several GaN cascodes and have found losses from 0.08 - 0.3 W* Ω /Mhz. showing that it is possible to lower or eliminate the cascode charge-sharing loss. For a given GaN FET, the loss may be eliminated by achieving balanced charging and discharging of the GaN FET Cds and Si FET Coss. This may be done by appropriate specification of the Si FET breakdown voltage and its capacitance Coss.

V. CONCLUSIONS

In conclusion, we present new electrical overstress and energy loss mechanisms for GaN cascodes, a method to measure the loss, and a FOM for benchmarking. We also provide analytical expressions to calculate the loss components. During turn-off, charge is coupled into the floating node through the Coss of the GaN device, which can cause overstress of both the Si drain and GaN gate. If the Si device avalanches, or a clamp is placed to limit the voltage, it causes a new Cascode charge-sharing energy-loss consisting of (a) avalanche loss during turn-off by the Si FET avalanching (or the clamp conducting) and (b) early turn-on of the GaN FET during the turn-on transition.

REFERENCES

[1] O. Ambacher, et.al, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics*, vol. 87, no. 1, pp. 334-344, Jan. 2000.

[2] http://epc-co.com/

[3] http://www.semicon.panasonic.co.jp/en/products/powerics/ganpower/

[4] J. Roberts, G. Klowak, L. Yushna, "GaN Transistors – Drive Control, Thermal Management, Isolation", *Power Electronics Technology*, pp. 24-28, Feb. 2013.

[5] D. C. Sheridan et. al, "Ultra-low Loss 600V-1200V GaN Power Transistors for High Efficiency Applications", *PCIM Europe*, pp. 318-324, 2014

[6] E. Persson, D. Raffo, "Appliance, Motor Drive Performance Improvements Using 600V GaN Cascode FETs", PCIM Europe, Nuremberg, pp. 330-337.2014.

[7] P. Parikh, Y. Wu, L. Shen, "Commercialization of High 600V GaN-on-Silicon Power HEMTs and Diodes", *IEEE EnergyTech*, 2014.

[8] J. Roberts, "GaN Transistors – Grrr or Great?", *Bodo's Power Systems*, pp. 42-43, July 2013.

[9] A. Lidow, J. Strydom, M. de Rooij, D. Reusch, "GaN Transistors for Efficient Power Conversion", Second edition, Wiley, 2014.

[10] M. D. Seeman, S. R. Bahl, D. I. Anderson and G. A. Shah, "Advantages of GaN in a High-Voltage Resonant LLC Converter", *Applied Power Electronics Conference (APEC)*, Ft. Worth, pp. 476-483, 2014.

[11] J. B. Fedison, M. Fornage, M. J. Harrison, D. R. Zimmanck, "Coss Related Energy Loss in Power MOSFETs Used in Zero-Voltage-Switched Applications, *Applied Power Electronics Conference (APEC)*, Ft. Worth, pp. 150-156, 2014.