Gate Driver Design for 1.7kV SiC MOSFET Module with Rogowski Current Sensor for Shortcircuit Protection

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***Abstract*—This paper shows a gate driver design for 1.7 kV SiC MOSFET module as well a Rogowski-coil based current sensor for effective shortcircuit protection. The design begins with the power architecture selection for better common-mode noise immunity as the driver is subjected to high dv/dt due to the very high switching speed of the SiC MOSFET modules. The selection of the most appropriate gate driver IC is made to ensure the best performance and full functionalities of the driver, followed by the circuitry designs of paralleled external current booster, Soft Turn-Off, and Miller Clamp. In addition to desaturation, a high bandwidth PCB-based Rogowski current sensor is proposed to serve as a more effective method for the shortcircuit protection for the high-cost SiC MOSFET modules.**

Keywords—SiC MOSFET Module; Gate Driver; Rogowski Current Sensor; EMI

I. INTRODUCTION

SiC MOSFET as a wide-bandgap device has superior performance for its high breakdown electric field, low on-state resistance, fast switching speed and high working temperature [1]. High switching speed enables high switching frequency, which improves the power density of high power converters. The cost of SiC MOSFET is also gradually decreasing due to the growing of usage in industry applications. Therefore, SiC MOSFET is of great potential in medium-voltage (MV) high power applications as a substitution of MV IGBTs. A well-performed gate driver with sufficient protections is critical to ensure excellent performance of a SiC MOSFET module. The driver must be capable of features such as low propagation delay, high driving current, good dv/dt immunity, and effective protections that includes correct detection and fast response. The basic specifications of the gate driver is shown in Table I, where one example SiC MOSFET Module that the gate driver can be applied to is also shown. The target of this paper is to design a driver that meets the specifications.

For the 1.2 kV IGBTs, a number of commercial driver ICs has been well developed with sufficient isolation rating and protection functionalities. Those driver ICs are fast enough to drive 1.2 kV SiC MOSFETs, and some commercial driver boards are designed based on the ICs. When it comes to 1.7 kV or higher rated voltage of devices, the isolation barrier of the driver ICs becomes insufficient. In commercial designs, fiber-optic cables [2] or pulse transformers [3] are used to realize the

TABLE I. SiC MOSFET and Gate Driver Specifications

Example device part number	Cree CAS300M17BM2
Device voltage rating	1700 V
Device current rating	225 A @T_C=90°C
Gate charge required	1076 nC
Device Package	62 mm
Maximum switching frequency	100 kHz
Maximum Propagation delays	150 ns
Maximum Propagation distortion	20 ns
Driving voltage	+20 V / −4 V
Maximum gate driving current	24 A
Functionalities	Under-voltage lockout; Shortcircuit; Soft Turn-Off; Active Miller Clamp

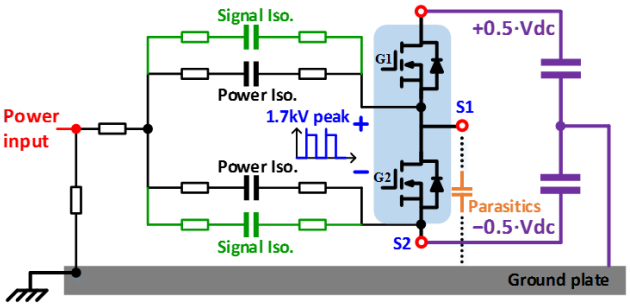

Fig. 1. Common model model of a isolated gate driver circuit

MV isolation for signal channels of the gate driver. Although the isolation requirement is satisfied by using optocouplers, fiber-optics or pulse transformers, the logic signal may still suffer from common-mode noise that is generated by the switching-transient dv/dt. This is analyzed in Section II, and different power/signal architectures are compared based on parasitics model. A best solution is found to minimize the chance of falsely turn-on of device that causes shortcircuit. In Section III, The driver IC is carefully screened and selected among a number of candidates. Detailed circuit design is presented in section IV. A solution of self-balanced paralleled current booster was proposed not only to meet the driving current capability but also to enable the two-level soft turn-off upon shortcircuit. The Soft Turn-Off (STO) mechanism is analyzed, and the parameter is design. A circuit for Active Miller Clamp (AMC) is proposed to solve a threshold issue

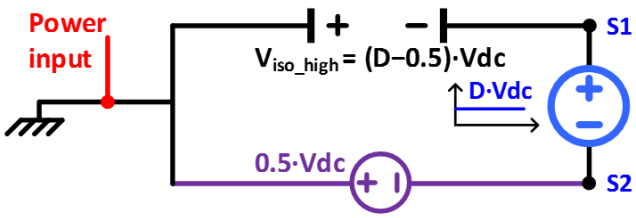

Fig. 2. DC analysis of the gate driver model

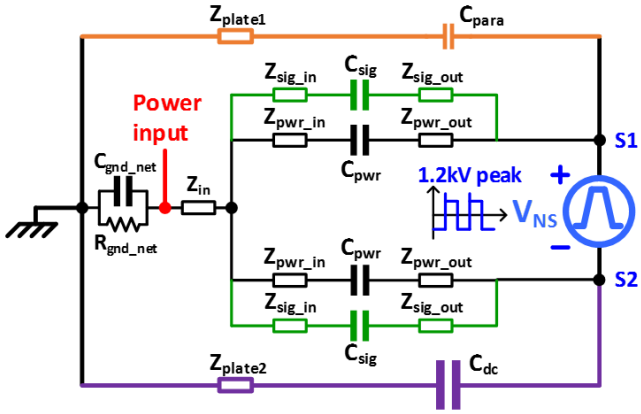

Fig. 3. AC analysis of the CM model of gate driver considering parasitics

limited by the driver IC. Due to the difference in output characteristics between SiC MOSFET and IGBT, the desaturation approach for shortcircuit protection may not be effective anymore. This is analyzed in Section V, and a Rogowski-coil based current sensor is proposed as another protection layer of shortcircuit. Experimental validations are shown together with the description of the designs.

II. Power Architecture Design

According to the specifications, the maximum switching transient can be as high as 1700/50 = 34 ns. Then the gate driver must be able to operate under the noise source below 15 MHz. A simplified model with gate driver parasitics in Fig. 1 represents the common-mode (CM) noise propagation in conventional gate driver configurations. Each trace in the figure indicates the ground path of different isolated voltages. The capacitor in the figure represents the coupling effect at isolation barriers. The rectangles in the figure is the impedances of the circuit traces. Note that the high-side gate driver ground is sitting on the source terminal of the high-side SiC MOSFET, which is jumping between the positive and negative rail at the switching transient. The voltage between S1 and S2 can be modeled as a noise voltage source because it is not impacted by the parasitics of the CM model. The signal isolation barrier is generally achieved by an isolated driver IC/optocoupler for 1.2 kV device, or by fiber-optics/pulse transformer for 1.7 kV device or higher. Any high-frequency noise current flowing through the signal path isolator can induce a voltage drop on the ground trace impedance, which will be added to the differential-mode logic signal and cause a falsely turn-on of the SiC MOSFET. In conventional designs, the power and signal isolation channels share the same ground at the primary and secondary side, respectively.

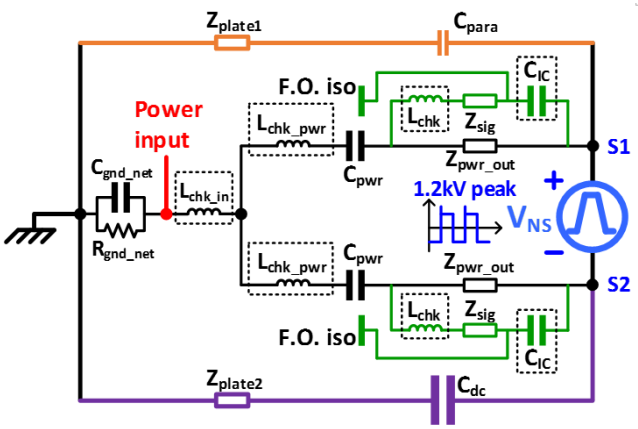

Fig. 4. CM model of the proposed gate driver configurations with high CM noise immunity for the control/logic circuit

A. DC Analysis of the Conventional Design

Fig. 2 shows the DC analysis of the CM model of the gate driver, where the capacitors are open-circuit and all the trace impedances are treated as short-circuit if they are in series with the capacitors. The voltage of one DC-link capacitor C_{dc} is $0.5{\cdot}V_{dc}$, and can be treated as a DC voltage source. The DC voltage of the low-side isolation barrier is 0.5·Vdc and the high-side one is $(D{-}0.5){\cdot}V_{dc}$, where D is the averaged duty cycle of the high-side switch. Accordingly, the low side isolation barrier will take most of the DC voltage stress, for both the signal and power isolations in the conventional design.

B. AC Analysis of the Conventional Design

The AC CM model of the gate driver circuit is shown in Fig. 3. The stray inductance of ground plate is estimated as 30 nH and the resistance as 1 mΩ. The same ground impedance assumption is made for the parasitic capacitance C_{para} whose value is around 0.2 nF. A low high-frequency impedance ground network is connected between the power-input terminal of the gate driver and the ground. All the other ground trace impedances are assumed to be 1 nH and 1 mΩ. The frequency-domain analysis of Fig. 5 tells, firstly, the high-side isolation barrier takes almost all of the high frequency voltage stress up to 20 MHz. At frequency high than 20 MHz, the isolation stress of high side is even higher than the noise source as the coupling capacitance C_{pwr} and C_{sig} resonate together with the ground plane impedance Z_{plane1} and Z_{plane2}. This indicates that the high side isolation barrier is subjected to almost all the AC noise which can even be amplified at certain frequency. Plus, all the AC noise stress will be placed on the coupling capacitance of C_{sig} such that large CM noise current is induced in the signal path. The noise in signal path can cause falsely turn-on, malfunction of logic, and even disable the controller if the noise current flow to the controller along with the signal path. Inserting CM chokes at the signal path will help attenuate the noise current, but the leakage inductance of the chokes will introduce delay or resonance to deteriorate the differential-mode signal.

In order to prevent the CM noise from flowing into the controller, the signal barrier is normally strengthened by using the fiber-optical cables instead of optocouplers. However, the

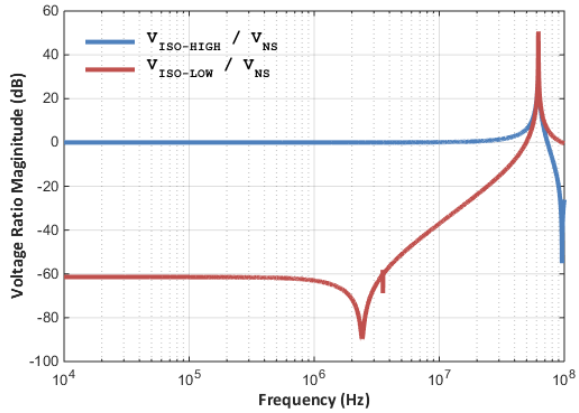

Fig. 5. AC voltage sharing between the high-side and low-side isolations

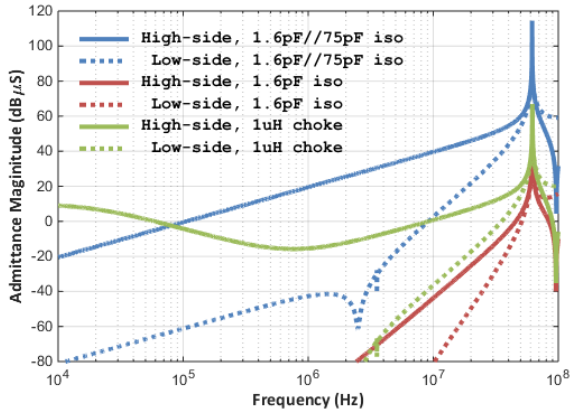

Fig. 6. Comparison between noise-immunity solutions for signal path

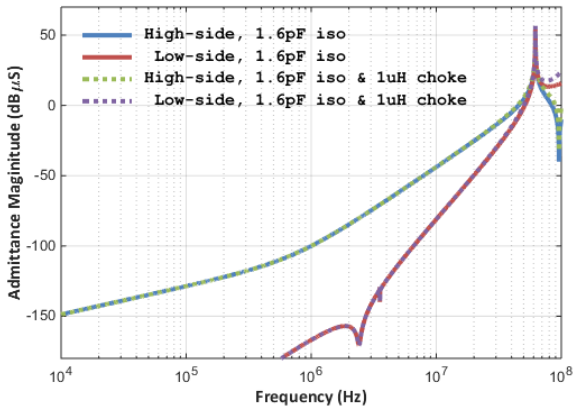

Fig. 7. Comparison to decide if CM choke is needed for signal path

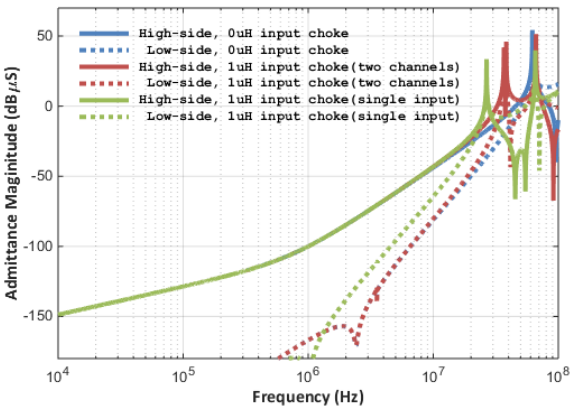

Fig. 8. Comparison to decide if CM choke is needed for power-input path

noise current at the signal path of the driver is still large, as long as the secondary sides of the power/signal isolation barriers share the same ground. The design objective is to increase the impedance mismatch between the signal path Z_{sig_out} and power path Z_{pwr_out}. The improved configuration is shown in Fig. 5. Either adding another isolation barrier or introducing a CM choke for the logic signal power supply will be a helpful solution. For comparison, the admittance from the signal-path noise current to noise voltage source is set as the criteria to represent the performance in noise attenuation. Fig. 6 shows the comparison result of different solutions where the CM choke inductance L_{chk} is selected to be 1 µH and the coupling capacitance of additional isolation barrier C_{IC} is measured to be 1.6 pF. Both of them show significant improvement than the conventional design. The isolation solution has lower admittance than the CM choke one at the wide low-frequency range, and even about 40 dB less at 10 MHz. Plus, as the signal path is paralleled with a low impedance power path, the added isolation barrier will not take any high voltage stress. Accordingly, the additional-isolation solution is selected for the driver architecture design.

To further identify if it brings any benefit by using the choke and the additional-isolation together, a comparison is made in Fig. 7 that shows they have almost the same performance below 50 MHz. Thus, a CM choke is not needed if the isolated-IC is already designed in the configurations.

In order to find out if CM chokes at the power input can further bring down the noise flowing through the signal path, two designs at the power input are made for comparison. In Fig. 8, it shows that one design is to add two 1 µH chokes L_{chk} at the two power channels, respectively, while the other is to add one 1 µH chokes L_{chk_in} at the common input. From the result, the admittance is not reduced significantly, but two more resonant peak is created at around 20~30 MHz, which can possibly be covered by the noise source. Therefore, CM chokes for the power path are not recommended.

It is worth noting that for all the comparison cases, the low-side signal path is always subjected to much less noise current than the high-side. The reason that the grounding network impedance Z_{gnd_net} and the ground plate impedance Z_{plate2} in series with the DC-link capacitor impedance is much lower than the low-side channel at frequency less than 60 MHz. This explains why most of the noise issues in signal path occur at the high-side channel. Based on all the analysis above, the power architecture is designed as shown in Fig. 9. Careful impedance control also need to be taken while designing the PCB layouts.

III. GATE DRIVER IC SELECTION

A. Critical characteristics of a gate driver IC

TABLE II. COMPREHENSIVE FUNCTIONALITIES COMPARISON OF GATE DRIVER IC CANDIDATES

Manufacturer	Part Number	Critical Functionalities				
		Propagation	UVLO	Desaturation	Soft Turn-Off	Active Miller Clamp
Avago	ACPL-332J	(d) 180 ns, 180 ns (r/f) 50 ns, 50 ns	+ 10.3 V	(th) 6.5 V, (r) 300 ns	LRTO	V_{EE} + 2.0 V
Avago	HCPL-316J	(d) 300 ns, 320 ns (r/f) 100 ns, 100 ns	+ 11.1 V	(th) 7.0 V, (r) 300 ns	LRTO	N/A
Fairchild	FOD8318	(d) 300 ns, 250 ns (r/f) 34 ns, 34 ns	+ 10.0 V	(th) 7.0 V, (r) 850 ns	LRTO	V_{EE} + 2.2 V
Toshiba	TLP5214	(d) 85 ns, 90 ns (r/f) 32 ns, 18 ns	+ 10.3 V	(th) 6.5 V, (r) 180 ns	LRTO	V_{EE} + 3.0 V
Infineon	1ED020I12	(d) 170 ns, 165 ns (r/f) 30 ns, 50 ns	+ 11.0 V	(th) 9.0 V, (r) 350 ns	N/A	V_{EE} + 2.1 V
On Semi	MC33153	(d) 80 ns, 120 ns (r/f) 17 ns, 17 ns	+ 11.0 V	(th) 6.5 V, (r) 300 ns	N/A	N/A
ROHM	BM6102FV-C	(d) 150 ns, 150 ns (r/f) 50 ns, 50 ns	+ 11.5 V	(th) 10 V, (r) 3250 ns	2LTO	V_{EE} + 2 V
STMicro	STGAP1S	(d) 100 ns, 100 ns (r/f) 25 ns, 25 ns	+ 13.0 V − 2.0 V	(th) 10 V, (r) 100 ns	2LTO	GND + 2 V

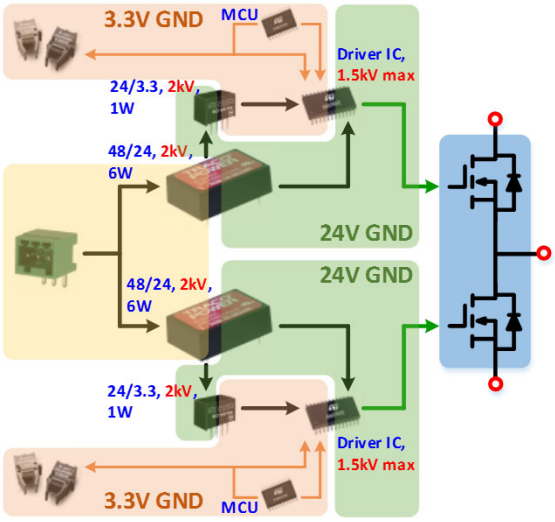

Fig. 9. Designed power architecture for the gate driver

As analyzed that an additional isolation barrier is needed for noise attenuation, it will be preferred to use a gate driver IC instead of an optocoupler, because the IC can provide more functionalities and save space for the driver board. As a gate driver IC for SiC MOSFET, it should propagate the gate signals with low delay, low distortions and low jittering. It should also be able to provide functionalities including undervoltage lockout (UVLO), shortcircuit protection, Soft Turn-Off (STO), and Active Miller Clamp (AMC). When selecting the driver IC, the critical characteristics of the IC should be marked at the first place.

For the SiC MOSFET design to switch at up to 100 kHz, thus the switching period is 10 μs. Typically, it takes 50~100 ns for the given Cree MOSFET module to complete the switching transient. The propagation delay of the driver IC should be as short as possible to ensure the MOSFET can promptly respond to the command from the controller for the control and protection purpose. The mismatch of the driver delays and rise/fall time between the turn-on and turn-off will cause duty-cycle distortions, but it is acceptable if the mismatch are close to delay characteristics of the device itself.

The UVLO is used to monitor the status of the power supply for the driving loop to ensure high switching speed and low conduction loss of the SiC MOSFET. If the power supply cannot maintain the designed voltage any more, the device should shut down and inform the controller. It is preferred to set a higher UVLO threshold, and to monitor the positive and the negative supply voltage at the same time.

The shortcircuit protection is the most critical functionality of the gate driver. As analyzed in Section II, the high-side signal path is usually subjected to high CM noise that possibly brings about falsely turn-on and shortcircuit if the low-side gate signal is also high. The shortcircuit protection can be realized by detecting the device current at its on-state. The detection must respond fast and have high bandwidth as the shortcircuit current can rise at very high di/dt slope. In high current applications, the conventional method to detect IGBT current is to measure the on-state voltage V_{CE} and calculate the collector current according to the device output characteristics. As soon as a very high V_{CE} is detected at on-state, the device is turned off. This is normally named desaturation (DeSat) protection because at shortcircuit the IGBT is deviated from its saturation region. In recent designs, the DeSat is also implemented to protect the SiC MOSFET from shortcircuit. Despite that the DeSat for SiC MOSFET is not as effective as for IGBT, the DeSat functionality is still used in the gate driver of this paper as a second-stage shortcircuit protection. To achieve the DeSat functionality, a driver IC should provide high enough threshold voltage for a given output characteristics of a SiC MOSFET. Also, the response time between detection and turn-off should be as short as possible.

A STO functionality is usually combined together with shortcircuit protection. The turn-off current will be extremely high when the shortcircuit protection is triggered, and a hard turn-off will kill the device due to the induced turn-off voltage spike. Therefore, either a soft turn-off process or a V_{DS} clamp circuit by using TVS diode is necessary for the shortcircuit turn-off. In this paper, the STO is selected because in the latter approach the breakdown voltage of TVS varies in a wide range such that the V_{DS} clamp voltage is difficult to control. In state-of-art designs, two typical STO mechanism are adopted by different driver ICs manufacturers. One is to increase the turn-

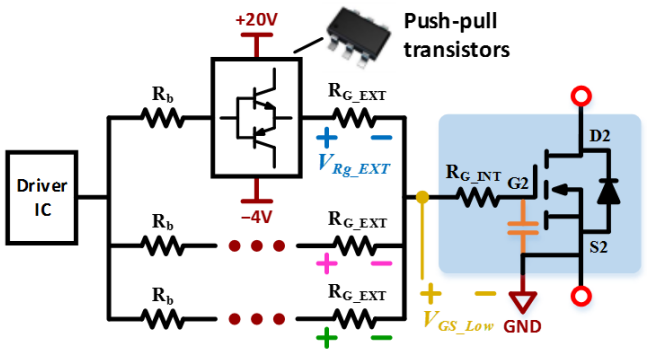

Fig. 10. Schematics of the self-balanced paralleled current boosters

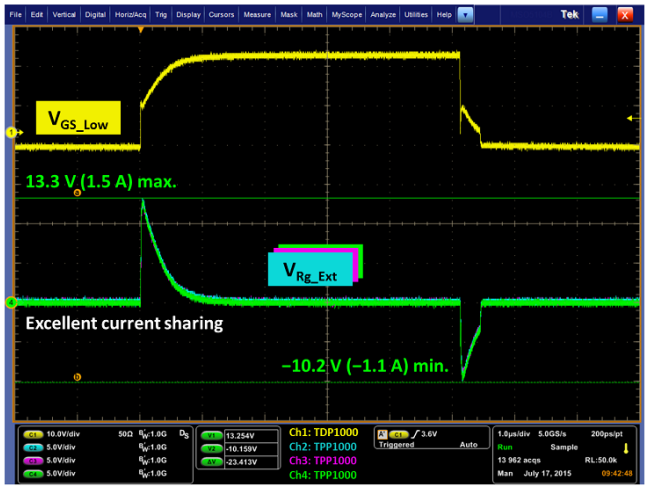

Fig. 11. Current comparison of three paralleled current boosters

off resistance hundreds times higher than normal when soft turn-off is triggered (LRTO), while the other is to use Two-Level Turn-Off (2LTO) voltages. The former approach does not apply to the designs where an external gate current booster is required. The driver IC with 2LTO is preferred, otherwise the 2LTO circuit has to be built by discrete components.

The AMC is the functionality that create a very low-impedance in the gate loop for the device in its off state. In this manner the cross-talk induced noise current will not cast a large noise voltage at the gate voltage V_{GS}. The Miller Clamp detects the gate voltage of the device, and enable the low-impedance path as soon as the gate voltage drop below the threshold. Usually an external bipolar transistor will be used to create the low impedance path, so the on-state resistance of AMC transistor inside the driver IC is not a critical parameter. An important requirement is that the threshold voltage of Miller Clamp should be lower than the device threshold voltage with enough margin, with consideration of the delays brought by the internal gate resistors inside the device package.

B. Gate Driver IC Comparison and Selection

Eight gate driver ICs from seven manufacturers are selected for comparison regarding the critical parameters as mentioned above. In Table II, the values are obtained from public datasheets of the IC manufacturers. In column "Propagation",

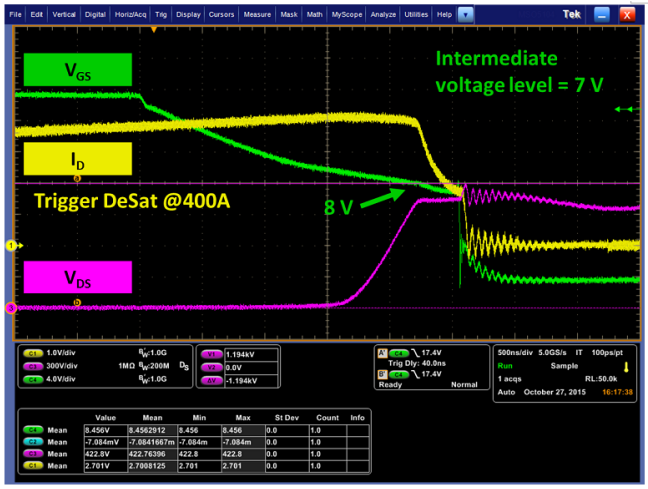

Fig. 12. Test waveform of Soft Turn-Off

"(d)" means delays and the first number indicates the turn-on delay while the second indicates the turn-off. "(r/f)" means rise/fall time and they are corresponding to the two numbers in row, respectively. In column "UVLO", the "+ number" indicates the threshold voltage where the under-voltage lockout will be triggered when the positive supply voltage drops, while the "− number" represents the threshold of the negative one. In column "Desaturation", the first value means the maximum threshold voltage while the second indicates the reaction time. In the column "Soft Turn-Off", two types of soft turn-off mechanisms are shown. In the column "Active Miller Clamp", the thresholds of gate voltage to enable the low-impedance gate loop are presented. Overall, the Driver IC STGAP1S has the best performance in the first four characteristics. The only shortcoming of it is that the AMC threshold voltage is almost the same as the device gate threshold, so the AMC circuit should be designed for this concern. Eventually, STGAP1S is selected to be the driver IC with an isolation barrier.

IV. Functional Circuits Design

The detailed circuits design is carried out based on the selected driver IC. Since the design for propagation and UVLO is determined by the driver IC and the DeSat circuit design can follow [3], this paper focuses only on the design of the current booster, STO, and AMC.

A. Current booster design

As specified in the selected driver IC datasheet [], the source/sink shortcircuit current at the driver output is 5 A, so the SiC MOSFET switching speed may be limited by the driver IC. To meet the 24 A peak driving current in the driver specifications, an external current booster is necessary. Typically, the current booster is a pair of push-pull MOSFETs or bipolar transistors. There is voltage drop on the on-resistance (about 0.3 Ω) of the MOSFET-based booster, which can be as high as 7.2 V when the highest peak current is reached. Therefore, the MOSFET-based booster will take 30% of the total driving loss if the total gate resistance is designed to be 1 Ω, then a very good cooling solution is. As a contrast, the bipolar transistor have a very low voltage drop such that the loss on the current booster will be very small. The

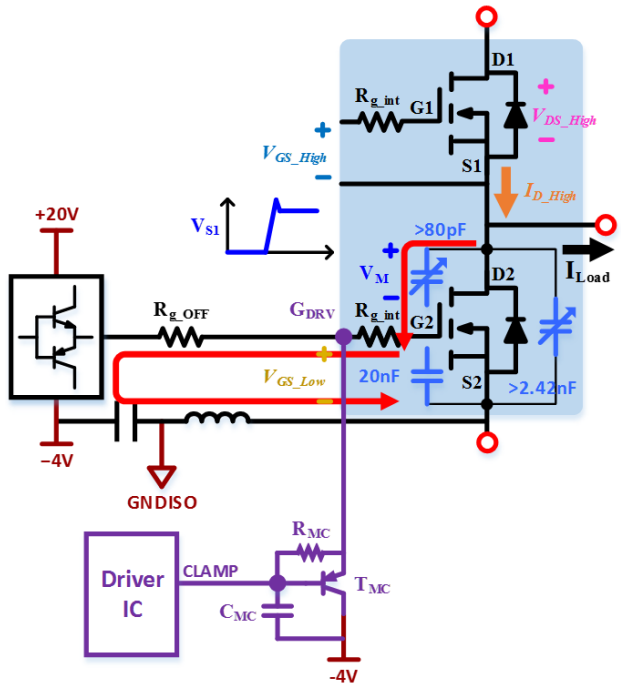

Fig. 13. Schematics of the Active Miller Clamp

disadvantage of the bipolar transistor is its output becomes high-Z if the gate voltage is higher than the positive rail voltage or lower than the negative rail voltage. This will occur when the cross-talk noise current generates a negative voltage spike when the device is at its off-state, as shown in Fig. 15. The recovery time span is determined by the discharging resistance across the device gate and source.

The current booster should be able to work together with the STO. For LRTO, [4] recommended a method by increasing the input capacitance of the current booster but the switching transient will also be delayed by hundreds of nanoseconds even at normal operations, which is not favorable to the SiC MOSFET. For 2LTO, the current booster should be able to deliver the intermediate voltage level following the driver IC output and only the bipolar transistor based current booster can achieve this goal. The highest peak current rating of available commercial transistor-based current boosters is 10 A, so three of the current booster are paralleled as shown in Fig.10. This design has a natural closed loop to balance the output currents of three boosters. When one of the boosters delivers higher current, the voltage drop on R_{G_Ext} will increase so the voltage on the base resistor R_b will decrease. Then the base current will decrease and the transistor emitter current is reduced. Fig. 11 shows the perfect balance of the three paralleled current boosters at switching transient.

B. *Soft Turn-Off design*

The transfer characteristics (I_D vs. V_{GS}) of the MOSFET determines how the gate voltage controls the drain current. The intermediate voltage level in 2LTO should be designed corresponding to the peak normal-operation current according to the transfer characteristics, as the normal turn-off is allowed at this peak current. The duration of this intermediate voltage

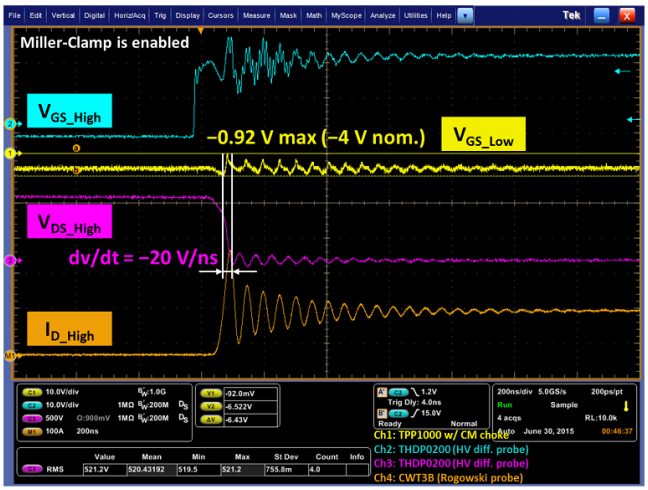

Fig. 14. Test waveform of the cross-talk issue at turn-on

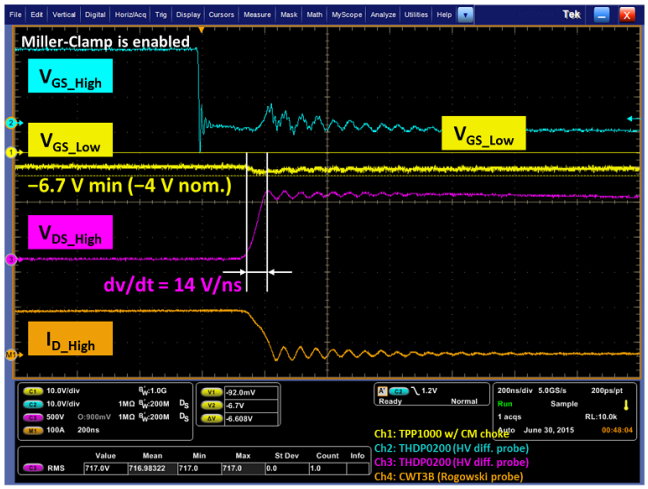

Fig. 15. Test waveform of the cross-talk issue at turn-off

level should be long enough for the drain current drops to the peak normal-operation current. As the date sheet only give the transfer characteristics at one drain-source voltage, but in practical application the drain-source voltage varies with the drain current, the proper intermediate voltage can only be design by tests. Fig.12 shows the STO behavior when the intermediate voltage is designed as 7 V and the time span for the current to drop is about 2 µs.

C. *Active Miller Clamp design*

The AMC design schematic is shown in Fig. 13. A PNP transistor T_{MC} is added to boost the clamp current capability of the driver IC. A resistor R_{MC} is put across the base and emitter to detect the gate voltage. Because the threshold voltage of AMC of the selected driver IC is very close the device threshold voltage, it is possible that the SiC MOSFET is not fully turned off when the AMC is activated, and the MOSFET is always turned off at zero gate resistance. Therefore, a capacitor C_{MC} is added to delay the detection of gate voltage drop, by which means the real gate voltage has dropped to the cutoff region when the AMC is triggered.

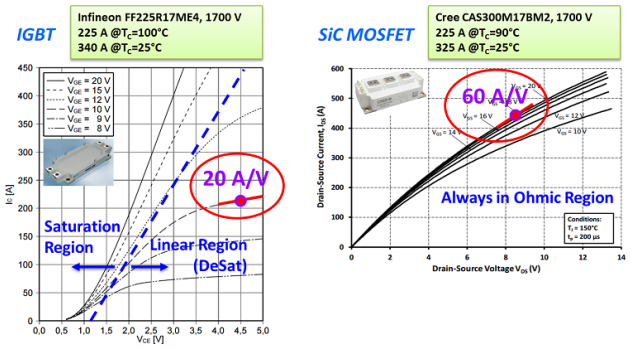

Fig. 16. Device output characeristics comparison, IGBT vs. SiC MOSFET

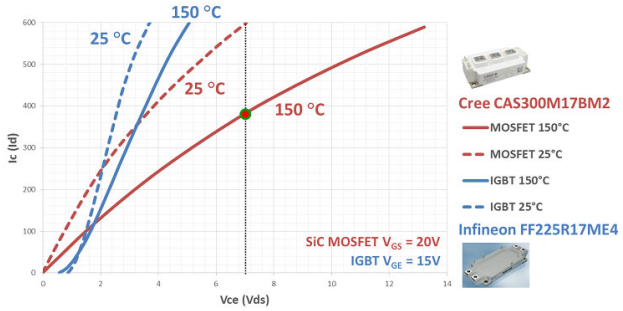

Fig. 17. Device output characeristics comparison against junction temperature

V. Rogowski Current Sensor Design

A. Motivations to design current sensor for gate driver

In recent protection designs for SiC MOSFET, the DeSat method is simply borrowed from the IGBT applications. However, DeSat protection for SiC MOSFET is not as effective as for IGBT because of two main reasons [5].

1) As shown in Fig.17, when shortcircuit occurs in IGBTs, the device drifts away from the saturation region and enters linear region where the current rising slope is getting smaller. Even at steady state of shortcircuit when the IGBT block the entire DC voltage, its collector current is still limited. Thus, the in-time shut down can be achieved easily even with detection delays and sensing errors because the current won't increase very fast. In comparison, however, The SiC MOSFET is still in its omic region where the current rising slope is much faster than IGBTs. At steady state, when the SiC MOSFET blocks the DC voltage, the drain current will rise to an extrmely high value. Therefore, delays or on-stage voltage sensing errors can lead to higher possibility of device damage before it can be shut down in time and safely.

2) Fig.2 shows that the on-state voltage of the SiC MOSFET is more temperature dependent than the IGBT. If a DeSat protection is designed for the nominal junction temperature, then it can never be effective when the device temperature is still low at the startup of the converter. Instead, if the protection is designed for low junction temperature, then it can be falsely triggered at nominal junction temperatures. As a result, the difference between two output characteristics curves in different temperature of the SiC MOSFET make it very difficult to design DeSat threshold voltage.

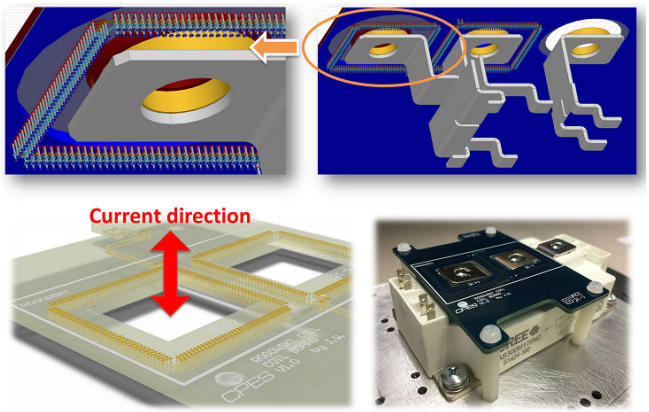

Fig. 18. Rogowski coil 3D model and assembly

As the DeSat protection may not function well for SiC MOSFET, a current sensor is a good additional option to detect the fault current. Reference [6] reviews and compares different current sensing method, including shunt, Hall, current transducer, Rogowski coil, GMR and GMI, concluding that the Rogowski coil has outstanding performances in terms of bandwidth, accuracy, linearity, implementation, profile and cost. Thus, the Rogowski-coil-based current sensor is selected and designed for shortcircuit protection.

B. Rogowski coil design

Because of the limited space between the two power terminals of the 62 mm package, the winding width is designed to be 1 mm. In order to minimize the noise from adjacent conductors, the coil almost encloses the terminal busbar, and has a one-turn winding in the opposite direct to compensate the one-turn effect of the coil. The physical assembly of coil is shown in Fig. 16. The turn number is designed to be 176 turns to minimize the noise flux from adjacent conductors, which is the maximum number that can be achieved by regular PCB fabrication techniques. The measured mutual inductance self-inductance L_S is 359 nH and the equivalent paralleled capacitance (EPC) of the winding C_S is 8.13 pF. These two parasitics compose a low-pass filter with the resonant frequency at 93 MHz, which is almost 5 times of the designed bandwidth of 20 MHz. A damping resistor connected to the output of the coil is designed to be $0.5\cdot(L_S/C_S)^{1/2} = 105\ \Omega$ for critically damped response of the LC resonant circuit.

C. Signal processing circuit design

Signal processing circuit is designed to integrate the di/dt information obtained from the Rogowski coil output. Active integration circuit using operational amplifier is selected instead of RC passive signal circuit to achieve wider sensor bandwidth [7]. The output of the integrator circuit is sent to a low-delay comparator. The output of the comparator is given to high-voltage side of the isolated gate driver IC to switch off the SiC MOSFET. The delay from the device current I_D to the comparator output V_{CMP_OUT} is designed to be less than 20 ns.

The input resistor R_{i1} and integration capacitor C_f determines the transducer gain G_{SENSOR} from device current I_D to comparator input V_{CMP_IN}. Note that the di/dt polarities of the

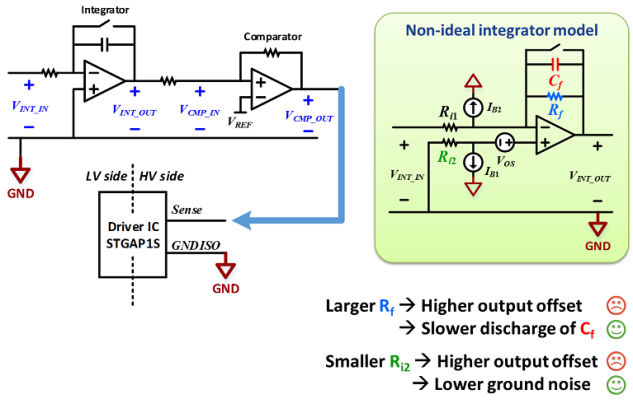

Fig. 19. Signal processing circuit diagram and non-ideal integrator model

positive and negative busbar are opposite and the values are identical with negligible EPC of the load inductor. Therefore, the equivalent mutual inductance is the different between the mutual inductance from the measured conductor and the adjacent conductor.

$$G_{SENSOR} = (M_1 - M_2) / (R_{i1} \cdot C_f) \quad (1)$$

Larger C_f is preferred to prevent integration error caused by C_f discharging. It is finally fine-tuned that R_{i1}= 403 Ω and C_f = 200 pF to achieve G_{SENSOR} = 0.02 Ω. Then the mutual inductance is calculated to be $M_1 - M_2$ = 1.61 nH, which is very close to the simulation result 1.70 nH. The reasonable error is likely caused by the difference between the simulation model and the real assembly.

The general non-idea characteristics of an operational amplifier can be modeled as shown in Fig. 19. The bias current I_{B1} and I_{B2} and offset voltage V_{OS} cause an output voltage offset at V_{OUT} when the input voltage V_{IN} is zero. In conventional designs, the feedback resistor R_f is designed to minimize the effect from offset voltage V_{OS}, and two identical input resistors R_{i1} and R_{i2} is selected to cancel out the effect of from bias current I_{B1} and I_{B2}. The larger R_f leads to higher output offset, but to slower discharge of the C_f such that the sensor gain will not decrease if the device conducting time is long. The smaller R_{i2} leads to higher output offset, but to lower ground noise at the non-inverting input terminal of operational amplifier. The R_f is finally designed to be open-circuit and R_{i2} is zero, in order to maximize the sensing performance. The offset issue can be resolved by an active reset switch. The reset switch is designed to turn on for a very short time when the SiC MOSFET is switched off. The tests setup is in Fig. 20. The result in Fig.21 shows that the Rogowski current sensor has fast enough response to capture the shortcircuit current of SiC MOSFET.

VI. Conclusions

The most important aspects in designing an industry-oriented gate driver for SiC MOSFET has been presented in this paper. Solutions to resolve critical issues are proposed and supported by experimental validations.

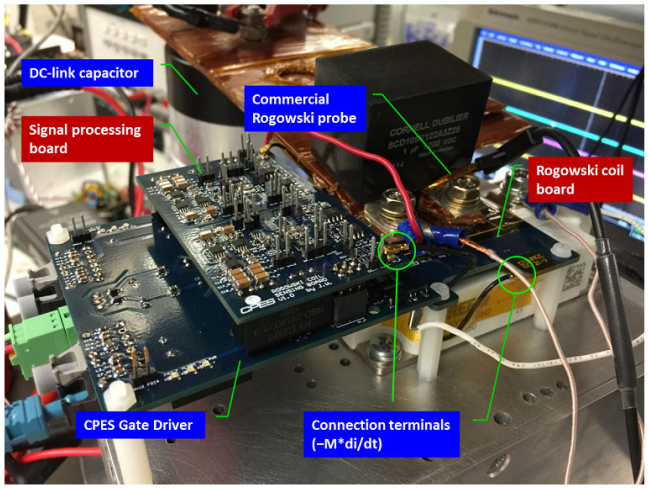

Fig. 20. Test setup and circuit boards

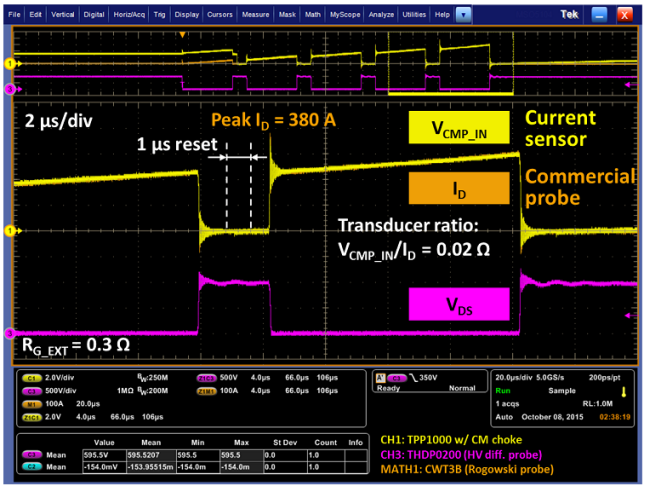

Fig. 21. Switching transient performances of the Rogowski current sensor

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