Virtual test reduces semiconductor product development time

by T. Hogan and D. Heffernan

In the semiconductor industry's evolutionary life cycle, the speed at which products are introduced to the market-place is key to the competitive success of individual companies. The semiconductor industry is classed as a fast-changing industry in which product technology, manufacturing process technology and industry organisation need to be continuously updated in relatively short cycle times. This paper looks at the test engineering aspect of the IC (integrated circuit) product development process and describes how an emerging 'virtual test' methodology can be effectively applied to reduce the overall product development time for semiconductor devices.

1 Virtual test

Virtual test is an emerging methodology that allows test engineers to create an early simulation of the manufacturing test environment for a new semiconductor IC product. In a virtual-test environment the test programs that will be used in the manufacturing test of the IC product can be developed and debugged 'off-line' before the first physical IC product samples become available. This approach relies upon an entirely software-based simulation environment where an emulated test capability interacts with a software model of the new IC device. The concept provides a *concurrent-engineering* approach to the design engineering and the test engineering functions. This concurrent approach can significantly reduce the time to manufacturing. The timely release of an integrated circuit device can decide the market success or failure for a semiconductor product.

Fig. 1*a* shows the traditional IC product development cycle. Here the bulk of the test development work needs to be scheduled into the era following the release of the first product samples. The test capability cannot be finalised prior to the availability of the first physical device samples. More than half of the development time, following the release of the first sample devices, can be spent on the debugging of manufacturing test programs and test circuits. When the first sample IC products arrive the role of the test engineer is to characterise the device so as to determine the actual functionality of the sample device in relation to the specifications listed on the device data sheet. However, such an evaluation cannot be concluded until the test engineer has successfully debugged the untried manufacturing test software and the supporting test hardware. Ideally this critical time, following the arrival of the first product samples, should be spent evaluating the performance of the new device rather than debugging the test environment.

Virtual test allows the simulation of the complete test environment, which includes the simulation of the physical test instruments, test programs, the new DUT (device under test) and the DIB (device interface board). Fig. 1*b* shows the product development process employing the virtual-test approach. In general, IC manufacturing companies believe that between 25% and 75% of the overall test capability development time can be saved using the virtual-test approach. Furthermore, since the cost of producing the first silicon samples is extremely high in terms of time and actual fabrication spend, it is very important that the design of an IC device is correct, first time, so as to avoid further iterations of the silicon design to sample fabrication cycle.

Fig. 2 shows a high-level flow chart for a development process that incorporates virtual test. The chart shows that, following the specification for the new device, the product design development and the development of the test environment are parallel activities.

IC manufacturers are predicting a significant reduction in IC product development times. For example, Motorola is committed to a very significant reduction in development time every five years. The adoption of virtual test is key to the success of such goals. In an attempt to reduce IC product development times various companies are co-operating to define integrated virtual-test approaches. For example, Integrated Measurement Systems has formed a strategic relationship with Teradyne and Motorola to develop a virtual-test capability that Motorola estimates will reduce the IC test development and debug times by up to 80%, which is optimistic and exceeds the general expectations of industry. Motorola claims that this can equate to a total IC development time saving of between 15% and 40% per design.

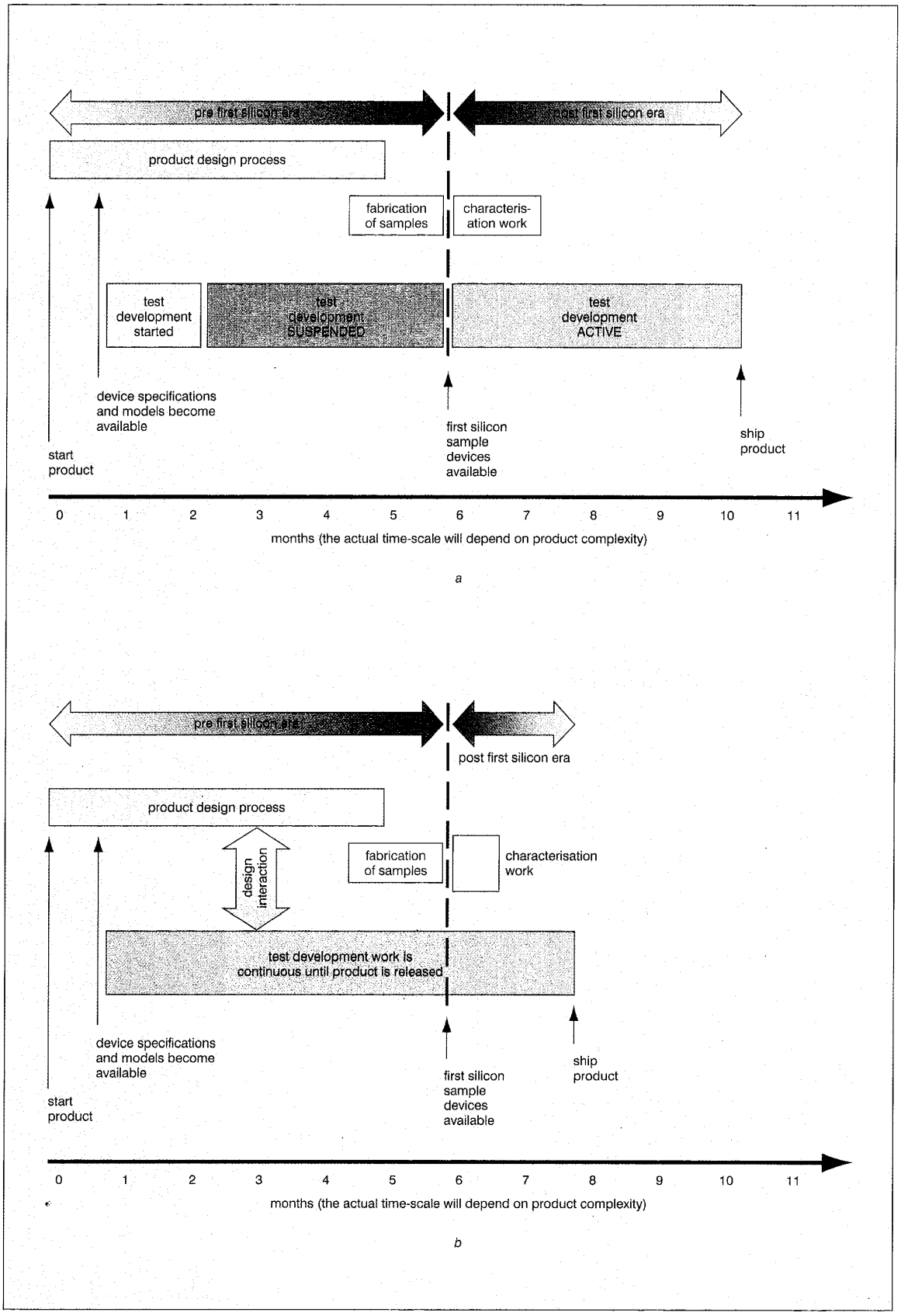


Fig. 1 Product development cycle for IC devices: (*a*) traditional product development cycle; (*b*) virtual test approach

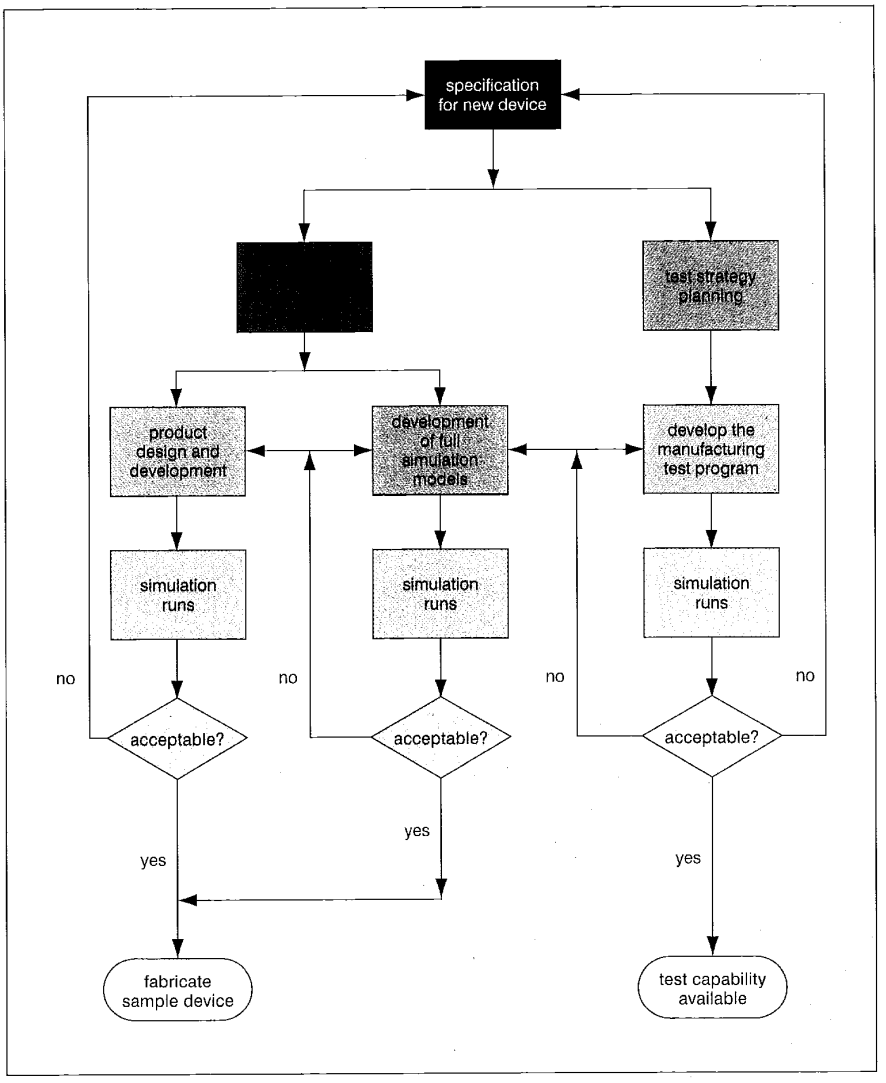


Fig. 2 Flow chart for development process using the virtual-test approach

2 An example virtual-test environment

Analog Devices designs and manufactures integrated circuits based on mixed-signal circuitry. The term 'mixed signal' usually implies that a single integrated circuit contains a complex mix of digital and analogue circuits, usually working at relatively high speeds. Mixed-signal ICs are more difficult to test than pure digital or pure analogue ICs. Analog Devices uses its proprietary ADICE design tool to design and model a new IC product before the first silicon product samples are produced. ADICE is a mixed-signal design simulator that provides a single unified simulation environment that supports simulation of analogue, digital and mixed-signal circuits, using any combination of modelling levels from the system behavioural level down to the detailed transistor level.

A typical IC product device is designed in the ADICE simulation environment and a manufacturing test solution for that product is developed based on Teradyne ATE (automatic test equipment) equipment. Fig. 3 shows the manufacturing test environment for an IC device. The Teradyne ATE tester includes various test instruments, which are programmed via the test program software to provide the various stimulations for the product under test and to evaluate the responses. The Teradyne tester interfaces to the DUT (device under test) via a DIB (device interface board). The DIB is a special interface board designed by the test engineers so as to condition the various stimuli and response signals on the Teradyne interface so as to meet the DUT interface requirements in terms of voltage levels, signal waveforms, timing and latching etc. The test equipment will typically include instruments such as a low-frequency signal generator, a high-frequency arbitrary-waveform generator, a precision multimeter and a signal digitiser. In the virtual-test approach, software models for all such ATE instruments are created in the ADICE design simulation environment, along with the models for the DIB and the DUT. In essence, just as a simulation model for the DUT is developed by the product design engineers, the test engineers develop the DIB board and the actual test instruments as simulation models so that the overall hardware test environment is simulated in software. The concept is simple: instead of just simulating the actual new

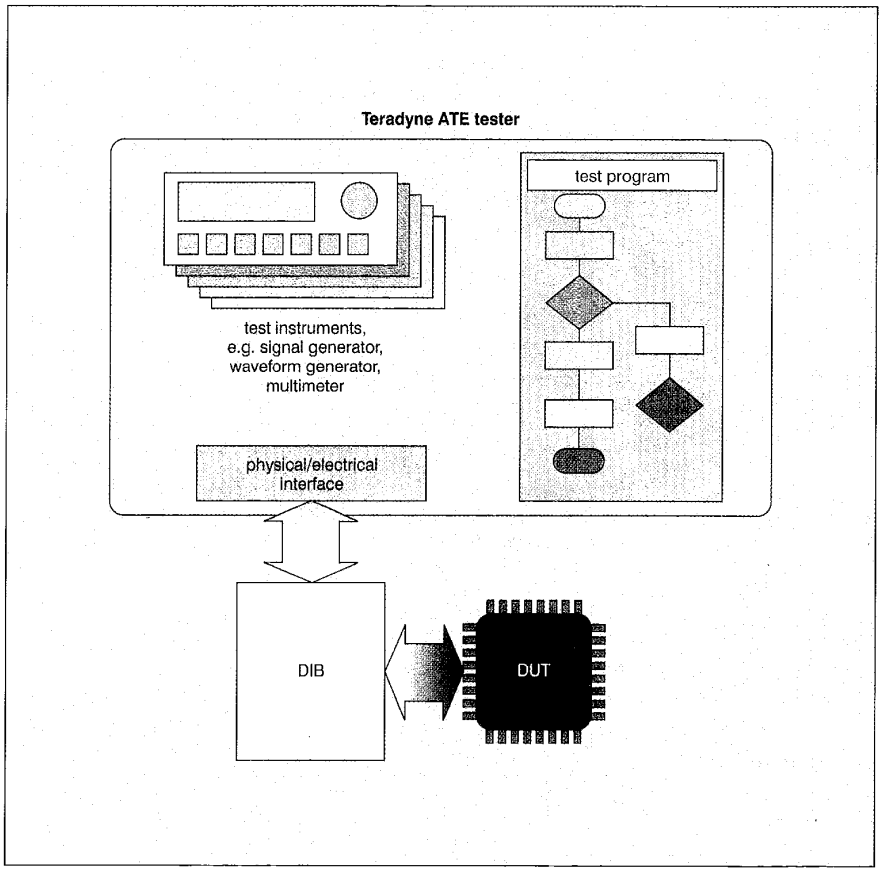


Fig. 3 The physical manufacturing test environment

product device itself the whole test environment is simulated also. The test program can then be developed to interact with this simulated test environment. Hence the interaction of the test program, the test instruments, the DIB and the new product device (the DUT model) can be developed before the first silicon sample products are fabricated. This provides a great opportunity to discover design errors in the new product device even before physical devices are produced.

Analog Devices has successfully developed its own custom virtual-test environment by integrating the Teradyne test environment with its ADICE simulation environment. A number of virtual-test pilot projects have been carried out over the past four or five years and the results of many of these projects have been published[1-3]. These pilot projects used a Teradyne mixed-signal ATE test system running Teradyne's programming environment, known as IMAGE. Teradyne also has an IMAGE ExChange product that supports test simulation for test programs developed in the IMAGE environment. Analog Devices has realised an integrated simulation of the test environment that links the IMAGE test development environment to the ADICE design simulation environment using IMAGE ExChange as the enabling interface. Fig. 4 shows a top-level model of this integrated software environment. The models of the test instruments, the DIB and the DUT exist as ADICE simulation models, while the Teradyne IMAGE environment becomes the test simulator where test programs can be developed, compiled and debugged. The relevant test programs are loaded from within the IMAGE programming environment's control, and the ADICE design simulation models run, all within a single workstation.

The IMAGE ExChange product is the key to the success in this integrated configuration. Using IMAGE ExChange the IMAGE environment sends time-stamped events to the ADICE design simulator to define which ATE resource lines need to be toggled at a given time. Time stamped responses are then evaluated. It is important to note that the design simulator is an event-driven simulator and is used to simulate the tester resources when the control lines are toggled. A global time-base is established for all software components so that the time-stamping activity has a sense of relative time.

In this simulated test environment the state of the entire test system, and all state changes that occur within the system, can be viewed over time. This view is achieved by describing the execution of a test program through the time-stamped events that describe changes to the state of the test system as the test program executes. At a program level, as each statement in the test program is executed, corresponding events are generated that precisely define what is happening within the test program. The time-stamped events can be logged to a file so that execution can be analysed off-line for detailed analysis of the behaviour of the test environment, effectively giving sequenced trace information to assist in

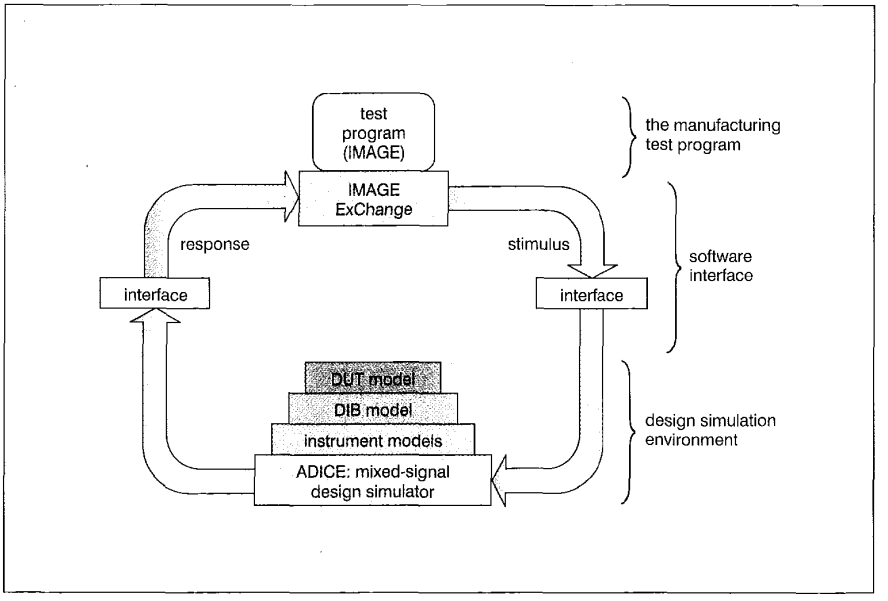


Fig. 4 Model of the integrated test environment. A software-based interactive closed-loop simulation models the actual test system.

the debug of the test capability.

Some example projects

The Analog Devices ADV7185 is a mixed-signal video decoder IC. A virtual-test approach was used in the development of this product and it is claimed[1] that engineers were able to report on the functionality of the part within 1 day of receiving the first silicon product samples. Without the use of the virtual-test approach the product managers would have needed to wait for weeks before getting such a report.

In another virtual-test pilot project Analog Devices adopted the virtual-test approach for the test of a significantly more challenging device, the ADu812MicroConverter™ product. This product is a single IC device that includes a full microcontroller with memory, a 12-bit ADC (analogue-to-digital converter), 12-bit DACs (digital-to-analogue converters) and a host of peripheral interfaces. Results of this pilot project have been published[2,3]. As a direct consequence of using the virtual-test approach, quantifiable benefits were realised, which can be summarised as follows:

- The need for test nodes on the IC were identified by the test process prior to producing the first product samples.
- Design bugs were discovered prior to the first product samples.
- Test program bugs were identified and resolved in the simulation environment.
- The device interface board was fully debugged during the test simulations so that no modifications to the physical DIB were required when the first silicon samples arrived.
- Within two days of receiving the first silicon samples ten major tests were executing correctly.

In a traditional approach it is estimated that it would have taken a few days to resolve problems with the DIB following the arrival of the first silicon samples and it would have taken a further eight weeks of test development time to get the first ten major tests working. The discovery of the various product design and test design bugs, prior to the fabrication of the first samples, saved an unknown amount of time and effort.

Summary conclusions on the Analog Devices experience

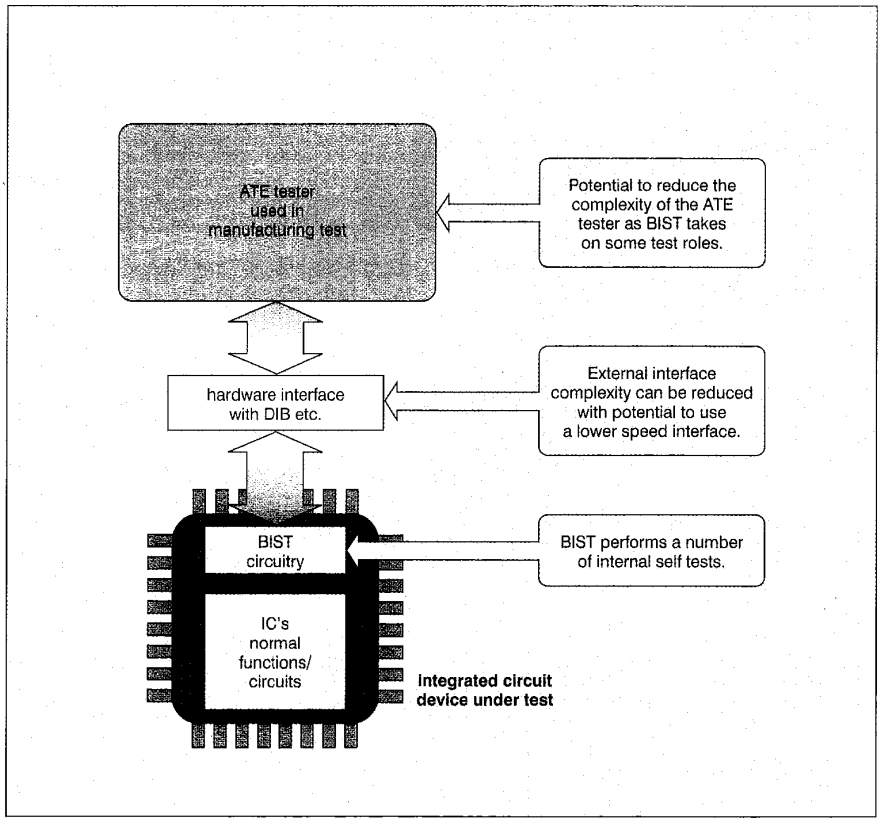
All of the virtual-test trials at Analog Devices to date have shown that the overall product development process can be improved and shortened by adopting a virtual-test approach. The trials were conducted while the virtual-test environment itself was under development. The results to date indicate that the industry expectation of a 25% to 75% reduction in test development time is realistic. However, as different products have different complexities and different test requirements it is difficult to apply any scientific benchmarking to the semiconductor test environment, although some researchers have attempted to do this[4].

3 Some difficulties in implementing virtual test

The move towards a virtual-test model often requires a significant change in the engineering organisation as the test engineering group and the design engineering group need to be closely integrated. In practice the management of the functions across these two groups, as parallel activities, has proven to be difficult as the process needs to maintain very tight version control on the simulation models and very close communication is required between the engineering groups.

Practical difficulties can arise with behavioural simulation results as accuracy often needs to be traded for faster simulation performance. This can result in a particular aspect of the device that is being tested not being reproduced in the behavioural simulation. Further complications can arise in the physical test environment due to conditions of interference and

Fig. 5 Example showing the BIST concept



grounding effects that are not allowed for in the simulations and can cause measurement readings to vary from the expected. It is sometimes recommended that estimated values are calculated and added to the simulation models.

In practice, problems can occur with the software linking of the design simulation and the simulated test environment due to the overhead of the extra circuitry which must coexist with the original DUT behavioural model. As the top-level behavioural model of the DUT is broken down to maximise speed of simulation the additional test circuitry can cause the simulation run times to slow down.

4 Emerging directions for virtual test

Currently the virtual-test concept is placing more emphasis on the test engineering aspects of product development and the model is moving towards the incorporation of DFT (design-for-testability) activity into IC design[5]. DFT is the process where IC product designers consider the engineering requirements for the manufacturing test process at the initial product design stage. DFT can increase the design engineer's productivity by allowing the automatic insertion of test pattern generation circuitry right onto the chip. DFT is now expanding to sophisticated BIST (built-in self test) solutions[6] for on-chip testing. The virtual-test model embraces the DFT and BIST developments very well as the on-chip test circuit models can all be seamlessly included in the simulation runs.

Fig. 5 shows the BIST test concept. BIST can be designed to perform a number of complex tests and report the results to the external interface. As ICs become faster the design of the physical interface to the ATE tester is becoming a problem. The BIST concept can allow high-speed testing to take place right inside the chip. Some industry analysts believe that BIST has the potential to reduce the reliance on expensive ATE equipment in the manufacturing environment. The downside of BIST is that it uses valuable IC real estate; customers are demanding more functionality from a chip at lower costs, so there is a reluctance to give too much space away to test functions. However, many high-speed processor chips are already providing such on-chip test support, not just for manufacturing test, but in the form of debug support for real-time software development[7]. Virtual-test simulations can quite comfortably model BIST circuits in the design environment.

The DFT process will put more emphasis on the concept of virtual design evaluation where rigorous systematic evaluation of the design can be carried out prior to the availability of the first silicon product samples. Many of the concepts for virtual design evaluation will be borrowed from the virtual test world. In the near future tools will emerge to integrate seamlessly virtual-test and virtual-design evaluation activities.

Test tool developers are working towards fully integrated IC design and test environments so that product design can support the test design in a seamless fashion. Teradyne offes the DigitalVX™ Test Simulation software for digital IC design and SpectreVX™ (from

Spectre) for mixed-signal IC design. Cadence Design Systems Inc. offer various IC design tool solutions and work with Synopsys Inc. to integrate the DFT Compiler™ into their tool suite to provide a 'DFT closure' solution for IC designers. DFT closure means the ability to meet all mandated testability requirements in a predictable time. DFT closure can only succeed if test tools are tightly integrated into designers' implementation and verification design flows. There are various other quality design simulation tools on the market which support test simulation work, such as Mentor Graphics ATPG DFT tool suite.

The virtual-test concept provides new opportunities for the training of test engineers. Traditionally much of this training work required the availability of very expensive ATE equipment. Virtual test will allow much of this work to be carried out in a software simulation environment. In fact, as the area of virtual test expands to more complex parts a requirement for a new class of test engineer, a simulation engineer[8], is being defined. The simulation engineer will work with the product design team and the test team, and will have extensive knowledge in the areas of modelling, simulation and test disciplines.

To maximise the benefit of the virtual-test approach more work needs to be done to decrease the simulation run times of the various component models. For complex ICs the simulation run time for the test environment is slow and this needs to be addressed.

If the virtual-test concept is to succeed in the long term it is vital that the developers of IC test equipment and the design tool developers continue to support the concept and work to provide more software tools that can be easily integrated into third party design simulation environments. There is a need for some standardisation in this area

5 Conclusions

The virtual-test concept promises to reduce significantly the development time for IC products by integrating the test engineering activity into the earlier stages of the product development cycle. However, the introduction of virtual test requires some reorganisation in the design engineering activities. Test development and simulation tools still have a long way to go before standardised solutions become available for the easy integration of virtual test. The virtual-test approach will work very well with other emerging test engineering innovations, such as the DFT approach which is moving test circuitry on to the chip. In the very competitive world of semiconductor product development the promised benefits of the virtual-test model will encourage all IC manufacturers to consider the approach.

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References

1 O'DOHERTY, J.: 'A virtual test approach to mixed signal test development'. IEE Colloquium on Systems on a Chip, 1999, IEE Colloquium Digest No. 1999/133, pp.11/1–11/1
2 O'RIORDAN, J. J.: 'Design of a test simulation environment for test program development'. Proc. IEEE Int. Test Conf., 1999, pp.237–244 (ISBN 0-7803-5737-1)
3 O'RIORDAN, J. J.: 'Design, implementation and use of a virtual test environment for test program development'. Masters degree thesis, 1998, University of Limerick, Ireland, pp.158–164
4 KAPUR, R., HAY, C., and WILLIAMS, T. W.: 'The mutating metric for benchmarking test', *IEEE Des. Test Comput.*, July/September 2000, **17**, (3), pp.18–21
5 DEARBORN, W. H., and PERKINS, E. G.: 'The virtual test program'. Proc. IEEE Systems Readiness Technology Conf., 1998, pp.149–159 (ISBN 0-7803-4420-0)
6 RUNYOU, R.: 'Testing big chips becomes an internal affair', *IEEE Spectrum*, April 1999, pp.49–55
7 MACNAMEE, C., and HEFFERNAN, D.: 'Emerging on chip debugging techniques for real-time embedded systems', *Comput. Control Eng. J.*, December 2000, **11**, (6), pp.295–303
8 FORCE, C., and AUSTIN, T.: 'Testing the design: the evolution of test simulation'. Proc. IEEE Int. Test Conf., 1998, pp.612–621 (ISBN 0-7803-5093-6)

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