SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors

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***Abstract*—Switching devices based on wide bandgap materials such as silicon carbide (SiC) offer a significant performance improvement on the switch level (specific on resistance, etc.) compared with Si devices. Well-known examples are SiC diodes employed, for example, in inverter drives with high switching frequencies. In this paper, the impact on the system-level performance, i.e., efficiency, power density, etc., of industrial inverter drives and of dc–dc converter resulting from the new SiC devices is evaluated based on analytical optimization procedures and prototype systems. There, normally on JFETs by SiCED and normally off JFETs by SemiSouth are considered.**

***Index Terms*—AC–DC power converters, DC–DC power converters, SiC power semiconductor switches.**

I. Introduction

THE continuous development of improved power semiconductors is a key enabling factor for propelling the constantly increasing demand for higher power density (P/V) and higher efficiency (η) in many power-electronic applications. Recently, the technological progress in manufacturing power devices based on wide bandgap materials, for example, silicon carbide (SiC) or gallium nitride (GaN), has resulted in a significant improvement of the operating-voltage range for unipolar devices and of the switching speed and/or specific on resistance compared with silicon power devices. In [1], the current status of SiC switching devices with respect to specific on resistance, maximal blocking voltage, specific capacitance, etc., is summarized. In Table I, some basic information about the SiC devices is given.

With these new devices, a question arises as to what increase in the system-level performance can be achieved by the improvements obtained at device level. Such performance indicators include power density and efficiency of the power-electronic converter. In [1], this influence has been investigated for single-phase power-factor correction (PFC) systems. Moreover, the demand on the system level has been transferred to a desired profile for the semiconductors, which is compared with the performance offered by the new SiC devices.

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TABLE I
CURRENT STATUS OF RELATIVELY MATURE SiC SWITCHES. SINCE THE ALLOWED DRAIN CURRENT I_D DEPENDS SIGNIFICANTLY ON THE COOLING CONDITIONS, THE VALUES SHOULD JUST GIVE A HINT ON THE CAPABILITIES OF THE RESPECTIVE SWITCH FOR OPERATION AT HIGHER JUNCTION TEMPERATURES (125 °C OR HIGHER). THE (SPECIFIC) ON RESISTANCE IS GIVEN FOR 25 °C. THE Si IGBT AND THE Si DIODE ARE PART OF THE FP15R12W1T4 MODULE BY INFINEON

	$V_{(\mathrm{BR})\mathrm{DSS}}$	I_D	$R_{\mathrm{DS(on)}}$	A_{Chip}
JFET (SiCED)	500V	∼5A	0.2Ω	5.76mm^2
JFET (SiCED)	1.2kV	∼5A	0.33Ω	5.76mm^2
JFET (SiCED)	1.2kV	∼17A	0.12Ω	17.3mm^2
JFET (SiCED)	6.5kV	∼5A	3.3Ω	5.76mm^2
JFET (SemiSouth)	1.2kV	>15A	0.125Ω	4mm^2
MOSFET (Cree)	1.2kV	>20A	0.075Ω	16.6mm^2
MOSFET (Cree)	10kV	∼10A	0.5Ω	65.8mm^2
	Si Reference Devices			
IPP60R099CP	650V	31A	0.09Ω	28mm^2
STY112N65M5	650V	59A	0.019Ω	≈71mm^2
	$V_{(\mathrm{BR})\mathrm{DSS}}$	I_N	V_F	
Si IGBT +	1.2kV	15A	0.8V	17.5mm^2
Si Diode	1.2kV	15A	0.9V	10.7mm^2
Si IGBT +	1.2kV	15A	0.8V	17.5mm^2
C2D10120 (SiC)	1.2kV	22A	0.8V	9.8mm^2

In the area of low-voltage motor drives, numerous papers about the comparison of Si insulated-gate bipolar transistor (IGBT) and SiC switching devices—mainly SiC JFETs–have been published. Here, usually, the Si devices in matrix converters [2], [3] or standard inverters [4], [5] are replaced by SiC devices, and the change in the system performance is evaluated. Depending on the operating point and the switching frequency [3], the SiC devices facilitate a significant performance improvement—particularly regarding the switching loss. This is due to the lack of diode reverse recovery and IGBT tail current which are observed in Si devices. The conduction loss of the SiC devices depends on the chip area since the applied devices are all unipolar ones. Consequently, the efficiency comparison is also dependent on the considered chip areas.

The lower switching loss of the SiC devices and the related freedom of being able to increase the switching frequency does not influence the achievable power density of standard voltage-source inverter except for the cooling system, which could be reduced when the losses are lower. However, the higher possible

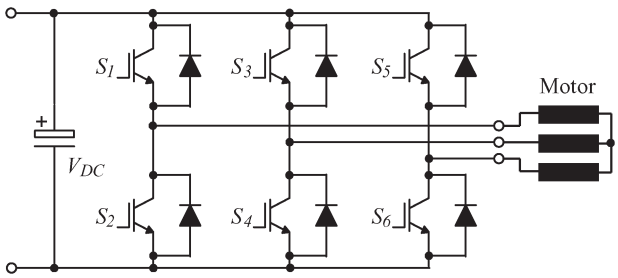


Fig. 1. Schematic of a two-level inverter for low-voltage standard motor drives.

switching frequencies at low switching loss are advantageous for dc–dc converter systems since they allow reducing the size of the inductor and/or transformer [6]. This is particularly true at medium-voltage levels [7], [8] where fast switching devices based on silicon are nonexistent and where new and ultraefficient converter systems are required for future energy-distribution networks [9].

Because in the literature, usually, only a pure replacement of the switching devices by SiC ones and no optimization/adoption of the operating points to the new devices has been presented, in Section II, first, the influence of the SiC devices on industrial inverter drives is investigated. Here, the link between the demands on the system level and the resulting required profile of the switching elements is also discussed. Thereafter, dc–dc converter systems are considered in Section III, where medium voltage dc–dc converters for future energy-distribution systems are also included. Here, the new switching devices based on wide bandgap materials offer a tremendous performance improvement compared with the state-of-the-art Si technology. In all considerations, a limitation of the junction temperature below 175 °C and the data of the SiC switches presented in Table I is assumed. Furthermore, the comparison is always based on the chip area and not on the current rating of the devices provided in the datasheets of the manufacturers as the chip area is proportional to the costs, and the current ratings are very much dependent on the application, the switching frequency, and the cooling conditions.

II. Inverter

Low-voltage (< 1000 V) industrial drives are an important power-semiconductor application area. Here, mainly two-level inverters operating at switching frequencies in the range of 4 to 16 kHz and at a dc-link voltage in the range of 600 V are used (cf., Fig. 1). In niche applications, matrix converters offering bidirectional power flow and three-level converters for higher operating frequencies can also be found.

Due to the high winding inductance of the motors, there is generally no need for higher operating frequencies, as shown in Fig. 2(a), except for special high-speed applications, where the fundamental frequency is significantly higher than 50 Hz, and the inductance values usually decrease. Also, there is no special need for higher kilowatts per kilogram and/or extreme power densities in most applications. Only, in integrated motor drives, a higher power density would be desirable, but in this application, with an improved cooling system, the requirements

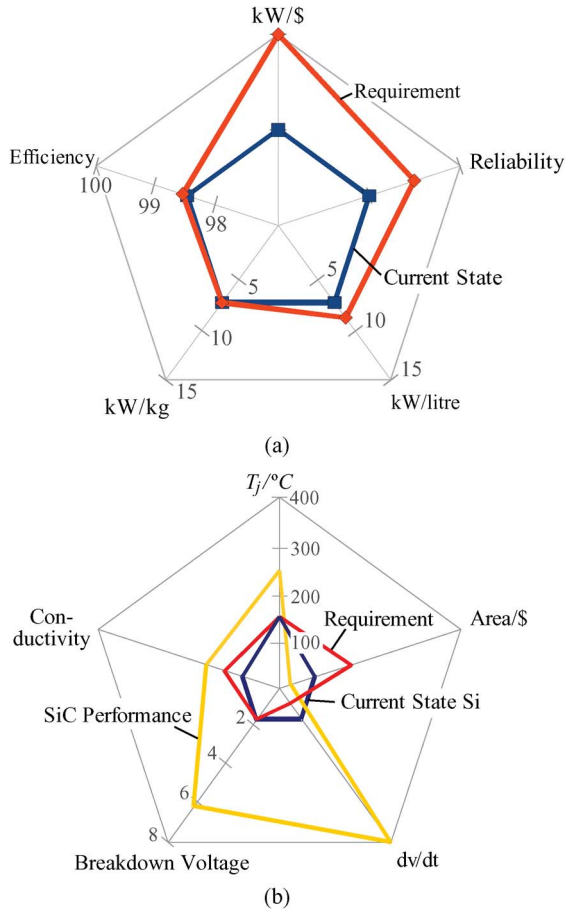


Fig. 2. (a) Radar chart of the system requirements for low-voltage industrial drives where the current status is shown in blue ($= 100\%$), and the desired values are shown in red. Based on the system requirements, the radar chart in (b) for the switching devices is derived, where the current status with silicon devices ($= 100\%$) is shown in blue, the requirements on the switch level are shown in yellow, and the offered performance of SiC devices is shown in red. The numbers are based on the prototype system presented in [10]. (a) System level requirements. (b) Component level requirements and performance.

often can be met. Since the efficiency of the standard inverters is already quite high and substantially exceeds the efficiency of the motor, there is (generally speaking) no further requirement for increased efficiency in comparison with silicon-based converters.

A major driving force is the cost, where a significant reduction could result in a more widespread application of inverter drives. In some areas, a higher reliability is also required, which, however, is difficult to meet with high-temperature operation/devices.

The system requirements are translated to the switch level in Fig. 2(b), where the current status for silicon devices is shown as reference level ($= 100\%$) in blue, the resulting requirements are shown in yellow, and the performance achievable with SiC devices is shown in red. Here, it could be seen that the achievable switching speed of SiC and even of Si devices is not required. Often, even the Si IGBTs are slowed down in order not to damage the motor-winding isolation/bearings with high dv/dt values and to reduce electromagnetic interference (EMI). Also, the high breakdown voltages and the high possible junction temperature of SiC are not required in low-voltage

TABLE II
SPECIFICATIONS OF THE INVERTER SYSTEM

Nominal Power	7.5kW
DC Link Voltage	700V
Switching Frequency	4kHz
Current Phase Displacement	30°
Modulation Index	0.9
Output Voltage	$364V_p$
Output Current	$15.9A_p$
CSPI	15W/(K dm^3)
Ambient Temperature	25°C
Junction Temperature	175°C
Thermal Resistance R_{j-HS}	30K/(W mm^2)

drives. Only the better conductivity of SiC, resulting in a smaller chip area, and the higher achievable efficiency could be beneficial for inverter systems, in case the costs do not increase. Here, the high costs for SiC devices are a significant limit at the moment.

After the more general remarks, the effect of SiC devices on a real prototype system with the specification given in Table II are discussed. Here, the following scenarios are considered.

1) How much chip area is required for achieving an efficiency of 98.3%?
2) How much chip area is required for keeping the power density constant at 25 kW/dm^3 (considering just the cooling system)?
3) How much chip area is required for an ultraefficient drive with an efficiency of 99.3%, i.e., 1% more than the prototype system?

In addition to the silicon IGBTs with Si-/SiC diodes, the 1.2-kV JFETs and MOSFETs as listed in Table I are also considered.

In Fig. 3, the results of the mentioned scenarios are shown. The results are based on some simplifying assumptions. First, it has to be noticed that only pure silicon performance has been analyzed, so additional losses of fans or digital control electronics will not be considered. The conduction loss is modeled with a typical simplified device behavior, namely

$$P_{\mathrm{Cond,IGBT}}(I) = V_{f,T} \cdot I + R_{\mathrm{on},T} \cdot I^2 \quad (1)$$

$$P_{\mathrm{Cond,Diode}}(I) = V_{f,D} \cdot I + R_{\mathrm{on},D} \cdot I^2 \quad (2)$$

$$P_{\mathrm{Cond,JFET}}(I) = R_{DS(\mathrm{on}),J} \cdot I^2 \quad (3)$$

$$P_{\mathrm{Cond,MOSFET}}(I) = R_{DS(\mathrm{on}),M} \cdot I^2. \quad (4)$$

The parameters are dependent on the junction temperature. For the bidirectional JFET and MOSFET devices, the loss characteristic in the forward and reverse current directions is assumed to be the same. With a low switching frequency of 4 kHz, the switching losses of JFET and MOSFET are much lower than the conduction losses and will be neglected. The switching losses of the IGBT and diode are modeled with the switching energies linearly scaled [11]

$$E_{\mathrm{On},T}(V,I) = E_{\mathrm{On}T,\mathrm{nom}} \cdot \frac{V}{V_{\mathrm{nom}}} \cdot \frac{I}{I_{\mathrm{nom}}} \quad (5)$$

$$E_{\mathrm{Off},T}(V,I) = E_{\mathrm{Off}T,\mathrm{nom}} \cdot \frac{V}{V_{\mathrm{nom}}} \cdot \frac{I}{I_{\mathrm{nom}}} \quad (6)$$

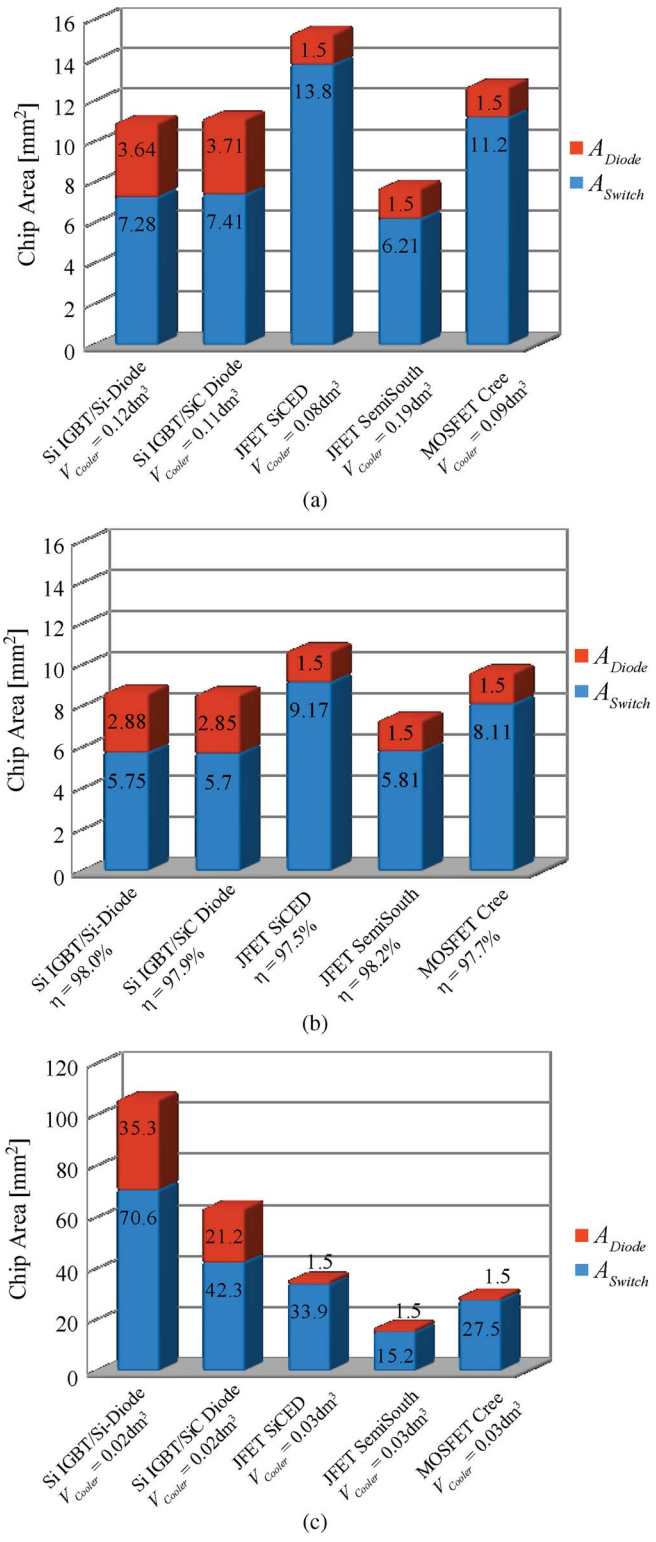


Fig. 3. Chip area of the 1.2-kV SiCED JFET, the 1.2-kV SemiSouth JFET, the 1.2-kV Cree MOSFET, and a Si IGBT with Si and with SiC diode for three different cases: (a) All systems have an efficiency of 98.3%, (b) all systems have a volume of 0.3 dm^3, and (c) the chip area required for an efficiency increase of 1%, i.e., for 99.3%.

$$E_{\mathrm{On},D}(V,I) = 0 \quad (7)$$

$$E_{\mathrm{Off},D}(V,I) = E_{\mathrm{Off}D,\mathrm{nom}} \cdot \frac{V}{V_{\mathrm{nom}}} \cdot \frac{I}{I_{\mathrm{nom}}}. \quad (8)$$

The nominal values are taken from datasheet values of the latest generation IGBT from Infineon (1.2 kV, 15 A) with parameters as listed in Table I. For the implementation variant with SiC antiparallel diodes, the diode turn-off energy is assumed to be zero, and the IGBT turn-on energy is assumed to be 30% smaller due to the missing diode reverse-recovery effect.

The device losses of the inverter system are calculated analytically for a symmetric space-vector modulation strategy. The well-known results for the average conduction and switching losses will not be repeated here but could be found in [11] and [12]. In a further step, the on resistances of all devices are made area dependent (cf., [13]) with the generic formula

$$R_{\mathrm{On}} = R_{\mathrm{On,nom}} \cdot \frac{A_{\mathrm{Chip,nom}}}{A_{\mathrm{Chip}}}. \tag{9}$$

For the dependence of the switching energies on the die size, no general trend could be observed. They are assumed to stay constant for the considered chip-area range.

In a same way, the thermal resistance $R_{\mathrm{th},J-S}$ for each device is made area dependent. The nominal value of the resistance of 30 $\mathrm{K}/(\mathrm{W}\cdot\mathrm{mm}^2)$ was fitted with a datasheet study in [13] and is used for all dies independent of technology

$$R_{\mathrm{th},J-S} = \frac{R_{\mathrm{th},J-S,\mathrm{Anom}}}{A_{\mathrm{Chip}}}. \tag{10}$$

Finally, a forced-air cooling system with a cooling-system performance index (CSPI) of 15 $\mathrm{W}/(\mathrm{K}\cdot\mathrm{dm}^3)$ is assumed. This allows for complete inclusion of the thermal model into the optimization process

$$R_{\mathrm{th},S-A} = \frac{1}{\mathrm{CSPI}\cdot \mathrm{Vol}_{\mathrm{HS}}}. \tag{11}$$

The heat-sink temperature can be calculated with the total losses of the inverter system

$$T_{\mathrm{HS}} = T_{\mathrm{Amb}} + P_{\mathrm{Total}} \cdot R_{\mathrm{th},S-A}. \tag{12}$$

The junction temperature of each chip die is given by

$$T_{J,\mathrm{Die}} = T_{\mathrm{HS}} + P_{\mathrm{AVG,Die}} \cdot R_{\mathrm{th},J-S}. \tag{13}$$

Now, the set of equations can be solved for the different scenarios defined previously. For each scenario, the junction temperature is assumed to be 175 °C. This implies that the fundamental output frequency is high so that average device losses can be used, and no time behavior of the thermal model has to be considered.

For a fixed efficiency, the formulas directly lead to the chip areas and size of the necessary heat sink. For the IGBT with antiparallel diodes, the chip size of the diode is assumed to be half of the IGBT chip size in order to reduce by a degree of freedom.

Due to the reverse-recovery losses of the internal diodes of the SiC JFETs and the SiC MOSFETs, antiparallel Schottky diodes are assumed, which only conduct shortly during the interlocking delay. For the rest of the time, the current is flowing in reverse direction through the channel of the unipolar device. Consequently, the area of the SiC diodes could be relatively small and is assumed to be 50% of the SiC diode area of the IGBT+SiC diode combination.

It is interesting to note that for a constant ambient temperature (e.g., 25 °C), the equations define a minimum efficiency for which a cooling solution exists. If the efficiency is chosen to be lower than this minimum, the resulting chip dies are so small that the temperature drop from the junction to the sink gets higher than the maximal 150 °C, and the heat-sink size grows to infinity.

For a fixed heat-sink size, the formulas directly lead to the necessary chip sizes and the resulting inverter efficiency. Finally, the increase in area for a high-performance 99.3% inverter efficiency (pure silicon) is calculated. It can be noted that the chip area of IGBT and diode has to be increased to unrealistic values, showing the advantages of SiC JFETs and MOSFETs for ultrahigh efficiency motor drives.

The higher efficiency achievable with SiC devices is, for example, very interesting for renewable energy conversion (photovoltaic inverter) where a special focus is put on efficiency. There, the higher costs of the SiC devices could be compensated by saved energy. In general, however, it is not important if the losses are saved at the generator or at the consumer side—except for the losses due to energy transmission/distribution.

In automotive industry, in addition to efficiency, a higher possible operating temperature is also advantageous due to high ambient temperatures if the power-electronic converter is mounted close to a combustion engine. There, the remaining components, e.g., capacitors, control electronics, or gate drives, are the limiting factors in addition to reliability issues. Furthermore, with a water cooler, a smaller footprint of the SiC devices would also be advantageous with respect to costs.

Higher possible junction temperatures could also improve the robustness of the converter systems in case of overload situations. Replacing the Si bipolar devices with fast SiC unipolar switches also requires considering the parasitics in the layout and the mechanical design more carefully due to fast switching transients.

III. DC–DC Converter

The second application area considered in this paper is the dc–dc converter, which is split as low-voltage converter—nonisolated and isolated—and high-voltage isolated dc–dc converter, which will be discussed next. However, the general requirements for low voltage dc–dc converter in telecommunication and in automotive applications are evaluated based on the net diagrams shown in Fig. 4.

The most important issue on the system level is cost since, in both areas, there is quite a high cost pressure and a very competitive market. In the automotive area, the weight of the converter and the power density are also important criteria since the first directly influences the fuel efficiency, and the second results from the limited available space. The latter is also true for telecommunication systems, as the costs of floor space are high. Also, for both application areas, the efficiency has become more and more important in the last years due to rising energy costs and environmental concerns, which is particularly true for

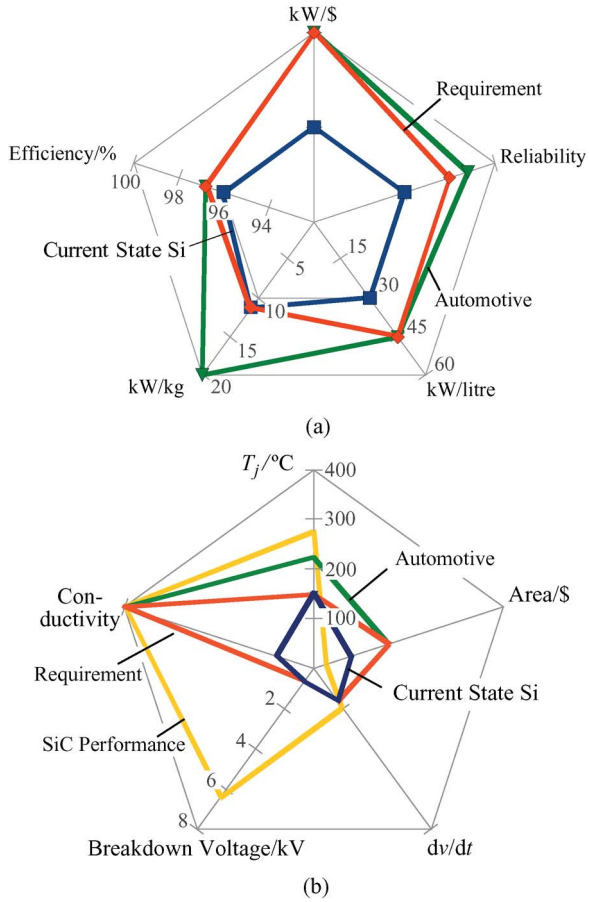


Fig. 4. Radar charts of the system and component level requirements for nonisolated dc–dc converter. Here, the numbers show typical values for the system shown in Fig. 7. (a) System level requirements. (b) Component level requirements and performance.

renewable energies and energy storage [14]. In particular, in the automotive area, with its harsh environmental conditions (e.g., vibrations, temperature), the reliability should be very high, which is difficult particularly if one thinks of high-temperature operation. Reliability is also an important issue in telecommunication supplies as shutdown of a data center is very expensive.

These system-level criteria result in the requirements for the switches, as shown in Fig. 4(b), where the current status is shown as reference value $(= 100\%)$ and where the achievable performance of SiC devices and the demands on switches in the automotive and the telecommunication area are also given. There, mainly, the higher conductivity per area of SiC devices and the higher junction temperature for automotive applications meet the demands. Higher blocking-voltage capability and improved switching performance are not required since the operating voltages are usually limited to a few hundred volts and soft switching could be achieved with very small additional effort. As with the other applications, the higher costs of SiC devices are a major drawback, and this significantly limits the area of the SiC devices which could be used at the same cost level, which influences the achievable system performance—particularly, efficiency. The two low-voltage systems considered now support this statement.

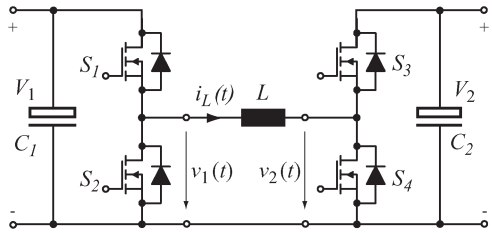


Fig. 5. Bidirectional buck–boost converter with specifications given in Table III for automotive applications.

TABLE III
SPECIFICATIONS OF THE AUTOMOTIVE DC–DC CONVERTER SHOWN IN FIG. 7

Parameter	Value
Voltage Range V_1	150V...450V
Voltage Range V_2	150V...450V
Output Power	-12kW...12kW
Switching Frequency	100kHz
Maximum Current I_{max}=I_1=I_2	40A
Required Efficiency η_{req}	$\geq$95% for P>0.1P_{max}
Ripple Amplitude $\hat{\tilde{v}}_1$	1V
Ripple Amplitude $\hat{\tilde{v}}_2$	1V

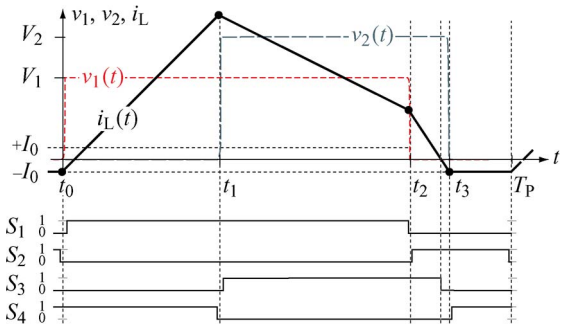


Fig. 6. Waveforms of the primary and secondary voltage and the inductor current.

A. Low-Voltage Converter

1) Nonisolated Automotive DC–DC Converter: First, a dc–dc converter without galvanic isolation is considered. A typical application area of such a converter is hybrid electrical vehicles or fuel-cell vehicles, where the converter is used for power management between the batteries, supercapacitors, and/or fuel cells [15], [16]. In these systems, a bidirectional power flow for providing energy during acceleration and storing energy during braking is often required.

A converter for this application has to meet the prevalent automotive requirements, such as being a low-cost design, and minimize the component size and count. This can be achieved by increased switching frequency and interleaved operation of multiple converter phases. Fixed-frequency operation is desired due to EMI restrictions, and a highly compact design and a low overall weight are required.

In Fig. 5, a schematic of the considered bidirectional dc–dc converter consisting of four switches, an inductor, and two capacitors is shown. The specifications of the converter are

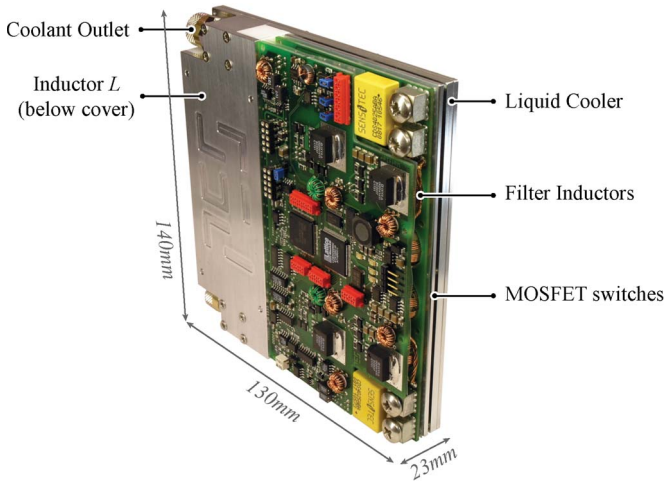


Fig. 7. Photograph of the bidirectional buck–boost converter with 150 . . . 450-V input and output voltages, 12-kW nominal power, and a switching frequency of 100 kHz.

listed in Table III, and the most important waveforms of the converter are shown in Fig. 6. There, the primary voltage v_1 and the secondary voltage v_2 as well as the inductor current i_L and the gate signals S_ν are given, and it could be seen that, in contrast to a normal buck–boost converter, a negative current flows in the inductor between t_3 and T_P. With this special modulation method, a soft switching of the converter could simply be achieved by control, and the efficiency could be increased. Further details about the control method are given in [17], and in [18], a similar structure is presented where the chip area is reduced by using snubbers, which however increase the circuit complexity and costs for the passive components.

A picture of the Si reference prototype system is shown in Fig. 7. This has been used to validate the analytical converter models presented in [19], which are used in the following to compare the achievable performance of Si and SiC devices. The reference system is based on IXYS IXFB82N60P devices where four MOSFETs are used in parallel for switch S_1/S_3 and three MOSFETs are used in parallel for switch S_2/S_4, in order to achieve the required efficiency of $\geq$ 95% in the complete input and output voltage range. For S_1/S_3, more MOSFETs are used since the rms currents for these switches are higher and, thus, the converter efficiency also benefits from an unbalanced distribution of the chip area. The prototype system utilizes a water cooler and can operate with a coolant temperature of up to 80 °C. Furthermore, six 12-kW units are interleaved for reducing the ripple current at the input/output.

For comparison of the performance of the Si devices with the SiC ones, it is assumed that the IXFB82N60P are replaced by the more recent STY112N65M5 from STMicroelectronics, which have a much lower specific on resistance.

In the upper half of Fig. 8, the resulting chip area for the four switches is shown. In the lower half, the mean efficiency as well as the power density for the different considered soft and hard switching systems is also shown. For the efficiency, the conduction loss of the switches, the core, and the HF winding losses of the inductor and the power required for the control are considered. Power for the water pump is neglected.

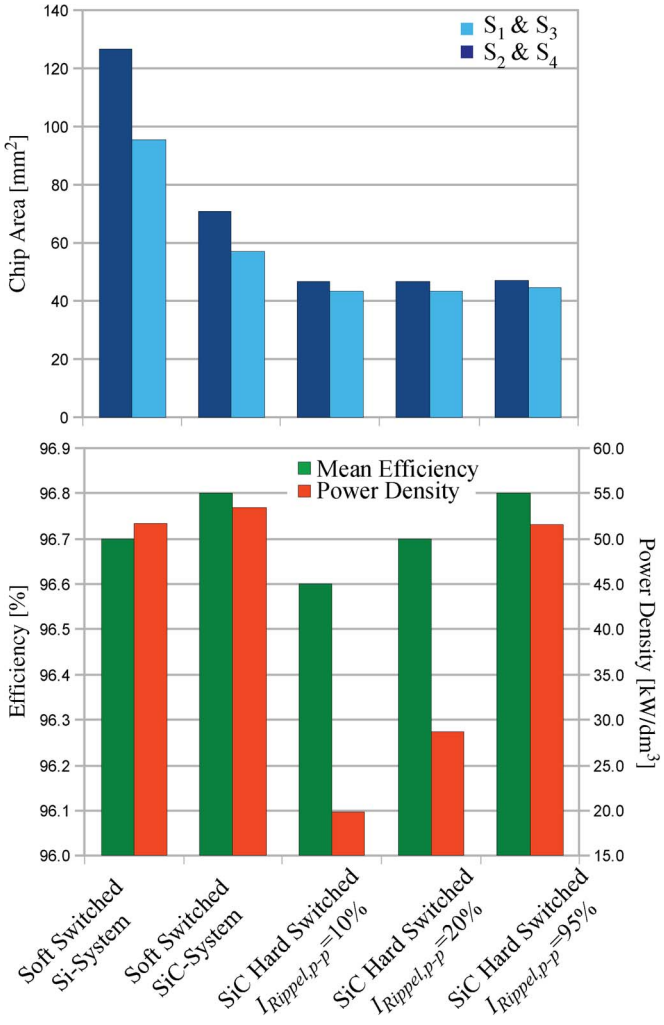


Fig. 8. Calculation results for a nonisolated dc–dc converter with Si MOSFET and/or SiC JFET scaled on the basis of the 500-V JFET by SiCED. For the SiC devices, soft-switching conditions as well as hard switching are considered. In case of hard switching, different limits for the peak-to-peak ripple current in the inductor are assumed. In all considered systems, the minimal efficiency in the whole operating range is higher than 95%; the mean efficiency usually is significantly higher. In the upper half, the required chip areas of the four switches is shown, and in the lower graph, the efficiency and the theoretical power density are shown.

Also, the volume of the water pump is not considered in the power density. Instead, it is assumed that a 25% volume must be added to account for the interconnections, isolation, and the geometrically not matching housings. The depicted prototype shows a reduced power density in comparison with the results provided in this paper mainly because of the larger volume required by the IXYS IXFB82N60P MOSFETs and the inductor made of planar cores. The analytical calculations assume an optimized inductor built with E-cores that result in a reduced volume. Additionally, the prototype is equipped with measurement circuitry, such as current sensors, that would only be required once in a multiphase converter design.

By utilizing 500-V SiCED JFETs and adapting the chip area so that the SiC system also has a minimal efficiency of 95% in the whole operating range, the performance shown in the second column of Fig. 8 is achieved. Due to the lower specific on resistance and the resulting limitation of the minimal chip area

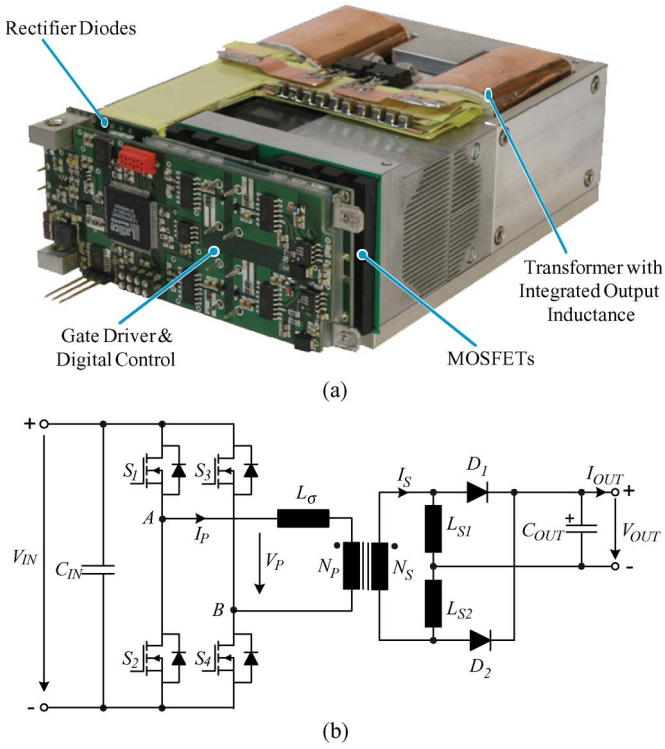


Fig. 9. Phase-shift dc–dc converter with current doubler output. (a) 5-kW prototype of the proposed 400 V/48 ... 54 V dc–dc converter: Height: 1 U, volume: 0.56 dm^3, power density: 147 W/in^3 (9 kW/dm^3). (b) Circuit schematic of the phase-shift full-bridge converter with current-doubler rectifier.

by thermal constraints, the mean efficiency of the SiC system is slightly higher. Also, the power density increases slightly due to the reduced volume required for the semiconductors.

In the third, fourth, and fifth column, the results for operation under hard-switching conditions with 500-V SiCED JFETs are shown. Here, different limits for the peak-to-peak ripple currents have been assumed, which results in a smaller inductance value if the ripple is larger. This also increases the power density of the system. In case of a 95% ripple, i.e., almost discontinuous operation, the power density becomes maximal. Here, the value and the volume of the boost inductor is larger as in the case of the soft-switched systems, but the volume reduction due to much smaller required chip area (i.e., also smaller cooling system) outweighs this. A relatively low dependence of the chip area on the ripple current in the case of the hard-switched system results since the rms current does not depend so much on the current ripple but on the dc component of the current. Furthermore, the efficiency is slightly higher than the desired 95% since the chip area is limited by thermal constraints so that the R_{DSon} is smaller than necessary.

In the case of soft-switching conditions, with SiC, the chip area could be reduced to approximately 60% of the Si chip area.

In the calculations performed for evaluating the performance of the different devices, for the inductor, an E-core with air gap made of N87 material, a maximal flux density of $B_{\max} = 0.3$ T, and a maximal temperature of $T_L = 100$ °C has been assumed. For the winding, litz wire is used, and the current density is limited to 5 A/mm^2. Further details on the inductor optimization can be found in [19].

TABLE IV
SPECIFICATIONS FOR THE PROPOSED IT DC–DC CONVERTER

Input Voltage	400 V
Output Voltage	48... 54 V
Output Power	5 kW
Output Ripple Voltage	300 mV$_{pp}$
Max. Ambient Temperature	45 °C
Max. Height	1 U ($\approx$ 44 mm)
Power Density	9kW/dm^3

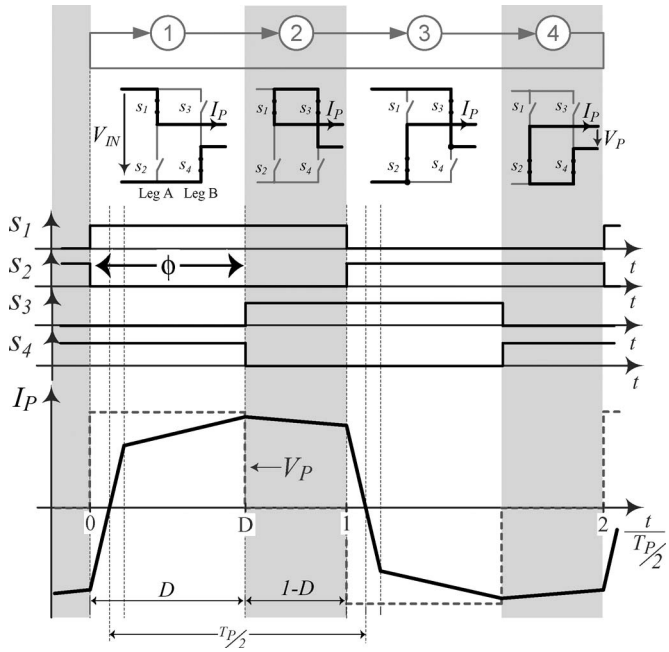
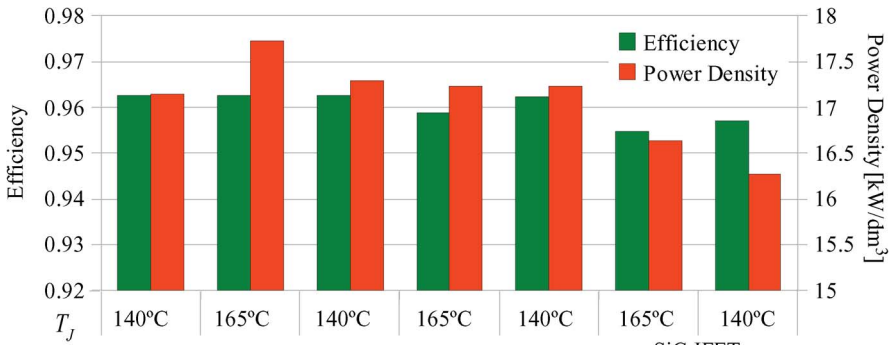


Fig. 10. Waveforms of the primary current and voltage of the current-doubler rectifier at nominal power operating with phase-shift modulation.

2) Isolated DC–DC Converter: A large market for isolated dc–dc converter in the kilowatt range is the telecommunication power supply, where often, full-bridge converters with soft switching or some kind of resonant converters are applied. These converter types meet the demands for high-power density and high efficiency—an issue which became more and more important due to rising energy costs. However, since initial costs are very important, usually relatively simple and robust designs are applied.

In Fig. 9, the circuit schematic and a photograph of a full-bridge converter with current doubler, which fulfills these requirements, are shown, and in Table IV, the specifications of the converter are given. The design of the converter is based on an optimization algorithm, which also includes the thermal and the electromagnetic design of the converter besides the electrical model. Further details on the design and the optimization procedure can be found in [20] and on the thermal design in [21]. The converter has been built for validating the models and is based on 500-V MOSFETs APT50M72B2 from Microsemi.

In Fig. 10, the basic waveforms for the primary current and the primary voltage are given. Due to the leakage inductance L_σ of the transformer and the phase-shift modulation, all four switches operate under zero-voltage-switching (ZVS) condition, resulting in negligible switching loss at a very low



T_J	140ºC	165ºC	140ºC	165ºC	140ºC	165ºC	140ºC
	Silicon MOSFET	SiC JFET Same η		SiC JFET Same P/V		SiC JFET $A_{SiC} = 1/5\, A_{Si}$	
$T_{HS,SW}$	129ºC	160ºC	135ºC	158ºC	135ºC	154ºC	130ºC
$T_{HS,Dio}$	125ºC	125ºC	125ºC	125ºC	125ºC	125ºC	125ºC
A_{Chip}	123mm^2	66mm^2	53mm^2	37mm^2	50mm^2	27mm^2	27mm^2
A_{SiC}/A_{Si}	-	54%	43%	30%	41%	20%	20%

Fig. 11. Efficiency and power density for the isolated dc–dc converter with Si MOSFETs (STY112N65M5) and/or the 500-V JFETs for the cases where the SiC chip area is scaled so that the converters have the same efficiency η or the same power density P/V and for the case where the chip area of the SiC devices is 1/5 ($A_{\mathrm{SiC}} = 1/5 A_{\mathrm{Si}}$). For the SiC devices, a 140 °C and a 165 °C limit for the junction temperature and separate heat sinks for the Si rectifier diodes and the switches of the full-bridge have been assumed. Below the graph, the temperature $T_{\mathrm{HS,SW}}$ of the heat sink for the switch and $T_{\mathrm{HS,Dio}}$ for the heat sink of the rectifier diodes are shown. The switching losses, which are relatively low, are evaluated based on measurements with the Si MOSFET and are assumed to be in the same range for the SiC devices.

effort on the circuit and control side. Consequently, only the conduction loss and therewith the on resistance of the switches is interesting. For achieving ZVS conditions and zero switching loss, the switches require a minimum output capacitance, which depends on the switching speed. With a smaller capacitance value, the switching loss increase, but it can also help to increase part of the load efficiency.

In spite of the negligible switching losses, the optimal switching frequency of the converter which results in maximal power density is just 200 kHz. Increasing the frequency will result in a smaller power density and efficiency as explained in [22]. There, it is also shown that for achieving a maximal efficiency of the considered converter systems, the switching frequency must be lower than the mentioned 200 kHz.

Based on the optimization procedure, the full-bridge converter has been optimized with the data of the 650-V MOSFET STY112N65M5 from ST on the silicon side and of the 500-V normally on JFET from SiCED on the SiC side. Here, the following assumptions have been made:

1) core material: N87 from EPCOS ($T_{\max} \leq 115$ °C);
2) windings: Foil windings ($T_{\max} \leq 125$ °C);
3) center-tapped secondary winding;
4) rectifier diode: APT100S20 from Microsemi;
5) CSPI: 23 (for transformer and semiconductor heat sink);
6) maximum junction temperature $T_{j,\max} \leq 140$ °C for Si MOSFET;
7) maximum junction temperature $T_{j,\max} \leq 140/165$ °C for SiC JFET.

Fig. 11 shows the results for the cases where the chip area is adapted so that the efficiency and/or the power density is the same for the Si- and the SiC-based converters and for the case where the chip area of the SiC devices is fixed to a fifth of the Si MOSFET. In all cases, the results for a junction temperature limit of the SiC JFET of 140 °C and 165 °C are shown, and it is assumed that the switches of the full-bridge converter are mounted on a different heat sink from that of the output rectifier diodes. With a junction temperature limit of 165 °C, the heat-sink temperature reaches a peak temperature of 160 °C, which requires a thermal isolation between the heat sink and the other components. In general, the heat-sink temperature is relatively close to the junction temperature in an optimized design since the thermal resistance between the junction and heat sink is relatively small. Consequently, with a junction temperature limit of 165 °C, the heat-sink temperature is also high.

The calculated peak-power density of 17.7 kW/dm^3 also has to be considered against the background of the high heat-sink temperature because a thermal isolation is not included in the power-density calculation so that in the real system, the power density might be lower. Basically, it is important to note that in the power density, only the net component volume is included, i.e., the power density decreases to roughly 2/3 (for systems without thermal isolation) in the final system due to the air in between the components required for insulation and due to the geometrically not matching housings of the components.

For achieving the same efficiency with SiC devices as with the Si MOSFET, approximately 43%–54% of the chip area is required for the SiC JFET. Due to the high heat-sink temperature, the size of the cooling system decreases, and therefore, the power density increases to 17.7 kW/dm^3 for a junction temperature limit of 165 °C.

The same power density could be achieved if the SiC devices have 30%–40% of the Si MOSFET chip area. Here, with a lower junction temperature, approximately the same efficiency could be achieved with the SiC devices as the on resistance increases with junction temperature.

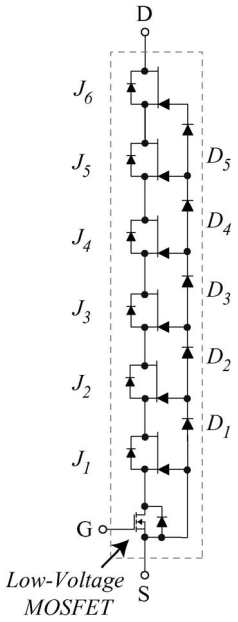


Fig. 12. Schematic of a Super Cascode consisting of six series-connected SiC JFETs and a silicon low-voltage MOSFET. At 5 kV, 5 A, and 25 °C, the Super Cascode has approximately 3.3-mJ turn-on losses, which decrease almost linearly to 1.2 mJ for 0 A. Due to the phase-shift operation, the turn-off losses are negligible [27].

B. High-Voltage Converter

The benefit of SiC devices in low-voltage applications is basically limited to some efficiency and/or power density increase–depending on the topology/application to a greater or lesser extent. However, with SiC devices, no major new application area is enabled except for environments with high ambient temperature. Moreover, the high costs of SiC devices and the new processing technology required for SiC often will constrict the application of the new devices to low-voltage systems.

Considering medium-voltage levels where new applications, for example, in future energy distribution, are emerging [23], [24], SiC devices could offer a functionality and performance which are not achievable with Si devices. In [25], for example, a 5-kV to 700-V isolated bidirectional dc–dc converter operating at 50 kHz is presented, which shows outstanding efficiency and power density enabled by the performance of SiC devices. The converter is based on the dual active bridge topology, which has soft-switching conditions, bidirectional power flow, and a relatively simple control [26].

On the 5-kV side, a cascode connection of normally on 1.2-kV JFETs and a low-voltage (40 V) Si MOSFET, as shown in Fig. 12 (a Super Cascode), is used. With this configuration, a blocking voltage of $6 \times 1.2\ \text{kV} = 7.2\ \text{kV}$ and very fast transients, as presented in [27], can be achieved. The voltage balancing of the JFETs is inherently achieved with avalanche diodes and additional small RC networks so that the whole Super Cascode could be controlled just via the gate of the Si-MOSFET and basically operates like a single switch.

The conduction losses in the dc–dc converter can simply be decreased by increasing the chip size of the JFETs and the MOSFET, and efficiencies in the range of 99% are possible with the SiC JFETs. Due to the ZVS operation, the high-

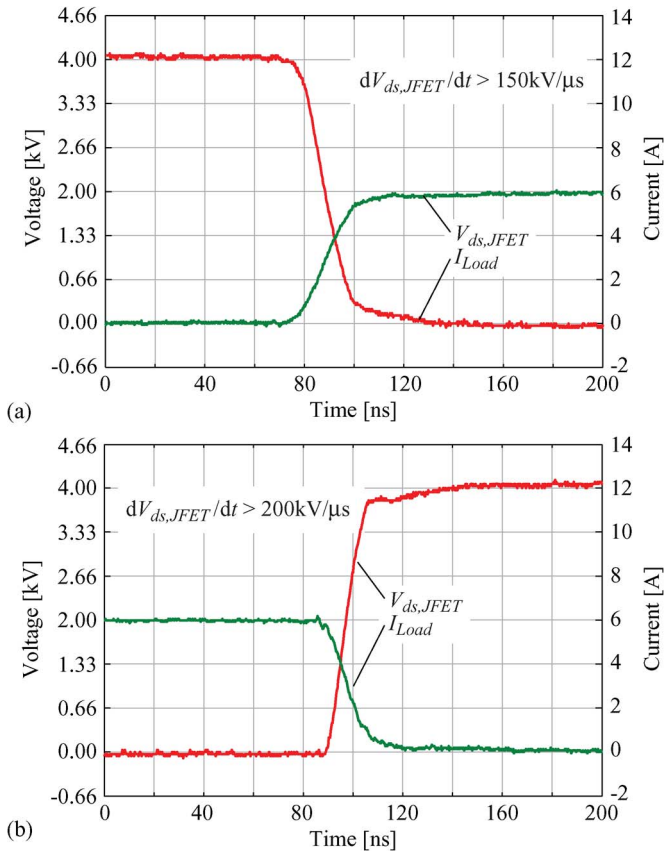


Fig. 13. (a) Turn-on and (b) turn-off switching transients of 6.5-kV JFETs in cascode connection operating as half bridge with ohmic load. The switches show outstanding transient performance enabling new converter concepts in the medium-voltage range.

operating frequency is possible, resulting in a very compact and low weight design. This could be, for example, very advantageously used in wind generators where the weight of the power-electronic conversion system directly influences the costs and size of the mechanical design of the tower/nacelle.

In the future, the operating voltage level of the Super Cascode will increase further, for example, by applying 6.5-kV JFETs. In Fig. 13, measurement results of such JFETs operating in a half-bridge connection are shown. Based on these, a Super Cascode with operating voltages of more than 20 kV will be possible, which will enable new converter concepts in this voltage range.

In addition to the semiconductors, other issues, e.g., the transient voltage distribution in the magnetic components, the packaging, and the low inductive/capacitive design meeting the requirements for high insulation voltages must also be solved before fast, ultracompact, and efficient SiC-based power-electronic converter systems in the voltage range higher than 10 kV will be available. However, with the functionality of such systems, the energy distribution and integration of fluctuating renewable energy sources will significantly change in the future.

IV. Conclusion

Considering low-voltage inverter drives limited to a few kilohertz switching frequency, the SiC switching devices do

not offer a performance boost compared with Si IGBTs, as a relatively high SiC chip area is required in order to achieve the same system performance as with Si. Just as with ultrahigh efficient drive systems ($> 99\%$) with SiC devices, a significantly smaller chip area is required as the unipolar devices allow an approximately linear conduction-loss reduction by increasing the chip area. This high efficiency could be advantageously used in converter systems for renewable energy e.g., photovoltaic, where the high costs of SiC will pay back to reduced losses and long operating time. In automotive industry, the higher possible junction temperature could be advantageous due to increased ambient temperatures if the converter is mounted close to a combustion engine. Furthermore, with SiC chips, a smaller footprint of the modules is possible.

In the area of low-voltage dc–dc converter where, very often, soft-switching conditions can be achieved with very low effort, SiC devices mainly offer the possibility of reducing the chip area for a desired efficiency. This could help to increase the power density as has been shown using the example of the nonisolated bidirectional buck–boost converter, where the chip area approximately could be reduced to 50% for achieving the same performance with SiC devices. Also, for isolated dc–dc converter for which a phase-shift converter with current-doubler rectifier has been evaluated in this paper, the main benefit is an improvement of power density and/or efficiency or the reduction of the chip area to approximately 35% at the same performance. Here, however, the costs of the SiC devices play an important role since these benefits often can be realized by significantly increasing the costs of the semiconductors. This might change in the future if the price of SiC devices drops.

In the future, the SiC devices could show a significant advantage compared with unipolar Si devices if the output capacitance of the SiC switches could be reduced significantly, as shown in [28], for GaN devices. This would reduce the switching losses in hard-switched applications resulting in a better efficiency and/or a more compact design.

Considering higher power levels and voltages in the medium-voltage-level range, the picture changes substantially since in this area, SiC devices offer a function and a performance which are not achievable with Si devices. In this paper, a 5-kV dc–dc converter operating at 50 kHz with an efficiency of approximately 99% is discussed. Such converters will play a significant role in the future (renewable) energy distribution and will allow a significant performance boost.

Also, in applications, e.g., accelerators or pulsed-power converters for medical systems, where a high output voltage is required, high-voltage SiC diodes offer a significant advantage as these enable a reduction of the total voltage drop across the rectifier, resulting in lower losses.

In particular, in such a high-voltage system and also in the considered low-voltage converters, passive components, isolation issues, and converter design must not be neglected since these often limit the system performance as much as the switches do. A good example are motor drives, where the dv/dt often must be reduced, even with the application of standard IGBTs, in order not to harm the isolation of the windings or to limit capacitive charging currents.

The results for the different systems could be summarized as shown in Fig. 14, where a clear performance improvement with

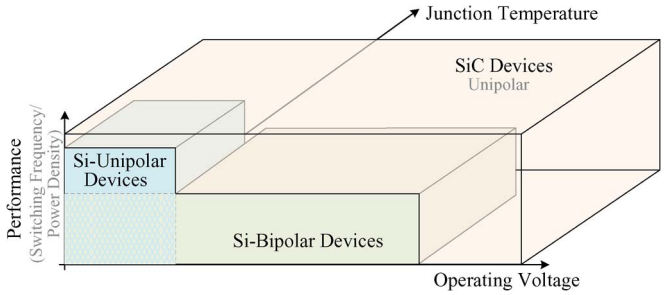


Fig. 14. Nowadays, SiC devices offer only a small performance improvement with respect to efficiency/power density in the lower operating-voltage range compared with current Si MOSFETs. With increasing operating voltages, the performance improvement increases significantly, particularly as there are only bipolar Si switching devices available which are relatively slow. The maximal possible operating temperature of SiC devices is significantly higher than that of the Si devices.

SiC devices is shown at higher operating-voltage levels and no unipolar Si devices are available. With current SiC devices, there is no significant performance improvement compared with unipolar Si devices, and, considering the costs, SiC devices have a clear disadvantage as the reduction of chip area is relatively small compared with the cost ratio between Si and SiC. This is also confirmed by the results which are presented in [1] for a single-phase PFC converter where some of the JFETs by SiCED show a lower performance than the Si switches, and only the JFETs by SemiSouth show a slight improvement from 99.09% to 99.14% efficiency. Therefore, it is also important to bear in mind that the SiC devices are relatively young and definitely will improve significantly in the future.

In addition to SiC, other wide bandgap materials, for example, GaN also shows interesting material properties and theoretically enables a tremendous reduction of the specific on resistance, which has an even lower theoretical limit than SiC. The GaN devices have a lower gate charge, and the output capacitance is also smaller [28], which reduces switching losses mainly in hard-switched applications. Furthermore, the processing of the material is simpler and might allow a faster decrease of production costs than is possible with SiC [29], [30].

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Mario Schweizer (S'08) was born in Münsterlingen, Switzerland, on February 20, 1983. He received the M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Zürich, Switzerland, in 2000. His Master thesis research involved implementation of a new control hardware and different control strategies for an ultrasparse matrix converter. He has been working toward the Ph.D. degree in the Power Electronic Systems Laboratory, ETH Zurich, since July 2008.

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