On-Line Semiconductor Switching Loss Measurement System for an Advanced Condition Monitoring Concept

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Keywords

≪Switching losses≫, ≪Current sensor≫, ≪Diagnostics≫, ≪Reliability≫, ≪IGBT≫, ≪Wind energy≫

Abstract

In this paper, an FPGA-based on-line switching loss measurement system for an advanced condition monitoring system is presented. For this purpose, an on-line measurement system for the semiconductor voltage and current transients integrated at the gate-driver voltage level is proposed. This system and the switching loss calculations are verified by experimental results.

Introduction

In this paper, an on-line semiconductor switching loss measurement system as part of an FPGA-based on-line condition monitoring system for high power IGBT modules is presented. The intended application of the condition monitoring system is for power semiconductor modules of wind turbine converters located in offshore wind farms. The accessibility of offshore wind turbines is very limited depending on weather conditions. Therefore, single failures can cause long downtime. The objective of the system is to increase the availability of the wind turbines by enabling better scheduling of replacement of aged power modules before reaching end of life.

The condition monitoring system focuses on two indicators for power module degradation, the on-state voltage and the thermal resistance. With these parameters, a bond wire lift-off and solder fatigue can be

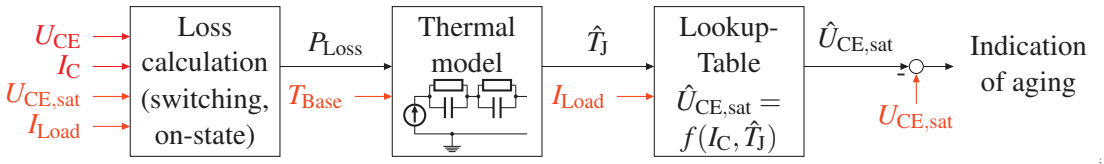

Fig. 1: Concept of the condition monitoring system

detected [1]. For the identification, the on-state voltage, the junction temperature, and the load current are necessary (Fig. 1). However, a direct measurement of the junction temperature is difficult to realize in a power module. Instead, the junction temperature could be determined by temperature-sensitive parameters. Sensitive parameters are the on-state voltage [2] or different parameters in the switching characteristic (e. g. shown in [3,4]). But parameter variations and module ageing could effect the monitoring system negatively. Another possibility is a model-based estimation of power losses and the junction temperature. But for a suitable estimation, detailed models are necessary, depending on various parameters. Furthermore, the losses and the thermal behavior are affected by ageing as well. Therefore, the junction temperature estimation is improved in the proposed monitoring system by using measured power losses (Fig. 1). This additionally enables a supervision of switching transients and losses and can be used for monitoring as well.

The semiconductor power losses can be classified into on-state losses and switching losses. The challenge for the on-state loss calculation is the accurate measurement of the on-state voltage. Possible circuits are discussed in [5].

In the proposed system, the switching losses are calculated by the transient voltage and current waveforms at the semiconductors. Therefore, fast measurement systems for a wide voltage and current range are presented in this paper. Furthermore, the current measurement must be implemented without increasing the switching losses by adding inductance to the commutation circuit. Two suitable concepts are presented and evaluated in this paper. The first one uses the voltage across parasitic inductances inside the module. It was shown that the inductance between the auxiliary emitter and the power emitter can be used for di/dt control during switching [6,7] or for over-current fault detection [8,9]. A combination of both functions is presented in [10]. In [11], the induced voltage is used for a load current estimation. For this purpose, the voltage is integrated by an analog integrator. A transient collector current estimation during switching is not investigated in the paper. The second approach is a PCB Rogowski coil. Concepts of it are presented in [12] and [13]. The design of the coil and the measurement errors are investigated in detail in [14]. The PCB Rogowski coil is suitable for di/dt control as well as for over-current protection. This is shown in [15] and [16].

In this paper, the digitizing system for collector-emitter voltage and collector current implemented at semiconductor voltage level are presented. Furthermore, the data processing in the FPGA is described. The system serves for calculating the losses of the IGBT and the antiparallel diode. For verification, experimental results from a prototype are given and compared to results from oscilloscope measurements with conventional voltage and current probes. The proposed system is designed for an Infineon PrimePACK^{TM}3 half-bridge power module. This is a widely-used module, but the concept can of course be adapted to other power modules.

Concept and Implementation

The proposed concept consists of analog-to-digital converters (ADC) and an FPGA and is separated into top and bottom systems (Fig. 2 and Fig. 4). The bottom system is located at the voltage level of the gate driver. Thus, no isolators are required for data acquisition and high ADC sampling rates and fast digital signal processing are possible. The top system is located at the auxiliary collector voltage level of the top IGBT. This voltage level is close to the positive DC link voltage level. The advantage compared to the gate driver voltage level of the top IGBT is that the reference ground changes only slightly during switching. Also, integration for several devices on one PCB is easier.

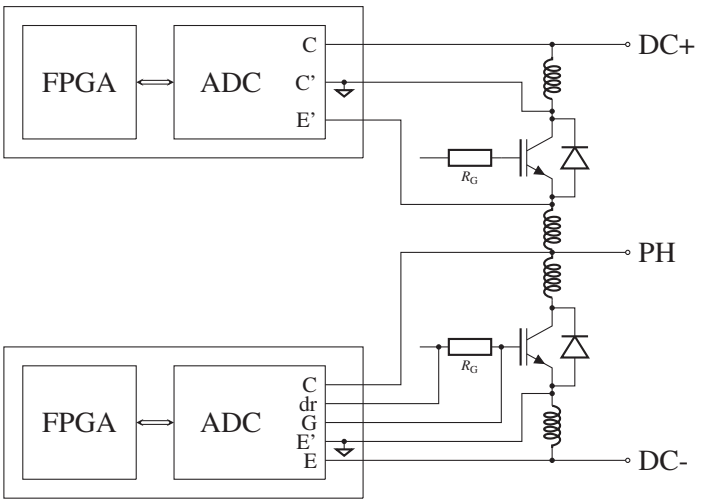

Fig. 2: Schematic of the measurement system using parasitic inductances for the transient collector current estimation

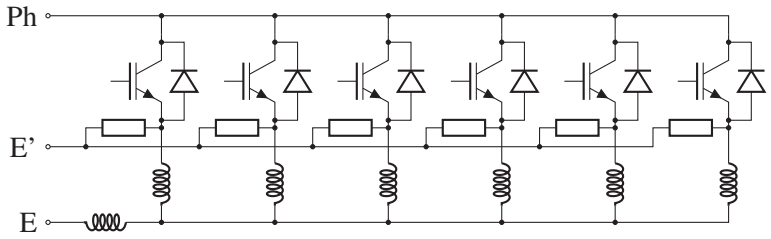

Fig. 3: Schematic of the low side switch in the selected power module

The time periods of the current and voltage transients during switching are below 100 ns. Therefore, an accurate loss calculation requires high sampling rates and large input ranges. In the prototype, a sampling rate of 125 mega samples per second (MSPS) at 12 bits resolution is realized. The collector-emitter voltage is reduced to the ADC input range by a frequency-compensated voltage divider. For the collector current measurement, two approaches are presented in the following sections. Both approaches are based on measurements of voltages which are proportional to the derivation of the collector current. The necessary integration for the collector current calculation is implemented as a discrete integration in the FPGA.

During switching, the losses are calculated by a discrete integration of the product of voltage and current in the FPGA. Beginning and end of the switching are detected in the FPGA by the measured signals. Thus, the discrete integrations for the collector current calculation and the loss calculation can be triggered internally.

Collector Current Measurement by Parasitic Inductances

The first approach for transient current measurement uses the induced voltages at parasitic inductances inside the power module. In Fig. 2, the concept for the loss calculation system for the top and bottom switches including this approach is given. For the current measurement of the bottom switch, the induced voltage at the parasitic inductance between auxiliary emitter terminal (E') and main emitter terminal (E) is selected. This voltage ($V_{\mathrm{EE'}}$) is influenced by the gate current (I_{G}) as well. The resulting voltage equation is given in eq. 1. The induced voltage at the inductance of the auxiliary emitter ($L_{\mathrm{E'}}$) can be neglected because of the low gate current gradient in the period of the collector current transient. Due to the high collector current gradient, the resistance of the main emitter path is very small compared to the impedance of the parasitic inductance. Thus the corresponding voltage does not need to be considered. Depending on the power module, the resistance of the auxiliary emitter cannot be neglected. In the selected module, six half-bridge substrates are connected in parallel. The auxiliary emitters of

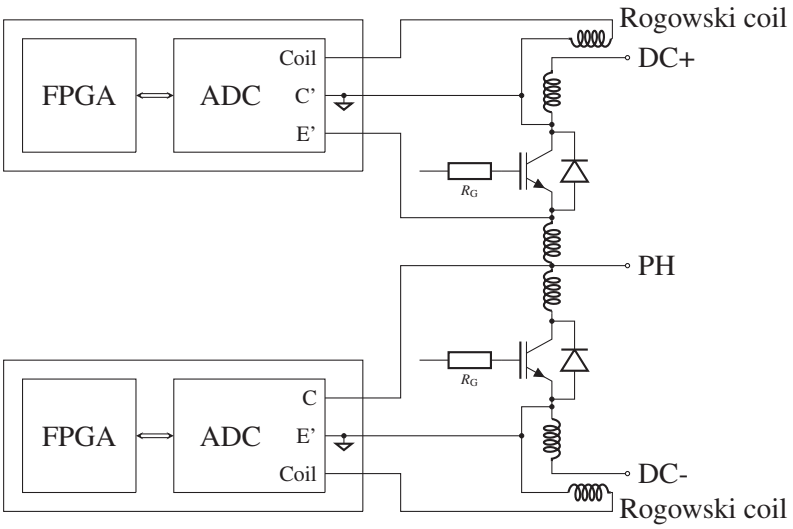

Fig. 4: Schematic of the measurement system using PCB Rogowski coils for the transient collector current estimation

the paralleled IGBTs are connected via resistors to avoid oscillations between the IGBTs during switching (Fig. 3). These resistors must be considered. The gate current can be determined by measurement of the voltages before and behind the external gate resistor (eq. 2). The equation resulting from these assumptions is given in eq. 3.

$$V_{\mathrm{EE'}} = R_{\mathrm{E'}}\, I_{\mathrm{G}} + L_{\mathrm{E'}}\, \frac{\mathrm{d}I_{\mathrm{G}}}{\mathrm{d}t} - R_{\mathrm{E}}\, I_{\mathrm{C}} - L_{\mathrm{E}}\, \frac{\mathrm{d}I_{\mathrm{C}}}{\mathrm{d}t} \tag{1}$$

$$I_{\mathrm{G}} = \frac{V_{\mathrm{G}} - V_{\mathrm{dr}}}{R_{\mathrm{G}}} \tag{2}$$

$$I_{\mathrm{C,bot}}(t) \approx -\frac{1}{L_{\mathrm{E}}} \int_0^t V_{\mathrm{EE'}}(\tau) - \frac{R_{\mathrm{E'}}}{R_{\mathrm{G}}}\, \left(V_{\mathrm{G}}(\tau) - V_{\mathrm{dr}}(\tau)\right)\, \mathrm{d}\tau + I_{\mathrm{C,bot}}(0) \tag{3}$$

The current of the top switch is estimated by the induced voltage between the main collector terminal (C) and the auxiliary collector terminal (C'). In the selected module, the auxiliary collector is intended to be used for the desaturation detection. The advantage of the voltage ($V_{\mathrm{CC'}}$) is that it is not affected by the gate current (eq. 5). Furthermore, the positive DC link voltage can be used as reference ground.

$$V_{\mathrm{CC'}} = R_{\mathrm{C}}\, I_{\mathrm{C}} + L_{\mathrm{C}}\, \frac{\mathrm{d}I_{\mathrm{C}}}{\mathrm{d}t} \tag{4}$$

$$I_{\mathrm{C,top}}(t) \approx \frac{1}{L_{\mathrm{C}}} \int_0^t V_{\mathrm{CC'}}(\tau)\, \mathrm{d}\tau + I_{\mathrm{C,top}}(0) \tag{5}$$

The currents during switching are calculated in the FPGAs by eq. 3 and eq. 5. For turn-on, the start currents $I_{\mathrm{C,bot}}(0)$ and $I_{\mathrm{C,top}}(0)$ are zero. The load current measured for the inverter control system can be used as start values for turn-off. The inductances for the current calculations can be determined by reference measurements for the module.

Collector Current Measurement by PCB Rogowski Coils

The second current measurement approach is the implementation of two independent PCB Rogowski coils. The resulting concept of the loss calculation system is given in Fig. 4. The derivation of the

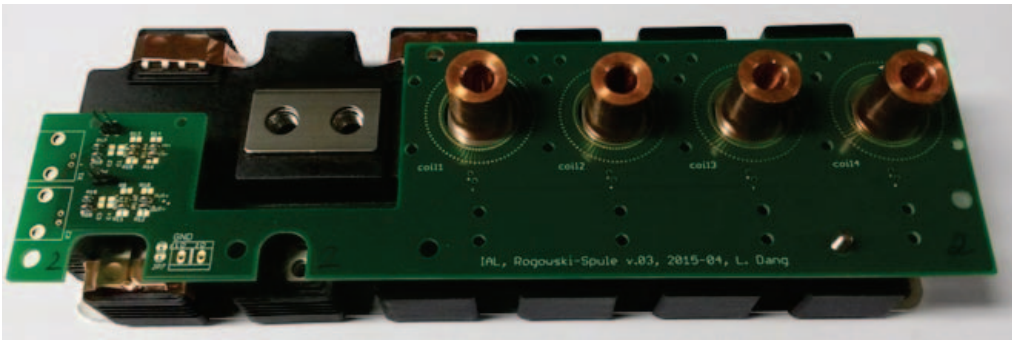

Fig. 5: Photograph of the IGBT module with the PCB Rogowski coils

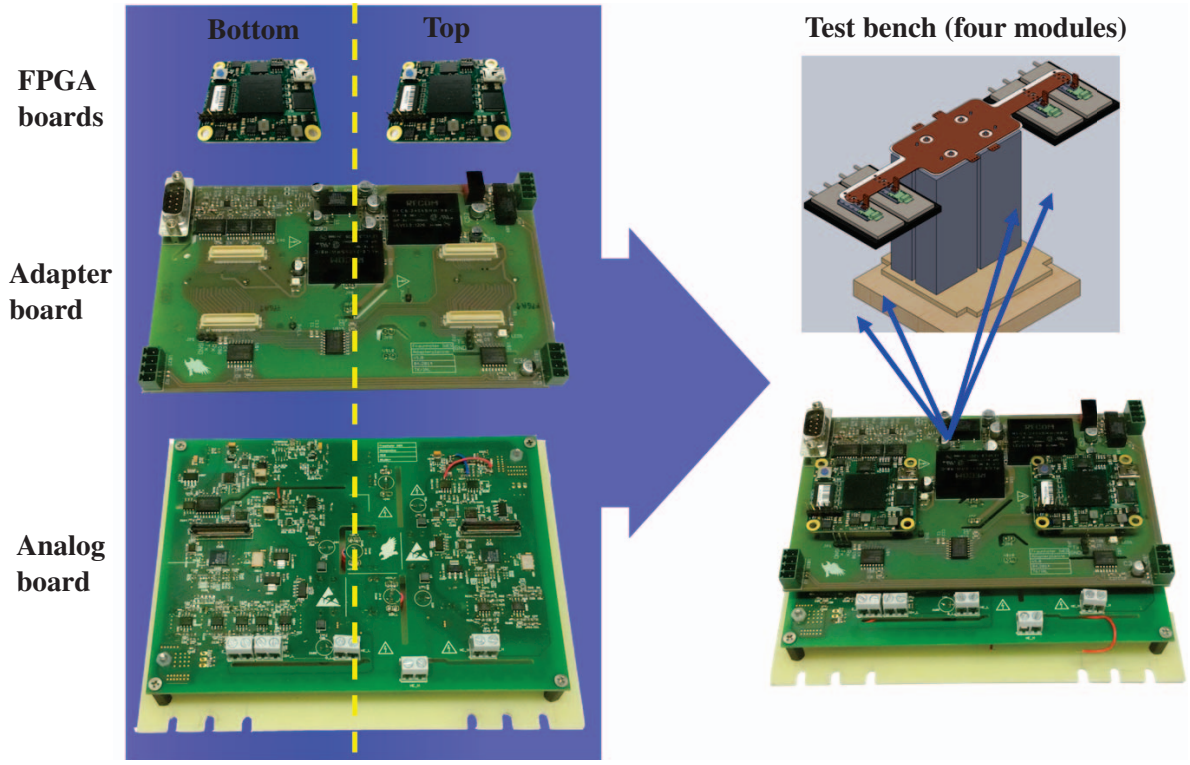

Fig. 6: Prototype of the condition monitoring system containing the switching loss measurement system

collector current of the bottom IGBT is measured by two coils in series around the two DC- terminals (Fig. 5, coil number 2 and 4). For the top switch, coils around the DC+ terminals are applied (Fig. 5, coil number 1 and 3). The advantage of the PCB Rogowski coils in comparison to the first approach is the independence from module parameters. The collector current can be calculated by the integration of the measured coil voltages (eq. 6). Instead of the self-inductance, the mutual inductance (M_{Coil}) between DC interconnections and the Rogowski coils must be determined here.

$$I_{\mathrm{C}}(t) = \frac{1}{M_{\mathrm{Coil}}} \int_0^t V_{\mathrm{Coil}}(\tau)\, \mathrm{d}\tau + I_{\mathrm{C}}(0) \tag{6}$$

Experimental Results

The prototype is designed for a 1700 V / 1000 A PrimePACK$^{\mathrm{TM}}$3 with silicon IGBTs and diodes. The prototype is separated into three parts (Fig. 6). The analog board contains the analog preprocessing and

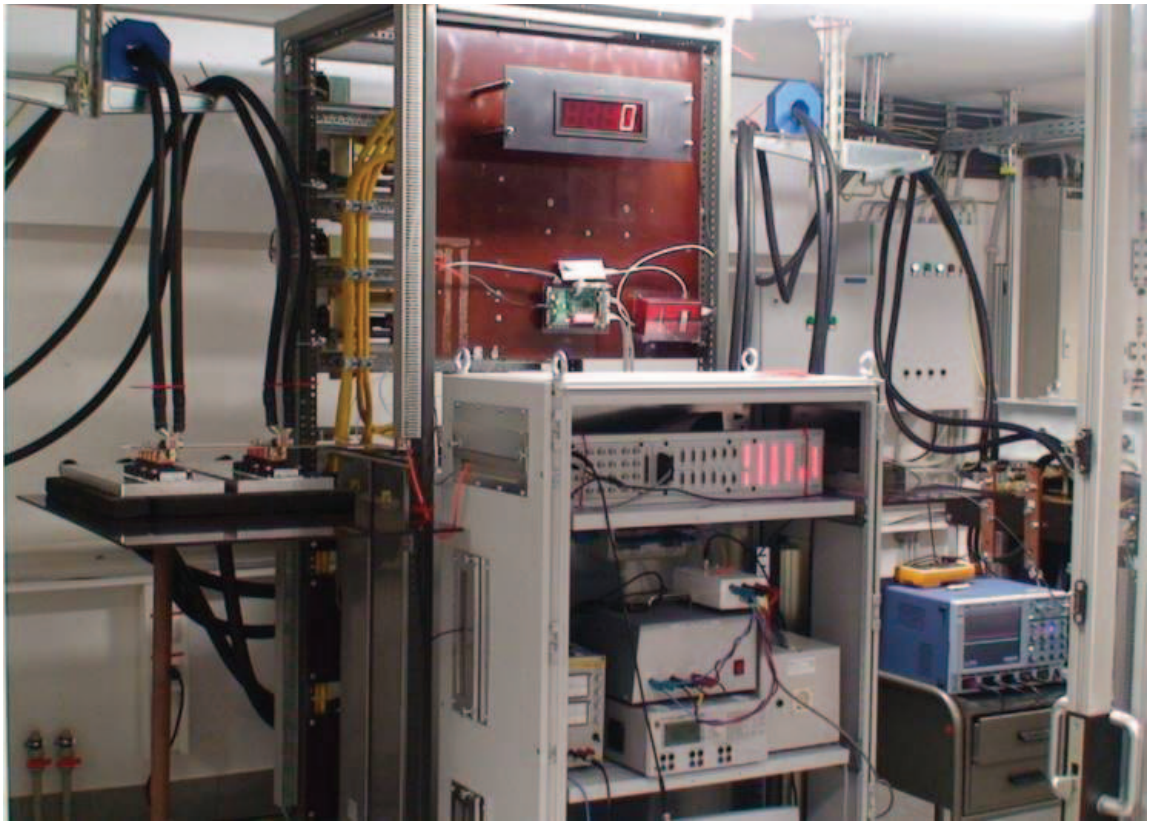

Fig. 7: Photograph of the test bench

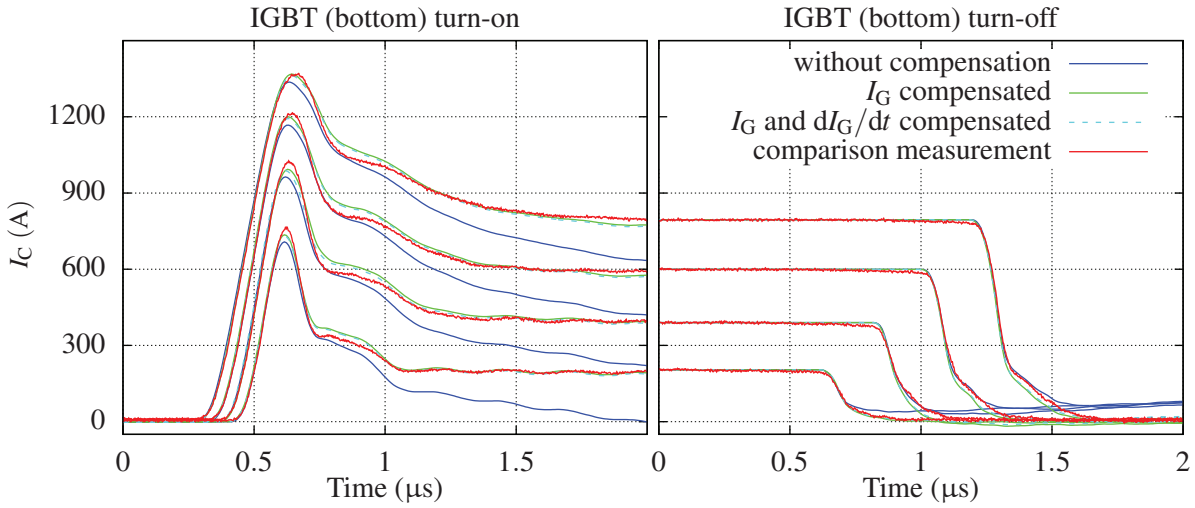

Fig. 8: Investigation of the gate current effect to the collector current calculation for several load currents

the analog to digital converters. The next board connects the analog board to the commercial FPGA boards. Furthermore, it contains the power supplies for the digital parts of the prototype. Top and bottom side are isolated against each other on these boards.

The test bench for the experimental tests consists of two H-bridges (Fig. 7) connected to one DC link capacitor (in the center of the test bench). Furthermore, the outputs of each H-bridge are connected to an inductor as a load. The prototype is validated by double-pulse tests performed on one of these H-bridges. For the validation, current and voltage at the semiconductor are compared to measurements by an oscilloscope with conventional voltage and current probes.

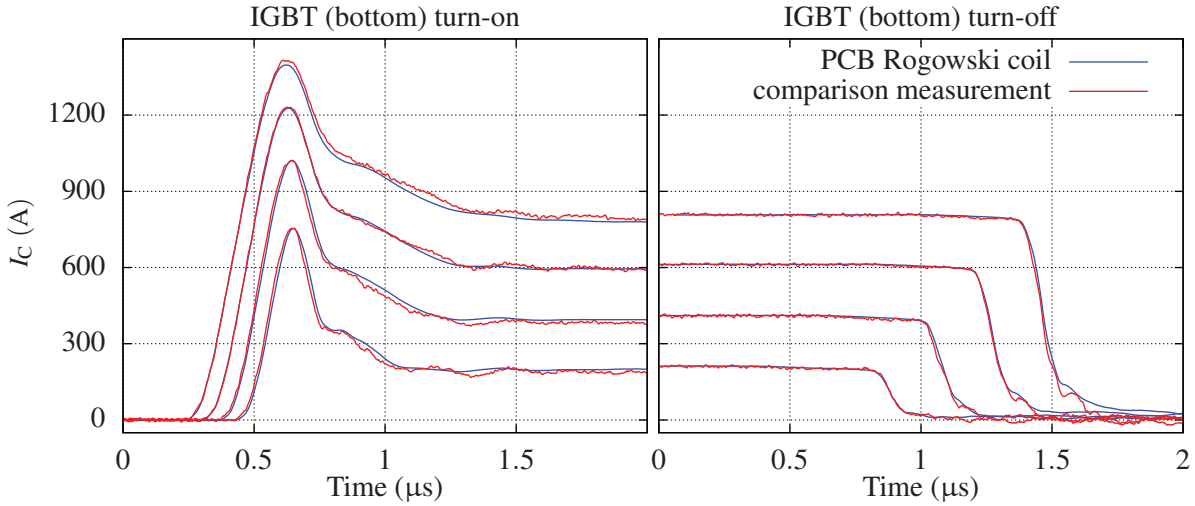

Fig. 9: Investigation of the PCB Rogowski coil for several load currents

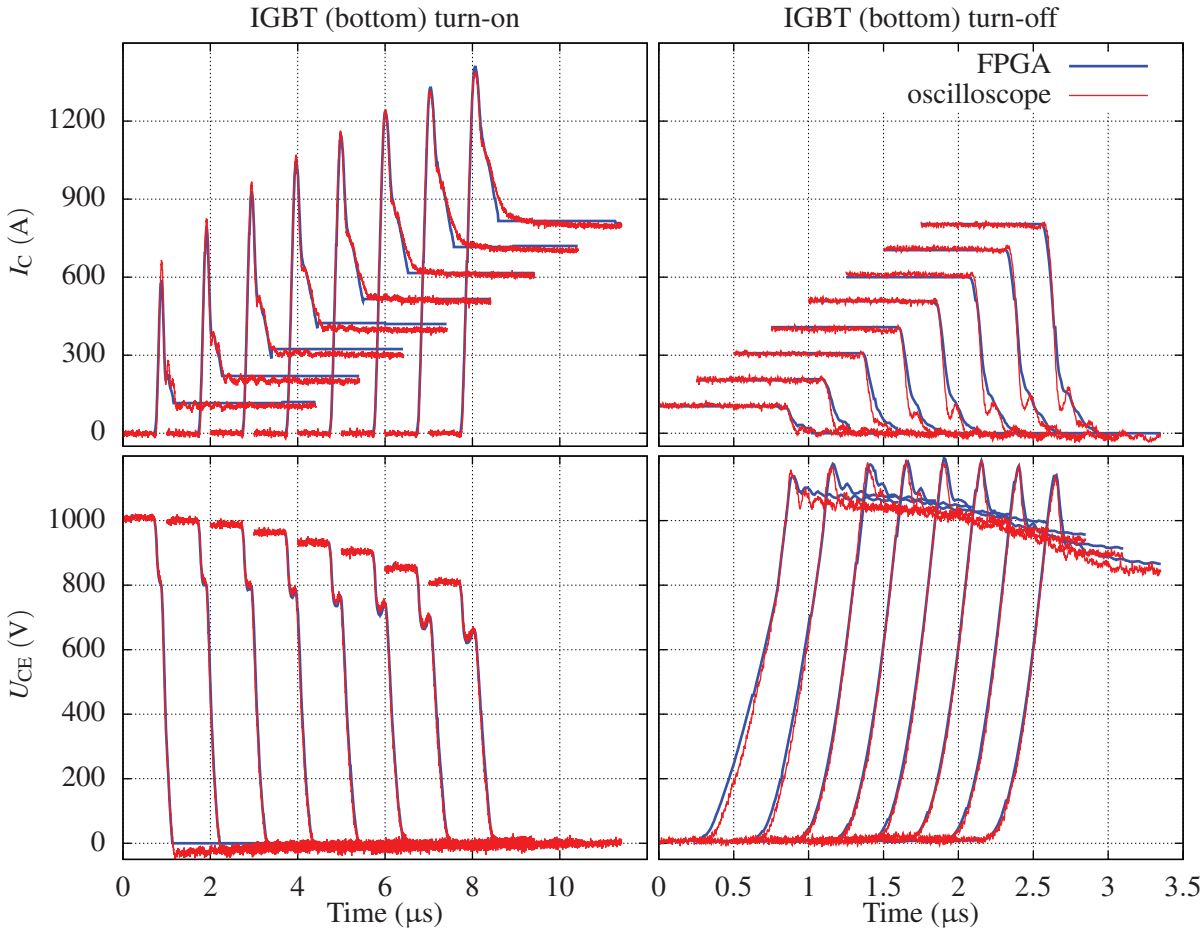

Fig. 10: Collector current and collector-emitter voltage of the bottom IGBT for several load currents (parasitic emitter inductance used for collector current estimation)

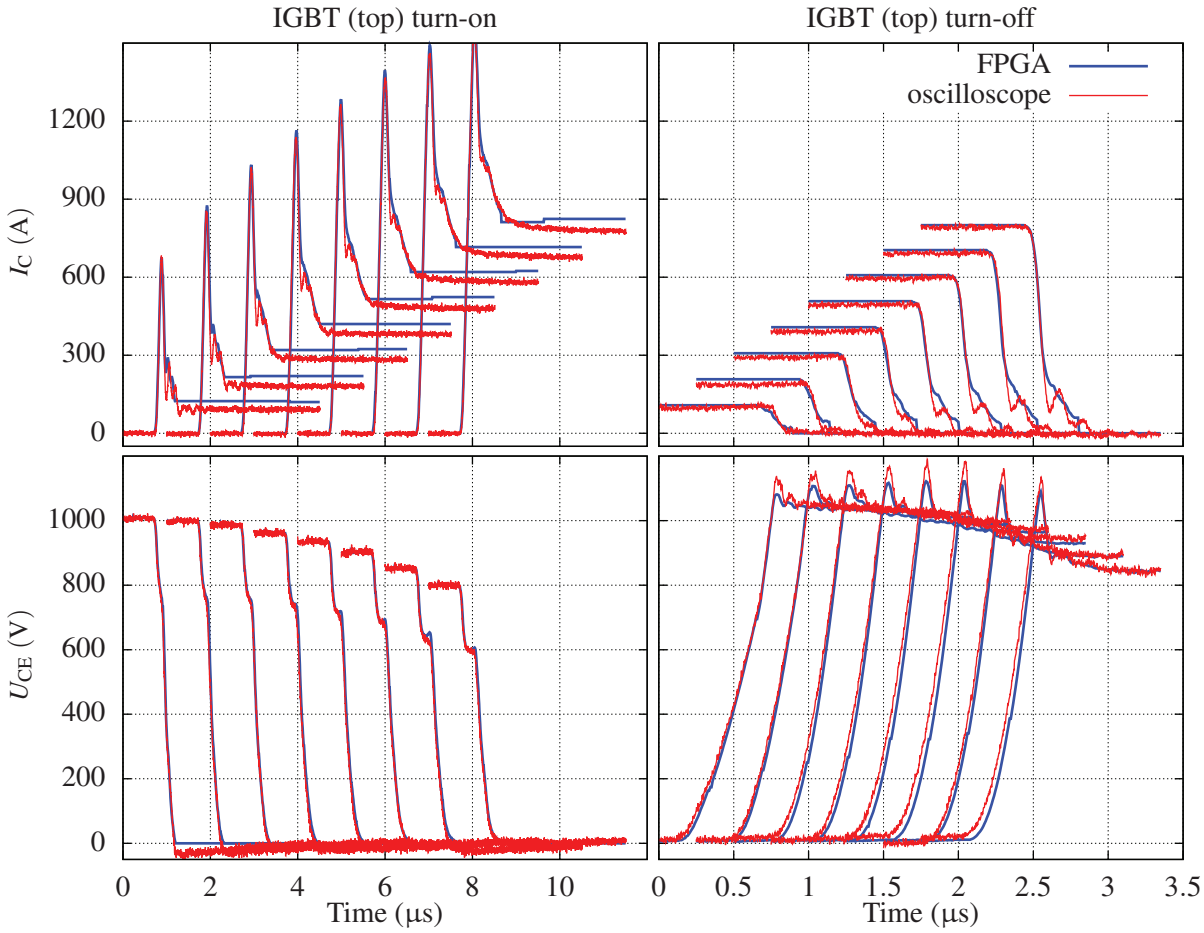

Fig. 11: Collector current and collector-emitter voltage of the top IGBT for several load currents (parasitic collector inductance used for collector current estimation)

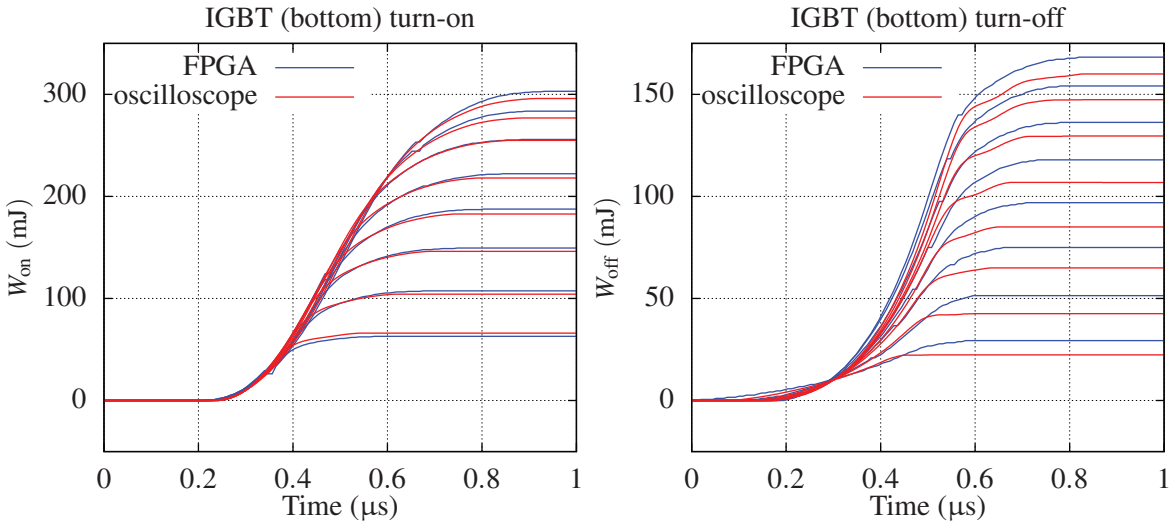

Fig. 12: Accumulated switching energies for several load currents ($I_{Load} = 100\,A \ldots 800\,A$)

Signal Accuracy

In the first step, the two proposed current measurement approaches are investigated by experimental tests. In Fig. 8, the influence of the gate current on the collector current calculation caused by the voltage induced between main and auxiliary emitter is analyzed. Therefore, the calculated currents without gate current compensation, with gate current compensation, and with gate current and gate current gradient compensation are given. For this investigation, the digitized voltages are stored in the FPGA during the double-pulse test and sent to a PC afterwards. The resulting collector current is calculated off-line. The comparison to the reference measurement using a commercial Rogowski current probe confirms the need for a gate current compensation. Furthermore, it proves that the effect of the gate current gradient on the measurement can be neglected. The calculated collector current waveforms with gate current compensation show a good correlation with the comparative waveform. The experimental results for the measurement approach by PCB Rogowski coil in Fig. 9 show that it is very suitable for this application.

In the next step, the analog and digital data acquisition including the data processing for the collector current calculation in the FPGA is tested. For the tests, the collector current is calculated by the voltage across parasitic inductances (Fig. 2). The data are stored in the FPGA memory with 125 MSPS during the double-pulse tests and sent to a PC afterwards. The switching waveforms of collector-emitter voltages and collector currents at the bottom IGBT for several load currents are given in Fig. 10. For comparison, the voltages and currents from an oscilloscope measured with conventional probes are presented in Fig. 10, too. The results for the top IGBT are given in Fig. 11. The waveforms from the FPGA match the comparative waveforms very well. An exception is the collector tail current during turn-off in the section after the steep current decrease. The current waveforms from the comparison measurements are oscillating in this section. But these oscillations appear only when voltages are measured with the same oscilloscope at the same time. For the measurements with no passive voltage probes connected, these oscillations do not occur (Fig. 8). Thus, the waveforms acquired by the FPGA are more realistic here than the oscilloscope traces.

Switching losses

In Fig. 12, the accumulated switching loss energies from the FPGA are compared to the energies determined by the oscilloscope measurements. The turn-on energies correlate very well. The differences are between 2.4 % at 800 A load current and 4.5 % at 100 A. The described differences between the turn-off collector current measurements also lead to larger differences between the turn-off energies. Again, the FPGA results are more realistic than the oscilloscope results here.

Conclusion

In this paper, an on-line switching loss calculation system is introduced. The system is integrated in an FPGA which is located at semiconductor voltage level. The switching losses are calculated by measured semiconductor voltage and current waveforms. It is shown that by the integration of the system at semiconductor voltage level, fast and accurate data acquisition is possible. Furthermore, two transient collector current measurement methods are presented. They enable the necessary on-line current measurement for the proposed system. The correct operation of the voltage and the current measurements as well as the functioning of the full switching loss calculation system are confirmed by experimental test results. The presented system enables an on-line junction temperature estimation which can be used for an advanced condition monitoring system.

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