High-Side Driving under High-Switching Speed: Technical Challenges and Testing Methods

Mehmet Kazanbas, Andressa Schittler, Samuel Araújo, Peter Zacharias
Center of Competence for Distributed Electric Power Technology (KDEE)
University of Kassel, Wilhelmshöher Allee 71, D-34121 Kassel, Germany
mehmet.kazanbas@uni-kassel.de

Abstract

The current design trend of power converters focuses on increasing efficiency and power density levels in order to minimize specific costs. Through the fast switching speed of semiconductors based on the wide-band gap (WBG) technology, such as Gallium-Nitride (GaN) and Silicon Carbide (SiC), it is possible to reduce the commutation losses, thus enabling higher switching frequency operation. Due to WBG devices high voltage variation rate during commutation, the galvanic isolation of high-side driver circuitries becomes a critical issue. The majority of state-of-the-art gate drivers are not suited for such high voltage transient levels due to limitations on the signal isolation. This paper will present an overview of current driver technologies for signal isolation, along with their inherent capabilities and limitations. An analysis of existing testing schemes and standards will be performed, making a parallel to real application conditions. Afterwards, tests considering such critical issues will be performed with selected devices. Finally, new testing and validation approaches for high-side driving isolation will be proposed regarding high-switching speed devices evaluation.

1. Introduction

1.1. Design aspects with innovative power semiconductors

In power converters design, there is a tradeoff among compactness, efficiency and cost, being the switching frequency increase without sacrificing the overall efficiency one of the main aims. Due to recent developments, this tradeoff can be achieved by the use of innovative power semiconductors such as SiC and GaN devices, which operate at high switching speeds thus reducing switching losses [1].
In order to validate such advantages, a 1.5 kW GaN-HEMT boost converter was built (Fig. Figure 1), with 250V input voltage and 350V output voltage. The converter was tested within two different scenarios: in the first one, the switching speed was kept under the limit of currently available gate drivers (100V/ns) and the switching frequency at 50 kHz, resulting in the measured European averaged efficiency of 98.98%; in the second scenario, the switching speed was increased to 150V/ns and the switching frequency to 150 kHz, with an efficiency level of 98.44%.
Moreover, from the first to the second configuration, the inductor had its volume reduced by a factor of two, which means that the power density can be correspondently increased. An output power sweeping for both scenarios is presented in Fig. Figure 2, where can be seen a reduction of only 0.54% in the Euro-Eta efficiency from the first to the second scenario. This is negligible efficiency reduction proves that the mentioned design aims can be achieved by increasing the switching speed.
On the other hand, state-of-the-art gate-drivers are not suited for such high rates of voltage variation with only very few examples specified at 100 V/ns. Furthermore, existing verification methods and standards for gate-drivers do not cover all aspects for such high switching speed levels, as tests found in safety standards are currently performed under switching transient times much larger than the ones from WBG-based switches.

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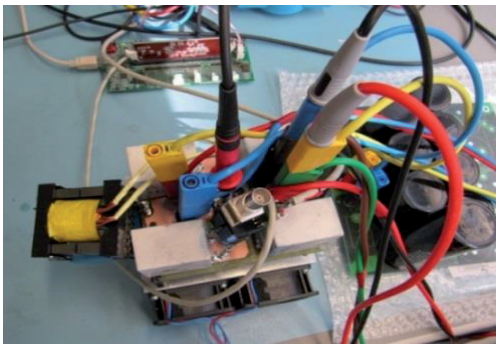

Figure 1: 1.5 kW Boost converter

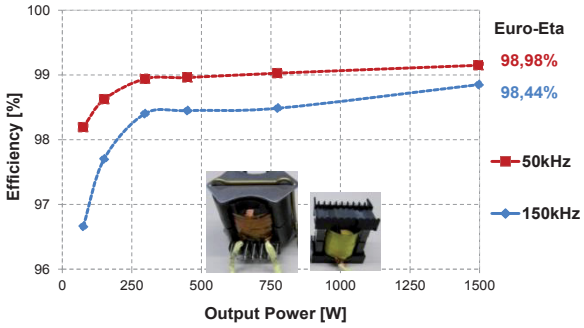

Figure 2: Efficiency curve at 250 Vin

1.2. High-side driving under high-switching speed

Due to high input voltages, power converters topologies with floating potential such as a half-bridge inverter need a galvanic isolated gate driver for the high-side switch, not only as a protection to the switch but also as a safety strategy, once the common-mode transient noise created by ground loops may affect systems stability as well as users' safety [2].
Depending on the switching states of the low side switch, the output side of the high-side driver is floating against the earth. As a result of the voltage transient of commutation events, a common-mode current can flow through parasitic capacitances (Fig. Figure 3). In order to limit these currents, isolation capacitances of signal as well as of supply devices should be as low as possible, especially in face of the capability of new Gallium-Nitride switches, that can commutate at more than 150V/ns [3].

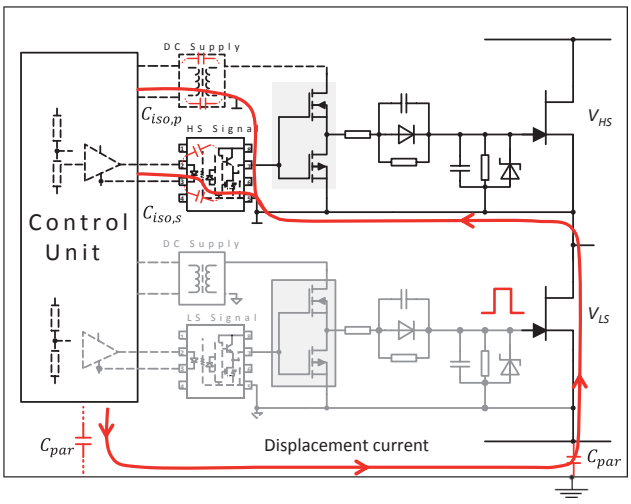

Figure 3: Common-mode current path

The peak value of the common mode current for different switching speeds can be calculated by Equation 1 and is illustrated in Fig. Figure 4. A simulation with a driver's Spice model has also been performed, in order to verify the disturbances with results presented in Fig. Figure 5. There not only the displacement currents can be observed, but also possible resultant voltage oscillations that might reach the device threshold level, probably leading bridge short-circuit.

Eq. 1. $$i_{CM} \approx C_p . \frac{\Delta V}{\Delta t}$$

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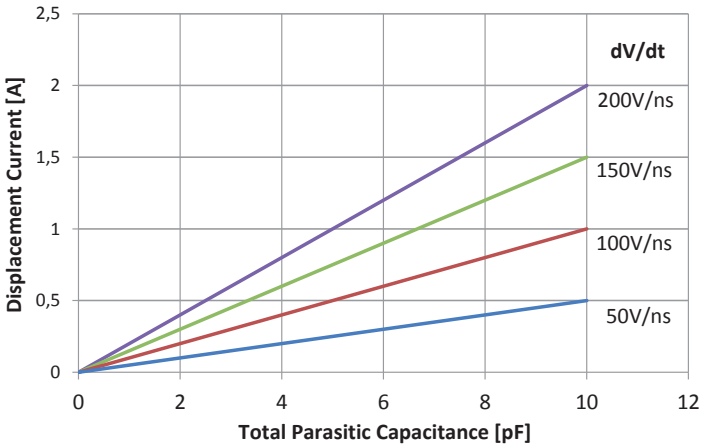

Figure 4: Displacement current versus galvanic isolation capacitance according to switching speed

Figure 5: Simulation results with different voltage slopes (input voltage of 500V)

This paper will focus on the analysis of state-of-the-art high-side drivers, as well as testing schemes and standards for common-mode rejection, verifying if they are still suitable for upcoming new semiconductor technologies.

2. Isolation approaches at component level

As previously seen, the coupling capacitance of isolation devices is the most significant factor in order to limit the amount of the common-mode noise. Table 1 shows different isolation solutions by using optic, magnetic and electric field that mainly differ in their mechanical structure, insulation material and thickness as well as isolation areas.
One of the most commonly used gate driver technology relies on the use of transformers at medium and high power level. Other gate driver technologies used at low power level rely on the GMR (Giant Magneto Resistance).

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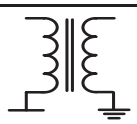
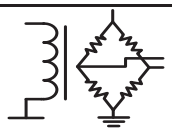
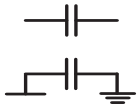
	Transmission by					
Technology	Magnetic field				Electric field	Light
	Pulse transformer	Core transformer	Coreless transformer	GMR	Capacitive	Optical
Structure						
Isolation type	Power and signal	Power or signal	Signal			
Isolation material	Various		SiO_2	Polyamide	SiO_2	Silicone and Polyamide
Distance through insulation	>2000µm		8µm-17µm			80µm-2000µm
Package	Magnet core		IC			
Integration	Complex		easy			
Limitation	Duty-cycle, efficiency, bulky, signal delay		EMI susceptibility		High voltage applications	LED degradation, timing performance

Table 1: Overview of supply and signal insulation technologies

3. Testing schemes and safety standards

At the gate-driver level, there are different standards concerning electrical tests, like partial discharge, insulation resistance, surge and overload for isolated devices. They principally vary in requirements for isolation levels with various applications and component structures. Furthermore, the safety isolation standards require a reinforced insulation for driving signal and supplying power, which can be achieved by using pulse transformers and optocouplers or new technologies such as digital isolators [2]. In table 2 the most important standards are presented according to the gate-driver isolation type.

Devices	***Norm***	***Region***	***Scope***
Core transformer	EN 61158	Europe	Safety of power transformers, power supplies, reactors and similar products
Optocoupler	IEC 60747-5-5	International	Semiconductor devices - Discrete devices – Part 5-5: Optoelectronic devices – Photocouplers
	UL 1577	US	Optical Isolators
Digital isolator	DIN VDE 0884-10	Germany	Semiconductor devices - magnetic and capacitive coupler for safe isolation

Table 2: Safety standards at component level

Based on these safety standards, there are mainly two testing schemes to verify the common-mode immunity of an isolation device. The first one is the static common-mode immunity test (Fig. Figure 6), which shows the signal-rejection ability when the input side is fixed at either logic-high or logic-low. In real applications, issues here might lead to falsely triggering the system in idle or standby state. The second one is the dynamic common-mode immunity test (Fig. Figure 7), that simulates real operation modes under which the system is found during common-mode stress. The device fails when the driving unit loses the control, possibly causing short-circuit and increased component stress, even leading to destruction. In both cases, voltage transient times are controlled by a voltage generator and the output stage is analyzed by an oscilloscope.

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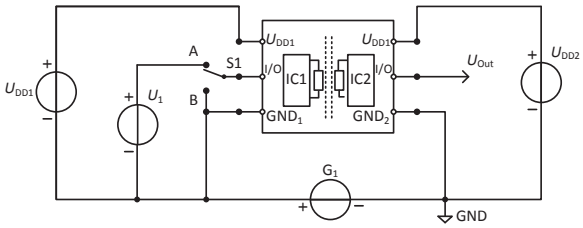

Figure 6: Static CM immunity test

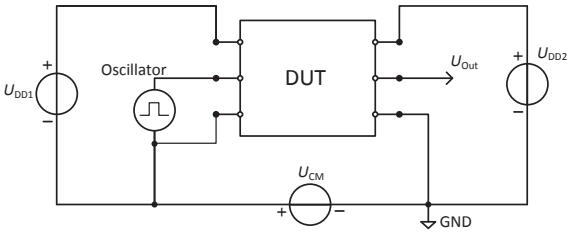

Figure 7: Dynamic CM immunity test

4. Robustness of gate drivers at different switching speeds

First of all, a new pulse generator capable of providing clear voltage steps in values in excess of 200V/ns at “prevalent” device voltage levels was developed and tested. According to state-of-the-art standards, parasitic currents generated by switches commutation are evaluated preventing unwanted gate triggering, either on or off. Such evaluation is conducted for both static and dynamic tests at 100V/ns voltage transient and 25°C, as follows:

At rise-off: as **Fehler! Verweisquelle konnte nicht gefunden werden.**, an unwanted/uncontrolled gate signal can be generated during the low-side switch turn-off. This is the most problematic case, as a short-circuit at the voltage source can occur, potentially harming users and damaging the system.

At rise-on: depicted in **Fehler! Verweisquelle konnte nicht gefunden werden.**, an overvoltage can occur at the high-side gate, potentially damaging the driver.

At fall-off: as depicted in Figure 8, a voltage at the driver’s output is induced due to the voltage transient during the turn-on of the lower side switch.

At fall-on: shown in Figure 9, the gate signal from the high side switch can be interrupted due to voltage transients at the lower side switch.

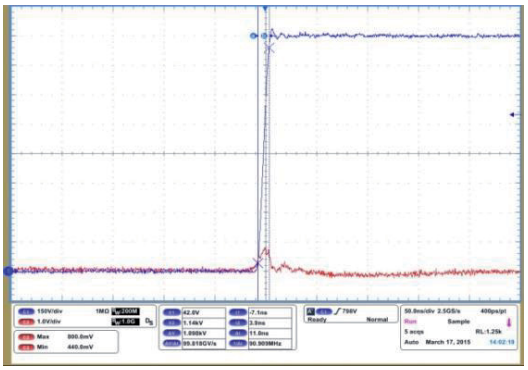

Figure 10: Rise-off: maximum voltage detected

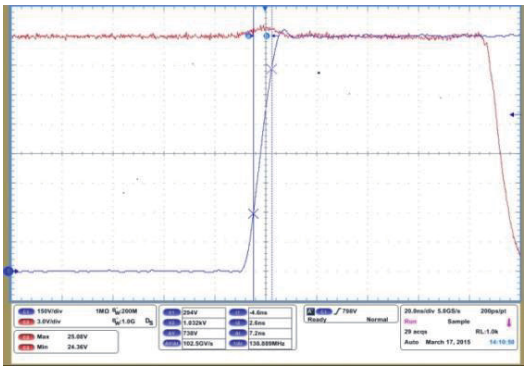

Figure 11: Rise-on: maximum voltage detected

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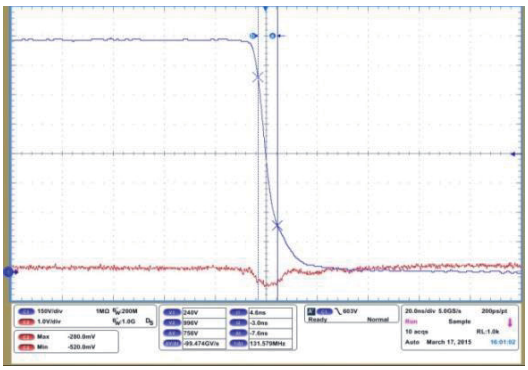

Figure 12: Fall-off: minimum voltage detected

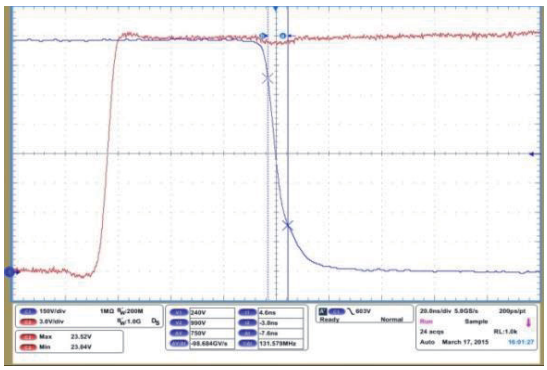

Figure 13: Fall-on: minimum voltage detected

As new technologies emerge, it is important to analyze if the standards cover all aspects in order to guarantee the proper system operation. For WBG-based switches, lower rise and fall times are observed, as well as lower threshold voltage and gate charge. Such changes can affect the standards, with introduction of the explicit requirement of minimum sample rate of oscilloscope and minimum bandwidth of probes.

4.1. Threshold voltage of semiconductor technologies

A review of the various semiconductors data has been performed in order to quantify the threshold voltage for each technology, which can be respectively seen at Fig.Figure 14 .
From Fig. 13, it can be concluded that the WBG-based switches, especially GaN, present very low threshold voltage. Consequently in a half-bridge topology, if the high-side gate driver is not properly isolated and tested against interference from the low-side commutation events, a short-circuit can occur and damage the circuit.

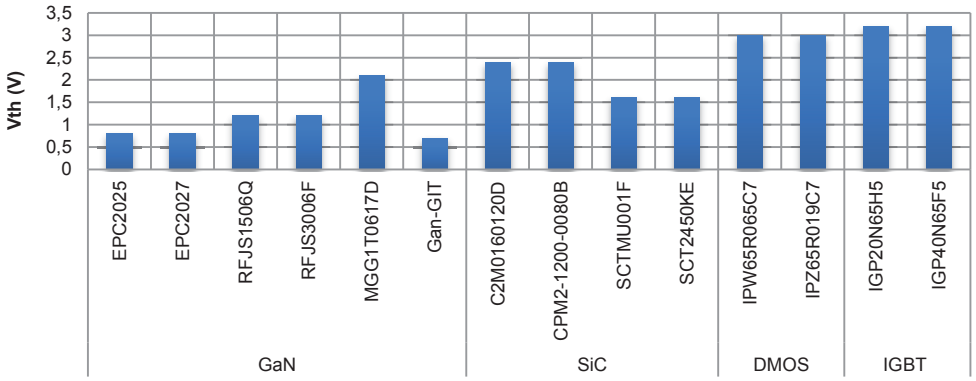

Figure 14: Threshold voltage versus technology

4.2. Static and Dynamic CM immunity tests

A variety of tests have been performed with two different gate driver ICs: Avago optocoupler, model ACPL-3130 (40V/ns) [5] and Infineon EiceDRIVER 1EDI20N12AF (100V/ns) [5], according to static and dynamic test requirements at the maximum working isolation voltage.

Based on measurement results, the most problematic case for high-side driver is actually at rise/off, because the high-side switch can be switched on due to the parasitic gate voltage. Therefore the comparison between static and dynamic test is essential, since this case is critical for the application level.

For the static test, the output voltage of the isolation device is 24V for the turn-on state while 0V is for the turn-off. In addition, the dynamic test is performed at the frequency of 1 MHz.

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The Optocoupler was tested at 630V. Figure 14 shows the test results at all test cases. Even though the parasitic gate voltage rise (Figure 15.a) is almost same for both test cases, it already reaches a critical value for new semiconductor devices. In rise on and fall off test conditions (Figure 15.b and c, respectively), some differences are also observed due to the high voltage transient, however they are not as relevant to the overall operation since they do not cause any damage in the circuit. False gate turn-off can also occur at the fall on case (Figure 15.d), as a voltage decrease is observed, however this situation has not been here measured.

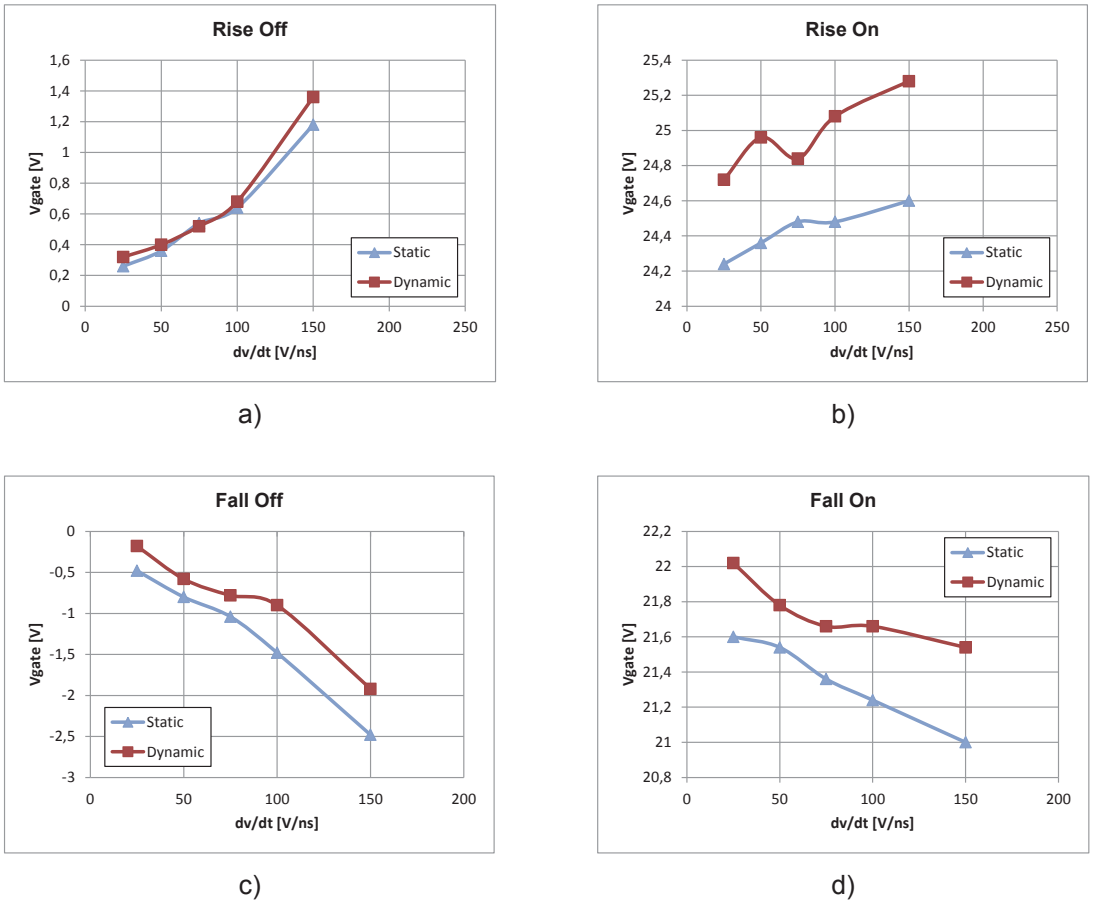

Figure 15: Test results for ACPL-3130

The same tests with Infineon's EiceDRIVER have been performed at 1200V (maximum rating) and the results are shown at Fig. Figure 16. For all cases, the dynamic performance shows higher parasitic voltage values than the static performance especially at rise off case.

The dynamic test is closer to the application condition and, as observed in the experimental results, more critical. Therefore it is important to require also the dynamic investigation in common-mode immunity test standards.

5. Conclusion

This paper presents an analysis of the state-of-the-art driver technologies for signal isolation. A review of standards and testing schemes has been also presented, in order to question if they are still applicable when newer semiconductors' technologies, such as GaN and SiC, are used. More investigation towards the gate voltage measurements is required to confirm if the disturbances at the drivers' isolation are capable of switching on and/or off the high-side

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gate. As the time constants for WBG-based technologies are much lower as usual Si-semiconductors, requirements such oscilloscope sample rate and probes bandwidth should also be suggested at such standards.

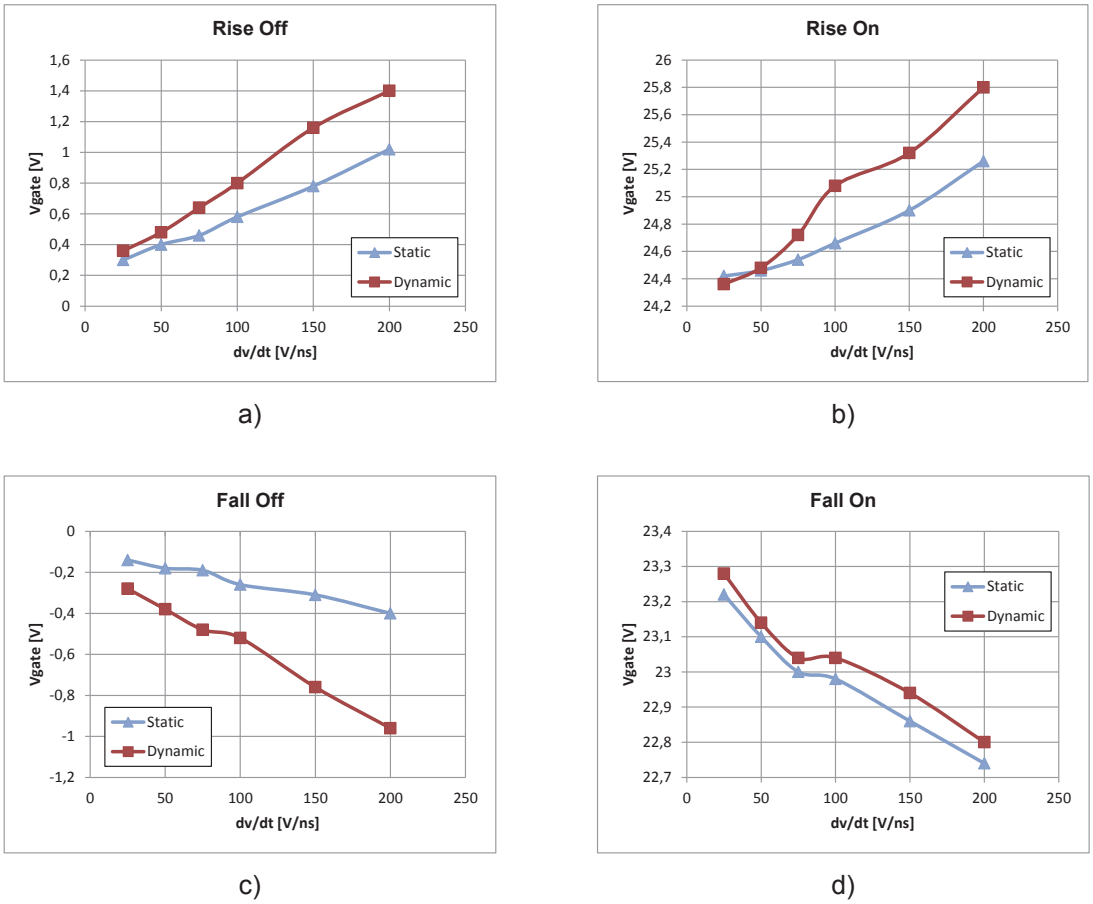

Figure 16: Test results for EiceDRIVER

6. Acknowledgments

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