Temperature Change Induced Degradation of SiC MOSFET Devices

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ABSTRACT

Besides the electric parameters of a semiconductor device, the lifetime is a key measure of quality. Overheating is one of the top failure causes in electronic systems. In this paper, a power cycling experiment done on silicon carbide (SiC) MOSFET devices is presented. The experimental setup and measurement conditions are described in detail and a discussion is given on the importance of the electrical setup and the control strategy.

The data collected during the power cycling are analyzed, and the primary failure modes are identified. The high-resolution monitoring of the voltage drop on the device, in combination with other monitored parameters, enables the detection of a bond wire lift-off or breakage. With the help of the thermal transient measurement and structure function analysis, the structural changes in the heat flow path can also be identified. Finally, the results of the electric measurements are compared and verified by scanning acoustic microscopy tests.

KEY WORDS: silicon carbide, power cycling, thermal transient testing, structure function, reliability testing, metal-oxide–semiconductor field-effect transistor (MOSFET)

NOMENCLATURE

k	temperature dependence [mV/K]
C_{th}	thermal capacitance [Ws/K]
I	current [A]
N_f	number of load cycles elapsed until device failure, [-]
R	electrical resistance [V]
R_{th}	thermal resistance [K/W]
V_f	forward voltage [V]
V_{th}	threshold voltage [V]

Subscripts

bond	bond wire
ch	channel
leads	leads between measurement point and bond wire pad
s	serial
DS	drain to source
GS	gate to source

INTRODUCTION

Because of its advantageous electrical and thermal properties, silicon carbide (SiC) as a semiconductor material has become the subject of great interest in the past one and a half decades. The sources of its outstanding performance are a wide band-gap, high breakdown voltage, and high thermal conductivity, which lead to higher efficiency, lower dissipation, smaller overall system size, and the opportunity for higher temperature operation [1]. For high-demand applications, the ruggedness of the silicon-carbide–based devices is not enough. The packaging of the semiconductor chip also has to be able to withstand these load conditions, which are typically high operation temperature, high current density, and high switching frequency [2]. New packaging technologies are being designed to fulfill these requirements, often using different materials than those used for silicon-based devices.

A general challenge is the elevated power density. Despite the faster switching transients and the lower switching losses, because of the typically higher switching frequencies, the overall dissipation does not change significantly compared to a silicon-based device. However, the size of the chip is typically much smaller because of the high cost of the SiC. This leads to elevated power density and the need for better heat spreading in the package [2]. The reduced chip area and the high current handling capability can also make it challenging to attach the bond wires in sufficient number and cross sections. To be able to handle the high current at high temperature, Au or Pt bond wires [3] or double-sided cooling might be used [2,4]. The good thermal and mechanical properties of the die-attach layer are also critical for package performance. High-melting–point solder materials [3,5] or the emerging sintering technology [6,7] can fulfill the requirements. Finally, the baseplate material also has to be carefully selected to be able to withstand the high copper thickness, while having sufficiently high thermal conductivity and a coefficient of thermal expansion similar to that of the semiconductor chip. In recent publications, AlN and SiN are typically mentioned as the most promising substrate materials [8]. These new technologies are promising higher reliability at the same operating conditions, but they all have to be thoroughly tested during the research and development phase to identify the weak points of the design and to enable the fine tuning of the technological parameters.

One of the most common causes of the failure is the temperature-induced degradation. During the normal operation of the devices, they are periodically heated up and cooled down because of the changing load conditions. This repeated temperature change rise leads to thermo-mechanical stresses and finally to the wear-out of the materials. Temperature

cycling and power cycling are two slightly different test methods for investigating the effect of periodical temperature changes on the device packaging.

The temperature cycling method defined by the JESD22-A104 JEDEC standard [9] is the most commonly used method because of its straightforward implementation. With temperature cycling, the device temperature is cyclically changed between two temperature extremes by the regulation of the environmental temperature. The temperature change rate is relatively slow to try to keep an even temperature distribution in the whole test specimen. This test method applies the same thermal load on all parts of the structure. The use of wide temperature extremes can greatly accelerate most thermo-mechanical stress-induced failure modes. Typical failure modes are substrate solder fatigue, die-attach delamination, and chip or substrate crack. The advantage of temperature cycling is that testing can be done in relatively high volumes on structures with dummy chips. However the test environment is very different from the normal application conditions; hence, it gives little information on the overall performance of the package. Accordingly, it is more suited for testing the reliability of selected features in the structure, especially large area interface layers like the substrate-baseplate contact technology.

The power cycling method (often called active cycling) uses the active chip to heat up the package and an application-like cooling environment to cool down the device when the heating is switched off. With appropriate regulation of the current and voltage drop on the device, controlling the dissipated heating power, the change rate of the temperature also could be regulated during both the heating and the cooling phase. Nevertheless, the most commonly used method is to apply stepwise changes between the heating and cooling states. In this case, the temperature change rate is only defined by the time constants of the test structure and only partly by the test environment. The rapid temperature change and the well-localized heat source leads to significant temperature gradients in the package structure. The features close to the junction of the chip will be exposed to higher temperature changes than the ones further away in the structure. According to the literature, this method was used primarily for bond wire testing [10], but the base of this classical view was that the wire bonding used to be the most vulnerable part of the whole structure in application-like load conditions. In later publications, it was shown that power cycling can also induce degradation in the die-attach and baseplate solder layers [11] (especially with appropriately selected test parameters). The advantage of the Power Cycling test method is that the resulting temperature and stress distribution in the test structure can be somewhat similar to the normal application conditions. Hence, it can give lifetime information not only about certain elements, but the entire structure.

The process and key parameters of the Power Cycling test method is defined by the JESD22-A122 JEDEC standard [12]; but because of the general wording of this standard, most of the test parameters are loosely defined. Measurement results acquired by different research groups can rarely be directly compared because of the differences in the measurement system and test parameters used during the experiments. All of these test parameters should be accurately documented and considered when different experiments are being compared.

In this paper, we demonstrate our power cycling test setup on a SiC metal-oxide–semiconductor field-effect transistor (MOSFET) device and discuss the effect of various parameters on the experienced device lifetime (N_f).

EXPERIMENTAL

One of the most important parameter of the power cycling is the change of the chip temperature during the cycles. Various methods are used for measuring the chip temperature, from a thermocouple-based solution to contactless IR temperature measurement setups, but each of these methods has their own drawbacks. The most straightforward way is to use a temperature-dependent electric parameter of the semiconductor device to measure its own temperature to be able to measure packaged components without removing the encapsulation. The thermal-impedance characterization method, also called thermal transient testing [13], is based on the same measurement principle, and hence the thermal transient measurement system could relatively easily be modified to be capable of doing power cycling tests.

Thermal transient testing

The temperature versus time response of a semiconductor chip which exposed to a power stepwise change is called thermal transient response. The semiconductor chip temperature measurement is based on the measurement of its temperature sensitive parameter (TSP). Nearly all semiconductor components such as diodes, bipolar junction transistors (BJTs), MOSFETs, insulated-gate bipolar transistors (IGBTs), and light emitting diodes (LEDs) have their own TSPs.

A typical TSP example is the forward voltage of a diode, which can be monitored using a small constant current. Most of the semiconductor components contain at least a parasitic diode that can be used for measurement purposes. Furthermore, the threshold voltage of a MOSFET or the channel resistance of a field-effect transistor (FET) can also be used for temperature sensing when a small constant current is applied.

The TSP has to be calibrated in order to translate the measured voltage into temperature. The calibration process requires the component placed into a temperature controlled environment. The TSP is registered at a range of temperature levels. This temperature dependence in the normal operation range of the devices can commonly assumed to be linear and the temperature dependence can be described with only the slope of the linear curve, the so-called k factor. When the linear assumption is not enough, a higher order curve can also be used for the transformation.

The thermal transient is captured from one steady state to another in order to characterize the whole system. A power step is applied to the component, and then the value of the TSP is measured with sufficiently high temporal and voltage resolution. This can be a jump from a lower to a higher power state or a jump from a higher power level to a lower one. In this way, the heating or the cooling transient of the device can be captured. Because the linear assumption can be applied to

most thermal systems, the two curves should be identical, except for a multiplication factor of -1.

With the appropriate post-processing of the captured transient data, the time constants of the curve can be identified, and a one-dimensional Cauer RC model of the system can be built containing thermal resistances (Rth) and thermal capacitances (Cth). By plotting the cumulative thermal resistances on the horizontal axis and the cumulative thermal capacitances on the vertical axis, a cumulative structure function is formed. The original work can be found in [13]. This cumulative structure function contains information about the physical structure of the package which helps detect delamination or degradation.

Power cycling solution

A thermal transient measurement system is able to apply stepwise power changes on the device under test and to capture its temperature with high resolution during the cooling and measure its voltage during the heating. If the system repeatedly applies a heating power on the device while letting it cool down between two power pulses, the result is a power cycling. In such a way, the system is not only capable to apply the heating pulses on the device to be tested but also to measure its voltage, temperature, minimum temperature, maximum temperature, temperature swing, and voltage during the heating, and, hence, the applied power step.

During the power cycling, a common practice is to increase the heating power to achieve the same junction temperature change in a shorter time. In such cases, the transient is not captured from one steady state to another, thus the thermal impedance of the system cannot be calculated in each cycle. However, the measurement system is capable of stopping the power cycling after a certain number of cycles to do a full-length thermal transient measurement using a reduced heating power, and hence calculate the actual Rth of the structure.

For the current experiment a market-available discrete SiC MOSFET was selected in a TO-247 style package. Because of the limited throughput of the test setup, only three MOSFET devices were tested in this experiment, but this number is enough to demonstrate the two primary failure modes that can be observed in such tests.

Mechanical setup

For the tests, the selected transistors had to be fixed to a water-cooled, temperature-stabilized cold plate (CP). The back side of the TO-247 packages was connected to the drain of the transistor, hence they had to be insulated from the cold-plate surface. Trial measurement showed that putting an electric insulator sheet between the transistor cooling surface and the cold plate would increase the overall thermal resistance of the structure at an unacceptable rate. The effect of this insulation layer can be significantly reduced by putting a ¼-inch copper block under each transistor package to act as a heat spreader. Consequently, the electric insulation was put between the copper block and the CP as shown in Fig. 1. Because the electrical setup (detailed later) enabled us to use low heating currents, crocodile clips were used for the electrical connections to avoid soldering.

Fig. 1 SiC MOSFET devices mounted on the cold plate.

Electrical setup

Depending on the purpose of the test and the tested electric component (diode, MOFET, IGBT), various different electrical setups can be used to apply the heating power on the devices. For lifetime testing purposes, the requirement is to use an electrical setup that ensures a dissipation distribution and, hence, a thermal load on the chip surface that is as similar as possible to the real application. In other cases when lifetime approximation is not targeted, the powering can be altered to fit better to the actual requirements.

In normal application, the dissipation is generated by the conduction loss and the switching losses. In the current power cycling experiment, the switching losses cannot be used for heating; although, the conduction loss can be used for heating the device. Although a higher load current than in normal application may have to be used to achieve the same heating effect. This puts extra load on the bond wires, especially at the connections to the die surface, hence it is more likely to increase the chance of the bond lift-off or heal crack. Also, the on-state channel resistance has a linear behavior. There is a significant voltage drop on it during the heating period when high current is applied. However, during the cooling, when only a small current can be applied to measure the cooling transient, i.e., the hot and cold temperature, there is a very low voltage drop on the channel resistance, hence the temperature sensitivity is extremely low.

As a result, the channel resistance cannot be efficiently used for accurate temperature measurement. The solution is to use the reverse diode for sensing the temperature by applying a negative measurement current during the cooling. This is a feasible option, but we have to calculate with an elongated electric transient covering the initial section of the cooling, and we lose the accuracy of the peek temperature.

For easier handling, the body diode of the MOSFET is commonly used instead of the transistor. This ensures a good-quality temperature measurement, while the heating and sensing current has the same polarity. The electric transient length can also be much shorter than in the previously discussed case. The drawback of this setup is that it again puts elevated load on the bond wires. However, additional problems arise when the one logical MOSFET switch is being realized by two or more parallel connected chips. In such cases, because of the small differences in the forward voltage of the individual chips, the even current distribution cannot be ensured. This leads to higher dissipation on one of the chips,

and so it will be hotter than the others. And, because the temperature dependence of the forward voltage is typically negative, this will lead to even higher current load. The result can be thermal runaway, which is only blocked by the serial ohmic resistance of the wirings.

Finally, the MOSFET can also be used as a temperature sensor device by connecting the gate to the drain as a two pole. When a small constant current is connected on it, the voltage drop on the device will be equal (slightly above) the threshold voltage, and it will show a quadratic characteristic. This setup is commonly called the "MOS Diode" or "Threshold Diode" setup. The schematic of the setup is shown in Fig. 2.

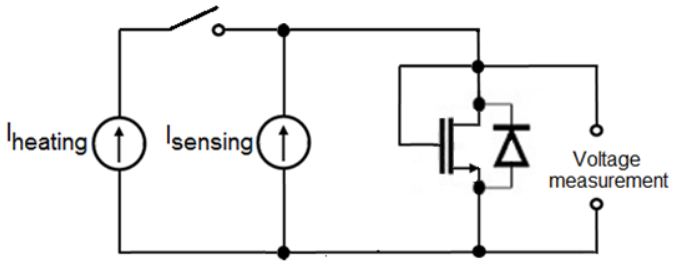

Fig. 2 Schematic of "MOS Diode" setup.

The threshold voltage has high temperature dependence in this mode, and hence it enables high accuracy temperature measurement. Also, because of the high voltage drop, the same power dissipation can be achieved using much lower heating currents. This put a lower load on the bond wires, which enables us to focus on the degradation of other layers, like the die-attach. The drawback of this setup is similar to that of the reverse diode; in the case of parallel connected chips, the even current distribution cannot be ensured.

In our tests, we had no parallel chips in the package, thus we selected the latter electric setup because of the high resolution and easy handling. Additionally compound semiconductor components tend to show special slow electric transients that can alter the thermal transient results, but we did not experience this for the selected component.

Control strategy

Using the above discussed parameters, electrical setup, heating time, and applied heating power, the desired temperature change can be selected, but this is true only at the beginning of the cycling experiment. During the lifetime test, the properties of the system, the thermal resistance, the voltage drop, etc. are expected to change, and hence the temperature change will also change. Previous studies show that temperature change has a significant effect on the power cycling lifetime and how to control the parameters during the test procedure [14]. We can define different control strategies, constant current, constant power, and constant junction temperature.

The cycle time in our experimental system was fixed after the initial setup. This cannot be changed during the cycling. The most straightforward and realistic control strategy is to use constant heating current. In a real application, it cannot be expected to apply a lower load on a module just because it is aging. If the thermal resistance increases, the temperature change will go up. If the voltage drop on the device increases because of the degradation of the bond wires, for example, the heating power will increase. These effects mean positive feedback during the cycling and increasing the load with the aging of the device; thus, powering with constant current is the most severe powering strategy.

The dissipated power also can be kept constant by slightly adjusting the heating current level. This significantly reduces the positive feedback caused by the changing electrical properties and leads to a longer measured lifetime. However, this strategy will provide measurement results that are comparable to lifetime simulations where the electrical changes cannot be handled effectively.

The temperature change can also be kept constant by the current regulation. As a result, neither the electrical changes nor the increase of the thermal resistance will affect the applied load. Although the cycles to failure will have limited connection to the real application lifetime when using this method, it can be used to perfectly control the temperature load to investigate certain failure modes.

In the current experiment, two out of the three devices were cycled using constant heating current; but for the third one, constant junction temperature change was selected. The parameters of the cycling are summarized in Table 1. The parameters maintained constant by the control strategy are marked with bold letters.

Table 1. Power cycling parameters.

Test channel	Ch1	Ch2	Ch3
Temperature sensitivity [mV/K]	-9.4	-9.4	-10.3
Ambient condition (liquid-cooled cold plate) [°C]	25	25	25
Cycling current [A]	**24**	**24**	22
Cycle on/off time [s]	10/10	10/10	10/10
Temperature swing [°C]	92.5	91	**100**
Control strategy	Constant current	Constant current	Constant ΔT
Thermal transient measurement frequency	once every 1,000 cycles		

RESULTS AND DISCUSSION

The first and most obvious result that is worth taking a look at is the number of cycles until the device fails (see Table 2). According to the cycling strategy, we would expect the device connected on ch3 to last longer than the other devices.

Table 2. Power cycling parameters.

Test channel	Ch1	Ch2	Ch3
Average temperature swing [°C]	92.5	92	100
Nf [-] (power cycles until device failure)	11992	9855	3612

Clearly, this did not happen. We unfortunately cannot draw reasonable conclusions on the effect of the power cycling strategy. However, we should take a deeper look into what happened to the device and what caused it to fail earlier. If we compare each channel's average temperature swing, we can see a significant difference between ch3 and the other two channels.

For more details, we have to take a look at the junction temperature swing versus applied power cycles graph (see Fig. 4). On channel 3, the regulation algorithm ensured a constant 100 °C temperature change in all cycles (except some disturbances after the full-length thermal transient measurements), but for the other two channels, temperature changes were visible. On one hand, the temperature decreased initially because of the thermal interface material between the package surface and the copper heat spreader block. This decrease was proved by the structure functions.

In the very first cycle, the temperature change was close to 96 °C on both ch1 and ch2. The higher temperature change means higher thermal stress which leads to shorter lifetime, but the ~8 °C difference in average temperature seems to be too small for such a significant difference.

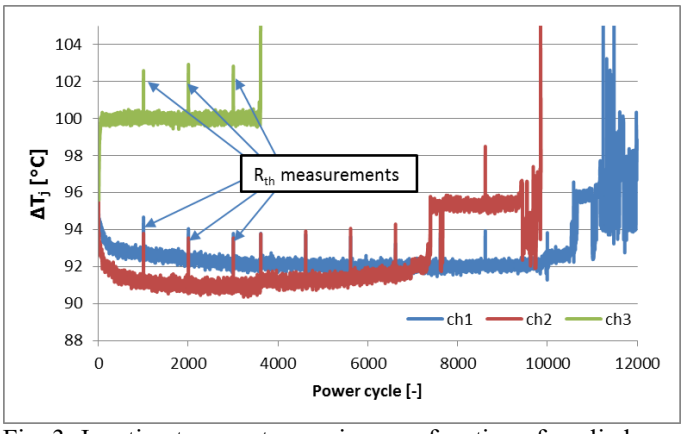

Fig. 3 Junction temperature swing as a function of applied power cycles.

However, stepwise changes occurred in the temperature swing at ~7,500 cycles on ch2 and at ~10,500 cycles on ch1. Such stepwise changes could not be seen on ch3 because the regulation algorithm compensated for the effect of electrical changes. The cause of the stepwise changes can be more clearly investigated on the changes of the devices voltage at high current as the function of power cycles (shown in Fig. 4). Here, stepwise changes in the forward voltage happened not only in the case of ch1 and ch2, but on ch3 also, but much earlier.

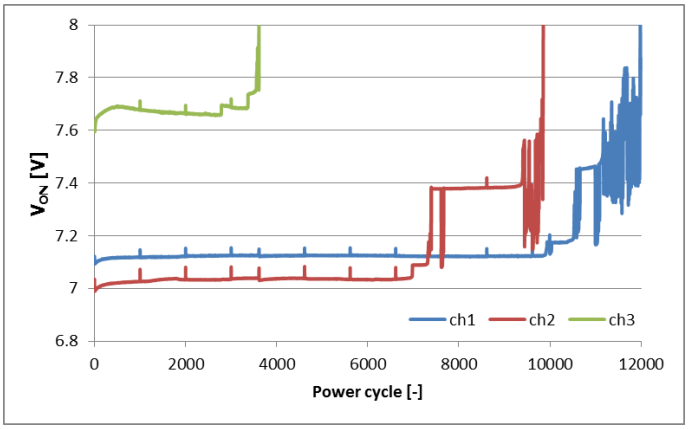

Fig. 4 Voltage drop on the device at heating current level as a function of applied power cycles.

Previous publications have shown that, in the case of devices heated in open state, the gradual change in the device voltage is caused by the degradation of the device characteristic and the crack propagation in the bond wires, whereas the quick changes are the increase of the serial ohmic resistance do to the lift-off or breakage of the individual bond wires [15]. In the case of the current electric setup (Fig. 2), the voltage drop we measured was nearly the gate voltage needed to achieve a channel resistance so that the gate-to-source voltage equaled the drain to source voltage.

$$V_{GS} = V_{DS} = IR_{DS} \quad (1)$$

The V_{DS} voltage measured at the transistor was equal to the load current (I) multiplied by the drain to source resistance (RDS), which is ideally equal to the channel resistance of the MOSFET. However, in the current case, we had to take into account the serial resistance of the wiring between the transistor and the pin connections:

$$R_{DS} = R_{ch} + R_s;\ \ R_s = R_{leads} + R_{bond} \quad (2)$$

When the equivalent resistance of the bond wires increases, the serial resistance of the package and the transistor voltage will also increase. The actual value of the voltage change cannot be expressed in closed form.

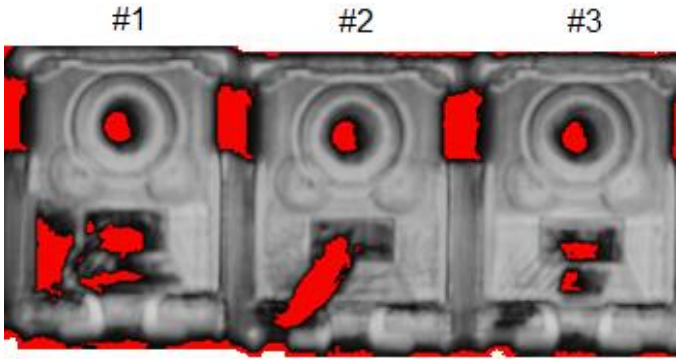

Fig. 5 SAM image highlighting the air gaps around the bond wires with red.

The devices were also checked using scanning acoustic microscopy (SAM) to verify the results found based on the electrical measurements. Fig. 5 shows the SAM picture of the three devices. The red color represents voids. Clearly, voids were formed in the area of the bond wires especially close to

the chip connection. Unfortunately, we had no chance to do a reference SAM measurement before the power cycling test, thus, the captured pictures cannot be compared to the original state. However, intact samples were also tested using the same settings, and no such air gap was visible around the bond wires. All of these tests verified that there was bond wire degradation for all the three devices.

The first steps are smaller because the overall resistance of the parallel bond wires changes only slightly, caused by the breakage of only one of them. But, as the number of bonds decrease, the relative change in the resistance becomes much higher, and the step size increases. Not all of the bond failures can be distinguished as at the end. The high overload destroys the last bonds soon after the others.

Structure functions

During the power cycling experiment, the measurement system enabled us to do regular full-length thermal transient measurements. As the degradation process is generally expected to be relatively low, we selected the measurement interval to be one after every 1,000 cycles.

Obviously, the thermal transient measurement gives the thermal resistance of the structure from junction to the ambient (that is currently the stabilized temperature cooling water), which includes the resistance of the chip, package, thermal interfaces, and other external features. However, as it was already described above, with appropriate post-processing, an equivalent one-dimensional distributed RC model can be identified that describes the partial resistances of the structural elements and contains structural information about the device [13].

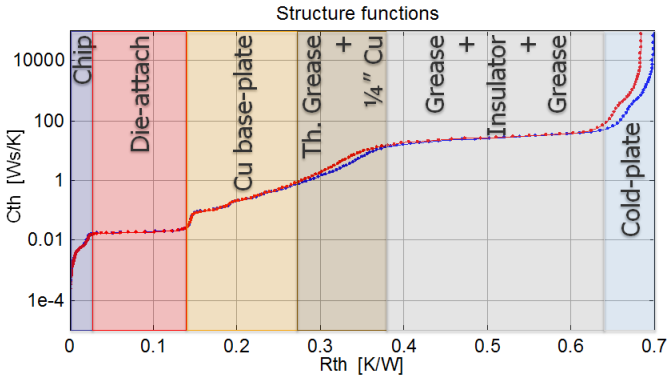

Fig. 6 Structure function of samples on ch1 and ch3, with the structural layers identified.

For interpretation, the resulting RC model is commonly plotted on a so-called "structure function" (SF), in which the thermal capacitance of the structure is plotted as the function of thermal resistance in an integral form. The dissipating point is always the origin of the plot, and the ambient is the infinite thermal capacitance represented by a singularity at the end of the curves. Between these two extremes, the structure of the system can be identified as the heat flows from the chip through the intermediate layers to the cold plate.

The structure function that correspond to the initial state of samples on ch1 (red) and ch3 (blue) is plotted in Fig. 6, where the different layers of the structure are identified and marked with different colors. The structural layers can be separated based on the changes of the slope of the curve and identified if the structure of the device under test is already known.

Where there is a steep section on the structure function, it means that the layer has a relatively large capacitance compared to its thermal resistance, and so it is a good conductor material like the semiconductor or the copper heat spreader. Opposite to that, the interface layers with relatively low thermal capacitance but higher resistance are represented by flat sections.

The two curves fit perfectly because the two samples are close to identical, but a difference can be seen above ~0.28 K/W. This difference is typically caused by the difference in the environment, the different coverage, and thickness of the thermal paste under the package. Hence, we can read the resistance until this point as the junction-to-case thermal resistance. This value shows good match with the value provided in the datasheet.

Now, as we understand the structure function of the samples, we can take a look at the diagrams and see how it changes with the applied power cycles. In Fig. 7, the structure functions captured on ch1 are visible after every 1,000 cycles. The initial state of the structure was also captured before the cycling started in the image, represented by blue color. This curve is slightly different than all the others captured after 1,000, 2,000, etc. cycles.

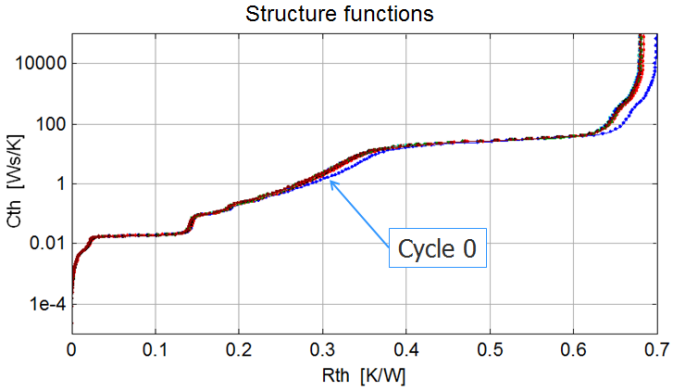

Fig. 7 Structure function of ch1 in the initial state (blue) and after every 1,000 cycles (red, black, etc.).

This initial decrease of the thermal resistance was already visible on the temperature-change diagram in Fig. 3. Now we cannot only see the effect, but we can identify the cause of the change. These curves also fit until about 2.8 K/W, and any difference can only be seen after this resistance. This proves that there was no structural change in the investigated package, but the change was caused by the spreading and thinning of the thermal interface material layer.

After the initial improvement of the thermal resistance, no further change is visible. The failure of the device was caused by degradation of the bond wire only and not because of the structural changes. This could also be verified by the SAM images, which showed no crack or delamination. The same effect could be seen in the structure functions corresponding to ch2.

More interesting results can be seen on ch3. In Fig. 8, the structure functions of ch3 are plotted after every 1,000 cycles (the post processing tool starts channel numbering with ch0, this causes the difference in the figure legend).

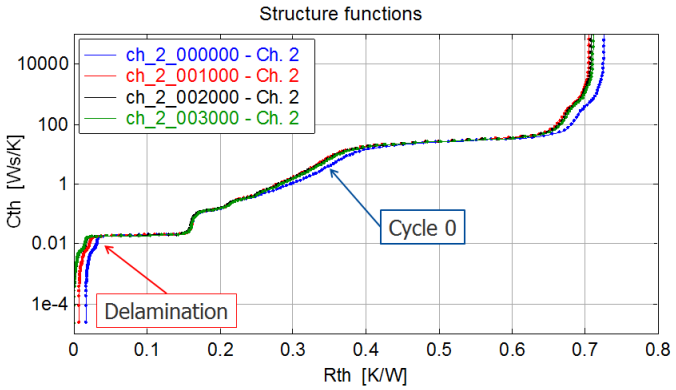

Fig. 8 Structure function of ch2 in the initial state (blue) and after every one thousand cycles (red, black, etc.).

The curves were moved from their original position, and they were fitted at the capacitance step of the copper baseplate of the TO-247 package. This modification in the original positions allowed us to separate the two effects that are visible on the plot.

First, we have to observe a similar reduction in the thermal resistance at the right side of the curve after the fitted section, caused by the spreading of the thermal interface material under the package. But we also see difference in the left side of the fitted section. A continuous increase in the length of the flat section around 0.1 K/W can be seen. This flat section represents the resistance of the die-attach layer, and the elongation of it shows a growing delamination in this layer.

In Fig. 9, the SAM image of the transistor connected to ch3 is visible, focused at the die-attach layer. A dark shade is visible under the chip (circled with red) that was not visible on the other samples. We can assume this is the same delamination that we observed on the structure functions.

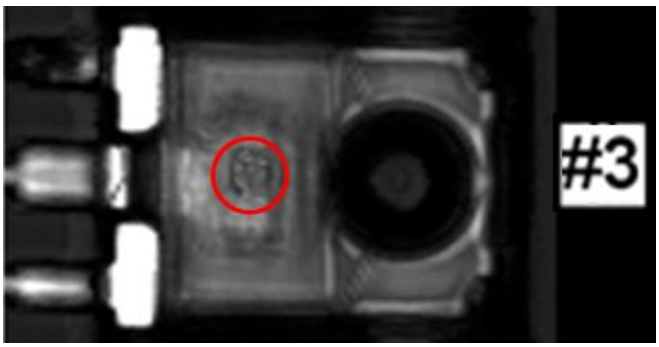

Fig. 9 SAM image of the die-attach layer of sample on ch3.

According to a discussion with the manufacturer, the cause of the early failure could have originated from the bending of the leads of this transistor or heated too long during soldering the pins, which elevated initial stress in the structure and led to the early damage of the die-attach layer.

CONCLUSIONS

In this paper, we presented the results of a power cycling experiment on SiC MOSFET devices. We found that the same power cycling arrangement based on the thermal transient measurement system is capable of doing power cycling not only on Si, but SiC-based devices as well. In the current experiment, we could apply the conventional electrical setups used for Si MOSFETs; but for more exotic components, it would be enough to find the appropriate electrical setup to enable the thermal transient measurement, which also could be used for power cycling. Although we selected a different method for heating the device than on the open channel, we were able to see the degradation and the breakage of the bond wires by monitoring the voltage drop on the device at high current load. The difference between the different control strategies could not be investigated because of the early failure of one device; but using the structure functions, we could clearly identify the root cause of the failures was due to degradation of the die-attach. The findings based on the structure functions were cross-checked using scanning acoustic microscopy. The two different investigation methods verified each other's results.

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