Model for Power Cycling lifetime of IGBT Modules – various factors influencing lifetime

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Abstract

A large number of power cycling data from different IGBT module generations and test conditions have been evaluated. Multiple regression with respect to the variables temperature swing ΔT_J, T_J, power-on-time (t_{on}), chip thickness, bonding technology, diameter (D) of bonding wire, current per wire bond (I) and package type was performed. It provided parameters for a new empirical model describing number of power cycles (N_f) in relation to these variables. For a fixed module technology and blocking voltage class, the set of variables have been restricted to ΔT_J, T_J, t_{on} and I as the factors influencing the number of cycles to failure. The model is used to estimate the power cycling capability for the new generation of 1200V-IGBT4 Modules, which are rated up to a junction temperature of 150°C in operation.

1 Introduction

Power cycling capability of power semiconductor modules is mostly modeled by a Coffin-Manson law, i.e. number of cycles to failure (N_f) is assumed to be proportional to $\Delta T_J^{-\alpha}$ [1], [2], [4] (ΔT_J stands for swing of junction temperature per power cycle, α is a constant). It appears as a straight line when plotting $\log(N_f)$ over $\log(\Delta T_J)$. More detailed models consider the dependence on absolute junction temperature (T_J), in addition [3], [5]. An Arrhenius factor is added to the Coffin-Manson law. From models for solder fatigue the impact of dwell time, ramp time or cycle time are also known as factors influencing the life time. But such models are rather established for passive thermal cycling tests and not for power cycling tests.

Due to progress in IGBT module technology, the number of power cycles to failure (N_f) increased by a large factor. Thus solder fatigue became a factor competing with wire bond lift off as failure mechanism [6]. Therefore an impact of cycle time on N_f can be expected, for example.

These considerations and the analysis of results from numerous different power cycling tests led to a revision of the life time model. Further factors influencing lifetime have been considered.

2 Power Cycling data

2.1 Test conditions

During power cycling tests conduction losses are turned on and off in the devices under test. The current has either rectangular or 100Hz ½-sine shape. Its amplitude is mostly chosen to be at rated current or higher. The Off-time is usually greater than or equal to the On-time. Junction temperature is measured through V_{CE} [7], [8] at a low sense current, before and after each On-pulse. The heat sink temperatures can be adjusted by cooling means to control the intended absolute base temperature, i.e. the starting temperature of Figure 5. Further details on conditions are given below.

2.2 Data analysis

A large number of power cycling data from different module technologies, which have been gathered over years at various conditions are analyzed in detail. When plotting this data over the different test variables, trends show up. They indicate impact of ΔT_J, T_J, power-on-time, blocking voltage of the Chip (V), bonding technology, diameter (D) of the bonding wire, current per wire (I) and package type. As the power-on-time, off-time and total cycle are correlated power-on-time is chosen to represent the impact of time. The blocking voltage of the chips under consideration is related to chip thickness. Therefore blocking voltage (V) can be chosen to be the place holder for thickness. The influence of current influencing N_f was picked to be the current per each bond foot attached to the chip surface. Total current in a power cycling test is therefore divided by the number of paralleled chips in a module, number of wires per chip and number of bonds per wire to gain the current under consideration.

The data shown in Figure 1 cover a wide range of ΔT_J (45K…150K), and a wide range of maximum junction temperatures T_J (80°C….205°C). Diameters of

bonding wires range from 75µm to 500µm and currents per wire bond (I) from 3A to 23A. IGBT and Diode chips with blocking voltages from 600V to 3300V, 7 bonding technologies and 7 different packages are represented.

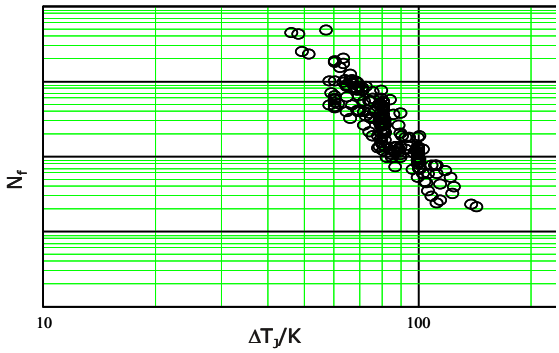

Figure 1: Power cycling test data (N_f) for different module generations and test conditions; variables are ΔT_J, T_J, blocking voltage of the Chip, bonding technology, diameter of the bonding wire, current per wire bond and package type

Figure 1 confirms a major contribution of a Coffin-Manson law, as commonly known. On the other hand, the spread of data indicates impact of other factors. Figure 2 represents the data plotted over reciprocal maximum junction temperature, which is reached during each test cycle. This plot indicates a more or less linear relation, which allows implementing the Arrhenius law, again. The spread of data in Figure 2 is larger than in Figure 1 as the dominating factor ΔT_J is varying for each T_J causing large difference in N_f.

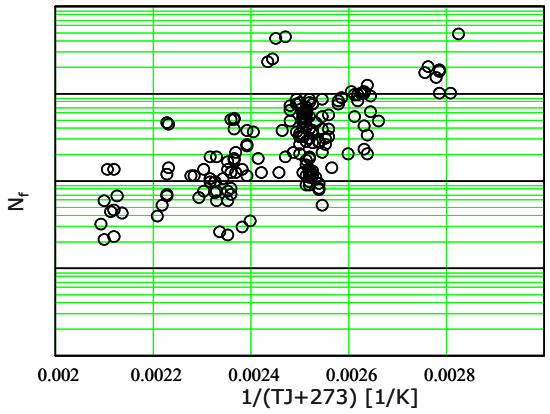

Figure 2: Data as in Fig. 1 plotted over $1/(T_J+273K)$ to check for an Arrhenius law.

Two further factors influencing the lifetime under power cycling are shown in Figures 3 and 4. These 2 factors are power-on-time and current per wire bond on the chip. As the ΔT_J and T_J are the dominating factors the spread of data in Figures 3, 4 is even larger. Nevertheless the impact of time shows up and cannot be neglected. Figure 4 may cause doubts about an impact of current. The reason is the largest spread of data caused by the other factors. Correction of the raw data with respect to ΔT_J, T_J and other factors pronounces the impact of current (Figure 10). The impact of wire diameter and blocking voltage was identified in a similar procedure.

Different bonding technologies represent categorical influences. Understanding their impact on power cycling lifetime allows transforming data from different technologies into one. Data of Figure 1 to Figure 4 contain this transformation, already.

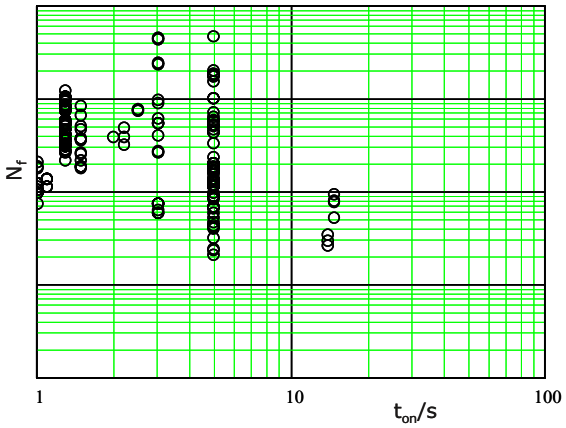

Figure 3: Data as in Fig. 1, 2 but plotted over power-on-time (t_{on}) to indicate influence of time

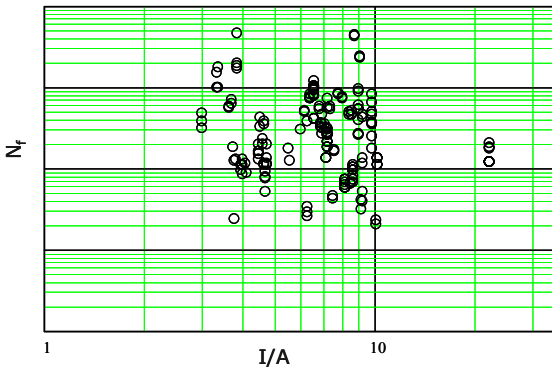

Figure 4: Data as in Fig. 1,2,3 but plotted over current per wire bond and the chip (I) to indicate influence of current

3 Lifetime model

3.1 Approach

Following existing formulas as from [3] empirical findings like in Figures 1-4 are used to extend the formula of [3]. The number of cycles to failure (N_f) are described by

$$N_f := K \cdot \Delta T_J^{\beta_1} \cdot e^{\frac{\beta_2}{T_J + 273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \quad \textbf{(1)}$$

The impact of ton, I, V, D are all represented by individual power laws where β_3 to β_6 are assumed to be negative. These power laws assume proportionality of $\log(N_f)$ to $\log(t_{on})$, $\log(I)$, $\log(V)$ and $\log(D)$. Exponential relations could also be used. Spread of data as in Figure 3 and Figure 4 does not allow establishing more than linear relations. As this is an empirical approach the formula is limited to the test data range and can not be used for extrapolation.

Despite the empirical approach physical reasons for attached factors (1) can be estimated:

The time dependence (t_{on}) can be caused by the transient thermal response of the temperature profile on the chip. For short times (=1s) lateral gradients in T_J can not develop as high as for longer times. The T_J measurement through V_{CE} therefore differs then for different times. Thermo-mechanical deformation and relaxation at interconnects can also cause the impact of time, i.e. pulse width.

The impact of current might be guessed to be caused by electro-migration. Detailed physical analysis (not reported here) of many power cycling tests has proven that electro-migration does not take place [9]. The current is rather accelerating the failure of wire bonds close to end of life by additional heating at the chip to bond interface.

The blocking voltage is correlated to chip thickness, which is assumed to be the reason for this influencing factor. 600V IGBT and diode chips are as thin as 70µm. In a module setup these thin Si layers follow the thermal expansion of wires, solders and substrates, to some extend. Thus the difference in thermal expansion is reduced for thin chips and more completely active for thick chips, i.e. high voltage chips.

Remark: This relation to chip thickness does not apply to modules for traction applications, as the module setup and bonding technology differs again for traction modules [4].

Larger wire diameter results in a larger bond interfaces on the chip, i.e. greater difference in thermal expansion. Some significance is seen by this factor when very thin wires like 75µm wires are used. Unfortunately such thin wires are not able to handle typical currents of today's IGBT and diodes. A range between 300µm and 500µm - normally used, is rather minor but can not be neglected here.

For a fixed voltage class and module technology the last two influencing factors (V, D) in (1) become constants and can be integrated into the constant K, resulting in a simplified formula (2), which depends on test conditions, only.

$$N_f := K \cdot \Delta T_J^{\beta_1} \cdot e^{\frac{\beta_2}{T_J + 273}} \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \quad \textbf{(2)}$$

3.2 Multiple linear regression

The parameters K, β_1 to β_6 in (1) are to be adjusted for best match of model and test data.

Equation (1) or (2) can be transferred into a function, which is linear in the parameters β_i by taking the logarithm of the whole equation. It results in

$$\ln(N_f) := \ln(K) + \beta_1 \cdot \ln(\Delta T_J) + \frac{\beta_2}{T_J + 273} + \beta_3 \cdot \ln(t_{on}) + \beta_4 \cdot \ln(I) + \beta_5 \cdot \ln(V) + \beta_6 \cdot \ln(D) \quad \textbf{(3)}$$

The raw data have to be transformed according to (3) and a least squares fit with 6 variables can than be performed. It means minimizing the sum of squared differences between data and model

$$\sum_k \left[\left(N_f(K, \beta_1, \beta_2, \beta_3, \beta_4, \beta_5, \beta_6)_k - \ln(N_{Test\ k}) \right)^2 \right] = \text{Min} \quad \textbf{(4)}$$

(Index k represents the index for the individual test data and conditions, N_{Test} represent the number of cycles to failure in the test, $N_f(K,\beta_i)$ represent the cycles calculated by the model), i.e. the derivatives by the different parameters K, β_1 have to become zero, simultaneously. The computation is done in MATHCAD using the "Solve block".

The solution leads to a set of β_i, (5) which can be used in eq. (1) or (2). Confidence intervals for β_i are shown as $\Delta\beta_i$.

$$\beta = \begin{pmatrix} -3.483 \\ 1.917 \times 10^3 \\ -0.438 \\ -0.717 \\ -0.751 \\ -0.564 \end{pmatrix} \quad +/- \quad \Delta\beta = \begin{pmatrix} 0.263 \\ 413.137 \\ 0.101 \\ 0.24 \\ 0.176 \\ 0.496 \end{pmatrix} \quad (5)$$

3.3 Assumption of normal distribution

A precondition for the successful least square regression is the distribution of data to be normal. This is not expected for lifetime data. It is well known that such data follow a Weibull distribution, normally. The simple least square regression was still used, but when the fit was completed the residuals have been checked for normal distribution, which turned out to be the

case. As reason the mixture of different failure mechanisms, and test inaccuracies can be considered.

3.4 Correlation of variables

Another precondition for the model building is the independence of variables used in the model. The variables in the model (2) are test conditions, which are correlated by the nature of a power system and a module setup.

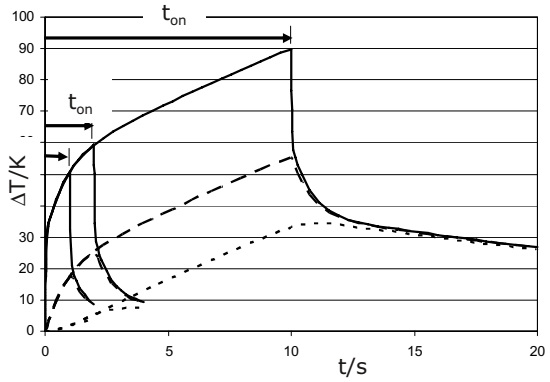

Figure 5: Temperature profile of a typical IGBT module for different pulse width during power cycling. Upper, solid traces represent junction temperature rise (T_J/°C), middle, dashed traces (T_C/°C) represent case temperature rise and lower, dotted traces represent heat sink temperature rise (T_S/°C). The responses for one cycle and 3 different pulse widths are shown.

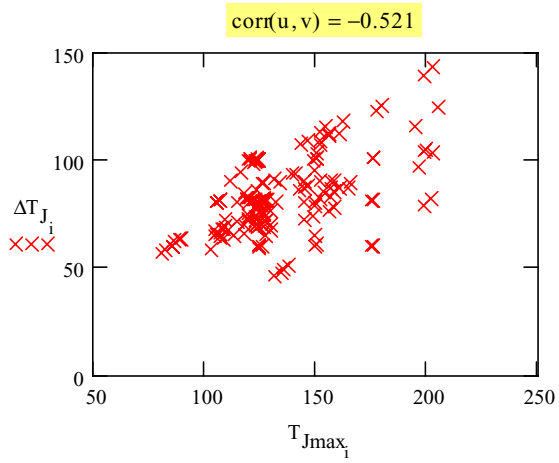

Figure 6: Example of correlation among variables. ΔT_J, $T_{J,max}$

According to this nature and considering the power profiles in the test (Figure 1) higher junction temperatures can be achieved by longer pulse width (Figure 6), higher ΔT_J leads to higher maximum T_J. Furthermore, higher current leads to higher power dissipated in the chip and due to the thermal impedance of the setup, it correlates to higher ΔT_J etc. The precondition of independent variables can therefore hardly be fulfilled One example of such correlations is shown in Figure 6 for ΔT_J, $T_{J,max}$ combinations within the selected data are scattered in a triangle (Figure 6), which results in a correlation factor > 0.5, which is rather high. Due to these kinds of correlations, certain tests had been selected to narrow the range of reasonable fit parameters. However, some uncertainties in the results persist, caused by the interdependence of variable. Therefore, the use of the model has to be restricted to the range where tests have been performed. Finally one correlation, i.e. between ΔT_J and $T_{J,max}$ could be resolved (Figure 7) by using the minimum i.e. starting junction temperature ($T_{J,min}$) to describe the effect of absolute junction temperature. As $T_{J,max}=T_{J,min}+\Delta T_J$ the variable $T_{J,min}$ in the model function can always be transformed into $T_{J,max}$ and thus N_f be expressed in both variables, alternatively. But both ways of least square regression lead to different curves. The use of $T_{J,min}$ as variable in the model increases the negative exponent in the Coffin-Manson portion and lowers the parameter in the Arrhenius term (6).

$$\beta = \begin{pmatrix} -4.416 \\ 1.285\times 10^{3} \\ -0.463 \\ -0.716 \\ -0.761 \\ -0.5 \end{pmatrix} \quad +/- \quad \Delta\beta = \begin{pmatrix} 0.281 \\ 269.197 \\ 0.099 \\ 0.238 \\ 0.175 \\ 0.496 \end{pmatrix} \qquad (6)$$

It therefore leads to a more curved shape of the model function in the N_f-ΔT_J-plot (Figure 8).

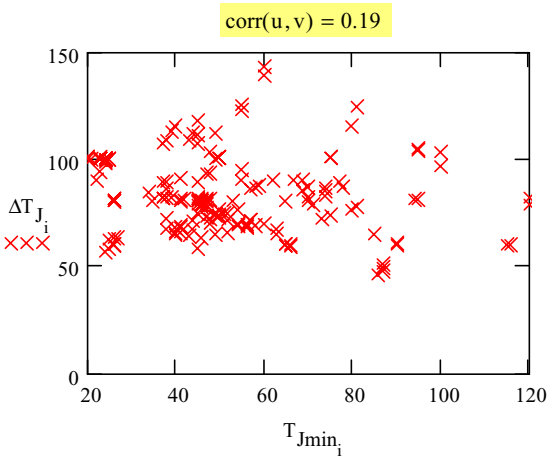

Figure 7: Correlation among variables, i.e. ΔT_J/K, T_J/°C eliminated, when using $T_{J,min}$ instead of $T_{J,max}$

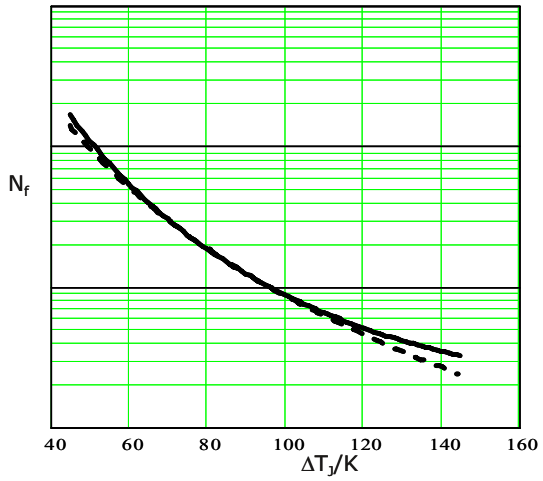

Figure 8: Least square fit of N_f according to eq. (1) with $T_{J,max}$ representing the influence of absolute junction temperature (dashed line) and with $T_{J,min}$ representing influence (solid line). For dashed line 1st set of β_i and for solid line 2nd set of $ß_i$ apply.

3.5 Result

The grade of agreement of test data and modeled data is illustrated in Figure 9. Considering natural spread of degradation processes and test accuracies of these tests the agreement can be accepted. Using the model data of Figure 4 can be transformed to a figure with fixed ΔT_J, T_J, t_{on}, V, D. The result is represented by

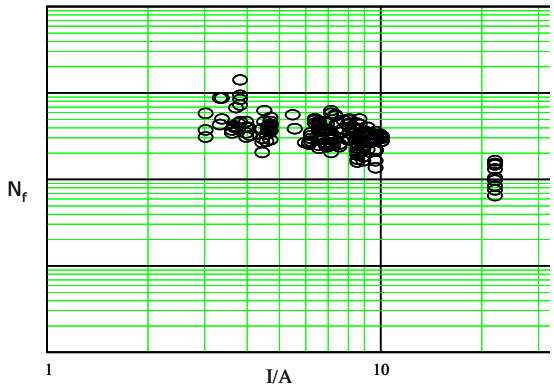

Figure 10: Better confirming the current to be an influencing factor.

Common statistical tests and criteria have successfully been used to verify the model. A comparison of the advanced module technology with former stages is given in Figure 11. For T_{Jmax}=125°C the curve above an approximate ΔT_J of 100K is extrapolated with respect to $T_{J,max}$, realized in the test. For T_{Jmax}=150°C the curve above an approximate ΔT_J of 125K is extrapolated with respect to $T_{J,max}$, realized in the test. This is a consequence of the correlation of conditions. The modeled curves are centered within the test data. When a longer pulse width (t_{on}) is considered, fatigue

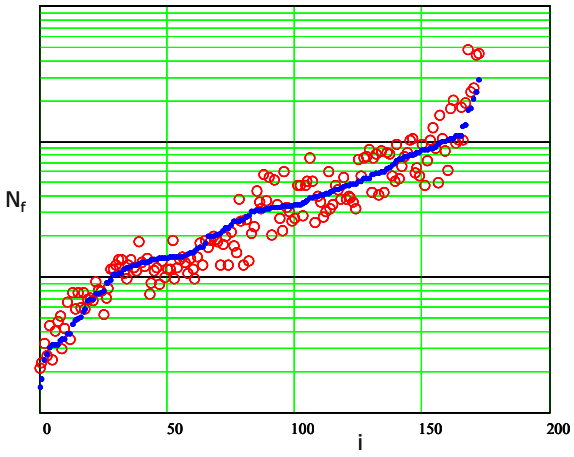

Figure 9: N_f test data (circles) and modelled N_f data (dots) plotted over Index of data in descending order of modelled N_f.

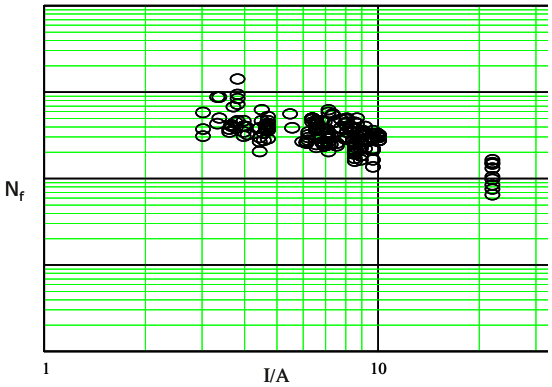

Figure 10: Data of Figure 4 now corrected with respect to ΔT_J, T_J, t_{on}, V, D by application of the model

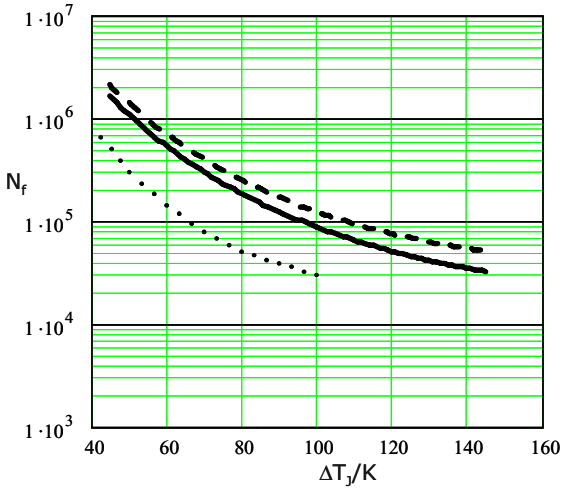

Figure 11: N_f-ΔT_J; former curve of modules for industrial application at $T_{J,max}$ of 125°C (lower, doted trace); Estimated N_f according to new model for Modules with IGBT4/1200V at $T_{J,max}$ of 150°C, ton=1.5s, I=10A (solid line); dashed line - same as solid line but $T_{J,max}$ of 125°C

of substrate to base plate solder limits the reliability above ΔT_J of about 100K. The model does not cover this lifetime.

Choosing low current values may result in extremely high N_f for devices with low blocking voltages, according to the model. In this case, fatigue of chip solder has to be considered as the limiting factor of reliability. The model becomes inaccurate in this area. Chip solder fatigue can roughly be considered to become limiting at the dashed curve, i.e. top curve of Figure 11.

4 Conclusion

Implementation of power-on-time and current into the model for reliability of advanced IGBT modules leads to a better description of number of cycles to failure. The method is used to establish the N_f relation for 1200V-IGBT4 modules. Some remaining correlation of variables used in the model restricts the model to ranges of test conditions of selected data. Therefore, authors strongly recommend not applying the model without consulting experts at Infineon Technologies. Special effort in the test apparatuses is needed to fill the white spots of variable combinations and to improve the model, further.

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