Reliability Challenges for Power Devices under Active Cycling

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***Abstract*— Power stages are subject to severe stress due to active cycling, resulting in e.g. fast thermal cycling. While some applications require several hundred millions of cycles under normal operation conditions, "disturbances" such as short circuit pose additional challenges. These issues are neither addressed by "classical" silicon wafer technology qualification nor by standard product qualification procedures. Challenges and limitations in applying the principles of Robustness Validation to these issues are discussed.**

Keywords: Reliability; power devices; active cycling; qualification

I. INTRODUCTION

Power devices have pervaded the market and found wide ranges of application. From the light-weight battery charger of your mobile phone to real heavy, multi-chip, high voltage power modules in traction, power devices are used either as discrete components or integrated together with CMOS and bipolar devices in so called Smart Power technologies. Voltages range from a few tens of volts to kilovolts, currents from a few to hundreds of amperes. The performance requirements, i.e. high isolation voltages, high gate voltages, high currents, imply that power device technologies have not followed the standard roadmap of CMOS, but rather have followed a separate line of development.

This paper will consider DMOS (double-diffused MOS) transistors; it will not discuss specifically IGBTs or other types of power devices, although some of the considerations presented in this paper can be applied to these kinds of devices in an analogous manner. DMOS transistors come as different variants: Vertical DMOS (VDMOS) transistors make up the major part of discrete devices and are also used in integrated technologies, while lateral devices (LDMOS) are used in many integrated technologies, because they can be integrated into a CMOS process flow more easily. Besides that, technologies have also seen a transition from planar to trench devices in recent years, resulting in further shrinkage of the devices, while, obviously, at the same time increasing the power density. The general trend of power density increase has led to technologies being driven to the limits of their capabilities. The very nature of power devices means that they have to withstand not only high voltages and currents, but also, due to the power dissipation, high temperatures. The active cycling of the power devices, i.e. their being exposed to current/voltage pulse conditions, causes specific failure mechanisms and necessitates specific reliability consideration, some of which will be discussed in the present paper.

II. REQUIREMENTS

Reliability is not an inherent property of a device, but related to a function that has to be fulfilled under certain conditions for a specified time. These conditions comprise what is termed a mission profile [1, 2]. The mission profile constitutes a set of requirements the product can experience in its life cycle. The requirements of the applications comprise, among others, the total lifetime (e.g. 15 years) and power-on time (e.g. approximately 10000h for automotive applications), temperature profiles, (passive) temperature cycling requirements, and supply voltages. Additionally, the power device is actively cycled, i.e. it is exposed to several kinds of voltage and current pulses that arise either due to its intended operation or "disturbances". These pulse conditions are critical for the reliability of the device and may vary widely depending on the kind of application and load. Table I shows an example of requirements for motor management in automotive applications. Different kinds of pulses are defined: an operating mode that corresponds to the regular driving of valves when the engine is running, and two further modes that correspond to special operating conditions that can occur during the lifetime of the car. The latter two do not constitute "failures" of the system. The last one, load dump, carries a very high energy, but with only a low number of events specified.

TABLE I. EXAMPLE OF REQUIREMENTS FOR DIFFERENT KINDS OF PULSES FOR A SMART POWER DEVICE IN AUTOMOTIVE MOTOR MANAGEMENT. NUMBERS GIVE ORDER OF MAGNITUDE.

Mode	Pulse Parameters	
	Max. Energy	*Number of Pulses*
Operating Mode	15 mJ	$500*10^6$
Jump Start	50 mJ	$10*10^3$
Load Dump	100 mJ	5

In this case the load is an inductance. Switching of inductive loads is especially challenging due to overvoltages that occur. Integrated devices typically use a clamping diode to prevent the device from going into an avalanche breakdown condition. Discrete power transistors may be subject to

unclamped inductive switching (UIS), which can result in the device entering an avalanche breakdown condition. During each of such switching events, the device experiences a simultaneous high voltage and high current condition, resulting in high power dissipation and corresponding heating of the device, as illustrated in Fig. 1.

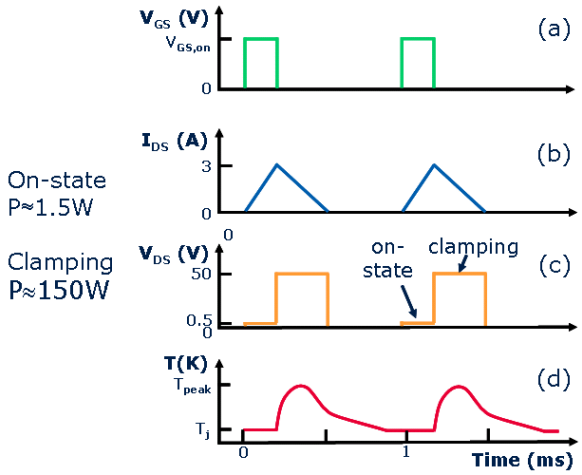

Figure 1. Illustration of time dependence of gate voltage (a), drain current (b), drain voltage (c), and temperature (d). Power dissipation during clamping is two orders of magnitude higher than in the on-state.

In addition to these requirements, there are requirements regarding short circuit behavior and electrostatic discharge (ESD). Short circuit represents a very severe condition that can lead to very high temperature excursions on the device, depending on the implemented protection strategy.

III. Failure Mechanisms and Modes

The safe operating area (SOA) of a power device gives the allowed operating area in terms of voltage and current subject to additional boundary conditions, e.g. temperature or frequency. Different kinds of SOA have been defined corresponding to different failure mechanism [3]. Triggering of the intrinsic bipolar transistor of the DMOS by either fast electrical pulses or excessive temperatures leads to destruction of the DMOS. These events are characterized by an electrical SOA or a thermal SOA, respectively [3, 4]. Single pulses exceeding the SOA may lead to destruction of the device by what is usually termed as electrical overstress (EOS).

Devices such as LDMOS transistors that have currents and high fields at or near to the silicon surface are especially prone to hot carrier effects. This effect has received much interest in recent years [5].

Because high temperatures also increase the effect of high gate bias on the stability of device parameters, commonly termed as bias temperature instabilities (BTI), this failure mechanism has been the subject of several investigations, although gate oxides are significantly thicker for power devices as for standard CMOS [6, 7].

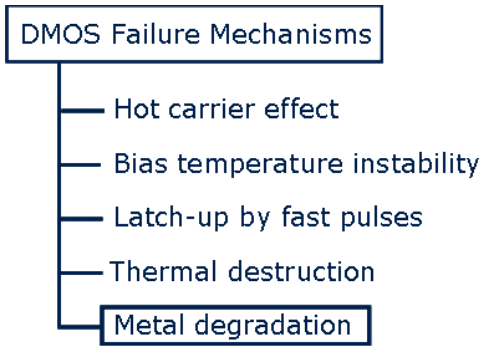

Figure 2. Failure mechanisms of DMOS transistors.

These DMOS failure mechanisms have been listed in Fig. 2. In this paper, we will concentrate on a different effect, namely the electro-thermo-mechanical stress that is exerted on the devices due to the active cycling. The temperature rise ΔT caused by the power dissipation is usually calculated using the thermal resistance R_{th} and the power P:

$$\Delta T = R_{th} P. \quad (1)$$

Under dynamic conditions the static thermal resistance R_{th} is substituted by the dynamic resistance Z_{th}.

A look at relevant time scales, as illustrated in Fig. 3, leads to the conclusion that there are conditions, for which a calculation using (1) is not adequate. The typical behavior is schematically illustrated in Fig. 1d, showing a time-dependent temperature rise over the junction temperature T_j. The time scales of the pulses fall into the same range as time scales relevant to the chip and/or the package. Therefore, the full dynamics of the system has to be taken into account.

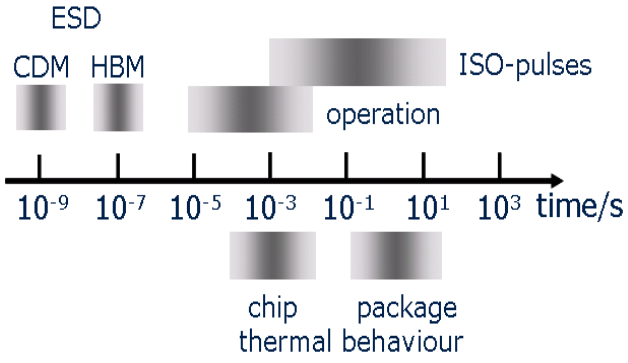

Figure 3. Timescales relevant to the operation of DMOS transistors

DMOS transistors exposed to pulses with high energies show strong degradation of the metallization. Such metal degradation was already observed several years ago, for example; by Ciappa and Malberti after power cycling of IGBTs [8]. In that work the phenomenon was termed *metal reconstruction*. It has received increasing attention recently, especially in the context of repetitive short circuit [9, 10]. Fig. 4 shows severe degradation of DMOS metallization (AlSiCu) after repetitive short circuit stress [9]. Similar metal degradation has also been observed on DMOS transistors after severe repetitive clamping (AlCu, 10^9 pulses, $\Delta T \approx 100$ K), as shown in Fig. 5. In general, the metallization shows buckling, cracks and voids. One possible failure mode may be bond lift-off. Another failure mode is a short in the DMOS between different potential, leading to destruction of the DMOS.

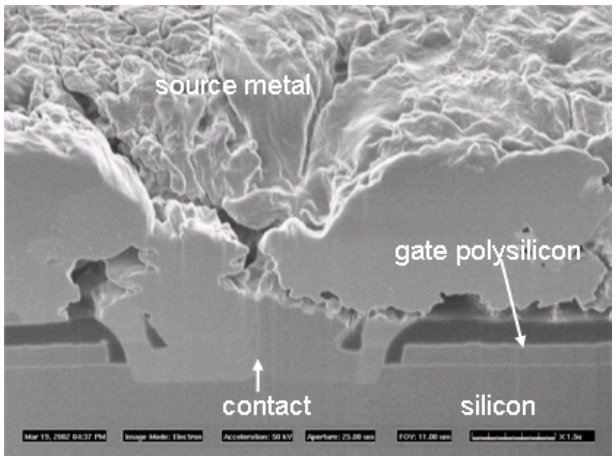

Figure 4. DMOS metallization after repetitive short circuit stress

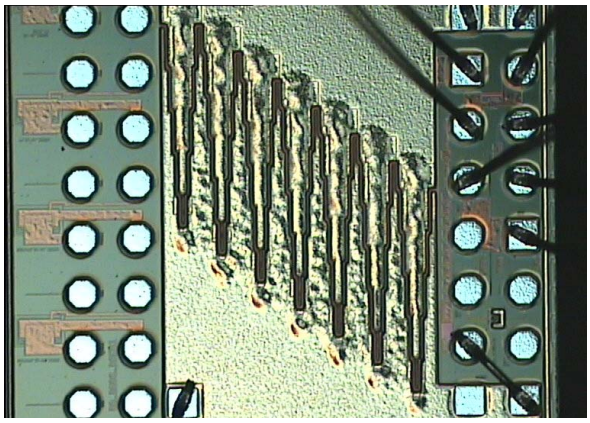

Figure 5. DMOS metallization after repetitive clamping.

The phenomenon of metal degradation under active cycling conditions was recently studied in depth by T. Smorodin et al. [11, 12]. He used a test structure consisting of a metal meander and a power metal layer, which was passively heated by an underlying polysilicon resistor, thereby avoiding any potential electromigration effects. In addition, also DMOS structures were stressed. The test devices were cycled by thermal pulses with pulse durations between 200 µs and a few milliseconds and temperature increases of 90 to >200 K. The results show a dependence of the cycles (or equivalently) time to fail on the temperature increase ΔT on the device. Fig. 6 gives an example of failure distributions for DMOS structures for temperature rises of 170 K and 190 K, the pulse duration was 1 ms.

As a result of the investigations, the following failure mechanism as illustrated in Fig. 7 emerges:

- The time-dependent voltage and current pulses cause power dissipation and thereby heating in the device.
- Because of the timescales of the pulses and the system chip/package, the spatial and time dependence of the temperature has to be taken into account. Simply calculating a junction temperature by (1) is not sufficient.
- The inhomogeneous temperature distribution causes stress in the metallization resulting in plastic deformation.
- The plastic deformation of the metallization causes stress in the intermetal dielectric, eventually leading to cracking and a short in the DMOS. Fig. 8 shows an example of an interlevel dielectric crack filled with aluminum at the periphery of a DMOS that was subjected to repetitive short circuit pulses.

The temperature rise is one essential parameter that influences the reliability of the DMOS. Lower ΔT means a higher number of pulses to fail. Naturally the question arises, what ΔT can be allowed to fulfill the requirements of several hundred million pulses as given in Table I, at he same time optimizing the chip area fulfilling also the stringent economic constraints for the products.

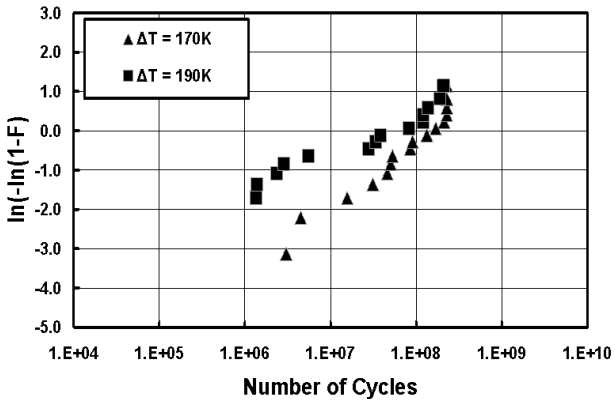

Figure 6. Cumulative fail distribution using a Weibull scale after repetitive clamping of DMOS transistors with two different values for the temperature increase.

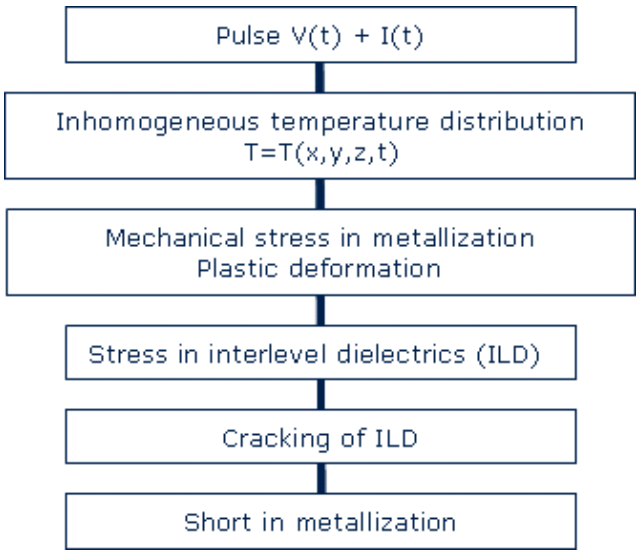

Figure 7. Failure mechanism of a DMOS transistor in a smart power technology under repetitive clamping stress due to metal degradation.

IV. A Look at Qualification Procedures

Having identified the relevant failure mechanism as plastic deformation of the metallization induced by actively cycling the device, leading to mechanical stress and cracking of the dielectric with a subsequent short, a procedure has to be found to characterize the reliability of the device with respect to this behavior. A look at "classical" tests used for silicon reliability reveals that none of the tests is suited for addressing this problem. This applies both to electromigration, which can be ruled out because of the results being obtained by passive heating, and to stressmigration. On the other hand, tests used for product qualification may provide a solution. In the standard AEC Q100 [13], which is the de facto standard for qualification of automotive integrated semiconductor components, tests that are actively stressing the device are the High Temperature Operating Life Test (HTOL) [14] and the Power Temperature Cycling Test (PTC) [15]. A closer scrutiny of these tests shows that product qualification procedures are totally inadequate to address the problem in hand. There are several reasons for this:

- The standard setup of the HTOL is oriented at the maximum junction temperature, which is, as we have seen, an unsuitable parameter for this failure mechanism.
- The same applies to the PTC test.
- The tacit assumption that these tests are accelerated in a manner to cover the lifetime requirements of the application does not stand up to closer investigation.
- Insufficient data on acceleration models and parameters for these failure mechanisms are available. Also, product qualification tests are generally not defined in a manner suitable to determination of such parameters. Even if the stress test were set up to expose the device to an adequate thermo-mechanical stress, this would only apply to one specific condition.
- The pass/fail criterion is fulfillment of the (electrical) specification after a typical test duration of 1000 h. In consequence, passing the test does not give any information on the acceleration and the lifetime model of the product, and, therefore, no assessment of the robustness margin (or, equivalently, the SOA) of the product with respect to the application requirements.

In conclusion, neither "classical" silicon reliability tests nor product qualification procedures are adequate to address the considered failure mechanism and do not provide a means for assessing the reliability.

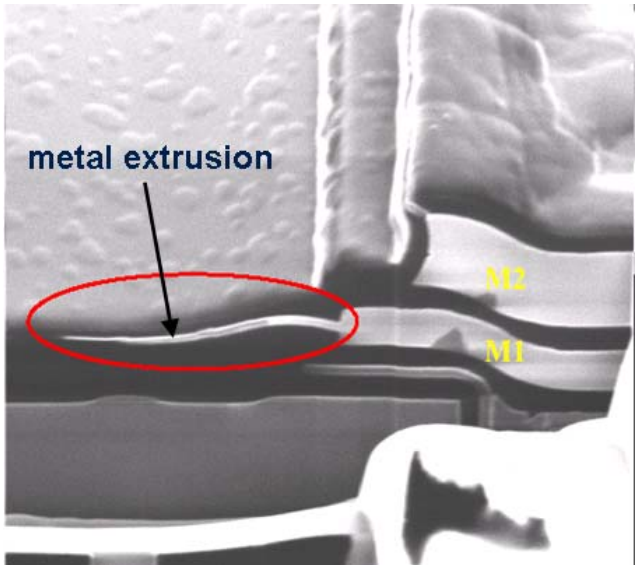

Figure 8. Example of a crack in the dielectric filled with aluminum after repetitive short circuit stress of a DMOS. M1 and M2 denote metal 1 and metal 2, respectively.

V. Characterization Strategy

Semiconductor suppliers, tier1s and OEMs have recently become increasingly aware of the deficiencies of a product qualification based on common standards like AEC Q100 [13] and JEDEC JESD47 [16]. Based on the work of a group involving participants from the whole supply chain, the

"Handbook for Robustness Validation of Semiconductor Devices in Automotive Applications" was released by the German ZVEI[1] in April 2007 and as an American standard by SAE[2] in October 2007. Robustness Validation is a failure mechanism-based approach that applies basic principles of silicon reliability methodology to product qualification. Its key components are:

- Knowledge of the conditions of use (mission profile).
- Knowledge of the failure mechanisms and failure modes.
- Knowledge of acceleration models for the failure mechanisms needed to define and assess accelerated tests.

That implies that Robustness Validation aims at test to fail, contrary to standard product qualification criteria, which require zero fails for passing qualification.

Applying these principles to active cycling, a suitable characterization strategy is proposed as illustrated in Fig. 9. Technology development should provide test to fail data, a model for the failure mechanism to relate stress conditions to use conditions, and a corresponding design strategy for products. A design strategy serves to build in reliability into the product. Only testing a posteriori is not a viable way to achieve reliability and, at the same time, meeting cost and time-to-market demands.

Having identified ΔT and t_{pulse} as major influencing parameters, an essential question to be answered is: What is the temperature increase ΔT? On the relevant timescales the temperature is far from being homogeneous over the device. Rather, we have to deal with a spatially and time-dependent temperature distribution. This information can only be obtained by electro-thermal simulation. The simulation is needed to convert the application requirements into technologically relevant information for a set of assumed operation conditions and a specific layout. Electro-thermal simulation in this way becomes an essential part both of the qualification and the design strategy for specific products. Fig. 10 gives an example of 3D electro-thermal simulations of test structures (size appr. 700x700 µm²) used for repetitive clamping investigations. Fig. 10a shows the time-dependent temperature behavior of the hot spot on the structure. Starting with a power of 18 W for a specific pulse duration of 5 ms, the peak temperature is seen to rise to 234 °C, i.e. 124 °C above the base temperature of 110 °C (case 1). Case 2 in Fig. 10a shows the time dependence for 1 ms pulse duration with the power adjusted to give the same temperature rise. Fig. 10b displays a 2D cut through the middle of the simulated structure showing the temperature distributions for both cases 1 and 2 of Fig. 10a at the point in time of maximum temperature. Calibration of the simulation with measured data is, of course, a prerequisite for usage of this tool. In the case of the test structure the resistance of an integrated small metal meander in the middle of the test structure was used for measurement of the temperature. In a similar manner, 3D simulations were also carried out for DMOS transistors. In that case calibration was based on special diodes embedded in DMOS structures [17].

The boundary conditions for active cycling, i.e. the number of pulses allowed for a specific ΔT and t_{pulse} have to be obtained during development of the wafer technology, and thereby constitute design rules for the products. Verification of the design rules (not the product specification) will be done on the lead product only. Follower products that have been designed according to these design rules, therefore, due not have to be qualified separately with respect to active cycling requirements, but will be referenced to the technology design rules, in the same vein as e.g. electromigration.

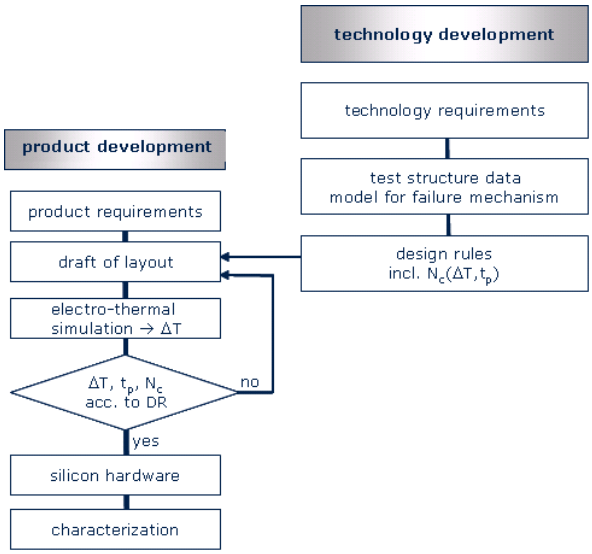

Figure 9. Flow for the characterization of active cycling

VI. Discussion

Active cycling can lead to strong metal degradation due to thermo-mechanical stress and destruction of power devices. Both "classical" silicon wafer technology reliability methods and standard product qualification procedures are inadequate to address this issue. An effective qualification strategy has to take into account the fact that loads and use conditions of the products can vary widely. Technology development has to provide a database also for active cycling issues, i.e. design rules, upon which product designs can be realized. An approach to assure the reliability of the devices is presented that is based on the principles of Robustness Validation and provides both a design strategy and a foundation for qualification. Electro-thermal simulation is an essential ingredient of this flow. By defining corresponding design rules for active cycling conditions based on investigations during technology development products can be referenced to these results, thereby reducing qualification testing for products realized in the technology.

[1] ZVEI: German Electrical and Electronic Manufacturers' Association
[2] SAE: Society of Automotive Engineers

Electro-thermal simulation is one essential ingredient of future design strategies. However, full understanding of the effect of metal degradation can only be obtained by support of thermo-mechanical simulation, because, eventually, it is the mechanical stress leading to the deformation. Such simulations have to be based on knowledge of material parameters such as the temperature dependent yield stress of the metal films. These parameters need advanced characterization methods and have to be obtained specifically for the technology under consideration.

Much work is still needed to gain a full understanding of the factors that potentially influence this failure mechanism. Acceleration modeling is not satisfactory today. In many cases, simple Coffin-Manson type relations are used that do not include the different influencing factors, raising the question of the range of applicability of the models.

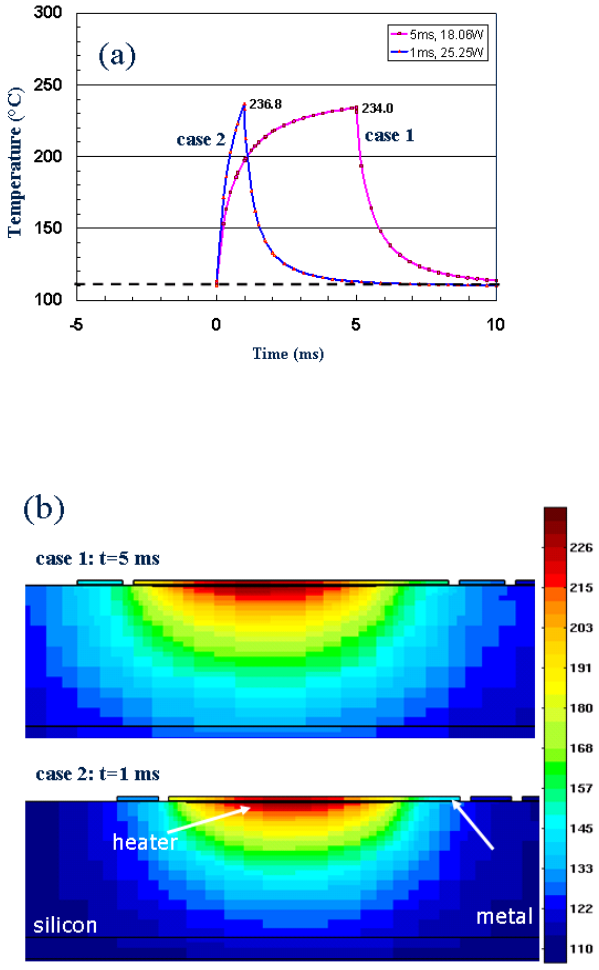

Figure 10. Electro-thermal simulation of a test structure for two pulse conditions, 1 ms and 5 ms pulse duration with power adjusted to give the same peak temperature: (a) time-dependence of temperature, (b) spatial distribution at peak temperature

Applying a strategy, as proposed, based on the principles of Robustness Validation is crucial to building in reliability into the products in the design phase. This implies not only solving technical problems but also cultural changes. However, adhering to qualification procedures as given in the common standards does not give adequate results and is no viable way into the future.

CONCLUSIONS

In conclusion, it was shown that active cycling of power devices can lead to severe degradation of the metallization of the power stage. Neither "classical" silicon reliability methods nor standard product qualification procedures are adequate to handle this problem. A procedure was proposed based on the principles of Robustness Validation. Electro-thermal simulation plays an important role in the design and qualification strategy and is indispensable for a failure mechanism based approach. More work is needed to increase understanding of different influencing factors and to obtain a lifetime model that takes these factors into account. Eventually this should serve to assess application requirements without doing costly and long-lasting tests or, even worse, relying on inadequate product qualification tests.

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