Short-Circuit Protection Circuits for Silicon-Carbide Power Transistors

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***Abstract*—An experimental analysis of the behavior under short-circuit conditions of three different silicon-carbide (SiC) 1200-V power devices is presented. It is found that all devices take up a substantial voltage, which is favorable for detection of short circuits. A transient thermal device simulation was performed to determine the temperature stress on the die during a short-circuit event, for the SiC MOSFET. It was found that, for reliability reasons, the short-circuit time should be limited to values well below Si IGBT tolerances. Guidelines toward a rugged design for short-circuit protection (SCP) are presented with an emphasis on improving the reliability and availability of the overall system. A SiC device driver with an integrated SCP is presented for each device-type, respectively, where a short-circuit detection is added to a conventional driver design in a simple way. The SCP driver was experimentally evaluated with a detection time of 180 ns. For all devices, short-circuit times well below 1 μs were achieved.**

***Index Terms*—Bipolar junction transistor (BJT), driver circuits, failure analysis, fault detection, fault protection, junction field-effect transistor (JFET), power MOSFET, semiconductor device reliability, short-circuit current, silicon carbide (SiC), wide-bandgap semiconductors.**

I. Introduction

SILICON-carbide (SiC) transistors have undergone a great development over the past few years, and their level of maturity is now sufficient for product development of converters for various applications [1] ranging from motor drives for different kinds of vehicles [2] to various industrial applications [3], high-temperature operation [4]–[7], high-frequency applications [8], and renewable energy generation [9]. This interest motivates research efforts toward application reliability. The currently existing SiC power devices are junction field-effect transistors (JFETs) and metal-oxide semiconductor field-effect transistors (MOSFETs), which are unipolar and voltage-controlled, and the bipolar junction transistor (BJT), which is bipolar and current-controlled. However, it behaves as a unipolar device both with respect to conduction and switching properties [10].

Transient robustness of SiC transistors under short-circuit conditions has already been investigated. In [11]–[13], the conclusions are that the SiC MOSFET can withstand short-circuit conditions for 13–80 μs depending on its gate-to-source voltage and on the dc-bus voltage. The short-circuit withstand time and critical energy of SiC MOSFETs are, however, reduced with the increase of case temperature [14]. In [15]–[20], the SiC JFET is also investigated and is found to be more rugged than the SiC MOSFET. It can handle short-circuit times of more than 1.4 ms with a 400-V dc-bus voltage [16]. The SiC BJT has been reported to withstand short-circuit conditions with durations of 15–20 μs [17], [21], and [22]. The good ruggedness indicates that a second breakdown is not likely with the SiC BJT, as it was with the power BJT in silicon [23].

For unipolar devices, it is observed in [16] that the saturation current density during a short-circuit event decreases significantly faster for the SiC JFET than for the SiC MOSFET leading to a faster temperature rise for the SiC MOSFET. The slower saturation process of the SiC MOSFET results in a higher current density than for the SiC JFET. Since the SiC BJT has the benefit of an intrinsic current limitation directly related to its amplification factor β, the SiC MOSFET is the device that will experience the highest short-circuit current with regard to the chip size. For this reason, it is likely that the MOSFET will experience the highest overvoltages when turning OFF the short-circuit current.

The failure analysis of the different SiC devices under short-circuit condition is in favor of an early short-circuit fault detection and extinction. Not only this strategy is limiting self-heating of the device, but also it is limiting the current that the device has to turn OFF. The oxide layer of SiC MOSFETs may be sensitive to high-temperature stress [24], [25], and gate failure can occur even after short-circuit has been turned OFF due to the heat spread from the drift region to the oxide [12], [26]. In [26], the gate oxide of SiC MOSFETs is shown to be less reliable than that of Si MOSFETs. The increased temperature during short-circuit conditions results in an increase of the gate leakage current [26], [27]. Even though it is likely that these issues will be alleviated in new generations of SiC MOSFETs [28], a limitation of the short-circuit time is probably still beneficial in terms of reliability.

The present paper investigates the possibility of detection and protection of a short-circuit event in the early stage of a fault as

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was already shown in [29]. To provide a better understanding of the short-circuit behavior at a die level, a transient thermal device simulation is performed for the SiC MOSFET. Guidelines regarding SCP times when high reliability is targeted are formulated. Finally, design rules toward an SCP driver preserving the device immunity are discussed.

In [30], a comparison of three different SCP implementations for SiC MOSFETs has recently been presented. This publication also supports the early detection and extinction of short-circuit events. Additionally, in order to avoid erroneous triggering, it is stressed that the short-circuit protection must have a high noise immunity against electromagnetic interference in fast-switching applications. The issue of overvoltages at the turn-OFF of a short-circuit event was also raised. In [31], on the other hand, an SCP for SiC JFETs is presented with a protection time below 100 μs. Solutions to solve the normally-ON behavior of SiC JFETs during the power-ON time of power converters are presented in [32] and [33]. In this paper, protection times are well below 1 μs. In addition, a discussion on the short-circuit behavior of SiC BJTs is presented. In contrast to [30] and [31], this publication not only focuses on three different devices but it aims to give a broad overview of the short-circuit behavior of SiC carbide devices and how to handle this fault in the most reliable manner. The devices tested are the most recent devices available. Finally, three SCP drivers are implemented.

The short-circuit behavior of SiC transistors is presented in Section II. Section III focuses on the transient thermal device simulation and its analysis. The short-circuit detection design is discussed in Section IV-A. Sections IV-B, IV-C, and IV-D present the SCP circuits of SiC BJTs, MOSFETs, and JFETs, respectively. Finally, a discussion is given in Section V. Section VI concludes this paper.

II. Short-Circuit Behavior of SiC Power Devices

There are two types of short-circuit faults. A fault occurring during the transistor turn-ON transient is referred to as hard switching fault (HSF), and a fault occurring during ON-state conditions is referred to as fault under load (FUL). A complete analysis of these two types of faults has been given in [34]. During both short-circuit types, the current rises rapidly and the device saturates. As previously investigated in [30], for SiC MOSFETs, both fault-types can be detected by means of the desaturation technique. However, the detection delay times are higher for HSF than for FUL. Consequently, only the HSF will be studied in this paper to limit the scope of investigation.

Prior to designing a SCP for SiC Power devices, the behavior of SiC power transistors during the early stage of a short-circuit fault is investigated. In Section III, the maximal short-circuit time acceptable with regards to reliability considerations will be discussed. The experiments aim for extracting the information on how a short-circuit fault can be detected and on how fast it can be detected. Moreover, the turn-OFF transients are analyzed to define an appropriate turn-OFF procedure in case of a short circuit. In fact, if the high switching speeds of SiC power transistors are fully utilized, this may cause excessive overvoltages when turning OFF a short-circuit current. Moreover, once a short-circuit condition has been detected, any additional

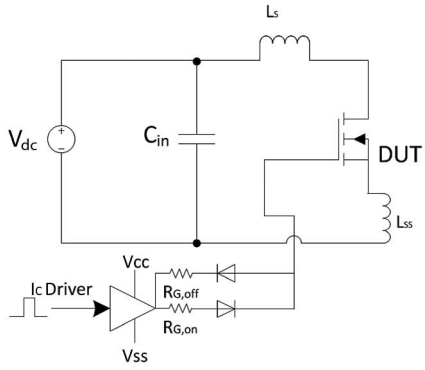


Fig. 1. Schematic of the short-circuit test for a discrete device.

delay before turning the short-circuit current OFF may reduce the lifetime of the device due to excessive localized heating. A short duration of the short-circuit condition is, therefore, preferable for reliability reasons. The test circuit is shown in Fig. 1. The dc-link voltage is $V_{\mathrm{dc}} = 600$ V. The circuit stray inductance L_s (excluding the capacitor and the device) has been determined experimentally to 32 nH. Assuming that the internal stray inductance L_{ss} of the TO-247 package is 10 nH, the total circuit stray inductance is approximately 42 nH.

The currently available SiC power semiconductors are the MOSFET, the JFET, and the BJT. The SiC MOSFET and the SiC JFET are voltage-controlled, and the BJT is current-controlled. As these two device "types" perform differently with regards to overcurrent, they will be analyzed separately in the following sections.

A. Short-Circuit Behavior of Voltage-Controlled SiC Power Semiconductors

First, two different SiC MOSFETs (C2M0025120D from Cree and SCT2080KE from Rohm) and one SiC normally-ON JFET (UJN1205K from USCi) are investigated. The short-circuit pulse is of 500 ns for the MOSFETs and 250 ns for the JFET. The main difference between the two MOSFETs is the chip size and the chip thickness. The driver output stage is powered by a positive voltage source of +24 V and a negative power source of −5 V. The external gate resistance is 20 Ω for both turn-ON and turn-OFF. This value guarantees low oscillations at turn-ON and turn-OFF, while the switching times remain below 40 ns. In the case of the normally-ON SiC JFET, the driver was powered by a negative voltage source of −30 V, and the gate resistor was replaced by a DRC network as in [35] and [36].

The short-circuit behavior of the SiC MOSFETs from Cree and Rohm is shown in Figs. 2 and 3, respectively. The voltage across the SiC MOSFET does not drop significantly during the short-circuit pulse. As soon as the switch is turned ON, the current starts rising fast. Then, the rising slope decreases with time. Fig. 4 shows the short-circuit behavior of the SiC JFET under test. This device has the smallest chip area/volume of all the investigated devices. Since the SiC JFET saturation current density has a negative temperature coefficient [16], this device saturates faster than the previously investigated devices, and the current rises at a slower pace. The short-circuit peak current

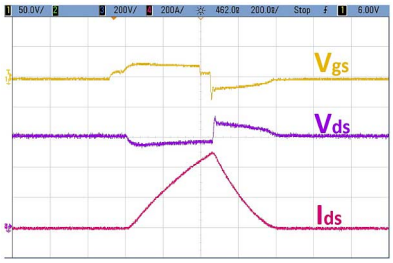


Fig. 2. Short-circuited Cree MOSFET, $R_G = 20\ \Omega$. Measured gate-to-source voltage (yellow line: 50 V/div), drain-to-source voltage (purple line: 200 V/div), and drain current (pink line: 200 A/div). Time base: 200 ns/div.

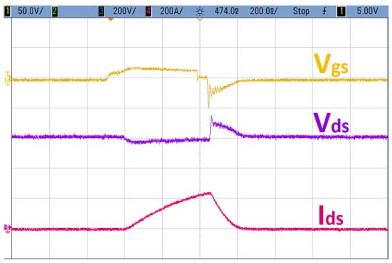


Fig. 3. Short-circuited Rohm MOSFET, $R_G = 20\ \Omega$. Measured gate-to-source voltage (yellow line: 50 V/div), drain-to-source voltage (purple line 200 V/div), and drain current (pink line: 200 A/div). Time base: 200 ns/div.

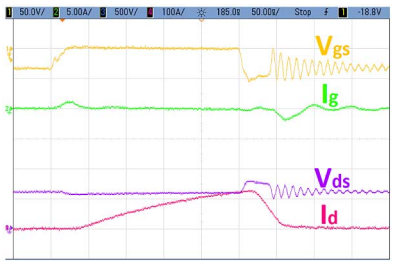


Fig. 4. Short-circuited normally ON JFET, $R_G = 10\ \Omega$. Measured gate-to-source voltage (yellow line: 50 V/div), gate current (green line: 5 A/div), drain-to-source voltage (purple line: 500 V/div), and drain current (pink line: 100 A/div). Time base: 50 ns/div.

TABLE I
SHORT-CIRCUIT BEHAVIOR OF VOLTAGE-CONTROLLED DEVICES

SiC DUTs	I_{peak} (A)	Overvoltage (V)	Turn-off time (ns)
C2M0025120D	500	200	320
SCT2080KE	300	150	140
UJN1205K	120	200	40

I_{peak}, the overvoltage, and the short-circuit turn-OFF time for the voltage-controlled devices are summarized in Table I.

B. Short-Circuit Behavior of Current-Controlled SiC Power Semiconductors

In this section, two devices rated at 1200 V/50 A from two different suppliers are analyzed. Those are the SiC BJT from Fairchild (FSICBH017A120) and the super-junction transistor (SJT) from GeneSiC (GA50JT12-247). SJTs are super-high current gain SiC BJTs. For simplicity, this device will be regarded as a BJT in this paper. The SiC BJTs are driven by a so-called dual-source driver using a high voltage for fast switching and a low voltage for the continuous base current [37].

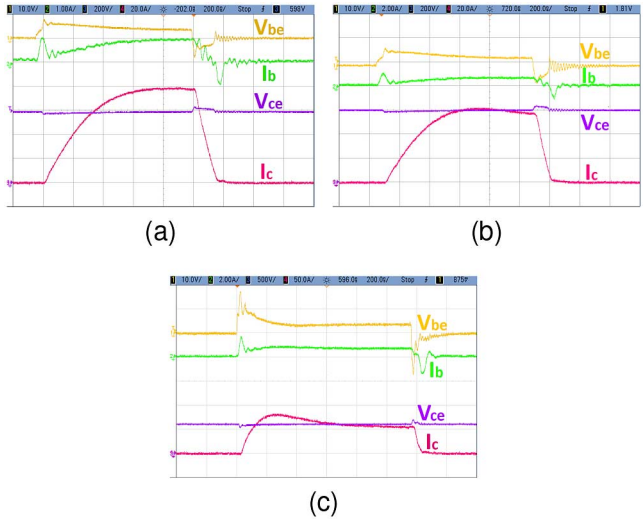


Fig. 5. (a) Short-circuited SiC BJT, $I_b = 1$ A. (b) Short-circuited SiC BJT, $I_b = 0.5$ A. (c) Short-circuited SiC SJT, $I_b = 0.75$ A. Measured base-to-emitter voltage (yellow line: 10 V/div); base current [green line: (a) 1 A/div, (b) and (c) 2 A/div]; collector–emitter voltage [purple line: (a) and (b) 200 V/div (c) 500 V/div]; and collector current [pink line: (a) 20 A/div and (b) 50 A/div]. Time base: 200 ns/div.

TABLE II
SHORT-CIRCUIT BEHAVIOR OF CURRENT-CONTROLLED DEVICES

SiC DUTs	I_b (A)	I_{peak} (A)	Turn-off time (ns)
FSICBH017A120	1	80	120
FSICBH017A120	0.5	60	100
GA50JT12-247	0.75	80	50

Even though the SiC BJT has similar conduction and switching properties as the voltage-controlled devices, it is current-controlled with regards to the maximum collector current. This feature, which can be seen as a limitation when it comes to driver designs, turns into an advantage when a reliable short-circuit protection is targeted. As the current is intrinsically limited, the turn-OFF voltage overshoot is expected to be limited. To emphasize the intrinsic current limitation of the SiC BJT, which depends on the base current I_b, the two tests are performed with a base current of 1 A and 0.5 A, respectively, for the device from Fairchild. The short-circuit pulse is of 1 µs. This can be seen in Fig. 5(a) and (b). The results are also stated in Table II. The collector peak currents are, as expected, considerably lower than the maximum currents observed for the unipolar devices. This results in a considerably low overvoltage at turn-OFF. A similar behavior is shown in Fig. 5(c) for the GeneSiC device although this device saturates quicker.

For all the tested devices, the voltage across the device during a short-circuit fault is approximately 300 times higher than during normal operation. Thus, the devices never leave the active region. As V_{ds} does not drop below 80% of the dc-bus voltage, an early detection is possible by measuring the

drain-to-source voltage of the device. This method, called "desaturation" technique, has already been used for Si devices [38]–[40]. SiC devices have a higher power density than their Si counterparts. Thus, it is important to clear the fault as soon as it has been detected to avoid unnecessary power dissipation and associated excessive heating. From a reliability point-of-view, a fast protection can prevent the device from early degradation. The short-circuit protection of SiC unipolar devices requires additional attention regarding the high-voltage overshoot at turn-OFF. On the contrary, the short-circuit protection of SiC BJTs does not require special considerations to handle the turn-OFF transients following a fault clearance. In fact, the limited short-circuit current reduces the overvoltages at turn-OFF. Moreover, the limited current limits the losses produced in the chip during fault events, which is certainly beneficial for reliability considerations. The authors believe that a proper protection strategy should improve the overall robustness of the converter.

III. Temperature Distribution in the Die During a Short Circuit

This section discusses the time evolution of the temperature distribution in the chip during a short-circuit event. The device investigated here is the SiC MOSFET as its oxide layer may be sensitive to heat dissipation in the die [41], [42]. The gate oxide of SiC MOSFETs is thinner than the one of Si MOSFETs [26]. It is thus exposed to a higher electric field for a given gate bias. The high electric field and current density to which the oxide layer is exposed to during short-circuit conditions may increase the tunneling effect known as the main degradation mechanism of the oxide layer of SiC power MOSFETs [41]. The failure modes of SiC MOSFETs when subjected to longer short-circuits have been investigated in [43]. The presence of a gate leakage current after a few microseconds of short circuit is observed, which is not the case for Si devices. SiC MOSFETs showed low robustness to cumulative short circuits for longer short-circuit durations. The failure mode translates in a short circuit between gate and source for some devices, and other devices additionally have shorted drain and source.

A transient simulation is performed on the SiC MOSFET from Rohm (SCH2080KE). The device was decapsulated and analyzed by optical microscopy and scanning electron microscopy, and reconstructed by the numerical simulation program Synopsis Medici [44]. The boundary conditions were implemented according to the datasheet values for the packaged DUT, considering the specific construction of the package. The results from this simulation agree with the measured results in Section II. The thermal resistance and capacitance used in the simulation are $R_{\text{th}} = 0.0918$ K/W and $C_{\text{th}} = 5e-3$ Ws/K.

In Fig. 6, the temperature distribution in the chip of the DUT after 500 ns of short circuit is shown. The maximum temperature is 267 °C, and any prolongation of the short-circuit duration will increase this value. The hotspot appears in the JFET region of the MOSFET (where the current concentrates) situated 2 μm below the gate oxide. This is not surprising, because this is the typical heat profile in any D-MOS device even during normal operation. Therefore, for any D-MOS SiC

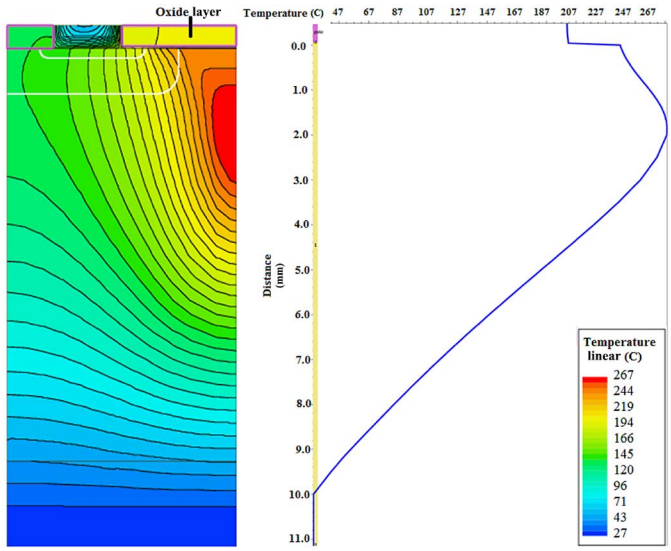


Fig. 6. Temperature distribution in the chip after 500 ns.

MOSFET, regardless of doping levels, the highest temperature will be situated just below the gate oxide. This supports the idea to clear the short circuit as fast as possible to prevent localized overheating of the gate oxide (for reliability reasons). The leakage current increase accelerates the oxide degradation during repetitive tests. An increase of the drain-to-source leakage current has also been reported in [12].

The SiC JFET has a recessed gate (or surface gate). In this case, the highest temperature is also situated close to the gate, and thus, the surface. Even though there is no oxide layer, repeated exposure to high temperature in time can be harmful for the passivation and metallization layers. The ageing of the SiC JFET due to multiple short-circuit events is characterized by an increase of the ON-state resistance [18], [45]. In [46], it is emphasized that, for the SiC JFET, a short duration of short circuit allows the device to sustain a considerably higher number of short-circuit events. Finally, for the BJT, the base region and collector region are about one order of magnitude narrower for SiC than for Si.

As the power density is higher for SiC compared to Si and since everything is thinner in SiC compared to Si, it is recommended, for reliability reasons, to consider short short-circuit times. The highest temperature occurs close to the top surface, which has much poorer cooling in wire-bonded encapsulated devices compared to the bottom surface. The reliability of SiC devices may be improved by means of an intelligent gate/base driver.

The source stray inductance also has an effect on the short-circuit behavior of SiC devices as shown in in Fig. 7. Low-inductive circuits thus require a faster reaction to preserve the chip and package immunity. At times when even more circuits are desired to be low-inductive, the need of turning OFF the fault quickly becomes very relevant.

IV. Short-Circuit Protection

With the knowledge of the behavior of various SiC devices under short-circuit conditions acquired in Section II, several

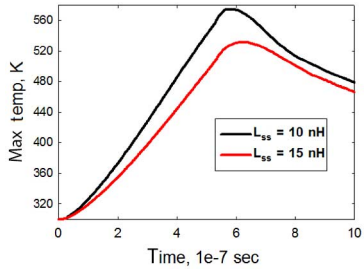


Fig. 7. Effect of the source stray inductance L_{ss} on the temperature rise.

design rules toward a rugged short-circuit detection can be derived. A driver with an integrated SCP can be designed based on those rules. While most driver manufacturers are targeting SiC MOSFETs, the proposed solution can also be applied to other SiC types. The main objective of this work is to implement a simple yet robust short-circuit detection that can be directly applied to a conventional driver design. Besides turning-OFF the short-circuit as quickly as possible, the SCP driver has to turn-OFF the fault in a safe manner. A fast detection combined with a slower turn-OFF is advisable for unipolar SiC devices, whereas for the BJT, only fast detection is beneficial due to the low-voltage overshoot at turn-OFF. Solutions for a gate driver providing a slower turn-OFF have been presented in [47]. In this paper, the slower turn-OFF is achieved, for the SiC MOSFET with asymmetrical gate resistors for turn-ON and turn-OFF, as shown in Fig. 1.

A solution for SiC MOSFETs has recently been presented in [30], where rapid short-circuit detection is achieved. However, the turn-OFF times are relatively long. A solution for SiC JFETs has also been presented in [31]. While these two concepts involve the use of a comparator for the detection of de-saturation, the proposed design proposes a novel solution to increase the noise immunity in fast-switching environments. Logic gates with integrated Schmitt triggers are used here for voltage comparison. This solution is motivated by the fact that the voltage during a fault is of the order of hundreds of volts as shown in Section II.

Gate drivers for IGBTs and SiC MOSFETs with desaturation protection are already available. Prodrive in association with Cree offers a driver with overcurrent protection. The turn-OFF time is stated to be of maximum 1 μs. Cree has another dual-channel driver for SiC MOSFET modules with SCP (CGD15HB62P). CISSOID also offers a driver (CHT-HADES2S) with SCP for high-temperature applications. This driver offers soft turn-OFF within 300 ns. The voltage comparison uses a comparator. The detection times are not clearly specified. Depending on the temperature of operation, 300 ns may be too long considering the change in short-circuit capabilities of SiC devices at higher temperatures [14].

SCALE-2 IGBT gate driver planar core from power integration is also offering an SCP. Its minimum response time is 1.2 μs. Even though time may have been improved in a newer version of the driver, the maximum output voltage (15–16 V) is below the required voltage to drive SiC MOSFETs in an efficient way. Similarly, Texas Instruments also have an IGBT and MOSFET driver with an integrated desaturation circuit having a reaction time of 2.7 μs.

Commercially available IGBT drivers using the desaturation detection technique could be used to detect a short circuit for SiC devices. Most drivers are also compatible with SiC MOSFETs and can offer a soft shutdown of the device in case of a short circuit. However, the offered reaction times are often too slow to provide a reliable protection of the device under fault. Nevertheless, from all the drivers specified above, the driver from CISSOID (CHT-HADES2S) is the most suitable driver for the short-circuit protection of SiC MOSFETs. The authors would like to stress the importance of dedicated desaturation circuits for SiC power devices.

The parameters that have to be taken into account when designing a SCP for SiC devices are briefly summarized in Section IV-A, where a clear description of the design challenges is provided.

A. Short-Circuit Detection Design

Since the ON-state voltage drop of the device during a short-circuit fault is much higher than during the normal operation, the short-circuit condition can easily be detected by comparing the control input with the drain-to-source voltage (or the collector–emitter voltage). This detection method is known as the desaturation method [38]–[40]. As emphasized earlier, a fast detection not only reduces the current level at which the device has to be shutdown but also it limits the self-heating of the device as well. Additionally, the voltage overshoot at turn-OFF is limited. The proposed implementation has the following targets:

1) fast detection;
2) fast reaction to limit overheating;
3) limited turn-OFF speed for the SiC MOSFET and JFET;
4) easy implementation in any driver design;
5) high noise immunity.

Besides these targets, the driver has to be placed as close as possible to the gate and source pins of the device to avoid undesired parasitic elements.

The speed of detection is limited by the turn-ON and turn-OFF times of the protected device. In addition, margins have to be considered to avoid false triggering or the SCP. In the present implementation, the fault detection delays are defined by RC filters. Fast detection delays are also limiting the overshoot at turn-OFF. A limited turn-OFF speed is also easily achieved by using different gate resistors for turn-ON and turn-OFF. A drawback of this solution is that the switching losses at turn-OFF are increased. However, if very high switching speeds (and low switching losses) are targeted, a solution using an alternative gate resistance in case of a fault could be a solution. The proposed solution provides an easy implementation enhancing the driver reliability without affecting the driver characteristics during normal operation.

The structure of the short-circuit detection is shown in Fig. 8 for the case of a SiC BJT. The concept of the detection circuit is the same for the SiC JFET and MOSFET. The logic circuits used in this realization are from the TTL series, with a 5-V supply voltage for the SiC BJT and from the CD4000B series,

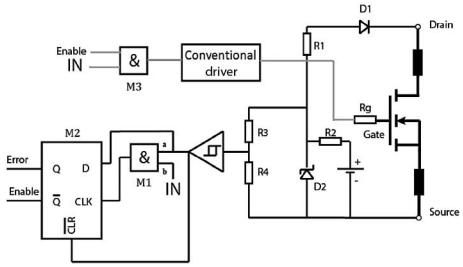


Fig. 8. Schematic diagram of the short-circuit detection.

TABLE III
TRUTH TABLE OF THE SHORT-CIRCUIT DETECTION METHOD

Control signal	V_{ds}	AND	Meaning
0	0	0	Circuit off
0	1	0	Off-state
1	0	0	On-state
1	1	1	Short-circuit or fault

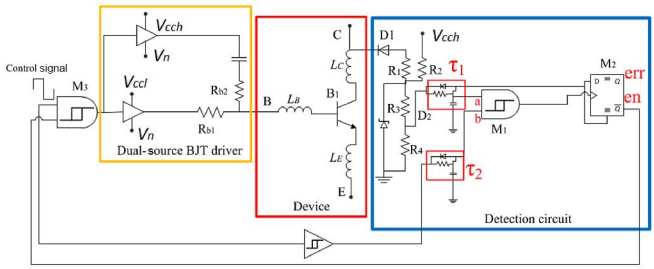


Fig. 9. Schematic diagram of the SCP driver for a SiC BJT.

with modifications, for the SiC MOSFET and JFET (12 V and 15 V, respectively).

The collector–emitter voltage is sensed through D_1. The diode D_2 clamps the sensed voltage to protect the logic circuits. A Schmitt trigger AND M_1 is chosen for its high noise immunity. Above a certain voltage sensed by D_1, M_1 will sense a high voltage at its input a. This voltage can be adjusted by means of the voltage divider formed by R_3 and R_4. Its output will toggle to high if, and only if, the voltage sensed by its input b, sensing the control signal, is high at the same time. Thus, the AND gate acts as a comparator. For a better understanding, the truth table for the detection circuit is given in Table III. A D-type flip-flop M_2 is used in a later stage to hold the detected short-circuit signal when the control signal returns to zero. At the rising edge of the clock signal, the D-latch transfers its D input to its Q and $\bar{Q}$ outputs. The Q and $\bar{Q}$ outputs are the error signal (*err*) and the enable signal (*en*), respectively. Depending on the application, the *err* signal can be used to alert the main control system that a failure has occurred while the *en* signal is used to force the driver input to the OFF state. $\bar{Q}$ remains low until the whole system is shut down. The RC filters τ_1 and τ_2 are added before M_1, as shown in Fig. 9. The detection delays corresponding to τ_1 and τ_2 are then calibrated depending on the chosen device and the final application.

The presented short-circuit detection can be directly integrated into a conventional SiC power semiconductor driver. This integration allows a fast turn-OFF of the device at the inception of a short circuit, because the fault handling is performed locally without involvement of external control circuits. Being fully independent from the driver, it can easily be combined with almost any kind of driver without adding much complexity. Three different SCP drivers have been designed. The SCP drivers for SiC power BJTs, SiC power MOSFETs, and SiC power JFETs are presented in Sections IV-B, IV-C, and IV-D, respectively. The performance of the SCP drivers is investigated by performing a short-circuit test and a double-pulse test. These tests are performed to verify that there are no erroneous short-circuit detections. The drivers—though without SCP—used in this paper have already been tested successfully in [48]–[50] for the SiC BJT, MOSFET, and JFET, respectively. The switching times during normal operation without SCP can be observed in these publications. Moreover, the robustness of the driver against noise was tested in an industrial converter in [49], where it is implemented in a 20-kHz three-phase 312-kVA inverter for an electrical vehicle with a total of 30 SiC MOSFET modules and 60 SCP drivers.

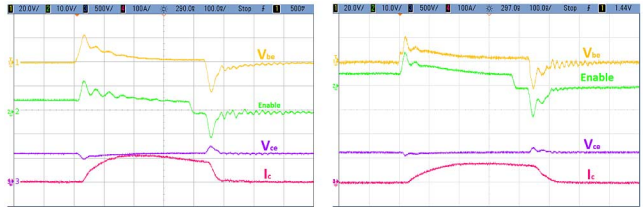


Fig. 10. Operation of the SCP driver under short-circuit condition for the SiC. (a) BJT and (b) SJT. Measured base-to-emitter voltage (yellow line: 20 V/div), *enable* signal (green line 10 V/div), collector–emitter voltage (purple line: 500 V/div), collector current (pink line: 100 A/div). Time base: 100 ns/div.

B. Short-Circuit Protection of SiC Power BJTs

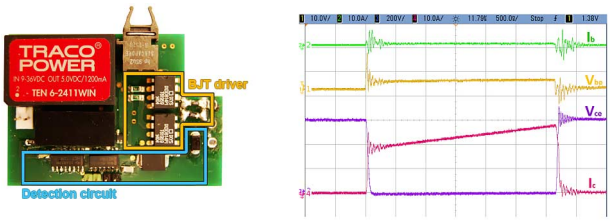
As seen in Section II, the peak fault current during a short-circuit condition is inherently limited for SiC BJTs. For a similar short-circuit duration, the SiC BJT will dissipate less energy than the SiC JFET and MOSFET. Nevertheless, there is no need to wait more than a few times the duration of a normal turn-ON to turn-OFF the short circuit. The RC filters are calibrated to achieve a short-circuit detection within 380 ns. The SiC BJT driver is the one used in Section II without modifications combined with the short-circuit detection [37].

The schematic diagram of the SCP driver for SiC BJTs is shown in Fig. 9, and its physical implementation is shown in Fig. 11(a). Additional components required for the detection circuit are also shown in the figure. In Fig. 9, M_1 and M_3 are two out of the four AND gates of a quadruple AND-gate circuit with Schmitt-trigger inputs SN74HC7001. The Schmitt trigger buffers are the single Schmitt-trigger buffer 741G17, and the flip-flop M_2 is a quad positive-edge triggered D-type flip-flop with reset 74HCT175.

The SCP driver performance during a short-circuit event is shown in Fig. 10 for both SiC BJTs and SJTs. The time delay between detection and protection T_d, the peak short-circuit current I_{peak}, as well as the short-circuit duration T_{sc} are summarized in Table IV. The undershoot of the *enable* signal is due to noise induced by the turn-OFF transients. The noise immunity

TABLE IV
SHORT-CIRCUIT PROTECTION DRIVER PERFORMANCE WITH SiC BJTs

SiC DUTs	T_d (ns)	I_{peak} (A)	T_{sc} (ns)
FSICBH017A120	380	120	450
GA50JT12-247	380	80	500



(a) (b)

Fig. 11. (a) Hardware realization of the SCP driver for SiC BJTs. (b) Double pulse test of the SiC BJT from Fairchild using the SCP driver. Measured collector–emitter voltage (purple line: 200 V/div) and collector current (pink line: 10 A/div). Time base: 50 ns/div.

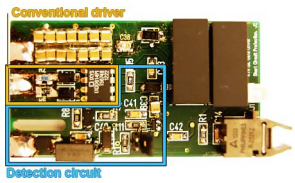


Fig. 12. Hardware realization of the SiC MOSFET driver for discrete devices and modules.

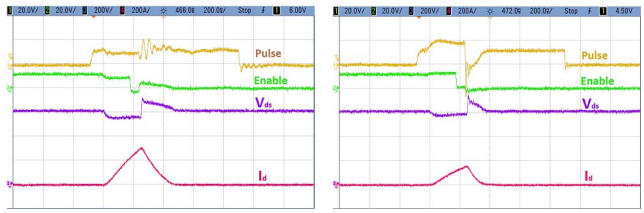
of the system is sufficiently high, such that the short-circuit fault is turned OFF safely within less than 100 ns after its detection. The operation of the SCP driver during normal operation is validated by Fig. 11(b).

C. Short-Circuit Protection of SiC Power MOSFETs

The SCP driver for SiC MOSFETs should be designed carefully for the reasons mentioned in Sections II and III. Thus, the short-circuit detection times are reduced to the minimum value allowing a small margin to avoid false triggering. The turn-OFF is slowed down by means of asymmetrical gate resistors. As for the SiC BJT, a high noise immunity is also a requirement. This is achieved by the use of a Schmitt-trigger buffer instead of a comparator. In the scope of this paper, the chosen gate resistance values are 20 Ω for turn-ON and 20 Ω for turn-OFF. These values can be tuned with regard to the final application.

The SCP driver for SiC MOSFETs is shown in Fig. 12. The schematic diagram of this realization is very close to the BJT implementation (see Fig. 9) with minor modifications. This driver has been tested in [49] in a real application for SiC MOSFET modules that have higher parasitic inductances than discrete devices. So far, no erroneous triggering of the SCP protection has been reported. In this realization, there is no real difference between driving a SiC discrete power device and a SiC power module.

The SCP driver is tested using the Cree (C2M0025120D) and Rohm (SCT2080KE) discrete devices as shown in Fig. 13. The short circuit is detected within 180 ns. The SCP driver



(a) (b)

Fig. 13. Operation of the MOSFET SCP driver under short-circuit condition for the (a) Cree and (b) Rohm devices. Measured control pulse (yellow line: 20 V/div), *enable* signal (green line: 20 V/div), drain-to-source voltage (purple line: 200 V/div), and drain current (pink line: 200 A/div). Time base: 100 ns/div.

TABLE V
SCP DRIVER PERFORMANCE WITH SiC MOSFETs

SiC DUTs	T_d (ns)	I_{peak} (A)	Overvoltage (V)	T_{sc} (ns)
C2M0025120D	180	300	150	420
SCT2080KE	180	150	150	360
CAS100H12AM1	200	750	400	360

with modified delays is also tested on a SiC MOSFET module (CAS100H12AM1 from Cree rated at 1.2 kV/100 A). The performance of the SCP driver during short-circuit conditions for the discrete devices and the module is stated in Table V. Comparing these values with the values obtained in Section II for a discrete SiC MOSFET (see Table I), the voltage overshoot has been reduced by 25% while the peak current was reduced by 40% for the Cree device. The overshoot voltage reduction is explained by the the lower current to be turned OFF. The lower current peak is explained by the shorter short-circuit duration. The SCP driver turns OFF the fault within 450 ns for both Cree and Rohm devices. The SCP driver was also tested during normal operation. For the sake of brevity, the double-pulse test is not shown here.

D. Short-Circuit Protection of SiC Power JFETs

The short-circuit protection of SiC JFETs is very similar to one of the SiC MOSFETs. The chosen power stage of the SiC JFET driver is the DRC network [35] with a −30-V power supply. Even though this driver topology speeds up the turn-ON and turn-OFF, the overvoltage of 200 V is judged to be within the reliability margin, since the peak overvoltage is 800 V. Moreover, the DRC network provides a stiff negative voltage to the gate at turn-OFF. The hardware realization of the SiC JFET SCP driver is presented in Fig. 14(a).

Fig. 14(b) shows the operation of the SCP driver with the normally ON JFET UJN1205K from USCi. The short circuit is turned-OFF within 610 ns after the turn-ON, which is a reasonable value since the JFET is known to be the most robust SiC device in terms of short-circuit durability (> 20 µs).

V. DISCUSSION

In Section II, it was found that all three SiC transistors had a V_{ds} that remained high during the short-circuit event. However,

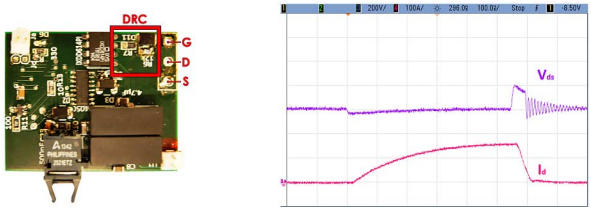


Fig. 14. Operation of the JFET SCP driver under short-circuit condition. (a) Hardware realization of the driver. (b) Measured drain-to-source voltage (purple line: 200 V/div) and drain current: 100 A/div. Time base: 100 ns/div.

the different devices had different behaviors with respect to the current and overvoltage during the turn-OFF of a short circuit. From this point of view, the BJT was superior to the other devices, and the MOSFET was found to exhibit the highest current peaks and overvoltages among the devices. In the MOSFET case, it may be advantageous to have a separate slow-switching turn-OFF procedure in case of short circuit to prevent excessive overvoltages during turn-OFF. For all cases, a fast detection is possible since the short circuit can be clearly differentiated from the normal operation. As discussed in Section III, short-circuit events should be turned OFF as soon as possible to avoid unnecessary heating which may compromise the device integrity. The latter is particularly important regarding the SiC MOSFET whose oxide layer may be sensitive to overheating. Consequently, if the protection integrated in the driver is able to limit the fault duration, a larger number of short-circuit events can be endured by the SiC transistor before an impact on its characteristics can be detected.

In the previous section, designed rules toward an SCP driver improving the system reliability and availability have been presented. According to these rules, three different SCP drivers were designed and evaluated for different kinds of SiC devices. A selective and fast detection was implemented using the desaturation method and Schmitt-trigger gates for noise immunity. It was shown to be reliable, even in a fast-switching environment. The detection speed is of 180 ns. The protections have successfully been tested under short-circuit conditions as well as in a double-pulse test. For the SiC Rohm MOSFET, the short circuit was turned-OFF in 360 ns and for the SiC Cree MOSFET in 420 ns.

In state-of-the-art SiC converters, it is not uncommon that discrete devices or modules are placed in parallel [36], [48]–[51]. In such cases, each device could have a separate driver if fast-switching transients are targeted. If every driver is equipped with a short-circuit detection, the protection will probably be faster than if only one detection circuit for the whole switch position is used. The reason for this is that the current is likely to be unevenly shared among the parallel-connected devices. Since both the *enable* and *error* signals are available on the driver, a fault can be reported to the main control circuitry.

An important aspect on how to tune the delays of the detection circuit is to match those to the waveform of the turn-ON transient of the specific application. Special care has to be taken on this aspect if the load exhibits significant capacitive currents at turn-ON, as, for instance, a motor winding [52], [53]. If the detection delay is too short, even normal transients may erroneously be detected as short circuits.

VI. Conclusion

In this paper, the short-circuit behaviors of SiC MOSFETs, SiC JFETs, and SiC BJTs have been presented. A transient thermal device simulation was performed for the SiC MOSFET revealing that the hottest temperature is located 2 μm below the oxide layer. After 500 ns, this point reaches a temperature of 267 °C. The analysis of the behavior led to guidelines toward the design of a selective and fast short-circuit detection and protection. The fastest detection speed was 180 ns. This value includes the delays considered to avoid erroneous triggering of the short-circuit protection. One driver for each device-type is presented and tested. The experimental results show that the drivers have the capability to clear a short-circuit fault within less than 600 ns for all three devices investigated (360 and 420 ns for MOSFETs, 500 ns for BJT, 600 ns for JFET). For all SiC device-types, the proposed short-circuit protection can easily be integrated in custom driver designs.

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