# A New, Continuous-Time Model For Current-Mode Control

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*Abstract*—**The accuracy of sampled-data modeling is combined with the simplicity of pole-zero representation to give a new current-mode control model, accurate to half the switching frequency. All of the small signal characteristics of current-mode control are predicted, including high-frequency subharmonic oscillation which can occur even at duty cycles of less than 0.5. The best representation for the control-to-output transfer function is shown to be third-order. Model predictions are confirmed with measurements on a buck converter.**

## I. Introduction

CURRENT-mode control has been used in switching power supplies for many years. Numerous attempts have been made to characterize this control system with small-signal models, all with limited degrees of accuracy or usefulness. Some continuous-time models [1]–[3] provide low-frequency models for the system, but they need to address the well-known phenomenon of current-loop instability as a separate issue. Other models [4] have attempted to explain this instability through a modulator gain model, but predictions are not confirmed by measurements. Conclusions based on this model presented in [5] give misleading information about the design of current-mode systems. Exact discrete-time and sampled-data models [6], [7] can accurately predict responses, but they provide very little design insight due to their complex formulations.

In this paper, the accuracy of sampled-data modeling is combined with the simplicity of the model of the three-terminal PWM switch [8] to provide a complete model which accurately predicts characteristics from dc to half the switching frequency. It is shown that an approximation to sampled-data results can provide a simple, accurate model with a finite number of poles. Feedforward gain terms from voltages applied across the inductor during on and off times of the power switch are derived to complete the analysis. Experimental results are presented to confirm the validity of the new model.

## II. Review of Voltage-Mode Control Model

Recent advances in analysis [8] have provided a flexible small-signal model which replaces the nonlinear switching action of the converter with a simple equivalent circuit. This small-signal circuit remains invariant in the different PWM converters and is easy to use. Fig. 1 shows the invariant PWM three-terminal switch model developed in [8]. The voltage source is determined by the steady-state dc voltage across the active and passive terminals, and by the duty cycle of the power stage.

Manuscript received May 5, 1990; revised November 8, 1990. The original version of this paper was presented at the 1989 Power Conversion and Intelligent Motion Conference, Long Beach, CA, October 16–20.

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IEEE Log Number 9042329.

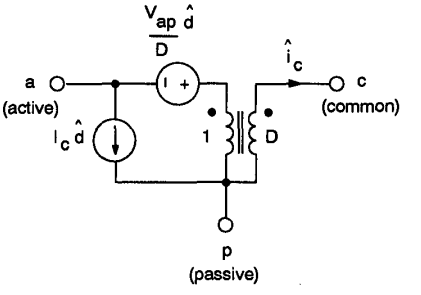


Fig. 1. PWM three-terminal small-signal switch model. Model can be used for all two-switch PWM converters operating in the continuous conduction mode. Source quantities $V_{ap}$, $I_c$, and $D$ are determined by dc operating conditions of the power stage.

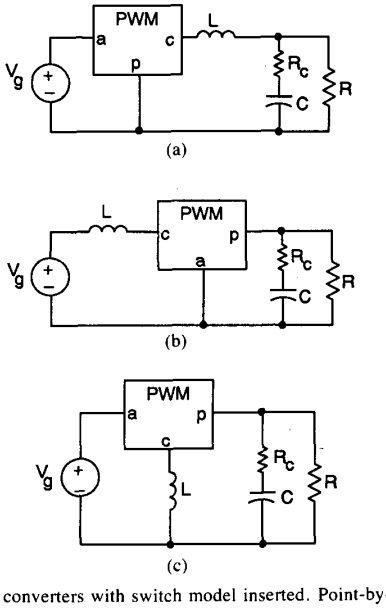


Fig. 2. PWM converters with switch model inserted. Point-by-point substitution of model of Fig. 1 gives complete power stage small-signal model for the (a) buck, (b) boost, and (c) flyback converters.

The current source is determined by the steady-state dc current, $I_c$, out of the common terminal of the three-terminal model. These quantities will depend upon the input voltage, output voltage, and steady-state inductor current of the converter in which the model is placed. Fig. 2 shows the PWM switch model configured for the buck, boost, and flyback circuits. Point-by-point substitution of the model of Fig. 1 into the PWM block gives the small-signal model of the power stage.

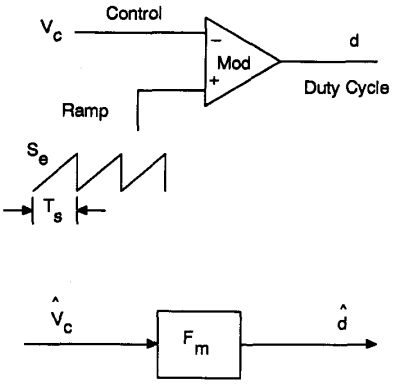


Fig. 3. Naturally-sampled duty-cycle modulator. Naturally-sampled modulator for single-loop control, consisting of sawtooth ramp waveform intersecting voltage reference, is modeled with simple gain block, $F_m$.

The duty cycle, $d$, for control of the converter is typically generated with a control voltage and a reference ramp clocked at the desired switching frequency. A naturally-sampled duty cycle modulator is shown in Fig. 3. A sawtooth ramp of slope $S_e$ intersects a control voltage, $v_c$, to produce the control parameter duty cycle, $d$. The small-signal model for this modulator has been found [9] to be

$$F_m = \frac{\hat{d}}{\hat{v}_c} = \frac{1}{S_e T_s} \tag{1}$$

where $T_s$ is the switching period. The model in Fig. 2, when combined with the duty-cycle modulator gain, $F_m$, gives small-signal transfer functions which can be shown experimentally to be accurate to half the switching frequency.

## III. Current-Mode Control Model

Fig. 4 shows a current-mode control modulation scheme. A constant-frequency clock initiates the on time of the switch, and the modulator ramp, provided by the sensed current, intersects a threshold to turn the switch off. An external ramp is added to the current waveform to provide design flexibility and stabilize the current feedback loop [1]–[4]. If the combined modulator slope, given by the sum of the external ramp and the current ramp, is the same as for voltage-mode control, the modulator gain for current-mode control remains the same as for voltage-mode control. The modulator gain of the circuit is then

$$F_m = \frac{1}{(S_n + S_e)T_s} = \frac{1}{m_c S_n T_s} \tag{2}$$

where

$$m_c = 1 + \frac{S_e}{S_n} \tag{3}$$

and $S_n$ is the on-time slope of the current-sense waveform. This modulator gain is different from that found in [1] and [4], resulting in very significant changes to the models. The power stage model, of course, is not affected by the presence of a different control circuit. Gain terms which model the action of the control circuit only should account for all the phenomena of current-mode control.

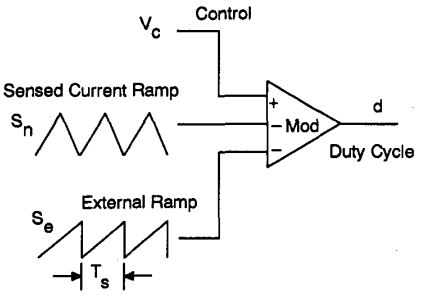


Fig. 4. Current-mode control modulator. Ramp of sensed current signal is summed with sawtooth ramp, and compared with reference voltage to control duty cycle.

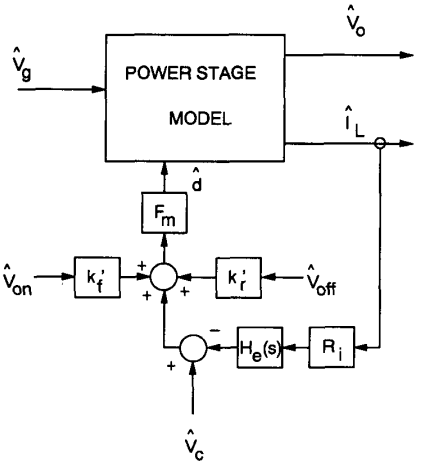


Fig. 5. Complete small-signal model for current-mode control. Appropriate power stage model from Fig. 2 is used. Feedback paths, $k_f'$ and $k_r'$, are created by closing current feedback path. Gain block $H_e(s)$ represents sampling action of the converter. Exteranl ramp added to circuit only affects modulator gain, $F_m$.

Fig. 5 shows a complete block diagram for PWM circuits with current-mode control. The power stage model remains the same as that in Fig. 2, and gain blocks $R_i$ and $H_e(s)$ represent the current feedback. $R_i$ is the linear gain of the current-sense network, and $H_e(s)$ will be used to model the sampling action of current-mode control. As will be seen later, proper approximation for this sampling block results in a powerful new small-signal model. Gains $k_f'$ and $k_r'$ provide feedforward of voltages across the inductor during the on and off-times of the converter, respectively. These gain paths are created by feedback of the inductor current, the slope of which depends upon the voltages applied to the inductor. The voltages $v_{on}$ and $v_{off}$ are, in general, linear combinations of other voltages in the circuit. Earlier models [1], [4] used feedforward from input and output voltages of the converters. This can yield the same results, but the model then changes for each different topology. The method used in this paper produces invariant gains for any converter.

The model of Fig. 5 remains the same for either current-mode control and for voltage-mode control. With no current feedback, $R_i = 0$, and the effect of the current loop and gain blocks $k_f'$ and $k_r'$ are zero. This provides great convenience in circuit modeling; a single circuit model can be used, regardless of control scheme.

## IV. Sampled-Data Current-Feedback Transfer Function

The power stage model of Fig. 2 provides accurate transfer functions with voltage-mode control without the need for any discrete-time or sampled-data modeling. However, current-mode control exhibits characteristics which can only be explained with discrete-time modeling. It is not necessary to attempt to model the complete power stage with discrete-time or sampled-data analysis. Only the current-sampling function needs to be modeled, and then converted into continuous-time representation and combined with the rest of the power stage and feedback models. The purpose of this section is to find the sampling gain, $H_e(s)$, of the model of Fig. 5.

For discrete-time analysis, the voltages applied across the inductor are kept constant, and the control-to-inductor current transfer function is derived with the current-feedback loop closed. This transfer function is independent of converter topology. With the inductor voltages fixed, the circuit shown in Fig. 6 results for all converters which can be modeled with the PWM switch. (For two-state converters, keeping the inductor voltages constant corresponds to fixing the input and output voltages of the converter.) Fig. 7 shows the sensed inductor current waveforms, scaled by feedback resistor $R_i$, with fixed voltages for constant-frequency control, with the clock initiating the on-time of the power switch. The solid line represents the steady-state condition, and the dashed line shows the perturbed waveform.

Fig. 7(b) shows the exact instantaneous perturbation of the inductor current from the steady-state condition, Fig. 7(c) shows the approximate equivalent sample-and-hold system waveforms. The only difference in the actual perturbation and the equivalent sample-and-hold system is a slight variation in the sampling instant, and a finite slope in the exact current. These differences are minor, and the constant-frequency current-mode control system can be considered a sample-and-hold system with the sampling instant occurring at the intersection of the current signal and the reference waveform.

The discrete-time equation describing the equivalent sample-and-hold function is

$$\hat{i}_L(k+1) = -\alpha \hat{i}_L(k) + \frac{1}{R_i}(1+\alpha)\hat{v}_c(k+1) \qquad (4)$$

where

$$\alpha = \frac{S_f - S_e}{S_n + S_e} \qquad (5)$$

The $z$-transform of (4) is given by

$$H(z) = \frac{\hat{i}_L(z)}{\hat{v}_c(z)} = \frac{1}{R_i}(1+\alpha)\frac{z}{z+\alpha} \qquad (6)$$

Notice that, with $S_n < S_f$ and no external ramp, the value of $\alpha$ is greater than unity, and the discrete-time system has a pole outside the unit circle. This explains the system instability at duty cycles greater than 0.5. However, the subharmonic instability can occur even at duty cycles lower than 0.5 when feedback compensation is added to the system, and this is discussed later.

The transformation of a first-order sample-and-hold system from discrete-time into continuous time is analyzed thoroughly in [10]. The continuous-time representation of the sample-and-hold circuit can be found from the $z$-transform expression by using the substitution $z = e^{sT_s}$, and multiplying by $1/sT_s$ ($1 - e^{-sT_s}$). The continuous-time representation of Eq. (6) is then given by

$$H(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s}-1}{e^{sT_s}+\alpha}. \qquad (7)$$

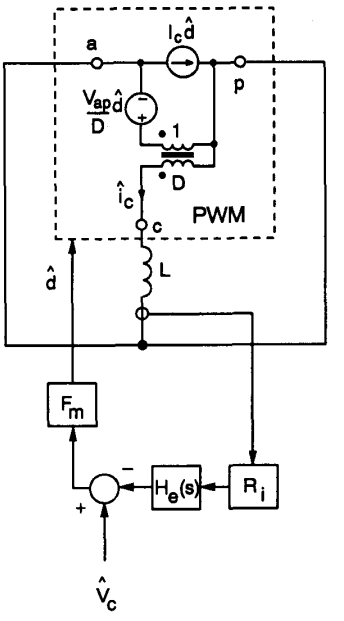


Fig. 6. Small-signal model for all power stages with fixed voltages. When voltages applied to inductor during on-time and off-time of power switch are fixed, current-mode model reduces to this simple form, common to all converters which can be modeled with PWM switch model.

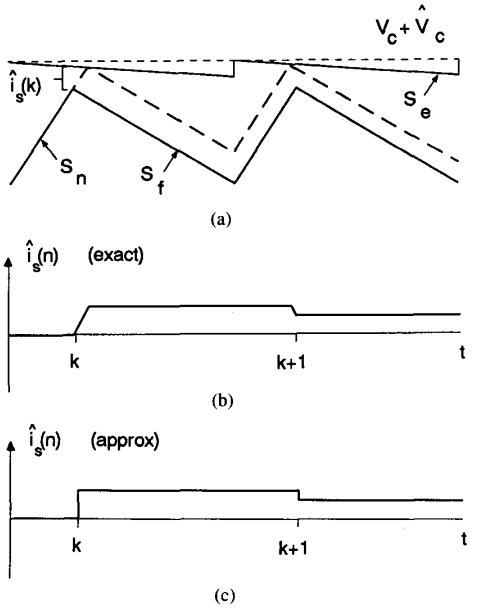


Fig. 7. Current-mode control modulator waveforms. Conditions for change in control voltage, $v_c$ are shown. Sensed current, $i_s$, is equal to the inductor current, $i_L$, scaled by the feedback network, $R_i$. Steady-state current-sense waveform is shown in solid lines, and transient response is shown in dashed lines. Fig. 7(b) plots exact perturbation from steady-state current waveform, and Fig. 7(c) shows equivalent first-order sample-and-hold system.

Equation (7) is now used with the circuit model of Fig. 6 to find the open-loop sampling gain, $H_e(s)$. All of the other gains of Fig. 6 are defined, and the power stage model is the same as for voltage-mode control. The analysis, presented in detail in Appendix I, results in:

$$H_e(s) = \frac{sT_s}{e^{sT_s} - 1}. \tag{8}$$

It can be shown that this sampling gain is actually invariant for all converters using constant frequency, constant on-time, or constant off-time control [15]. This invariant equation can now be approximated to give a simple model.

## V. Continuous-Time Approximation to Sampled-Data Model

The sampled-data model has been realized before [6] for the high-frequency portion of the current-loop of just the buck converter, but it has never been exploited to its full potential. The exact continuous-time model of (8) has an infinite number of poles and zeros [6]. Since such a representation is not useful for design and analysis, applications of the sampled-data model have been limited.

Attempts to model all of the poles of the sampled-data model in (8) are neither necessary nor useful. In fact, it is only necessary to accurately model the sampled-data expression up to half the switching frequency. A complex pair of RHP zeros provides an accurate representation of the transfer function $H_e(s)$. This second-order model of the sampled-data system can be chosen to match the exact equation at the lower and upper limits of the frequency range of interest, from dc to half the switching frequency. The transfer function of this second-order model is

$$H_e(s) \simeq 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{9}$$

where

$$Q_z = \frac{-2}{\pi} \tag{10}$$

and

$$\omega_n = \frac{\pi}{T_s}. \tag{11}$$

Fig. 8 is a plot of the exact sampled-data model of (8) and the approximate second-order model of (9)–(11). It can be seen that the approximate model is exact at dc and half the switching frequency, and deviates by less than 0.2 dB and 3 degrees at frequencies in between.

This new model gives the possibility of transfer functions which have more zeros than poles, as will be seen when the current loop gain is derived. The reason for this apparent anomaly is the choice of a model which is good only to half the switching frequency. If the model is extended to higher frequencies, more poles will be needed for accurate modeling of $H_e(s)$, and the number of zeros will not be greater than the number of poles. The extra zeros in the current feedback loop will cause additional poles in the closed-loop transfer functions, leading to the significant differences and usefulness of the new model.

## VI. Complete Continuous-Time Model

The new current-mode control model of Fig. 5 can now be completed with the derivation of gains $k_f'$ and $k_r'$. The average

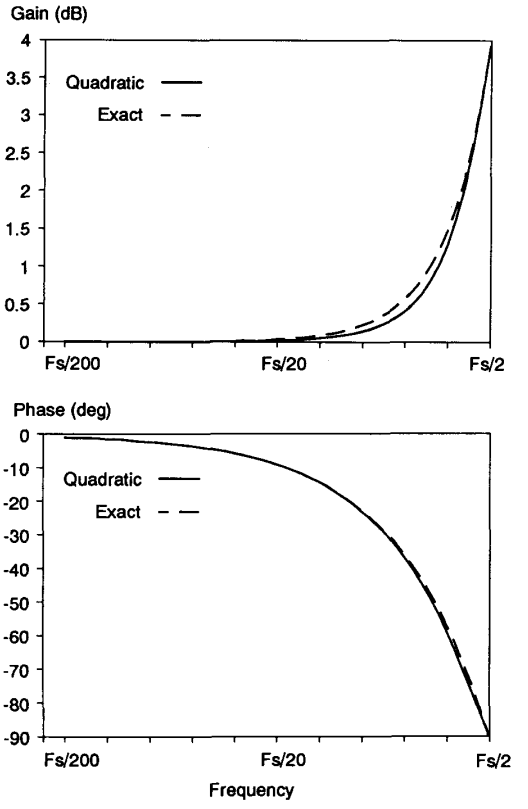


Fig. 8. Exact sampled-data model and quadratic approximation. Exact and approximate expressions match exactly at dc and half switching frequency, and differ by less than 0.2 dB and 3 degrees at all frequencies in between. Current loop gain is very accurately modeled, therefore, by transfer function which has pair of complex RHP zeros at half switching frequency, in addition to usual poles and zero of current loop.

inductor current of the circuit, used in the power stage model, is related to the instantaneous current, used in the modulator, through the current ripple. The current ripple is affected by both the voltage applied to the inductor during the on-time and the off-time of the circuit. The feedforward gains, $k_f'$ and $k_r'$, are used to model this dependence. Referring to the steady-state waveforms of Fig. 7, the describing function for the inductor current is given by

$$R_i \langle i_L \rangle = V_c - DT_s S_e - \frac{S_f D' T_s}{2}. \tag{12}$$

The quantity $\langle i_L \rangle$ denotes the average value of inductor current under steady-state conditions. This equation can be perturbed, assuming the off-time inductor voltage is constant, to obtain the dependence of inductor current on the on-time voltage. The gains of Fig. 5 can then be substituted to give the desired results for the gain $k_f'$. This derivation is performed in detail in Appendix II. (12) can also be perturbed, with the on-time voltage constant, to obtain the dependence of inductor current on the off-time voltage. The gains of Fig. 5 can then be substituted to give the desired value of $k_r'$. The values of both $k_f'$ and $k_r'$ are presented in Table I, together with a summary of the other parameters of the new current-mode control model. This model can now be used for accurate analysis and design.

TABLE I
SUMMARY OF GAIN PARAMETERS OF FIG. 5

| | |
|---|---|
| $k_f'$ | $-\frac{DT_sR_i}{L}\left[1-\frac{D}{2}\right]$ |
| $k_r'$ | $\frac{D'^2T_sR_i}{2L}$ |
| $F_m$ | $\frac{1}{(S_n+S_e)T_s}$ |
| $H_e(s)$ | $1+\frac{s}{\omega_n Q_z}+\frac{s^2}{\omega_n^2}$ |
| | $Q_z=\frac{-2}{\pi} \quad \omega_n=\frac{\pi}{T_s}$ |

## VII. TRANSFER FUNCTIONS OF NEW MODEL

### A. Buck Converter Example

The benefits and features of the new small-signal model are clearly demonstrated with an example. The buck converter shows some of the most interesting characteristics with current-mode control, so this converter was modeled, with the following parameters:

$$V_g = 11\text{ V} \qquad V_o = 5\text{ V}$$
$$L = 37.5\ \mu\text{H} \qquad C = 400\ \mu\text{F} \qquad R = 1\ \Omega$$
$$R_c = 14\ \text{m}\Omega \qquad R_i = 0.33\ \Omega \qquad T_s = 20\ \mu\text{s}.$$

The small-signal parameters of the three-terminal switch and current-mode model can be calculated from

$$I_c = \frac{V_o}{R} = 5\text{ A} \qquad V_{ap} = V_g = 11\text{ V} \qquad D = 0.45$$
$$k_f' = -0.0614 \qquad k_r' = 0.0266.$$

The small-signal model of Fig. 5 was built with a PSpice [13] file (see Appendix III for details), using the above circuit parameters. The second-order approximation of the sampling block, $H_e(s)$, in (9), was easily built in PSpice using a simple operational amplifier network. The PSpice model was used to generate all of the transfer functions in this section of the paper.

### B. Current Loop Gain

The first transfer function of interest is the current-loop gain measured at the output of the duty-cycle modulator feedback, and will show the cause of subharmonic oscillation. Fig. 9 shows a plot of the current-loop gain with different values of external ramp. For the case with no external ramp ($m_c = 1$), it can be seen that there is very little gain margin or phase margin in this loop. If the duty cycle increases further, the gain increases and the system becomes unstable at $D = 0.5$. The shape of the gain and phase curves do not change with added external ramp. Even with low current feedback ($m_c = 8$), there is significant gain at the filter resonant frequency, and other transfer functions of the converter will be considerably altered from those obtained for voltage-mode control.

It can be shown that the gain blocks $k_f'$ and $k_r'$ have little effect on the current-loop gain. Ignoring these gains, the approximate current-loop gain of the buck converter is

$$T_i(s) \simeq \frac{L}{RD'T_sm_c}\,\frac{1+sCR}{\Delta(s)}\,H_e(s). \tag{13}$$

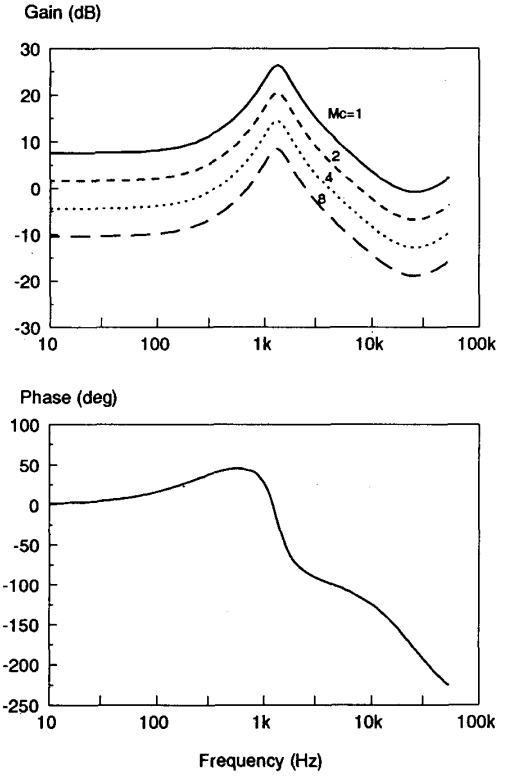


Fig. 9. Buck converter current-loop gain. Two RHP zeros at half switching frequency are apparent in figure. Gain increases after this frequency, while phase drops down additional ninety degrees. If insufficient ramp is added, there is very little phase margin in loop gain.

The demonimator $\Delta(s)$ is the familiar power stage transfer function denominator given by

$$\Delta(s) = 1 + \frac{s}{\omega_o Q_p} + \frac{s^2}{\omega_o^2} \tag{14}$$

where

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{15}$$

and

$$Q_p = \frac{1}{\omega_o\left[\frac{L}{R}+CR_c\right]}. \tag{16}$$

This current-loop gain expression differs significantly from conventional averaged models [1]–[4]. The complex RHP zeros give an extra ninety degrees phase delay at half the switching frequency. Furthermore, it can be seen that the maximum crossover frequency before the system goes unstable is half the switching frequency, which is consistent with Nyquist sampling theory.

### C. Control-to-Output Gain

A new control-to-output-voltage transfer function is created when the current loop is closed, and the implications of the new model for current-mode control are profound. Fig. 10 shows a

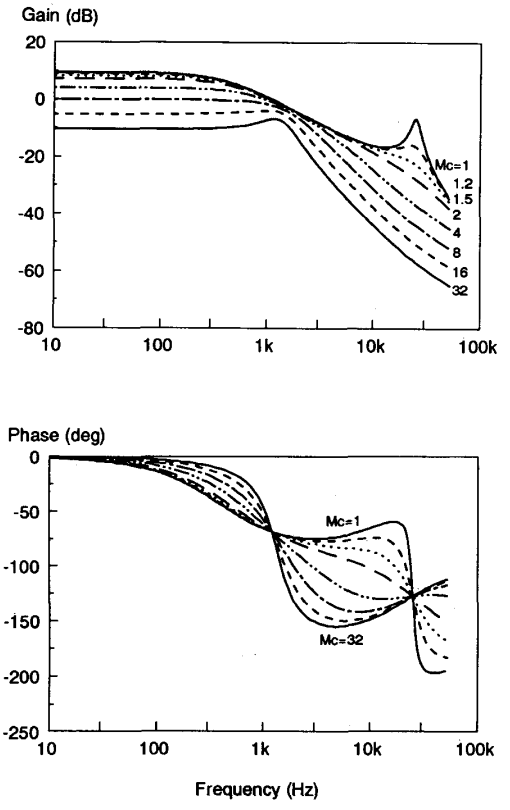


Fig. 10. Control-output transfer function for buck converter. Plot shows transition from current-mode control to voltage-mode control as more external ramp, $S_e$, is added. Curve for $m_c = 1$ has no added external ramp, and high-Q double pole at half switching frequency is apparent. As more ramp is added, double pole is damped, and eventually splits into two real poles. One of these poles then merges with low-frequency pole to form the $LC$ filter double pole of voltage-mode control, and other moves out beyond half switching frequency.

plot of this transfer function for a converter with different values of external ramp, operating with a 0.45 duty cycle. The accurate representation of the system is neither first-order, as suggested in [2], [3], or second order, as suggested in [1], [4], but third order. Furthermore, the significant peaking that can occur at half the switching frequency when no external ramp is used means that the effect of the complex poles needs to be considered even with low crossover-frequency systems. If an integral-and-lead network were added to the system shown in Fig. 10 with a value of $m_c = 1$, the maximum crossover frequency without instability would be about 3 kHz. This is a significant feature of the new model. It clearly shows how subharmonic oscillation can occur, even at duty cycles of less than 0.5, when voltage-loop compensation is added. This effect was noted in [12], but was not quantified.

The new model highlights the role of the external ramp, which is used to control the Q of the second-order pole at half the switching frequency. A small external ramp results in high peaking of the control transfer function. When compensation is added to the control, this peaking will determine the maximum crossover frequency before subharmonic oscillations occur.

The approximate control-to-output transfer function for the buck converter with current-mode control is given by

$$\frac{\hat{v}_o}{\hat{v}_c} \simeq \frac{R}{R_i} \frac{1}{1 + \frac{RT_s}{L}[m_c D' - 0.5]} F_p(s) F_h(s) \tag{17}$$

where

$$F_p(s) = \frac{1 + sCR_c}{1 + \frac{s}{\omega_p}} \tag{18}$$

where

$$\omega_p = \frac{1}{CR} + \frac{T_s}{LC}(m_c D' - 0.5) \tag{19}$$

and

$$F_h(s) = \frac{1}{1 + \frac{s}{\omega_n Q} + \frac{s^2}{\omega_n^2}} \tag{20}$$

where

$$Q = \frac{1}{\pi(m_c D' - 0.5)}. \tag{21}$$

It is interesting to note that the transfer function defined by (20)–(21) is common to all converters. The approximate control-output transfer function is very useful for design purposes. (21) allows suitable choice of external ramp to prevent peaking at half the switching frequency. The simple form of (21) makes the choice of external ramp very straightforward for any PWM converter with current-mode control.

### D. Audio Susceptibility

The audio susceptibility of the buck converter shows one of the most interesting properties of current-mode control. Since the gain term, $k_f'$, has a negative value, it is possible to completely null the circuit response to input-voltage perturbations with a suitable choice of external ramp. The null in audio susceptibility occurs with an external ramp value $S_e = S_f/2$. The theoretical value of this nulling ramp confirms the empirical observations in [3] that the audio susceptibility can be made to be zero. Fig. 11 shows a plot of the audio susceptibility of the buck converter as external ramp is added. The audio decreases until the null value of external ramp is reached, then increases with the addition of further ramp. Choosing the external ramp to null the audio susceptibility can be useful for applications where output noise is extremely critical. However, the audio susceptibility is very sensitive to changing values of the external ramp around this null value, and it can be difficult to obtain a precise null. The approximate audio transfer function for the buck converter is

$$\frac{\hat{v}_o}{\hat{v}_g} = \frac{D[m_c D' - (1 - D/2)]}{\frac{L}{RT_s} + (m_c D' - 0.5)} F_p(s) F_h(s) \tag{22}$$

where $F_p(s)$ and $F_h(s)$ are given in (18) and (20), respectively.

### E. Output Impedance

Closing the current feedback loop has a strong effect on the output impedance of the converter. With high current feedback, the output impedance of the buck converter looks like the impedance of just the load capacitor and resistor. The signifi-

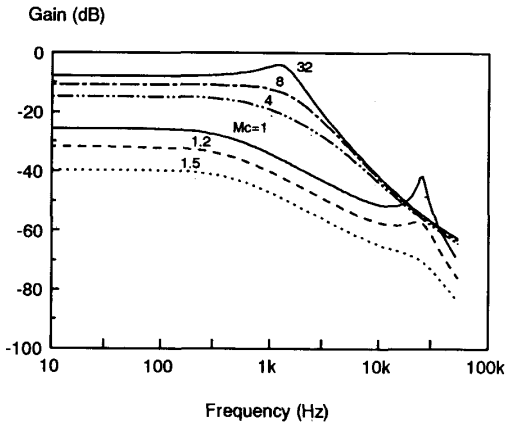


Fig. 11. Audio susceptibility of the buck converter. Plot shows transition from current-mode control to voltage-mode control, as more external ramp, $S_e$, is added. Double pole at half switching frequency is again apparent. Buck converter audio is special case where input voltage perturbation can actually be nulled by addition of external ramp. This is due to the feedforward term, $k_f'$. Audio is very sensitive function of external ramp around null value $S_e = S_f/2$.

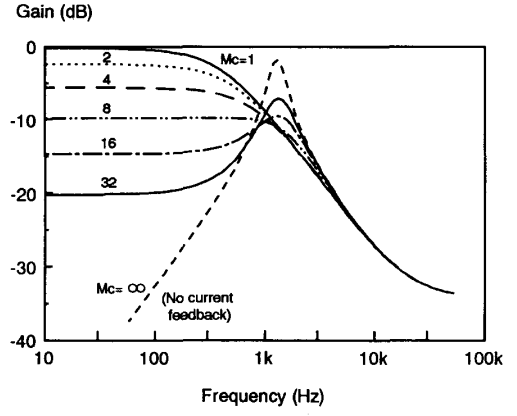


Fig. 12. Output impedance of the buck converter. Plot shows effect on output impedance as more external ramp, $S_e$, is added. Current-mode control gives high output impedance at low frequency, but has no peaking at filter resonance frequency. Even at very low levels of current feedback, $M_c = 32$, there is strong effect on low-frequency output impedance.

cant differences from the output impedance of the open-loop converter are the high dc value, and the absence of any resonant peaking. Fig. 12 shows the output impedance of the buck converter with different values of $m_c$. Even with low levels of current feedback, there is a significant effect on low-frequency asymptote and damping of the $LC$ filter resonance.

The approximate output impedance transfer function for the buck converter is

$$Z(s) \simeq \frac{R}{1 + \frac{RT_s}{L}(m_c D' - 0.5)} F_p(s). \qquad (23)$$

For a converter operating deep in the continuous-conduction region, the first term of this expression reduces to just the load resistor, $R$.

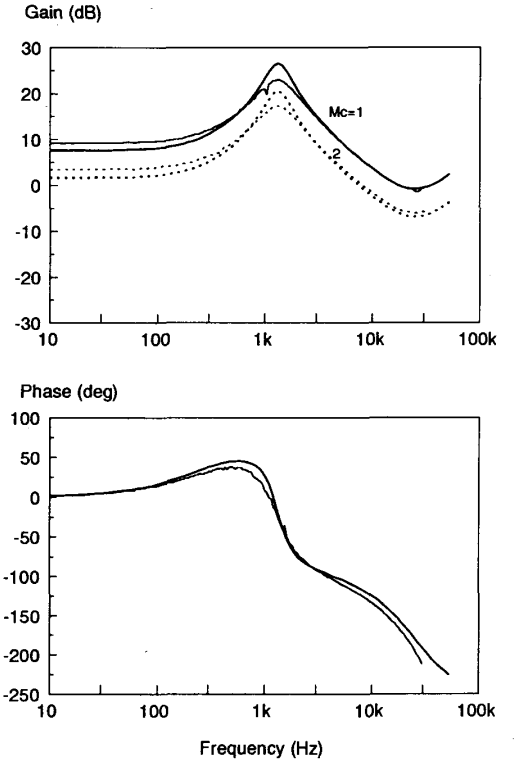


Fig. 13. Buck converter current-loop gain measurements. Except for small discrepancies in low-frequency gain and lower $Q$ at filter resonant frequency, theoretical and measured gain agree very well. Measured and predicted phase are also very close.

## VIII. Experimental Verification

A converter was built with the same component values as those given for the example in the previous section. It was necessary to increase the input voltage to 14 V to achieve a duty cycle of 0.45. Circuit inefficiencies and semiconductor voltage drops, not modeled in the analysis, accounted for the increased input voltage. All of the approximate expressions of the previous section are function of duty cycle, not input voltage, so the change in input voltage does not introduce discrepancies between measurements and predictions.

The measured and predicted current loop gains for $m_c = 1$ (no external ramp) and $m_c = 2$ are shown in Fig. 13. Both the gain and phase measurements agreed very well with predictions up to half the switching frequency. It is important to point out that a digital modulator [11] was used to measure the loop gain. This ensures that the correct sampled-data loop gain is obtained [12], and that all the feedback paths created by the current loop are measured. All other measurements in this section were performed with conventional analog measurement techniques.

The control-to-output-voltage transfer function, measured with the current loop closed, is shown in Fig. 14. The gain and phase measurements again show very good correlation with the theoretical results. The peaking of the gain at half the switching frequency clearly shows the existence of two complex poles. This control-to-output measurement allows the voltage feedback compensation to be properly designed, and the onset of subharmonic oscillation can be predicted.

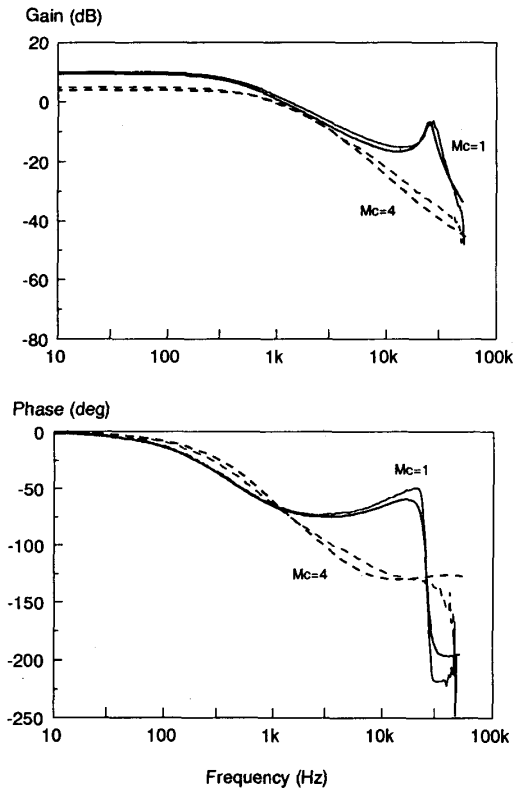


Fig. 14. Control-output transfer measurements for buck converter. Effect of second-order poles is clearly shown in experimental measurements when no external ramp is used.

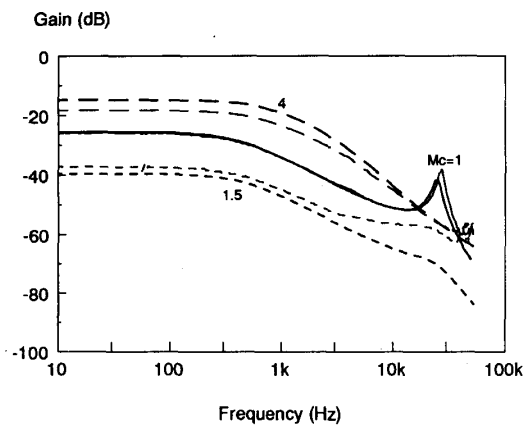


Fig. 15. Audio susceptibility measurements of the buck converter. Experimental results show reduction in audio as external ramp is increased from zero, then an increase as more than nulling value is added. Measurements below −55 dB were very difficult to obtain, and this is reason for discrepancies at high frequencies with $m_c = 1.5$.

The measurements of audio susceptibility are shown in Fig. 15. The theory and experiment agree very well with no external ramp, but measurements were difficult to obtain as the audio susceptibility became lower with more external ramp. Higher frequency measurements below −55 dB were unreliable, due to noise and grounding problems. However, the nulling effect of the external ramp was experimentally verified, with the audio susceptibility decreasing to a very low minimum value, then increasing again with more external ramp. The measurements were extremely sensitive around the value $m_c = 1.5$, with small variations in the ramp causing large changes in the audio susceptibility. The phase of the audio measurement, not shown in this figure, flipped by −180 degrees as the external ramp increased through its null value. This switch in polarity of the audio is predicted by the audiosusceptibility expression of (22).

The measured and predicted output impedance shown in Fig. 16, agreed well with external ramp added to give values of $m_c$ from 1 to 4. The second-order poles at half the switching frequency are not apparent in this measurement.

## IX. Conclusion

A new current-mode control model which is accurate at frequencies from dc to half the switching frequency has been described for constant-frequency operation. Using simple pole-zero transfer function, the model is able to predict subharmonic oscillation without the need for discrete-time $z$-transform models. The accuracy of sampled-data modeling is incorporated into the new model by a second-order representation of the sampled-data transfer function which is valid up to half the switching frequency.

Several new observations are shown about converter systems with current-mode control. The current loop gain has a pair of complex RHP zeros which cause the instability in this loop when the external ramp is too small. The control-to-output transfer functions of two-state converters are best modeled by a three-pole expression. Two of these poles are at half the switching frequency, with high Q when no external ramp is used. The peaking at this frequency can be damped with the addition of external ramp, which eventually splits the poles on the real axis.

The new model can easily be built into any circuit analysis program such as PSpice, and can be used to show the transition from current-mode to voltage-mode control as the external ramp of the system is increased. Predictions of current loop gain, control-to-output, output impedance, and audio susceptibility transfer functions were confirmed with measurements on a buck converter. The audio susceptibility of the buck converter can be nulled with the appropriate value of external ramp.

Modeling in this paper concentrates on constant-frequency PWM converters, but the methods can be applied to variable-frequency control, and discontinuous conduction mode [15].

## Appendix I
## Derivation of $H_e(s)$

The control-to-inductor-current transfer function, with the current feedback loop closed, and with fixed voltages across the inductor, can be found from the circuit diagram of Fig. 6 to be

$$H(s) = \frac{\hat{i}_L(s)}{\hat{v}_c(s)} = \frac{F_m F_i}{1 + F_m F_i R_i H_c}. \tag{24}$$

The current gain, $F_i$, is the duty-cycle-to-inductor-current transfer function, found by inserting the PWM switch model in the power stage block. With fixed voltages, this gain can be expressed for all converters as

$$F_i = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{1}{R_i} \frac{S_n + S_f}{s}. \tag{25}$$

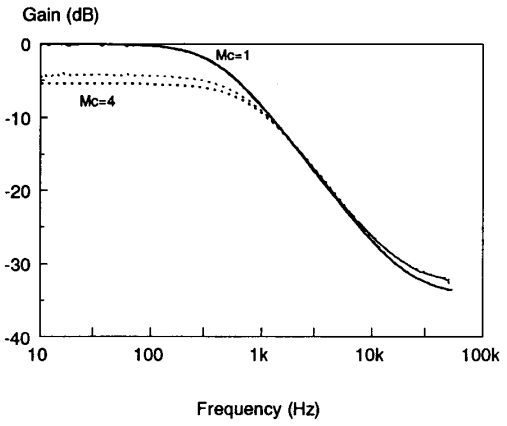


Fig. 16. Output impedance measurements of the buck converter. Measured and predicted results agree well, showing first-order response of output impedance with no resonant peaking.

When this expression is combined with the modulator gain of (2), we obtain

$$F_m F_i = \frac{1}{(S_n + S_e)T_s}\frac{1}{R_i}\frac{S_n + S_f}{s} = \frac{1}{R_i}\frac{1+\alpha}{sT_s} \tag{26}$$

where $\alpha$ is defined in (5).

The control-to-inductor-current transfer function was also derived in (7). Setting the two expressions for this transfer function to be equal, we obtain

$$\frac{F_m F_i}{1 + F_m F_i R_i H_e} = \frac{1}{R_i}\frac{1+\alpha}{sT_s}\frac{e^{sT_s} - 1}{e^{sT_s} + \alpha}. \tag{27}$$

Substitution of $F_m F_i$ into this equation allows us to solve for $H_e(s)$, yielding the result given in (8).

## Appendix II
## Derivation of $k_f'$ and $k_r'$

The steady-state waveforms of the current-mode system give the describing function for the average inductor current expressed in (12). In this expression, the duty cycle, $D$, and the off-time slope, $S_f$, are generally functions of the voltage applied across the inductor during on- and off-times. The steady-state, small-signal dependence of the average inductor current on the on-time voltage can be found by differentiating (12) with respect to this voltage. Differentiation and rearrangement of the result yields

$$\frac{\langle \hat{i}_L \rangle}{\hat{v}_{on}} = \frac{DS_e T_s}{V_{ap} R_i} - \frac{D^2 T_s}{2L} \tag{28}$$

The voltage $V_{ap}$ is the steady-state voltage across the active-passive terminals of the PWM switch model.

This transfer function can also be found from the circuit diagram of Fig. 17, in terms of the feedforward gain, $k_f'$. The gain block, $H_e(s)$, is unity at zero frequency, and does not appear in Fig. 17. For steady-state conditions to exist, the voltage across the inductor must be zero. The perturbations in duty cycle, $\hat{d}$, are produced by feedback of the inductor current, and feedforward of the on-time voltage. Substituting for the duty cycle perturbations, and rearranging, we obtain

$$\frac{\langle \hat{i}_L \rangle}{\hat{v}_{on}} = \frac{1}{R_i}\left[\frac{D}{F_m V_{ap}} + k_f'\right]. \tag{29}$$

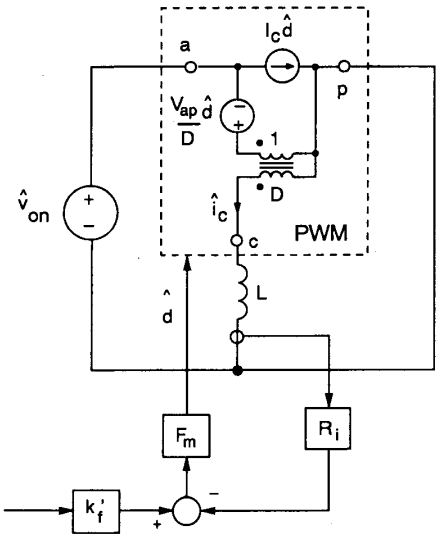


Fig. 17. Circuit model for derivation of feedforward gain. Small-signal off-time voltage perturbation is zero, and gain $k_f'$ is eliminated from this figure. Sampling gain $H_e(s)$ is unity at dc.

The feedforward gain term, $k_f'$, can be solved for by equating the two expressions of (28) and (29), with the appropriate values substituted for modulator gain, $F_m$. The simple relationship

$$S_n = \frac{V_{ac} R_i}{L} = \frac{D' V_{ap} R_i}{L} \tag{30}$$

resulting from basic relationships of the switch-model voltages, is used to obtain the result:

$$k_f' = \frac{-DT_s R_i}{L}\left[1 - \frac{D}{2}\right] \tag{31}$$

This process can be repeated for the gain term, $k_r'$. When finding $k_r'$, the on-time voltage is held constant, and (12) is differentiated with respect to the off-time voltage.

## Appendix III
## PSpice Model for Current-Mode Control

The new current-mode control model is very amenable to implementation in any circuit analysis package such as PSpice. All of the results can be incorporated into a single subcircuit which models the current feedback, sampling gain, power stage, modulator gain, and feedforward gains $k_f'$ and $k_r'$. This single subcircuit remains invariant for any PWM converter using either voltage-mode or current-mode control.

External connections to the control subcircuit are the active, passive, and common connections of the power stage, the voltage on the far side of the inductor from the common terminal, and the control voltage input. An example connection for the buck converter is shown in Fig. 18. The PSpice listing for the buck converter is given in Table II. This circuit description was used to generate the curve for control-to-output in Fig. 10, with $m_c = 1$. The circuit was run on the student version of PSpice. Use of a more sophisticated version of Spice would allow simplification of the description since the sampling gain could be representated by a single-line Laplace function.

Details of Spice listings for other converters are presented in [15]. Care should be taken to note the polarity of the current-

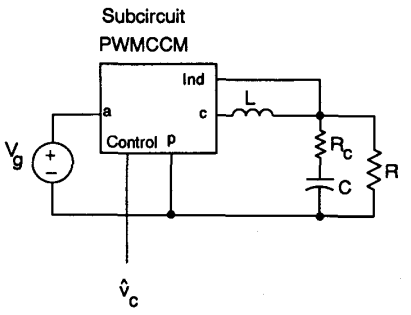


Fig. 18. PSpice modeling of the buck converter. Universal controller and power stage model, PWMCCM, contains all of information of model derived in paper. Control and power stage subcircuit is invariant for all PWM converters, with either voltage-mode or current-mode control.

TABLE II
PSPICE LISTING FOR BUCK CONVERTER

```
    Vin   1  0    AC   0
    L     2  5    37.5uH
    Rc    5  6    0.02
    C     6  0    400uF
    R     5  0    1
    Vc   11  0    AC   1
    X1    1  0  2  5  11  PWMCCM
.AC    DEC   25   10HZ 50KHZ
.PROBE

* PWMCCM:     Active Passive Common Inductor Control
.SUBCKT PWMCCM  1       2       3       4       5
* Switch model: E2=Vap/D G1=Ic Fxf=D Exf=D
    E2   7  1 17  0     24.44
    G1   1  2 17  0      5.0
    Fxf  7  2    Vxf     0.45
    Exf  9  2  7  2      0.45
    Vxf  9  3    0
    Rvc  5  0    1G
* He(s) Circuit values:  L1=C1=C2 = Ts/Pi
    Hi  10  0    Vxf   1
    C1  10 12    6.37uF
    L1  12 13    6.37uH
    C2  13 14    6.37uF
    Re  14 15    -1.57
    E1  15  0 12  0   -1E6
    R2  12  0    1G
* Summing Gains:                          0    Kf'    Kr'   Ri  1
    Ed  16  0  Poly(4) 1,4 4,2 15,0 5,0 0 -0.0614 0.0266 0.33 1
    Rd  16  0  1G
* Modulator gain. Fm = L/(VacMcTsRi) = 1/(Vp + VacTsRi/L)
    EFm 17  0 16  0   0.939
    RFm 17  0    1G
.ENDS
.END
```

sensing network for some PWM converters such as the boost converter. Also, the correct equivalent inductance should be used in calculating the modulator ramp slope for two-inductor converters such as the Cuk converter.

## ACKNOWLEDGMENT

The author wishes to thank Dr. Vatché Vorpérian for many hours of valuable discussion on current-mode control.

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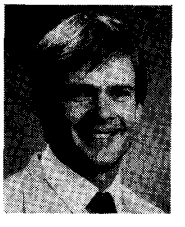

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