A Voltage Clamp Circuit for the Real-Time Measurement of the On-State Voltage of Power Transistors

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***Abstract*—For real-time monitoring of the on-resistance of a power transistor, the voltage and current should be measured during the switching operation. When the voltage waveform is measured, the amplifier inside the measuring oscilloscope may be distorted if the range of the measurement channel is not set wide enough to measure both on-state and off-state voltage levels, resulting in failure to accurately measure the voltage. Conventional circuits partially solve this problem by clamping the off-state voltage to a lower value. However, they introduce problems such as voltage peaks, measurement offset, and delays caused by *RC* time constants. In this paper, traditional clamping circuits are explained and discussed to illustrate their disadvantages first. Then, a new voltage clamp circuit is presented. The proposed circuit can solve the problems of *RC* time constants and voltage peaks during state transitions of the device under test. Finally, the performance of the proposed circuit is illustrated by measurements on a 100-kHz Buck converter.**

Keywords—real-time monitoring, on-resistance, clamping circuits, measurements, Buck converter

I. INTRODUCTION

Reliability of power electronic converters and lifetime prediction has been a major topic of research in the last few decades [1], especially in the field of aerospace. According to an industry-based survey presented in [2], power semiconductor device failures are proved to be a major concern for the reliability of power electronic converters. The failure precursor is an event or series of events indicative of an impending failure [3]. Identifying the precursor parameters of failures to be monitored is an important aspect in the reliability research. From the existing literature study, the on-resistance, found to be the most promising aging precursor in MOSFETs, is predominantly used as a failure indicator [4][5][6]. Therefore, accurate real-time measurement of the on-resistance is indispensable.

The on-resistance of the device under test (DUT) can be obtained by dividing the voltage and current waveforms during the on-state. When the voltage waveform is measured, the measurement range on the oscilloscope must be set wide enough, in order to measure both on-state and off-state voltage levels. If this is not the case, the characteristics of amplifiers inside the oscilloscope are distorted, due to a phenomenon known as "Oscilloscope Overdrive" and the lack of recovery thereof, resulting in failure to accurately measure the on-state voltage [7]. However, with the same analog-to-digital converter, a wide measurement range results in inaccurate values of the on-state voltage, which may even be perceived as negative because of the large quantization error. Moreover, for recently developed wide-band-gap devices, this problem is even more prominent because these devices exhibit a much higher blocking voltage and a much lower on-resistance than silicon devices. This means that an even higher measurement resolution is required.

Conventional circuits partially solve this problem by clamping the off-state voltage to a lower value [8][9]. However, they introduce problems such as voltage peaks, measurement offset, delays due to *RC* time constants, and additional power loss. These problems get even worse with increasing switching frequency. To address these problems, the traditional circuits will be built and simulated first to confirm their advantages and disadvantages and then improved circuits are presented and validated by simulation results accordingly. Moreover, a new voltage clamp circuit is presented, which improves the accuracy of the on-state voltage measurements. Compared to the traditional clamp circuits, the presented circuit can reduce the delay caused by *RC* time constants and suppress the peak voltage during state transitions of the DUT. The presented circuit is simple and easy to realize inside measurement units.

This paper is organized as follows. Three traditional voltage clamping circuits are explained and discussed first to illustrate their disadvantages in Section II. On this basis, optimization circuits are presented and assessed using simulations. Then, the novel clamp circuit is described and analyzed analytically and through simulations in Section III. Section IV presents the experiment results, which confirms the validity of the proposed circuit. Finally, the summary is presented in Section V.

II. ANALYSIS AND OPTIMIZATION OF TRADITIONAL VOLTAGE CLAMP CIRCUITS

A. Voltage Clamp Circuit I: based on a Zener diode

The first voltage clamp circuit is based on a Zener diode, as shown in Fig. 1. The input nodes *D* and *S* are connected to the drain and source terminals of the DUT respectively. The measurement of the drain-to-source voltage is performed with

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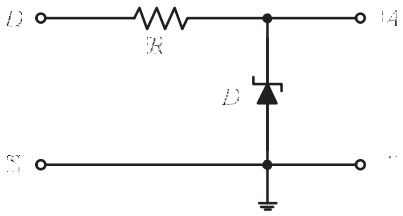


Fig. 1. Voltage clamp circuit I.

an oscilloscope by placing a voltage probe between output nodes *A* and *B*. During the OFF-state, the drain-to-source voltage (V_{DS}) of the DUT is high and the voltage between the output nodes *A* and *B* (V_{AB}) is clamped to the Zener voltage across Zener diode *D*. The Zener voltage is called the clamping voltage.

Note that the Zener voltage of *D* must be chosen greater than the on-state voltage of the DUT. If it is not the case, the drain-to-source voltage during the on-state will be clamped to the clamping voltage, resulting in failure to measure the on-state voltage. Because the highest measured voltage is the clamping voltage, the measurement range of the oscilloscope just needs to be set to a value wide enough to measure the clamping voltage instead of the high off-state voltage. Therefore, the resolution of the measurement is improved.

However, this circuit has some disadvantages. The value of *R* must be set to achieve correct Zener operation. For most Zener diodes, a current of a couple of milliamperes is required. That is to say, *R* is a value of several kilohms and the higher the off-state drain-to-source voltage is, the larger the resistance needs to be. Such a resistance, together with the junction capacitance of diode *D*, leads to an observed *RC* delay in the measurement. In high-speed switching occasions, there will be no enough time for the output voltage decrease from the clamping voltage to the real on-state voltage, resulting in the measurement failure. Furthermore, during the on-state, there is a leakage current flowing through the Zener diode, resulting in a voltage drop across the resistance *R*. Although the leakage current is small, the high resistance value will lead to a significant voltage drop. Therefore, the measured voltage between the points *A* and *B* is the actual on-state voltage minus the voltage drop across *R*. Due to these disadvantages, this circuit cannot be applied to the high-frequency or high-voltage applications.

According to [9], to address these problems, a diode D_1 is introduced in series with the Zener diode *D* as shown in Fig. 2. With the addition of D_1, the total parasitic capacitance is reduced. For this reason, as shown in Fig. 3(a), the *RC* delay is reduced. Moreover, during the on-state, the voltage across the junction capacitance of *D* will transfer to the junction capacitance of D_1, resulting in both *D* and D_1 under reverse voltage. Therefore, there is almost no current flowing through *R*, which means the voltage drop across *R* is zero during the on-state as shown in Fig. 3(b).

Although adding series diodes like the diode D_1 is an effective way to reduce the *RC* delay caused by the junction capacitance and the measurement error caused by the leakage current of *D*, more diodes added means higher clamping voltage. When it comes to high-frequency and high-voltage applications, this circuit may be helpless.

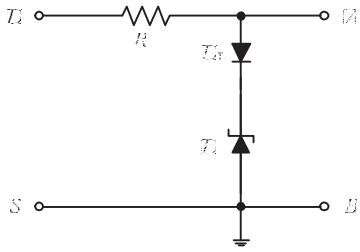
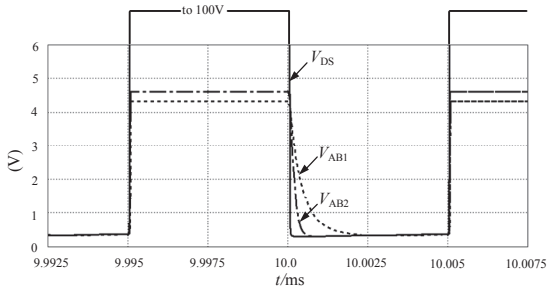
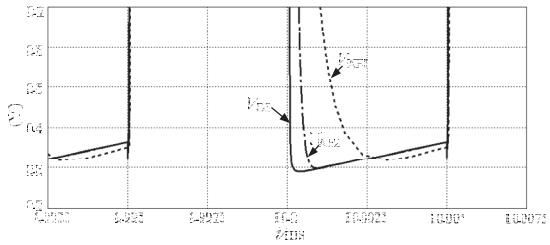


Fig. 2. Improved voltage clamp circuit I.



(a)



(b)

Fig. 3. Simulation results of circuit I (100 kHz), D_1 = 1N4148, *D*=1N4731, *R* =2 kΩ, switch = XFK64n50p, 5 A, 100 V; V_{AB1}: without the diode D_1, V_{AB2}: with the diode D_1.

B. Voltage Clamp Circuit II: based on a transistor

The second voltage clamp circuit is depicted in Fig. 4. *M* is an N-channel enhancement mode MOSFET. The gate of *M* is connected to a positive dc voltage supply V_{cc} whose voltage is higher than the threshold voltage of *M*. The input nodes *D* and *S* are connected to the drain and source terminals of the DUT and the output is V_{AB}. During the off-state of the DUT, the MOSFET *M* works in the saturation region and the current flowing through the resistance *R* is governed by

$$i_R = g_{fs}(v_{gs} - V_{th}) \tag{1}$$

where g_{fs} is the transconductance, V_{th} is the threshold voltage and v_{gs} is the gate-to-source of the transistor *M*. At this point, the clamping voltage can be given by

$$V_{clamp} = \frac{g_{fs}(V_{cc} - V_{th})R}{1+g_{fs}R} \tag{2}$$

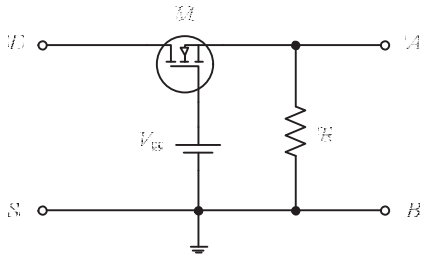


Fig. 4. Voltage clamp circuit II.

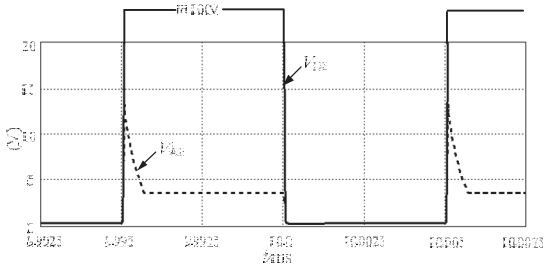


Fig. 5. Simulation results of circuit II (100 kHz), V_{cc}=8V, R =50 Ω, M=switch = XFK64n50p (V_{th}=4.35V), 5 A, 100 V.

In general, $g_{fs}R$>>1, so V_{lamp} can be approximated by

$$V_{clamp} = V_{cc} - V_{th} \tag{3}$$

When the DUT is turned on, the drain-to-source voltage of the transistor M decreases, causing v_{gs} to increase and bringing the transistor to working in ohmic region. As a result, the on-state voltage of the DUT is measured and the actual measured voltage can be expressed by

$$V_{AB} = \frac{R}{R + R_{on(M)}} V_{on(real)} \tag{4}$$

where $R_{on(M)}$ is the on-resistance of the transistor M and $V_{on(real)}$ is the real on-state voltage of DUT.

This circuit has a few disadvantages. When the DUT switches off, voltage spike usually could be produced because of the effect of the drain-to-source junction capacitance of transistor M, as shown in Fig. 5. The voltage spike increases with the value of the resistance R, which may be several times the clamping voltage. Such voltage spike not only results in failure to clamp the output voltage but also may cause v_{gs} to become more negative than allowed, which might lead to its destruction. Moreover, if the resistance R is set as small as possible to reduce the voltage spike, an observed error may be introduced in the measurement, which can be seen from the equation (4).

To reduce the voltage peaks, an improved clamp circuit is described in reference [8], which is shown in Fig. 6. It is connected to the drain and source terminals of the DUT and the output of the circuit is the voltage between the nodes A and B. The resistance R_1 and capacitance C are added to provide the current caused by a large dv/dt during the transition to off-state of the DUT. The Schottky diodes D_1, D_2 and the Zener diode D_3 together with the resistor R_2 are used to reduce the voltage spikes. During the off-state of DUT, this circuit may have two

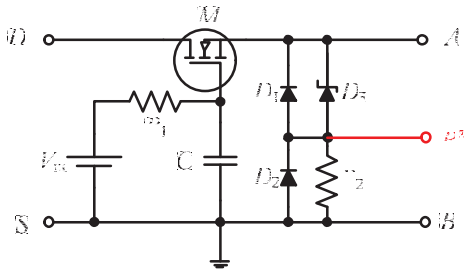
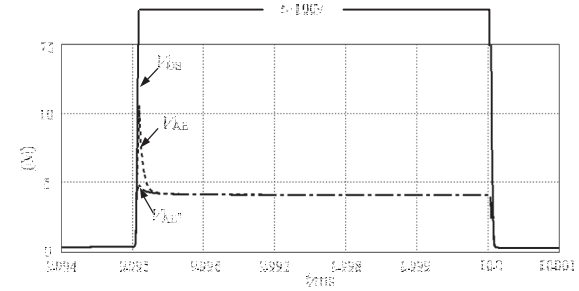


Fig. 6. Improved voltage clamp circuit II.



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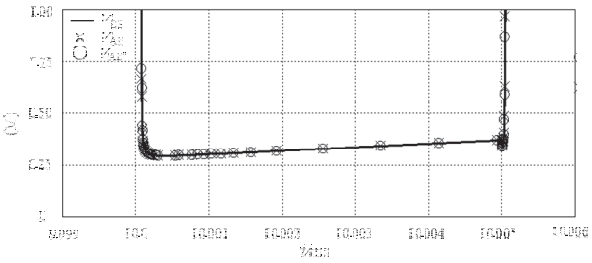


(b)

Fig. 7. Simulation results of improved circuit II (100 kHz), D_1 = D_2=1N4148, D_3=1N4731, R_1 =20Ω, R_2=5Ω, C=10nF, M=switch = XFK64n50p, V_{cc}=8V, 5 A, 100 V.

operating modes and $I_{leakage(M)}$= $I_{leakage(D1)}$+ $I_{leakage(D3)}$ is the boundary condition. Both of them are described as follows.

Case I ($I_{leakage(M)}$> $I_{leakage(D1)}$+ $I_{leakage(D3)}$): The MOSFET M works in the cutoff region. The output clamping voltage is governed by

$$V_{clamp} = V_{Z(D3)} \tag{5}$$

where $V_{Z(D3)}$ is the Zener voltage of the Zener diode D_3.

Case II ($I_{leakage(M)}$< $I_{leakage(D1)}$+ $I_{leakage(D3)}$): The MOSFET M works in the saturation region. The output clamping voltage is V_{cc}-V_{th}, just the same as that of the circuit II.

The effect of these additional components to reduce the voltage spike is limited, which can be seen from Fig. 7(a). However, from another perspective the resistance of R_2 can be set to a low value, which means the voltage drop across it is neglectable during the on-state of DUT. In this point, the voltage between the nodes A and B' ($V_{AB'}$), whose voltage spike is limited to the Zener voltage of the Zener diode D_3, can

be regarded as the output voltage. In Fig. 7, simulation results at 100-kHz switching frequency are shown, which verifies the analysis above.

A common disadvantage of the clamp circuit II and its improved circuit is that Transistor M should carry the high voltage that the DUT also carries, and thus has a large size, implicating that the parasitic drain-to-source capacitance has a large value.

C. Voltage Clamp Circuit III: based on a current mirror

In [9], another voltage clamp circuit is described, which is based on a current mirror. It is shown in Fig. 8. It consists of a current mirror, two high- voltage diodes D_A and D_B which are asked for the same I-V characteristics, and a series connection of several clamping diodes connected between the points A and B. During the off-state, the drain-to-source voltage is high and the left mirror current is forced to flow through the clamping diodes, as indicated by the solid line in Fig. 8. The output voltage is the sum of the forward voltage drops of the clamping diodes, which is called the clamping voltage V_{clamp}. During the on-state of the DUT, the drain-to-source voltage is lower than the V_{clamp}, and the mirror current flows through the diodes D_A and D_B, as shown in Fig. 8 with the dashed lines. At this moment, the measured voltage can be given by

$$V_{AB} = V_{on(D_A)} + V_{on(real)} - V_{on(D_B)} \tag{6}$$

As the mirror currents are equal and the diodes D_A and D_B have the same I–V characteristics, the voltage drops across D_A and D_B are equal, and the voltage between A and B is equal to the real on-state voltage of the DUT.

However, this circuit has a few disadvantages. First, there is an error between the output current (I_o) and the current flowing through the resistance R (I_R). If the dc current gains of the bipolar junction transistors (BJTs) in the mirror circuit are supposed to be equal, the relationship between I_o and I_R can be

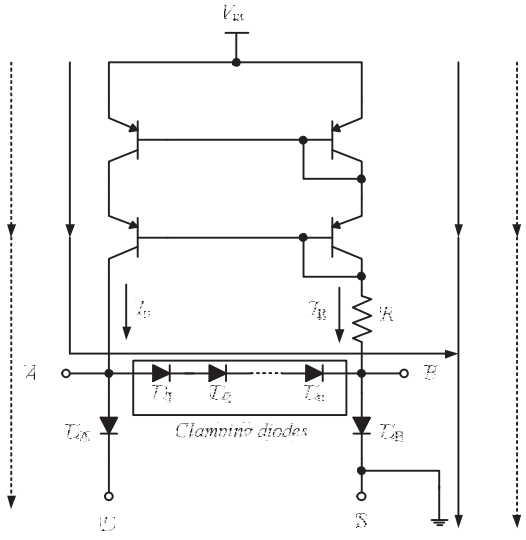


Fig. 8. Voltage clamp circuit III.

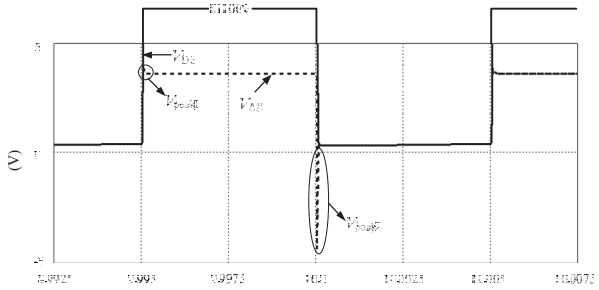


Fig. 9. Simulation results of improved circuit III (100 kHz), D_A = D_B=BAV102, D_1=…= D_5=BAV102, R =10kΩ, R_2=5Ω, BJTs=BC556, switch = XFK64n50p, V_{cc}=8V, 5 A, 100 V.

given by

$$I_o = \frac{\beta^2}{\beta^2 + 4\beta + 2} I_R \approx (1 - \frac{4}{\beta})\ I_R \tag{7}$$

where the I_R can be approximated by

$$I_R = \frac{V_{cc} - 2V_{BE}}{R} \tag{8}$$

where V_{BE} is the base-emitter saturation voltage of the BJTs. The difference between the currents flowing through the diodes D_A and D_B will cause measurement error. Moreover, the I–V characteristics of the D_A and D_B are impossible to be identical, especially when the D_A and D_B are working under difference electrical stress. Second, there is an observed loss in the mirror circuit, and the loss power can be approximated by

$$P_{loss} = \frac{2V_{cc}(V_{cc} - 2V_{BE})}{R} \tag{9}$$

Third, to reduce the P_{loss}, the resistance R has to be taken as large as possible. However, during the transition from the off state to the on state of the DUT, the high voltage across the junction capacitor of the D_A needs to be discharged by the current I_o. If the resistance of the R is large enough, the discharged current I_o will be small, causing a delay in the measurement. Moreover, if the voltage across the junction capacitor of the D_A decreases slowly, a high voltage may be placed across the left BJTs of the mirror circuit, as shown in Fig. 9 (V_{peak2}), which might lead to their destruction. The positive voltage peak (V_{peak1}) is caused by the large charging current of the junction capacitor of the diode D_A flowing through the clamping diodes during the transition to the off state of the DUT. Four, the voltage should be measured with a differential probe.

III. Novel Voltage Clamp Circuit

In Fig. 10, the proposed voltage clamp circuit is presented. It consists of a high-voltage diode D_1, a transient voltage suppressor D_2, a dc voltage supply V_{cc} and two resistances, R_1 and R_2. The input nodes D and S are connected to the drain and source terminals of the DUT and the output of the clamp circuit is the voltage V_{AB} between the points A and B. The diode D_1 is used to carry the high voltage and the diode D_2 is used to suppress the voltage spike during the transitions of the DUT. The resistance R_1 is set to a high value to reduce the power loss

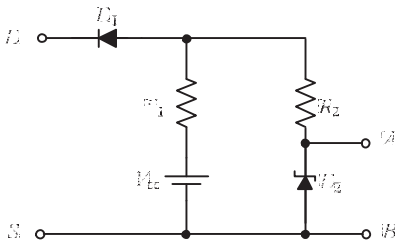


Fig. 10. Proposed voltage clamp circuit.

of the circuit and the resistance R_2 is set as low as possible to reduce the RC delay in the measurement. The voltage of the V_{cc} should be higher than the on-state voltage of the DUT.

During the off-state of the DUT, the high voltage is carried by D_1 and the output voltage V_{AB} is clamped to the clamping voltage V_{clamp}, which can be expressed by

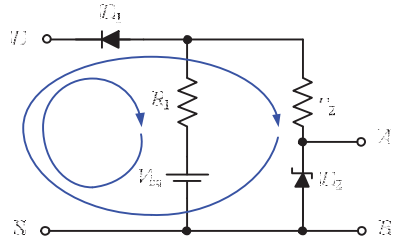
$$V_{clamp} = V_{cc} + R_1 I_{lk1} - (R_1 + R_2) I_{lk2} \tag{10}$$

where I_{lk1} is the leakage current of D_1 and I_{lk2} is the leakage current of D_2. Usually, the values of $R_1 I_{lk1}$ and $R_1 I_{lk2}$ are much smaller than V_{cc} and therefore the voltage V_{clamp} is a value around V_{cc}. When the DUT is turned on, the voltage of the supply V_{cc}, which is higher than the on-state voltage of the DUT, brings the diode D_1 into conduction. As a result, the on-state voltage is measured at the output of the circuit and the measured voltage can be given by

$$V_{AB(on)} = V_{on(real)} + V_{on(D1)} - I_{lk2} R_2 \tag{11}$$

where $V_{on(D1)}$ is the voltage drop of the diode D_1. With a small value of R_2, the value of $I_{lk2}R_2$ is very small (a few microvolts) and can be negligible. As V_{AB} can be obtained and V_{cc} is known, the current flowing through the R_1 can be derived, which means the current flowing through D_1 can be acquired. If the I–V characteristic of the diode D_1 is known, the measurement result can be corrected.

During the transition from on-state to off-state of the DUT, the transient voltage peak is caused by the parasitic capacitance of the diode D_1 through the loops as shown in Fig. 11(a). The transient voltage peak in V_{AB} can be suppressed by the diode D_2. After this transition of the DUT, there may be two operating modes in the circuit as shown in Fig 11(b), which is determined by the parasitic capacitance values of D_1 and D_2. Mode I ($V_{off}C_{D1}/ C_{D2}<V_{cc}$): V_{AB} reaches the steady state through the loops as shown by solid lines. Mode II ($V_{off}C_{D1}/ C_{D2}>V_{cc}$): V_{AB} reaches the steady state through the loops as shown by dotted lines.



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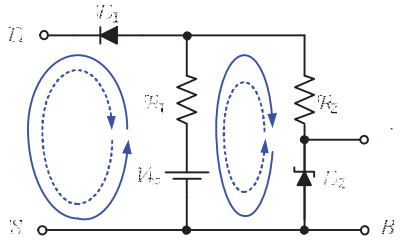

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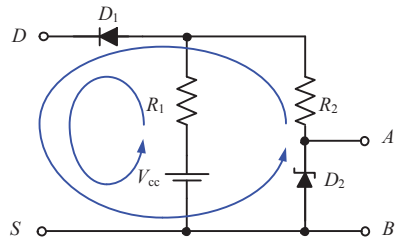
Fig. 11 On-to-off transient



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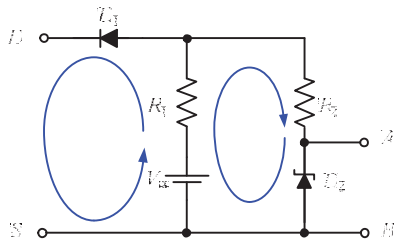
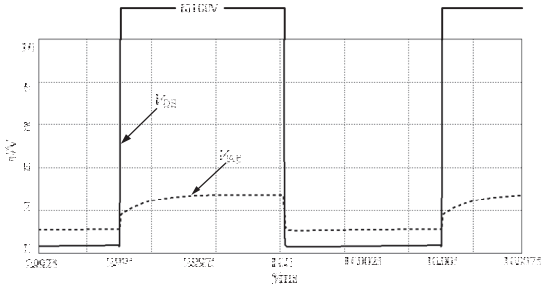


(b)

Fig. 12 Off-to-on transient

During the transition from off-state to on-state of the DUT, the clamp voltage across D_2 is decreased through R_2 as shown in Fig. 12(a). Due to the low resistance of R_2, the transition is fast. However, if the charge on the junction capacitance of D_2 and the branch current of V_{cc} are not enough for the discharge of the junction capacitance of D_1, the diode D_2 will conduct. In this case, after the discharge of the junction capacitance of D_1, V_{cc} needs to charge the junction capacitance of D_2 through the loops as shown in Fig 12(b), which will cause a RC delay due to the large value of R_1. Therefore, the parameters design of the circuit should be compromised.



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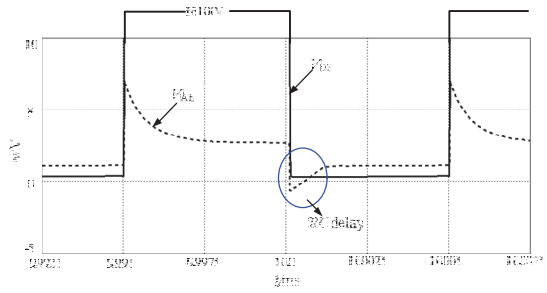


(b)

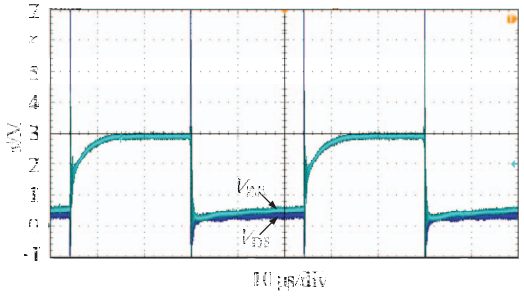
Fig. 13 Simulation results of proposed circuit (100 kHz), D_1 = BAV102, D_2=SA6.0, R_1=1kΩ, R_2=5Ω, V_{cc}=3V, switch = XFK64n50p, 5 A, 100 V.

Fig.13 shows simulation results of the proposed circuit. In the simulation, there are no voltage peaks at the output during the state transitions and *RC* delay during the transition to the on-state. However, during the on-state of the DUT, a voltage offset can be observed, which is caused by the forward voltage drop of the diode D_1. Fig. 13(b) shows the simulation results after increasing the parasitic capacitance of D_1. The increased parasitic capacitance of D_1 makes the circuit work on Mode II during the transition from on-state to off-state of the DUT and causes a *RC* delay due to the mode as shown in Fig. 12(b). Therefore, the parameters of the circuit may needs adjustments for different applications.

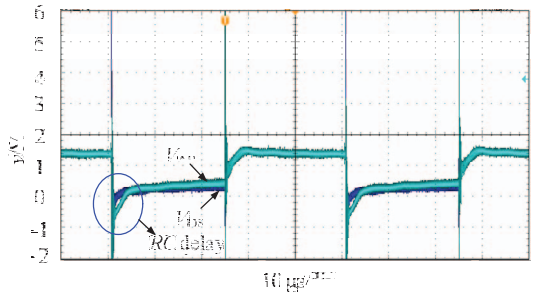
The main advantage of the proposed voltage clamp circuit is that it can suppress the voltage spike and minimize the delay caused by *RC* time constants during state transitions of the DUT. In addition, the power loss caused by the clamp circuit is very low. The disadvantage of the proposed circuit is that the measurement result needs to be corrected.

IV. Measurement Results

The measurements are done on a Buck converter with the presented voltage clamp circuit. The voltage clamp circuit consists of a high-voltage diode, a transient suppressor SA 5.0. The supply voltage of V_{cc} is 3V. The resistance of R_2 is 5Ω. Fig. 14 shows the voltage waveforms measured on XFK64n50p with an off-state drain-to-source voltage of 40V, an average current of 4A, frequency f = 100 kHz, driving voltage V_{gs} from -10 to 15V, and duty cycle D = 0.5. Fig 14(a)、(b) are measured with R_1=1 kΩ and R_1=200 kΩ respectively.



(a)



(b)

Fig. 14. Experimental results of the proposed circuit (100 kHz). (a) R_1=1kΩ b) R_1=200kΩ.

As shown in Fig. 14(a), the off-state drain-to-source voltage is clamped from approximately 90V (the voltage peak) to 6V and there is no *RC* delay during the transition to the on-state of the DUT. However, if the resistance R_1 is too large, a *RC* delay will be caused, which can be seen in Fig. 14(b). Moreover, the large value of R_1 decreases the clamping voltage, which can be explained by equation (1). A positive voltage offset can be observed in both Fig. 14(a) and (b), and the voltage offset in Fig. 14(b) is smaller than that in Fig. 14(a), which are caused by different voltage drops of D_1 at different currents.

V. Conclusions

Conventional circuits for measuring the on-state voltage waveform of a transistor exhibit a number of problems, such as an *RC* time delay, measurement offset, voltage spike during the state transitions, a large measurement loss, etc. These problems get even worse with increasing switching frequency and voltage level. To address these problems, a novel voltage clamp circuit is proposed. The proposed voltage clamp circuit can suppress the voltage spike and minimize the delay caused by *RC* time constants during state transitions of the DUT. The disadvantage is a positive measurement offset is introduced, but this offset is easy to be corrected. The performance of the proposed circuit is illustrated by measurements on a 100-kHz Buck converter, which confirms the validity of the proposed circuit.

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