Power Cycling Reliability of Power Module: A Survey

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Power Cycling Reliability of Power Module: a Survey

C. Durand, M. Klingler, D. Coutellier and H. Naceur,

Abstract—**Electronic devices using semiconductors like Insulated Gate Bipolar Transistor (IGBT) Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and diodes are extensively used in electrical traction applications such as locomotive, elevator, subway and car. The long-term reliability of such power modules is then highly demanded and their main reliability criterion is their power cycling capability. Thus, power cycling test is the most important reliability test for power modules. This test consists in periodically applying a current to a device mounted onto a heat sink. This leads to power loss in the entire module and results in a rise of the semiconductor temperature. In this paper, the different kind of semiconductors and power modules used for traction applications are described. Experimental and simulation methods employed for power cycling tests are presented. Modules weak points and fatigue processes are pointed out. Then, a detailed statistical review of publications from 1994 to 2015 dealing with power cycling is presented. This review gives a clear overview of all studies dealing with power cycling that were carried out until now. It reveals the principal trends in power electronic devices and highlights the main reliability issues for which an important lack of knowledge remains.**

Index Terms— **Reliability estimation, Semiconductor device modeling, Semiconductor device testing, Semiconductor materials, Statistics**

I. Introduction

POWER electronic devices use semiconductor technology to convert and control electrical power. The take up of electronics in transport systems has resulted in tremendous growth in the use of power electronics devices such as Insulated Gate Bipolar Transistor (IGBT), Metal Oxide Semiconductor Field Effect Transistor (MOSFET), and diodes. These devices are being increasingly used in electrical traction applications such as locomotive, elevator, subway and car. Thus, manufacturers seek to estimate lifetimes of semiconductors and the conditions under which they fail. Such lifetime estimation and reliability testing is usually done through Active Power Cycling (APC) tests as it reproduces working conditions. The modules are mounted on a heat sink and a voltage is applied in a forward direction to reach a defined current. This current through the device under test leads to power loss throughout the entire module and results in an increase in the semiconductor temperature. By periodically switching the current on and off, the temperature of the chip rises and falls due to alternate heating and cooling, inducing a junction temperature swing ΔT_j. One power cycle is defined as the period of heating up the junction from minimum temperature T_{jmin} to maximum T_{jmax} and cooling it down. In most set ups, the temperature and electrical data are monitored during each cycle. If these values increase more than a previously determined amount (e.g. 20%), the End of Life criteria is fulfilled, and the corresponding number of cycles to failure N_f is then used in models for lifetime estimation [1].

Active Power Cycling (APC) can be distinguished from Passive Temperature Cycling (PTC) test as the heating source differs: in APC the chip is the internal heating source (active) whereas in PTC the heating source comes from its environment (passive). Thus, the temperature distribution in the device being tested is also different: the temperature is spatially not homogenously distributed in APC whereas for PTC the temperature of the module is uniformed. Moreover, the commonly used cycle times are about ten to one-hundred times shorter at APC (from 0,2 seconds to 1 minute) than at PTC (from 15 minutes to 1 hour).

The main failure mechanisms reported to occur in power modules are: bond wire fatigue, aluminum reconstruction and ratcheting, solder fatigue, delamination at the interface between Mold/Copper and chip cracking. Bond wire and solder fatigue are often taken as responsible for device failure as bond wire and solder are both weak components located at critical interfaces.

Two projects are the main references concerning power cycling capability of power modules: the Swiss LESIT project (1993-1995) [30] and the RAPSDRA (Reliability of Advanced Power Semiconductor Devices for Railway traction Applications, (1995-1998)) [32] project. The LESIT project has power cycled IGBT modules with a base plate coming from different manufacturers in 14 tests with different thermal conditions. The main failure mechanism considered was the bond wire lift-off. The result of the study was the determination of a lifetime model depending on the thermal conditions of the test, see Fig. 1, and in (1). The important result of LESIT project is the prediction that besides ΔT_j, also the medium junction temperature T_m has considerable influence on the power cycling reliability.

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$$N_f = A \cdot \Delta T_j^{\alpha} \cdot e^{\left(\frac{Q}{R \cdot T_m}\right)} \quad (1)$$

With R being the gas constant (8,314 J/mol.K) and T_m in Kelvin make A = 640, α = -5, and Q= 7,8×10^{4}J.mol^{-1} (or about 0,8 eV).

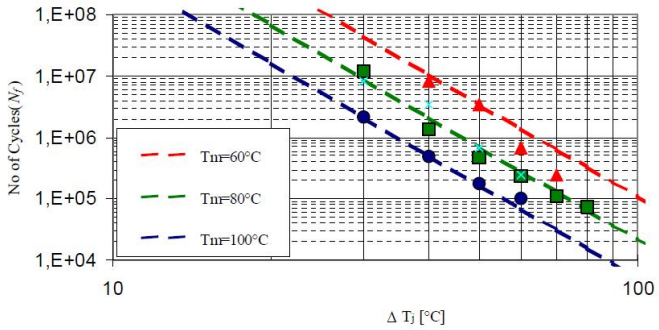


Fig. 1. Number of cycles to failure versus ΔT_j and T_m from the LESIT project [30]

The RAPSDRA project has proposed 2 APC tests conditions. The first test focuses on the bond wire reliability and recommends testing devices with a short t_{on} so that the period of cycle does not exceed 3 seconds. The second test aims at determining solder reliability and recommends testing devices with a long period 1-minute cycle. This shows the influence of t_{on} on the failure mechanisms development and how this dependency can be used to study preferably one phenomenon or another.

The LESIT and RAPSDRA projects were among the first ones to study APC, to determine the influence of test parameters on the reliability of power modules and to provide a lifetime model. But these studies were carried out 20 years ago and since then technologies have evolved. Thus it would be interesting to review the results of studies published from 1994 until now, regarding the reliability of power modules under APC.

In the following, the different types of semiconductors and power modules architectures are described. Modules weak points and fatigue processes are pointed out. Experimental and simulation methods employed for APC tests are presented. These descriptions show the variety of APC methods existing for experiments and simulations, as well as the variety of issues concerning power modules reliability. Then, publications from 1994 to 2015 dealing with APC are statistically reviewed. The variety of modules studied, the kind of tests performed and the goal of studies are analyzed in detail. This allows having a clear overview of all studies dealing with APC that were carried out until now. It also reveals the principal trends in power electronic devices and highlights the main reliability issues for which an important lack of knowledge remains.

II. A Variety of Semiconductors And Power Modules

Since the early stages of power electronics, a wide range of semiconductors have been developed: GTO (Gate Turn Off Thyristor), BJT (Bipolar Junction Transistor), IGBT (Isolated Gate Bipolar Transistor), IGCT (integrated Gate Commutated Thyristor), MCT (MOS Controlled Thyristor), MOSFET (Metal Oxide Semiconductor Field Effect Transistor)… These converters are being used over a wide power range, with ratings from milliwatts up to gigawatts. Depending on the required voltage and current ratings of the power semiconductors, different types of power semiconductors are being used, see Fig. 2.

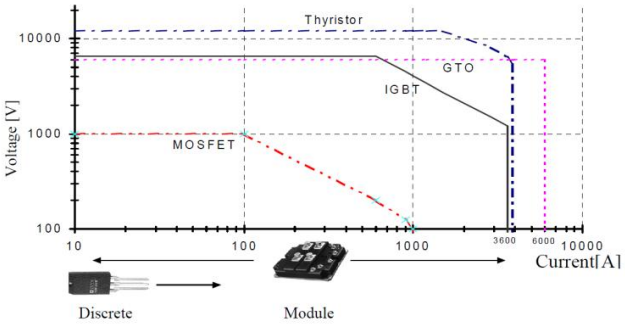


Fig. 2 . Power levels of power electronic components [2]

All power electronic converters listed above are using Si based power semiconductors, but since 2011 semiconductors made of silicon carbide SiC have been emerging. The SiC technology remains under development, but once processing and fabrication issues with SiC are solved, a significant reduction in power electronic converters conduction and switching losses can be achieved by replacing Si devices with those made from SiC [3, 4].

So a wide variety of semiconductors are available to design a power module. Then, regarding the power module's structure, one can consider that there are two main standard module designs in power electronic for packages capable of housing multiple chips per electrical function in parallel: Direct Copper Bonding (DCB) based modules and lead frame based modules.

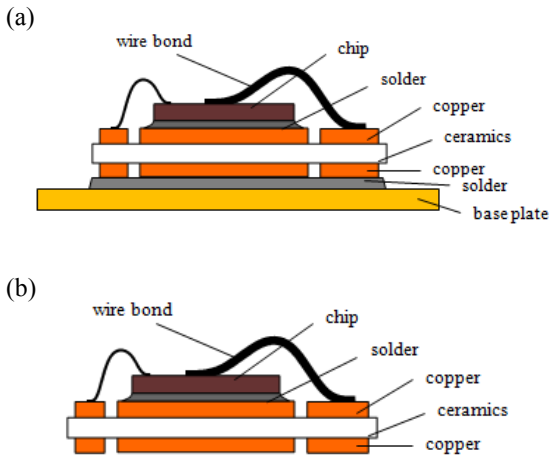


Fig. 3. (a) Internal structure of a DCB based module with a base plate and (b) without base plate

For all modules, the electrical connection of the chip is usually achieved by aluminum wire bond ultrasonically welded on the top side of the chip. The difference between DCB based and lead frame based modules comes from the bottom side of the chip.

For DCB based modules, the bottom side of the chip is soldered onto the upper copper metallization of the DCB. The ceramic is usually made of aluminum oxide Al_2O_3 or aluminum nitride AlN. The AlN is more advantageous: its thermal conductivity is 7 times higher than for Al_2O_3, and its Coefficient of Thermal Expansion (CTE) is almost 2 times lower. Then, there are 2 variants (Fig. 3): one with a based plate and a more recent one without a base plate. In the first version, the DCB is mounted on a metallic base plate, usually made of copper, which maintains the module on the heat sink through thermal paste. This construction is found in 70-80% of all power modules produced by European manufacturers (Infineon, Semikron, IXYS, Danfoss, Dynex) and is also common in modules produced by Asian manufacturers. In the second version, there is no base plate, and the DCB is directly mounted on the heat sink through a thermal paste. This solution shows better thermal performances and avoids the stress inductance caused by the CTE mismatch between the ceramic and the base plate. DCB based modules are usually not encapsulated by a mold.

For lead frame based modules, the bottom side of the chip is soldered on a metal lead frame, mostly made of a copper alloy. To ensure the electrical isolation and the mechanical protection of chips, the subassembly, excepting the lead frame, is generally transfer molded by a plastic molding compound [5]. The package is then mounted on the heat sink through thermal paste. This internal structure (Fig. 4) is used in the discrete power devices of the TO- family. Power devices of TO cases are widely used in low and middle power applications like DC/DC and AC/DC converters.

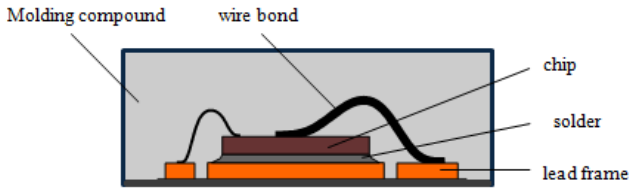
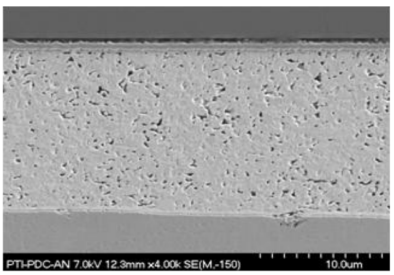


Fig. 4: Internal structure of a lead frame based module

Interconnects and assembly technologies are constantly evolving. Regarding joining technology, the chip or DCB attaches were initially lead containing solder. Then due to the Reduction of Hazardous Substances (RoHS) legislation, the lead containing solder were progressively replaced by lead-free solder. Today soft soldering techniques limit the lifetime of devices because of the low melting point of standard tin-based soft solders, thus new materials or alloys have to be considered. The two main solutions that are currently developed are Low Temperature Joining Technique (LTJT) also called silver sintering and diffusion soldering (Fig 5). For Ag sintering, the traditional solder paste is replaced by a paste consisting of silver flakes embedded in a semi-fluid matrix and the assembly is sintered under a relatively high pressure (e.g. 10 - 40 MPa) and moderate temperatures (e.g. 230°C) [6]. A porous interconnection is obtained without voids and with a high melting point (961°C) [44]. The diffusion soldering process creates a bond which is solely formed from intermetallics. This soldering technology is based on the inter-diffusion of a low melting point metal (Sn) in the other element (Cu), having a higher melting point. For the Cu-Sn system the joint can e.g. be produced by the formation of Cu_3Sn and Cu_6Sn_5 intermetallic phases which have much higher melting points and higher mechanical strengths than the Sn-based soft solder base materials [7].

(a)



(b)

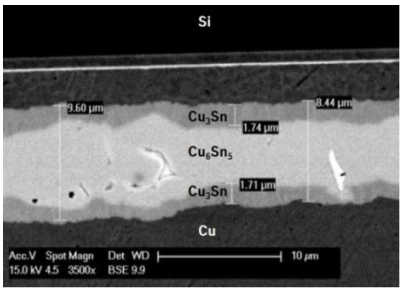


Fig 5.(a) Cross sections of an Ag sinter joint [6] and (b) a diffusion bonded joint [6]

Regarding interconnect technology, Al wire bonding is the most widely used technology, but wire bonds often represent the weakest part of power modules, and thus limits their lifetime. To overcome this limit, new interconnect technologies have been developed: Cu and Al-clad Cu wire bonds, ribbons, and Cu clips (Fig. 6). The Al of wire bond can be replaced by Cu as it offers better electrical, thermal and mechanical properties. An alternative to pure Cu wire bonds are Al-clad Cu wire bonds. The Al/Cu composite material combines the benefits of both constituent materials. The excellent mechanical, electrical, and thermal properties of Cu and the softness and strong bonding characteristics of pure Al should result in a very reliable bonding joint without losing the versatility of the standard pure Al bonding processes [69]. Ribbon bonding is an attractive alternative solution to standard Al wire bonding, due to the lower number of ribbons required to achieve the same interconnects resistance, meaning a reliability increase combined with a cost reduction for the same electrical performance [8]. The Cu clip technology is typically used for MOSFET devices and provides improved electrical performances when compared to multiple wires or even with ribbons. The clip interconnect also reduces the electrical and thermal resistance and package inductance and improves the current distribution into the device. The clip-bonded package has an option of adding a heat sink on top of

the clip or using a thick clip for dual side cooling. The implementation of dual side cooling improves the thermal performance of the module, which the wire bond technique cannot achieve.

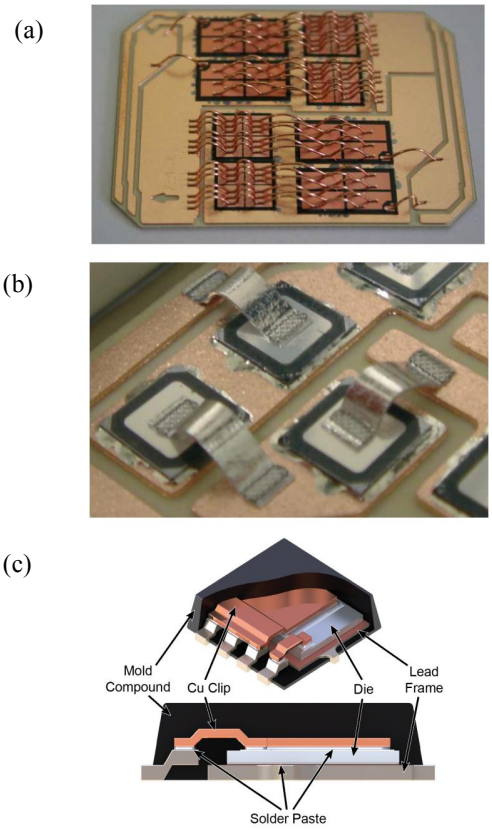


Fig. 6. (a) Cu wire bonds on an IGBT [9], (b) a DCB substrate with Al ribbons [10], and (c) a Cu clip package SO8-FL from Amkor [11]

As simply applying one improvement step will not necessarily lead to a better reliability, manufacturers are developing technologies which are combining different improvement steps. For example, the Danfoss Bond Buffer (DBB) technology combines the advantages of the sintering and the Cu bonding process [94]. Infineon has developed a similar technology, called .XT. It consists of a combination of Cu bond wires, diffusion soldering and improved system soldering for the die to DCB interconnection [12]. The SKiN device developed by Semikron, contains power chips which are sintered on both sides. The chip top side is sintered to a special flexible circuit board, which is the key design element of the package. [13].

III. A Variety of Test Methods

First of all, 3 different types of APC tests are in use: DC current, Pulse Width Modulation PWM, or superimposed tests. The DC current injection induces thermal stress by creating a thermal flux in the module. This kind of test is relatively simple but the excitation of devices is not realistic (no switching and no high voltage). PWM tests generate APC with realistic electrical stress in power devices. The DUT acts as a single phase PWM inverter, its switching frequency is adjustable and provides a regulated sinusoidal current to an inductive load. Here the operating conditions are similar to those existing in a drive inverter [91]. In a superimposed test, devices are submitted to a combination of PTC and APC. During the dwell time of a PTC test, power injections are applied. This test also aims at a better representation of real applications in which power modules undergo both PTC and APC simultaneously. Obviously the number of cycles to failure obtained for the same device under those 3 different tests will be different as the loading conditions differ. But, even by assuming that all tests are performed under DC current, some differences can still be observed in the test set-ups.

The cooling function of the heat sink can be ensured with air-cooling or fluid-cooling systems. Fluid-cooling presents the difficulty that one has to deal with pumps, pipes and to regulate the coolant flow. On the other hand with air-cooling the maximum cycle frequency is limited [14].

Besides the cooling system, the parameter monitoring is also an important issue in APC. Two main parameters are generally considered as good ageing indicators in power device ageing tests and are monitored: the thermal resistance between the junction and the base plate (R_{th}), the on-state voltage (Collector-Emitter voltage V_{ce} in case of an IGBT, Drain-Source voltage V_{DS} for a MOSFET and forward voltage V_F for a diode). Sometimes, the leakage current is also monitored as an aging indicator. The on-state voltage measurement makes it possible to detect wire bonds' damages by instantaneous stepwise increases. The relative variations due to this damage are very low because the low voltage across the connections constitutes a weak part of the total on-state voltage. Therefore this measurement must be made with a very high degree of accuracy. R_{th} is an indicator for characterizing the assembly integrity between the chip and the base plate. R_{th} increases if a fracture appears and significantly modifies the heat transfer. Its evaluation is the most delicate and requires measuring junction and base plate temperatures under a fixed thermal flux. By calculating the power dissipation P_d the thermal resistance R_{th} can be estimated (e.g. of an IGBT):

$$R_{th} = \frac{T_{j\,max} - T_c}{P_d} = \frac{T_{j\,max} - T_c}{V_{ce\,sat} \cdot (I_{load} + I_{meas})} \qquad (2)$$

With T_c the heat sink temperature (also called case temperature), $V_{ce\,sat}$ the collector-emitter saturation voltage, I_{load} the loading current and I_{meas} the measuring current.

The case temperature is usually measured via a thermal sensor i.e thermocouple glued to the base plate of the device under test. In contrast, there are several methods of measuring the junction temperature T_j. If a closed molded package is under test, the only way to measure T_j is via the measurement of Thermo-Sensitive Parameters (TSP), such as the on-state voltage. In the case of an open module with accessible die, T_j can be determined via the measurement of the chip surface temperature, for which there are 3 main methods: infra-red cameras, thermocouples and optical fibers with crystal senses

on their ends. Infra-red method is a fast, accurate and non-contact temperature measurement. This method provides thermal imaging of the whole modules, which can be useful to have a first evaluation of the temperature distribution. Thermocouples method is a contact chip temperature measurement with a response time of about 10 ms but this response time and the measurement accuracy can be altered due to a bad thermal contact with the measurement area. Two sorts of contact optical fibers are used: fibers with GaAs sensors and whose response time is about 100 ms, and fibers with phosphor sensors with a response time at 63% of 25 ms (not depending on the environment of the sensor) and a measurement delivered every 250 ms. This last tool can provide reliable dynamic temperature measurements through the silicone gel recovering the chips. [29]

So, depending on the method used to measure the junction temperature, the result obtained can be more or less precise, thus influencing the accuracy of the R_{th} ageing indicator. And ageing indicators are used to determine the number of cycles to failure via failure criteria. Indeed, when the on-state voltage or the R_{th} are increasing to a certain amount previously defined, the test is stopped and the DUT is considered to be failed (Fig. 7). Moreover, some variations are to be observed in the definition of the failure criteria. For the on-state voltage based failure criteria, the amount of increase traditionally used ranges from 5% to 20%. For the R_{th} based failure criteria, the amount of increase varies from 10% to 20%.

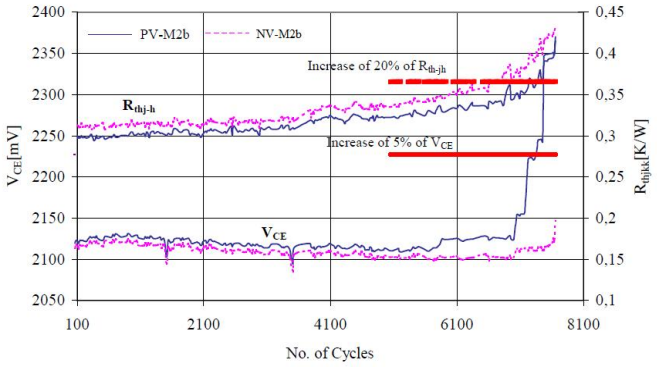


Fig. 7. Evolution of V_{ce} and R_{th} during APC test of ECONOPACK power modules at ΔT_j=113K [44]

More recently, other failure indicators were monitored, like the drain to source on state resistance R_{DSon} [73] or the thermal impedance Z_{th} [59]. To determine the R_{DSon}, APC has to be stopped, a small current is injected in the DUT and the exact drain current I_d that is injected through the device and the drain to source voltage V_{DS} are measured. R_{DSon} tends to increase in electrical tests when the component thermal performances are decreasing and a steep increase is observed when the percentage of failure is important. Monitoring the thermal impedance spectrum also requires test interruption. The Z_{th} is usually measured in the cooling phase, after that a load pulse is applied through a load current in the DUT. So, there is a wide range of variations concerning failure criteria.

The definition of the control strategy of an APC test, i.e. the strategy of reacting to degradation effects in the DUT is also of prime importance. It was just seen that degradations effects can affect the device parameters and thus cause a change of the test condition during the test duration. Solder fatigue increases the thermal resistance of the DUT which increases the temperature swing under constant test conditions (load current, on-time, cooling conditions). As well as wire bonds, degradations enhance the on-state losses in the device and increase the temperature swing. The positive temperature coefficient of modern devices will consequently lead to increased losses, which again will increase the device temperature. This positive feedback loop can significantly accelerate the failure process. Therefore, the control strategy is a very important feature of the APC test. There are 4 different control strategies which were described and compared in [57]:

1) t_{on} = constant and t_{off} = constant

This strategy of constant timing switches the load current on and off in fixed time intervals. ΔT_j is defined at the test's start via e.g the definition of a constant current and T_{jmax}, T_{jmin} and ΔT_j may increase during the test's duration due to aging effects with no compensation by a control strategy. This is the method closest to application and the most severe one.

2) ΔT_c = constant

This strategy controls the heat sink temperature. On-time and off-time are not fixed, but are determined by the time needed to heat and cool the device to the specified temperatures. Here a change in the cooling liquid temperature would be compensated by adjusting the heating and cooling times. This maintains a constant temperature swing. Since a possible degradation of the thermal interface between module and heat sink would be compensated, this strategy is less severe than the strategy 1. Taking the strategy 1 has a reference, an increase of about 50% in the number of cycles to failure is observed by testing with strategy 2 in [57].

3) P_v = constant

This control method is based on constant t_{on} and t_{off} times but with the additional requirement, that the power losses P_v are kept constant. This requirement is achieved by controlling the gate voltage or current to compensate an increase in the voltage drop V_{ce}. This strategy is much less severe for a module, as it reduces the acceleration effect of different failure modes, and results in a significant increased number of cycles to failure. In this case, the number of cycles to failure increases to 120% compared with strategy 1 [57].

4) ΔT_j = constant

This latest strategy supervises T_{jmin} and T_{jmax} and reduces t_{on} or the current load I_{load} to keep this parameter constant. This compensates all degradation effects and leads to the highest lifetime. Indeed, the number of cycles to failure increases to 220% in comparison with the reference [57].
It is therefore essential to know the control strategy, if APC tests are to be compared.

The complexity in interpreting and comparing different APC studies also comes from the interdependence of all failure mechanisms and the influence of diverse test

parameters. Recently, a pure statistical analysis [50] of a significant number of APC tests suggested the impact of several parameters, in addition to ΔT_j and T_m known from the LESIT project. In this analysis, the power on-time t_{on}, the wire bond thickness d_{bond}, the current density and the chip's voltage class are shown as parameters influencing the lifetime.

IV. A Variety of Simulation Methods

Different methods to simulate APC exist. Some papers are simulating APC via an equivalent electronic RC circuit with a current source. The electric current corresponds to the power loss, the voltage of the resistor corresponds to the temperature difference ΔT_j, the electrical capacitance C to the thermal capacitance C_{th} and the electrical resistance to the thermal resistance R_{th} [66]. Boundary Element Method (BEM) and Finite Element Method (FEM) are also often employed. Those methods will be the center of our interest. Simulating APC with FEM is more complex than simulating PTC. Indeed, for APC a coupling of analyses, like an electro-thermal analysis or a thermo-mechanical analysis, is required. For an electro-thermal simulation, first an electrical analysis is made: the electrical properties of the different materials should be registered (electrical conductivity, resistivity...) and a current pulse is simulated as the loading condition. At the end of this first analysis, the voltage mapping of the device in function of the time is known. This voltage mapping will then be the load in the second analysis, the thermal one. The thermal properties of the material (specific heat, heat conductivity) should also be implemented in the model as well as some thermal boundary conditions. For example, the environment temperature, and the heat sink temperature. After calculation, the temperature mapping of the device in function of the time is determined. In a thermo-mechanical analysis, the loading conditions for the first analysis are thermal. The environment and heat sink temperature, and/or convection factor of the air or of the cooling system should be known. Then, an internal heat generation is simulated in the chip for a determined time. This corresponds to the current pulse of APC. Of course, the thermal material properties are also registered. After calculation the temperature distribution of the device in function of the time is available. This temperature distribution will then be the load in the second analysis, the mechanical one. The mechanical properties (Young's modulus, Poisson's coefficient, CTE) are implemented. A boundary condition such as a fixation point is added. Then the mechanical analysis delivered a deformation map of the module from which stresses and strains are derived. In some few papers, electro-thermal simulation is followed by a thermo-mechanical simulation to accurately simulate APC. As this coupling of analyses required a long calculation time, some approximations should be made by modeling the device. For example, a 3D model with symmetries can be reduced to 2D, or the mesh can be refined in important areas but coarsen in others. Models can also be focused only on the layers of interest, like wire bonds, or a bi-layer with the die and its metallization. Another way of modeling can be to represent the whole module but without the thinnest layers. The accuracy of material properties is also an issue, as implemented e.g. complex viscoplastic behavior will increase the calculation time, in the case of a mechanical analysis. A way to solve this problem is to consider all material layers having a simple linear behavior, except the material of interest which can be precisely modeled with temperature dependencies and a plasticity model.

V. A Variety of Interests

Abundant studies on APC have been carried out since 1994, but with different goals. In most publications, one material layer of the power device constitutes the center of interest of the study. The layer being under focus depends on the preponderant failure mechanism occurring in the module. The main failure mechanisms that are usually taking place in power electronics modules are:

- Bond wire fatigue
- Aluminum reconstruction and ratcheting
- Solder fatigue
- Delamination at the interface between Mold/Copper
- Chip cracking

Bond wires are often reported as the weakest component of power modules, responsible for device failures [15, 16, 37]. The bond wire lift-off failure is caused by the CTE mismatch between the Si of the chip (2,8 ppm/K) and the Al wire (23,5 ppm/K). Plastic strain accumulates in Al as it is a ductile material and after a number of cycles, the interface is destroyed and the wire lifts off.

The CTE mismatch between Si and Al is also responsible for the reconstruction of the Al metallization, an Al layer located just on top of the chip. The plastic strain accumulates in the Al metallization during pulsed operation and leads to a texture change of the layer [17]. In molded packages, the Al metallization can also suffer from ratcheting due to a CTE mismatch between Si and mold [18, 87].

Solder layers represent a critical interface in power assemblies, as lead-free and lead-rich solder alloys used in power devices exhibit a CTE which is heavily mismatched with that of Si and DCB or Cu lead frame. Creep strain accumulates in solder layers and after some cycles some cracks appear.

Interfacial delamination is one of the major reliability issues of electronic packages encapsulated by a mold. Due to a CTE mismatch, the interface between the molding compound and Cu lead frame is often a weak link. Indeed, under cyclic thermal variations, the CTE mismatch leads to incompatible thermal strains along materials interfaces, and initiates delamination [19].

Micro die cracks can occur during the manufacturing process through crystal growth, wafer scrubbing and slicing and die separation and during wire bonding or soldering [20]. Due to the CTE mismatch between Si and substrates, tensile stresses at the center of the chip and shear stresses at the edges are developed during pulsed operation. This leads to cracks growth by stable fatigue propagation and can cause brittle failure of the die [15, 21].

Thus wire bonds or Al metallization or solder layers or chip or molding compounds can constitute the center of interest of a study in order to analyze the failure mechanisms that are taking place in that specific location. Moreover, final

objectives of studies can differ. For some studies the goal is to understand a failure mechanism. Therefore this mechanism can be analyzed at different scales (macro and micro), or some comparisons can be made regarding the type of failure mechanisms and their evolutions under 2 different test conditions. Then, influences of the module's design on the apparition of failure can be studied. Test parameters also have an influence on the development of failure mechanisms and this can be studied as well. Finally after having understood failure mechanism and studied the influence of test parameters the last step is to determine the lifetime model of the mechanism in function with test parameters.

VI. Statistical State Of The Art In APC Tests

In order to have a clear overview about all the APC tests that were performed until now, 70 publications from 1993 to 2014 were reviewed [25-95]. For all these papers, the quantity of modules tested, the type of modules, the test conditions as well as the analysis methods, the goal of studies and the lifetime estimations are reported and analyzed

A. Quantity and type of device tested

First of all, the number of samples tested per publication was reported and its distribution is plotted in Fig. 8. For some papers the number of samples per test run was missing, so the quantity was assumed to be one. The statistical power is important to know in order to recognize significant effects between different APC tests. As there are minor deviations in the production parameters, the result for every sample can differ, therefore a minimum of 10-15 samples per test is generally required to obtain reliable results.

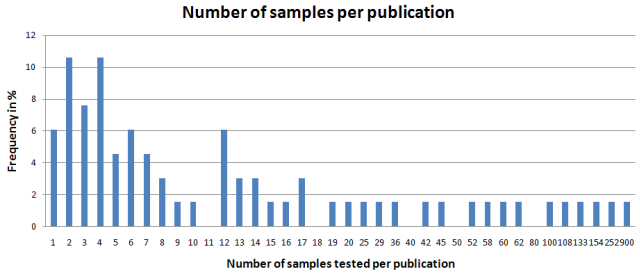


Fig. 8: Distribution of the number of tested samples per publication

As can be seen from the Fig. 8, most papers are generally tested up to 10 samples or less. In a few cases, more than 100 devices were tested in total. But in 86% of cases there is only one sample per test run.

The type of semiconductors that were submitted to APC was analyzed Fig. 9. It reveals that with a frequency of 65% the vast majority of tests are performed with IGBT. Then, come diode and MOSFET, both with about 10% of testing frequency. DMOS (Double-Diffused MOS), TRIAC (Triode for Alternating Current), HDTMOS (Third Generation of High Density TMOS), JFET (Junction Gate Field-Effect Transistor), and transistor were also tested but in small proportion. Here, the supremacy of IGBT on all other types of semiconductor appears clearly.

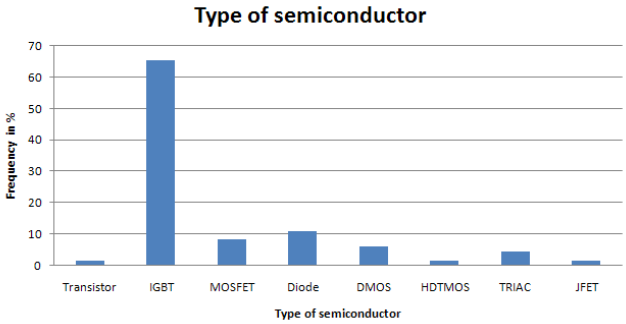


Fig. 9. Histogram showing the type of semiconductors tested per publication

Details regarding the internal structure of the modules undergoing testing were also investigated. The most widespread interconnect is the Al wire, representing 85% of interconnects; 5% of the tested modules had either Cu wires or a Cu clip as interconnects and fewer had Ag stripes or Al-clad Cu wires (Fig. 10).

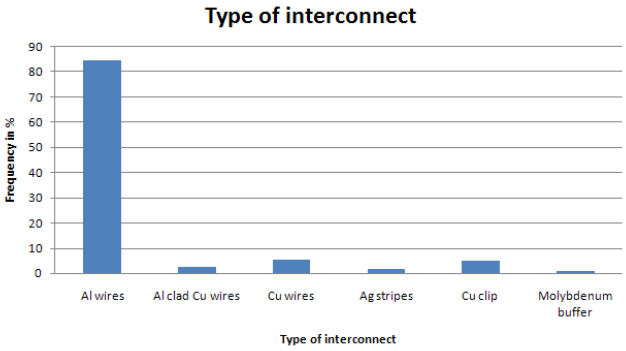


Fig. 10. Histogram showing the type of interconnects in the tested modules

Concerning the metallization layer on top of the chip, 94% of the modules had a metallization made of an aluminum alloy (e.g. AlSiCu or AlCu…). Only 6% of them had a Cu metallization.

The die itself, was made of silicon, except for 4% of the modules which had a chip of silicon carbide SiC.

The die was attached to its substrate mostly via soldering. Only 12% of the dies were attached with Ag sintering. The solder alloy used for the die attach was quite often not mentioned. By analyzing the available data on solder alloys, one can see on Fig. 11 that a short majority of modules are using lead-free solder rather than lead-rich solder. Diffusion soldering remains an exception.

The substrate is at 90% a DCB, at 6% a Cu lead frame and at 4% a Printed Circuit Board (PCB). In almost half of the cases, the exact type of DCB was not mentioned, but concerning the available data, Fig. 12 shows that DCB with Al_2O_3 is preferred to DCB with AlN.

60% of the modules are designed with a base plate. Among those modules, the majority had a Cu base plate, whereas the others had a new AlSiC or an Al base plate (Fig. 13).

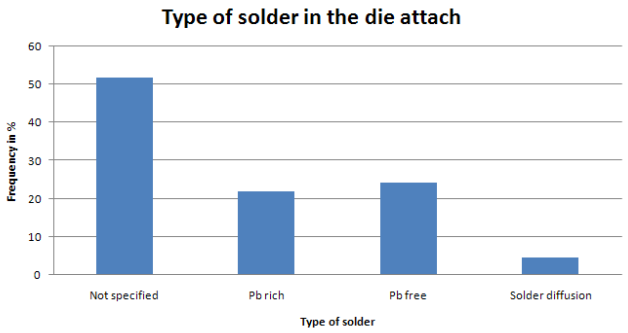


Fig. 11. Histogram showing the type of solder for the die attach in the tested modules

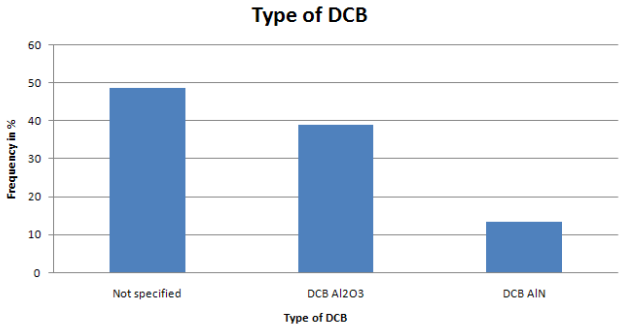


Fig. 12. Histogram showing the type of DCB in the tested modules

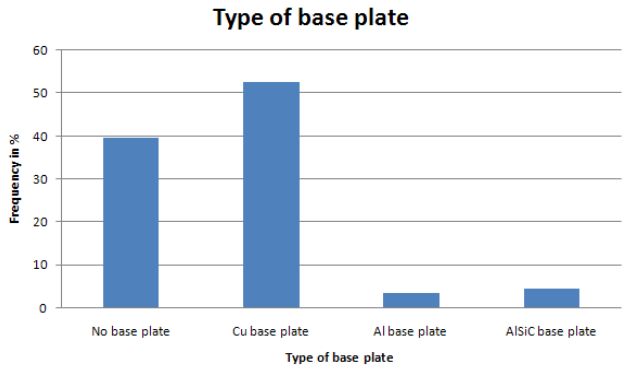


Fig. 13. Histogram showing the type of base plate in the tested modules

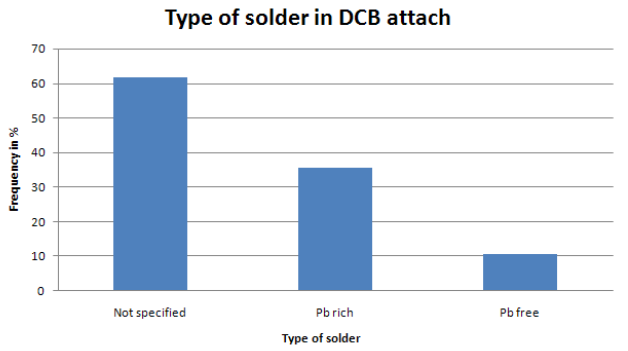


Fig. 14. Histogram showing the type of solder for the DCB attach of the tested modules

The DCB attach, which corresponds to the joint between the lower Cu layer of the DCB and the base plate, is achieved at 96% via soldering. The rest of the joints are Ag sintered. For more than 60% of the solder joints, the type of alloy used was not specified. But, by analyzing the collected data, it clearly appears that for this joint, lead-rich alloys are by far preferred (Fig. 14). Indeed, in order to avoid the remelting of the alloy used for the die attach during soldering steps in production, high-lead alloys with melting points above 260°C are used. Due to a lack of cost-effective lead-free alternatives, those alloys are exempt from RoHS.
Finally, only 18% of the tested modules are epoxy-molded.

To summarize, most of the DUTs were standard IGBT modules, with Al wires, a lead-free die attach, a DCB soldered with a lead-rich alloy on a Cu base plate, and without any encapsulants. But one should also notice that quite often a lot of information was missing, such as the type of solder for both the die attach and the DCB attach, as well as the type of DCB that was used.

B. Test methods

Now let's analyze the variety of testing conditions. First concerning the cooling method, fluid-cooling systems are used at 65%, whereas air-cooling systems are used at only 35%.
Moving on to the art of APC test performed, almost all tests are performed with the DC current test bench. Only 5% of the tests are PWM tests and not a single paper studied the behavior of modules under this superimposed test. This comes from the fact that setting up a test bench able to perform PWM or a combination of PTC and APC is far more complicated than setting up a conventional DC test bench.

The test strategy chosen in 65% is the strategy fixing constant time intervals for t_{on} and t_{off} (Fig. 15). Almost 20% of tests are done with the "ΔT_C = constant" control method. This is the preferred testing method, when a multitude of test equipments are connected to a single common cooling loop. Finally, 10% of the tests are using the "ΔT_j = constant" and 6% the "P_v = constant" control methods. Their use remains for academic purposes, or to separate failure modes.

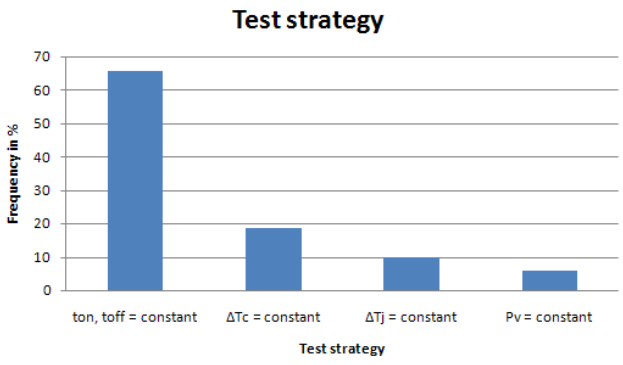


Fig. 15. Histogram showing the test strategies used to test modules

Regarding the measurement of the junction temperature T_j (Fig. 16), the preferred method is the Thermo-Sensitive Parameter (TSP). Optic fibers and thermocouples are used in

about 10% of cases. The Infra-red method, despite its accuracy is used only in 5% of cases due to its expensive cost. One can notice that the TSP method is sometimes coupled with a direct measurement method.

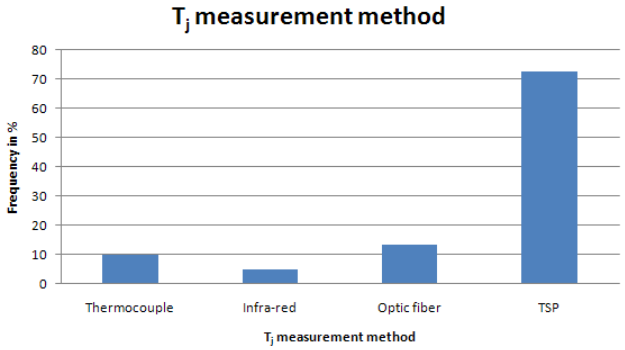


Fig. 16. Histogram showing the junction temperature's measurement methods

There is quite a large variety of failure criteria (Fig. 17). The criterion can be based on 6 different parameters: V_{ce}, R_{th}, Z_{th}, R_{DSon}, I_{GES}, or T_{jmax}. Then the amount of the parameter increase also varies depending on the papers: 5%, 10% or 20% of parameter increases are often used. In some papers no failure criterion is defined and the test lasts until the complete failure of the device, which is referred as the End of Life of the device. Most of tests take an increase of 5% in V_{ce} and of 20% in R_{th} as failure criteria, often in combination. An increase of 20% in V_{ce} is also used as failure criterion in 13% of the tests. The use of R_{DSon} as failure criteria is beginning to expand.

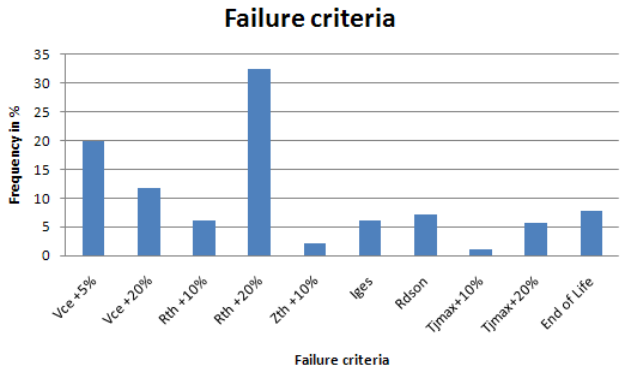


Fig. 17. Histogram showing the failure criteria in use

Finally the variation of different test parameters (T_c, ΔT_j, and t_{on}) was reported. Fig. 18 shows that 39% of the papers did not cycle under different test parameters. Those papers in general are more focused on the understanding of failure mechanisms. For the other papers, the variation of the ΔT_j is often studied. This is done with the perspective of establishing a lifetime curve in function of ΔT_j. Variation of T_c is also quite common. But it is remarkable that only about 6% of publications are interested in the influence of t_{on} on APC results. This is a very small amount.

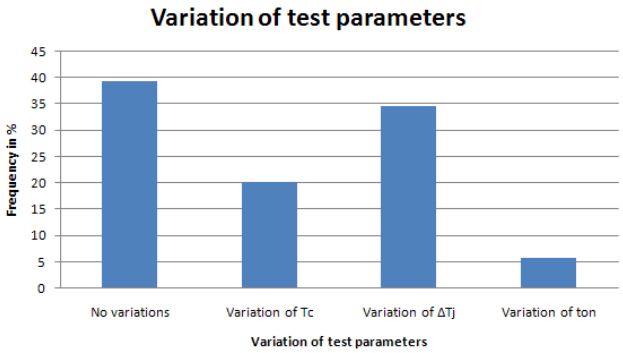


Fig. 18. Histogram showing the test parameters variations studied

This review of the different testing methods used by the 70 publications dealing with APC reveals a quite large variety in terms of control strategies used, as well as temperature measurement methods and failure criteria applied. This can generate a widespread range of the number of cycles to failure for the same kind of module under investigation.

C. *Results analysis and interpretations*

In most of cases, once APC tests are done, a failure analysis is performed. About 35% of the publications are scanning the modules with an Acoustic Microscope (SAM) in order to detect delamination. An Optical Microscope (OM) and a Scanning Electron Microscope (SEM) are both used to analyze 17% of the samples. Cross-sections in the samples are often cut for a detailed observation of the internal structure (15%). More rarely specimens are investigated with techniques like X-ray, Focused Ion Beam (FIB), Differential Interference Contrast Microscope (DICM) or Transmission Electron Microscope (TEM). In papers focusing on wire bonds, shear or pull tests were performed on connected wires, to evaluate their degradation range (Fig. 19).

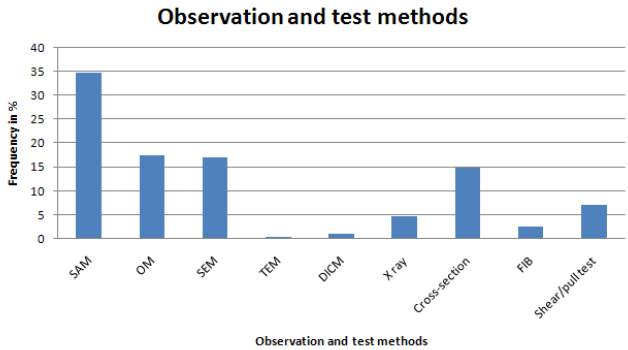


Fig. 19. Histogram showing the observations and tests methods in use

Failure analyses are often dedicated to study one particular layer of the module (Fig. 20). In more than 30% of cases, the die attach is the center of interest, followed by wire bonds studied in 28% of papers. The chip metallization on top of the chip is also frequently observed (18%), as well as the DCB attach (15%). These results are quite logical as the main failure mechanisms appearing in power modules are wire bond

lift-offs or cracking and delamination of solder layers. The Al reconstruction is also a failure mechanism known and discussed since the beginning of APC [28]. The chip and the DCB are not really in focus as failures rarely occur there. The formation and growth of intermetallic at solder layers is observed only in the few papers that are studying deeply the micro-structural changes. The molding compound is also rarely studied, probably because only 18% of the tested devices were encapsulated.

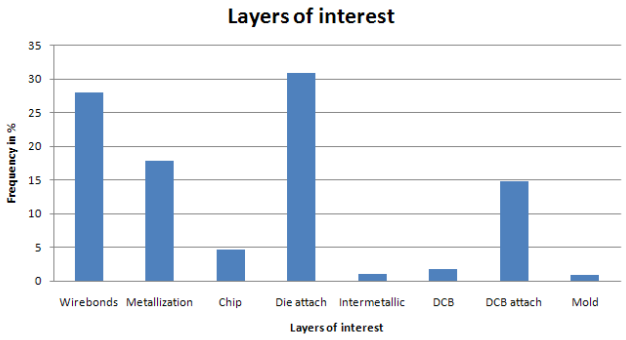


Fig. 20. Histogram showing the layers of interest in failure analyses

The final goals of those studies were identified and classified into 10 categories (Fig. 21). The influence of the design and the process is the most important goal with a frequency of 23%. In these studies, differences between the same type of semiconductor coming from different manufacturers, or modules with different geometries and/or dimensions, or even with different materials or joining processes are investigated and compared. Often it results in a comparison of lifetime models. Lifetime prediction is frequently the ultimate goal of APC publications (20%). Quite often the lifetime predictions are modeled in the form of a curve in function of ΔT_j, which necessitate studying the influence of the temperature (T_c and ΔT_j). Before, in order to be able to develop a lifetime model, the failure mechanisms first had to be known and understood, that is why 14% of the papers are doing failure analyses. To monitor and detect failure apparition, a correlation between the evolution of one parameter and the corresponding failure status would be of great help. This was done in 9% of the studies, with for example a correlation determined between the R_{DSon} value and the delamination area in the die attach [25]. Some other publications are proposing adequate testing methods to investigate either solder degradations or wire bond failures, or some control strategies to reflect well-working conditions. A comparison between failure mechanisms occurring in PTC and APC was made in a few papers [84, 85]. For some others, the main goal was to have a precise idea of the temperature distribution in the whole module, or to investigate the effects of t_{on} on APC results, or to study the micro-structural mechanisms that are taking place in different layers in detail.

It results in most studies focusing on determining the lifetime of improved devices in function of the temperature swing, with wire bonds and solder degradation as the main failure mechanisms. Which makes sense as the semiconductor lifetime is a key factor for a sustainable use of devices and the optimization of its reliability.

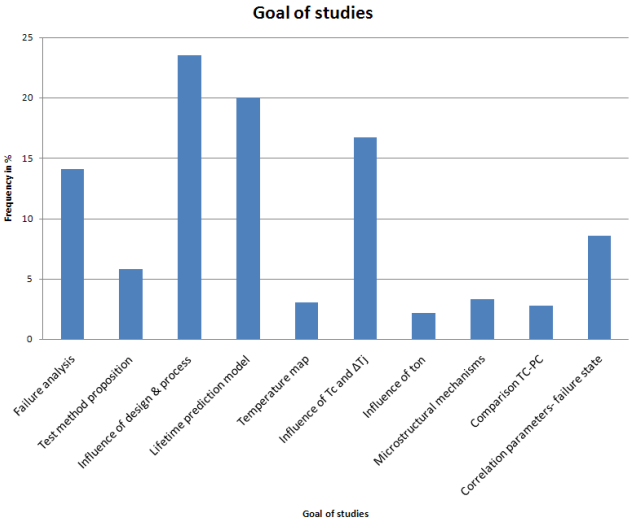


Fig. 21. Histogram showing the goals of the studies

D. *Lifetime prediction*

In order to have an overview of all the APC results obtained from 1993 until now, all the number of failed cycles that were published versus the temperature swings were plotted in Fig. 22. The interpretation of the graph is limited because as just seen, many different devices were tested, with different test conditions. Moreover, the lifetime is not only dependent on the temperature swing but also on other test parameters, thus influencing the results of the tests. However, the temperature swing is a parameter of such large importance, that a trend line can emerge from the graphic.

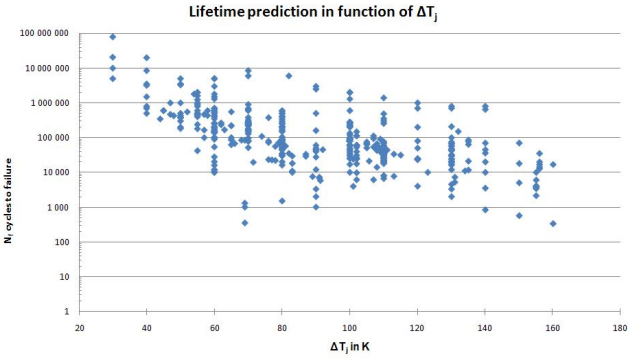


Fig. 22. Number of cycles to failure versus the temperature swing ΔT_j

The number of cycles to failure versus T_{jmin} was plotted in Fig. 23. T_{jmin} is also a test parameter of influence but, here it is difficult to make any interpretations of the results or to distinguish a trend line.

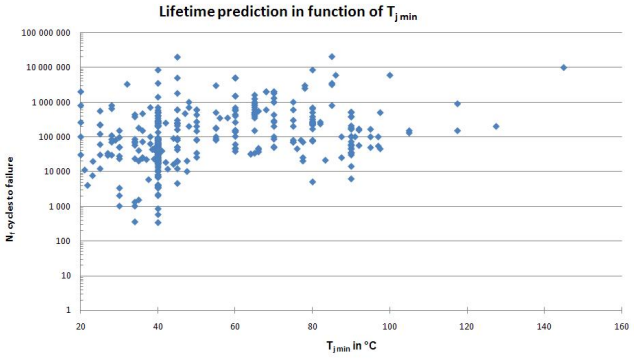


Fig. 23. Number of cycles to failure versus the minimum junction temperature T_{jmin}

Finally the influence of the heating time t_{on} on the lifetime was studied Fig. 24. Unfortunately this information was often missing, which resulted in a smaller data set than for the other diagrams. Some papers did state the cycle times but without mentioning the ratio of on and off times.

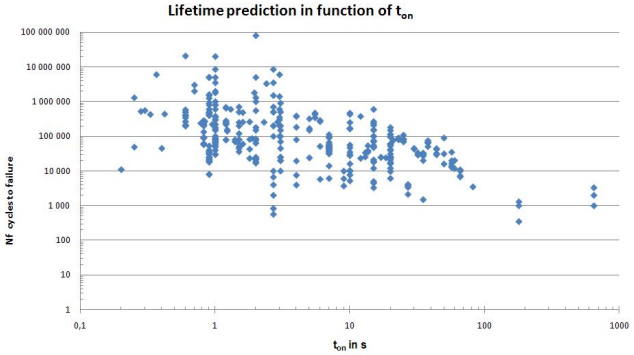


Fig. 24. Number of cycles to failure versus the heating time t_{on}

This study shows that despite the fact that most of the publications are investigating standard modules with a focus on wire bonds and solder degradations, the variety of test set-ups, measurement and monitoring methods as well as control strategies significantly influenced the APC results. The diversity of testing methods was also highlighted by [1]. For the authors, this might be due to the fact that an international standard for APC does not exist. In fact, there are several standards [22, 23, 24] that differ in regards to the main focus of the test.

Moreover, the study reveals that the influence of test parameters on the lifetime was not extensively studied. The influence of the heating time was especially neglected. This can be partially explained by the fact that testing a high number of cycles requires long testing times of several months. This implies that testing a wide-range of application conditions is not feasible. To overcome all these difficulties, a solution could be to simulate APC. Indeed, the problem of testing method diversity would be reduced, and it would no longer be time consuming to simulate APC with varying test parameters.

VII. Statistical State Of The Art In Simulation Of APC

In the same way as it was done for APC tests, 27 publications from 1997 to 2014 dealing with APC simulations were reviewed [77-104]. All simulations were using FEM except two of them, both of which chose BEM in order to simplify the problem to solve [78, 79].

A. Types of device simulated

First of all, the type of the component under study was analyzed, Fig. 25. IGBTs are once again the preferred device as they are simulated in 65% of publications. Then, come MOSFETs and diodes which are both modeled in approximately 10% of the papers studied. TRIAC and DMOS are rarely modeled as these two kinds of devices appear only in 7% of publications; 75% of these devices were modeled in 3D, and only 25% in 2D.

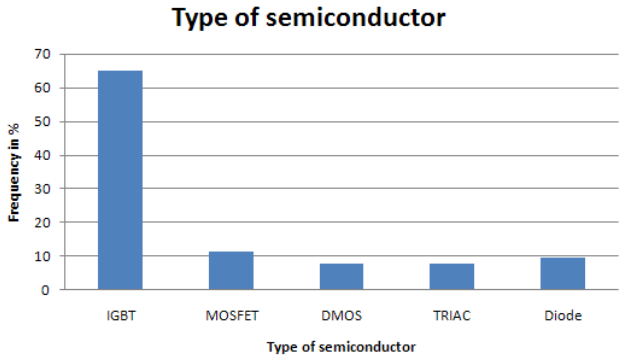


Fig. 25. Histogram showing the type of semiconductors simulated

The internal architecture of the different models was also observed. For 56% of simulations, interconnects were not part of the model, when those were supposed to be Al wires. This can be explained by the fact that modeling a wire is complex, because of its geometry. So, if the study is not especially focused on wire bonds, those ones can be removed from the model for the sake of simplicity. On the other hand, 32% of publications did pay attention to the wires' behavior by including them in the model. Cu clips, Al stripes and Cu wires were modeled as interconnects respectively in 7%, 4% and 1% of papers (Fig. 26). When Al wires were modeled, they were considered to have linear elastic properties except in one a paper [103] which included temperature dependencies and plastic properties. Ag stripes were also modeled with an elasto-plastic behavior, whereas Cu clips and wires were described as linear elastic material.

Almost all devices simulated were supposed to have a metallization of aluminum, but this layer was modeled in only 22% of simulations. On the other hand, every time that the metallization was included in a model, it was with precise material models that took both the temperature dependencies and the elasto-plastic behavior of Al into account. The die itself was made of silicon except for 2% of cases which had

SiC, and the die was always modeled with a linear elastic behavior.

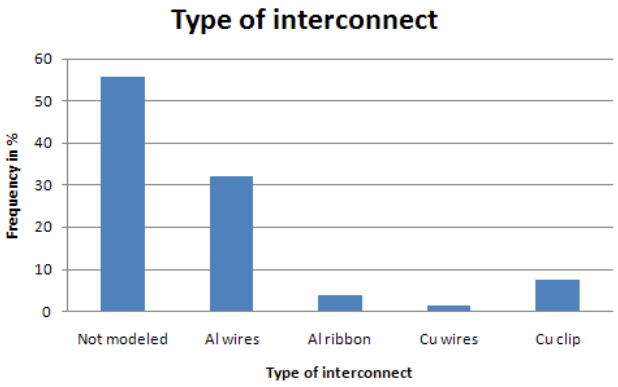


Fig. 26. Histogram showing the type of interconnect of simulated modules

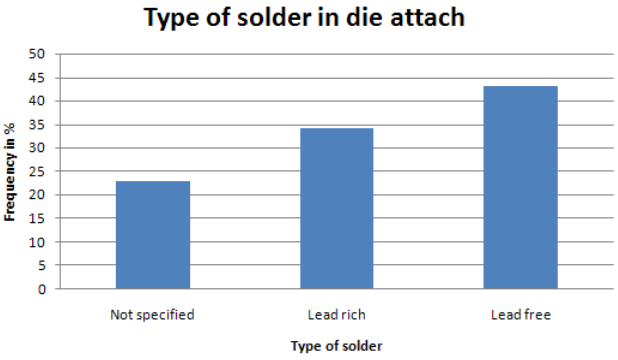


Fig. 27. Histogram showing the type of solder alloy in the die attach of simulated modules

For the die attach, only 8% were Ag sinter joints, the rest was solder joints. Among these solder joints, lead free alloys were used in a majority of cases with 43% of occurrence while lead rich solders were used in 34% of solder layers (Fig. 27). The solder alloy was not mentioned in 23% of papers. Concerning the mechanical behavior of these die attaches, almost 50% were described with a viscoplastic model. Plastic-creep and elastic-plastic models were both employed in about 12% of publications. In 10% of simulations, a simple elastic model was applied for the joint and the other papers did not mention anything on material properties (Fig. 28).

The die was attached to a DCB in 84% of the simulated devices, 9% had a Cu lead frame and the 7% left a PCB (Fig. 29). The type of DCB used was made with Al_2O_3 ceramic to 40% and with AlN to 27%.

The remaining 32% did not specify the type of DCB, which is already a high amount. Copper layers of DCB were considered elastic or elasto-plastic and the ceramic was always linear elastic (Fig. 30).

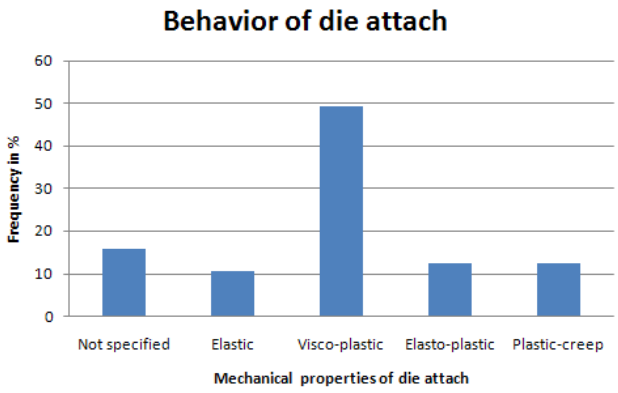


Fig. 28. Histogram showing the die attach mechanical behaviors of simulation models

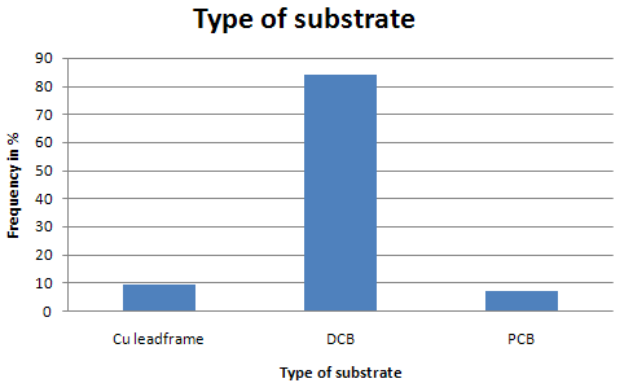


Fig. 29. Histogram showing the type of substrate in simulated modules

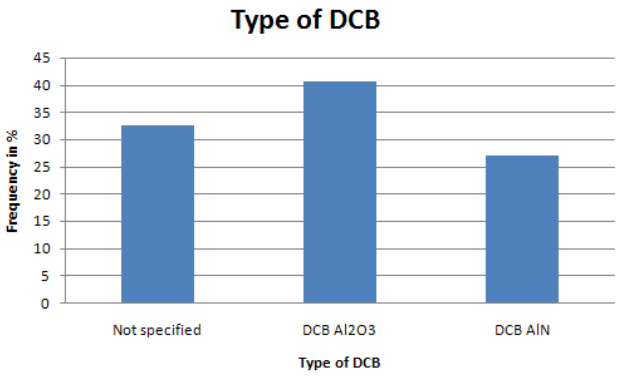


Fig. 30. Histogram showing the type of DCB in modules simulated

33% of modules simulated did not have a base plate. The others were built with a Cu base plate, described with elastic or elasto-plastic material model. The DCB was always soldered to the base plate. In 40% of papers no information concerning the solder alloy was found. A lead-rich alloy was employed in 32% and the 28% left were soldered with lead free alloy (Fig. 31).

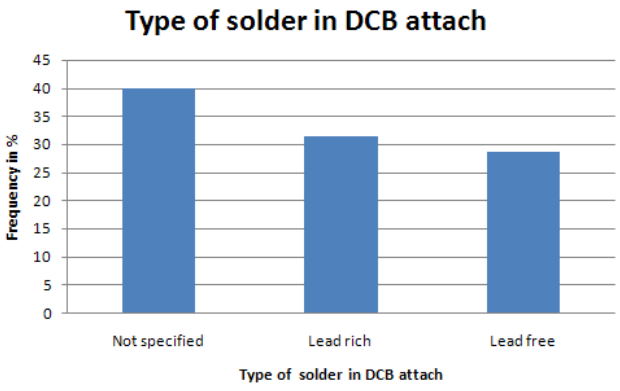


Fig. 31. Histogram showing the type of solder in DCB attach of simulated modules

27% of papers did not precise what material model was used to describe the mechanical behavior of solder. More than 30% of simulations were performed assuming a viscoplastic behavior for solders, whereas plastic-creep, elasto-plastic and elastic behavior were used in 14% each. For the DCB attach, less information was available about the material model than for the die attach. Nevertheless, both distributions are following the same trend with a predominance of viscoplastic models compared to elastic, elasto-plastic or plastic-creep models (Fig. 32).

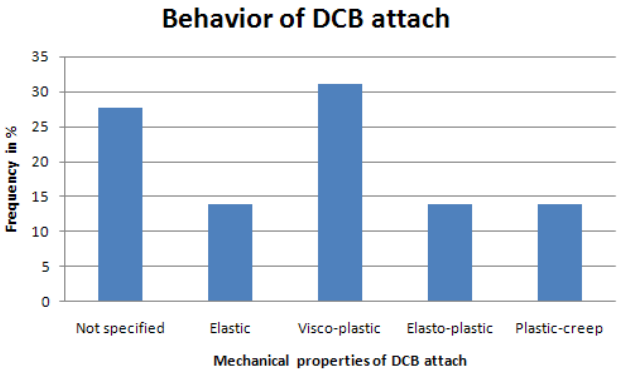


Fig. 32. Histogram showing the type of DCB attach mechanical behaviors in simulated modules

Only 14% of modules were epoxy molded. For 25% of them, the mechanical behavior of the mold was not mentioned. Half of the papers considered the molding compound to be elastic, whereas only 25% took the viscoplastic behavior of the encapsulant into account.

To summarize, the type of modules that were simulated in publications correspond to the ones which were submitted to APC tests. Indeed, IGBT is once again the most studied device. Most of the time, the internal architecture corresponds to a standard structure with Al wires, a chip soldered on a DCB, which is soldered onto a Cu base plate. But in simulations, one can simplify the model to be studied, and quite frequently the Al wire bonds were not included in the model because of their complex geometry. The same was also observed for the metallization, which was often neglected due to its very small dimensions. Quite often, information about materials and their assumed behavior were missing, especially concerning the DCB and DCB attach. Moreover, a relatively wide-variety of material models were used in the different simulations.

B. Types of analysis and loading conditions

The most stimulated APC test is the DC current test, in 90% of the papers studied. PWM tests and superimposed tests are each simulated in about 5% of the cases. This distribution of simulated tests is similar to the one of experimental tests. This is due to the fact that simulation models are often validated with the help of experiments. Indeed, results of both experiments and simulations are compared and should be similar. Moreover, just like for experiments, simulating DC current tests is easier than simulating PWM tests or superimposed tests. However, it is to notice that superimposed tests were simulated, whereas no experimental tests were performed. This shows that even though superimposed tests are complex to model, it is still easier to simulate such a test than to set up a complete test bench.

The type of analysis use to simulate APC was also taken into account. 26% of simulations are electro-thermal and 67% are thermo-mechanical analysis. Some papers did both kinds of simulations, one after the other [97, 99, 101, 103]. The 7% left were purely thermal simulations.

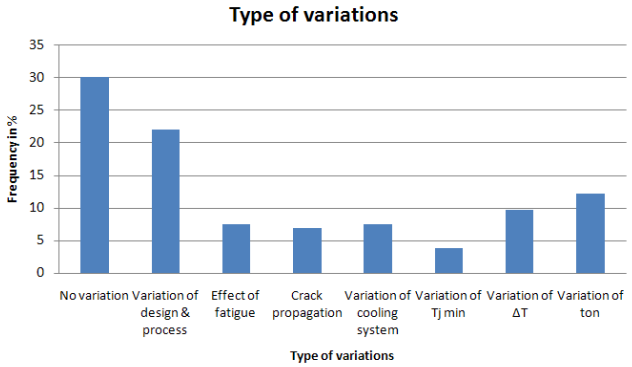


Fig. 33. Histogram showing the type of variations studied with simulation

The different parameter variations and design effects studied were identified and plotted in Fig. 33. 30% of papers did not manage to perform any variations of neither the test parameters nor the design. 22% made variations in geometrical design, materials and processes. ΔT_j and t_{on} variations were studied in respectively 9% and 12% of simulations. 7% of papers choose to respectively study variations of cooling systems, the effect of fatigue by including delamination areas in the model, and crack propagation under APC. A few other studies focused on the variations of T_{jmin}. This shows that a wide-range of test parameters variations was studied in a relatively small amount of publications.

C. *Results analysis and interpretations*

Layers on which papers are focusing were reported, and the corresponding distribution is shown Fig. 34. The first layer of interest appears clearly: the die attach was in focus in 36% of papers. The chip comes in second with 26% of papers that concentrate on its behavior. Wire bonds are also of big interest for 10% of studies. The DCB and metallization have both 9% of publications focusing on them. Surprisingly the DCB attach was the object of study for only 8% of papers. The difference in interest between the die attach and DCB attach is quite important, although both solder joints are subjected to degradation under APC. This can be explained by the fact that not every module had a base plate and thus a DCB attach layer. But it might also come from the fact that solder degradations are more extensively studied under PTC, as this test is more critical for solder layers due to the long dwelling time. The interconnect attach is also not frequently studied, as this layer is only present in modules using a Cu clip instead of wire bonds.

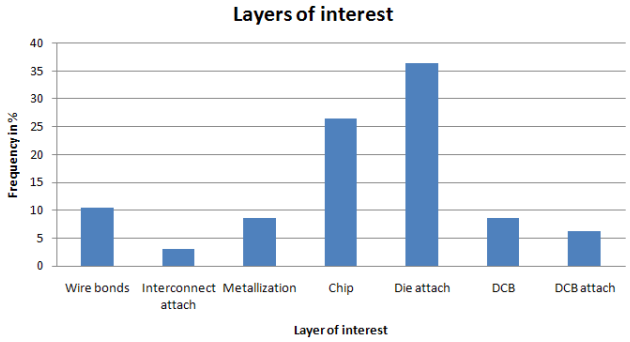


Fig. 34. Histogram showing the layers of interest in simulations

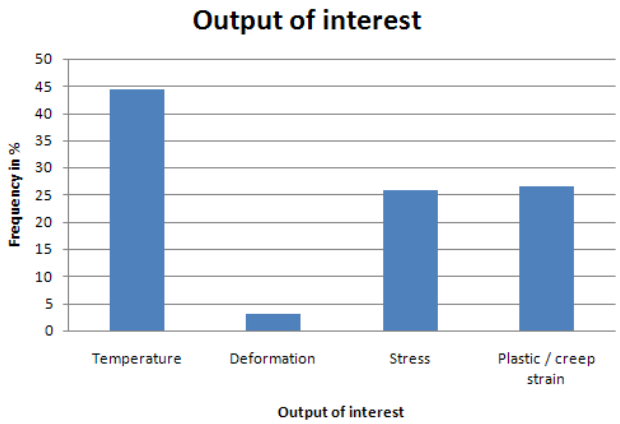


Fig. 35. Histogram showing the outputs of interest in simulations

The results obtained via simulations were analyzed, and 4 main outputs of interest emerged from them: temperature, deformation, stress and strain. These results were often shown as a map of the entire module. The voltage was also often observed, but it was not taken into account here, as the study is more focused on the thermal and mechanical behavior of modules rather than on their electrical behavior. Determining the temperature distribution through the module was the first interest of these studies. In about 45% of publications a temperature map was shown. Stresses and strains were also of importance, as each of them is discussed in 25% of papers. The deformation was observed only in a few papers which were looking more precisely at the phenomenon of metallization reconstruction [87, 90] (Fig. 35).

Finally the different goals of the studies were highlighted and plotted in Fig. 36. For 24% of papers studied, the main objective remains to understand the mechanisms that take place in modules. Then, 20% of papers focus on design and process optimization. The lifetime prediction is a goal of more than 15% of simulations. 11% of papers wanted to characterize and understand the differences between PTC and APC. Determining the influence of temperature on the number of cycles to failure was also an important point. Some papers look at the influence of fatigue on the APC results, for example by simulating a delamination area in a solder layer. Others wanted to determine the temperature profile of the module during power pulses. Papers which have made PWM power cycling manage to compare the results obtained with both DC current and PWM tests. Few studies also investigated the influence of cooling systems on the APC results of a module. Finally, very few simulations had the objective of studying the influence of the heating time t_{on} on the behavior of the module. This is quite surprising, as once the model is set up, simulation could be an appropriate tool when testing different combinations of test parameters. One can also notice that the goal was quite different depending on the study; a relatively large range of aspects influencing APC results was reviewed. But the main problem remains to understand mechanisms, optimize design and determine the lifetime of modules.

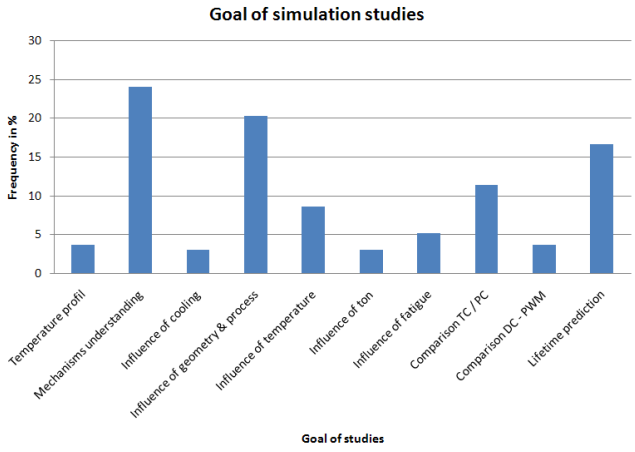


Fig. 36. Histogram showing the goals of the simulations studies

These statistics give an overview on APC simulation studies and reveal the simulation trends in power electronics. But relations between the architecture of the module, the method employed to simulate materials behavior and the objectives to reach, are not visible. Thus, the Table 1 describes the module and the material behavior simulated as well as the objective of each study. Information is given for all the 27 papers dealing with APC simulation that were reviewed.

N	Ref.	Semiconductor	Analyse	Interconnect	Die attach	DCB attach	Objectives
1	[78]	IGBT	TM	Not modeled	solder elastic	solder elastic	Determine the influence of geometry and process on stress distribution in DCB
2	[79]	IGBT	T	Not modeled	solder	solder	Determine the influence of geometry and process on temperature distribution in chip and DCB attach
3	[80]	IGBT	ET	Not modeled	lead-rich	lead-rich	Determine the temperature distribution in chip and DCB
4	[81]	IGBT	TM	Not modeled	lead-rich/free elasto-plastic	solder elasto-plastic	Study of plastic strain in die attach to determine the influence of geometry, process and temperature parameters and predict lifetime
5	[82]	MOSFET	TM	Not modeled	lead-rich visco-plastic		Study of temperature, stress and plastic strain in die attach to predict lifetime
6	[83]	IGBT	TM	Not modeled	lead-free visco-plastic	lead-rich visco-plastic	Study of temperature and stress distribution in chip, DCB and DCB attach to compare PTC/APC
7	[84]	IGBT	TM	Not modeled	lead-free visco-plastic	lead-rich visco-plastic	Study of temperature and stress distribution in chip and DCB to determine the influence of temperature parameters
8	[85]	Diode	TM	Not modeled	lead-free visco-plastic		Compare PTC/APC for stress and plastic strain in die attach
9	[87]	TRIAC	TM	Cu clip elastic	lead-rich visco-plastic		Study of stress distribution in interconnect attach and die attach to understand the mechanisms
10	[88]	DMOS	TM	Not modeled			Study of temperature, deformation, stress and plastic strain in metallization and chip to understand the mechanisms
11	[89]	IGBT	TM	Not modeled	lead-rich	lead-rich	Study of stress distribution in the die attach to understand the mechanisms
12	[90]	TRIAC	TM	Cu clip elastic	lead-rich visco-plastic	lead-rich visco-plastic	Study of plastic strain in interconnect, die and DCB attaches to determine the influence of geometry, process, temperature and ton parameters and predict lifetime
13	[91]	DMOS	ET+TM	Not modeled			Study of temperature, deformation, stress and plastic strain distribution in metallization and chip to understand the mechanisms and predict lifetime
14	[92]	IGBT	ET	Not modeled	solder	lead-rich	Study of temperature distribution in chip to compare DC/PWM tests
15	[93]	IGBT	TM	Not modeled	lead-free elasto-plastic	lead-free elasto-plastic	Study of temperature and plastic strain distribution in chip and die attach to understand the mechanisms
16	[94]	IGBT + Diode	TM	Al wires elastic	lead-free visco-plastic		Study of temperature and plastic strain in chip and die attach to determine the influence of geometry and process and predict lifetime
17	[95]	Diode	T	Al + Cu wires elastic	Ag sintered	solder	Determine the influence of geometry and process on temperature distribution in chip and die attach
18	[96]	IGBT	TM	Al wires elastic	solder visco-plastic	solder visco-plastic	Study of temperature and plastic strain distribution in chip and die attach to determine the influence of geometry, process and ton parameter and predict lifetime
19	[97]	IGBT	TM	Not modeled	lead-rich visco-plastic	lead-rich visco-plastic	Study of stress and plastic strain in die attach and DCB to compare PTC/APC and predict lifetime
20	[98]	IGBT	ET+TM	Al wires elastic	lead-free plastic-creep	lead-free plastic-creep	Study of temperature and creep strain distribution in die attach to understand the mechanisms , determine the influence of temperature parameters and fatigue and compare PTC/APC
21	[99]	MOSFET	ET	Al wires elastic	lead-rich		Study of temperature distribution in metallization and die attach to determine the influence of geometry, process and fatigue
22	[100]	IGBT	ET+TM	Al wires elastic	lead-free plastic-creep	lead-free plastic-creep	Study of temperature and creep strain distribution in die attach to determine the infuence of fatigue, compare PTC/APC and predict lifetime
23	[101]	MOSFET	ET	Al wires elastic	solder		Study of temperature distribution in wire-bonds, metallization and chip to determine the influence of cooling systems, geometry, process and fatigue
24	[102]	IGBT	ET+TM	Al ribbon elasto-plastic			Study of temperature and plastic strain in wire bonds to understand mechanisms, determine the influence of geometry, process, temperature parameters and predict lifetime
25	[103]	IGBT	ET+TM	Al wires elastic	lead-free	lead-free	Study of temperature and stress distribution in wire bonds to understand the mechanisms
26	[104]	IGBT	ET+TM	Al wires elasto-plastic	lead-free elastic	lead-free elastic	Study of temperature, stress and plastic strain distribution in wire bonds and metallization to determine the influence of temperature and predict lifetime
27	[105]	IGBT	TM	Not modeled	Ag sintered elasto-plastic	solder	Study of temperature, deformation and stress distribution in chip to understand the mechanisms and determine the influence of cooling systems

ET: Electro-Thermal
T: Thermal
TM: Termo-mechanical

Table 1: Summary of module and material model simulated in relation with the objectives of the studies

D. *Lifetime prediction based on simulations*

Numbers of cycles to failure obtained with simulation were plotted in function of the temperature swing ΔT_j, Fig. 37. The quantity of data available was quite limited. The difference in the number of data obtained with papers performing APC tests is really important. Plotting the lifetime prediction in function with the heating time or the T_{jmin} was not even possible because of missing data.

To conclude this review, FEM simulations are still not extensively used to study APC. Until now, studies using simulations are concentrated on standard modules with Al wires as interconnect, an IGBT chip soldered to a DCB, soldered itself to a Cu base plate and without encapsulation. Models are often simplified and do not take all actual present layers in the module into account. Too many times, the material model was not mentioned and for some materials the model used to describe the mechanical behavior was not precise enough. Studies are mainly focused on the die attach, the chip and wire bonds. The temperature distribution is still of prime interest, before stress and strain distribution. Main goals of these studies are: first to understand the mechanisms occurring; then optimize the design of modules and predict the lifetime. The influence of many different effects on different test parameters was studied, but only superficially. As of now, no publication which has managed to test different combinations of parameters and report their influences on APC results has been found. In simulations just like for experiments the study of the influence of heating time on modules under APC is neglected. But one should take advantage of simulation and intensively study the influence of different combination of parameters on the mechanical behavior of modules. Indeed, in simulation, once a model is set up and validated, it is quite easy to modify some parameters and restart an analysis.

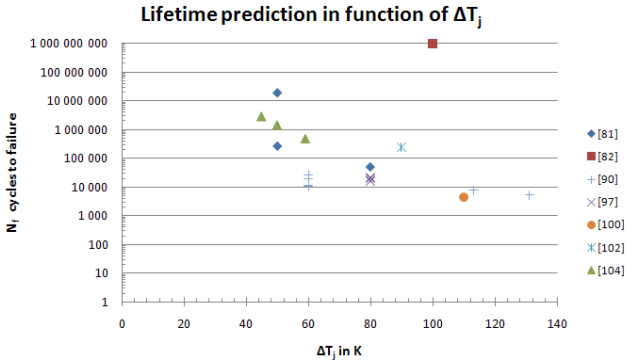


Fig. 37. Number of cycles to failure predicted via simulation versus the temperature swing ΔTj

VIII. Conclusion

This review of studies on APC tests and simulations reveals that until now, the power modules under study correspond to standard modules with Al wires bonded to a Si chip soldered on a DCB, itself soldered on a Cu base plate and without epoxy molding compounds. It is only very recently that a few publications are managing to study modules with new technologies like SiC chip or Cu wires or clip or Ag sinter joint. Moreover, it was highlighted that a variety of test methods are available to perform APC tests, leading to quite different reliability results. This leads to think that one international standard should be defined to regulate the practice of APC tests. Besides, performing APC test is time consuming and impedes to carry out a thorough study on the influence of tests parameters on the reliability of power modules. Thus numerical simulations can be considered as an interesting tool used to overcome these experimental difficulties and analyze the behavior of power modules under varying test conditions. But actually, the use of simulations to determine the power cycling reliability is still quite recent and not very common. Less than half the number of papers dealing with APC tests was found regarding APC simulations. Furthermore, these studies dealing with APC simulations had quite different goals and were focusing mainly on one or two determined layers. This meaning that, despite the easy reproducibility of an analysis and the rapidity of calculation allowed by simulations, no extensive numerical study on the influence of test parameter on reliability was carried out. Thus, this review highlights a lack of numerical investigations on the influence of tests parameters, especially for power modules with new technologies.

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