Online Chip Temperature Monitoring Using υ_{ce}-Load Current and IR Thermography

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***Abstract*—This paper presents on-state collector-emitter voltage ($\upsilon_{ce,on}$)-load current (I_c) method to monitor chip temperature on power insulated gate bipolar transistor (IGBT) modules in converter operation. The measurement method is also evaluated using infrared (IR) thermography. Temperature dependencies of $\upsilon_{ce,on}$ at load current is measured and temperature dependency calibration factor is formulated. This method needs a correction to compensate a deviation in the interconnection resistance from homogeneous temperature field in calibration to non-homogeneous field in loading. The correction parameter is obtained from a static calibration and the method is proposed in the paper. Ageing compensation in estimating the temperature is illustrated. The correction parameter is also analysed in finite element model and also investigated experimentally superimposing heat by conducting device for a longer time in the calibration.**

I. Introduction

Thermal systems are designed based on operating ($T_{vj,op}$) and maximum operating temperature ($T_{vj,max}$) provided by semiconductor manufacturers in power electronics [1]. Hence, it is important to monitor electrical and thermal parameters to operate within a design limit. Until today, there is still a challenge to implement $T_{vj,op}$ monitoring for field applications [2]. During converter operation, heat is generated by switching and conduction loss in semiconductor chips inside a power module. Effectively, the losses evolves temperature gradients laterally and also in series interconnections. However, the amplitude of temperature and it's gradient are governed by materials used, cooling interface, and power density.

Challenges for module technology are high current density (require good interconnects), high power density (low thermal resistance), and high switching speeds (low inductance). Temperature is neither simply proportional to the power consumption nor to power density. However one can either reduce power or increase area to reduce the temperature. The temporal and spatial distribution of temperature also needs to be considered for high frequency switching applications, because of larger time constant of a chip and package tends to filter out fast changes in temperature. Similarly, for power changes over a small dimension, high spatial frequency temperature may filter out. Generally, these effects are modelled by solving heat diffusion/convection equations [3].

Generally, single junction temperature is used to model chip temperature in a chip and package related thermal design, which is not sufficient for power-constraint design. Increasingly non-uniform power dissipation across the chip leads to local hot spots and elevated temperature gradients across the silicon die. The spatial distribution in chip is high. Hence, a temporal and spatial distribution of temperature consideration is required.

The scope of temperature monitoring using this method can be applied for several applications namely: reliability studies, short time overload control, uprating/ derating power control, preventive maintenance, improve thermal design etc.

Initially, a brief overview on temperature estimation methods is given. The proposed method is introduced and experimental test setup is described. Implementation of this technique is illustrated and method to obtain correction parameters is described. Finally, temperature measurement using both infra-red (IR) thermography and the proposed method are evaluated in the paper.

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II. Overview of Temperature Estimation methods

Temperature sensitive electrical parameters (TSEPs) from static and dynamic characteristics are preferable methods to estimate temperature in converter operation. However, the options are limited in implementing for real time monitoring [2] [4] [5] [6] [7].

Modern devices have a built-in NTC thermistor on top of the baseplate, which is located on the edge of baseplate hence is not able to detect the chip temperature. Thus, two major approaches, such as analytical (electro-thermal models of devices) and physical (measurement) are being used for a chip temperature estimation. In the first method, an accurate 3D structure finite element model (FEM) could give a close temperature field, but it requires post-processing, and often takes a long computational time. In the second method, direct and indirect measurements can be done. In a direct method, a temperature sensor can be integrated directly onto a chip, such as thermocouple or fiber optics with/without a temperature sensor. Similarly, temperature field can be measured by an IR thermal camera. However, these methods require modification on a device packaging as well as pose functional limitations to implement in a converter. In an indirect method, several TSEPs can be used which are more application oriented. Hence, innovative measurement methods are being introduced lately. Mainly, dynamic and static characteristics of a power module (PM) can be utilized to find temperature dependencies with a function of gate voltage, I_C, and forward voltage drop. In dynamic characteristics, IGBT turn-on [8], turn-off, peak gate current [9] and rise time are used, where gate resistance and parasitic capacitances are the dominating parameters.

In static characteristics, $\upsilon_{ce,on}$ is used in both low current and high current methods. In a low current method, a small current runs through the device when converter is offline. Therefore, it has a negligible contribution to device heat up. However, it requires a modification in converter control, halting normal operation for a short period of time during the measurement. On the other hand, high current method introduces self-heating, if the calibration is not conducted in a short time. In addition, $\upsilon_{ce,on}$ changes due to the temperature gradient in series interconnection. Nonetheless, this method is regarded as a suitable and cheaper technique in real-time operation, though maintaining an accuracy and implementing in the operation are still challenging. A key benefit is that this method does not require any functional or structural modifications in the converter. However, the measurement circuitry has to fulfill certain requirements to estimate the chip temperature.

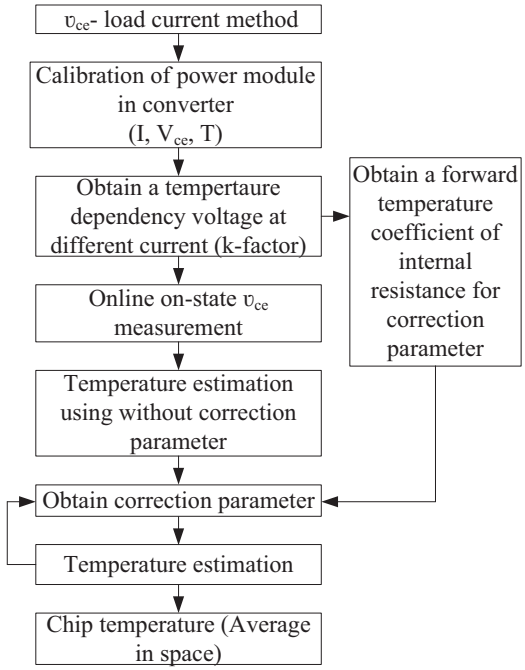


Fig. 1. A layout of chip tempertaure monitoring using a υ_{ce}-load current method.

III. υ_{ce}-Load Current Method

A layout of measurement steps in this method is given in Fig. 1. The measurement is conducted mainly in two steps; firstly a calibration is conducted to obtain a calibration factor. Secondly, actual $\upsilon_{ce,on}$ is measured at load currents. The final temperature estimation includes correction parameter, calibrated reference voltage and real time measurement data. Because of a higher sensitivity, the online measurement of $\upsilon_{ce,on}$ and load current demands higher accuracy.

In PMs, the total $\upsilon_{ce,on}$ includes voltage dropped in packaging (bond wires, solder, metallization etc.) and the chip. The $\upsilon_{ce,on}$ is modelled using a Shockley model with a series resistor as given by Eq. 1 from static characteristics.

$$\upsilon_{ce,on} = \eta.V_T.ln(\frac{i_C}{I_S}+1) + i_C \times R + V_o \tag{1}$$

$$V_T = \frac{k_B T_j}{q}.i_C \tag{2}$$

Where η is a ideality factor and V_T is the thermal voltage as given in Eq. (2). i_C, I_S and V_o are collector current,

saturation current, and offset voltage, respectively. K_B is a Boltzmann constant ($1.3806488e^{-23}\ J/K$) and q is electron charge ($1.602176565\ C$). In this method, the measurement circuitry should fulfil essential requirements to estimate temperature average in space ($T_{avg,sp}$) as listed;

- Sensitivity: Minimum of $1\ mV/°C$ would be better,
- Measurement accuracy: Minimum of $1\ mV$ would be better,
- Measurement resolution: $0.61\ mV$,
- Calibration time: As short as possible, in case of $P3$ module (used in this paper) for less than $200\ uS$,
- Homogeneous temperature field across module during calibration,
- Ageing compensation: varies with the packaging from ageing, typically $20\ mV$ in $P3$ module,
- Failure compensation: varies with the packaging mainly from bond wire lift-off, typically $5\ mV$ to $7\ mV$ in $P3$ module.

IV. Experimental Setup

In order to emulate field operating stress, the device under test (DUT) is used in 3-legs power converter [10], as shown in Fig. 2a. The DC-link voltage (V_{DC}) is reduced to $450\ V$ for an open module, where the DUT is used only to evaluate the method with IR thermography. The DUT consists of six half-bridge sections sharing the load current. To capture temperature field in the DUT, the converter setup is reconfigured as given in Fig. 2b. For this test, initially open DUT (rated as $1\ kA$, $1.7\ kV$) is prepared for the test as demonstrated in Fig. 2b. The online $\upsilon_{ce,on}$ monitoring circuit is shown in Fig. 3, details in measurement are available in [10].

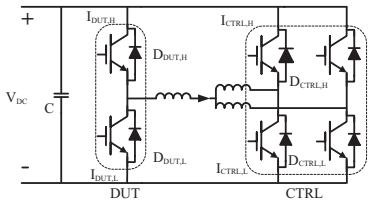
In Fig. 2a, $I_{DUT,H}$, $D_{DUT,H}$, $I_{DUT,L}$, and $D_{DUT,L}$ are high side IGBT, high side diode, low side IGBT, and low side diode for DUT. Similarly, CTRL is control sides of test converter.

V. Measurement Technique

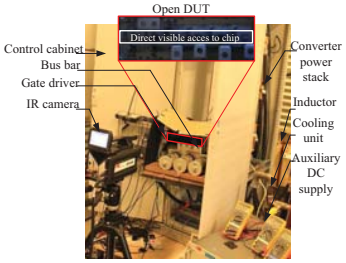
Fig. 1 illustrates the monitoring procedure, in the following sections the methods are described in detail.

A. Calibration

A characterization process called a current-plateau method is introduced, which can be implemented in converter. In this method, load current is initially raised to desired value in $100\ \mu s$. Current is circulating through devices for a short time $40\ \mu s$ as shown in Fig. 4, while the $\upsilon_{ce,on}$, i_c, and T are measured. A $2\ \mu s$ second ramp up is used in the same routine to calibrate diode of



(a) A converter layout.



(b) A test setup.

Fig. 2. Experimental test setup (a) layout of converter (b) test setup for IR thermography.

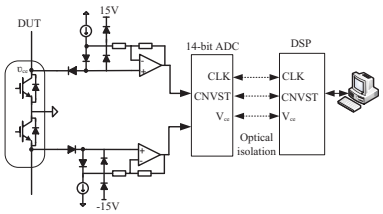


Fig. 3. $\upsilon_{ce,on}$ monitoring circuit.

opposite side (bottom or upper) at the same time. The temperature rise is also monitored through a IR camera, as shown in Fig. 5. Calibration factor (K-factor) gives the temperature dependency on $\upsilon_{ce,on}$ of each device at load current. This can be calculated by using on-state υ_{ce} at two different temperatures for each load current.

$$\mathrm{K} = \frac{T_{cal2} - T_{cal1}}{\upsilon_{ce2,_{cal2}} - \upsilon_{ce1,_{cal1}}}, \tag{3}$$

A major limitation using load current for characterization

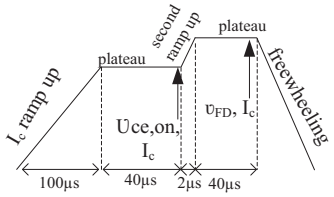


Fig. 4. $\upsilon_{ce,on}$-(T) calibrating current.

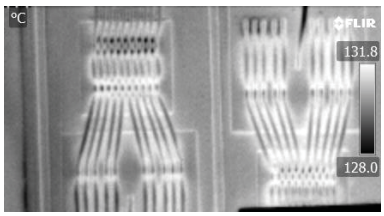


Fig. 5. Tempertaure field at high temperature during calibration.

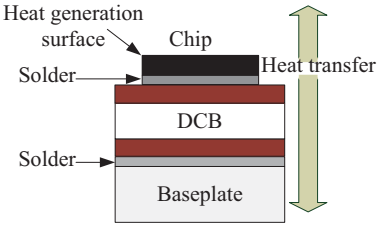


Fig. 6. A vertical cross-sectional layers shwoing a heat flow during calibration.

is that the high current heat up the device as shown in Fig. 6. However, this can be minimized using a short turn-on time. The heat up during calibration is investigated by increasing plateau time at different temperatures. Here the baseplate temperatures are considered at $40°C$, $60°C$ and $80°C$, see Fig. 7.
The power loss during calibration is obtained as given in Eq. (4):

$$\begin{aligned} P_{tot} &= \frac{1}{t_o}\int_{t_o} \upsilon_{ce,on}(t,i_c)i_c(t)dt \\ &= \frac{1}{t_o}\int_{t_o} R_{ce}(i_c)i_c(t)^2dt; \quad i_c = I_p \\ &= R_{ce}I_p^2 \end{aligned} \tag{4}$$

If one regards the heating of the chip as a simple 1D system. The heating during calibration can be calculated from standard calorimetry combined with an outward flux. If this carried out in small time steps compared

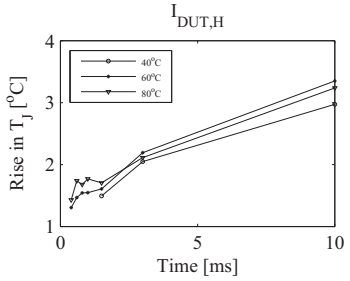


Fig. 7. Rise in T_j during calibration.

to the heating (finite difference method) the temperature is obtained:

$$\begin{aligned} Q &= \rho C_p(T - T_o) \\ Q &= R_{ce}I_p^2 t_o - q_{sp}t_o \end{aligned} \tag{5}$$

$$T = \frac{R_{ce}I_p^2 t_o}{\rho C_p} - \frac{q_{sp}}{\rho C_p} + T_o \tag{6}$$

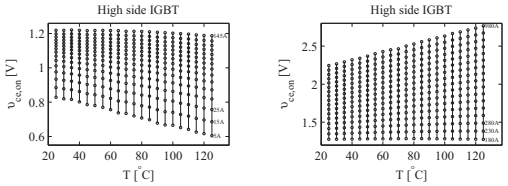
In summary,

$$\delta T(t) = \frac{1}{\rho C_p}(R_{ce}I_p^2 t_o - q_{sp}(\delta T, t)t) \tag{7}$$

Solving heat energy and power module geometry parameters Eqs. (5) to (7), a final Eq. (8) is introduced. The final Eq. (8) is used for estimation of temperature increase.

$$\delta T = \delta T(t_o) + \int_{t_o}^{t_1} \frac{q_g - q_c}{c_p \nu \rho} dt \tag{8}$$

where q_g is the generated heat by the current load, q_c is the heat dissipating away from the chip, and $c_p \nu \rho$ are material/ geometry parameters. The heat dissipation is calculated using the direct copper bonded (DCB) thermal impedance and capacitance. Generated heat is derived from a Shockley model with a series resistor, see Eq. 1, in order to remove the contribution from interconnections it's contribution is subtracted. The temperature during calibration is estimated based on simple $1D$ finite difference approach, which is validated using a finite element simulation method (FEM) and IR thermography. The



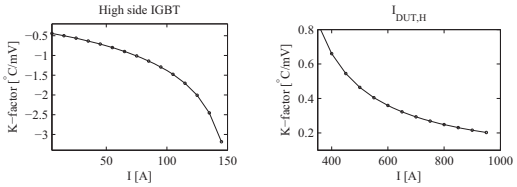
(a) At NTC current. (b) At PTC current.

Fig. 8. Voltage and temperature dependency at NTC and PTC for HS IGBT.

calibration is conducted for $25°C$ to $125°C$ at the load current from $5\,A$ upto $1000\,A$. Fig 8 shows voltage and temperature dependency at negative temperature coefficient (NTC) and positive temperature coefficient (PTC) for high side IGBT. At NTC to PTC cross-over current, the υ_{ce} is temperature independent, hence has large K-factor as well as error in the temperature estimation. Therefore, in final calculation, the load current close to cross-over magnitude can be ignored. In the formulation

of K-factor, the contribution of voltage drop in series elements are cancelled for the same current level.

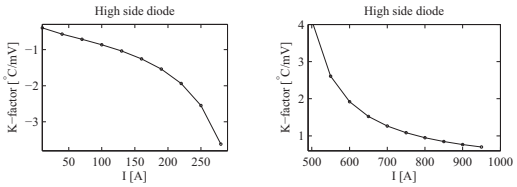
The K-factors for HS IGBT for both NTC and PTC



(a) At NTC current. (b) At PTC current.

Fig. 9. Current and temperature dependency at NTC and PTC for HS IGBT.

are shown in Fig. 9. Similarly, the K-factors for HS diode for both NTC and PTC are shown in Fig. 10.



(a) At NTC current. (b) At PTC current.

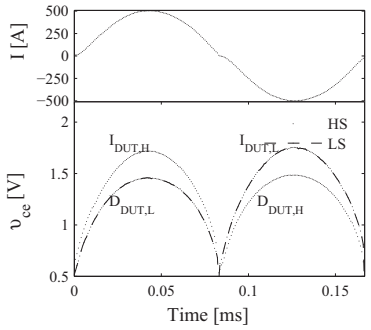
Fig. 10. Current and temperature dependency at NTC and PTC for HS diode.

B. Measurement in a Converter Operation

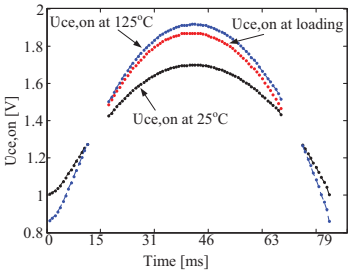
The online voltage ($\upsilon_{ce,on}$ and $\upsilon_{FD,on}$) is measured using a circuitry, see Fig. 3, with a 1 mV accuracy. The open DUT is switched at 2.5 kHz and tested at 6 Hz sinusoidal current in a converter as shown in Fig. 11a. Here $\upsilon_{ce,on}$ and load current are measured on each switching modulations [10]. During measurement, the temperature field is also monitored through a high resolution IR camera ($X8400SC$). Fig. 11b shows current and $\upsilon_{ce,on}$ measurement in an open module, where the device is operated for $500A_{Peak}$ at $6Hz$ output frequency. A full IR thermography image of active area of DUT is depicted in Fig. 12a. Similarly, an isothermic temperature profile from left to right is demonstrated in Fig. 12b for LS diode and HS IGBT.

C. Correction Parameters

The temperature estimation process involves two major steps: calibration and normal loading, where dynamics of temperature profile changes from homogeneous to non-homogeneous. Based on two different behaviours of temperature profiles, two correction parameters are



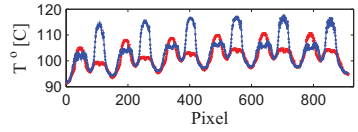
(a) I, $\upsilon_{ce,on}$ and υ_{FD} measurement for one cycle.



(b) $\upsilon_{ce,on}$ calibrated at 25°C and 125°C and during converter operation at $500A_{Peak}$ for $I_{DUT,H}$.

Fig. 11. Online measurement of (a) I, $\upsilon_{ce,on}$ and υ_{FD} measurement for one cycle, (b) $\upsilon_{ce,on}$ calibrated at 25°C and 125°C and during converter operation at $500A_{Peak}$.

(a) A full thermography image of chip area.



(b) An isothermic profile from left to right for LS diode is conducting.

Fig. 12. A full IR-thermograpgy image of P3 module at 500 A_{peak}.

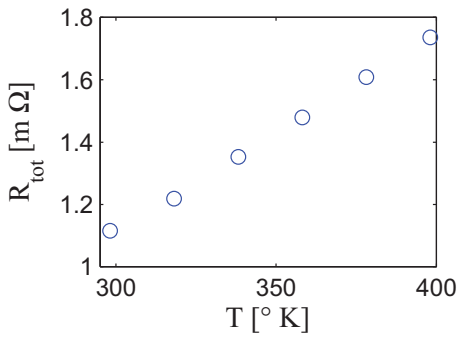


Fig. 13. Rise in internl resistance as a function of tempertaure.

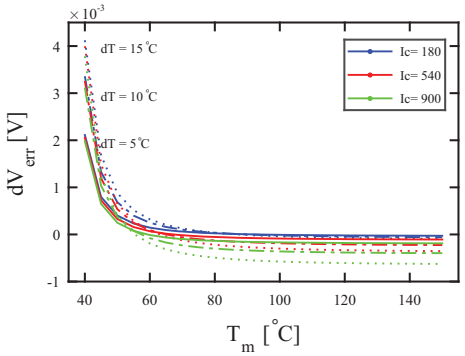


Fig. 14. $\Delta\upsilon_{err}$ at different current and ΔT on a IGBT obtained from a FEM simulation.

introduced. T_{cor} is the heat up during calibration, see Fig. 7, which has to be added to the reference temperature. However, this parameter has limited influence on the estimation process, because the calibration is completed in 140 μs. Another major correction parameter is $\Delta\upsilon_{err}$, which is the correction in forward voltage from a homogeneous calibration temperature field to an online inhomogeneous field. The $\Delta\upsilon_{err}$ depends on packaging and location of a chip. Fig. 13 shows internal resistance obtained from a Shockley model with a series resistor as given in Eq. (1) from the calibration. Using this model, the temperature coefficient is found $0.0042/K$, which is close to the temperature coefficient of Al. This provides a qualitative idea that the resistance is mainly contributed by bond wires and metallization. A resistance with a function of temperature (R_{slope}) is obtained as $6.27e^{-6}\ \Omega/K$ for HS IGBT. Similarly, the R_{slope} is also obtained for other devices: LS IGBT ($12.56e^{-6}\ \Omega/K$), HS diode ($5.56e^{-6}\ \Omega/K$) and LS diode ($4.7e^{-6}\ \Omega/K$) from a static calibration. The R_{slope} will be used to obtain $\Delta\upsilon_{err}$ for individual component during the temperature estimation. This $\Delta\upsilon_{err}$ correction depends on the difference in chip temperature from center to edge, see Fig. 14 obtained from a full FEM simulation. The $\Delta\upsilon_{err}$ from the simulation shows a linear and steady change at high temperature. Later the effective change in resistance from simulation is also compared with R_{slope} and found very close to a typical value. In spite of these correction parameters, a recalibration of power module is required to remove the ageing effect on on-state voltage drop.

D. Temperature Estimation

The K-factor is used to obtain chip junction temperature from the TSEPs as given in Eq. (9). Initial T_j is calculated without using correction parameters.

$$T_j = T_{ref} + K(\upsilon_{ce,meas} - \upsilon_{ref}(T_{ref})) \tag{9}$$

The correction parameter $\Delta\upsilon_{err}$ is obtained from T_j, corresponding baseplate temperature and R_{slope} at corresponding load current using an Eq. (10). Here a scaling factor (SF) is required. The factor may changes depending upon the location and packaging of power modules.

$$\Delta\upsilon_{err} = (T_j - (T_b) \times R_{slope} \times i_L \times SF \tag{10}$$

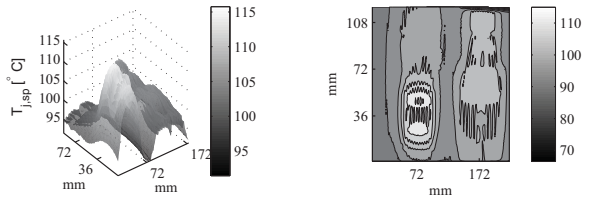
Finally, after obtaining a $\Delta\upsilon_{err}$, the $T_{avg,sp}$ is calculated as shown in Eq. (11). The $T_{avg,sp}$ on the chip surface is obtained by taking a mean value of temperature across chip surface excluding bond wires. The temperature distribution is observed from IR camera and hence shadow and the surface underneath the wires are excluded to obtain an approximate $T_{avg,sp}$.

$$T_{avg,sp} = T_{ref} + T_{cor} + K(\upsilon_{ce,meas} - \upsilon_{ref}(T_{ref}) + \Delta\upsilon_{err}) \tag{11}$$

where T_{ref} is the reference temperature used for calibration (in this case $25°C$), υ_{ref} is the on-state voltage at T_{ref} and $T_{cor}/\Delta\upsilon err$ are corrections for the calibration approach. On-state voltage correction from homogeneous to inhomogeneous temperature distribution is also investigated using FEM simulations under required circumstances, deriving on-state voltage, and comparing to homogeneous case.

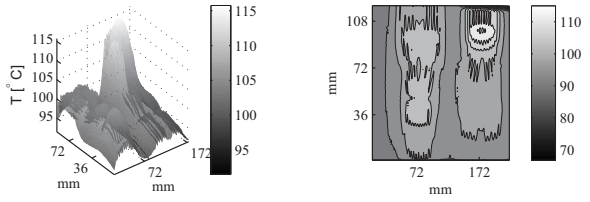
E. IR Thermography

Fig. 15a shows temperature field in the first section of DUT measured by IR thermography, when $D_{DUT,H}$ and $I_{DUT,L}$ are operating and at maximum temperature. Similarly, Fig. 16a temperature field when $D_{DUT,L}$ and $I_{DUT,H}$ are are operating and at maximum temperature. The spatial temperature variation along diagonal isother-



(a) Temperature field. (b) Contour.

Fig. 15. Temperature field and contour at $500A_{Peak}$ for one section when $D_{DUT,H}$ is hotter.



(a) Temperature field. (b) Contour.

Fig. 16. Temperature field and contour at $500A_{Peak}$ for one section when $D_{DUT,L}$ is hotter.

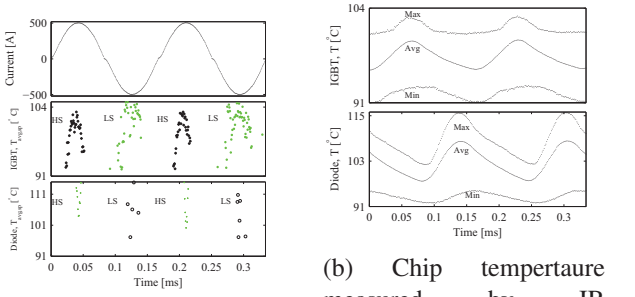
mic lines on $I_{DUT,H}$ are shown in Fig. 17 when the chip temperature is at maximum.

VI. Thermal dynamics

The primary power loss in switched semiconductor devices are around the active junctions. In a standard vertical trench based IGBT chip three PN-junctions are present, but only one is open or closed depending on gate voltage, namely region two situated close to the emitter side. While conduction loss occurs across the entire chip, the region around junction two experiences the highest power loss. Accordingly, this region is heated faster than the remaining part of the die and the metallization surface. Due to distance and thermal conductivity of aluminium, the die surface temperature is the quickest way to monitor temperature variation - apart from electronic parameters. This is reason for using IR thermography to monitor chip temperature. However, the downside of this approach is the necessity of black paint on top of the module, which significantly increase the thermal response time.

VII. Results

The estimated chip temperature using $\upsilon_{ce,on}$-load current method and IR measurement for two current cycles at $500A_{peak}$, $6\,Hz$ are shown in Fig. 18. Fig. 18a shows estimated temperature above $400\,A$ for IGBT and above $460\,A$ for diodes.Fig.19 shows enlarged view for estimated temperature close to peak current levels for IGBT. The SF varies from 0.4 to 0.22 between LS and HS IGBT and diode. Table I gives temperature measurement at different I_c when at peak for $6Hz$ output frequency and at corresponding tabulated baseplate temperature for $I_{DUT,H}$.



(a) Estimated $T_{avg,sp}$.

(b) Chip tempertaure measured by IR thermograpghy.

Fig. 18. Estimated and direct measured temperature at $500A_{peak}$ in a converter operation.

VIII. Discussion

This paper demonstrates chip temperature estimation using $\upsilon_{ce,on}$-load current method in converter operation.

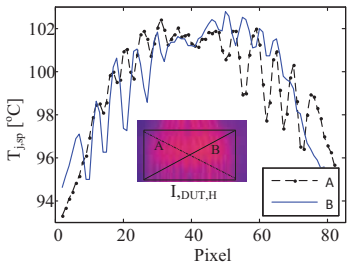


Fig. 17. Spatial variation of temperature diagonally along line A and B in $I_{DUT,H}$ when temperature is at peak.

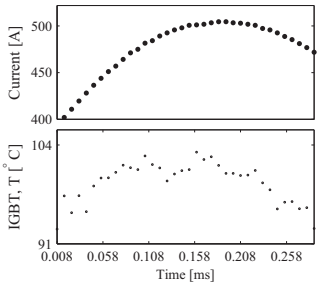


Fig. 19. Estimated $T_{avg,sp}$ from υ_{ce}-I_c method at $500A_{Peak}$ for $I_{DUT,H}$.

TABLE I. Temperature measurement from $\upsilon_{ce,on}$-load current and IR thermography (The peak temperature shown in table reaches nearly after 20ms of current peak)

Current	Proposed method	IR thermography on $I_{DUT,H}$			
$I_{c,peak}$	T_{est}	$T_{baseplate}$	T_{avg}	T_{max}	T_{min}
(A)	$(^{\circ}C)$	$(^{\circ}C)$	$(^{\circ}C)$	$(^{\circ}C)$	$(^{\circ}C)$
500	100	88	99.5	102.6	92.9
450	81	71	79.6	82	74.8
400	110	101.6	110.4	113.7	104.5

Some key challenges such as self-heating during calibration, contribution in voltage drop from series interconnection, deviation in total effective resistance during loading, and ageing and in interconnection are addressed to avoid an error in the estimation. Eq. (11) shows a final formulation including all correction and compensation parameters. The temperature sensitivity depends on the current magnitude and varies from 1-5 $mV/^{\circ}C$ for upto 1000 A in tested power module, hence it demands a very high accuracy in the measurement. Fig. 19 shows a fluctuation in temperature, because of 1-3 mV changes $\upsilon_{ce,on}$ as well as 1-2 A variations in the peak value of load current. The IR thermography in Fig. 15a shows spatial distribution of temperature field when the high side diode is at maximum temperature. The temperature reaches peak after nearly 20 ms delay than the current peak. This delayed thermal response could be due to heating of black paint which effect is unknown. Table I shows the estimated $T_{avg,sp}$ when the current is at peak. The estimated value is closer to the IR thermography at current peak, but the temperature keeps rising due to a slower time constant even after the current starts falling. As a result, the estimated value has errors increasingly more than $5^{\circ}C$ while current is rising and falling due to ohmic contribution in voltage drop. The SF may vary with the location and packaging of the chip. For a similar packaging and at the same location for the chip, this factor could be similar.

IX. Conclusion

This paper proposes a method to monitor chip temperature variation in faster response using υ_{ce}-load current method in converter operation. The method is also evaluated using direct measurement by IR thermography in similar working condition. The essential requirements for the proposed method are specified. Although, more statistical data need to be generated to do sensitivity analysis, the results and ease in integration into system makes the method suitable to be implemented in real time operation without any modifications in the converter. Because of higher sensitivity, this method demands very high accuracy 1 mV on the on-state voltage measurement to attain higher accuracy.

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