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INSTRUCTOR: DR. RAJ CHOWDHURY

Research Paper

BURN-IN, RELIABILITY TESTING, AND MANUFACTURING OF SEMICONDUCTORS

Prepared by:
Cagatay Bozturk

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Cagatay Bozturk

Abstract—In this paper I present the manufacturing stage of semiconductors and reliability of semiconductors. Failure Stage intervals were examined, regarding to graph of Failure Rate & Time. Effects of Burn-in Stress Test on semiconductors were inspected. Methodologies were examined for qualifications of semiconductors.

INTRODUCTION

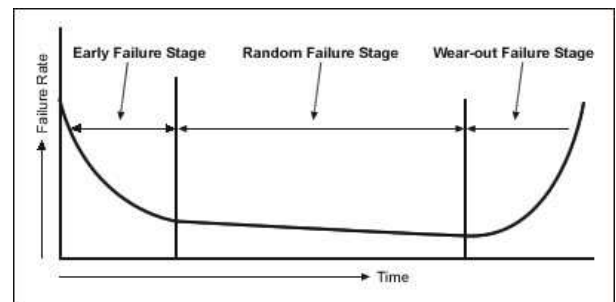
Burn-In is the application of thermal and electrical stress for the purposes of inducing the failure of "marginal (microelectronic) devices, those with inherent defects or defects resulting from manufacturing aberrations which cause time and stress dependant failures.

The manufacturing of semiconductor products consists of four distinct stages: wafer fabrication, wafer sort and test, packaging and assembly, and functional (electrical) tests. These four stages can be divided into two categories. Wafer fabrication and wafer sort and test are referred to as front-end manufacturing operations. Packaging, assembly, and functional testing are referred to as backend manufacturing operations.

RELIABILITY OF SEMICONDUCTORS

To evaluate the reliability of an electronic system, reliability information on the components used in that system is important. Failure rates are often used as an index for reliability. A failure rate

indicates how often a failure occurs per unit time, and failure-rate values generally change overtime as shown below



Early failure stage:

During this stage, failures occur at a high rate following the initial operation of semiconductor devices. They occur very soon and thus the failure rate declines rapidly over time. This is because the potential failures that could not be removed through a selective process are included and surface in a short time if a stress such as temperature or voltage is applied after use of the device is started. In the case of semiconductors, these failures are usually due to defects that could not be removed during production, such as micro dust collecting on the wafer, or to material defects.

Random failure stage:

When early failures are eliminated, the failure rate drops to an extremely low value. However, there is always the possibility of a potential failure accidentally occurring after a long time.

Consequently the failure rate never decreases to zero. It is almost constant because failures occur sporadically,

Wear-out failure stage:

During this stage, failures occur with increasing frequency over time and are caused by age-related wear and fatigue. In the case of a semiconductor device, electronic migration or oxide film destruction (TDDDB) may occur.

WHAT IS 'RELIABILITY & LIFE TESTING'?

The reliability of a semiconductor device is determined by its ability to perform its required functions under the stipulated conditions for a finite period of time. Quantifiable yardsticks such as the reliability rate, failure rate, and mean time to failure (MTTF) are used to measure reliability.

Customers naturally expect semiconductor devices to perform the required functions from the moment they are first used, and they also expect the devices to function without failure throughout the expected period of use.

The objective of reliability testing is to confirm a semiconductor device's fault-free operation and estimated useful life by exposing the device to accelerated or marginal stress, based on the amount of stress (thermal stress, mechanical stress, electrical stress etc) that the device is estimated to undergo during manufacture, shipping and normal use.

WHAT IS "QUALIFICATIONS"?

This methodology applies to the qualification of all semiconductor processes, packages and materials used by the manufacturer including:

- New processes, Packages, Products, Wafer Foundries, Assembly Subcontractors.
- Changes to Processes/Packages/Materials/Locations/Design Rules.

Successful completion of the qualification process is a precursor to a design receiving approval to be released for sale or for a manufacturing or assembly process to be approved. [¹]

SEMICONDUCTOR MANUFACTURING

Semiconductor manufacturing consists of the following steps:

- 1) production of silicon wafers from very pure silicon ingots;
- 2) fabrication of integrated circuits onto these wafers;
- 3) assembly of every integrated circuit on the wafer into a finished product; and
- 4) testing and back-end processing of the finished products.

Wafer Fabrication

Wafer fabrication generally refers to the process of building integrated circuits on silicon wafers. Prior to wafer fabrication, the raw silicon wafers to be used for this purpose are first produced from very pure silicon ingots, through either the Czochralski (CZ) or the Float Zone (FZ) method. The ingots are shaped then sliced into thin wafers through a process called wafering.

The semiconductor industry has already advanced tremendously that there now exist so many distinct wafer fab processes, allowing the device designer to

¹ <http://www.reltech.co.uk>

optimize his design by selecting the best fab process for his device. Nonetheless, all existing fab processes today simply consist of a series of steps to deposit special material layers on the wafers one at a time in precise amounts and patterns.

Assembly

The process of putting the integrated circuit inside a package to make it reliable and convenient to use is known as semiconductor package assembly, or simply 'assembly'. Over the years, the direction of assembly technology is to develop smaller, cheaper, more reliable, and more environment-friendly packages. Just like wafer fabrication technology, assembly technology has advanced tremendously that there are now a multitude of packages to choose from.

Despite glaring differences between the various packages available in the industry today, all packages share some things in common. To name a few, all of them: 1) provide the integrated circuit with a structure to operate in; 2) protect the integrated circuit from the environment; 3) connect the integrated circuit to the outside world; and 4) help optimize the operation of the device.

In general, an assembly process would consist of the following steps: 1) *die preparation*, which cuts the wafer into individual integrated circuits or dice; 2) *die attach*, which attaches the die to the support structure (e.g., the leadframe) of the package; 3) *bonding*, which connects the circuit to the electrical extremities of the package, thereby allowing the circuit to be connected to the outside world; and 4) *encapsulation* (usually by plastic molding), which provides 'body' to the package of the circuit for physical and chemical protection.

Subsequent steps that give the package its final form and appearance

(e.g., DTFS) vary from package to package. Steps like marking and lead finish give the product its own identity, improve reliability, and add an extra shine at that.

Test

Once assembled, the integrated circuit is ready to use. However, owing to the imperfection of this world, assembled devices don't always work. Many things can go wrong to make a device fail, e.g., the die has wafer fab-related defects, or the die cracked during assembly, or the bonds were poorly connected or not connected at all. Thus, prior to shipment to the customer, assembled devices must first be electrically tested.

Electrical testing of devices in big volumes must be done fast and inexpensively. Mass-production electrical testing therefore requires an automated system for doing the test. Equipment used to test devices are called, well, testers, and equipment used to handle the devices while undergoing testing are called, well, handlers. Tester/handler systems are also known as automatic test equipment (ATE).

Different products require different levels of sophistication in ATE requirements. Electrical testing of voltage reference circuits certainly don't require high-end ATE such as those used to test state-of-the-art microprocessors or digital signal processors. One area of electrical testing that continuously challenge engineers is building an ATE that can test the speed of new IC's that are much faster than what they can use in building their ATE's.

Software written for testing a device with an ATE is known as a test program. Test programs consist of a series of subroutines known as test blocks. Generally, each test block has a corresponding device parameter to test under specific conditions. This is

accomplished by subjecting the device under test (DUT) to specific excitation and measuring the response of the device. The measurement is then compared to the pass/fail limits set in the test program. After the device is tested, the handler bins it out either as a reject or as a good unit.

After a lot is tested, it is subjected to other back-end processes prior to shipment to the customer. Tape and reel is the process of packing surface mount devices in tapes with pockets while this tape is being wound around a reel. Boxing and labeling is the process of putting the reels or tubes in shipment boxes, and labeling these shipment boxes in accordance with customer requirements.

BURN-IN

Burn-in is an electrical stress test that employs voltage and temperature to accelerate the electrical failure of a device. Burn-in essentially simulates the operating life of the device, since the electrical excitation applied during burn-in may mirror the worst-case bias that the device will be subjected to in the course of its useable life. Depending on the burn-in duration used, the reliability information obtained may pertain to the device's early life or its wear-out. Burn-in may be used as a reliability monitor or as a production screen to weed out potential infant mortalities from the lot.

Burn-in is usually done at 125 deg C, with electrical excitation applied to the samples. The burn-in process is facilitated by using burn-in boards (see Fig. 1) where the samples are loaded. These burn-in boards are then inserted into the burn-in oven (see Fig. 2), which supplies the necessary voltages to the samples while maintaining the oven temperature at 125 deg C. The electrical bias applied may either be static or dynamic, depending on the failure mechanism being accelerated.

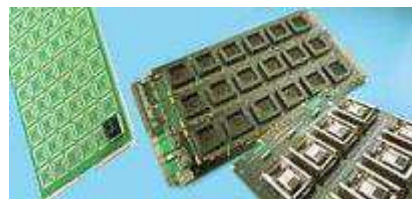


Figure 1. Photo of Bare and Socket-populated Burn-in Boards

The operating life cycle distribution of a population of devices may be modeled as a bath tub curve, if the failures are plotted on the y-axis against the operating life in the x-axis. The bath tub curve shows that the highest failure rates experienced by a population of devices occur during the early stage of the life cycle, or early life, and during the wear-out period of the life cycle. Between the early life and wear-out stages is a long period wherein the devices fail very sparingly.

Early life failure (ELF) monitor burn-in, as the name implies, is performed to screen out potential early life failures. It is conducted for a duration of 168 hours or less, and normally for only 48 hours. Electrical failures after ELF monitor burn-in are known as early life failures or infant mortality, which means that these units will fail prematurely if they were used in their normal operation.

High Temperature Operating Life (HTOL) Test is the opposite of ELF monitor burn-in, testing the reliability of the samples in their wear-out phase. HTOL is conducted for a duration of 1000 hours, with intermediate read points at 168 H and 500 H.

Although the electrical excitation applied to the samples are often defined in terms of voltages, failure mechanisms accelerated by current (such as electromigration) and electric fields (such

as dielectric rupture) are understandably accelerated by burn-in as well. [²]

CONCLUSION

Burn-in helps us to detect problem trends / determine critical components in a system failure(s), and, analyze the system for Effective reliability. Thanks to burn-in, we can predict reliability performance and Life-cycle of the products. It provides valid field “failure data” and timely corrected actions. Although it is difficult determine to optimum burn-in, optimum burn-in helps us to facilitate the reliability design.

REFERENCES

- [1]<http://www.reltech.co.uk/>
- [2]<http://www.semiconfareast.com>
- [3]TECH 65800 Burn-in/ Stress Test
Lecture Notes (Dr. A. Raj Chowdhury)

² <http://www.semiconfareast.com>