Switching and conducting performance of SiC-JFET and ESBT against MOSFET and IGBT

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***Abstract*—Here the switching and conducting performance of a SiC-JFET, an Emitter-Switching Bipolar Transistor (ESBT) and conventional power semiconductors as MOSFET and IGBT with Si- and SiC-diode is presented. The variety of power semiconductors is growing and there is a need to get rules to select them for the application given. The structure and special characteristics of the new devices are explained. The switching and conducting behavior of the devices is measured and investigated. The test circuit and the measurement method are presented. Based on the measured waveforms the power losses are calculated. The results of the switching and conducting performance of these power semiconductors are discussed.**

***Keywords*—SiC-device, JFET, IGBT, MOSFET, Bipolar device, Power semiconductor device, Device characterization, New switching devices.**

I. INTRODUCTION

Power converters as three phase inverters for feeding electrical machines or for application as uninterruptible power supplies are standard for general purpose in industry. In these applications, IGBTs and MOSFETs are the first choice because of their good switching and conducting behavior, their simple driving circuits and their price.

These power devices operate in most applications in the hard switching mode. The variety of power semiconductors is growing.

New devices are introduced into the market with new advantages and disadvantages [1-3]. The aim of the development of power semiconductors is low on-resistance, high operating temperature, high breakdown voltage, and fast switching abilities. These abilities allow higher switching frequencies and that results in a reduction of passive component size. This is very attractive for applications that demand high power density or high operating temperature. Interesting power semiconductors are silicon carbide (SiC) types as SiC junction field effect transistor and SiC-MOSFET.

The intention of this paper is an analysis of the switching and conducting performance of a Junction Field Effect Transistor (JFET) based on silicon carbide and an Emitter-Switching Bipolar Transistor (ESBT) with an IGBT and a 600 V MOSFET. For a fair comparison the IGBT and the MOSFET are tested with their internal Si-freewheeling diode and with an external SiC-diode. The analysis will be on the conducting and switching losses, since there is a trend towards increasing the switching frequency. IGBTs are on behalf of their switching power losses well suited for medium frequency applications [4]. They show the advantage of high blocking voltage. In contrast MOSFETs have lower switching losses but only limited blocking abilities and a poor freewheeling diode. ESBTs and SiC-JFETs seem to combine the advantages and avoid the disadvantages of IGBTs and MOSFETs.

In this paper, the static and switching characteristics of a SiC-JFET and ESBT with a bus voltage of 500 V are measured. The comparative low bus voltage is chosen since the breakdown voltage of the MOSFET is 600 V. Comparisons are carried out with state of the art IGBT and MOSFET. The main emphasis is put on the total losses of the switched device.

Section II describes the specific characteristics of the devices. In section III measurements are presented which show the conducting and switching behavior. After that in section IV the results will be compared and evaluated concerning the power losses and the complexity of their gate drivers. Section V includes the conclusion.

II. DEVICE CHARACTERISTICS AND STRUCTURE

A. ESBT characteristics

The Emitter-Switching Bipolar Transistor is a combination of a NPN bipolar transistor (BJT) and MOSFET. The BJT has an enhanced voltage blocking characteristic. The fast switching low voltage n-channel power MOSFET is realized inside the emitter of the BJT [5]. An equivalent circuit is shown in Fig. 2. In order to drive the BJT and MOSFET independently two separate terminals, gate and base, are required. Thus four terminals are necessary for the cascaded structure. The driving circuit presented in Fig. 1 allows connecting only the gate to the PWM-controller whereas the base is driven automatically by the circuit. The base current is proportional to the collector current. Thus a transformer can couple the collector and the base current [6]. The capacitor in the driving circuit takes the negative base current while the device is switched off. The stored energy of the capacitor provides the positive base current for the following turn-on [7]. Because the capacitor is shortened by the base the turn-on current starts with a peak for a fast opening of the collector-emitter path. The base current is provided by the transformer [6]. For the switch-off firstly the MOSFET is turned off and its drain current falls very fast down to zero. The collector current has to commutate to the base and flows through the capacitor to ground and the transistor starts blocking. With zero bias at the gate node and the zero BJT base current, the device behaves like a reverse biased PN diode in off state. All in all a high voltage device is obtained, with a breakdown voltage equal to the collector-base junction voltage from the BJT [1].

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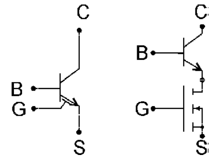

Fig. 2. ESBT symbol and equivalent circuit

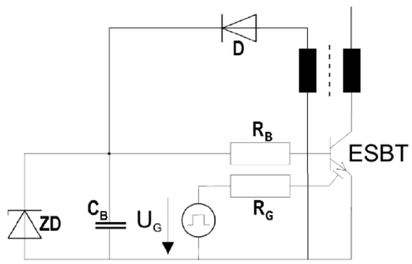

Fig. 1. ESBT driving circuit with transformer for the basis current

The speed of the turn-off switching is limited by the storage time of the devices. Thus, a suitable base current sink is required in order to speed up the turn-off process. So, in an ESBT device, the base charge is removed through a base current equal to the collector current [1]. A switching frequency above 100 kHz is published to be possible [7].

B. SiC-JFET Characteristics

Silicon carbide is a promising material for power semiconductors, since it has a large band gap of 3,26 eV that allows a high blocking voltage and a high junction temperature [8-11]. Besides that SiC has high electron mobility, so that switching frequencies above 100 kHz are published to be possible [12]. After SiC-Schottky-diodes are commercially available since 2001 the first switchable power devices based on SiC will come into the market in 2008. They will be designed as JFETs [3,13]. Characteristic for JFETs is that they are normally on, that means a negative voltage has to be provided to switch the device off. For this reason conventional gate drivers are not suitable. The advantages are that the theoretical operating temperature is above 350°C but momentarily limited by its maximum case temperature. Another advantage is that because of their low switching losses these devices can operate at high switching frequency [12-14]. The principle structure of a JFET is illustrated in Fig. 3. As long as there is no voltage at the gate contacts the n-channel between the p-doped gate zones is conducting. If a negative gate voltage is applied the depletion layer expends until the saturated voltage is reached and the n-channel is totally pinched off so that the JFET is blocking. In the conducting mode there is no pn-junction between drain and source so that the conducting losses are only caused by the $R_{DS,ON}$ of the channel. For power electronics a vertical structure with a buried gate seems to be the most promising structure because the high breakdown field can be fully used. The vertical JFET structure has an internal freewheeling pn-diode. Because of the wide band gap its forward voltage is with 3.5 V very high, so that an external SiC-Schottky-diode is recommended. In addition it is also possible to switch the JFET on while the diode is conducting, so that the conducting losses are just caused by the $R_{DS,ON}$ of the JFET.

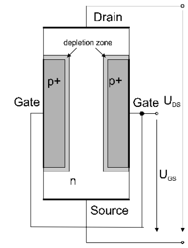

Fig. 3. sketched structure of a JFET

C. IGBT with Si- and SiC-Freewheeling Diode Charcteristics

Since IGBTs are very sensitive to backwards voltages, there is normally an external freewheeling diode placed next to the IGBT chip in the case [15]. For these investigations a non punch through IGBT in combination with an inverse parallel Schottky SiC-diode and a Si-diode to show the benefit of the SiC-diode are used separately. The advantage of the SiC-diode is that its reverse recovery charge is very small compared to Si-diode. That results in a very low reverse recovery current while the IGBT is turned on because there are only a few charge carriers in the diode that has to be removed.

D. MOSFET Characteristics

MOSFETs have an internal freewheeling diode because of their internal pn junctions. Characteristic for this diode is that it has a low forward voltage but a worse switching behavior. Because of the low forward voltage it is not possible to apply an external diode since it will always has a higher forward voltage and the current will flow through the MOS-diode. For a fair comparison the switching behavior is also investigated with a SiC-diode, even if that is not possible in most applications as DC to AC and AC to DC inverters. Also characteristic for the MOSFET is that the typical breakdown is limited to 600 V (however there are some exceptions with V_{BR} = 800 V but with an even worse diode).

III. Measurements of SiC-JFET, MOSFET, IGBT and ESBT

A. Tested Power Semiconductors and Conditions

In this section the measurement results of the semiconductors (B), a SiC-JFET, an ESBT, a CoolMOS and an IGBT with a freewheeling SiC-Schottky diode are presented. For the IGBT and the MOSFET the measurements have been carried out with their internal

TABLE I.
USED SEMICONDUCTORS (*WITH SIC-DIODE)

	Type	Breakdown -voltage (V)	Max Current @ 100 °C (A)
MOSFET	SPW47N60CFD [16]	600 V	27
IGBT	SKW25N120 [17]	1200 V	25
ESBT	STC08IE120HV [18]	1200 V	8
SiC-JFET*	sample SiCED [19]	1200 V	8
SiC-Diode*	C2D20120D [20]	1200 V	2x10

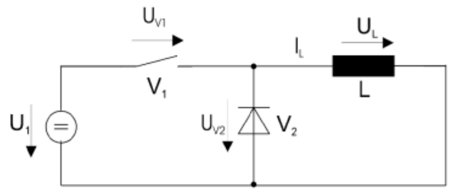

Fig. 4. buck converter as test circuit

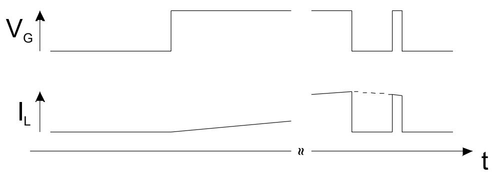

Fig. 5. Test signal (double pulse) for the test circuit: Gate-Signal from V_1 (upper) and the current through the inductor L (lower).

diode and an external SiC-diode, separately. The focus of the measurements is on switching and conducting behavior and their losses. All devices are tested at a bus voltage of 500 V and a current up to 10 A. For the ESBT, MOSFET and IGBT the recommended gate resistors are used. Since there is no datasheet for the JFET available a gate resistor of 20 Ω is applied. This resistor allows safe on- and off-switching without EMC disturbance.

All measurements are done with a very fast gate driver (rise and fall time < 30ns). The signals are measured with a Tektronix DPO4054 scope linked to Matlab for automatic storaging of the data, displaying the waveforms and calculting of the power losses.

B. *Test setup for the Switching Characteristics*

A buck converter shown in Fig. 4 is chosen as test setup there V_1 is the device under test and V_2 is the freewheeling diode.

For the investigation of the switching characteristics a double pulse gate signal is used (Fig. 5) [15,21]. By the length of the first conducting period of the device under test the current through it is adjusted because of the linear increase of the current through the inductance. Than the device under test (DUT) is switched off for the first time and the current commutates to the freewheeling diode until the DUT is switched on again. With this test setup the switching behavior can be investigated at defined voltage and current. Since the device is operating for very short period of time and only two switching cycles take place its self-heating can be neglected. For the measurements the devices are heated externally by a heating plate to 100°C for the experiments.

C. *Calculation of the power losses*

The power losses and the switching energy are calculated based on the measured waveforms by the following equations:

$$P_{SW} = u(t) \cdot i(t) \tag{1}$$

$$E_{ON}, E_{OFF} = \int_{t_{ON}, t_{OFF}} u(t) \cdot i(t) dt \tag{2}$$

The integration is realized by summing up all products of the discrete measuring points and multiplying them by the sample rate. The voltage drop across the stray inductance of the semiconductor L_σ (L_σ = 5...10 nH) is smaller than one percent because the measuring probe is directly connected to the pins of the device.

D. *Measurements*

i.) ESBT

The turn-off switching characteristic of the ESBT for different currents is shown in Fig. 6. When the gate signal of the MOSFET is low, the open emitter condition forces the collector current to flow through the base path of the BJT. Thus, the extraction of the charge stored in the base of the BJT is operated at current equal to collector current. So the storage time and by that the turn-off time varies extremely with the switched current (see TABLE II). The high delay time while turning off the ESBT might cause difficulties regarding driving and controlling of the converter.

The measured current includes the driver current from the base. In Fig. 7 the turn-on and turn-off waveforms with bus voltages of 500V from the ESBT are shown.

It is shown that the ESBT has a very small rise- and fall-time (70 ns, 20 ns) and the reverse recovery effect of the SiC-Diode is very low. The turn-on and turn-off losses of the ESBT are shown in Fig. 8 as function of load current.

ii.) SiC-JFET

Fig. 9 shows the turn-on and turn-off waveforms of the SiC-JFET. The bus voltage is 500V and the switching current is 8 A. For the turn on Fig. 9 shows that the rise time of the gate voltage is 30ns and of the drain current is 85 ns. Because of the SiC-freewheeling diode the reverse recovery current peak is very low. The drain-source-voltage falls within 80ns to zero after the current reaches the 8 A. The turn on losses are shown in the lower left figure and reach their maximum at the maximum of the reverse recovery current.

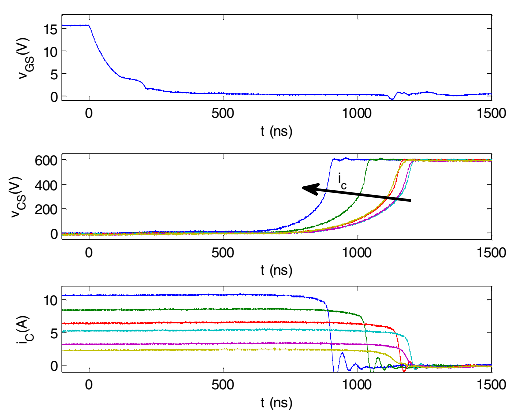

Fig. 6. turn-off switching time versus the current
@ V_{bus} = 600 V, R_G = 47 Ω, R_B = 0,33 Ω, $V_{GS,on}$ = 15 V
I_C = [2,2A; 3,1A; 5,2A; 6,3A; 8,4A; 10,7A]

TABLE II.
TURN OFF TIME FOR DIFFERENT CURRENTS (ESBT)

I (A)	T_{off} (ns)
5	1200
6	1170
8	1050
10	900

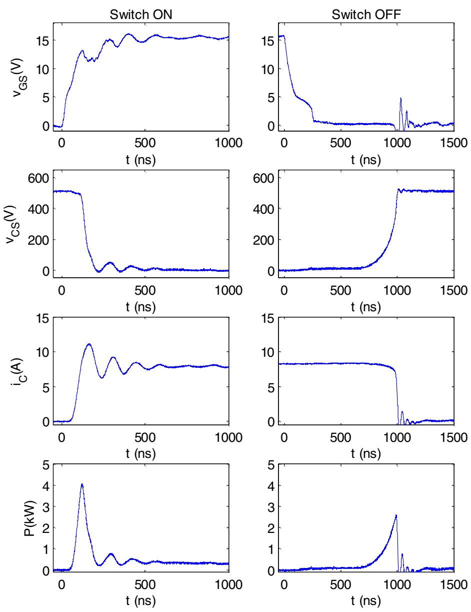

Fig. 7. Switching Waveforms of the ESBT with transformer for the basis current
@ V_{bus} = 500 V, I_C = 8 A, R_G = 47 Ω, R_B = 0,33 Ω, $V_{GS,on}$ = 15 V, T_J = 100°C

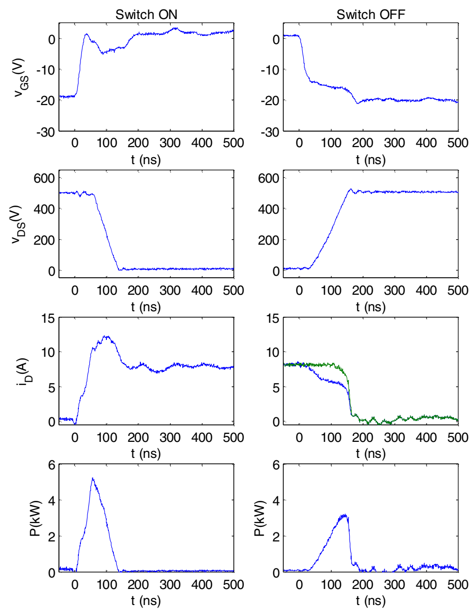

Fig. 9. Switching Waveforms of the SiC-JFET with SiC-Diode with measured (blue) and expected (green) waveform
@ V_{bus} = 500 V, R_G = 20 Ω, $V_{GS,off}$ = -19 V, I_D = 8 A, T_J = 100°C

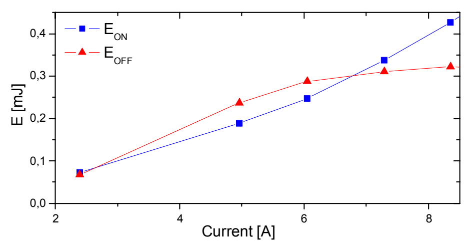

Fig. 8. Turn-on and turn-off loss versus current for the ESBT
@ V_{bus} = 500 V, $V_{GS,on}$ = 15 V, T_J = 100°C

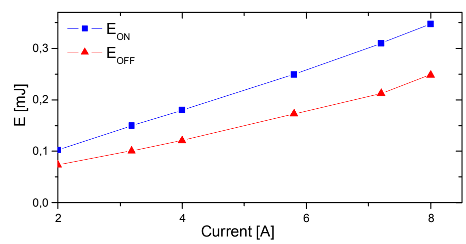

Fig. 10. Turn-on and turn-off loss versus current for the JFET
@ V_{bus} = 500V, $V_{GS,off}$ = -19 V, T_J = 100°C

The turn-off behavior is shown on the right side of Fig. 9. Here the gate source voltage drops initially to 75 % of its pinch-off voltage. However the drain-source-voltage begins to rise at the same time. Since the pinch-off voltage of the JFET is -19.0 V v_{DS} should not rise until the pinch-off voltage is reached. For that reason it can be assumed that this effect (v_{DS} rising before v_{GS} < -19 V) is caused by electromagnetic injection to the measuring probe and that the plateau at 15 V of v_{GS} does not exist in reality. The same effect appears at the drain current that starts slightly to fall at the beginning of the switching event. The green line shows the expected waveform that is also used for calculating the turn off losses. Nevertheless the rise time of the v_{DS} is with 134 ns longer than for the turn on. The turn-off losses are smaller than the one for the turn-on, due to the reverse recovery current of the diode at the transistor turn on.

In Fig. 10 the switching energy versus the current is displayed. It can be seen that the losses increase with the current and that the switching energy is higher for the turn on.

iii.) IGBT

The main limitation to the turn-off speed of an IGBT is the lifetime of the minority carriers in the base of the BJT. Since the base is not accessible, external drive circuitry cannot be used to improve the switching time. This charge stored in the base causes the characteristic “tail” in the current´s waveform of an IGBT. This tail current slightly increases the turn-off losses [4,22]. The switching characteristics are shown in Fig. 11 and the switching losses in Fig. 12.

iv.) MOSFET

The intrinsic diode of the MOSFET has a very high reverse recovery charge. This charge results from the minority carrier recombination at the turn-off of the diode. This reverse recovery current is added to the MOSFET current and results to a very high current spike at the switch on-time from the MOSFET. This is shown in Fig. 13. A peak reverse recovery current of 74 A at a load current of 10 A is measured and results in very high turn on losses. This current peak results in a voltage drop of v_{ds} across the stray inductance of the source.

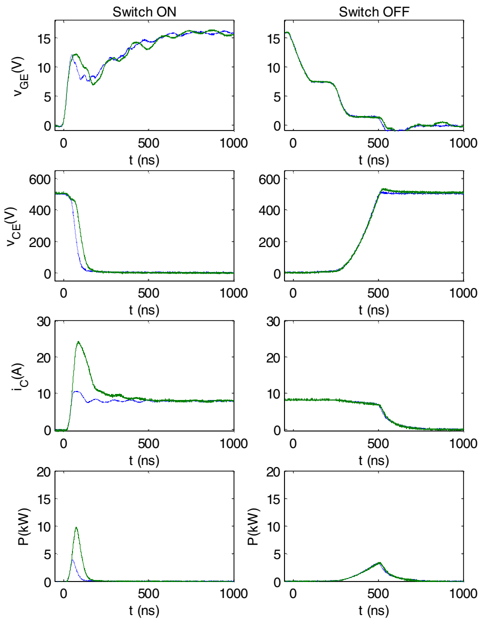

Fig. 11. Switching characteristic from the IGBT with internal Si-Diode (solid green line) and with SiC-Diode (dotted blue line) @ V_{bus} = 500 V, R_G = 22 Ω, $V_{GE,on}$ = 15 V, I_C = 8 A, T_J = 100°C

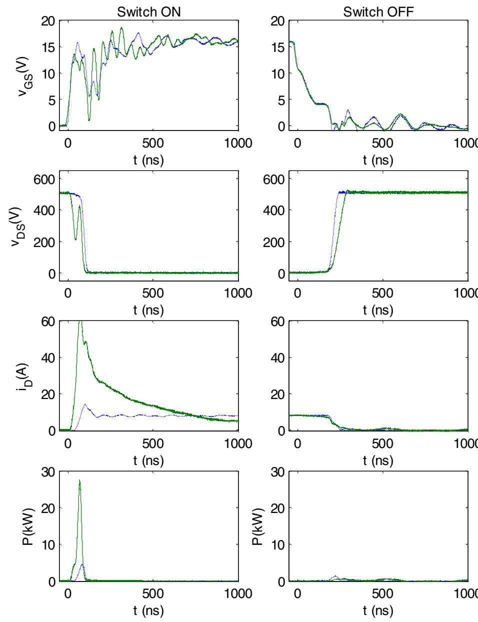

Fig. 13. Switching characteristic from the MOSFET with internal Si-Diode (solid green line) and with SiC-Diode (dotted blue line) @ V_{bus} = 500 V, R_G = 3,3 Ω, I_D = 8 A, $V_{GS,on}$ = 15 V, T_J = 100°C

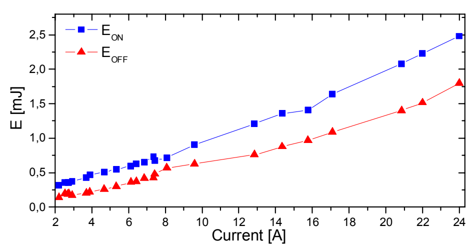

Fig. 12. Turn-on and turn-off loss versus current for the IGBT with Si-Diode
@ V_{bus} = 500 V, $V_{GE,on}$ = 15 V, T_J = 100°C

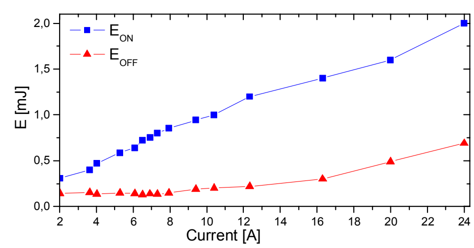

Fig. 14. Turn-on and turn-off loss versus current for the MOSFET with Si-Diode
@ V_{bus} = 500 V, $V_{GS,on}$ = 15 V, T_J = 100°C

The very low reverse recovery current of the SiC-Diode is also shown in Fig. 13.

During the turn-off of the MOSFET, the internal capacitances have to be recharged, so that there are no charge carrier influences in the channel area. Thereafter, the neutrality interference in this area will quickly be reduced and the drain current will drop rapidly. This results in very low turn-off losses.

E. *Test setup and Measurements for the Conducting Characteristics*

For the investigation of the conducting behavior the device under test (DUT) is in conducting state. To prevent self-heating of the device another switched semiconductor is connected in series and is switched on for a short pulse. The load is an adjustable resistor for limiting the current (Fig. 15). As before for the measurement of the switching behavior the DUT is external heated to T_J = 100 °C with a heating plate.

The voltage drop across the ESBT device is given by two contributions: the $V_{CE,SAT}$ of the BJT and the voltage drop across the low voltage MOSFET ($R_{DS,ON}$).

The ESBT has implemented a NPN BJT, that has a lower $V_{CE,SAT}$ in comparison to an PNP BJT that is included in the IGBT. So the saturation voltage of an IGBT is higher.

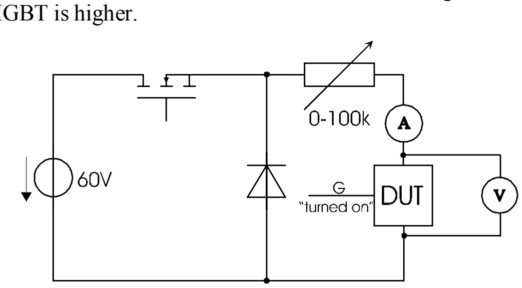

Fig. 15. Test circuit for the conducting behavior

The conducting losses of the JFET and MOSFET are caused by its $R_{DS,ON}$. The conducting losses of ESBT, JFET, MOSFET and IGBT are measured for different input currents in Fig. 16.

IV. Comparision of SiC-JFET, MOSFET, IGBT and ESBT

The semiconductors are compared with respect to their switching and conducting losses as well as the effort for their driving circuits.

A. *Conducting and switching losses*

For semiconductor power loss reduction the maximum current of the MOSFET and IGBT has to be derated to 24 A for a switching frequency of $f_{SW} = 50$ kHz. Otherwise the heat cannot be dissipating over the heat sink. Fig. 16 shows the conducting losses of the four devices. It can be seen that the conducting losses of the ESBT and JFET are well below to them of the IGBT and MOSFET.

Fig. 17 shows the switching losses of ESBT, JFET, MOSFET and IGBT. For the ESBT and the JFET it is assumed that three devices are connected in parallel for having the same current carrying ability as the MOSFET and the IGBT. For the MOSFET and the IGBT their internal diodes are used, while for the ESBT and JFET SiC-diodes are connected inverse parallel.

The turn-off and turn-on losses of the ESBT and SiC-JFET are both much smaller than those of the IGBT and MOSFET. Two factors are the main reason of the different switching losses. These are the high switching speed (rise and fall time) and the reduced reverse recovery current of the freewheeling diode.

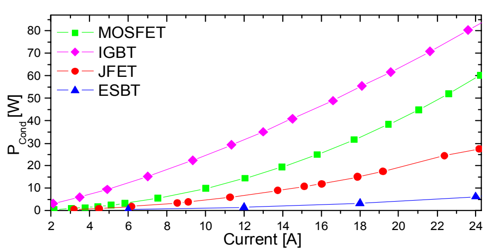

Fig. 16. Conducting losses versus current of ESBT, SiC-JFET, IGBT and MOSFET (For ESBT & JFET three chips in parallel) @ $V_{bus} = 500$ V, $T_J = 100$°C

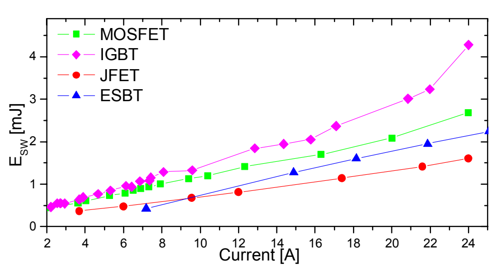

Fig. 17. Comparison of switching loss versus current between ESBT, SiC-JFET, IGBT and MOSFET (For ESBT & JFET three chips in parallel) @ $V_{bus} = 500$ V, $T_J = 100$°C

B. *Total losses in a switching application*

To compare the total losses a high switching frequency application with a switching frequency of $f_{SW} = 50$ kHz and a duty cycle of $D = 0.5$ is used.

The switching losses are calculated as

$$P_{SW,ON} = E_{ON} \cdot f_{SW} \tag{3}$$

$$P_{SW,OFF} = E_{OFF} \cdot f_{SW} \tag{4}$$

$$P_{Total} = P_{SW,ON} + P_{SW,OFF} + P_{Cond} \cdot D \tag{5}$$

Fig. 18 and Table III shows a total loss comparison at 24 A and 500 V.

C. *Driver efforts*

The drivers for the IGBT and MOSFET are comparable simple, since only a constant positive and additional for the IGBT a constant negative voltage has to be provided. However the ESBT demands for a complex circuit providing the base current and for the JFET a high negative voltage is necessary. In practical use the driving circuit for the JFET is even more complex because of the normally on behavior of the device and that each single JFET has a different pinch-off voltage that is close to the maximum negative gate voltage. However it is possible to use the JFET in a cascode circuit for driving it with a MOSFET driver [23]. Therefore the drain of a low voltage MOSFET is connected to the source of the JFET and the gate of JFET is linked to the source of the MOSFET. If the MOSFET is turned off, its drain to source voltages rises and the gate of the JFET gets a negative voltage so that the JFET starts blocking as well. The disadvantages of these circuits are that the conducting losses increase because of the two devices in series

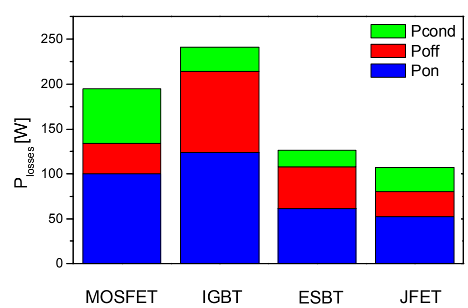

Fig. 18. Loss Comparison of ESBT, SiC-JFET, IGBT and MOSFET @ $V_{bus} = 500$ V, I = 24A $T_J = 100$°C, $f_T = 50$ kHz

TABLE III.
Switching power losses $V_{BUS} = 500$ V, I = 24 A, $F_T = 50$ kHz

	E_{ON} [µJ]	E_{OFF} [µJ]	P_{Cond} [W]	P_{SW} [W]
MOSFET	2000	689	60,2	134,45
IGBT	2480	1800	27	124
3xESBT + SiC-diode	1227	925	18,7	107,61
3xSiC-JFET + SiC-diode	1044	561	27,4	80,25

and that the operating temperature is limited to the maximum junction temperature of the MOSFET.

V. CONCLUSION

Four different power semiconductors (ESBT, SiC-JFET, MOSFET and IGBT, last one with SiC-diode and Si-diode) have been investigated concerning their switching and conducting behavior, their power losses and the efforts which have to be done to drive the device.

The measurements show that the new devices JFET and ESBT have a better performance than the well established ones as IGBT and MOSFET. The switching losses of the IGBT can be reduced by replacing the Si-diode by a SiC-freewheeling-diode which has a very low reverse recovery current. However the efforts for the drivers of the JFET and the ESBT are high. Because of the drivers and the SiC substrate of the JFET converters based on these devices are more expensive than converters with traditional power semiconductors. In applications where efficiency, cooling or operation at very low or high temperature is of importance the JFET and the ESBT may be an interesting alternative.

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