



Hybrid Circuit Breaker Test Bench

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Abstract

The target application of the Hybrid Circuit Breaker presented in this paper is a 6.6 kV/60 Hz network for an electric ship. This Hybrid Circuit Breaker is based on a series association of IGCTs (Integrated Gate Commutated Thyristors) and a fast mechanical switch. In this new topology, thanks to the IGCT turn off control, the fault current is strongly limited and the mechanical switch, turned off at zero current, provides the voltage sustaining. To validate the principle of this Hybrid Circuit Breaker, the authors propose a test bench that can provide a 50 Hz sinusoidal short circuit current with a 18 kA-peak value and a maximum di/dt of 20kA/ms. This test bench displays interesting results and validates many key points of the new topology.

Introduction

A relevant feature about ships with electric propulsion is that they rely on several energy sources so as to supply both the ship electric network and the propulsion motors. The rated power levels of the 6.6 kV propulsion network keep on increasing and can reach up to 100 MW. That implies an increase in the maximum short-circuit current limits, exceeding the breaking capabilities of current circuit breakers (around 50 kA). Moreover, the electric constraints caused by a default on distribution equipments (buses, cables, transformers...) are difficult to withstand with standard equipments.

The recent advances regarding power electronic devices enable the fast interruption of a current default with a limiting effect. As a consequence the DGA launched a study to evaluate the advantages of limiting the short circuit currents on ship electric components. This study includes itself within a research program called "All Electric Ship".

The target application for the study is a 6.6 kV/60Hz propulsion network. The circuit breaker is used to protect a 6.6 kV/440 V transformer. The power flow in this branch range itself from 1.5MW to 5MW.

The study carried out by TECHNICATOME and CAPSIM was divided in two parts:

- A first part of concept definition was accomplished with the EPFL to define a new topology of hybrid circuit breakers (Fig. 2) using controlled turn-off semiconductors [1, 2]. This study leads to patent TECHNICATOME n  03 293 050.5.
- A second part was carried out in collaboration with the LEEI research laboratory and consisted in a test bench realisation so as to validate the hybrid circuit breaker principle. This second part is detailed in the paper.

The basic principle of the hybrid circuit breaker is presented by Fig. 2. This structure uses thyristors in the "Current Interrupting" block and IGCTs (Integrated Gate Commutated Thyristors) as controlled turn-off devices in the "Current Transferring Block" [3], [4, 5]. When a surge current is detected, the current in the main branch is bypassed in the resonant circuit by turning off the IGCTs. The impedance of the resonant circuit limits the fault cur-

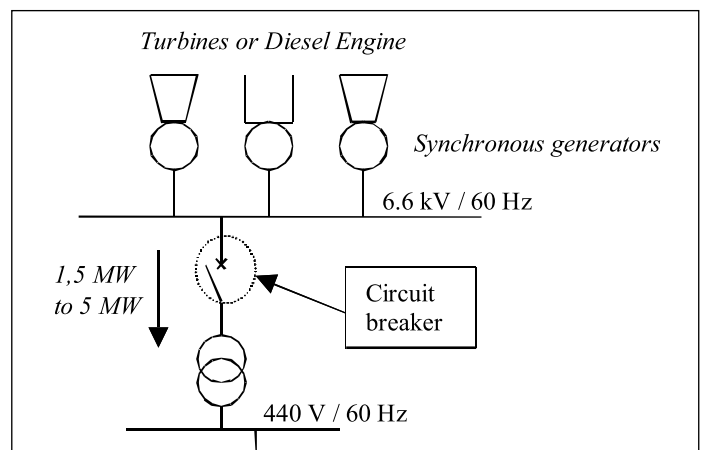


Fig. 1: Application network topology

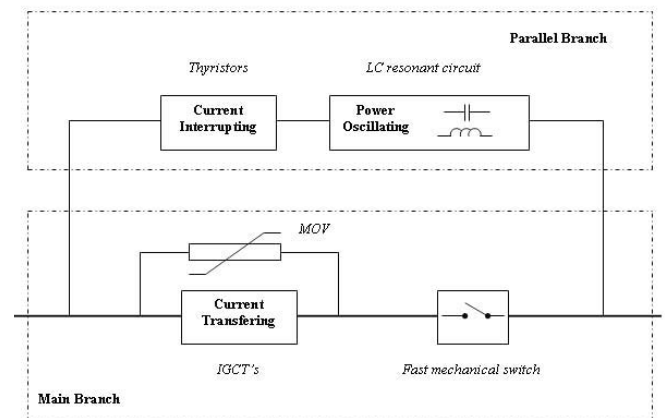


Fig. 2: Basic principle of the hybrid circuit breaker

rent which is rapidly interrupted at zero current crossing when thyristors spontaneously turn off. The mechanical switch is opened with no current during the oscillation of the parallel branch and provides the voltage sustained by the main branch, which avoids a serial association of IGCTs.

Test bench feature

The main characteristics of the test bench are:

- single phase circuit operating only for positive short circuit current;
- input voltage level : 1.5 kV;
- full scale short circuit current level and di/dt (18 kA, 20 kA/ms);
- short circuit current limited to 2.2 kA;
- short circuit current obtained with a capacitor discharging in an inductor;
- fast mechanical contact replaced by a semiconductor device.

The aim of the test bench is to validate some key points of the hybrid circuit breaker:

- fast short circuit current detection;
- current bypassing managed by MOV saturation at IGCT turn-off;
- mechanical contact switching off with zero current;
- current limitation by the impedance of the parallel branch.

The test bench source is composed by a discharge circuit L_s and C_s that can provide a 50 Hz sinusoidal short circuit current with a 18 kA-peak value and a maximum 20 kA/ms di/dt for an initial capacitor voltage that equals $V_{DC} = 1.5$ kV.

The main branch of the circuit breaker is composed of two reverse conducting IGCTs and one fast recovery diode. IGCT_2 replaces the fast mechanical contact normally used in the full scale model. D1 is a fast recovery diode which avoids the reverse conduction of the main branch. IGCT_3 is used to short circuit the resistive load. IGCT_1 is turned off to open the circuit when the short circuit current threshold is reached. A MOV nonlinear resistance associated in parallel limits the IGCT_1 turn off voltage to V_{MOV} .

The parallel branch is composed of a thyristor Th and a resonant circuit $L_0 C_0$. When IGCT_1 is turned off, the thyristor is simultaneously turned on. The voltage across the resonant circuit $L_0 C_0$ is imposed by the MOV, current i_2 reaches up to i_s and current i_1 decreases to zero. At the end of this sequence ($t = t_1$) the current is bypassed in the parallel branch. As it is shown by Fig. 2, the oscillation of the resonant circuit ($L_s + L_0, C_0$) allows the spontaneous turn-off of the thyristor at zero current crossing, which ends the breaking sequence ($t = t_1 + t_2$). The mechanical switch must be open before the voltage across IGCT_1 reaches again the MOV conducting threshold.

A snubber circuit (r, c) is associated in parallel with the thyristor in order to limit the overvoltage at turn-off. The resistor R_d allows discharging the capacitor C_0 .

Test bench design

C_s and L_s are calculated to get a 50 Hz sinusoidal short circuit current with a peak value of 18 kA and a maximum di/dt of 20 kA/ms for an initial capacitor voltage $V_{DC} = 1.5$ kV. The value of L_0 fixes the di/dt in the resonant circuit when IGCT_1 is turned off and thyristor Th is turned on: $dI_2/dt \approx V_{MOV}/L_0$. Thus, L_0 is chosen with respect to the turn on di/dt sustained by the thyristor.

As it is shown by Fig. 4, when current is bypassed in the parallel branch, the oscillation pulsation ω_0 and the maximum short circuit current I_{SCMax} depend on the capacitor value C_0 .

The test bench design was validated using the PSIM simulation software. Specific models for MOV and thyristor Th were implemented as described below.

The choice of the MOV (Metal Oxyde Varistance) must be done carefully. This component is often used as an overvoltage protec-

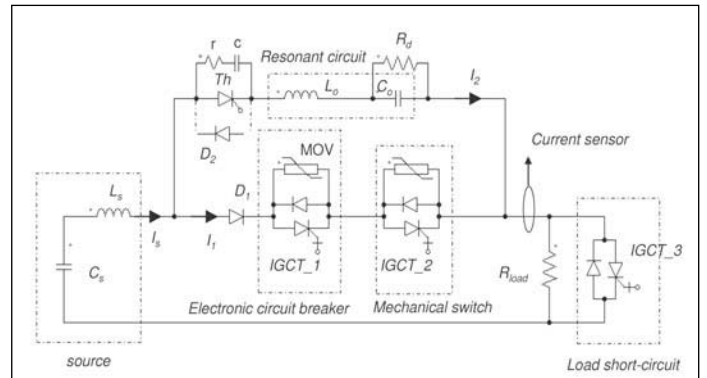


Fig. 3: Test bench circuit

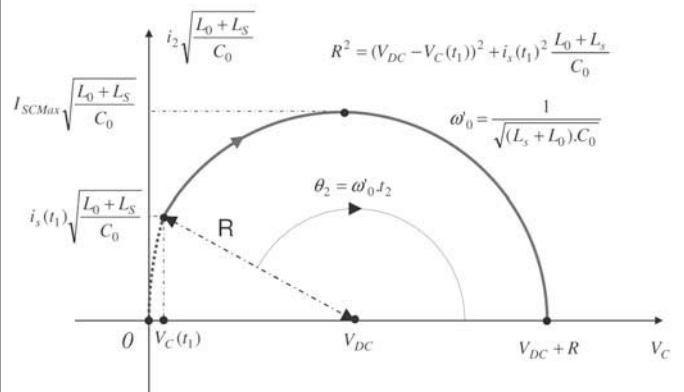


Fig. 4: state plane for resonant circuit ($L_s + L_0$) and C_0 (damping neglected)

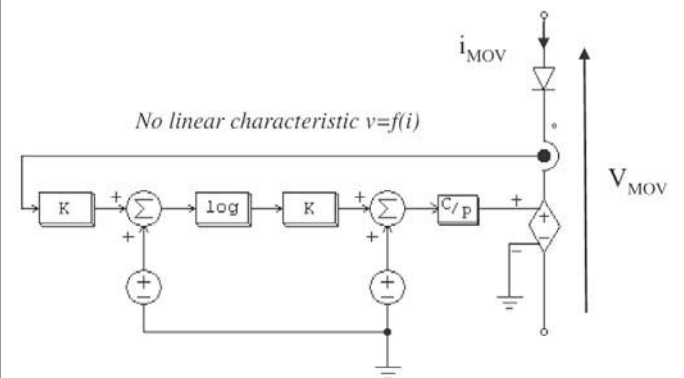


Fig. 5: PSIM model of Metal Oxyde Varistance

tion but in our case, the saturation voltage is also used to bypass the current in the resonant circuit. The value of this voltage will thus determine the deflection time t_1 , and that is why it is necessary to foresee exactly the saturation voltage when IGCT_1 is turned off. The PSIM model, shown in Fig. 5, takes into account the nonlinear characteristic of the MOV given in the manufacturer's data sheet.

Simulation results presented in Fig. 6, show that the saturation voltage and the threshold voltage are different when the MOV is conducting high current. This point will be verified further by experimental results.

To determine the values of the r and c elements (thyristor snubber), the thyristor recovery current must be taken into account. In PSIM software, the semiconductors are considered only as binary resistors and it was necessary to develop a model to analyse the

recovery current influence on the blocking overvoltage. This model includes an ideal thyristor model and a controlled current source which supplies the recovery current. The recovery time is fixed by the RL circuit in series with the ideal thyristor.

As it is shown in Fig. 8, the simulation results exemplify a thyristor turn off voltage close to -3 kV.

Fig. 9 shows the simulation results obtained with PSIM software. The final value of the voltage across capacitor C_0 is 3 kV and the maximum value of the limited short-circuit current is 2.2 kA. These values are closed to the theoretical values calculated with a neglected damping. After IGCT_1 turn off, the mechanical switch must be opened before the voltage across the resonant circuit reaches again the MOV threshold. According to these simulation results, the maximum delay for switch opening at zero current is equal to 230 μ s.

Test bench description

All the semiconductors and the MOVs are assembled with mechanical clamps. Considering the current levels, the clamps and the L/C blocks are connected by bus bars. A complete design of the test bench was realised with a 3D design software before the final mounting.

Experimental results

In this part, the main experimental results are presented, first in case of diode D2 disconnection (instantaneous breaking mode) and then with D2 connection (delayed breaking mode).

Instantaneous breaking mode

At the beginning of the sequence, capacitor C_s is charged at 1500 V, IGCT_1 and IGCT_2 are turned on to supply the resistive load R_{load} . When current i_s reaches 180A, IGCT_3 short circuits the load, hence current i_s rises with a di/dt of 20 kA/ms. Short circuit current threshold for i_s is fixed at 1.6 kA.

Current in IGCT_1 and Th are presented by Fig. 11a: current i_1 rises until 1.6 kA and then IGCT_1 is turned off. In the deflection parallel branch the current rises strongly and the oscillation begins with pulsation ω_0 . (See previous section). As expected in the simulations, the short circuit current is limited at 2.2 kA, which is 8 times lower than the possible short circuit current of 18 kA. After short circuit detection, the circuit opens after 400 μ s. At the end of the sequence the energy stored in capacitor C_0 is dissipated in resistor R_d .

Fig. 11b demonstrates the zero current opening for the mechanical switch simulated by IGCT_2. IGCT_2 is turned off 210 μ s after short-circuit detection. Current i_1 in the main branch is equal to zero and the voltage across IGCT_2 increases without any overvoltage.

Fig. 12 shows a zoom of the deflecting sequence at IGCT_1 turn off. In this case, a special attention must be paid to the thyristor turn-on and its gate control: when the short circuit is detected, thyristor turns on order is given 10 μ s before IGCT_1 turn off order. Thanks to the MOV voltage, current i_2 increases and current i_1 in the main branch decreases to zero. These waveforms validate perfectly the simulation results presented in section 3, excepted for the high frequency oscillations of V_{MOV} which are due to the semiconductor off-state capacitance and inductor L_0 .

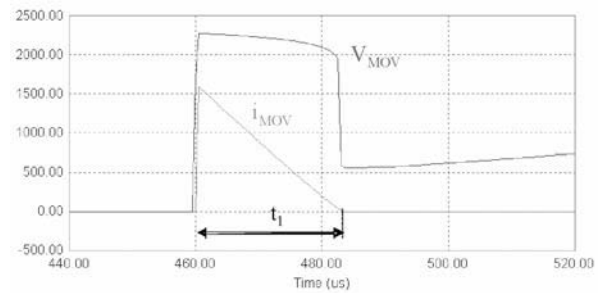


Fig. 6: MOV saturation voltage at IGCT_1 turn off

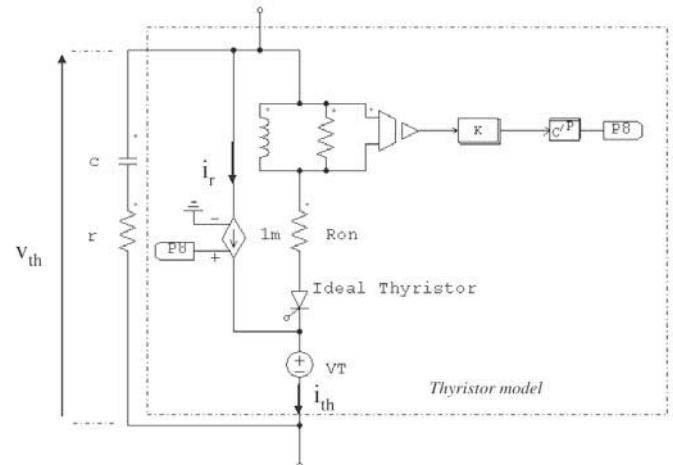


Fig. 7: Thyristor PSIM model

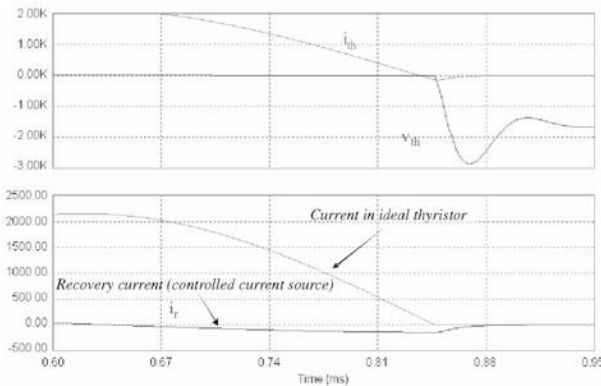


Fig. 8: PSIM simulation results for thyristor turn off

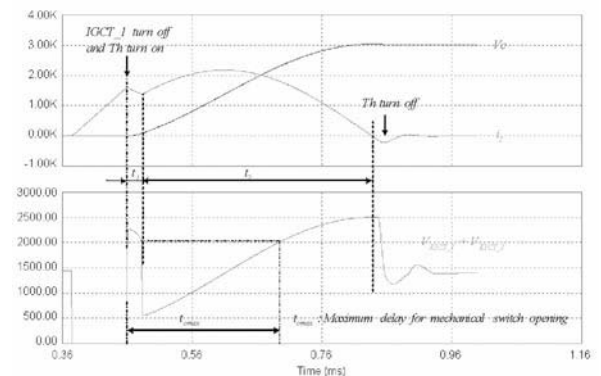


Fig.9: Hybrid circuit breaker operation. Simulation Results

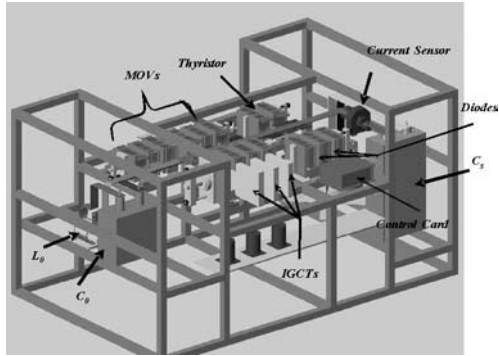
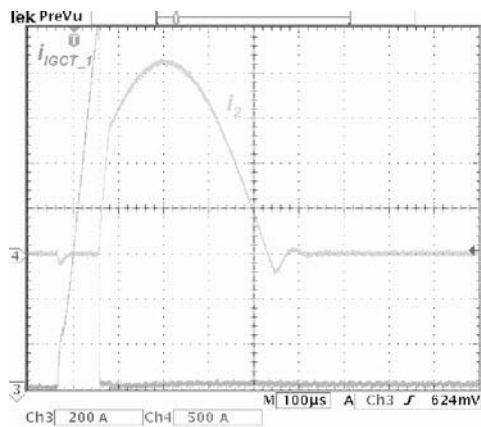
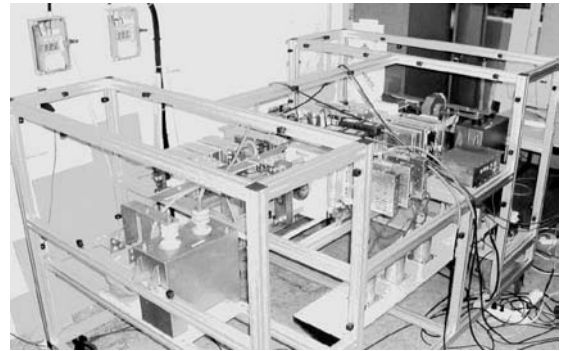
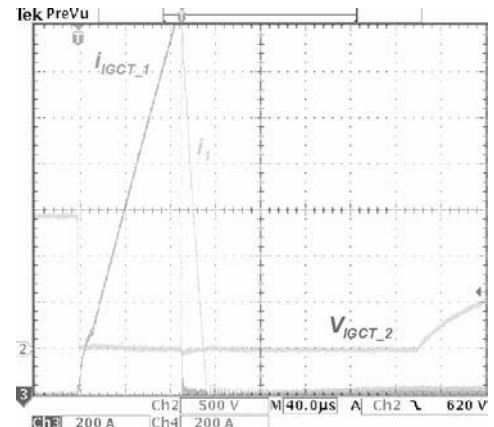


Fig. 10: Test Bench



(a):currents in IGCT_1 and Th



(b) IGCT_2 Zero current turn off

Fig. 11: Short-circuit breaking test

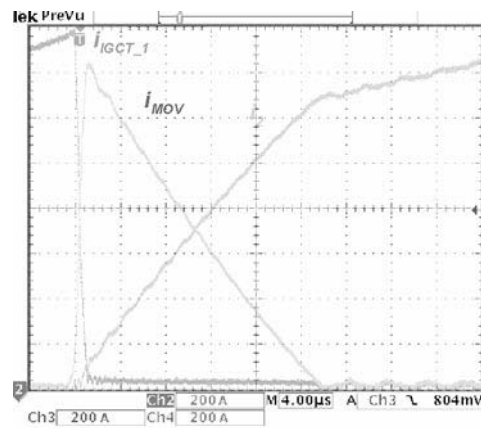


Fig. 12: Deflecting sequence at IGCT_1 turn off

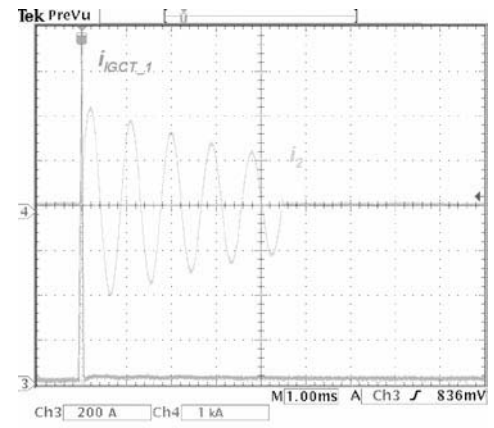


Fig. 13: Delayed breaking mode

Delayed breaking mode

During this test, diode D2 is connected in the parallel branch. Then, the thyristor turn-off can be delayed and the oscillations of the resonant circuit happen. This operating mode could be used to provide selectivity of the protection on a power network.

Conclusion

This test bench displayed interesting results and validated many key points of the new topology of hybrid circuit breaker such as:

- current deflection using MOV saturation voltage;
- the ability to limit the short circuit current;
- opening of the mechanical contact with no electric arc;
- two different utilisations: the instant breaking sequence or the delayed sequence, which allows slowing down the circuit breaker to let other protections open in a electric network configuration.

Nevertheless, in the future, the development of such circuit breakers is provided by the tuning of fast mechanical switches.

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Glossary

IGCT: Integrated Gate Commutated Thyristor.
 DGA: Délégation Générale pour l'Armement – French defense procurement agency.
 LEEI: Laboratoire d'Electrotechnique et d'Electronique Industrielle (Toulouse – France)
 EPFL: Ecole Polytechnique Fédérale de Lausanne (Suisse)

The authors



Guillaume Bats was born in France in 1982. He received the Electrical Engineering Degree from ENSEEIHT, France, in 2004. He works in CAPSIM, company specialized in the analysis of multi-domain power systems and electrical network. His fields of competence concerns power electronic, flux calculation and network study.



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Marc Francis. Merchant Marine Officer, graduated from SUPELEC (Ecole Supérieure d'Electricité), he is working since 2003 at AREVA TA as an electrical systems engineer.