# Optimization of the Specific On-Resistance of the COOLMOS<sup>TM</sup>

Xing-Bi Chen, Senior Member, IEEE and Johnny K. O. Sin, Senior Member, IEEE

Abstract—The optimized values for the physical and geometrical parameters of the p- and n-regions used in the voltage-sustaining layer of the COOLMOSTM1 are presented. Design of the parameters is aimed to produce the lowest specific on-resistance,  $R_{\rm on}$ , for a given breakdown voltage,  $V_B$ . A new relationship between the  $R_{\rm on}$  and  $V_B$  for the COOLMOSTM is developed as  $R_{\rm on} = C \cdot V_B^{1.32}$ , where the constant C is dependent on the cell dimension and pattern geometry. It is also found that by putting a thin layer of insulator between the p-region and its neighboring n-regions, the value of  $R_{\rm on}$  can be further reduced. The possibility of incorporating the insulating layer may open up opportunities for practical implementation of the COOLMOSTM for volume production.

Index Terms—Charge compensation, COOLMOS, on-resistance, power transistor, VDMOS.

### I. INTRODUCTION

NOVEL voltage sustaining structure using the principle of charge compensation to break the silicon limit of power MOSFETs has been proposed [1], [2], [3] and called a composite buffer (CB) structure [2]. The conceptual structure was experimentally realized later on, and it was called the COOLMOS<sup>TM</sup> [4]. More theoretical analysis on the structure was reported, and the structure was also called the super junction MOSFET [5], or the super multi-resurf MOSFET [6]. The COOLMOS<sup>TM</sup> breaks the traditional limit of the specific on-resistance  $R_{\rm on}$ , and reduces the  $R_{\rm on}$  by a factor of 5. Since the dimensions of the repetitive p- and n-regions used in the CB-structure can take up different dimensions and geometrical shapes [2], it is important to predict the theoretical limit of the  $R_{\rm on}$  versus breakdown voltage  $V_B$  for the different designs.

As proposed previously [2], the repetitive p- and n-regions can have different patterns for optimizing the on-resistance. In this paper, the  $R_{\rm on}$  of four patterns (interdigitated, hexagonal, square, and lattice) will be studied. Comparisons will be made among the various designs for the smallest on-resistance. Furthermore, it will be shown that a thin layer of insulator can be put between the p-region and its neighboring n-regions to further

Manuscript received September 20, 1999; revised April 14, 2000. This work was supported by the NSFC Grant 69 836 010 and 69 776 041, and the UGC Research Infrastructure Grant, Hong Kong SAR Government, RI95/96.EG24. The review of this paper was arranged by Editor M. A. Shibib.

X.-B. Chen is with the Dept. of Electronic Engineering, University of Electronic Science and Technology of China, Sichuan, 610054 (e-mail: xbchen@uestc.edu.cn).

J. K. O. Sin is with the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology, Clear Water Bay, Hong Kong.

Publisher Item Identifier S 0018-9383(01)00778-X.

<sup>1</sup>TMCOOLMOS is a trademark name from Siemens, AG, Germany.

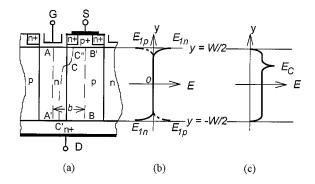


Fig. 1. Schematic cross-sectional view of an RMOST using the CB-structure concept, and the corresponding field profiles: (a) The structure; (b) field profiles of  $E_1$  along AA' (solid-curve) and along BB' (dashed curve); (c) field profile along a field line passing through point C.

reduce the on-resistance. Incorporation of the insulating layer may open up opportunities for practical implementation of the COOLMOS structure for volume production.

## II. On-RESISTANCE FOR DIFFERENT DESIGNS

Although a relationship between  $R_{\rm on}$  and  $V_B$  for the COOLMOS<sup>TM</sup> structure has been reported previously [2], the analytical analysis for the interleaf structure was published only recently, and very good agreement between the analytical result and the simulation result was obtained [7]. There have also been some theories on  $R_{\rm on}$  derived earlier [5], [8], [9]. All the results showed that  $R_{\rm on}$  is proportional to  $V_B$ . The theories of  $V_B$  in these analyzes are based on a critical field  $E_{\rm crit}$  which was treated as doping density dependent only [8] or simply as a constant of  $2 \times 10^5$  V/cm [5]. Since the breakdown voltage should be determined by the condition of the ionization integral along a field line equal to one, a constant of  $E_{crit}$  is only applicable in the ideal one-dimensional (1-D) case. In this paper, the breakdown voltage is evaluated using the ionization integral along the critical field line [7], and the relationship between the on-resistance and the breakdown voltage is in turn determined.

Fig. 1(a) shows the schematic cross section of a RMOST (recess MOSFET). It is designed using a CB-structure with a voltage sustaining layer thickness of W. The four patterns (interdigitated, hexagonal, square, and lattice) for the arrangement of the n- and p-regions of the structure studied are shown in Fig. 2. The sizes of the cell pitch for the patterns are denoted as b or fractions of b according to the pattern used. Actually, the size of a cell pitch can be arbitrary. For instance, if one requires each cell to be a basic unit having the smallest area with the same physical boundary conditions, there will be 1, 12, 8, and 8

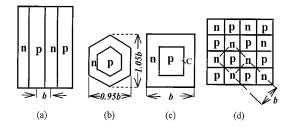


Fig. 2. Different design patterns of the CB-structure. (a) Interdigitated layout. (b) Hexagonal layout. (c) Square layout. (d) Lattice layout.

cell pitches for the patterns in Fig. 2(a)–(c) and (d), respectively. For Fig. 2(b)–(d), a cell pitch consists of a p-region and its surrounding n-region, where the n-region is continuous. Using this arrangement, it is convenient to evaluate the current flow based on a unit width of the active channel at the top of the p-regions.

When a reverse voltage close to  $V_B$  is applied across the top  ${\bf p^+}$ -region and the bottom  ${\bf n^+}$  region, the electric field E can be expressed by two components. One of them is

$$E_0 = V_B/W \tag{1}$$

which is the electric field of a  $p^+$ -i-n $^+$  diode under a reverse voltage of  $V_B$  (i.e., no space charge between the top  $p^+$ - and the bottom  $n^+$ -region). The other electric field component is  $E_1$ , which is due to the charges in the voltage sustaining structure when it is fully depleted, and the potentials at the top and the bottom of the structure are equal. The difference between the potential underneath the gate oxide and the potential at the source-body ( $p^+$ -region) in Fig. 1(a) has been neglected.

The CB-structure concept, by its principle of charge compensation, requires the amount of net doping in any cross-section to be zero. Assuming that the ratio of the area of an n-region in a unit cell to the total area of the unit cell is a, then

$$N_D a = N_A (1 - a) \tag{2}$$

where  $N_D$  is the donor concentration of the n-region, and  $N_A$  is the acceptor concentration of the p-region. Due to the charge compensation principle, the vertical component  $E_{1y}$  of  $E_1$  is almost zero except at a place near the top  $p^+$ -region or the bottom  $n^+$ -region. The field profile of  $E_{1y}$  along the middle lines of the n-region [AA' in Fig. 1(a)] and p-region (BB' in Fig. 1(a)) are schematically shown in Fig. 1(b).

It has been proven that the peak field at A, A', B, and B' in Fig. 1(a) is independent of W as long as W is larger than two times the size of b in a unit cell [10]. This brings out the important advantage of the CB-structure in comparison with the conventional voltage-sustaining layer which has a uniform doping concentration  $N_D$ . In the latter case, the peak field  $E_{1n}$  due to the charge in the layer is proportional to W,  $E_{1n} = qN_DW/2\varepsilon_s$ . Since  $E_0$  must be at least equal to  $E_{1n}$  to make the voltage sustaining layer to be fully depleted, the maximum field is larger or equal to  $2E_{1n} = qN_DW/\varepsilon_s$ . As the value of the maximum field is limited by impact ionization, when a higher breakdown voltage is needed, W has to be larger and  $N_D$  has to be smaller. So that in the latter case,  $R_{\rm on}$  increases drastically with increasing  $V_B$ .

It has also been proven that when W is larger than 2b, the peak value of  $E_1$  is at points A (the top center of the n-region) and B (the bottom center of the p-region) in Fig. 1(a) [10], and can be expressed as

$$E_{1n} = c_n q N_D b / \varepsilon_S \quad (at A) \tag{3a}$$

$$E_{1p} = c_p q N_A b / \varepsilon_S$$
 (at B) (3b)

where the constants  $c_n$  and  $c_p$  are determined by the values of a [10]. Note that in the previously reported analysis [8], a factor of 1/2 instead of  $c_n$  or  $c_p$  is used. However, this assumption of using the factor 1/2 to be the field at point A or B has no physical reason. Actually, close to point A, only those field lines generated from the donors located near the n-region side are terminated by the acceptors in the neighboring p-regions. The field lines generated by the donors close to point A are terminated by the top  $p^+$ -region or the gate. Therefore, the field there is very small and not equal to 1/2.

In order to make both the n-region and p-region to be fully depleted under a reverse voltage  $V_B, E_0$  should be equal to  $E_{1n}$  if the value of  $N_D$  is chosen so large as to make  $R_{\rm on}$  small, and hence  $E_{1n}$  is larger than  $E_{1p}$ . A further reduction of  $R_{\rm on}$  can be made by increasing the ratio a. This can be achieved by increasing  $N_A$ , which makes  $E_{1p}$  to increase. It turns out that the best design for the CB-structure is [10]

$$E_0 = E_{1n} = E_{1p}. (4)$$

In other words

$$c_n/a = c_p/(1-a).$$
 (5)

The values for  $a,c_n$  and  $c_p$  which satisfy the above condition are listed in Table I.

The value of  $E_0$  for a given breakdown voltage  $V_B$  is determined by the integral of the impact ionization rate  $\alpha_i$  along any field lines:  $\int \alpha_i \, ds = 1$ , where s is the distance along the field line from the starting point. In order to obtain an analytical expression for  $E_0$ , Fulop's approximation of  $\alpha_i$  is used:  $\alpha_i = 1.8 \times 10^{-35} E^7$  [11].

Since  $E_1$  along the field line BB' in Fig. 1(a) can be approximated by  $E_1 \exp(-\beta s)$ , where s is the distance from point B and  $\beta$  is a constant and determined by the slope of  $E_1$  at point B. Using  $E=E_0+E_1$  and  $E_{1p}=E_0$ , one obtains

$$E(s) = E_0 + E_0 \exp(-\beta s) \tag{6}$$

where the last term represents  $E_1$ , and  $\beta = -dE_1/(E_0\,ds)$  at B (where s=0). According to the Poisson's equation, one has  $\partial E_x/\partial x + \partial E_y/\partial y = -qN_A/\varepsilon_S$ . Since  $\partial E_x/\partial_x = 0$  due to the fact that B is a symmetrical point in the x-coordinate and  $\partial E_y/\partial y = dE/ds$ , it follows that  $dE/ds = -qN_A/\varepsilon_s$ . By using (3) and (4),  $\beta = 1/(bc_p)$  is obtained.

Substituting (6) into  $\alpha_i = 1.8 \times 10^{-35} E^7$  and then substituting  $\alpha_i$  into  $\int_0^w \alpha_i ds = 1$ , one obtains

$$E_0 = 6.18 \times 10^5 V_B^{-1/6} (1 + f_p b/W)^{-1/6} \tag{7}$$

where in the calculation of the integral  $\int_0^w$ , the  $\exp(-\beta W)$  terms have been neglected and  $W=V_B/E_0$  was used.  $f_p$  is

TABLE I
GEOMETRICAL AND MODELING PARAMETERS OF THE CB-STRUCTURE
DESIGNED USING DIFFERENT CELL PATTERNS. (DERIVATIONS OF THE VARIOUS
MODEL PARAMETERS ARE GIVEN IN A PRIOR PUBLICATION [10])

Layout	Interdigitated	Hexagonal	Square	Lattice
Pattern	n p	np	n p	n p p n
а	0.5	0.36	0.465	0.5
$c_p$	0.371	0.375	0.205	0.205
$C_n$	0.371	0.211	0.178	0.205
d	0.5	0.113	0.172	0.237
$f_p$	16.1	16,3	8,91	8.91
$f_n$	16.1	9.16	7.73	8.91
$f_{cp}$	2.42	3.21	0.742	1.15
$f_{cn}$	2.42	0.76	0.833	1.15
$f_c = f_{cp} + f_{ch}$	4.84	3.97	1.56	2.3
g	1.910	1.58	1.05	1.11
g <sub>c</sub>	2.50	0.889	1.02	1.27

a constant and is listed in Table I. Similar expression can be obtained for the field line AA', and  $f_p$  is replaced by  $f_n$  which is also listed in Table I.

The term  $f_pb/W$  in (7) represents the imperfect offset of the fields by the acceptors around point B in the p-region to the donors around point A' in the n-region. Suppose  $f_pb/W \rightarrow 0$ , then  $E_0$  is the field of a p<sup>+</sup>-i-n<sup>+</sup> diode under a voltage of  $V_B$ . Due to this imperfect offset, the average field  $E_0$  becomes lower, and a larger thickness W of the CB-structure should be used compared to a p<sup>+</sup>-i-n<sup>+</sup> diode under the same breakdown voltage.

In the hexagonal and square layout, due to the fact that the p-region has a larger area (a < 0.5), and therefore  $N_A < N_D$ , it follows from (3) and (4) that  $c_p > c_n$  and  $f_p > f_n$ . Thus, the ionization integral along the line BB' is always larger than that along the line AA'. It turns out that  $f_p$  should be used to calculate the value of  $E_0$ .

The specific on-resistance  $R_{\rm on}$  of the voltage sustaining layer of an n-COOLMOS<sup>TM</sup> can be determined by  $R_{\rm on}=W/(aq\mu_nN_D)$ , where  $\mu_n$  is the electron mobility. The depletion region of the n-regions due to the built-in voltage between the n-region and the p-region has been neglected. Using (1), (3a) and (4) to eliminate W, one obtains

$$R_{\rm on} = c_n b V_B / a \mu_n \varepsilon_s E_0^2. \tag{8}$$

(9)

The value of  $\mu_n$  can also be expressed in terms of  $E_0$ . In the range of  $N_D=1\times 10^{15}$  to  $3\times 10^{16}$  cm<sup>-3</sup>,  $\mu_n$  can be expressed as  $\mu_n=2.58\times 10^4N_D^{-1/12}$  [12]. Using (3a) and (4), one obtains  $\mu_n=2.58\times 10^4(\varepsilon_s E_0/c_n qb)^{-1/12}$ . Substituting this expression into (8) and eliminating  $E_0$  using (7), one obtains

$$R_{\rm on} = 1 \times 10^{-7} g V_B^{1.32} b^{11/12} (1 + f_p b/W)^{0.32} \; \Omega \cdot {\rm cm}^2$$

where  $g=2.369c_n^{11/12}a^{-1}$ , and b and W are in microns. The values of g are from 1 to 2.5, depending on the layout pattern used, and they are also listed in Table I.

If the aspect ratio W/b of a unit cell were infinite large, then the bracket in (7) and (9) will become one, and  $E_0$  is the same electric field as in a  $p^+$ -i- $n^+$  diode under breakdown. However, the value of W/b is limited by the capability of the technology, and its finite value makes  $E_0$  to be smaller than that in the ideal case of a  $p^+$ -i- $n^+$  diode.

In the previous analysis [5], the critical field at breakdown is occurred at point C at the boundary between the p- and its neighboring n-regions as shown in Fig. 1(a). Note that at this point the field  $E_C = (E_{Cx}^2 + E_{Cy}^2)^{1/2}$ , where  $E_{Cx}$  and  $E_{Cy}$  are the vertical and lateral components of the field  $E_C$  at point C. According to the solution obtained previously [10],  $E_{Cy} = E_0$  and  $E_{Cx} = dqN_Db/\varepsilon_s$ , where d is a constant dependent on the pattern used and also listed in Table I. Using 3(a) and (4), one obtains  $E_{Cx} = (d/c_n)E_0$ . Since the value of  $d/c_n$  is less than 1.35 (d and  $e_n$  are known) for any pattern used,  $e_n$  is calculated as less than 1.7 $e_n$  after  $e_n$  and  $e_n$  are obtained. Since  $e_n$  is less than the field at point A or B which is equal to  $e_n$  breakdown will not occur at point C. Instead, breakdown will occur at point A or B at which higher field is reached.

The previously published simulation results on  $R_{\rm on}$  for a 500 V COOLMOS<sup>TM</sup> with interdigitated layout [5], [9] shows a little larger than that obtained using (9). This is because the effect of the built-in electric field across the p- and n-regions has not been considered in (9) but considered in the previously published simulation results. Since the built-in electric field will deplete part of the conducting n- and p-regions, the  $R_{\rm on}$  obtained previously is a little larger than that obtained using (9).

## III. INSULATING FILM ADDED BETWEEN THE N- AND P-REGIONS

One method that can be used to increase  $E_0$  and decrease  $R_{\rm on}$  is to reduce the donor and acceptor concentration at the top of the n-region and the bottom of the p-region, respectively. In that case, the peak field  $E_{1n}$  and  $E_{1p}$  induced by the CB-structure will be decreased. However, in doing so, a maximum field will be occurred at point C shown in Fig. 1(a), assuming that point C has a distance larger than b to the top  $p^+$ -region or to the bottom  $n^+$ -region.

From the discussion of the field at point C stated before, since  $E_0 = V_B/W$ , then the field  $E_C$  at point C is given by

$$E_C^2 = (V_B/W)^2 + (dqN_Db/\varepsilon_S)^2.$$
 (10)

In order to minimize the on-resistance under a certain bias  $V_B$ , one wants  $N_D/W$  to be maximized. That is to say, product of the two terms on the right-hand side of (10) should be maximized; whereas the sum of them should be kept constant. To satisfy the above conditions, both terms should be equal. It turns out that

$$E_0 = dq N_D b / \varepsilon_S = E_C / \sqrt{2}. \tag{11}$$

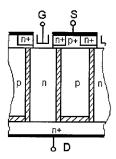


Fig. 3. A thin oxide layer between the n- and p-region of the RMOST (shaded area represents the oxide).

The field along the field lines CC' (in n-region) and CC" (in p-region) in Fig. 1(a) is shown in Fig. 1(c) and can be approximated by

$$E = E_0 + (E_C - E_0) \exp(-\beta s)$$

where s represents the distance from point C along the field line,  $\beta$  has different values for CC' and CC''. The derivation of  $\beta$  was published previously [10]. It turns out that

$$E_0 = 6.18 \times 10^5 V_B^{-1/6} [1 + (f_{cp} + f_{cn})b/W]^{-1/6}$$
 (12)

where  $f_{cp}$  and  $f_{cn}$  represent the contributions of the field in the p-region and n-region, respectively. The values of  $f_{cp}$  and  $f_{cn}$  and its sum,  $f_c$ , are listed in Table I for the different patterns. Note that  $f_c$  is smaller than  $f_p$  and  $f_n$  due to the fact that the maximum field is  $\sqrt{2}E_0$  instead of  $2E_0$  as in the case of without the insulating film in Section II.

It is interesting to point out that for the COOLMOS<sup>TM</sup>, it will still work if an insulating film exists between the n- and p-regions as shown in Fig. 3 [2]. In that case, only  $f_{cp}$  should be used in (12) since  $f_{cp}$  is larger or equal to  $f_{cn}$  for all of the patterns. This brings about a reduction on  $R_{on}$  due to the increase in  $E_0$ , and thereby an increase in  $N_D$  and a decrease in W. With such an insulating film, one obtains the same expression for minimum  $R_{on}$  as in (9), except that in (9) g should be replaced by  $g_c$  and  $f_p$  should be replaced by  $f_{cp}$ .

Two examples (one with and one without the insulating film) of a 1 KV RMOST with interdigitated layout (a=0.5) and W/b=5 are designed and simulated. Without the insulating film, according to (7) with f=16.1, one obtains  $E_0=1.54\times 10^5$  V/cm,  $W=65.2~\mu m$ , and from (3a) and (4),  $N_D=2.07\times 10^{15}$  cm<sup>-3</sup>. With an oxide thickness of 0.5  $\mu m$  between thenand p-regions and f=2.42, one obtains  $E_0=1.83\times 10^5$  V/cm,  $W=55~\mu m$ , and  $N_D=2.15\times 10^{15}$  cm<sup>-3</sup>. The latter has a reduced donor concentration at the top of each n-region by an additional acceptor implant with a dose of  $6.5\times 10^{11}$  cm<sup>-2</sup>, a characteristic depth of 3.6  $\mu m$ , and a width of 2  $\mu m$  for each cell. An additional donor implant with the same dose, depth and width at the bottom of each p-region was also used. So under 1 KV, the maximum field at A and B is lower than  $2E_0$ .

Fig. 4 shows the simulation results of both devices using MEDICI [13]. It can be seen that  $R_{\rm on}$  of the former device (without insulating film) is  $3.54~\Omega \cdot {\rm mm}^2$  and that of the latter device (with insulating film) is  $3.04~\Omega \cdot {\rm mm}^2$ .  $V_B$  of both the former and latter devices is 944 V. Thus, the latter has a reduction on  $R_{\rm on}$  of about 14%. Although 14% reduction on  $R_{\rm on}$  does not

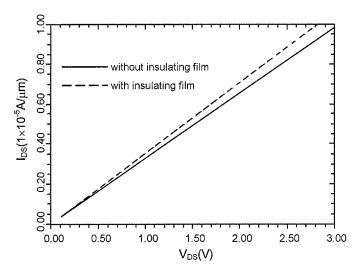


Fig. 4. Simulated  $I\!-\!V$  characteristics of two 1 KV RMOSTs at  $V_G=20$  V with (0.5  $\mu$ m) and without the insulating film.

seem to be too significant, this approach does point out a very important fact that a thin layer of oxide is indeed allowed to be placed between the alternating n and p layers in the CB-structure. This may open up opportunities for practical implementation of the structure for volume production. An example of the fabrication process is given as follows: First, an n-layer is grown on an  $n^+$ -substrate by epitaxy. Then trenches are made in the n-epi-layer and oxide is grown on the wall of the trenches. The trenches are refilled with p-type silicon. The remaining processes are the same as those for fabricating conventional power MOSFETs. Introducing an oxide layer between the p- and n-regions can also prevent the diffusion of the acceptors and donors to the opposite regions so that the value of b can be made very small

## IV. DISCUSSIONS AND CONCLUSIONS

A model to determine the physical and geometrical parameters of the different design patterns for the optimization of the specific on-resistance  $R_{\rm on}$  of the COOLMOS<sup>TM</sup> was presented. For a high aspect ratio of the CB-layer thickness, W, to the size of the unit cell, b, the  $R_{\rm on}$  from (9) is

$$R_{\rm on} = 1 \cdot 10^{-7} g V_B^{1.32} b^{11/12} \; \Omega \cdot {\rm cm}^2$$

where g has a value between 1 and 2.5 depending on the pattern used, and b is in the unit of  $\mu m$ . This relationship is a breakthrough compared to the traditional limitation of

$$R_{\rm on} = 8.3 \cdot 10^{-9} V_B^{2.5} \,\Omega \cdot {\rm cm}^2$$
 [14]

Among the different cell pattern designs, the hexagonal layout provides the lowest  $R_{\rm on}$  (with g=0.83), and the interdigitated layout has the highest  $R_{\rm on}$  (with g=1.9). The physical reason for this is that in the interdigitated layout, the charge compensation effect is not as effective as in the other layouts because in the interdigitated layout, only a 1-D compensation exists; whereas in the other layouts, 2-D compensation exists. The reason for the hexagonal layout being the best is because it is the closest-packed layout so that the compensation is most effective. Finally, between the square and lattice layouts, the

square layout is approximately 5% lower in  $R_{\rm on}$  as compared to that of the lattice layout.

For a rough comparison, a simple formula for  $R_{\rm on}$  can be obtained if  $\mu_n=1000~{\rm cm^2/Vs},\,E_0=6.18\times10^5~{\rm V/cm},$  and  $c_n/a=0.4$  are used in (10), and

$$R_{\rm on} = 1 \times 10^{-7} b V_B^{1.33} \,\Omega \cdot {\rm cm}^2.$$

For a small aspect ratio of W/b, an insulating film (approximately  $0.5~\mu m$ ) can be added between the n- and the neighboring p-regions to help to reduce the on-resistance and to add design flexibilities for practical implementation of the structure.

#### REFERENCES

- [1] D. J. Coe, "High voltage semiconductor device," U.S. Patent 4 754 310,
- [2] X. B. Chen, "Semiconductor power devices with alternating conductivity," U.S. Patent 5 216 275, 1993.
- [3] J. Tihanyi, "Power MOSFET," U.S. Patent 5 438 215, 1995.
- [4] G. Deboy *et al.*, "A new generation of high voltage MOSFET's breaks the limit line of silicon," in *IEDM Tech. Dig.*, Dec. 1998, pp. 683–686.
- [5] P. M. Shenoy, A. Bhalla, and G. M. Dolny, "Analysis of the effect of charge imbalance on the static and dynamic characteristics of the super junction MOSFET," in *Proc. 11th Int. Symp. Power Semiconductor De*vices and ICs, ON, Canada, May 1999, pp. 99–102.
- [6] Y. Kawaguchi, K. Nakamura, A. Yahata, and A. Nakagawa, "Predicted electrical characteristics of 4500 V super multi-resurf MOSFETs," in *Proc. 11th Int. Symp. Power Semiconductor Device and ICs*, ON, Canada, May 1999, pp. 95–98.
- [7] X. B. Chen, "Theory of a novel voltage-sustaining composite buffer (CB) layer for power devices," *Chin. J. Electron.*, vol. 7, pp. 211–216, 1998
- [8] T. Fujihira, "Theory of semiconductor superjunction devices," *Jpn. J. Appl. Phys.*, vol. 36, pp. 6254–6262, 1997.
- [9] T. Fujihira and Y. Miyasaka, "Simulated superior performances of semiconductor superjunction devices," in *Proc. 10th Int. Symp. Power Semi*conductor Devices and ICs, Kyoto, Japan, May 1998, pp. 423–426.
- [10] X. Chen, "Optimum design parameters for different patterns of composite buffer (CB) structure," Chin. J. Electron., vol. 9, pp. 6–10, 2000.
- [11] W. Fulop, "Calculation of avalanche breakdown voltage of silicon *p-n* junctions," *Solid-State Electron.*, vol. 10, pp. 39–47, 1967.
- [12] S. M. Sze, Physics of Semiconductor Devices, 2nd ed. New York: Wiley, 1981, p. 29.
- [13] MEDICI User Manual, Version 2.: Technol. Model. Assoc., 1994.
- [14] C. Hu, "Optimum doping profile for minimum ohmic resistance and high breakdown voltage," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 243–245, Mar. 1979.



Xing-Bi Chen (SM'91) was born in Shanghai, China. He is an Academician of the Chinese Academy of Science and a Professor at the University of Electronic Science and Technology of China (UESTC), Sichuan, and the Honorary Director of the Research Institute of Micro-Electronics. His recent interests include power devices, smart power ICs, and device physics. He has published six books and more than 40 papers and holds two U.S. patents and three Chinese Invention Patents.

Dr. Chen is a fellow of the Chinese Institute of Electronics (CIE) and an editorial member of the *Journal of Semiconductors* of China as well as board

member of Sichuan Branch of CIE. He has received more than ten awards from the Chinese Government.



**Johnny K. O. Sin** (S'79–M'88–SM'96) was born in Hong Kong. He received the B.A.Sc., MASc, and Ph.D. degrees, all in electrical engineering, from the University of Toronto, Toronto, ON, Canada, in 1981, 1983, and 1988, respectively.

He joined Philips Laboratories, Briarcliff Manor, NY, upon the completion of his Ph.D. studies, where he was Senior Member of Research Staff from 1988 to 1991. He joined the Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology (HKUST), Hong Kong,

in August 1991, as an Assistant Professor, and became Associate Professor in 1996. He is one of the founding members of the Department, and has been serving as the Director of the Undergraduate Studies program in the Department since Fall 1998. His research interests lie in the general area of microelectronic devices and fabrication technology, and is currently working in the areas of power semiconductor devices and ICs, thin-film transistors, SOI rf and power devices and technology, and integrated gas sensors for integrated microsystem applications. He holds five U.S. patents with two pending, and has published over 150 papers in technical journals and refereed conferences in the above areas.

Dr. Sin is an Editor of IEEE ELECTRON DEVICE LETTERS. He is a member of the EDS Power Devices and ICs Technical Committee. He served as technical committee member of the International Conference on Microelectronics Test Structures (ICMTS). He is also a technical committee member of the International Symposium on Power Semiconductor Devices and ICs (ISPSD). In Fall 1998, he was awarded the Teaching Excellence Appreciation Award by the School of Engineering, HKUST. He was made an Honorary Visiting Professor of the Dalian University of Technology, Dalian, China, in 1996.