Electrothermal Characterization for Reliability of Modern Low-Voltage PowerMOSFETs

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***Abstract*—This paper deals with the experimental characterization of modern semiconductor devices under realistic operational conditions. First, a method for monitoring their thermal evolution as a response to transient electrical stimuli is presented. The proposed solution belongs in the category of optical infrared methods and offers good time and space resolution. In line with the requirements of leading-edge research and development activities, it is also characterized by a high-degree of versatility, which makes it a powerful tool in many diverse lines of investigations. Then, examples of the critical operation of modern-generation low-voltage power transistors are discussed. The cases proposed are selected from an actual application scenario and well demonstrate, on the one side, the need for accurate characterization of the components and, on the other side, the validity of the chosen solution.**

***Index Terms*—Avalanche-breakdown, electrothermal effects, powerMOSFETs, reliability, short-circuit, thermal instability.**

NOMENCLATURE

$\vec{E}$	Electric field in (volts per meter).
H	Heat-generation rate in (watts per cubic meter).
$\vec{J}$	Current density in (amperes per square meter).
P_{D}	Power dissipation in (watts).
q	Elementary charge [1.6e19 C].
T	Temperature in (kelvin).
$Z_{\mathrm{Th,JA}}$	Junction-to-Ambient Thermal Impedance in (kelvin per watt).
Φ	Power flux in (watts per square meter).
c_{Th}	Volumetric heat-capacity in (joules per cubic meter kelvin).
ε	Emissivity [adimensional].
λ_{Th}	Thermal conductivity in (watts per meter kelvin).
λ	Wavelength in (meter).
μ	Mobility of the charge-carriers in (voltseconds per meter).
σ	Stefan–Boltzmann's Constant [$5.7\ 10^{-8}\ \mathrm{W}\cdot\mathrm{m}^{-2}\cdot\mathrm{K}^{-4}$].

I. INTRODUCTION

A QUEST for ever improving power-density figures has set the trend for a steady shrinkage of the dimensions of power devices. Since the heat-generation rates within the silicon dies increase correspondingly, the temperature swings that the components undergo during transient operation can be very ample and fast. Additionally, recent developments in power electronics (e.g., in automotive applications) have broadened the operational spectrum of solid-state devices, which are being employed more and more as protective elements, too [1]. In this role, the devices are meant to withstand dissipation of considerable power levels; furthermore, they are also required to work under thermally unstable bias conditions, where, as a consequence of current-crowding phenomena, very inhomogeneous temperature distributions exist and even hot-spots can be formed [2], [3]. Because of the different thermomechanical properties (e.g., the coefficient of thermal expansion) of the various materials employed in their fabrication (Si, SiO2, Al), the result is a severe stress and degradation of the transistors, particularly when repetitive switching is taken into account.

Thus, the ability to monitor the space- and time-resolved temperature distribution in power ICs as a response to pulsed electrical excitations has become crucial to many tasks and investigations, such as characterization and modeling, technology development, reliability assessment and design optimization. Simulations can be very time-consuming and generally do not allow for a quick analysis of different operational conditions. Experimental analysis is often the preferred solution. For a measurement method to be convenient, however, it needs to satisfy a series of requirements. First, proper space and time resolution are required. Then, the ability to characterize the devices in a condition descriptive of the actual application must be guaranteed. Additionally, the ability to minimize the effort associated with sample preparation, while ensuring the possibility of multiple measurements on the same sample, completes the spectrum of qualifying features for the chosen solution.

In the sequel, first, a method that satisfies all of the above requirements is described, along with the experimental solutions used to put it into practice; issues bearing relevance to its usage with low-voltage power devices are discussed in particular. Then, a selection of examples taken from an actual application scenario is presented, highlighting in particular reliability-related aspects.

II. METHOD AND EQUIPMENT FOR TRANSIENT THERMAL CHARACTERIZATION

Heat-generation mechanisms in semiconductor devices are manifold and an accurate description of the phenomenon yields nontrivial analytical expressions [4]. For the purposes of this

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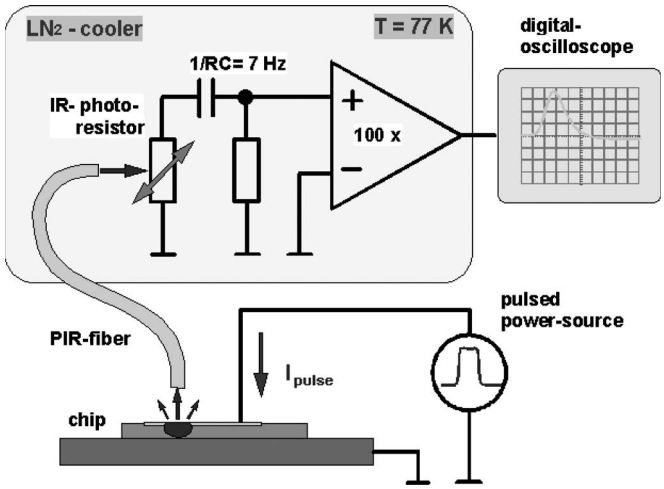


Fig. 1. Schematic representation of the setup for the fast transient thermal characterization of power devices.

paper, the main contribution can be identified in Joule's heat and the corresponding generation-rate expressed as

$$H(t) \equiv \frac{P_{\mathrm{D}}(t)}{V} = \vec{J} \cdot \vec{E}. \tag{1}$$

The heat is typically generated within a subvolume of the component and spreads across the silicon die according to

$$c_{\mathrm{Th}} \cdot \frac{\partial T}{\partial t} = \nabla \cdot (\lambda_{\mathrm{Th}} \cdot \vec{\nabla} T) + H(t) \tag{2}$$

where both c_{Th} and λ_{Th} are temperature dependent [5]–[7]. A portion of the heat-wave will reach the surface of the device, typically covered with an aluminum layer to provide a contacting surface for the wirebonds; here, it will generate thermal radiation. According to Planck's theory, the thermal power per unit surface radiated by a body at temperature T is given by

$$\Phi = \varepsilon \cdot \sigma \cdot T^4 \tag{3}$$

where ε is the emissivity $(0 < \varepsilon < 1)$ of the radiating surface and σ is Stefan-Boltzmann's constant ($\sigma = 5.7\ 10^{-8}$ W $\cdot$ m$^{-2} \cdot$ K^{-4}). Therefore, information about temperature can be extracted from a measurement of the radiated power. For power devices, in particular, the region of heat-generation is usually located in the close vicinity (i.e., few micrometers away) of the upper surface and so, for most device-types and for most widths of the electrical power pulse, the temperature measured at the surface is well representative of the maximum value reached inside the chip, usually referred to as the junction temperature of the device.

The thermal characterization procedure adopted here belongs to the category of optical infrared methods [8]. The experimental setup employed for measuring the radiated thermal power is schematically depicted in Fig. 1. An optical fiber is used to convey the infrared radiation onto a photodetector, which converts it into an electrical signal; the signal is properly processed by an amplification chain, whose output can be directly connected to an oscilloscope. The optical fiber is of multimode, polycrystalline type: it is made of a solid solution

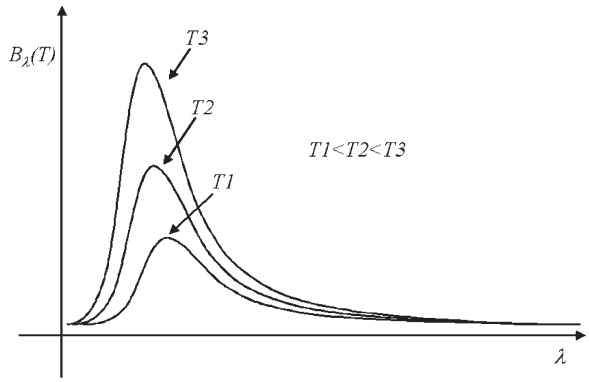


Fig. 2. Qualitative indication of the blackbody intensity of radiation as a function of wavelength.

TABLE I
WAVELENGTH OF MAXIMUM EMISSION AS A FUNCTION OF TEMPERATURE FOR A BLACK-BODY

T [°C]	λ_{max} [μm]
0	10.6
100	7.7
200	6.1
300	5
400	4.3

of silver-halide crystals and is electrically neutral, largely insensitive to mechanical disturbances and can withstand ambient temperatures ranging from below −200 °C to above 200 °C; the detector is a mercury-cadmium-telluride alloy photoconductor [9]. Fig. 2 proposes a qualitative plot of the spectral intensity of radiation, $B_\lambda(T)$, as a function of wavelength for different temperatures of the emitting body. The position of the peak as a function of temperatures is given by Wien's Displacement Law; expressing the wavelength in micrometers and the temperature in kelvin, it can be written as

$$\lambda_{\max} \simeq \frac{2898}{T} \tag{4}$$

Table I summarizes the values of $\lambda_{\max}$ for temperature values in a range of interest for the envisaged purposes. The employed system works between 8 and 12 μm, thus providing high signal resolution already at ambient temperature. Although the peak intensity of emission shifts out of the working range with increasing temperature, the overall intensity of radiation between 8 and 12 μm increases; so, signal resolution improves as the temperature gets higher. The bandwidth of the detection and amplification chain, 7 Hz to 1 MHz, enables fast transient temperature measurements, well down to the μs-range. Both the detector and the amplification circuitry are immersed in liquid nitrogen (approximately −200 °C) to optimize the signal-to-noise ratio of the equipment.

Fig. 3 shows the photographs of two PowerMOSFETs. The transistor in (a) is a vertical device in TO-220 package, with a total surface of about 25 mm^2; the transistor in (b) is in ReSURF technology [10], of the kind used to fabricate Smart-Power (Section III-C) integrated circuits (ICs in the following): its surface is about 1 mm^2 and its package is an experimental structure used in predevelopment activities. The tip of the

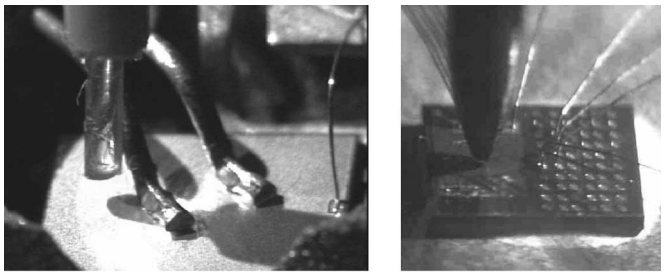


Fig. 3. (a) Photograph of a discrete low-voltage vertical PowerMOSFET, in TO-220 package: its lateral dimensions are about 5×5 mm, the cross section of the bond-wires 400 μm; the tip of the optical fiber is also visible: its diameter is 500 μm. (b) Photograph of a RESURF-technology power IC used for the predevelopment activities of Smart-Power ICs; the surface of the silicon chip is 1×1 mm^2 and the tip of the fiber in this case has a diameter of less than 200 μm.

optical fiber is also visible in both pictures: in (a), its diameter is 500 μm; in (b), the same fiber was reduced mechanically to a diameter of less than 200 μm. In both cases, as can be appreciated from Fig. 3, a sufficient space resolution can be achieved, determined by the numerical aperture of the fiber and by the distance between the surface of the device and the tip of the fiber. Another option to enhance the spatial resolution consists in the use of infrared lenses, but the handling becomes much more complex and no attempt was done here.

Some difficulties must be overcome to apply the envisaged methodology to semiconductor devices. They are discussed in detail in the next paragraphs.

A. Partial Coating for Uniform and Improved Emissivity

As already mentioned above, the surface of most power devices consists of an aluminum layer. Its emissivity is usually so low that only very small signals can be detected even at quite high temperatures, thus impairing the signal resolution of the equipment. Second, due to the fabrication of the device or to the presence of "dirt," the surface emissivity can be highly nonuniform. That makes it more difficult to extract useful information from a thermal measurement, requiring in particular a punctual calibration procedure. To increase the signal resolution even at lower temperature values and to ensure uniform emissivity, the surface of the components needs to be coated. Standard procedures, commonly used for example with infrared-cameras, imply the creation of a relatively thick additional layer, which also affects to some extent the thermal response of the device. If that is not a problem for steady-state or long time-scale measurements, it is on the other hand undesirable for measurements in the μs to ms range. To overcome such difficulties, an original partial coating procedure was developed, using a diluted carbon-based paint, properly applied to the device surface by air-spraying. Fig. 4 shows a portion of a PowerMOSFET surface. In (a) and (b), the cell structure can be recognized, without and with the coating applied, respectively. It can be observed that the coating does not consist of overlapping layers of material, but rather of isolated grains, with dimensions of some micrometers. Thus, it does not introduce any significant thermal time-constant. Fig. 4(c) displays the

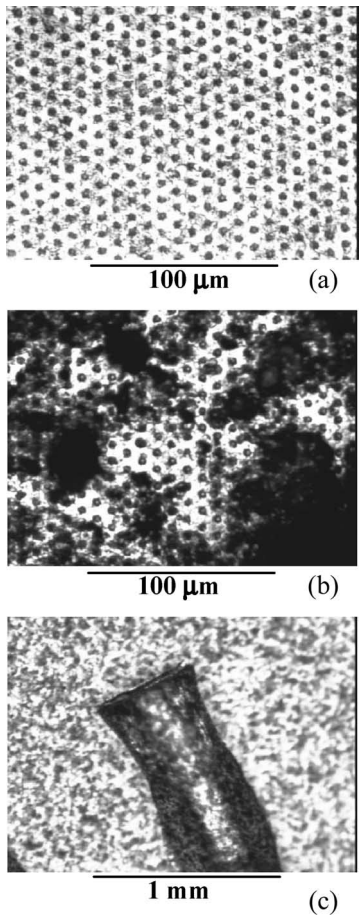


Fig. 4. Coated and uncoated surface of a PowerMOSFET at different levels of magnification. (a) 100 μm. (b) 100 μm. (c) 1 mm.

device at a lower level of magnification (a source bonding-pad is also visible): here the homogeneity of the coating (i.e., of the surface emissivity) on a larger scale can be appreciated. This kind of coating can be easily removed, simply by immersing the transistor into an acetone bath, without any damage for the device.

B. Calibration

Quantitative temperature measurements can be obtained after proper calibration. Various possibilities can be considered, also depending on the device being measured. In this case, the following solution is chosen. The PowerMOSFET is heated up at various steady-state temperatures, while monitoring its junction temperature by means of the forward voltage drop of the body-diode [11]. The corresponding voltage–temperature characteristics have been measured independently by the chip manufacturer.

To the end of generating a transient signal, as required by the detection and amplification chain, the optical fiber was mechanically shifted between the coated component, at a given stationary temperature, and a reference-object. The tip of the fiber was fixed onto a sliding bar, connected to a cylindrical motor. Thus, rotation could be transformed into a periodical horizontal translation at a proper frequency (25 Hz in this case). With regard to the choice of a proper reference, a sample

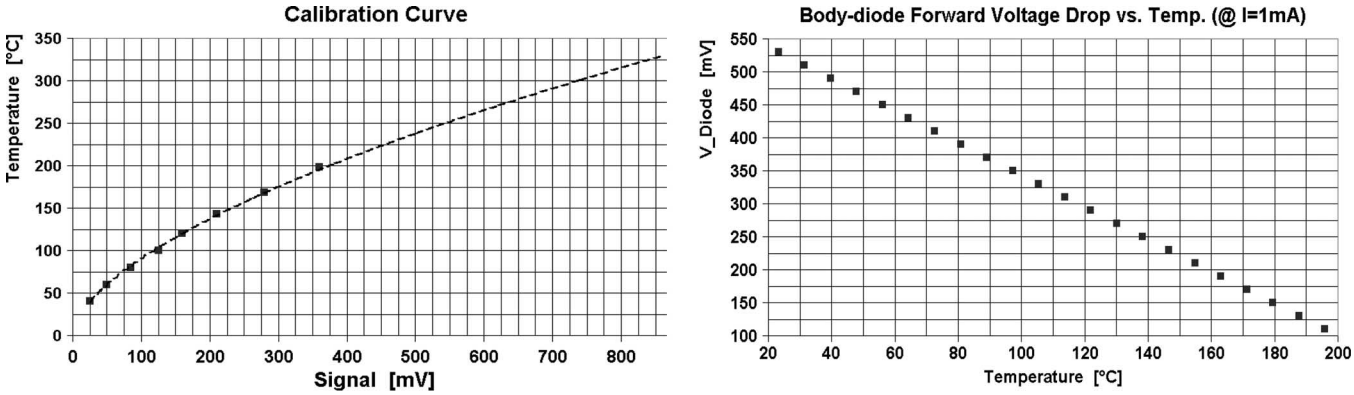


Fig. 5. (a) Sample calibration curve: the square marks represent the measurements, the dashed is the fitting curve used for extrapolation at higher temperature values. (b) Body-diode forward voltage-drop as a function of temperature, for the PowerMOSFET in a Smart-Power IC.

of highly reflective material was used. Emissivity equals absorptance at thermal equilibrium (Kirchhoff's Law); therefore, good reflective materials (i.e., bad absorbing ones) emit very poorly and are thus very good mirrors at higher temperatures. In this case, plated gold was chosen, which shows with good approximation ambient temperature all over the range of interest, indicatively 25 °C to 400 °C. This allows for the positioning of the reference-object in the direct vicinity of the device under test (DUT in the sequel), minimizing the oscillation amplitude and not requiring any particular mechanical solution to avoid the warming-up of the DUT.

With the chosen calibration method, the DUT can only be heated up to about its maximum specified steady-state temperature, which is below 200 °C for most commercial devices. During transient operation, however, temperatures far in excess of such value can be reached at some chip locations. The required extension of the calibration curve to higher temperatures was obtained by polynomial interpolation of the measured values. The calibration procedure can be performed repeatedly, until a satisfying agreement among the fitting curves is obtained. An example of a calibration curve is provided in Fig. 5(a), with (b) displaying the voltage–temperature characteristics of the body-diode.

An alternative to the method discussed above is the use of a coated cold object as a mirror. Since its emission properties are mainly determined by the coating itself if properly applied, it would be in principle only necessary to perform the spray-coating of the DUT and of the reference-object at the same time, to guarantee that the two bodies have approximately the same emissivity. Since the spray-coating process is performed manually, however, it is sometimes not so easy to satisfy such condition. Furthermore, the reference-object needs to be located, for practical reasons, relatively close to the component which is heated up, so that precautions must be taken to ensure that it is kept at reference temperature. This is also nontrivial in many cases, when standard equipment (i.e., quite cumbersome heat-plates) is used and may require a mechanical preparation of the reference in order to reduce the heat-flow between it and the DUT.

A second possibility consists of sacrificing a component for the sake of calibration; that is, of using a second device as a hot-body that can be heated-up to the maximum temperature of interest. The problem remains, however, that the equality between the emissivity of the DUT and that of the substitute can only be checked at lower temperatures. When heated up to a steady-state temperature of 300 °C and above, the coating is observed to undergo modifications, which are on the other hand not observed on the devices, even if they reach the same or higher temperature levels at some locations during transient operation.

All of the solutions considered above were tried out and the method summarized in Fig. 5(a) and (b) emerged as the most convenient. In some cases it has been possible to compare the experimental results with accurate finite elements method simulations [12] and theoretical predictions, obtaining very satisfactory agreement.

It must be noted that, to account for the relative orientation of the emitting surface and of the observer, (3) needs to be corrected with a $\cos\theta$-factor, where θ is the angle between the normal to the surface of the radiating body and the line of sight of the observer [13]. For all measurements presented here, $\theta = 0$ can be reasonably assumed.

III. Experimental Results

A. Avalanche-Breakdown

Avalanche-breakdown is becoming more and more relevant in modern power applications. This operational mode is taken advantage of to dissipate the energy contained within inductive components (both parasitic and load inductances), thus sparing on additional protection circuitry, such as clamps and snubbers [14]. The operation of a PowerMOSFET in avalanche-breakdown can be explained with the help of Fig. 6: a current I_{BD} is forced into the device, from drain to source terminal, with no gate voltage applied (i.e., no channel existing); this current flows then as inverse current of the p^{+}-n^{-} junction formed by the source well (p^{+}) and the drift region (n^{-}); the junction is thus reverse-biased and the voltage across it reaches the breakdown value, V_{BD}, already for quite low values of I_{BD}.

The highest current density is to be found at the curvature of the p^{+}-zone, so that I_{BD} features lateral flow in this region

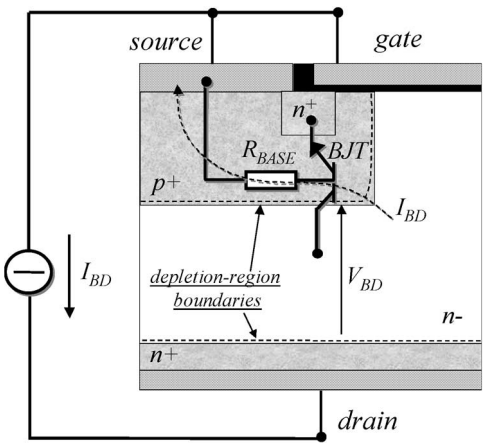


Fig. 6. Operation of the DUT during avalanche-breakdown.

to reach the source contact. Here, it causes a voltage drop across the resistance of the p^+-well, indicated as $R_{\rm BASE}$ in Fig. 6. This resistance can be approximately described as

$$R_{\rm BASE}(T_{\rm J}) = \frac{1}{q \cdot \mu(T_{\rm J}) \cdot N_{\rm A}} \cdot \frac{1}{S} \tag{5}$$

where $N_{\rm A}$ indicates an average doping value for the p^+-region, l its lateral dimension and S its cross section. If the voltage drop across it becomes high enough to forward-bias the p^+-n^+ junction in the source region, then the intrinsic bipolar junction transistor (BJT) formed by the n^--p^+-n^+ structure is biased in its forward active region and starts conducting. Since bipolar transistors exhibit a positive temperature coefficient of the collector-emitter current [15], if activation of the BJT takes place the current distribution within the MOSFET can become highly nonuniform and can lead to the formation of hot-spots and thermal runaway and thus to the failure of the transistor [16]. Since the value of $R_{\rm BASE}$ and the minimum voltage drop required to forward bias the intrinsic BJT are both functions of temperature, its maximum value plays a central role in the failure of the PowerMOSFET. Technological improvements aimed at reducing the value of $R_{\rm BASE}$ have resulted in the production of avalanche-rated devices.

In the application, a PowerMOSFET is typically driven into avalanche breakdown as a consequence of the interruption of a low impedance path for an inductive current, which, to satisfy its condition of continuity, forces its way into a high impedance one. The conditions encountered in real applications can be reconstructed by means of the circuit schematically depicted in Fig. 7: when S is closed, the inductor current increases proportionally to $\rm Vin/\mathit{L}$; if S is opened, then the inductor current flows into the parasitic circuit capacitance, charging it up. By proper choice of S, the DUT can be driven into avalanche breakdown first. This condition is held until the energy contained in L has been fully dissipated (i.e., the current has dropped to zero). Then, the time in avalanche, $t_{\rm AV}$, equals

$$t_{\rm AV} = \frac{I_0 \cdot L}{V_{\rm BD} - \rm Vin} \tag{6}$$

where I_0 is the initial value of the breakdown current and $V_{\rm BD}$ is the breakdown voltage of the DUT.

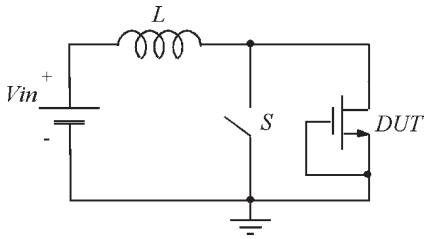


Fig. 7. Schematic of the circuit used for the experimental characterization of the devices in the avalanche breakdown condition.

Often, the ability of a transistor to withstand single or repetitive breakdown events is expressed in terms of energy. With relevance to the circuit of Fig. 7, the total avalanche energy dissipated within the device can be written as

$$E_{\rm BD} = \frac{1}{2} L I_0^2 \cdot \frac{V_{\rm BD}}{V_{\rm BD} - \rm Vin} \tag{7}$$

where $V_{\rm BD}$ is the breakdown voltage of the device and Vin the nominal input voltage. However, the information about energy is not particularly meaningful when given alone, since there is no direct relation between the energy dissipated and the maximum temperature reached inside the device. Simulation is used to exemplify the above assertion: power pulses of different amplitude and duration, but corresponding to the same total energy, are applied to a thermal-impedance and the resulting temperature evolution calculated. Constant thermal properties are assumed, so that the temperature relates to the instant power dissipation, $P_{\rm D}(t)$, as

$$T_{\rm J}(t) = T_0 + \int_0^t P_{\rm D}(\tau) \cdot \frac{dZ_{\rm Th,JA}(t-\tau)}{dt} d\tau \tag{8}$$

where $Z_{\rm Th,JA}(t)$ indicates the junction-to-ambient thermal impedance of the component.

Fig. 8(a) shows the results for the case of a triangular power pulse applied: higher maximum temperatures are obtained increasing I_0 and decreasing the value of L, for a constant value of the breakdown energy (i.e., the time-integral of the power waveforms). Fig. 8(b) proposes the comparison between a triangular and a square power pulse, both amounting to the same total energy. In this case also, the peak temperature is higher for a higher initial value of the power pulse. Therefore, the information the maximum avalanche energy specification depends on the initial current and temperature values.

The ability to monitor the thermal evolution of a transistor for different initial conditions is of fundamental importance for guaranteeing the safe operation of the device, particularly when power pulses of considerable amplitude and short duration are considered. Fig. 9 proposes the results of a measurement performed on a 75 V/80 A avalanche-rated vertical PowerMOSFET, in TO-220 package [the same device shown in Fig. 3(a)]. $V_{\rm DS}$ and $I_{\rm DS}$ indicate the drain–source voltage and current, respectively; ΔT the temperature increase at the point of measurement on the surface. The total dissipated energy amounts in this case to about 25 mJ, which is still far below

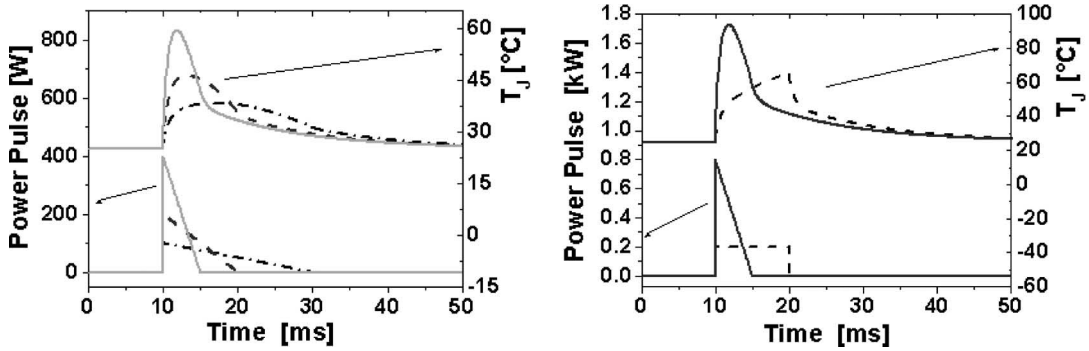


Fig. 8. Evolution of the device junction temperature as a response to different total dissipated energy, left, and for the same energy applied, but by means of different power pulses, right.

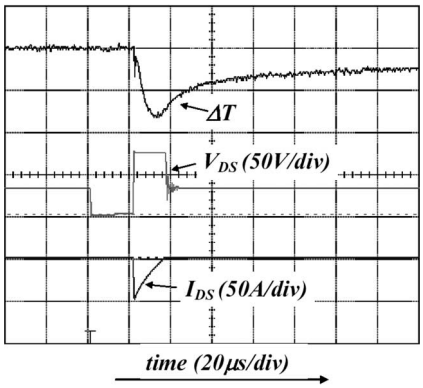


Fig. 9. Measured drain-source current, $I_{\rm DS}$, drain-source voltage, $V_{\rm DS}$ and temperature increase for a PowerMOSFET driven into avalanche breakdown.

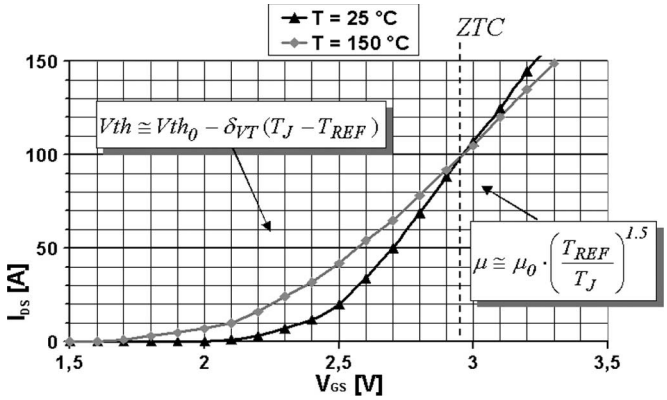


Fig. 10. Transfer characteristics of a low-voltage PowerMOSFET measured at two different temperature values.

the maximum single event specification for the considered transistor: the power is dissipated uniformly over all cells and no failure is observed. This result well demonstrates the suitability of the method proposed to be used for very fast transient measurements, well down into the microseconds-range and provides very useful information for the characterization of the behavior of the device in avalanche-breakdown (e.g., for the calibration of simulation models).

B. Thermal-Instability and Short-Circuit

Fig. 10 shows the transfer-characteristics of a low-voltage PowerMOSFET, measured at 25 °C and 150 °C, respectively. These results can be interpreted in relation to the temperature coefficient of the drain current

$$\alpha_{\rm T} = \frac{\partial I_{\rm DS}}{\partial T} \tag{9}$$

which is seen to change sign as a function of $V_{\rm GS}$. More precisely, for moderate values of $V_{\rm GS}$, $\alpha_{\rm T}$ is positive—an increase in temperature causes an increase of the drain current. At higher values of $V_{\rm GS}$, however, the device exhibits a negative $\alpha_{\rm T}$, with the current decreasing as a result of a temperature increase. The explanation for such behavior is to be found in the decrease with temperature of the threshold voltage, Vth, and of the carrier mobility, μ, which prevail in one or the other case, respectively. The transition between the two operational regions is referred to as the point of zero temperature coefficient

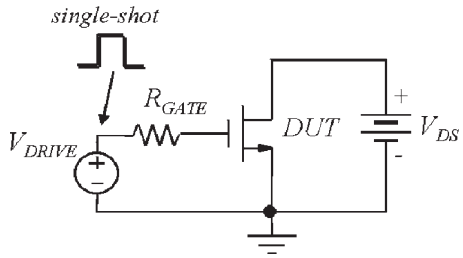


Fig. 11. Schematic of the circuit used for the experimental characterization of the devices in thermally stable and unstable conditions.

(ZTC in Fig. 10 and in the following). Clearly, the operation left of the ZTC is thermally unstable. Moreover, hundreds of thousands of basic cells are connected in parallel to make up a PowerMOSFET; thus, due to inevitable mismatches in their electrothermal characteristics, operation of the transistor left of the ZTC can quickly lead to nonuniform power-sharing among them.

When a PowerMOSFET is used as a high-frequency switch in power conversion circuitry (i.e., dc–dc, ac–dc converters), it is either on or off, that is, its $V_{\rm GS}$ swings from the off-value up to a full ON-state value in very short times. However, in modern applications, the transistors are being used more and more as protective elements, for example as circuit-breakers or load-dumping elements. In this case, their $V_{\rm GS}$ becomes a function of a variable to be controlled and it can span all over the range of allowed values [3]. Some studies have also pointed out that

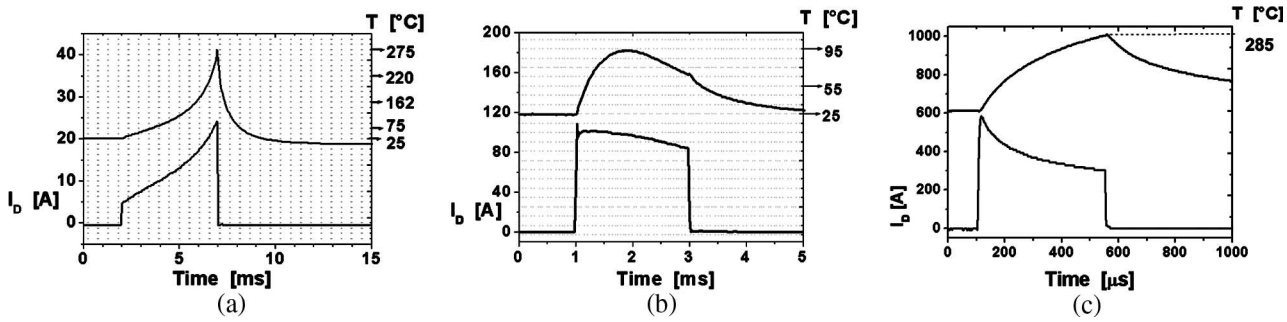


Fig. 12. Experimental results. (a) (Bottom) Current and (top) temperature waveforms for the device biased left of the ZTC: the existence of positive feedback between current and temperature is manifest. (b) (Bottom) Current and (top) temperature waveforms for the device biased right of the ZTC, where operation becomes stable. (c) (Bottom) Current and (top) temperature waveforms for the device biased at the far-end of the thermally-stable region of operation (short-circuit). For all pictures, the left axis corresponds to the bottom curve, the right axis to the upper one.

the region of thermally unstable bias conditions broadens inversely to the channel length [17], [18] and so, operation under thermally unstable bias conditions is a concern for devices of the modern generation, including trench technologies.

Fig. 11 shows the schematic of the circuit used for experimental analysis. In this case, a voltage, $V_{\rm DS}$, of constant amplitude is applied between the drain–source device terminals, while a single-shot pulse, $V_{\rm DRIVE}$, of variable amplitude and width is applied between gate and source. Therefore, the device can be biased left or right of the ZTC. The same transistor type as in the case of avalanche breakdown is considered. In the transient regime, the observations made above translate into the results of Fig. 12, which reports the drain–source current and temperature increase on the chip surface, for the transistor driven with constant $V_{\rm DS}$, while $V_{\rm GS}$ decreases from around 12 V in Fig. 12(a) to slightly above threshold in the case of Fig. 12(c); Fig. 12(b) corresponds to an intermediate value. Whereas the device is in a self-protecting operational mode in the case of Fig. 12(a) and (b), the situation reverses as $V_{\rm GS}$ is decreased [Fig. 12(c)]. These results identify three distinct working conditions, referred to in the sequel as short-circuit [Fig. 12(a)], stable operation [Fig. 12(b)], and thermally unstable operation [Fig. 12(c)].

Thermally unstable operation and short-circuit are both associated with the achievement of very high junction-temperatures, still before any failure occurs. On the other hand, significant differences can be also detected between the two operational modes.

In short-circuit, since the device is in the region of negative $\alpha_{\rm T}$, the temperature is evenly distributed within the silicon chip; in the unstable region, on the other hand, the spread in threshold-voltage value and the mismatch in thermal coupling among the many cells lead to current-crowding phenomena and to the formation of hot-spots [2]. Fig. 13 proposes the photographs of the analyzed transistors: the device in (a) has failed under thermally unstable bias conditions; the one in (b) under short-circuit conditions. These failure patterns were found repetitively and confirmed the fact that the location of failure was next to the bond-wire for operation in thermal instability and beneath the bond-wire for operation in short-circuit. Just as for the case of avalanche-breakdown, the ultimate cause of failure in both cases is the activation of the intrinsic BJT, due to thermal generation of carriers [2], [18].

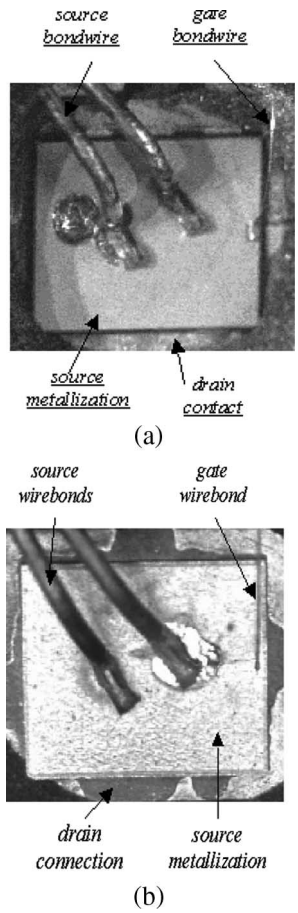
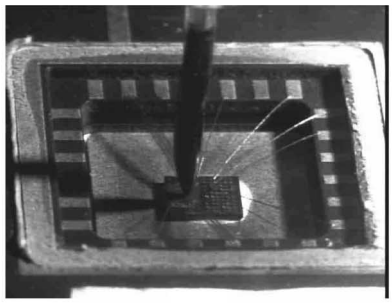
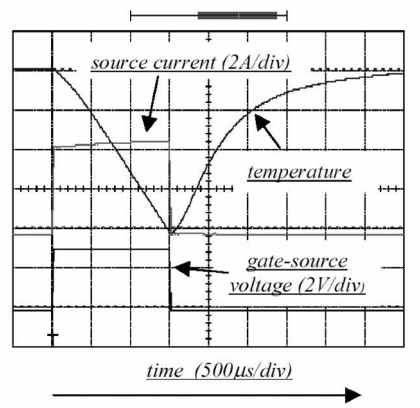


Fig. 13. (a) Photograph of a PowerMOSFET (a 75 V-80 A rated transistor in TO-220 package) failed in conditions of thermal instability. The hot-spot and eventual location of failure, clearly recognisable, is always located in the close vicinity of the bonding pad. (b) Photograph of the same device type failed in short-circuit operation. In this case the hot-spot is positioned just below the bonding-pad.

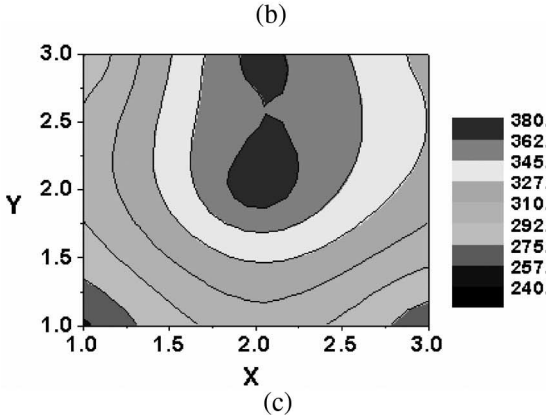
The difference in the location of failure can be attributed to the relative features of thermally stable and unstable behavior of the transistor and to the influence of the bond-wires in either case. In fact, according to the value of current being conducted (indicatively, 10 and 400 A in Fig. 12(a) and (c), respectively) the bond-wire can act as a heat-sink or as a heat-generator. Thus, it is reasonable to assume that the cells beneath the



(a)



(b)



(c)

Fig. 14. (a) Photograph with view of package for the device of Fig. 3 (b); (b) transient waveforms for the transistor driven under thermally unstable bias conditions; (c) corresponding thermal map at the time of maximum temperature.

bonding pad are colder than the surrounding ones in the case of thermally unstable operation.

For the sake of completeness, an additional result for operation under thermally unstable bias conditions is presented. It refers to the device shown in Fig. 3(b), a PowerMOSFET in ReSURF technology, of the kind used in fabricating Smart-Power ICs (see next section), with a surface of around 1 mm^2. In the case considered, the packaging represents an experimental solution used for predevelopment activities [Fig. 14(a)]. Fig. 14(b) displays the transient waveforms of the gate–source voltage, drain–source current, and temperature increase on one point of the chip surface. As mentioned above, the tip of the fiber, also visible in Fig. 14(a), had a diameter of less than 200 μm in this case. By acquiring such measurements as in Fig. 14(b) at various locations of the chip surface, thermal maps of the kind proposed in Fig. 14(c) could be generated (the

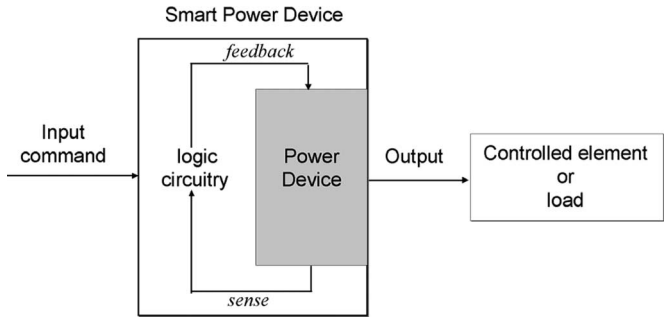


Fig. 15. Scheme of principle of a Smart-Power device.

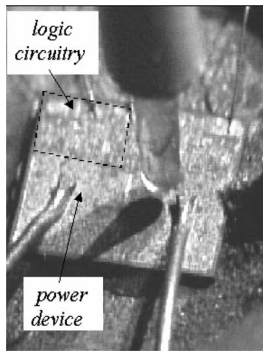


Fig. 16. Photograph of a Smart-Power-IC chip for automotive applications. The tip of the infrared fiber can be also recognised.

x- and y-coordinates correspond to an arbitrary partition of the chip surface). Here, due to the absence of bonding pads, the hot-spot is located in the center of the device. The different thermal behavior at the top and at the bottom of Fig. 14(c) can be directly related with the employed packaging concept. The results of Figs. 12(a) and 14(b) both correspond to a drain–source voltage of 20 V. It can be appreciated, however, that although the current is lower in this case, much higher peak temperatures are reached with shorter pulsewidths. This is due to the smaller volume of the transistor and to the correspondingly higher heat-generation rate. Such results also represent fundamental information for the development of robust transistors.

C. Smart-Power-IC With Integrated Temperature Sensor

As schematically represented in Fig. 15, Smart-Power-ICs owe their name to the fact of consisting of one or more power devices, typically used as transducers toward a load, monolithically integrated with logic circuitry that controls their operation according to the demands of the load. To provide the signals for the control unit, the current needs to flow through proper sensing elements, typically located on the chip surface, so that a horizontal current flow is required. Therefore, the power device is often a MOSFET in lateral technology.

Fig. 16 shows a Smart-Power IC. Each of the "bigger" bonding pads indicates one lateral PowerMOSFET; the smaller bond-wires connect the logic circuitry to the outer world. Each power device is about 1.5 by 1.5 mm and the dimensions of the whole chip are about 3.5 by 2.5 mm, in a 16-pin DIP package. The IC is used repetitively to limit the short-circuit current flowing through it. A temperature sensor is integrated in the

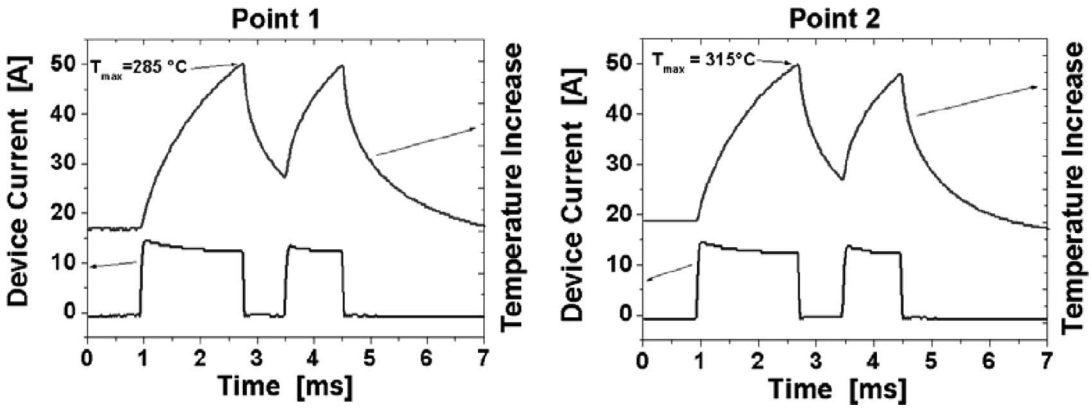


Fig. 17. Measured current and temperature waveforms on two different points of the chip surface.

device and, if the temperature reaches an upper threshold, the transistor is switched off. After the temperature has fallen below a given threshold, the device automatically turns on again. Such devices are used, for example, in lamp-ballasts for automotive applications. During operation as current limiter, the power density on the active chip area can reach values of up to 100 W/mm^2.

Fig. 17(a) and (b) display the drain current of the device and the temperature waveform as measured on two different points of the chip surface. An enable signal, not reported in Fig. 8, is applied at Time = 1 ms and removed after 4 ms. In line with the above description, between 2.5 and 3 ms, an automatic turn-off of the PowerMOSFET takes place as soon as the higher temperature threshold is exceeded at the location of the sensor. Then, at about 3.5 ms, the transistor is automatically turned on again. At 4.5 ms, automatic turn-off takes place again. Such behavior continues as long as the enable signal is kept high. The results of Fig. 17 clearly indicate the occurrence of very high maximum temperatures. The existence of a temperature gradient on the small chip surface during operation is also evident. The proposed analysis reveals that the position of the temperature sensor does not correspond exactly to the location of highest temperature. This information is essential for the improvement and the optimization of the design of the IC, in particular with a view to ensuring the required safe operational lifetime: the peak temperature constitutes, along with the repetition rate of the power pulses, one of the main factors influencing the lifetime of power devices [19]. The measured values fully correspond to the degradation and failure mechanisms independently observed on the devices as part of routine reliability tests.

IV. Conclusion

Modern power electronics applications have broadened the operational spectrum of low-voltage PowerMOSFETs. In particular, the transistors must withstand increasing heat-generation levels and at the same time comply with tight performance and reliability requirements. Since the reliability of the components is strictly related to the temperature excursions they experience, the ability to monitor their thermal evolution as a response to an electrical excitation is becoming paramount. The experimental method, however, must enable realistic characterization possibility (i.e., under conditions descriptive of those found in the application), while offering proper space and time resolution and a certain degree of versatility. The approach described in this paper satisfies all of these conditions. A selection of examples derived from an automotive application scenario has demonstrated the validity of the proposed solution, which qualifies as a powerful tool for the electrothermal characterization of low-voltage components in many different lines of investigation. In particular, device engineers can use experimental data to sustain and complement simulation in developing more robust components; application engineers and power electronics designers can gain a deeper insight and develop a better feeling about the actual limits of safe operation of the transistors.

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