Architecture and Design Analysis of a Digital Single-Event Transient/Upset Measurement Chip

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Abstract—**This paper presents the architecture and a detailed design analysis of a digital measurement chip which facilitates long-term irradiation experiments of basic asynchronous circuits. It combines radiation targets like Muller C-elements and elastic pipelines as well as standard combinational gates and flip-flops with an elaborate on-chip measurement infrastructure. Major architectural challenges result from the fact that the latter must operate reliably under the same radiation conditions the target circuits are exposed to, without wasting precious die area for a rad-hard design. A measurement architecture based on multiple non-rad-hard counters is used, which we show to be resilient against double faults, as well as many triple and even higher-multiplicity faults. The analysis is done by means of comprehensive fault injection experiments, which are based on detailed Spice models of the circuits in conjunction with a standard double-exponential current injection model for single-event transients. We also provide probabilistic calculations of the sustainable particle flow rates, based on the results of a detailed area analysis in conjunction with experimentally determined cross section data for the ASIC implementation technology used. The results confirm that the overall architecture indeed supports significant target hit rates, without exceeding the resilience bound of the measurement infrastructure.**

I. INTRODUCTION

TU Vienna's FATAL project (Fault-tolerant Asynchronous Logic)[1] is devoted to the foundations of a framework for modeling and analysis of fault-tolerant asynchronous digital circuits, using fault-tolerant distributed algorithms knowledge [1]. Besides handling circuit/environment specifications, composition & decomposition and hierarchical proofs [2]–[4], it also addresses adequate failure and metastability models for digital circuits. Unlike most research in this area, FATAL is primarily (albeit not exclusively) focusing on asynchronous circuits. This is backed-up by the fact that, ultimately, the operation of any combinational digital logic gate is inherently asynchronous. Moreover, asynchrony is also a quite natural phenomenon at higher system layers, as in *Globally Asynchronous, Locally Synchronous* (GALS) architectures [5], for example. Unfortunately, unlike for synchronous systems, fault-tolerance is difficult to guarantee in asynchronous systems [6], and has hence received not much attention in asynchronous digital circuits [7]–[11].

In order to systematically reason about fault-tolerant VLSI circuits, suitable failure models are mandatory. For "classic" sources of errors, like aging and electric wear-out [12], there is a huge body of work to rely upon. For radiation-induced errors, however, which are increasingly dominating the failure rate of deep submicron VLSI circuits [13], [14], this is not the case. Radiation-induced errors, collectively termed *single-event effects* (SEEs) in literature, occur when the active area of a VLSI circuit is hit by ionized particles (or even by neutrons, which typically result from heavy ion interactions with nitrogen or oxygen atoms in the atmosphere).

As opposed to permanent SEEs such as latch-up, threshold voltage shifts and even destructive burn-outs in power semiconductors [15]–[17], the primary concern in modern VLSI circuits are transient SEEs: An ionized particle hitting a reverse-biased junction of a transistor deposits charge along its track, which in turn can cause a *single-event transient* (SET) pulse (0.1–1 ns range) at the output. If the affected transistor is part of a storage element (e.g. an SRAM cell or a latch), this may cause the element to flip its state, leading to a *single-event upset* (SEU). Unfortunately, SEUs may also occur if the hit transistor is part of combinational logic, since a sufficiently strong SET may propagate until it reaches a storage element where it is latched. In any case, however, the errors resulting from SEUs are not permanent but rather transient (i.e., can be corrected), and are hence called *soft errors*.

This paper presents the architecture and a thorough design analysis, based on a detailed Spice model, of a special digital radiation target chip (FRad Chip) that facilitates long-term monitoring of radiation-induced failures in basic asynchronous circuits. It is organized as follows: After a very brief overview of our overall approach and some related work in Sec. II, we describe and justify the selection of our radiation targets resp. measurement architecture in Sec. III resp. V. Sec. VI is devoted to the analysis of the resulting area requirements and fault-tolerance properties, which employ the SET current injection model described in Sec. IV. Sec. VII provides a probabilistic analysis based on cross-section data. Some conclusions in Sec. VIII eventually complete the paper.

II. FATAL GENERAL APPROACH AND RELATED WORK

The ultimate goal of FATAL is *not* the faithful and detailed modeling of the generation and propagation of SETs/SEUs in a

circuit (which is the usual approach, see e.g. [18]), but rather the development of a *digital failure model* that focuses on the *observable behavior* of a digital circuit under radiation, at some chosen level of detail (see e.g. [19] for an early example of this approach). Clearly, developing a meaningful digital failure model primarily requires means for validating and calibrating the failures predicted by the model for certain operating conditions (which of course also include radiation field characteristics) w.r.t. the actual failures observed in a real chip under these conditions.

As validating and calibrating candidate digital failure models cannot reasonably be done by means of experiments with real circuits due to lacking controllability and excessive measurement times and efforts, we use two intermediate lower-level simulation models, the *3D model* and the *Spice model*, for this purpose, cp. [20]–[22]. The 3D model is a Synopsis 3D TCAD model of our elementary target circuits, which include (a chain of) inverters, Muller C-gates, etc. Particle hits are incorporated via the SRIM-TRIM nuclear code simulation software [23]. In order to calibrate the 3D model, which also depends on technology parameters like doping profiles, we manufactured our target circuits in 90 nm UMC CMOS technology and performed analog SET recording experiments under carefully controlled micro-beam irradiation at the GSI in Darmstadt [24].

The Spice model consists of the analog schematics models of our target circuits augmented by Spice models that mimic SET generation in all critical parts. For the latter, we use single-ended injection of a double-exponential current into the drain of a transistor [25], appropriately calibrated according to the 3D model simulation results. Since Spice model simulations are orders of magnitude faster than 3D model simulations, the Spice model finally turned out to be a suitable tool for the thorough (and reasonably fast) investigation of the SET behavior of any digital circuit made up of an arbitrary combination of our elementary target circuits.

Nevertheless, in order to rule out unnoticed modeling errors in the 3D model and/or in the Spice model, and to validate the accuracy of the digital failure model w.r.t. technology-related parameters like transistor sizes, doping profiles etc., we are currently designing a special digital FRad Chip (and its corresponding Spice model) that will allow us to do long-term digital monitoring of radiation-induced failures. Its design and pre-fabrication analysis and evaluation are the main focus of this paper.

SET test circuits for radiation experiments described in the literature use a variety of selective SET capturing methods [26]–[28], variable delay latches [29], or self-triggered inverter + latch chains [30]–[32] for digital SET pulse-width measurements; they have been designed and used primarily for SET characterization in short-term experiments. By contrast, our FRad Chip incorporates digital measurement circuitry that *continuously* captures and counts radiation-induced failures in long-term experiments. Unlike for SEUs, where bit-flips in SRAM memory arrays are a convenient means for collecting SEU statistics, see e.g. [16], we are not aware of any existing test circuit for collecting SET statistics.

III. SELECTION OF RADIATION TARGET CIRCUITS

The specific purpose of the FRad Chip leads to the following design requirements and constraints:
• There is no need to capture analog effects.
• The transformation of analog effects to the digital domain obviously influences digital observations. In order to be as realistic as possible, this transformation shall solely be performed by the target circuits (implicitly).
• In order to get relevant results, we need to select target circuits that are elementary and/or frequently used in practice.
• To explore the behavior of target circuits both in dynamic and steady state, we need the option of exercising/stimulating the targets when exposed to radiation.
• We want to apply sources of radiation whose characteristics is similar to what circuits are typically exposed to in practice. These sources have in common that (a) time and location of particle hits are not controllable, (b) the particle hit rate is reasonably low, and (c) the target has to be brought into some environment (e.g., a radiation chamber) that is spatially confined. This substantially impacts the design of the overall measurement infrastructure.

Considering these issues, we have decided for a set of target circuits that will be detailed below.
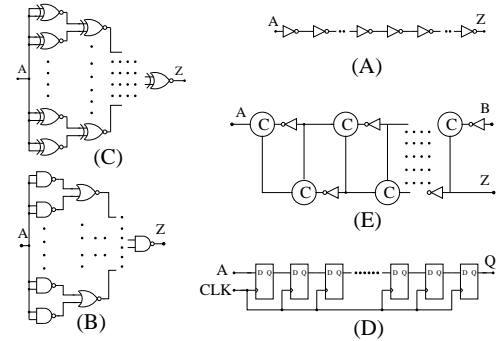

Fig. 1.   Gate Level Schematics of Target Circuits

A. Inverter Chain

Inverters are the most basic and simple elements in CMOS and thus the preferred radiation targets in the existing literature. For a given transistor sizing, they are also the fastest CMOS circuits, thus potentially vulnerable to even very short SETs. Incorporating inverters in our study is hence not only relevant in practice, but also allows us to compare our results to the literature. In order to have a reasonably large target area and a rich testbed for investigating propagation effects, we provide a chain of 17 inverters, as shown in Fig. 1.(A) (in fact, multiple instances thereof).

B. NAND-NOR Tree

NAND trees have always been a topic of interest in terms of testing and SETs. NAND and NOR implementations are slightly more complex than inverters and therefore exhibit different phenomena. One is the availability of two inputs,

which allows us to form a tree structure. Another one is the possibility of logical masking of errors.

We have 64 NAND gates in the first stage that are all driven by a single input signal, which allows us to jointly stimulate activity with minimal overhead. The outputs of the NAND gates fan-in as inputs for NOR gates and so on, yielding a tree with 127 gates in total, see Fig. 1.(B). The tree has 7 levels, hence in the fault-free case the output will be the inverse of the input.

C. XNOR Tree

The XNOR gate forms the equivalent of the logical OR for transitions, another very basic functionality in asynchronous circuits and also fundamental for parity checking circuits. Compared to NAND/NOR gates, it has a very different internal structure. We use a XNOR gate implementation based on a CMOS transmission gate with inverter.

We again use a 7 level tree structure. It is apparent from Fig. 1.(C) that two outputs of XNOR gates fan-in to an XNOR gate at the next level. The inputs of the 64 XNOR gates in the first stage are again all connected to a single input. Due to the XNOR function all gates will therefore, independently from this input, present a logic 1 at their outputs, and the tree output will transiently go to low only in case of an SET somewhere in the tree. As we will see, this behavior is very convenient for our purposes.

D. Flip-Flop Chain

Flip-flops are the fundamental building blocks of virtually every synchronous design. Like inverters, they have hence received much attention in radiation-related research in the past, which will allow us to compare our results against existing data. As shown in Fig. 1.(D), we provide a chain of 33 edge-triggered D-flip-flops, which are implemented using transmission gates and inverters.

E. Elastic Pipeline

An elastic pipeline is built from Muller C-elements and inverters as shown in Fig. 1.(E). A Muller C-element is *the* fundamental building block in the design of self-timed digital circuits [33]. Although it can be viewed as a (combinational) AND for transitions, it is a state-holding element much like an asynchronous set-reset latch. Three different CMOS implementations have become popular, all of which we will use as target circuits:

- a) CMOS implementation introduced by Van Berkel [34], see Fig. 2.(a).
- b) CMOS implementation using an inverter latch introduced by Martin [34], see Fig. 2.(b).
- c) Conventional pull-up pull-down CMOS implementation introduced by Sutherland [34], see Fig. 2.(c).

The elastic pipeline in Fig. 1.(E) is essentially a FIFO buffer for signal transitions that is often used in handshake-based circuits. The C-elements in the pipeline propagate the signals in a carefully controlled way that maintains the integrity of
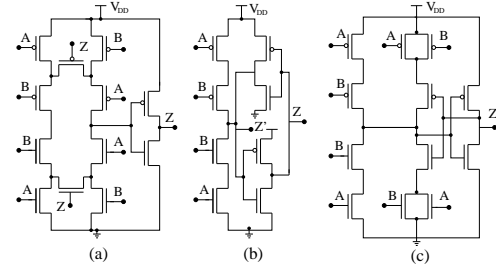

Fig. 2. Transistor Level Schematics of: (a) Van Berkel, (b) Weak-Feedback, (c) Conventional Muller C-elements

each wave [34], [35]. The speed of signal propagation is determined by the actual delays of the circuit.

The most interesting property of the circuit is that it is delay-insensitive, i.e., it works correctly regardless of wire and gate delays. Since many asynchronous designs are based on elastic pipelines, its behavior in the presence of radiation effects (SET generation, propagation and latching) is of utmost relevance. As we will see later on, beyond being an attractive target, elastic pipelines are also useful as measurement circuits.

IV. THE SPICE MODEL FOR SETS

A number of Spice models have been proposed in the literature over the years, which model radiation hits via current injection. Most proposed models agree in the qualitative definition, but differ in essential quantitative aspects [36]. Roche et al. [37] only considered peak currents, which is not realistic for the time-varying restoring current, and also overestimates the critical charge Q_{crit}. These issues have been addressed to some extent by Xu et.al [38], by defining Q_{crit} with respect to the static tripping point of an SRAM cell; it fails to consider the corporate dynamics of voltage transients at the struck node, however. Zhang et al. [39] estimated Q_{crit} in terms of transistor parameters and injected currents, characterized by magnitude and duration, but observed a discrepancy w.r.t. reality. One of the reasons is the use of a suitably matched rectangular current pulse, instead of an exponential one. Actually, the only current model known so far that agreeably mimics the actual charge deposition mechanism of a particle strike uses double exponential currents [40], so we adopt it for our analysis as well.

Our target circuit uses a current source connected to the source of the hit transistor for injecting a double exponential current pulse according to eq. (1) at the struck node [41].

$$I_P(t) = I_0(e^{-t/T_\alpha} - e^{-t/T_\beta}) \qquad (1)$$

Herein, I_P is the transient current pulse, I_0 is the peak current, T_α is the decay time of the current pulse, and T_β is the time constant for initially establishing the ion track. All our simulation experiments were conducted using HSPICE and Cadence Spectre simulators.

During the simulations, we kept the time parameters of the double exponential current source constant while varying I_0 to generate sufficiently strong, i.e., digitally visible, SETs. In order to get some basic understanding of the transformation of

an analog current spike in an inverter to a digital voltage pulse at the output, we plot the length of the SET observed at the buffered output against the peak amplitude of the exponential current pulse in Fig. 3. Notice that for 1 mA there is a digitally visible effect of the SET with the length of 210 ps, while for current peaks between 2 mA and 10 mA the length of the observed digital SET grows (approximately logarithmically) from 280 ps to 450 ps. It is important to note, however, that the simple relation in Fig. 3 does not continue to hold if the current pulse timing parameters T_α, T_β are varied.
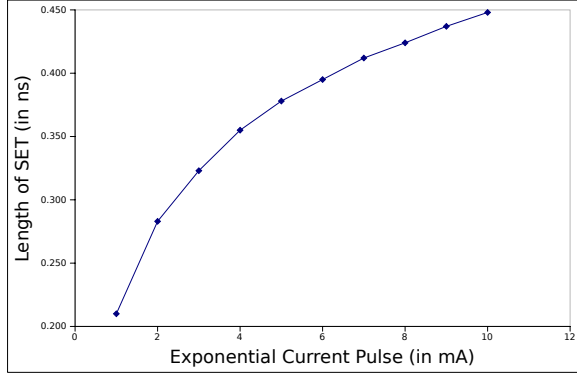

Fig. 3.   Length of SET vs. Exponential Current Pulse

To calibrate our Spice model with respect to the ASIC technology used for manufacturing the FRad Chip, we use the approach outlined in Section II. The Spice model parameters used in the analysis presented here have been estimated according to our measurement results, and will be fine-tuned based on the fully calibrated 3D model to faithfully model the SET generation process in the FRad Chip.

V. MEASUREMENT ARCHITECTURE

The measurement architecture of the FRad Chip must facilitate the continuous monitoring and recording of all occurring SETs, at the level of digital signals, in statistical long-term experiments. To get as much information as possible from an experiment, as many nodes in our target circuits (abbreviated DUT, for *device under test* in the sequel) as possible must be monitored simultaneously. At the same time, the number of monitored nodes is limited by the available die area and the number of pins of the FRad Chip.

On-chip preprocessing is used to reconcile these requirements: (i) We extract SET occurrences out of the possibly superposed dynamic operation of the DUTs as early as possible. (ii) Since we are not interested in the precise time of occurrence of SETs in statistical analysis, it suffices to just count the number of SETs in consecutive *measurement periods*, at the end of which the counts will be transferred to some off-chip data recording unit and be reset. (iii) To save pins, the data transfer will be performed serially after parallel/serial conversion (PISO). (iv) Since DUTs and on-chip preprocessing circuitry compete for the same die area, the latter must be as lean as possible.
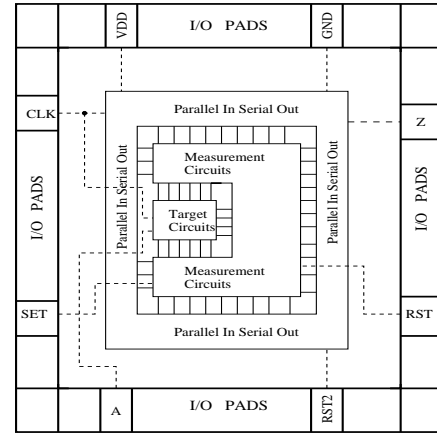

Fig. 4.   Structure of the Chip

Fig. 4 shows the structure of the resulting FRad Chip architecture. Notice the strict separation between target circuits, measurement circuits and PISO that may turn out helpful in specialized ion-beam experiments, in which radiation hits can be restricted to a certain area.

We want to investigate SET generation in our DUTs both in static and in dynamic mode. For the latter, we provide a common data signal that can be used to collectively stimulate switching activity. Recall that the XNOR tree has the beneficial property of exhibiting activity at its output only in case of a particle hit. Therefore, it is sufficient to use a simple incrementer for counting SETs here. Unfortunately, not all our other DUTs exhibit this nice behavior. Since the generation of the stimuli is under our control, however, we can easily provide a correct reference signal for comparison/subtraction purposes. This may be achieved by a simplified version of the DUT (even a simple wire or an inverter does the job, since all our DUTs except the XNOR tree exhibit a behavior equivalent to that of a wire or inverter) or by another instance of the same DUT. In principle, any mismatch between the DUT output and the reference signal can be extracted by an XOR, whose output feeds the SET counter, see Fig. 5.(a). The problem here is that the XOR tends to produce glitches in case of a non-zero skew between DUT and reference, thus potentially leading to spurious counts. Considering that we are not interested in the exact *temporal* matching of the behaviors of DUT and reference, but rather in matching their signal traces, a more appropriate solution is an up/down counter, with the DUT output feeding one input and the reference signal feeding the other one, see Fig. 5.(b). Obviously, we cannot use a synchronous up/down counter, since SETs would not adhere to setup/hold constraints and hence cause metastability. Moreover, in order to catch even short SETs, our counters should be as fast and sensitive as possible. Fortunately, there is a nice and area efficient way of building an asynchronous up/down counter for transitions that is based on an elastic pipeline. Fig. 8(c) illustrates its principle.

Alternatively, we may use an incrementer as well to count the transitions performed by the DUT during a measurement

period. However, in this case, we will see the sum of transitions due to the SETs in the DUT plus those due to the regular DUT switching activity. As the stimuli applied to the DUT are under our full control, we can subtract the latter a posteriori; the incrementer must accommodate a much larger count value, though.
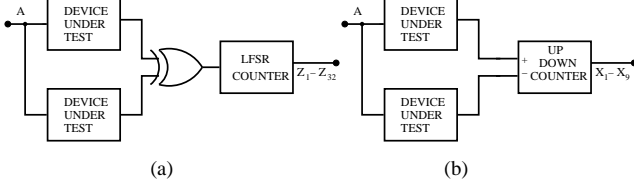

Fig. 5. Extracting SET occurrences from the observed activity by (a) XOR or (b) difference counter

Being on-chip, the measurement circuitry will be exposed to radiation just like the DUTs and hence has to operate properly in the presence of particle hits. There are many options available for making a circuit tolerant against these single, uncorrelated particle hits, such as TMR [42], coding [43], time redundancy [44], or radiation hardening [45]. However, all of those tend to cause high overheads (at least 200%), thus rendering a pretty large share of the die area unusable for additional DUTs. Considering that both proposed types of counters resemble interesting target structures by themselves (namely, a flip-flop chain as well as an elastic pipeline), we decided *not* to mask particle hits in these circuits but rather to let them occur: This effectively turns the on-chip measurement infrastructure into an additional radiation target. The remaining challenge is, however, to find a clever arrangement that allows us to distinguish between errors that occurred in the original target circuit and those in the counters. To this end, we use the following three strategies:

• For our SET counters, we employ a *Linear Feedback Shift Register* (LFSR) instead of a simple incrementer. The important benefit of doing so is that the counting sequence in a (carefully chosen) LFSR always involves multiple bit changes per count, hence a single bit flip caused by an SEU will lead to a dramatic change in the count sequence that is easily recognizable by an a posteriori analysis.

• To make sure that we have a correct copy of the count available even in case of a counter hit, we use duplication. Since, thanks to using an LFSR counter, we can identify the corrupted value, there is no need to go for triplication.

• For the difference counter, we cannot rely on recognizing erroneous counts. Duplication just allows us error detection but not recovery. A viable alternative is using an up/down counter in combination with an LFSR counter (which must be quite wide then, of course). This will not only allow recovery of the correct count, but will also provide diversity that might turn out very beneficial in a radiation environment.

Fig. 6 shows the finally chosen architectures. For the XNOR tree, we simply use two LFSR counters in parallel, as shown in 6.(a). Although we expect only few hits per DUT in a measurement period on average (see Sec. VII), we decided

to go for a 16-bit LFSR (for details see below) in order to retain a sufficiently long counting sequence; this makes the recognition of incorrect counts more reliable. By using two LFSR counters, we make sure that we have a correct count available in case one LFSR has been hit.
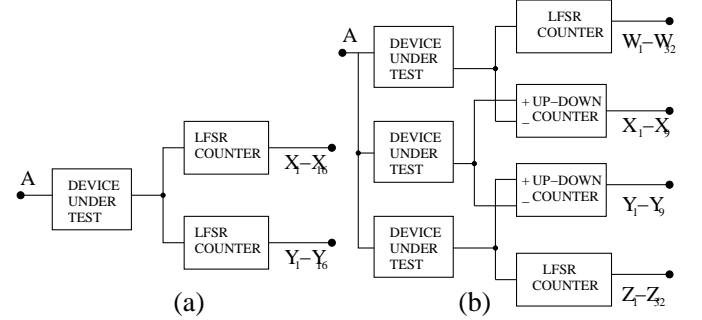

Fig. 6. Proposed Measurement Architectures for (a) XNOR tree; (b) all other target circuits

For all the other target circuits, we use the architecture shown in Fig. 6.(b). It comprises three DUTs of the same type, which we mutually use as a reference. For example, the behavior of DUT_2 is observed by the two Up/Down counters UDC_1 and UDC_2. Note that these counters have different references (DUT_1 and DUT_3, respectively) and use different polarity (UDC_1 counting down and UDC_2 counting up on output transitions of DUT_2). In principle, this architecture allows us to tolerate any of the two up/down counters becoming faulty. However, as we cannot be sure to safely recognize every SEU of an up/down counter, it may (in rare cases) happen that we end up with two counts indicating different numbers of SETs, which without additional information are both plausible.

For DUT_1, we use a different strategy: Its behavior is observed by both UDC_1 (counting up) and an LFSR counter. The benefit here is that, as motivated above, we can trust to recognize any faulty behavior of the latter. So in case the LFSR counter indicates a plausible number of SET occurrences in the target, we can simply trust it, while otherwise we still have the result of UDC_1 as a backup. Here we need a 32-bit LFSR for reasonably long measurement periods without wrap-around (42 seconds for a 100MHz input data stimulus), which we consider necessary for a safe recognition of counter hits. Finally, we use the same strategy for DUT_3.

Given the relatively low hit rate (according to Sec. VII, we will tune measurement period and radiation intensity to experience only a few hits per period), our general strategy in interpreting an observed scenario is to assume the lowest possible number of hits that could have led to the given observation. Considering, e.g., that UDC_1 counts up for failures in DUT_1 while it counts down for those in DUT_2, one might argue that SET observations may cancel out each other. This is, however, not the case, since we have redundant information in UDC_2 and the LFSR counter. With this combined information, it is possible to accurately identify every single hit, all double hits in both the target and the measurement circuits, and even many multiple hits correctly (for details

see Sec. VI-E). Backed up by the probabilistic calculations in Sec. VII, we are convinced that our architecture represents an excellent choice with respect to the combined criteria of area efficiency, fault tolerance, diagnosability and diversity. Overall, it clearly surpasses the more evident solutions using three LFSR counters or three up/down counters.

In the following we will present some details of our SET counter implementations.

A. Linear Feedback Shift Register (LFSR) based counters

An LFSR is a synchronous shift register with XOR gates forming selected feedbacks [46], which produces a deterministic and periodic pseudo-random counting sequence. It is heavily used in practice for generating CRC checksums and pseudo-random bit strings. Compared to conventional binary counters [47], an LFSR reduces the amount of required logic and minimizes routing complexity. With feedbacks forming a "maximum length polynomial", an LFSR with n flip-flops can implement a $2^n - 1$ state counter [46], [48]. Two circuit structures can be used to implement a given polynomial, namely, the many-to-one design and the one-to-many design.

We selected the 32-degree polynomial $x^{32} + x^{22} + x^2 + x + 1$ shown in Fig. 7 and the 16-degree polynomial $x^{16} + x^{14} + x^{13} + x^{11} + 1$ for our measurement architecture. We chose a one-to-many design based on XNOR gates for both, since the associated count sequence involves many bit changes per step, which is beneficial for detecting a single bit fault.
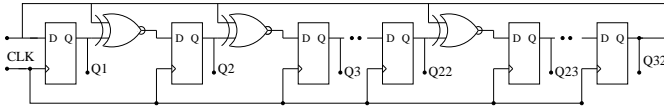

Fig. 7.   32-bit LFSR

B. Up-Down Counters

Our SET up/down counters will be implemented as 9-stage pipelines made up of Muller-C gates [49] with weak feedback inverters. Inputs A and B in Fig. 1.(E) are used as up and down count inputs, connected to the DUTs; the output Z is not used. In order to enable the possibility of counting down, we preset the pipeline to a value of 5 upon reset. For this purpose, we need to add extra transistors (with appropriate sizing) to the Muller-C gates as shown in Fig. 8.(a) and (b).

The up/down counter utilizing the two versions of the C-gates (with set and rst) and inverters is shown in Fig. 8.(c). The outputs $Z1 - Z5$ are preset to 1, while $Z6 - Z9$ are preset to 0; all bottom-row C-gates are initialized to 0. A transition on *UP* will add to the transitions already present in the pipeline, while a transition at *DOWN* will remove one transition from the pipe, thus decreasing the count.

VI. EVALUATION AND ANALYSIS

The goal of this section is to provide an overview and some results of our pre-fabrication analysis of the proposed measurement architecture of the FRad chip. Apart from area considerations, our primary concern is an evaluation of the resilience against particle hits.
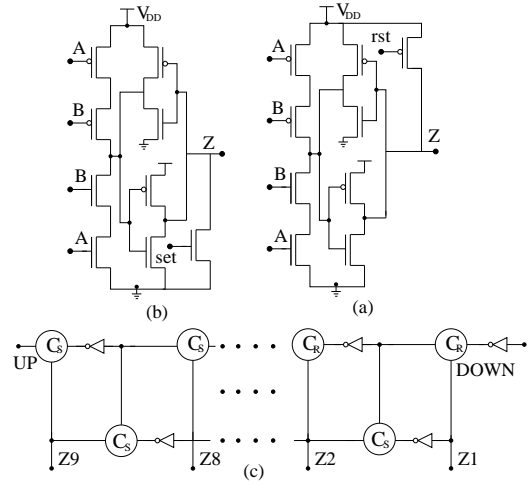

Fig. 8.   Schematic of (a) Muller-C gate with reset, (b) Muller-C gate with set and (c) Up/Down Counter

A. Overhead Analysis

Table I lists the total number of transistors required by the different target circuits described in Sec. III and the SET counters introduced in Sec. V.

TABLE I
NUMBER OF TRANSISTORS FOR DIFFERENT ARCHITECTURES

Architecture	Total No. of Transistors
17-Inverter Chain	34
33-Flip-Flop Chain	594
128-input NAND-NOR Tree	508
128-input XNOR Tree	1016
35 C-Gate Van-Berkel elastic pipeline	490
35 C-Gate Weak-Feedback elastic pipeline	350
35 C-Gate Conventional elastic pipeline	490
16-bit LFSR Counter	440
32-bit LFSR Counter	856
9-bit up/down Counter	187

The FRad Chip hosts three instances of each target circuit, two 32-bit LFSR counters and two up/down counters for every measurement setup. The exception to this is the XNOR tree target, one instance of which is monitored by two 16-bit LFSR counters. The resulting area consumption and the overhead incurred by the measurement circuits over the target circuits are given in Table II. Note that the only substantial overhead incurred by the measurement setup occurs for the inverter chains, which is due to the small size of the target. For the other target circuits, the measurement overhead is very reasonable. On average, the measurement circuitry consumes 19% more area (in fact fewer transistors) than the target circuits. Given that our SET counters can also be seen as additional target circuits in our architecture, the overhead is acceptable.

B. Fault-Tolerance Analysis Setup

The primary tool for the analysis of our measurement circuits' resilience against particle hits is simulation-based fault injection, using appropriate Spice models as described

TABLE II
HARDWARE OVERHEAD ANALYSIS FOR MEASUREMENT SETUP

Architecture	No. of Trans. for Target Circuits	No. of Trans. for Measurement Circuits	Overhead Factor (Target Circuit as base)
Inverter Chain	102	2086	20.451
Flip-Flop Chain	1782	2086	1.171
NAND-NOR Tree	1524	2086	1.369
XNOR Tree	3048	880	0.289
Elastic Pipeline	1330	2086	1.568
All	7786	9224	1.185

in Sec. IV. To get confidence in our architecture, we injected faults in each and every gate of each SET counter and analyzed the resulting behavior of the circuit.

We used release 5.10.41 of the Cadence Virtuoso Front-end to Back-end design environment to create the schematics of our circuits. They were all designed using UMC 90nm NMOS and PMOS device models. We chose custom W/L (width/length) ratios for the NMOS transistors, while the W/L ratios of the PMOS transistors were chosen based on the structure of the corresponding circuit. The Spice netlists were extracted from the respective Cadence schematics.

We performed all our analog simulations using HSPICE Version D-2010, using the following setup: To generate switching activity in the circuits, we toggled the data input every 5ns. After 10ns, we triggered the set and rst signals of the counters for about 40ns, which initializes the LFSR counter to 0 and the up/down counters to 5. At specifically selected times during normal operation, we triggered SETs by injecting a current pulse in the SPICE netlist (refer to Sec. IV).

C. LFSR Counter Evaluation

The regular operation of the 32-bit LFSR is illustrated in Table III: With each rising clock edge, the counting proceeds by one step; the 32-bit LFSR will step through a sequence of about 4.2 billion different values. A low at the RST input resets the count value to 0.

TABLE III
OPERATION OF THE LFSR COUNTER IN NO-FAULT SCENARIO

Time	LFSR Count	Actual Count
0-10ns	4194310	1
10-50ns	0	0
50-60ns	4194310	1
60-70ns	12582922	2
70-80ns	29360146	3
80-90ns	62914594	4

For our fault-tolerance analysis, we injected faults in each of the XNOR gates and flip-flops independently. Selected results are listed below (see also Table IV):

• Injection of an SET causing a bit flip from 1 to 0 in the XNOR gate tapped between Q_1 and Q_2 (please refer to Figure 7) at 75ns: Here the benefit of using an LFSR for counting becomes apparent. While only one bit of the output actually changes due to the SET, the related change in the counting sequence is drastic and hence easily recognizable: According to Table III the value following 29360146 should be 62914594,

but here it is 29360144, effectively causing a huge jump (see rightmost column).

• Injection of an SET causing a bit flip from 0 to 1 in the flip-flop with output Q_{15} at 80ns: This increased the LFSR count by 2^{15} and the actual count by 1.64 billion steps approximately. Again this is easy to detect.

TABLE IV
LFSR COUNTER – SETs IN XNOR GATES & FLIP-FLOPS

Time	LFSR Count	Actual Count
XNOR gate tapped between Q_1 and Q_2		
60-70ns	12582922	2
70-75ns	29360146	3
75-80ns	29360144	**2325803548**
80-90ns	62914598	**2325803549**
Flip-Flop with output Q_{15}		
60-70ns	12582922	2
70-80ns	29360146	3
80-90ns	62**947362**	**1647004572**
90-100ns	130**089026**	**1647004573**

Overall, this confirms that a single bit flip in the LFSR counter is witnessed as billions of skipped transitions. Due to our careful selection of the LFSR polynomial, its one-to-many implementation (see Sec. III), and backed up by numerous further experiments, we can indeed generalize this observation: A single bit flip in any LFSR cell will always infer a much larger and hence easily detectable effect in the actual count, which finally justifies our decision to use an LFSR counter.

D. Up/Down Counter Evaluation

In our analysis, SETs were injected into all C-gates and inverters to evaluate the resulting behavior of the up/down counter introduced in Sec. V. Table V lists some of the scenarios obtained (e.g. at 75ns and 105ns). Recall that the up/down counters are initialized to a count of 5, represented by 111110000 on $Z_9 \ldots Z_1$ in Fig. 8.(c). A fault injected at 130 ns in the C-gate that drives the output Z_8, e.g., changed the outputs Z_6, Z_7 and Z_8 to 1. There were also many instances when the fault injected at the same node in a different time interval just changed the output Z_8 temporarily to 1 (for one step) and switched back to 0.

Overall, we observe that the effect of an SET in an up/down counter is dependent on the location and the direction of the resulting bit flip. Unlike in the LFSR case, the initial effect of the fault is not "amplified", such that a particle hit in the up/down counter cannot easily be distinguished from a regular counting step caused by an SET in the associated target. This confirms that some kind of replication is indeed mandatory for using these counters in our measurement architecture.

E. Overall Measurement Architecture & Fault Dictionary

We have created a comprehensive fault dictionary for our measurement architecture, which associates every fault scenario (single or multiple SET hit(s) in counters and targets) with its "syndrome", i.e. the set (U_1, U_2, L_1, L_2) of resulting readouts on the up/down counters UDC$_1$ and UDC$_2$, as well as the LFSRs 1 and 2. Used in the reverse direction, this dictionary allows us to infer from an observed syndrome the

Time	Up/Down Count	Actual Count
Muller-C gate (with set) between the outputs Z_4 and Z_5		
65-70ns	111110000	5
70-75ns	000001111	5
75-80ns	111**1**00000	**4**
80-85ns	000**1**1111	**4**
Muller-C gate (with rst) at output Z_5		
95-100ns	111110000	5
100-105ns	000001111	5
105-110ns	111**1**00000	**4**
110-115ns	000**1**1111	**4**
Muller-C gate (with set) at output Z_8		
120-125ns	111110000	5
125-130ns	000001111	5
130-135ns	000000**001**	**8**
135-140ns	11111**1110**	**8**

Observed Syndrome				Location of Faults	
U_1	U_2	L_1	L_2	Actual Location	Interpretation
No Fault Scenario					
5	5	√	√	− − −	− − −
Single Fault Scenario					
6	5	+	√	D_1	D_1
4	6	√	√	D_2	D_2
5	4	√	+	D_3	D_3
*	5	√	√	U_1	U_1
5	*	√	√	U_2	U_2
5	5	X	√	L_1	L_1
5	5	√	X	L_2	L_2
Double Faults Scenario					
location of all faults traceable					
Problematic Triple Fault Scenarios					
*	5	X	√	(U_1 , L_1 , D_1)	(U_1 , L_1)
*	*	√	√	(U_1 , U_2 , D_2)	(U_1 , U_2)
5	*	√	X	(U_2 , L_2 , D_3)	(U_2 , L_2)
Problematic Quadruple Fault Scenarios					
*	*	+	√	(D_1 , D_2 , U_2 , U_1)	(D_1 , U_2 , U_1)
6	*	+	X	(D_1 , D_3 , U_2 , L_2)	(D_1 , U_2 , L_2)
*	*	X	√	(D_1 , U_1 , U_2 , L_1)	(U_1 , U_2 , L_1)
*	6	X	√	(D_1 , D_2 , U_1 , L_1)	(U_1 , D_2 , L_1)
5	*	X	√	(D_1 , D_2 , U_2 , L_2)	(D_1 , U_2 , L_2)
*	5	X	X	(D_1 , U_1 , L_1 , L_2)	(U_1 , L_1 , L_2)
*	*	√	+	(D_2 , D_3 , U_1 , U_2)	(D_3 , U_2 , U_1)
*	5	√	X	(D_2 , D_3 , U_1 , L_2)	(L_2 , U_1)
4	*	√	X	(D_2 , D_3 , U_2 , L_2)	(D_2 , U_2 , L_2)
*	*	X	√	(D_2 , U_1 , U_2 , L_1)	(U_1 , U_2 , L_1)
*	*	√	X	(D_2 , U_1 , U_2 , L_2)	(U_1 , U_2 , L_2)
*	*	√	X	(D_3 , U_1 , U_2 , L_2)	(U_1 , U_2 , L_2)
5	*	X	X	(D_3 , U_2 , L_1 , L_2)	(U_2 , L_1 , L_2)

fault scenario that caused it, with, e.g., (U_1, L_2, D_2) indicating that UDC$_1$, LFSR$_2$ and DUT$_2$ have been affected by an SET. This mapping, unfortunately, is not bijective, as different multiple-fault scenarios may map to the same syndrome. We use two strategies to handle this issue: (1) By carefully choosing the measurement period (see Sec. VII), we can safely neglect the probability of experiencing many SET hits within one period (i.e., before reading out and re-initializing the counters). This allows us to ignore fault scenarios involving more than, e.g., 4 SETs in our dictionary. The same reasoning supports our strategy (2), namely, associating an observed syndrome with the scenario that involves the lowest number of faults, as it is far more probable to occur than other matching scenarios that might exist. Of course, however, this can lead to misinterpretation in rare cases[2].

Table VI shows an excerpt of our fault dictionary. Herein "*" and "X" both indicate an incorrect counter value, with the latter being recognizable as an error and the former not. "√" indicates that the expected LFSR value for the fault free case is read, "+" stands for a correctly incremented LFSR value.

It turns out that our architecture facilitates correct identification of the hit circuit for all single faults. The same is true for double faults (not shown for brevity). Furthermore, most of the triple faults and even quadruple faults are correctly identified; the few problematic cases that lead to a wrong interpretation are shown in the table. In the case when all four counters are hit, we do not have any useful information left, of course.

Our fault dictionary has been validated by means of numerous simulated SET injections (up to seven at a time) into various locations. We are hence convinced that the chosen measurement architecture will indeed work as expected.

VII. PROBABILISTIC ANALYSIS

Given the non-negligible number of transistors I_M of the measurement circuitry M as compared to the number of transistors I_T of the target circuitry T in Table II in Sec. VI on one hand, and the ability of M to tolerate just a double hit for sure[3]

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[2]This can be resolved on a statistical basis, which is one of our future aims.
[3]Given that M can also tolerate many triple and even higher-order faults, this is a very conservative assumption.

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on the other hand, the question about feasible measurement periods $\Delta = \Delta(\phi)$ for a given particle flux ϕ (in particles per $\mu m^2 \cdot s$) arises: Δ must be chosen small enough such that, with reasonably high probability, there are at most two hits in M during Δ; we call such a measurement period *safe*. At the same time, with reasonably high probability, two consecutive hits in T should occur within some P safe measurement periods sufficiently often, in order to get statistically meaningful data on the SET generation process.

A gross estimate of Δ and P can be determined using cross section data. Although such an estimate necessarily ignores the fact that target and measurement circuitry have very different structure and topology, it provides meaningful results due to the fact that we do not rely on single-event-upset (SEU) cross sections but rather on SET cross sections: Whereas it is known that memory elements like flip-flops are more susceptible to radiation than combinational logic, this is primarily a consequence of the fact that SETs in combinational logic are relatively unlikely to be latched. Consequently, they do not as easily lead to an SEU as SETs resulting from a direct hit of a flip-flop. By contrast, the SET generation process is the same both in combinational logic and in flip-flops.

Our radiation experiments for validating the 3D model provided a (saturated) SET cross section γ of about $\gamma = 5$ μm^2 for our 90 nm ASIC technology, which matches the figures given in the literature [50]. Recall that the cross section

expresses that a total fluence of 1 particle per γ results in 1 SET per device of interest (in our case, per transistor) on average. Trivial calculations based on expected values reveal that if we choose $\phi\Delta = \frac{1}{\gamma I_M}$, we get one hit in M during Δ on average. Since Δ should be chosen large enough to fully exploit M's double-hit resilience, but should only rarely lead to triple hits, we choose

$$\Delta = \frac{C}{\gamma\phi I_M},$$

for some constant $0 < C \leq 2$, which leads to $E[H_M] = C$ hits in M on average. For arbitrary distributions of the number of hits H_M in a single measurement period in M, Markov's inequality $P\{H_M \geq h\} \leq E[H_M]/h$ reveals a triple-hit probability of $p = P\{H_M \geq 3\} \leq C/3$; it can be made sufficiently small by choosing C sufficiently small. As this results in a geometric distribution of safe measurement periods, we can expect an average of $P_M = 1/p \geq 3/C$ consecutive safe measurement periods.

On the other hand, the average number of hits in T during Δ is CI_T/I_M, so we can expect one hit on average in T after

$$P = \frac{I_M}{CI_T} \quad (2)$$

measurement periods; note that they eat up a total time of $P\Delta = \frac{1}{\gamma\phi I_T}$.

To see a hit in T before the measurement is affected by a triple hit in M on average, we should have something like $P \leq P_M$, which is guaranteed if $\frac{I_M}{I_T} \leq 3$. This is a very conservative estimate, however. To obtain the actual probability of failure P_{fail}, i.e., of an unsafe measurement period within two consecutive target hits, we will assume that the number of hits in M and T follow a compound Poisson distribution with the same average hit rate per $\mu m \cdot s$. This implies a rate $\lambda_M = C$ per measurement period in M, and $\lambda_T = CI_T/I_M$ in T.

Recalling the geometric distribution of safe measurement periods with parameter p and the fact that the probability of no target hit within k measurement periods is $e^{-\lambda_T k} = e^{-C_T k}$, where we used the abbreviation $C_T = CI_T/I_M$, we find

$$P_{fail} = \sum_{k\geq 0} p(1-p)^k e^{-C_T k} = \frac{p}{1-\frac{1-p}{e^{C_T}}} = \frac{pe^{C_T}}{e^{C_T}-1+p}.$$

Since the Poisson distribution of H_M implies $p = P\{H_M \geq 3\} = 1 - (1 + C + C^2/2)e^{-C} = 1 - (1+C')e^{-C}$ with $C' = C + C^2/2$, we thus easily obtain

$$P_{fail} = \frac{\left(1-(1+C')e^{-C}\right)e^{C_T}}{e^{C_T}-(1+C')e^{-C}} = \frac{1-(1+C')e^{-C}}{1-(1+C')e^{-C-C_T}}$$

$$= \frac{1-(1+C+\frac{C^2}{2})e^{-C}}{1-(1+C+\frac{C^2}{2})e^{-C(\frac{I_M+I_T}{I_M})}} \quad (3)$$

Expression (3) for P_{fail} can be made as small as desired by choosing $C \in (0,2]$ sufficiently small, for all reasonable ratios I_T/I_M. For example, for $I_T = I_M/2$, which is more than reasonable for all target circuits except for the inverter chain

according to Table II, we obtain $P_{fail} < 0.01$ for $C = 0.2$. For the inverter chain, Table II reveals $I_T = I_M/20$, which yields $P_{fail} < 0.1$ for $C = 0.2$. Note that, according to (2), $C = 0.2$ leads to $P = 5$ measurement periods between two target hits on average. Given the quite conservative assumptions underlying our probabilistic analysis, we can hence finally conclude that our measurement architecture is indeed excellently suited for collecting statistically meaningful long-term data.

VIII. Conclusions

We presented our choice of target circuits and on-chip measurement architecture for capturing single-event transients in VLSI circuits in long-term physical radiation experiments. Key challenges are (i) distinguishing SETs from normal switching activity of the target circuits, (ii) providing reliable SET data acquisition in spite of radiation hits in the measurement infrastructure, and (iii) leaving as much of the die area available for the target circuits as possible. Rather than employing a rad-hard design, our architecture considers the measurement circuitry as additional target circuits, and hence allows to tolerate hits in the former by an architectural design that supports reliable fault detection based on a fault dictionary. Both elaborate fault-injection experiments based on detailed Spice models and some probabilistic analysis have been used for a comprehensive design validation, which is *the* major step along the road towards the final FRad ASIC.

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