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Invited Paper

Reliability challenges of automotive power electronics

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ABSTRACT

A high reliability of power electronic modules is an essential requirement for hybrid traction applications. This includes a high capability to withstand the stress of repeated active and passive thermal cycles in order to meet the lifetime requirements. Active power cycling requirements are not especially severe for hybrid traction applications compared to many industrial applications. The lifetime for passive thermal cycles by a change of ambient conditions in contrast is defined by the materials and the architecture of a power module. The classical module design with Cu base plates is limited in lifetime particularly with respect to passive temperature cycles due to CTE mismatch. The advanced pressure contact design eliminates the base plate together with the base plate solder and the terminal solder interconnections and thus enhances the thermal cycling capability. As a synergy effect, this design establishes a very balanced static and transient current distribution for paralleled chips. Finally, the last remaining solder interface – the chip solder layer – can be replaced by an Ag diffusion sinter technology. The presented cycling test results will confirm, that the first 100% solder-free module shows an improved performance in passive and active cycling tests.

1. Introduction

The capability to withstand the considerable stress induced by thermal cycles is a prerequisite for high reliability and lifetime of power modules in every application. These thermal cycles are caused by active power cycles on the one hand, when thermal losses are generated inside the power chips by conducting high currents or by switching the current on and off. On the other hand, passive thermal cycles are occurring due to changes in environmental temperature, which could result from either changes in the ambient temperature or from temperature excursions of the system environment like the change of heat sink temperature or of the cooling liquid.

Both types of cycles are different in some aspects. First, considerable temperature gradients are present in a power module during active power cycles with the maximum temperature in the center of the active devices and the minimum temperature in the heat sink. During passive temperature cycles in contrast, all layer are required to reach the corner temperatures defined by the test conditions, so that no temperature gradients at all are remaining. Therefore, the latter test condition generates considerably more stress in a classical module design in which the active devices exhibit the smallest coefficient of thermal expansion (CTE) and the base plate show much larger CTE values.

Secondly, the lifetime during active power cycling can be controlled by the implemented device area, so that principally any lifetime requirement can be met by incorporation of sufficient active silicon area, when cost and footprint size are disregarded. However, this is not possible for increasing the lifetime in passive temperature cycling, because the stress between layers rigidly joined (by a solder interface for example) is defined by the difference in CTE values. Therefore, the selected materials und the reliability of the interconnect layers constitute the module lifetime, which can only be improved by progressive module architectures and advanced interconnection technologies.

While both active and passive thermal cycles are limiting the lifetime of power modules in many applications, hybrid automotive traction systems represent a unique challenge for the module reliability because the requirement to endure passive thermal cycles is much higher than in conventional industrial applications.

Table 1 gives a typical overview of lifetime requirements for power applications in hybrid electric vehicles (HEV). While the engine on time results in quite moderate requirements with respect to active power cycles (12,000 h are equivalent to 500 days of continuous 24 h operation), the on/off cycles are a challenge to power electronic systems. Especially when the combustion engine liquid cooling system is used for the cooling of power electronic systems, considerable passive temperature cycles must be expected.

As emphasized before, the only way to enhance the passive cycling capability of power electronic systems is to review the system architecture and the interconnection technologies

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Table 1
Typical lifetime requirements for automotive applications [1].

Service life time	15 years (=131.400 h)	
Mileage	600.000 km	High level high mileage request for stand alone EEM (not for mechatronics)
Engine on time	12.000 h	Engine on time is directly proportional to mileage. Operating time of single component may be different than engine on time
Engine on/ off cycles	54.000	Without additional start/stop functions

implemented and to eliminate the weak links in the chain. This process shall be discussed in the following sections.

2. Limits of classical module design

The classical module design implements solid copper base plates as assembly platform for the insulating ceramic substrates, which are assembled on the base plate by solder technology. These base plates provide the thermal contact to the cooling heat sink.

The base plate is pressed to the heat sink only by a limited number of mounting bolts, which are conventionally positioned at the corner and/or along the edges of the base plate. In order to achieve an interface layer with a low thermal resistance, special shaping techniques are applied. Closer investigations have shown, that it is difficult to produce an ideal shape of the base plate, even more so because the stress incorporated in the solder layer between the base plate and the substrates leads to a creep in the visco-plastic solder interface, which changes the amplitude and shape of the base plate curvature during the shelf storage of the module [2]. This makes is very difficult to design a perfect base plate for large footprint power modules.

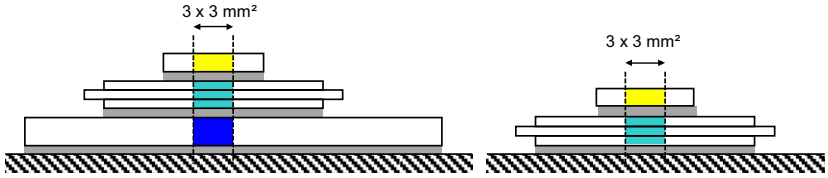
This perception was one of the major driving factors for the introduction of module architectures without base plate. A simulation illustrates the consequence on the stress induced in a module with and without a base plate. A three-dimensional thermal model was calculated for an IGBT sized 13.6 × 13.6 mm^2 for a dissipated power of 270 W [3]. Assuming a homogeneous temperature in a center column of 3 × 3 mm^2, the temperature rise of the layers relative to the heat sink temperature was calculated for a system with and without base plate and the lateral thermal expansion for this column was calculated with the CTE values in both systems.

Fig. 1 shows the simulated temperatures and layer elongations inside the center column. The junction temperature of the base plate module is lower than the junction temperature of the system without base plate. This effect is caused by the missing thermal spreading of the 3 mm thick Cu base plate and the difference in ceramic thickness used for this comparison. But the difference in thermal expansion is lower in the system without base plate, because the substrate with the higher CTE has a lower temperature (because it is closer to the heat sink) and the silicon chip with the low CTE has a higher temperature. Therefore, the stress induced in the solder layer between chip and substrate is reduced, even though a higher junction temperature is observed.

This comparison shows that the value of the absolute junction temperature is not sufficient to evaluate the reliability of different system designs. For stress conditions, where solder fatigue is the dominating failure mechanism, the system without base plate will have a higher lifetime because of the reduced stress, even though the maximum junction temperature is higher.

But the module design without base plate shows its real advantage, when ceramic materials other than Al_2O_3 are implemented. Fig. 2 shows a simulation comparison of two base plate designs with the architecture without base plate for AlN substrates. The same geometry and power dissipation as in Fig. 1 was applied. The higher thermal conductivity of AlN yields lower junction temperatures for all models. The base plate module with a Cu base plate shows an extreme thermal mismatch between the substrate and the base plate, resulting in reduced lifetime of this construction.

By replacing Cu with AlSiC as base plate material this mismatch can be reduced [4] at the cost of a higher junction temperature due to the smaller thermal conductivity of AlSiC. The design without base plate yields the lowest junction temperature and the smallest mismatch between the chip and the substrate and is therefore the superior solution. This was confirmed by end-of-life power cycling tests [5].



System:	standard 34mm module 0,38mm-Al2O3 / Cu base plate			SKiiP pressure system 0,63mm-Al2O3		
Results:	T-Ts [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Ts [K]	ΔL/L [1E-6/K]	ΔL [µm]
silicon	69,7	4,1	0,86	72,6	4,1	0,89
substrate	55,4	8,3	1,38	52,7	7,8	1,23
base plate	40,5	17,5	2,13	—	—	—

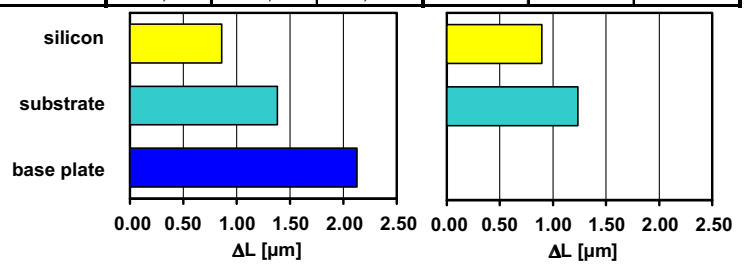
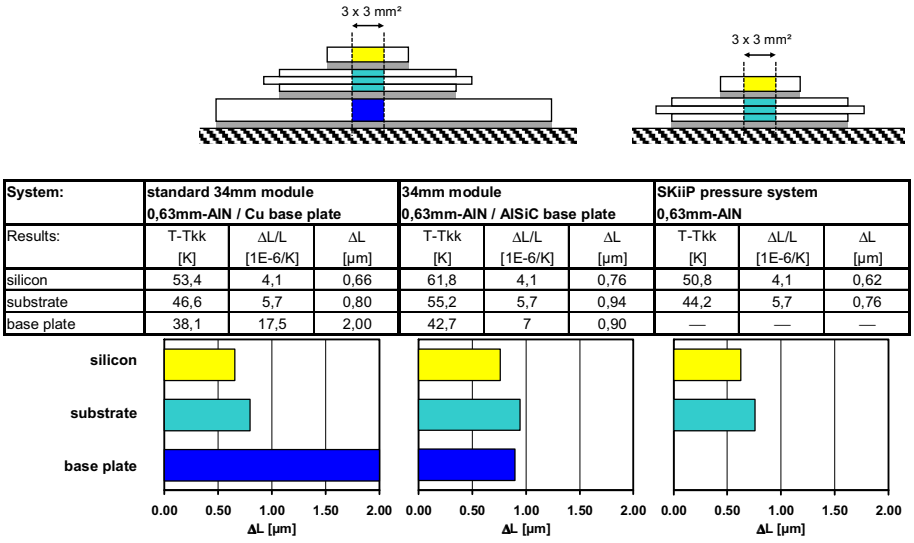


Fig. 1. Three-dimensional thermal simulation of a base plate module and a module without base plate using Al_2O_3 substrates [3].



System:	standard 34mm module 0,63mm-AlN / Cu base plate			34mm module 0,63mm-AlN / AlSiC base plate			SKiiP pressure system 0,63mm-AlN		
Results:	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]	T-Tkk [K]	ΔL/L [1E-6/K]	ΔL [µm]
silicon	53,4	4,1	0,66	61,8	4,1	0,76	50,8	4,1	0,62
substrate	46,6	5,7	0,80	55,2	5,7	0,94	44,2	5,7	0,76
base plate	38,1	17,5	2,00	42,7	7	0,90	—	—	—

Fig. 2. Thermal simulation of a base plate module with different base plate materials and a module without base plate using AlN substrates [3].

However, the design without base plate has a penalty for the application: the thermal capacity of the base plate is not available anymore. The thermal impedance for the three systems simulated in Fig. 2 is displayed in Fig. 3.

The comparison of the single pulse thermal impedance of the three different AlN systems discussed in Fig. 2 illustrates, that in the pulse length interval between 50 ms and 500 ms, the thermal impedance of the non base plate system is higher than the thermal impedance of the AlSiC base plate design. Form this single pulse behavior some engineers have derived a general weakness of designs without base plate for every application [6]. But a more detailed investigation shows that this argument is only true for a very limited group of applications with a small duty cycle.

The elimination of the base plate has also eliminated its thermal capacity. For single pulses or very small duty cycles, this has a disadvantageous impact on the thermal impedance. But this is only relevant, if the base plate has the time to transfer the heat stored in it to the heat sink before the next pulse arrives.

But when a duty cycle of 50% is assumed – as is the case for IGBTs in a three phase inverter for a motor drive application – the time for dissipating the heat to the heat sink is too short, so that the storage capacity of the base plate affects the thermal impedance only marginally. The dashed curves for the 50% duty cycle in Fig. 3 illustrate, that the AlSiC base plate design shows higher thermal impedance than the architecture without a base plate for the whole time scale.

3. The pressure contact technology

The elimination of the base plate allows a new module architecture called pressure contact system design. This technology is established for years in many power electronic applications; it was first introduced in the Semikron SKiiP® system. Any desired ceramic substrate can be implemented in this system, because the lack of rigid interconnection eliminates the need for CTE adaptation. So Al_2O_3 or AlN substrates can be used for the package without any adaptation of the module architecture [7]. Additionally, the substrate size is no more restricted to maximum limits and large area substrates can be implemented and make numerous interconnections between individual small substrates obsolete.

Fig. 4 shows a cross sectional view of the SKiiP® pressure contact system. A non-conductive bridge element transfers the force from the pressure system, consisting of a rigid pressure plate and a pressure foam layer, to the substrate. The pressure system also presses the load contacts to the substrate. It thus establishes the thermal contact and electrical contacts at the same time.

When this first pressure contact system design was developed, an important synergy effect was not anticipated: it is advantageous to replace the bridge element by a multi contact bus bar structure for the load contacts as shown in Fig. 5. In this design, mechanical pressure to assure a good thermal contact of the substrate to the heat sink is transferred by multiple load current connectors of the internal bus bar system. This concept exhibits fundamental

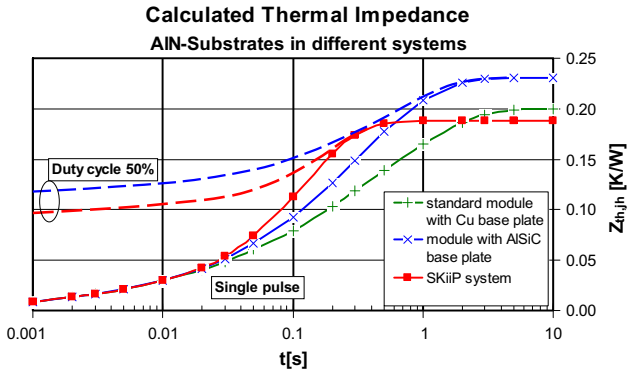


Fig. 3. Thermal impedance for the simulated model in Fig. 2, the dashed lines represent the thermal impedance for a duty cycle of 50%.

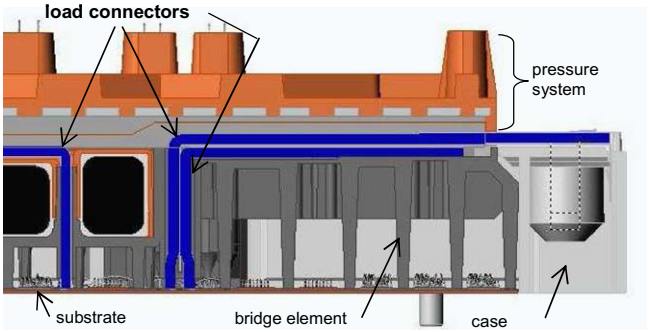


Fig. 4. Design of the pressure contact system in the SKiiP® architecture. The cross section shows the bridge element, the pressure system and the load contacts on the power substrate.

advantages for the static and dynamic current sharing in paralleled chips.

First, a simulation of current sharing in a SKiM®63 module will illustrate the advantage for the static current sharing. Fig. 6 shows the current flow for the considered example. The current is fed in through the +DC connector of the first phase leg. The current branches through the parallel connected TOP IGBTs and is collected by the AC trace. From here it flows to the external AC terminal which is connected by a bridge with the AC terminal of a second phase leg. From there the current branches through the BOT IGBTs of the second phase leg and is collected by the minus trace and conducted to the −DC terminal.

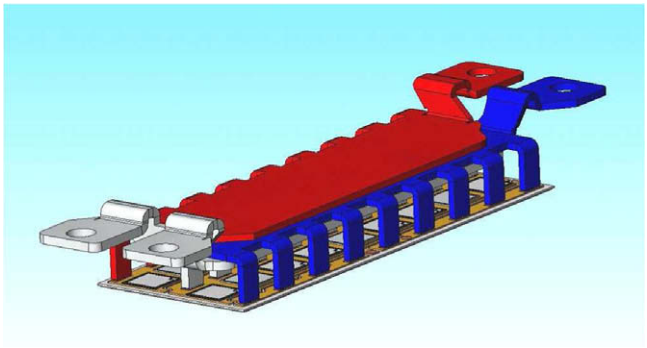


Fig. 5. Improved pressure contact system with multiple load contacts in a bus bar structure. The drawing shows the plus contacts (red), the minus contact (blue) and the AC-contact (grey) of a SKiM®93 phase leg, establishing both mechanical (thermal) contact and current contacts. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

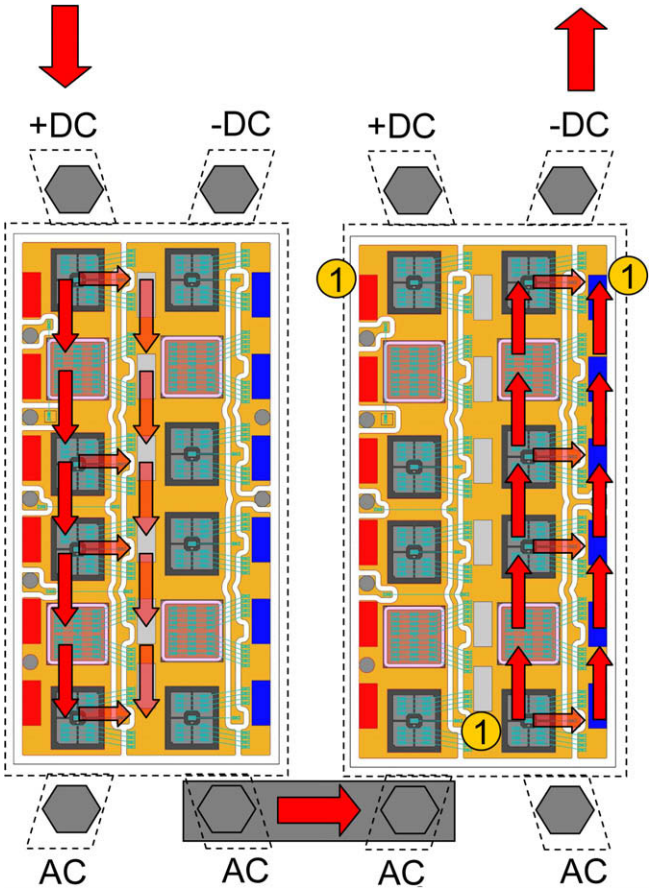


Fig. 6. Two phase legs of the SKiM®63 module with the current flow used for the simulation of the static current distribution. The circled 1 indicates the contact for the reference simulation.

In order to simulate the current distribution between the parallel chips, the path resistance on the DBC substrate as well as the path resistance of the bus bar structure was calculated from the geometry and the specific resistance of copper. The chips were assumed identical and their forward characteristic was approximated by a linear relationship between current and voltage drop, which describes the current voltage characteristic close to the nominal current sufficiently well. The resistance of the wire bonds was also calculated form their geometry and material parameters. Then, the so derived electrical equivalent network was calculated with PSPICE.

Fig. 7 displays the results for the SKiM®63 module with four chips per switch in parallel. The current deviates from the nominal 100 A per switch less than 0.3 A and thus shows an imbalance of approximately 0.3%.

To evaluate this result, a modified system was analyzed with the same simulation strategy. In contrast to the realistic bus bar contact system with multiple contacts, only a single contact spot on the DBC substrate was assumed (i.e. the first contact relative to the terminal of the original bus bar system). The positions are indicated by the circled 1 in Fig. 6. For the +DC and −DC connectors the position of the single contact was on the top side of the substrate, for the AC connector the contact was located at the bottom side of the substrate. Thus, each contact position was close to the related load terminal, which is a realistic assumption for conventional packages. The current distribution for this hypothetical system is also shown in Fig. 7.

The current imbalance in this case amounts to 9%. The imbalance is especially pronounced for the BOT switch, reflecting the fact, that the minus trace on the DBC substrate is typically much smaller than the plus or AC trace, because no chips are placed on this trace. The comparison shows, that the bus bar concept with multiple load contacts substantially improves the static current sharing in power modules with several parallel chips. An evenly balanced current sharing distributes the stress in application evenly between the chips and thus increases the reliability of the package, which is always determined by the weakest link of the chain.

Additionally to the static current sharing, the dynamic current distribution during switching is of great interest for a power module package. Measurements performed on a SKiM®63 phase leg have confirmed that the variation of parasitic inductance amounts to less than 1 nH between the paralleled chips [8].

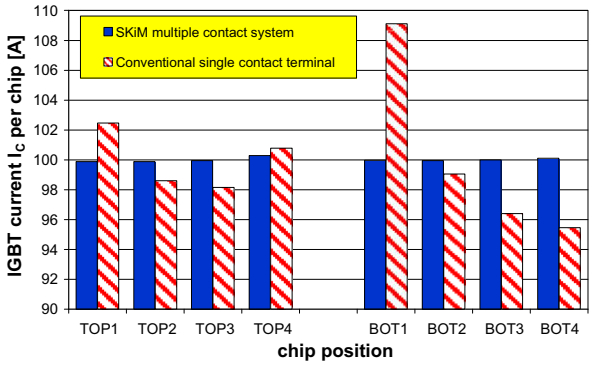


Fig. 7. Comparison of the current distribution in a SKiM®63 module with multiple contact points to a system, where the current is only distributed by a single contact point as marked in Fig. 6.

This experimental result corroborates the statement of very homogeneous current distribution derived from simulation and illustrates the considerable improvement that the pressure system design in combination with an internal bus bar structure with multiple contacts exhibits in comparison to traditional power module designs.

4. Sinter technology

With the replacement of the soldered base plate by a pressure contact technology, the limited reliability during passive thermal cycles is improved. Even if theoretically, any lifetime requirement during active thermal cycles can be achieved by implementing sufficient chip area, this is no possible solution for hybrid cars. The constrictions in space and weight available for the power electronic components require the highest possible package density. Additionally, the intention to use the combustion engine cooling system for the cooling of the power electronic components increases the requirements for the reliability during active power cycles. Maximum cooling liquid temperatures of 110 °C demand to utilize the power chips to the maximum of the operation temperature range, limited only by the maximum junction temperature of 175 °C. Under these boundary conditions, the reliability during active power cycles must be as high as possible for hybrid traction applications.

Therefore, the last remaining solder interface between the chip and the substrate was replaced by a superior interconnection technology: the silver diffusion sinter technique. This technology was originally developed to join large area round SCRs with molybdenum discs. In the middle of the 90s, first attempts were made to adapt the process to the interconnection of modern small size IGBT and diode chips to ceramic substrates [9].

Today, Semikron has developed a process for the silver sinter technology compatible with the requirements of power module series production. The process allows joining a variety of different chips on a substrate in a single process step as shown in Fig. 8. On a 5 in. by 7 in. master card, 48 IGBTs, 48 small gate resistor chips and 24 freewheeling diodes (FWD) are connected via silver diffusion technique in this example. Thus, four phase leg substrates are assembled in a single process step.

For the sinter process, a paste is applied to the substrate. This paste consists of silver flakes embedded in a semi-fluid matrix. The silver flakes are coated with an organic protective cover to prevent an agglomeration before the process start. The chips are then placed into the paste, comparable to a solder paste process.

Then the assembled substrate master card is pressurized with a hydrostatic pressure in the range of 40 MPa while at the same time, the temperature is increased to 200–250 °C. The protective coating of the silver flakes is dissolved by the elevated temperature and assisted by the pressure the particles are densified and diffuse together to form a porous interconnection layer. Noble metal surfaces on both partners are required for the formation of an interconnection.

The silver diffusion sinter technology has numerous advantages compared to the classical solder interface. First of all, no transition to a fluid phase occurs in the interface layer. During such a liquid phase as encountered in every solder process, the chip floats on a liquid layer and can move or turn out of the desired position. The absence of a liquid phase transition in the sinter process prevents such a shifting of chips and allows to exactly position the chips at the desired location. Additionally, no voids can form in a silver sinter layer, only a homogeneous porosity is formed in the interface.

Furthermore, all material parameters of the silver diffusion interface – which have been extensively studied [10] – are superior to conventional solder interfaces as illustrated in Table 2.

The thermal conductivity is more than a factor of three better than that of a tin–silver solder interface. This improves the transfer of heat together with the reduced layer thickness. The electrical conductivity is enhanced as well. The mechanical characteristics as CTE and tensile strength are favorable for the implementation in power electronic packages.

However, the most important feature of the silver sintering interface is the high melting point of the silver layer. This aspect can best be illustrated by the concept of homologous temperature, which is well known to mechanical engineers. The stability of a material under mechanical stress can be evaluated by comparing the ratio of operational temperature to the melting point temperature on the absolute temperature scale. Fig. 9 shows this ratio for the silver sinter layer in comparison for two solder materials, the widely known SnAg(3) solder and a high melting AuGe(3) solder with a liquidus temperature of 363 °C. Assuming an operation temperature of 150 °C for all three systems, the two solder systems

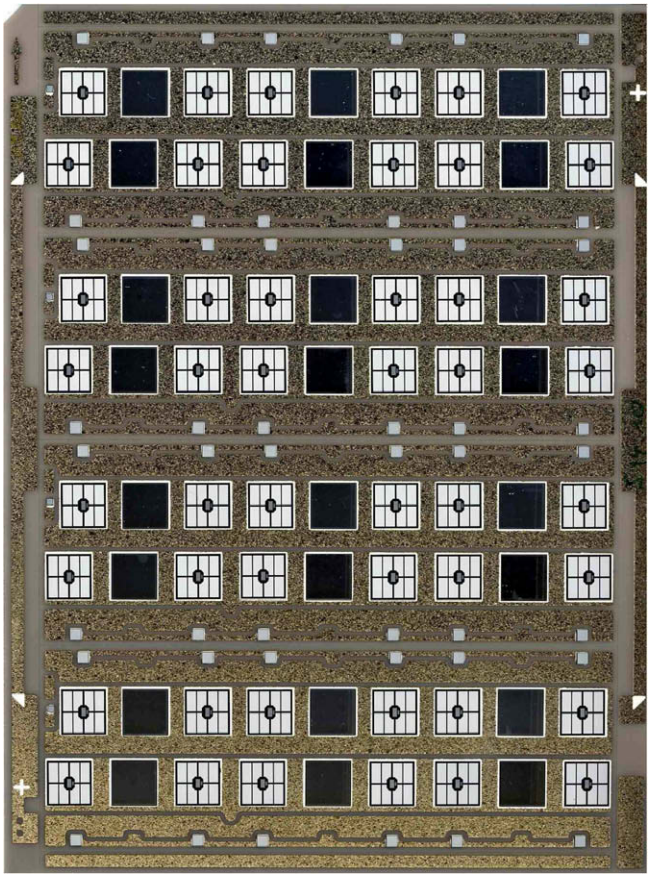


Fig. 8. Ceramic substrate 5 in. × 7 in. master card after the diffusion sinter process – 120 chips are assembled in a single process step.

Table 2
Material parameters for the silver diffusion sinter layer in comparison to a standard solder interface.

Properties	Unit	Solder layer SnAg(3)	Ag diffusion sinter layer
Melting temperature	°C	221	962
Thermal conductivity	W/m/K	70	240
Electrical conductivity	MS/m	8	41
Layer thickness	μm	~90	~20
CTE	ppm/K	28	19
Tensile strength	MPa	30	55

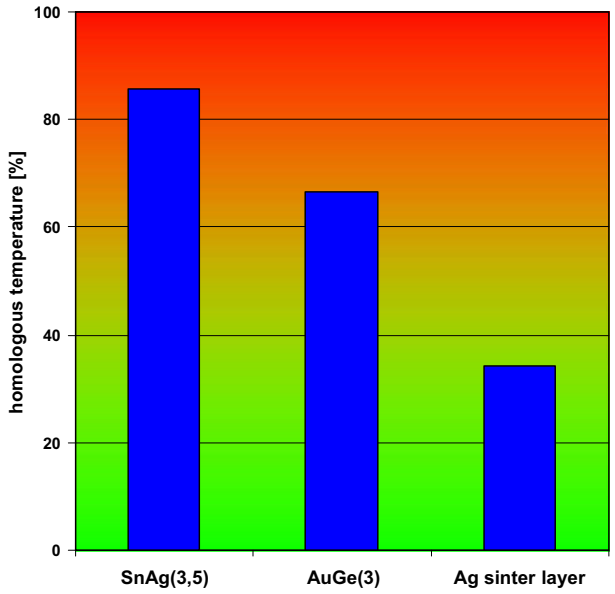


Fig. 9. Homologous temperature for chip interconnection layers assuming an operation temperature of 150 °C. The homologous temperature is the ratio of operation temperature to liquidus temperature in Kelvin.

exhibit homologous temperatures above 60%, while the silver sinter technology has a homologous temperature below 40% due to the high melting point of silver. For the long time stability under mechanical stress, homologous temperatures below 40% are considered appropriate, between 40% and 60% materials are in the so-called creep range and are therefore sensitive to strain, whereas above 60% homologous temperature, materials are considered 'unable to bear engineering loads'.

An enhanced reliability can be anticipated as a consequence of these favorable characteristics of the sinter technology, because degradation effects as known from solder interfaces are not expected for silver sinter interconnections.

5. The 100% solder-free module

Combining all technologies discussed above in a single module leads to the first modern power module without a single solder interface. Fig. 10 shows an explosion view of the module architecture. Looking at the construction form bottom up, the construction elements can be identified.

On the bottom, the three phase leg power substrates are displayed, carrying two switches formed by six IGBTs and three FWDs each. Each diode is placed between two IGBTs, so that the commutation paths are kept as short as possible. The blue rectangles[1] indicate the landing position of the multi-contact internal bus bars, while the blue circles mark the landing area of the control and sensor contact springs.

The gray housing element aligns the DBC substrates and all electrical connections. The columns for the springs and the mounting bolts (not shown) assure the necessary creepage and clearance distances in the package. A high temperature resistive foil insulates the three elements of the multi-contact internal bus bar systems against each other.

The dark gray pressure foam distributes the pressure homogeneously to all contact positions of the internal bus bar structure. The dark red pressure plate on top – a molded steal structure – transfers the pressure to the whole system.

The presented modules have successfully passed the series qualification program and are available in two different versions. The SKiM®63 module combines four IGBTs and two FWDs per switch in a sixpack configuration with a nominal current of 600 A for 600 V blocking voltage. The SKiM®93 package combines six IGBTs and three FWDs per switch to form a 900 A sixpack module for 600 V blocking voltage. Both package sizes are also available for higher blocking voltages.

Reliability tests confirm the expected high reliability of the package. Fig. 11 shows the temperature cycling test result in a

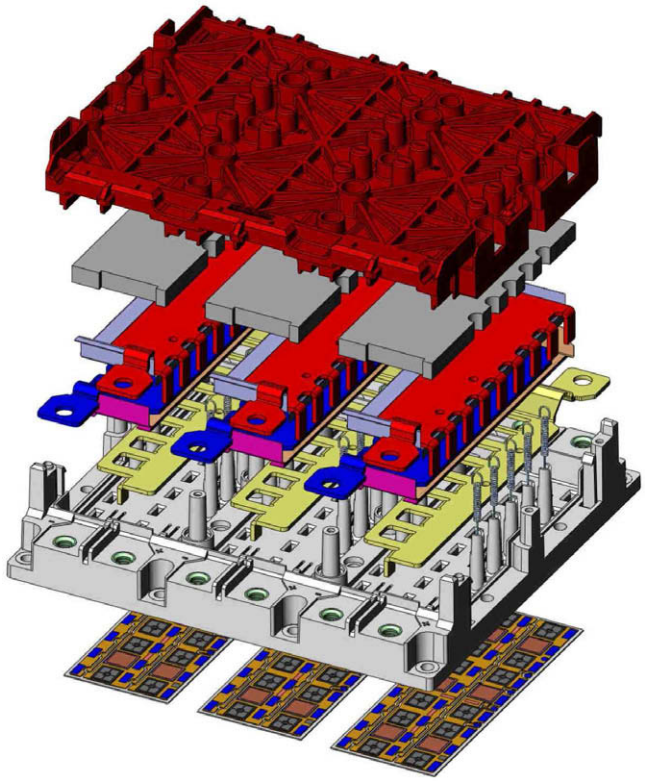


Fig. 10. Explosion view of the first 100% solder-free module showing the sintered substrates, the multi-contact internal bus bar, the springs for the control and sensor contacts and the pressure system.

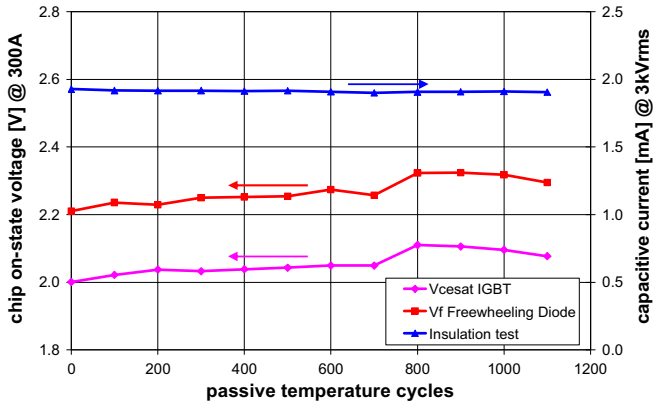


Fig. 11. Temperature shock test results (−40 °C/+125 °C) for a SKiM®63 proving stable contact and insulation properties for 1100 cycles.

[1] For interpretation of color in Fig. 10, the reader is referred to the web version of this article.

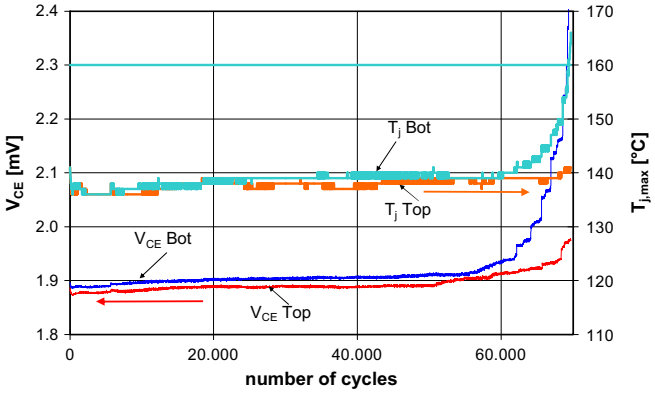


Fig. 12. Power cycling test on a 1200 V SKiM®63 module: the elimination of all solder interfaces increases the lifetime during active power cycles by more than 50%.

two chamber temperature shock test (air to air) with chamber temperatures of −40 °C and +125 °C and dwell times of 90 min in each chamber.

Fig. 11 displays typical results for the test, which is an end-of-life test performed with a group of six modules. All modules have passed 1100 cycles without failure. This result verifies that the presented module architecture is capable of surviving more than 1100 passive temperature cycles, which is far beyond the capability of a classical module design with a copper base plate. The end-of-life temperature cycling test will be continued to establish a data base for statistical lifetime estimation and to identify failure modes.

The reliability of the SKiM® module during active power cycles was investigated by an end-of-life test as well. The TOP and BOT switch of a single phase leg were connected in series and subjected to a constant DC current of 209 A. During the heating time of approx. 80 s, the chips were heated up to a medium temperature of 140 °C, measured by the $V_{CE}(T)$-method with a small sense current right after the turn-off of the load current. These temperature values were monitored after every cycle for both switches. The on-state voltages of the two IGBT switches were recorded shortly before the load current turn-off. The results are depicted in Fig. 12.

For soldered power modules, the number of cycles to failure does not exceed 40,000 cycles under these test conditions, while the SKiM® module survives more than 69,000 cycles until failure. This result confirms that the improvement of the chip to substrate interconnection by the silver diffusion sinter technique leads to an increased lifetime during active power cycling due to the absence of solder degradation effects.

6. Conclusions

The classical module design with copper base plate is limited in the capability to withstand passive temperature cycles. The pressure contact system, which eliminates the base plate, can improve the stability under passive temperature cycles considerably.

The current distribution for static and dynamic conditions is efficiently improved by the implementation of internal bus bars with multiple contact positions. This architecture provides an evenly distribution of stress to several paralleled chips and thus increases the system reliability.

The silver diffusion technology enhances the lifetime of power electronic packages by eliminating the degradation of the conventional solder layer between the chip and the substrate.

The reliability test results confirm this expectation and show that the pressure contact technology combined with an internal bus bar structure with multiple contacts and the silver diffusion sinter technology can fulfill the demands of hybrid vehicle traction applications.

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