Impact of Absolute Junction Temperature on Power Cycling Lifetime

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Abstract

The influence of the absolute junction temperature T_j^* on IGBT power module lifetime was systematically investigated by means of active power cycling tests. Both the impact on the wire bond lift-off and the chip solder degradation mechanism could be determined separately by applying the concept of *separating failure modes*. The test results not only prove that classical lifetime models overestimate the influence of T_j^*, but also show that the two dominant failure mechanisms have to be treated differently. The wire bond lift-off failure mode is weakly affected by the absolute temperature level and possesses a very small activation energy of 0.069 eV. The solder degradation mode exhibits a significantly larger activation energy of 0.159 eV, which results in a massive decrease (factor 3) in power cycling capability when increasing T_j^* by 85 K. For junction temperatures above 175 °C SnAg-based solder joints are no longer suitable for reliable power module designs and advanced die attach technologies such as silver sintering have to be deployed. For the description of such advanced power modules specific lifetime curves are under development which exclusively represent the pure wire bond lifetime, as for common power cycling conditions the silver sintered die attach is not subjected to ageing.

Introduction

The useful lifetime of a classical power electronic module is mainly restricted by thermo-mechanical stress produced by either passive or active temperature cycles and the resulting ageing of interconnects. Especially the joints in the direct vicinity of the semiconductor dies are subjected to fast thermal changes with significant temperature amplitudes produced by the chips' power losses. More distant interconnects such as the baseplate solder layer undergo less severe temperature excursions from active operation due to the higher thermal capacities of substrate and baseplate. Therefore, only longer load cycles with power-on times exceeding 10 s produce sufficiently high temperature swings to stress the solder layer sustainably. Nevertheless, these large-area solder layers are usually quite sensitive to passive thermal cycles, which are produced by variations in the ambient conditions such as coolant temperature or ambient air.

For the lifetime estimation of a power electronic system all the expected active and passive temperature swings have to be considered and thoroughly counted by a Rainflow algorithm [1]. In practice, often either

typical or very critical load sequences are evaluated towards their temperature swings. The resulting numbers of temperature cycles can then be linked with their corresponding lifetime consumption by applying an appropriate lifetime model and a linear accumulation of damage approach following Palmgren-Miner's rule [2].

In the end the overall accuracy of the lifetime estimation depends to equal parts on the exact knowledge of the load profile, the thermal model which translates the load profile into the corresponding temperature profile and the quality of the used lifetime model.

Due to the demand for cost reduction of power electronic systems nowadays safety margins are reduced and the accuracy of lifetime estimation becomes more and more important. As a consequence, significant work has been invested in improving the accuracy of lifetime models in the last years.

The raw data used for the creation of a lifetime model have to be gathered by means of temperature cycling or *power cycling* (PC) tests. These endurance tests link the number of cycles to failure to certain specific test parameters and have to be performed under accelerated conditions to get lifetime information within reasonable testing time. The lifetime estimation of a power module system is then based on extrapolating the accelerated test results to application relevant conditions. While long-term power cycling tests at smaller temperature swings are beneficial to extend the interpolation range, it should be emphasized that these cannot eliminate the need for extrapolation to target lifetimes of 20 years and more with the associated uncertainty. This contribution focuses on active power cycles and the corresponding power cycling lifetime curves.

Power Cycling Lifetime

Modern power cycling lifetime curves contain several parameters influencing the expected number of cycles to failure N_F. Besides the junction temperature swing ΔT_j, as most important parameter, also the absolute junction temperature T_j^* was identified as important factor within the 1990s LESIT project [3].

In the context of active power cycling tests T_j^* can be either expressed by the maximum junction temperature $T_\mathrm{j,max}$, the minimum junction temperature $T_\mathrm{j,min}$ or the medium junction temperature $T_\mathrm{j,m}$, which is defined as $T_\mathrm{j,min} + \Delta T_\mathrm{j}/2$. For a given ΔT_j these reference temperature values can be easily transformed into each other, however this is not the case for the exponential functions, so that the associated parameter values are different for different selections of T_j^*.

There are good arguments for all three possible selections. As the physics of failure usually is accelerated by higher temperature it seems to be most appropriate to use $T_\mathrm{j,max}$ as a reference temperature as this temperature is closer to physics of failure relevant material parameters such as the melting temperature of solder material for example. On the other hand, $T_\mathrm{j,min}$ exhibits less correlations to other parameters as the authors of the CIPS2008 model discussed in detail [4]. Other authors prefer the medium temperature $T_\mathrm{j,m}$ as a good compromise between the two extremes.

While the dependence on ΔT_j is expressed by a power law $N_\mathrm{F} \propto \Delta T_\mathrm{j}^x$, with x being a negative number in the range of $-3 \ldots -5$, the influence of the absolute junction temperature is usually considered as an Arrhenius term $N_\mathrm{F} \propto \exp\left(E_\mathrm{A}/(k_\mathrm{B} \cdot T_\mathrm{j}^*)\right)$ with a characteristic activation energy E_A and the Boltzmann constant k_B. A relatively high activation energy of 0.62 eV was derived for the $T_\mathrm{j,m}$-dependence in the LESIT model according to a consistent least square fit of parameters to the LESIT data [5].

A refined lifetime model was introduced in 2008 by Bayerer et al. as the CIPS2008 model [4]. More than 170 single power cycling test results were statistically analyzed and additional parameters such as the power-on time, the wire bond thickness, the chip voltage class and the current per wire bond stitch were identified. The $T_\mathrm{j,max}$-dependence found in this analysis was expressed with a much lower activation energy of 0.165 eV. The huge difference compared to the LESIT model was very surprising but might be explained by significant improvements in today's packaging technology (e.g. the transition from lead-based soldering towards lead-free soldering, improved wire bonding etc.) and the fact that the LESIT model did not take into account other important test parameters such as the power on-time t_on for example.

The drastic impact of the difference in activation energies becomes visible when comparing the increase in calculated power cycling capability by reducing the junction temperature level by 60 K. Following the LESIT model an increase in N_F by a factor of 20 is expected, whereas for the CIPS2008 model the power cycling capability only doubles. Obviously, the influence of T_j^* on N_F had to be clarified by experiment.

A general problem of both power cycling lifetime models discussed above is that there is no clear distinction between the relevant failure modes occurring during active power cycling. In this contribution the focus lies on the typical failure modes produced close to the semiconductor die by short power cycles ($t_{on} < 10\,s$). Other failure modes such as baseplate solder fatigue have to be investigated in separate studies with different samples and suitable power cycling parameters.

On the one hand, there is the wire bond lift-off failure which is driven by the mismatch of the *coefficients of thermal expansion* (CTE) of the wire material (usually aluminum) and the silicon chip. The resulting thermo-mechanical stress during power cycling initiates crack formation and drives crack propagation within the Al wire [6, 7]. On the other hand, there is chip solder fatigue which is also driven by thermo-mechanical stress, but in this case is mainly determined by the material parameters of the *Direct Bonded Copper* (DBC) substrate and the Si-Chip. Depending on the solder material, the power density in the semiconductor chip and the geometry the ageing of the solder layer can either start from the edges or from the center of the chip [8].

Although both failure modes are induced by similar driving factors they occur in different materials (Al or SnAg-based solder) and the physics of failure is not necessarily identical. As a consequence, also the functional dependencies on the power cycling test parameters might differ. Therefore, the description of a classical power module's lifetime by just one single function is not ideal and the dominant failure mechanism for a given set of test parameters cannot be predicted. A more appropriate approach to describing the *end-of-life* (EOL) of power modules should use individual lifetime curves for each relevant failure mode and the failure to happen first has to be evaluated for the given test conditions. Also a possible interaction of both failure modes could then be taken into account [9].

The substitution of solder layers in classical power modules by the much more reliable silver-sintered joints [10] made it possible to determine the wire bond lifetime separate from other failure mechanisms. A first power cycling lifetime curve for such advanced modules without any solder layer was recently published by Scheuermann et al. [11]. In addition to the parameters used in the CIPS2008 model this new lifetime curve also contains a special parameter describing the geometry of the wire bond loop. As the silver sintered die attach is not subjected to ageing for common power cycling conditions this lifetime curve can be used to describe the pure wire bond lift-off failure also in soldered modules.

The aim of the present investigation was to determine the impact of T_j^* on the above mentioned failure modes. Unlike the previous investigations, this power cycling study exclusively focuses on the impact of T_j^* and all other parameters influencing the lifetime were kept constant. A significant difference between solder degradation and wire bond lift-off is expected as a previous investigation by Goehre et al. showed that the absolute junction temperature T_j^* does not have a significant impact on the crack propagation in the wire bond foot during power cycling testing [7].

Power Cycling Study

For the present power cycling study the concept of *separating failure modes* was deployed to investigate the impact of T_j^* on wire bond lift-off and solder fatigue separately [9]. As mentioned above the wire bond lift-off failure can be studied on solder-free modules containing a silver sintered die attach. These types of module are now in series production and are fully qualified.

On the other hand, several advanced chip top side contact technologies have been developed in the last years. Besides new wire bond materials, such as Al-clad Cu wire bonds [12] or pure Cu-wire bonds [13] also Cu-flexlayers [14] have proven to enhance the power cycling capability by at least one order of magnitude. In combination with a soldered die attach special test samples can be produced that allow for studying the solder degradation failure without the disturbing interaction of wire bond failures.

Two groups of samples were prepared based on a 1200 V baseplate-less six-pack module with 300 A nominal current [15]:
Group 1 was the standard series product containing a silver sintered die attach and standard Al wire bonds of reasonable loop geometries (aspect ratio of 0.29). For the group 2 samples the chips were soldered to the DBC by a common vapor phase soldering process using $SnAg_{3.5}$ solder. For the chip top side contact Al-clad copper wires were bonded to the standard Al chip surface. Due to the high reliability of silver sintered layers all group 1 modules are expected to solely fail due to wire bond failure mechanisms, whereas the high-reliability wire bonding of group 2 modules should lead to 100 % solder degradation failures.

All samples of both groups were mounted onto identical water coolers using thermal grease as interface material. For all tests identical test benches were used which allowed for testing one of the three half-bridges (top and bottom switch) per test run. The same power cycling conditions were applied to all samples:
The junction temperature swing of the *Insulated Gate Bipolar Transistors* (IGBTs) was set close to $\Delta T_\mathrm{j} = 110\,\mathrm{K}$ (target value 108 K) and a constant power on-time of $t_\mathrm{on} = 7\,\mathrm{s}$ was used. By adjusting the cooling water temperature it was possible to vary the absolute junction temperature level. Four different temperature levels were tested covering a wide range of 85 K ($T_\mathrm{j,min} = -20\,^\circ\mathrm{C}, 10\,^\circ\mathrm{C}, 40\,^\circ\mathrm{C}$ and $65\,^\circ\mathrm{C}$). Due to the positive temperature coefficient of the IGBT the tests at lower temperatures had to be conducted with slightly higher load currents I_L to apply the same dissipated power and compensate for the reduced V_CE. Nevertheless, the applied load currents only varied between 300 A and 330 A and therefore no significant influence on the number of cycles to failure is expected.

The low-temperature tests ($T_\mathrm{j,min} = -20\,^\circ\mathrm{C}$ to $T_\mathrm{j,max} = 90\,^\circ\mathrm{C}$) were performed inside a climatic chamber with an ambient temperature of $-25\,^\circ\mathrm{C}$ to prevent condensation on the module. In this case a 50/50 mixture of water/glycol had to be used as coolant ($T_\mathrm{coolant} = -23\,^\circ\mathrm{C}$).

Impact of T_j^* on wire bond lift-off

The group 1 power modules were tested in four test runs at different absolute junction temperature levels. Fig. 1 shows the evolution of $T_\mathrm{j,max}$ and V_CE for the top and the bottom switch of sample 1A, tested at the lowest temperature level. As expected for the sintered type of modules the thermal resistance $R_\mathrm{th(j\text{-}s)}$ stays constant over the whole test and no significant increase in $T_\mathrm{j,max}$ could be observed during the test. As failure criterion a 5 % increase in V_CE was evaluated. Shortly before reaching the end-of-life at 66 630 cycles several steep steps in the V_CE of the top switch indicate the gradual loss of wire bond connections. The after-test analysis revealed that wire bond lift-off is the only failure mechanism and no heel cracking occurred. No degradation of the silver sintered die attach could be observed in the *Scanning Acoustic Microscopy* (SAM) images.

Similar curves were recorded for the 3 other modules tested at higher junction temperature levels. All failure events were solely limited to wire bond lift-off. The exact power cycling test parameters and the resulting number of cycles to failure are summarized in Table I. For the samples 1C and 1D both IGBT of the tested half bridge reached the failure criterion and could be used for the determination of the activation energy.

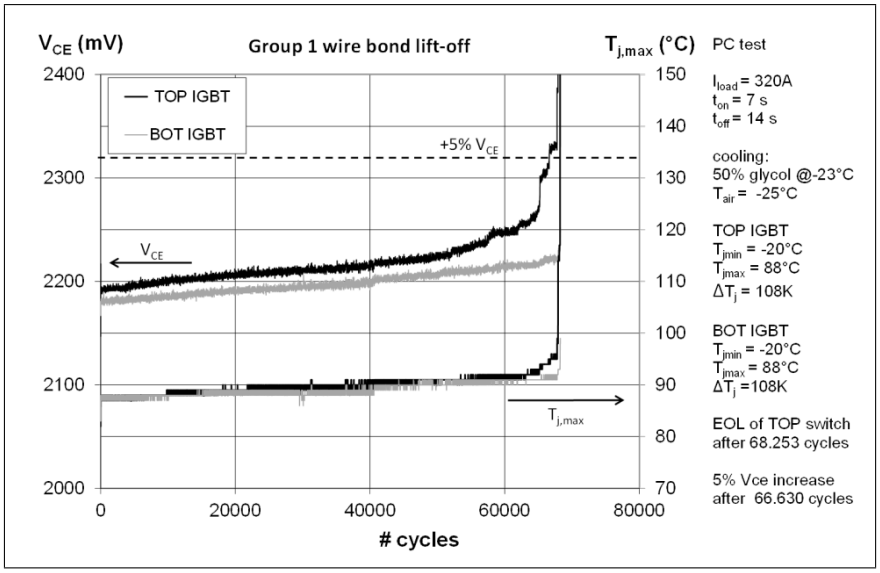

Figure 1: Power cycling diagram of sample 1E; Evolution of V_{CE} and $T_{j,max}$

The power cycling test on sample 1B ran with a slightly reduced ΔT_j of only 106 K instead of 108 K. As only one test result was obtained for this temperature level N_F had to be corrected for a ΔT_j^x-dependence with $x = -4.4$ to be able to compare with the other tests [4]. This correction leads to a 5.5 % reduction of the original N_F-value. As expected, the number of cycles to failure steadily decreases with increasing

Table I: Power cycling results of group 1

Sample	$T_{j,min}$ in °C	$T_{j,max}$ in °C	$T_{j,m}$ in °C	ΔT_j in K	I_L in A	Cycles to failure	Corrected for ΔT_j^x
1A	−20	88	34	108	320	66630	
1B	10	116	63	106	326	63090	59620
1C	40	148	94	108	310	46040	
1C	40	148	94	108	310	49321	
1D	66	174	120	108	300	46550	
1D	66	174	120	108	300	42730	

absolute junction temperature. While for the low-temperature test on sample 1A still 66630 cycles were achieved the number of power cycles drops to a mean value of 44640 for the test running to the maximum rated temperature of the IGBT at $T_{j,max} = 175\,°C$. Although the difference in junction temperature level is 85 K the reduction in power cycling capability is only in the range of 30 to 35 %.

Plotting $\ln(N_F)$ over $1/T_{j,max}$ allows for a linear fitting of the Arrhenius dependency (Fig. 2). An activation energy of 0.069 eV was deduced from the data. If the same data is interpreted for the medium junction temperature an even smaller activation energy of 0.052 eV is found. Both values illustrate the very weak influence of absolute junction temperature level T_j^* on the pure wire bond lift-off failure and are in good agreement with the value recently reported by Schilling et al. [16].

Consequently, the absolute junction temperature only plays a minor role for the power cycling capability of Al-wire bonded sinter-modules and the activation energies for $T_{j,m}$- or $T_{j,max}$-dependences proposed in the lifetime models above do not apply.

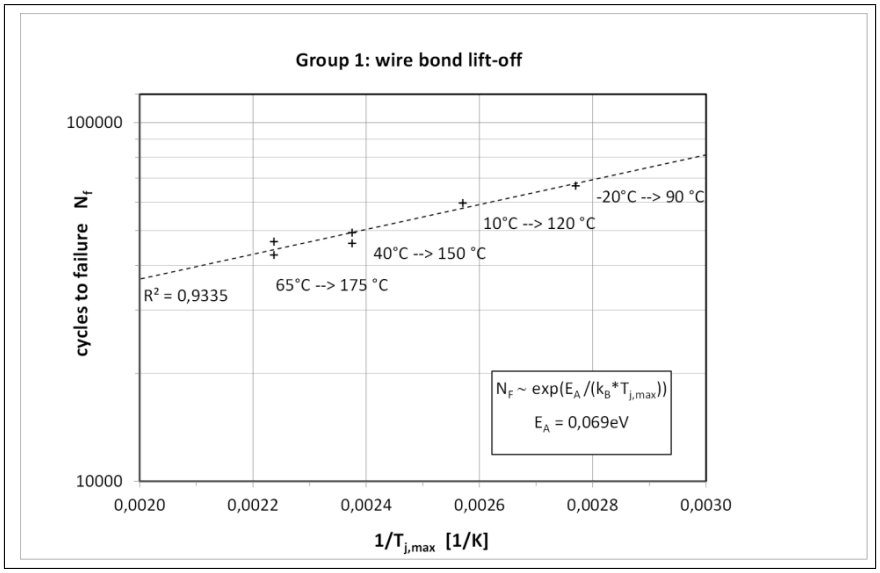

Figure 2: Power cycling results of group 1 samples plotted over $1/T_{\mathrm{j,max}}$: Determination of the activation energy for the wire bond lift-off failure

Impact of T_{j}^{*} on solder fatigue

A similar set of power cycling tests was carried out on the soldered and Al-clad Cu-wire bonded modules of group 2. As intended, all tested samples showed solder degradation failures at the test end as verified by SAM images before and after the tests (Fig. 3). Apparently, the solder fatigue starts from the center of the IGBT chips subjected to power cycling. No lift-off of the Al/Cu-wires occurred prior to reaching the EOL-criterion of 10 % increase in thermal resistance.

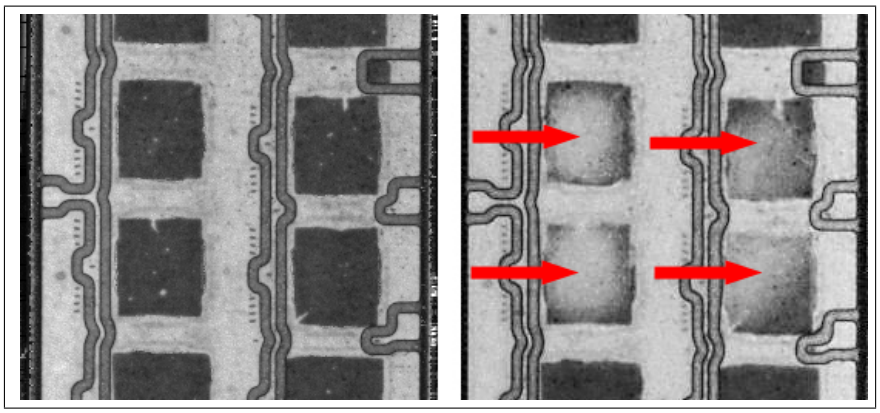

Figure 3: SAM images, before and after PC test: massive solder degradation at the positions of the tested IGBT chips

A typical power cycling diagram for the soldered samples (here sample 2E) is depicted in Fig. 4. It illustrates the drastic increase of the upper switching temperature $T_{\mathrm{j,max}}$ during the last quarter of the test indicating the increase in thermal resistance $R_{\mathrm{th(j\text{-}s)}}$ due to chip solder fatigue. Owing to its positive temperature coefficient also V_{CE} increases with rising junction temperature. Nevertheless, no steps are present in the evolution of the V_{CE} which indicates the loss of wire bond connections. As typical for pure solder degradation failures, the $+10\,\%$ $R_{\mathrm{th(j\text{-}s)}}$ failure criterion is reached much earlier than the $+5\,\%$ V_{CE} criterion used for the wire bond failures of group 1 samples.

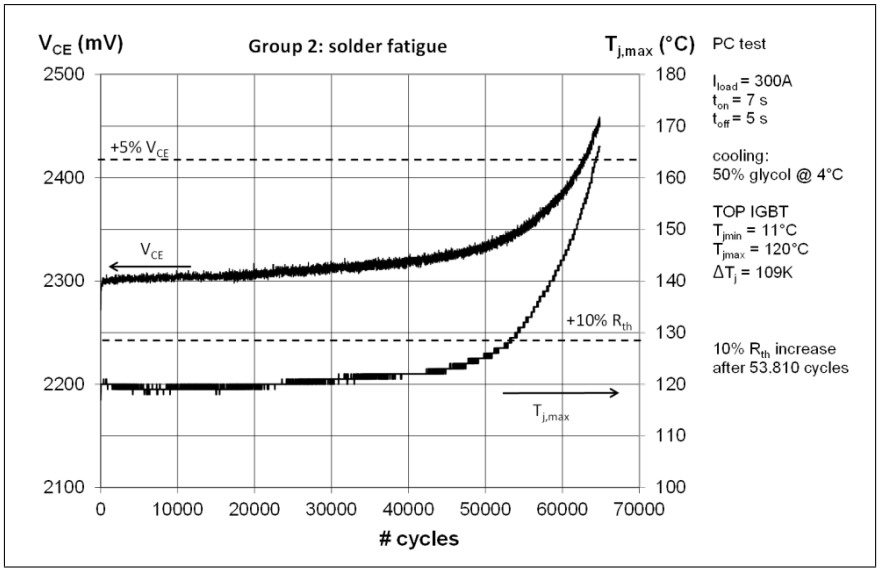

Figure 4: Power cycling diagram of sample 2E; evolution of V_{CE} and$T_{\mathrm{j,max}}$

Table II: Power cycling results of group 2

Sample	$T_{\mathrm{j,min}}$ in °C	$T_{\mathrm{j,max}}$ in °C	$T_{\mathrm{j,m}}$ in °C	ΔT_{j} in K	I_{L} in A	Cycles to failure
2A	−19	90	33.5	109	329	90761
2B	−19	88	34.5	107	300	93530
2B	−19	88	34.5	107	300	111677
2C	11	121	66.0	110	315	51910
2C	11	120	65.5	109	315	46710
2D	10	119	64.5	109	300	46180
2D	11	119	65.0	108	300	54850
2E	11	121	66.0	110	300	48320
2E	12	119	65.5	107	300	53810
2F	39	148	93.5	109	295	42520
2F	39	147	93.0	108	295	46154
2G	41	150	95.5	109	300	38721
2G	40	151	95.5	111	300	43971
2H	64	174	119.0	110	295	32035
2H	64	174	119.0	110	295	31485
2I	65	178	121.5	113	300	33508
2I	66	176	121.0	110	300	36630
2J	90	197	143.5	107	295	6110
2J	90	198	144.0	108	295	14010

For the group 2 samples more than one test was performed for a certain temperature level. Table II summarizes these test results. Except for sample 2A all tests could be evaluated for the top and the bottom IGBT. Sample 2J was tested at an elevated temperature level exceeding the maximum rated temperature of the IGBT. These results were not used for the determination of the activation energy.

The samples 2A and 2B were tested at the low-temperature condition (target: $T_{\mathrm{j,min}} = -20\,^{\circ}\mathrm{C}, T_{\mathrm{j,max}} = 90\,^{\circ}\mathrm{C}$) and withstood between 90000 and 112000 cycles before reaching the EOL-criterion. Direct comparison with the Al-wire bonded samples of group 1 (wire bond failure after 66630 cycles) proves the

high reliability of the Al-clad Cu wire bond contacts, which were still completely intact at the end of the test. On the other hand, it shows that the solder layer has a significantly higher lifetime than the investigated Al-wire bonds at the present low-temperature test condition.
The following tests at higher absolute junction temperature levels (2C - 2I) yield significantly decreased numbers of cycles to failure. For instance, for the power cycling test with cycles between $T_{\mathrm{j,min}} = 65\,^{\circ}\mathrm{C}$ and $T_{\mathrm{j,max}} = 175\,^{\circ}\mathrm{C}$ only an average of 33 400 cycles could be completed. This means a reduction of a factor 3 within 85 K of absolute temperature range. Less cycles to failure were passed than for the corresponding group 1 test indicating that at high absolute temperature levels the solder layer has a lower power cycling capability than the Al-wire bond. Obviously, the solder fatigue lifetime decreases much faster with increasing temperature level than for the wire bond lift-off failure mode.
In Fig. 5 the power cycling test results of the group 2 samples are plotted over $1/T_{\mathrm{j,max}}$ to deduce the activation energy of the solder degradation failure mode. An activation energy of $E_{\mathrm{A}} = 0.159\,\mathrm{eV}$ for the $T_{\mathrm{j,max}}$-dependence and of $E_{\mathrm{A}} = 0.121\,\mathrm{eV}$ for the $T_{\mathrm{j,m}}$-dependence are found. The value for the influence of $T_{\mathrm{j,max}}$ is very close to the activation energy used in the CIPS2008 lifetime model.

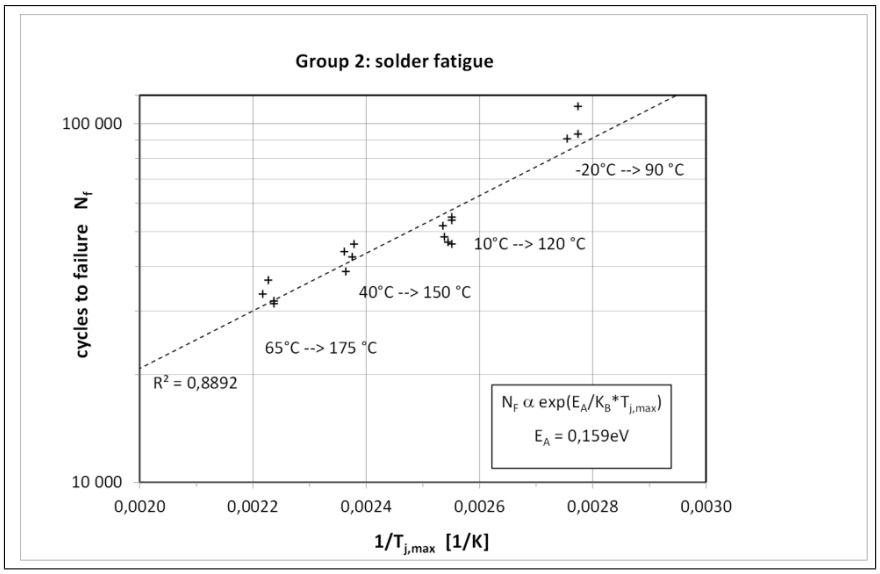

Figure 5: Power cycling results of group 2 plotted over $1/T_{\mathrm{j,max}}$: Determination of the activation energy for solder fatigue failure

To check for the confidence range of the Arrhenius type model for the T_{j}^{*} dependence, an additional sample (2J) was tested even beyond the maximum rated junction temperature of the IGBT chip. With a $T_{\mathrm{j,max}}$ of almost 200 °C the chip temperature reached values very close to the melting point of the used $SnAg_{3.5}$-solder ($T_{\mathrm{melt}} = 221\,^{\circ}\mathrm{C}$). Considering the fact that significant lateral temperature gradients are present on the chip and that the virtual junction temperature evaluated during the power cycling test only represents an average chip temperature, central chip regions are even closer to the melting point [17].
The high temperature tests failed after 6110 and 14 010 cycles in the top and the bottom IGBT, respectively. This is much earlier than expected from an extrapolation of the previous test results. Apparently, the description of the solder degradation failure by an Arrhenius term is no longer valid in temperature regions close to the melting point of the solder. The ageing occurs much faster and the thermal resistance increases rapidly, eventually leading to hot spots and local melting of the solder. This failure scenario could be verified by the SAM- and polished micrograph analysis after the test where larger parts of the solder layer could be identified to be melted during the power cycling test.
Beyond 175 °C not only the Arrhenius model is at its limit, also solder die attaches cannot be operated at such high temperatures with sufficient reliability. For a higher junction temperature of 200 °C and more, which already was announced for future IGBT generations and advanced devices made of wide bandgap semiconductor materials (SiC, GaN), advanced die attach technologies have to be deployed.

Good alternatives to SnAg-based soldering are the silver-sintering technology and diffusion soldering, which both have proven to realize very reliable joints even under severe power cycling conditions [18].

Conclusion

A systematic study on the impact of absolute junction temperature level T_j^* on the power cycling lifetime was performed. The study verifies that the two dominant end-of-life failure mechanisms present in classical power modules exhibit different activation energies. A very weak impact of T_j^* on the power cycling capability of Al wire bonds was found. The small activation energy for the $T_{j,max}$dependence of 0.069 eV is consistent with results of other recently reported studies. The impact on the solder fatigue process is much more pronounced and for the activation energy a value of 0.159 eV could be derived. The massive decrease in number of cycles to failure for higher temperature levels shows the need for superior die attach technologies and beyond 175 °C SnAg-based solder joints are not considered to be reliable.

The activation energy of 0.159 eV for the solder fatigue is quite close to the value used in the CIPS2008 lifetime model. However, the significantly higher activation energy proposed in the LESIT model is not confirmed for today's power modules. Lifetime predictions based on the LESIT curve overestimate the lifetime gain as a consequence of extrapolating accelerated test results at high absolute junction temperatures to application conditions at typically smaller temperature levels.

In the near future, when more advanced power modules with silver sintered die attach will be used, the elimination of solder fatigue facilitates the lifetime prediction. With the power cycling capability of the silver sintered die attach being at least one order of magnitude higher than for the Al wire bond only the wire bond remains as failure source. For such modules the lifetime curve recently published by Scheuermann et al. is proposed as the basis for pure wire bond failures [11]. In this model the activation energy of 0.066 eV derived for the $T_{j,m}$-dependence is slightly higher than the value obtained in the present study, but is much smaller than for the solder fatigue mechanism.

The presented study additionally illustrates how changing the test condition can lead to a change in the failure mode. Let us consider a classical power module with soldered die attach and comparable Al wire bonds like used in this investigation. At low temperature operation and comparable temperature swings such a module would fail due to pure wire bond lift-off. But the results of the present study show that situation changes when operating at higher temperature. As the decrease in power cycling capability is much faster for the chip solder fatigue it will become the dominating failure mechanism at high temperature. For an intermediate temperature range both failure modes compete and their interaction eventually accelerates the end-of-life failure so that a mixture of both failure modes would be observed in the end-of-life analysis.

The power cycling test study described in this article solely focused on testing at a relatively high ΔT_j of 110 K. Usually power cycling parameters are not necessarily independent and it might be possible that changing one parameter, e.g. the temperature swing could have impact on the activation energy of the T_j^* dependence. Therefore, the results of the presented investigation must be validated at other temperature swings and power-on times.

In general, the principle of *separating failure modes* can be applied to determine different functional dependencies on other relevant power cycling test parameters. Of great interest are the ΔT_j and the power-on time t_{on}. If individual lifetime models would be available for each relevant failure mode, the correlation of different degradation mechanisms could be better understood and more precise lifetime predictions would be possible.

References

[1] S.D.Downing, D.F.Socie: *Simple rainflow counting algorithms*, International Journal of Fatigue **4**, (1982), 31-40.

[2] M.Ciappa: *Lifetime Prediction on the Base of Mission Profiles*, Microelectronics Reliability **45**, (2005), 12931298.

[3] M.Held, P.Jacob, G.Nicoletti, P.Scacco, M.H.Poech: *Fast Power Cycling Test for IGBT Modules in Traction Application*, Proc. Power Electronics and Drive Systems, (1997), 425-430.

[4] R.Bayerer, T.Herrmann, T.Licht, J.Lutz, M.Feller: *Model for Power Cycling Lifetime of IGBT Modules – various factors influencing lifetime*, Proc. CIPS 2008, 37-42.

[5] M.Ikonen, U.Scheuermann, P.Silventoinen: *Power Cycling Lifetime of Power Modules at High Junction Temperature Swings*, Proc. PCIM Europe, PP8, CD-ROM, Nürnberg, 2007.

[6] J.Onuki, M.Koizumi, M.Suwa: *Reliability of thick Al wire bonds in IGBT modules for traction motor drives.* IEEE Trans. Advanced Packaging **23**, Nr. 1 (2000), 108-112.

[7] J.Goehre, M.Schneider-Ramelow, K.-D.Lang, U.Geißler: *Interface Degradation of Al Heavy Wire Bonds on Power Semiconductors during Active Power Cycling Measured by the Shear Test*, Proc. CIPS 2010, 97-102.

[8] A.Morozumi, K.Yamada, T.Miyasaka, S.Sumi, Y.Seki: *Reliability of Power Cycling for IGBT Power Semiconductor Modules*, IEEE Transactions on Industry Applications **39**, (2003), 665-671.

[9] R.Schmidt, U.Scheuermann: *Separating failure modes in power cycling tests*, Proc. CIPS 2012, ETG-Fachbericht **133**, (2012), 97-102.

[10] U.Scheuermann, P.Wiedl: *Low temperature joining technology – a high reliability alternative to solder contacts*, Workshop on Metal Ceramic Composites for Functional Applications, Wien, (1997), 181-192.

[11] U.Scheuermann, R.Schmidt: *A New Lifetime Model for Advanced Power Modules with Sintered Chips and Optimized Al Wire Bonds*, Proc. PCIM Europe 2013, 810-817.

[12] R.Schmidt, C.König, P.Prenosil: *Novel wire bond material for advanced power module packages*, Microelectronics Reliability **52**, (2012), 22832288, http://dx.doi.org/10.1016/j.microrel.2012.06.139

[13] D.Siepe, R.Bayerer, R.Roth: *The future of wire bonding is? Wire bonding*, Proc. of CIPS 2010, ETG-Fachbericht **121**, (2010), 115-118.

[14] P.Beckedahl, M.Hermann, M.Kind, M.Knebel, J.Nascimento, A.Wintrich: *Performance comparison of traditional packaging technologies to a novel bond wire-less all sintered power module*, Proc. of PCIM Europe, (2011), 247-252.

[15] U.Scheuermann, P.Beckedahl: *The Road to the Next Generation Power Module* – 100 % *Solder Free Design*, Proc. CIPS 2008, ETG-Fachbericht **111**, (2008), 111-120.

[16] O.Schilling, M.Schäfer, K.Mainka, M.Thoben, F.Sauerland: *Power Cycling Testing and FE Modelling Focussed on Al Wire Bond Fatigue in High Power IGBT Modules*, Microelectronics Reliability **52**, (2012), 23472352, http://dx.doi.org/10.1016/j.microrel.2012.06.095

[17] R.Schmidt, U.Scheuermann: *Using the chip as a temperature sensor – The influence of steep lateral temperature gradients on the $V_{CE}(T)$-measurement*, Proc. of EPE 2009, Barcelona, Spain (2009)

[18] K.Guth, N.Oeschler, L.Böwer, R.Speckels, G.Strotmann, N.Heuck, S.Krasel, A.Ciliox: *New assembly and interconnect technologies for power modules*, Proc. CIPS 2012, ETG-Fachbericht **133**, (2012), 380-384.