Condition Monitoring for Device Reliability in Power Electronic Converters: A Review

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***Abstract*—Condition monitoring (CM) has already been proven to be a cost effective means of enhancing reliability and improving customer service in power equipment, such as transformers and rotating electrical machinery. CM for power semiconductor devices in power electronic converters is at a more embryonic stage; however, as progress is made in understanding semiconductor device failure modes, appropriate sensor technologies, and signal processing techniques, this situation will rapidly improve. This technical review is carried out with the aim of describing the current state of the art in CM research for power electronics. Reliability models for power electronics, including dominant failure mechanisms of devices are described first. This is followed by a description of recently proposed CM techniques. The benefits and limitations of these techniques are then discussed. It is intended that this review will provide the basis for future developments in power electronics CM.**

***Index Terms*—Condition monitoring (CM), failure mechanism, fault detection, power electronics, prognosis, reliability.**

I. Introduction

CONDITION monitoring (CM) is a technique or a process of monitoring the operating characteristic of a physical system, so that the change of the monitored characteristic can be used to schedule maintenance before serious deterioration or break down occurs [1]. CM embraces a knowledge of failure mechanisms of individual parts or the integrated system, sensor technologies, data acquisition and analysis, and the ability to estimate the health condition of the system [2].

Referring to Fig. 1, CM is different to prognosis and diagnosis, although detecting faults is an essential part for all three. We can make the following definitions.

1) *Diagnosis:* Given that a fault has occurred, diagnosis is to identify the root cause of that fault.
2) *Prognosis:* Prognosis assesses the current health level of a component, and predicts the health of the component at some point in the future.

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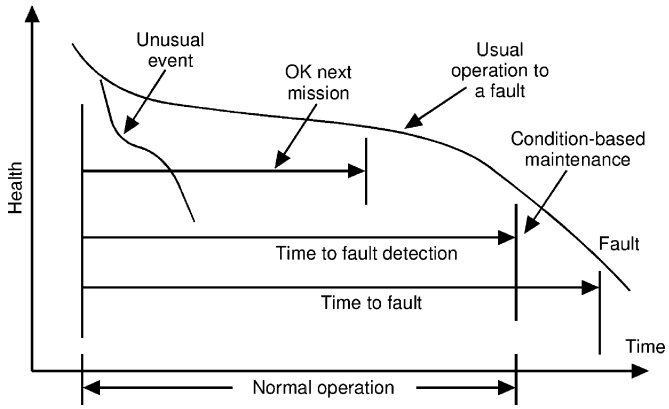


Fig. 1. Fault prognosis, diagnosis, and CM schemes [3]. The fault event causes the jump in health level shown.

3) *CM:* CM is to real-time measure the condition of a component, such that if it drifts away from the healthy condition an appropriate action to be taken.

The application of CM to power electronics is increasing in importance for the following reasons.

1) The increasing use of power electronics in safety critical systems, where an unpredicted failure may trigger a catastrophic accident or unscheduled maintenance resulting in high penalty cost.
2) New knowledge about the failure modes of power devices and development in sensor technologies and signal processing make it realistic to develop effective power electronic converter CM systems.

Applying the concept of CM to power electronics is challenging due to an as yet inadequate correlation between the known degradation or incipient failure and the measured physical states. The former requires further knowledge regarding device or system failure mechanisms, and the latter requires practical techniques to monitor performance degradation. These are being actively addressed in the research to be reviewed.

In this paper, the up-to-date knowledge of the reliability of power devices in converters, including reliability requirements and aging, and failure mechanisms, will be reviewed. This will be followed by a review of reliability modeling approaches from the device structure, thermoelectrical and thermomechanical points of view. Power electronics CM techniques developed to date—including those that are sensor or model based—are then reviewed to reflect the state-of-the-art of research. These techniques are generally based on the knowledge of the failure modes of power electronic converters and past experience in fault detection. This review will examine the recent progress of

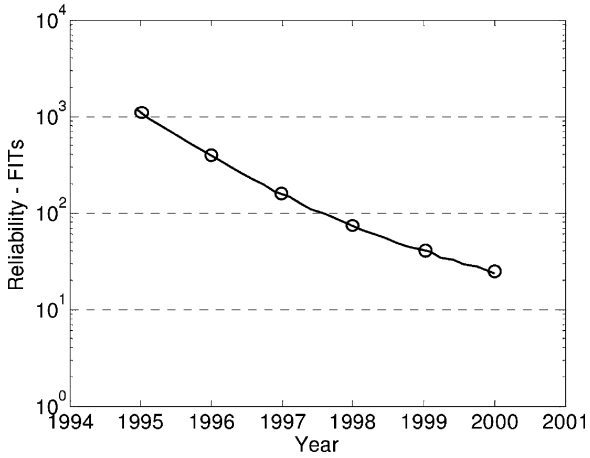


Fig. 2. Device (IGBT) FIT rate evolution [5].

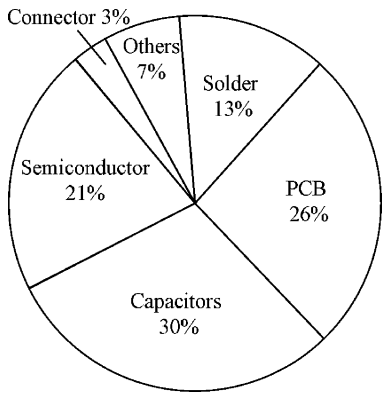


Fig. 3. Failure distribution and ranking [7].

CM, and put this in the perspective to stimulate further development in the future.

II. Reliability of Power Devices

The reliability requirements for power electronic converters are described first, followed by a review of past power electronics reliability projects. The progressive failure mechanisms for power devices are divided into those associated with the chip and those associated with the packaging.

A. Reliability Requirements of Power Devices

Factors such as electrical loading, mechanical vibration, and environmental condition, all exert stresses on a power electronics system. For example, the electrical traction drive for an urban tram may experience 10^6–10^8 power cycles, with temperature swings up to 80 °C, during its lifetime [4]. These power cycles critically affect the reliability and lifetime of the power device packaging. This has been a key driver in improving the reliability of power devices. As shown in Fig. 2 based on 500 000 IHM/IHV (insulated gate bipolar transistor (IGBT) high power and high voltage) modules, the failure rate dropped from 1000 failures in time (FITs) in 1995 to 20 FITs in 2000 [5], and to only a few FITs nowadays, where 1 FIT $= 1 \times 10^{-9}$ failures per device-hour. Furthermore, for safety-critical applications, such as aeroplanes, the zero-defect concept has been proposed to meet stricter reliability requirements [6].

Although the failure rates of power devices have been greatly reduced, reliability is always a focus. As shown in Fig. 3, semiconductor and soldering failures in device modules totals 34% of converter system failures, according to a survey based on over 200 products from 80 companies [7]. According to another survey, around 38% of the faults in variable-speed ac drives are due to failures of power devices [8]. Typically demanding applications for converters are in traction, especially metro rail traction and urban driving for automotive electric traction, and for renewables wind turbines. The results of a recent questionnaire for industrial power electronics [10] also showed that only 50% of respondents were satisfied with reliability monitoring methods, showing that research effort is needed in health management.

Fig. 3 also indicates that capacitors are fragile. The failure mechanisms for electrolytic capacitors and a relevant CM technique for monitoring the variation of capacitance and equivalent series resistance (ESR) are well documented in [9]. They are not repeated here as this review is concerned with the switching devices; indeed the questionnaire in [10] indicated that power devices were the most important area of concern.

B. Review of Past Projects

Several projects have been carried out in recent years to understand and improve power device reliability. Most of the work in recent years has concentrated on IGBTs for power electronic converters.

The LESIT project investigated the reliability of IGBT modules for traction applications, including IGBT bond wire liftoff, solder fatigue, and other reliability issues in traction applications [4], [11]–[13], the results of which have been used in later work [14]–[16]. The model has been recently extended to include more up-to-date devices and additional influences on reliability [123].

The EU RAPSDRA project aimed to apply IGBTs to the next generation of railway traction converters [17]. RAPSDRA contributed to IGBT technology by improving the reliability tests and by achieving agreement on standardized accelerated tests [18], [19]. Publications including [18], [20]–[24] and two handbooks were produced, covering basic device failure analyses and failure mechanisms. A related EU project, PORTE, has also generated results on traction applications [16], [25]–[28].

There are also projects at the CALCE group, covering a range of reliability areas, such as lead-free soldering, accelerated testing, failure analysis, and thermal management. Power devices are included, for example, investigation into failure precursors for IGBTs [29]. Recent work at the IeMRC, e.g., [30], has also investigated device packaging reliability prognostics, with emphasis on a physics of failure approach to the design, qualification, and modeling of power electronic modules.

C. Chip-Related Failure Mechanisms

Chip-related failure mechanisms are ultimately those that destroy a device. These are separated from packaging-related mechanisms, but may be interlinked for a failure event. The following points—overstress and wear out mechanisms during operation—are generally believed to cause characteristic degradations and potential failures in the long term. These need to be seriously considered when implementing a CM scheme and designing a converter [31], [32].

1) Electrical Overstress: Electrical overstress (EOS) is associated with overvoltage and overcurrent conditions. Heating effects under high-voltage conditions can be significant, and secondary breakdown is a major concern in some devices. It is necessary to ensure that the SOA for the power device is suitable for the application as well as to meet the heat sinking specification for the part [31]. For thyristors, the nonuniform current distribution during turn OFF, caused by fast *di*/*dt*, can lead to increased power dissipation and eventual thermal damage; a fast rising voltage ramp may cause displacement current, which can spuriously turn ON the device [33], resulting in a short circuit and failure.

2) Electrostatic Discharge (ESD): The contribution of electrostatic discharge (ESD) to the general set of EOS failure is difficult to define, since both EOS and ESD mechanisms result in similar failure modes [31]. ESD can partially puncture the gate oxide, allowing the device to work sufficiently well for the device to pass inspection, and finally, causing device failure after a period of operation [34]. Gate shorting has been reportedly caused by ESD when excessive voltage is applied to the gate if no protection is provided [34], [35]. Partial gate failure can be detected by measuring the time constant of the decay of gate charge [34].

3) Latch-Up and Triggering of Parasitics: Too large a value of *dv*/*dt* during turn OFF may cause triggering of the parasitic thyristor in IGBTs—causing latch-up—or triggering of the parasitic bipolar junction transistor (BJT) in power MOSFETs [36]. Depending on the location of the failure, the amount of energy the device is capable of handling may differ [37]. Although the latch-free technology has been developed [38], proper circuit design to confine the ramp rate of reapplied voltage in the reversed bias SOA to avoid latch-up is important [39].

4) Charge Effects—Ionic Contamination or Hot Carrier Injection: Two failure mechanisms are the most common for power MOSFETs. The first is the electric field distortion by the accumulation of ionic contaminants in the passivation of the high-field region, the second is the growth of defects in the gate oxide [34]. During high-temperature operations, hot carriers can be injected into the gate oxide or other interfaces when the carriers attains high energy beyond the lattice potential barrier, resulting in charge trap and interface state generation [40]. (Note that for MOS-gated power devices, hot carrier injection (HCI) is rarely a significant issue due to the relatively thick gate oxide.) These two mechanisms lead to shifts in the device performance characteristics—such as the threshold voltage, leakage current, transconductance, or saturation current—and eventually to device degradation [41], [42].

5) Electromigration, Contact, and Stress-Induced Migration: Atomic migration may occur due to electromotive force, interdiffusion, and the mechanical stress during the manufacturing process. These mechanisms are related to the metallization of the semiconductor devices and have an effect on long-term reliability. Such effects are rarely observed in power devices due to the large areas, however, some contact migration has been identified as a problem with Schottky diodes [31]. There has also been aluminium bond pad reconstruction observed during repetitive short-circuit testing, especially at high temperature, leading to an increase in resistance [126].

6) Thermal Activation: Thermally activated processes are enhanced by an increase in temperature, according to Arrhenius' law

$$\text{rate of activation } \propto \exp\left(-\frac{E_a}{RT}\right) \tag{1}$$

where E_a is the activation energy (in joule per mole), T is the temperature (in kelvin), and R is the gas constant (in joule per mole per kelvin). The degradation processes for nearly all silicon power devices are accelerated by increased temperature [34].

7) External Radiation—Mobile Ions and Particles: Both bipolar and MOS devices are affected by external radiation. For avionic applications, ionization and displacement damage in power semiconductor devices was observed due to the protons and electrons confined in the earth's magnetic field [34]. For terrestrial applications, a single event induced burnout can happen when heavy ions, also called cosmic rays, strike a device [43], [44]. Radiation-hardened materials and structures have been reported [34], [45].

8) Other Mechanisms for MOS-Gated Devices: Several mechanisms do not arise in properly constructed power MOS devices, though they cause failures in other type of semiconductor devices. These include the developing of slow trapping levels, microcracking of aluminium metallization, and electromigration of metallization (which can occur at high-current densities) [34].

Failures can be caused by more than one mechanism. The operating and environment conditions, and the device structures must be considered when examining a failure, which are as follows.

1) Gate oxide breakdown, related to the gate circuit and device structure. Particularly, vulnerable periods are during inductive switching, when overvoltage or rapid reapplication of voltage occurs due to excessive *dv*/*dt* [31], [46].
2) SOA failures for MOSFETs and IGBTs are normally caused by excessive thermal transients or poor heat sinking [13], [34], [47], [48], which may result from electrical stress, device structure or packaging issues. Examples of thermal failures are given in [49], with the destruction of an n-channel punch through IGBT in forward-biased SOA caused by the thermal disappearance of built-in potential between the n+ emitter and the p base. A similar case was reported in [50], where destruction was caused by thermal runaway.

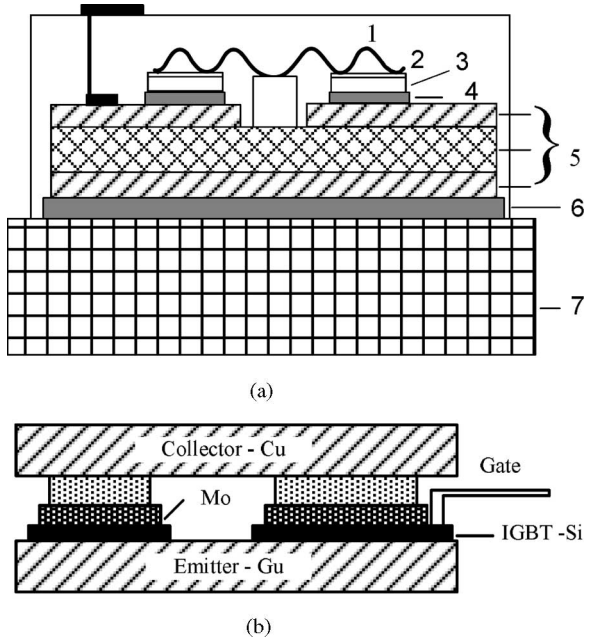


Fig. 4. IGBT packaging and structures. (a) Structure of an IGBT power module package [4]; 1: bond wire—Al, 2: chip metal—Al, 3: chip—Si, 4: die attach—solder, 5: DBC, 6: DBC attach—solder and, 7: base plate—Cu. (b) Structure of a PPI package [51].

Failure mechanisms on chips often interact with package-related failure mechanisms. These are thermally triggered and tend to be more significant, and are discussed in the next section.

D. Package-Related Failure Mechanisms

The failure mechanisms that are most frequently observed in power devices are due to the thermomechanical fatigue stress experienced by the packaging materials. (Humidity can also be a source of packaging degradation [119], although it is not covered here.) The main driving forces of such failure mechanisms are the mismatch in the coefficients of thermal expansion (CTE) of the different materials in the chip and package, and the local temperature swings to which they are subjected [27]. The two principal power device package types are compared first, followed by packaging failure modes.

1) Comparison of Packaging Types: Two packaging technologies, power modules and press packs, have been adopted for power devices. The cross-sectional structures of a power-module IGBT (PMI) and a press-pack IGBT (PPI) are shown in Fig. 4.

The power module is characterized by the chips (e.g. IGBTs, diodes, and MOSFETs) bonded to conductors on an insulating dielectric using solder. The dielectric, which provides heat conduction from the chips, is then soldered to a metal base plate, through which the heat flows to the external heat sink. The electrical isolation leads to straightforward heat sinking.

The press-pack structure, historically applied to thyristors and rectifier-grade diodes, is characterized by the device wafer or chips clamped under pressure to ensure uniform thermal and electrical contacts. The mountings must be electrically insulated externally.

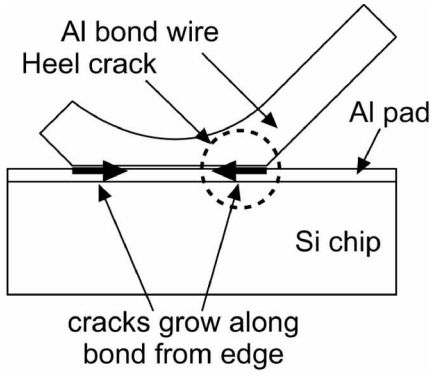
The press pack has an advantage in high-voltage series connected applications, which can survive after a short circuit fault, since a single device remains shorted due to the direct connection between the die and the metal contacts [52]. Therefore, PPIs have been developed in recent years to replace thyristors and gate turn-off thyristors (GTOs) in traction systems [53], [54], large motor drives [55]–[57], power systems [58]–[60], and pulsed power applications [61]. The reliability record for press-pack devices is much higher than power modules largely due to a better tolerance to thermal cycling: the press pack allows double-sided cooling to lower the thermal impedance [56], [62]. However, the cooling for the press-pack device relies on oil or another deionized liquid, to prevent the coolant from conducting current [62]. Contamination in the coolant may lead to electrical failures. For the PPI, during the formation of the conducting alloy and at later operation stages, molten aluminium (Al) attacking molybdenum (Mo) can form cracks in the base plate. The interaction of Mo particles with Si and Al over a period of time generates various intermetallics, reducing its conductivity and leading to further deterioration [58].

The more frequently used PMIs, on the other hand, are more susceptible to reliability concerns. These concerns arise from the connections between the chip, dielectric, and base plate. These principally consist of bond wire liftoff and solder fatigue, as described in the following sections.

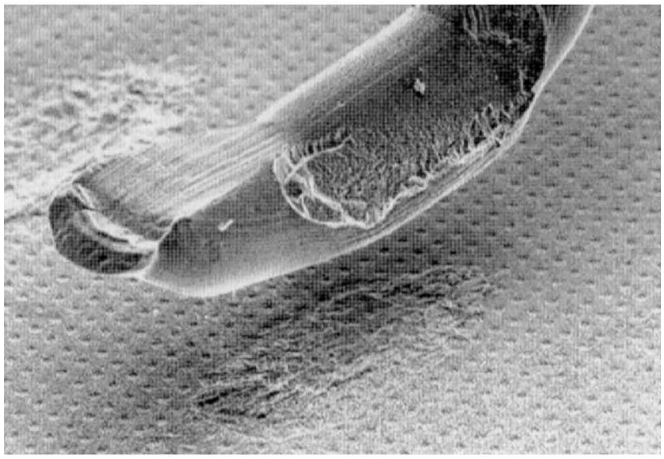
2) Bond Wire Liftoff: Bond failures are mainly caused by crack growth at the bond wire/chip interface due to temperature swings and the different CTEs between Si and Al [4]. The difference in strain in the two materials causes stress at the material interface; the resulting stress is dependent on the temperature. The resulting crack initiation and propagation is driven by stress–strain hysteresis energy loss as the temperature, and hence, stress cycles during operation. Fig. 5(a) shows typical crack propagation in a wire bond. In thermal fatigue testing with sufficiently high-junction temperature swings (ΔT_j), cracks propagate from both ends to the center along the small grain boundaries of Al wires. When the crack reaches the center, the bond wire lifts off [4], [22]. The bond wire liftoff failure mechanism is clarified by microstructural examination. An SEM image of a lifted bond wire can be seen in Fig. 5(b). Bond wire grain sizes are 5–15 μm at the bonding interface, since they do not grow during fatigue tests due to the restriction of the Al–Si film, and 100–300 μm at the center [63].

Bond wire heel cracking, as shown in Fig. 5, rarely occurs in advanced IGBT multichip modules, though it can be observed after long endurance tests, and especially in cases, where the ultrasonic bonding process was not optimized. Bond wire liftoff has been observed to affect MOSFETs, IGBTs, and freewheeling diodes [64], and is regarded as a principal failure mechanism for power electronics modules.

During tests, bonding wire liftoff can be electrically detected by measuring $V_{\mathrm{CE,sat}}$ under low IC conditions [65]–[67]. The criterion to detect bond-wire failure was a $+5\%$ increment of $V_{\mathrm{CE,sat}}$ [15], [68]. Since other failure mechanisms may also cause the increment of $V_{\mathrm{CE,sat}}$, microscopy techniques are often used offline to determine the exact cause [27].



(a)



(b)

Fig. 5. Bond wire liftoff due to crack growth. (a) Crack propagation causing bond wire liftoff, showing the heel crack. (b) SEM image of a lifted bond wire [4].

The observed failure mode can vary depending on the stress to which the devices are subjected. If the test is not interrupted after exceeding a predefined threshold, the failure mode during power cycling is the melting of the surviving bond wires. However, a frequently observed secondary failure mode, during high-voltage test or field operation, is the triggering of parasitics [27]. The parasitic effects related to the close inductive coupling between bond wires cause nonuniform current distribution between the wires, unbalanced transient current between paralleled chips, and the mechanical stress induced by the magnetic fields. These effects also contribute to the bond wire lift off [69].

Finally, recent work has observed annealing of bond wire interfaces at high temperatures during thermal cycling [93]. These annealing effects, which occurred in the wire during the high-temperature portion of cycling, were shown to remove some of the damage accumulated during the low-temperature portion, for a temperature change ΔT of more than 200 K.

3) Solder Fatigue: A major failure mode for power module is the solder fatigue and cracking between the module substrate and the base plate and/or the device chip and substrate [70]. Solder failures are related to the initial solder microstructure, substrate metallization, and intermetallic compounds [21], [71].

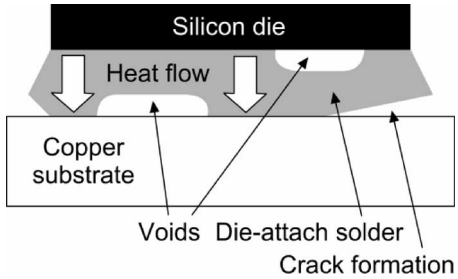


Fig. 6. Cracking and void formation in die-attach solder [80].

The mechanism arises because the silicon die and copper substrate have different CTE, resulting in a shear stress in the solder layer and eventually cracks (voids), as shown in Fig. 6. These voids reduce the effective area for heat to escape by conduction from the die; therefore, the die becomes hotter on average, and the process accelerates as the voids grow [27], [72]. The severe localized heating due to increased thermal resistance of the die attach can damage the chip [73], [74].

The strain and related stress in the solder arise from the difference in CTEs of the silicon and copper layers. The difference in strain—resulting from a temperature rise in the materials due to device heating—causes a net strain in the solder $\Delta\varepsilon$, and a resulting stress σ. In the case of solder, elastic, plastic, and creep-induced strain are all significant, with the total strain being the sum of these components. Therefore, the strain experienced depends on the applied stress, temperature, and because of creep and time. A partitioned model to describe the dependence of strain is given by [95], [129]

$$\Delta\varepsilon_t = \Delta\varepsilon_e + \Delta\varepsilon_p + \Delta\varepsilon_c \tag{2}$$

$$\Delta\varepsilon_e = \frac{\sigma}{E(T)} \tag{3}$$

$$(\Delta\varepsilon_p)^{n_1(T)} = \frac{\sigma}{k(T)} \tag{4}$$

$$\frac{d}{dt}(\Delta\varepsilon_c) = A\sigma^{n_2(T)} \exp\left(-\frac{E_a}{RT_m}\right) \tag{5}$$

where $\Delta\varepsilon_t$ is the total strain, $\Delta\varepsilon_e$ is the elastic strain, $\Delta\varepsilon_p$ is the plastic strain, $\Delta\varepsilon_c$ is the strain due to creep, and σ is the associated stress (in megapascal). E is the Young's modulus (in megapascal), and k, n_1, and n_2 are material constants, all of which depend on the temperature T (in kelvin).

In cyclic loading cases, where the materials are cycling thermally due to power cycling in the converter, the thermal cycles result in strain cycling and induced stress cycling in the solder. The crack length in the solder increases with the number of cycles N. After large numbers of cycles, the rate of crack length progression per cycle *da/dN*, increases as the hysteresis area increases in the stress–strain plot, as shown in Fig. 7. Thus, failure is approached rapidly at the end of the solder life as the crack acceleration increases. Section III-B2 describes in more detail modeling processes used in predicting fatigue life of solder layers.

4) Electrical Stress Effects: The effect of stress induced by packaging thermal expansion has been observed in experiment

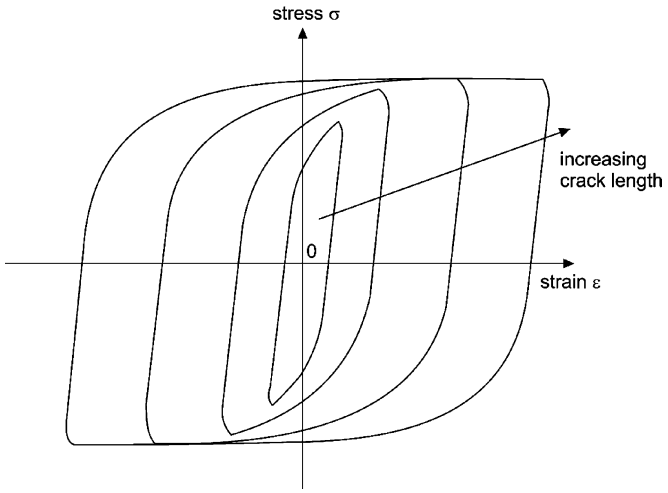


Fig. 7. Example of the hysteresis area increasing with crack length [95].

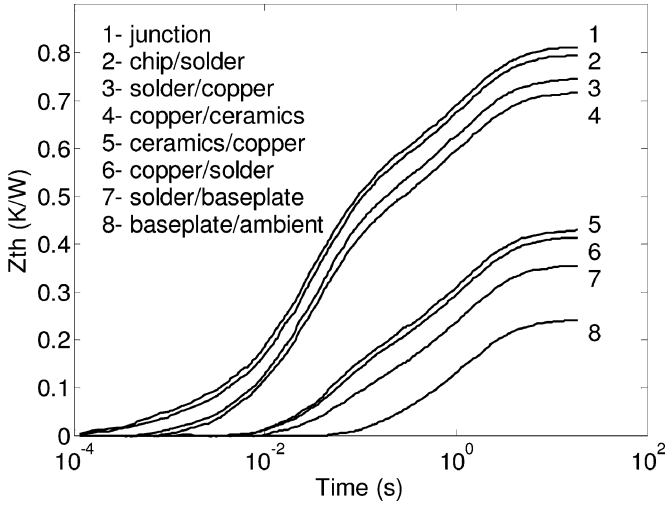


Fig. 8. Simulated transient thermal impedances of a MOSFET [77].

in [127] and in simulation in [128]. The experimental results in [127] have shown that the ON-state *I–V* curves of IGBTs depend on the applied stress (up to 400 MPa, both compressive and tensile), with about 10% change in ON-state voltage arising from a lateral (shear) stress on the device chip. The simulation results in [128] show that the electron mobility is the principal cause of lateral stress dependence of the IGBT electrical properties.

III. Reliability Modeling

Based on the knowledge of failure mechanisms, reliability models of power device packaging can be built to help in implementation of CM, failure analysis, and lifetime prediction without resorting to costly tests. However, such models require further development to ensure a wide applicability.

Modeling of the fracture mechanics and crack propagation within the bond wire and solder layer is a multidisciplinary problem. Purpose-built physical models, in conjunction with dedicated experimental procedures, are currently the only feasible approach [77]. Two steps are involved in reliability modeling as follows.

1) Electrothermal modeling of the device chip and packaging during a given load cycle, generating the temperatures throughout the load cycle.
2) Thermomechanical modeling of the packaging materials, predicting the accumulated damage and/or lifetime, dependent on the thermal cycling.

Silicon chip failures, such as time-dependent dielectric breakdown, negative-bias temperature instability, electromigration, and HCI, can be simulated using traditional electrical modeling techniques [40], [78], which are not reviewed here.

A. Thermal and Electrothermal Models

Prediction of the temperature throughout the packaging structure is required to estimate the thermomechanical stresses on the packaging materials. The temperature changes with the converter load can be predicted using thermal models of the packaging and electrothermal models of the converter.

Thermal models would employ 3-D finite-element method (FEM). The accuracy of such a model can be high. At present, however, complex 3-D finite-element simulation for the long transient thermal load cycles required for power electronic applications, lasting several minutes, are unfeasible because of the problem size [77].

A developed 3-D finite-element thermal model was recently demonstrated in [77]. The starting point of the procedure was a static 3-D finite-element thermal model of the converter, including the module and the heat sink [79], [80]. This model was initially calibrated with experimental data, acquired by infrared thermography or internal thermometry techniques. Once calibrated, the 3-D finite-element model was used to extract the thermal impedance of the system, as shown in Fig. 8. The drawback of this approach is that it requires a 3-D model of the packaging, which is difficult to develop.

Thermal equivalent networks are frequently used in electrothermal modeling of converters, and may be used easily in circuit simulators. Foster or Cauer networks are used to represent the thermal diffusion in the packaging. An example of a Cauer network is shown in Fig. 9; this is used to study the intermediate interfaces (e.g., solder layer), which may be helpful to assess the health condition of the solder attach. Foster networks are frequently given in device manufacturers' datasheets; although these are straightforward to extract, they cannot be combined with other thermal components in the packaging structure unless transformation to a Cauer network takes place beforehand [81].

A more compact method of modeling thermal effects in packaging has been developed recently in [82]–[84]. It uses Fourier series to model the thermal diffusion, which is possible if given the simple structure of packaging layers. They promise fast computation while maintaining sufficient accuracy for reliability estimation. They also avoid the need to extract *R–C* cell thermal equivalent circuit models from FEM simulations.

Ideally, any consideration of thermal modeling for packaging should include power device electrical behavior, given the strong coupling present in the device. To study the correlated electrical and thermal behavior of power devices caused by

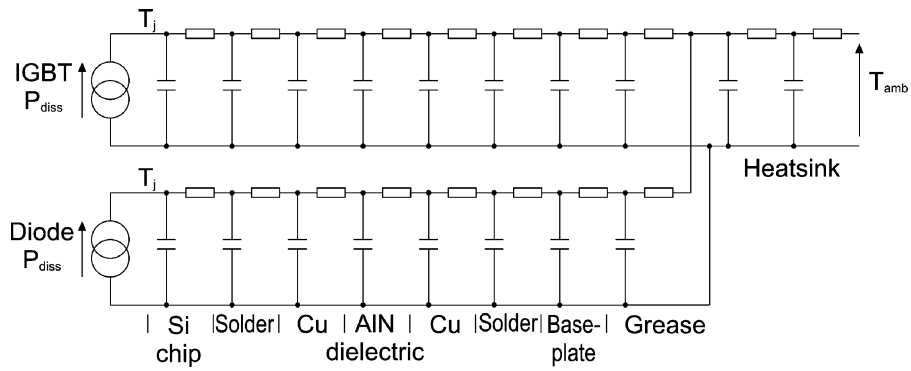


Fig. 9. Compact thermal model (Cauer network) for an IGBT/diode package.

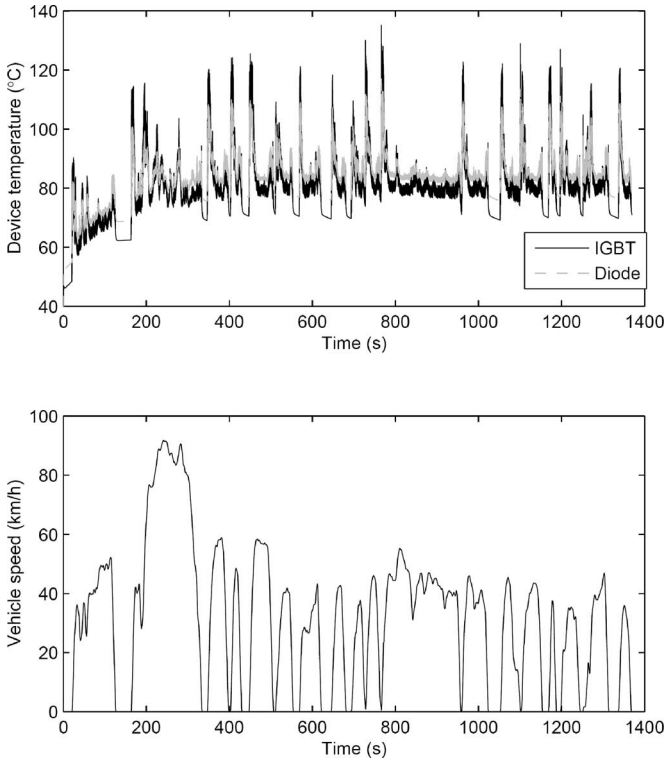


Fig. 10. Example of simulated device temperature using a fast device and converter simulation method [117]. The device temperatures in an electric vehicle drive converter are shown against the vehicle speed.

system level effects, electrothermal compact device models have been developed [85]–[88]. With these models, the transient junction temperature profile can be calculated, and the effects of ambient temperature, load cycle (e.g., driving style in automotive applications) and converter design on reliability can be investigated [84], [117]. This approach uses look-up tables of device losses to speed up simulation, decoupling device, and converter/thermal simulation. An example of the resulting simulated device temperature profile is shown in Fig. 10.

If the device model required does not need to be fully physics-based, a simpler approach can be used, where the switching and conduction losses can be estimated as simple mathematical functions of the inverter voltage and current. This approach was used to estimate the reliability of converters at the design stage in [120]–[122].

B. Thermomechanical Models

Thermomechanical models capture two principal failure mechanisms: bond wire liftoff and solder cracking. The stress and strain relationships within packaging are related to lifetime and reliability, and will be reviewed later.

1) Bond Wire Liftoff Thermomechanical Models: The equivalent strain amplitude $\varepsilon_{\rm tot}$ due to the temperature swing and the difference of CTEs during temperature cycling can be given by [4]

$$\varepsilon_{\rm tot} = \frac{(\alpha_{\rm Al} - \alpha_{\rm Si})\Delta T_j}{1-\nu} \tag{6}$$

where $\alpha_{\rm Al}$ and $\alpha_{\rm Si}$ are the CTEs of Al and Si, respectively (per kelvin), v is the Poisson ratio ($v = 0.345$ for aluminium in the elastic range), and ΔT_j is the junction temperature swing (in kelvin). For uniform cycling on a material sample, the Coffin–Manson law states that the number of cycles to failure N_f, is dependent on the cyclic strain $\varepsilon_{\rm tot}$

$$N_f \propto \varepsilon_{\rm tot}^{-n}. \tag{7}$$

Combining (4) and (5)

$$N_f \propto \Delta T_j^{-n}. \tag{8}$$

In practice, different exponents n apply to elastic and plastic contributions to fatigue, and the total strain for a given number of cycles is given by the sum of the two. Elastic strain dominates at low strain amplitudes and high numbers of cycles to failure, while plastic strain dominates at high strain amplitudes and low numbers of cycles to failure. Ultimately, it is plastic strain that causes damage accumulation due to the energy absorbed in hysteresis.

Experimental work suggests that the bond wire liftoff is a thermally activated mechanism and can therefore be expressed by an Arrhenius relationship [4]

$$N_f = A\Delta T_j^{-n} \exp\left(-\frac{E_a}{RT_m}\right) \tag{9}$$

where T_m is the mean temperature during cycling (in kelvin), and A and n are constants. The relationship in (7) can be plotted on log scales, as shown in Fig. 11 for the LESIT project data.

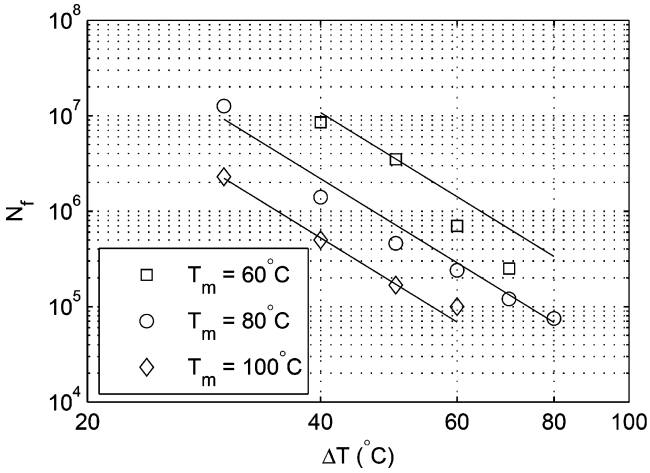


Fig. 11. LESIT results for different ΔT_j [4].

Bond wire liftoff is the result of cumulative damage occurring as a result of a set of different stress or strain levels. For such cases, the Palmgren–Miner linear cumulative damage rule, which assumes linear damage accumulation throughout the lifetime of the packaging, give the accumulated damage

$$D = \sum_{i=1}^{n} R_i = \sum_{i=1}^{n} \frac{N_i}{N_{fi}} \tag{10}$$

where R_i represents the fractional amount of damage produced in N_i mechanical reversals at a stress level i, and N_{fi} represents the number of reversals to failure at that particular stress level. The bond wire completely lifts off when $D = 1$. For nonuniform random cycling, as would be practically experienced, individual cycles must be counted for each combination of temperature range (ΔT_j) and mean temperature (T_m), accomplished by a rain flow counting process, as explained in [89].

A more detailed approach may be used to analyze the crack propagation in the wire bond itself. The Coffin–Manson law is used to predict crack initiation; once this occurs, the Paris law relates the crack propagation growth rate during cyclic loading to the amplitude of the stress intensity factor [76], [90]

$$\frac{da}{dN} = C\Delta K^m \tag{11}$$

where a is the crack length (in meter), N is the number of load cycles, C and m are material constants, and ΔK is the range of the stress intensity factor [91]. A simple form for K is given by [90]

$$K = \sigma\, a^{1/2} \tag{12}$$

where σ is the applied stress (in megapascal) [76], [92]. Given a, ΔK is determined as σ varies in a load cycle.

An example of using the Paris law to analyze bond wire liftoff is shown in Fig. 12. The remaining wire contact length L after cycles is equal to the original length L_0 subtracting the crack length *2a*. If L is not larger than the bottom limit value L_{critical}, the bond wire fails, i.e., lifts off.

The microstructural response of Al wire bonds to thermal cycling is complex, and is not adequately described in simple

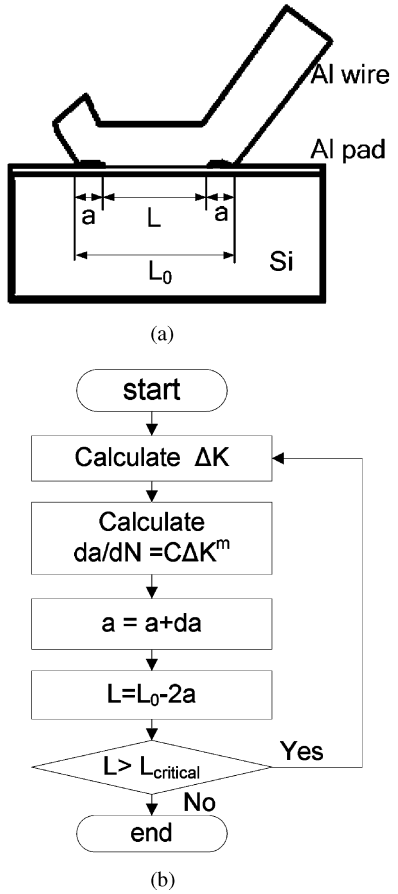


Fig. 12. Paris law flowchart for crack propagation [92]. (a) Bonding wire cracks. (b) Paris law for crack propagation.

thermomechanical models. At sufficiently high peak chip temperature ($T_{j,\max}$), approximately 170 °C, annealing is activated. This removes some of the damage accumulated; therefore, the earlier equations cannot accurately predict the actual damage. The damage accumulation and self-healing in cycling depends on the thermal range and $T_{j,\max}$ [93].

2) Solder Fatigue Thermomechanical Models: As shown in (3), solder fatigue depends on the creep strain $\Delta\varepsilon_c$ as well as the elastic and plastic strains $\Delta\varepsilon_e$ and $\Delta\varepsilon_p$, which are related to the number of cycles to failure, as explained earlier. For elastic deformation, Basquin's equation gives [32]

$$\frac{\Delta\varepsilon_e}{2} = \frac{\sigma_a}{2E} = \frac{\sigma_f}{2E}\,(2N_f)^b \tag{13}$$

where $\Delta\varepsilon_e/2$ is the elastic deformation in one reversal (i.e., one half-cycle), N_f is the number of stress reversals, σ_a is the stress amplitude (in megapascal), as shown in Fig. 7, σ_f is the fatigue strength coefficient (typically the true fracture stress) (in megapascal), and b is the Basquin exponent (typically between -0.12 and -0.05). For plastic deformation, the Coffin–Manson law gives

$$\frac{\Delta\varepsilon_p}{2} = \varepsilon_{pf}\,(2N_f)^c \tag{14}$$

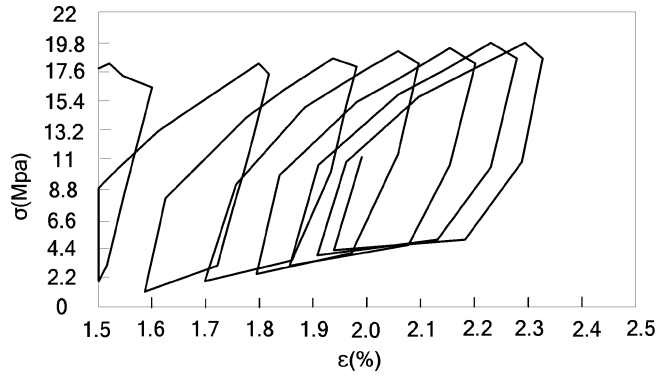


Fig. 13. Stress–strain plot for a mission profile [98].

where ε_{pf} is the fatigue ductivity coefficient [approximately 0.65/2 for eutectic solder (^{63}Sn^{37}Pb)] and c is the fatigue ductility exponent (for ^{63}Sn^{37}Pb, $c = -0.442 - 6 \times 10^{-4} T_m + 1.74 \ln(1 + 360/t_D)$, where t_D is the half-cycle dwell time [32]). Finally, the creep rate can be expressed with an Arrhenius law, since it is a thermally activated mechanism

$$\frac{d\varepsilon_c}{dt} = A\sigma^{n_2(T)} \exp\left(-\frac{E_a}{RT_m}\right) \tag{15}$$

where A and n are material-related constants.

A simple method of calculating the creep strain is not to relate it to the duration of the cycle, but simply to examine the number of cycles to failure, as in [76]. It should be noted, however, that this is a quasi-static model, so its applicability is limited. Summing the elastic, plastic, and creep deformations gives as follows:

$$\frac{\Delta\varepsilon}{2} = \frac{\Delta\varepsilon_e}{2} + \frac{\Delta\varepsilon_p}{2} + \frac{\Delta\varepsilon_c}{2} = \frac{\sigma_f}{2E}(2N_f)^b + \varepsilon_{pf}(2N_f)^c + \varepsilon_{cf}(2N_f)^d \tag{16}$$

where ε_{cf} is the fatigue ductility coefficient for creep deformation and d is the exponent. The main component of the strain is the creep strain and [94]

$$N_f = 0.159 \times (\Delta\varepsilon_c)^{-1.98}. \tag{17}$$

A more detailed model of solder creep and crack propagation uses the Paris law. A typical form is [76], [95], [96]

$$\frac{da}{dN} = C\Delta W^m \tag{18}$$

where ΔW is the plastic strain energy density (in joule per cubic meter), determined from the area within a stable hysteresis loop. With this method, the total plastic deformation work associated with a mission profile is used to estimate the lifetime. An example of plotting hysteresis loops to calculate the total plastic strain energy accumulated is shown in Fig. 13. The solder attach is assumed to reach its end-of-life as a total amount of deformation work W_{tot}, has been accumulated [77], [80], [97]. The main limitation is that, similar to Coffin–Manson approach, it fails to predict the decrease of the module lifetime when operated at high average temperatures [77].

A similar method is also used in [100], but simply relates the crack propagation rate *da/dN* to the accumulated plastic strain per cycle, $\Delta\varepsilon_p$

$$\frac{da}{dN} = a(\Delta\varepsilon_p)^b. \tag{19}$$

Simulation of the solder layer can elucidate the dependence of $\Delta\varepsilon_p$ on the mean and peak–peak temperatures in a thermal cycle T_m and ΔT, for example, in [100], this is given by a response curve, so that $\Delta\varepsilon_p = f(\Delta T, T_m)$. This approach then assumes that the number of cycles to failure N_L, for a given solder attach length L is simply given by

$$L = N_L \frac{da}{dN} \tag{20}$$

i.e., the crack length accumulates linearly, and therefore, Miner's rule can be used to estimate the accumulated damage when subjected to a random thermal cycle, as for the bond wire liftoff in Section III-B1. However, the work in [95] suggests that this is not the case, since the crack length propagation rate depends on the hysteresis area, and hence, number of cycles; therefore, for more accurate estimations of the solder fatigue life the dependence of *da/dN* on N may have to be accounted for.

C. Challenges in Reliability Modeling

The modeling approaches presented all provide an initial foundation for studying the thermomechanical packaging reliability. However, the crack initiation and propagation is complicated—nearly all models and equations require distributed parameters, such as stress, which is dependent on geometry, material, and load levels. Most studies, so far, have solved this problem by the aid of FEM, which requires lengthy simulation to calculate the thermomechanical behavior. One approach to avoid this is to use FEM of a particular packaging structure to build a look-up table of number of cycles to failure against temperature swing (ΔT_j), the mean temperature (T_m), and in the case of creep-dependent solder fatigue, the time duration of each cycle (Δt_d). Initial development of such an approach is given in [99], [100], and [124].

Although models for bond wire liftoff and solder cracking have been developed, they are only useful, where the exact packaging structure is known. Ultimately, a simple method of predicting the packaging lifetime is required. This should be obtainable from module parameters supplied by a device manufacturer and a characteristic thermal load cycle, calculated from both the application and modeling of the devices and converter. The nonlinearity present in packaging wear out, identified in [101], should also be considered. Little, if any, work has been carried out on developing such a complete packaging reliability model; this would integrate the bond wire liftoff and solder cracking models, and provide a complete description of the interaction between failure mechanisms.

IV. CM Power Electronics

Reliability modeling gives a tool of achieving a specified lifetime expectation as the converter design proceeds. This may reduce converter failure rate, but cannot prevent a catastrophic

failure from happening. In order to guarantee converter reliability during operation, a CM scheme can be implemented and the aforementioned modeling work can also be applied to inform the development of such a scheme. This allows warning to be issued of device deterioration. In this sense, CM serves as an aid in scheduling maintenance to extend the lifetime of the converter system. Like for rotating electrical machines and transformers, this is to capture weak signatures hidden in large signals during normal operation. Another challenge of CM power electronics is that the high-power density of a semiconductor device means that it will be difficult to embed sensors inside the device; it is more favorable to capture signatures in external measurements that are already used for converter control and protection. Furthermore, the operating condition of a converter is likely to vary, accompanied by loss and temperature excursions. As explained earlier, most failure mechanisms have a thermal aspect, so the masking effect of normal load variation must be addressed.

To develop a CM scheme, the effects of semiconductor device degradation on its terminal characteristic and converter performance should be understood. In principle, CM can be implemented through the following three ways, though they may be combined, to capture and interpret the corresponding signatures.

1) Device parameters indicative of the degradation. For an IGBT, these include ON-state voltage or resistance $V_{\mathrm{CE,sat}}$ or R_{ON}, threshold gate voltage $V_{\mathrm{GE,th}}$, and internal thermal resistance R_{th}. These parameters, which are difficult to measure in practice, may in turn cause changes in the operational characteristics at a device or converter system level. The latter may be more practical to capture for the purpose of CM.
2) Dedicated sensors embedded in the device can be used to directly monitor the occurrence and the level of physical degradation, for example, *in situ* mechanical stress monitoring using strain gauges and bonding wire lift off detection through localized electrical resistance measurement within a device or module.
3) Model-based CM is particularly attractive to converter systems working under variable load and ambient conditions, such as in electric vehicles and renewable energy systems. It is expected that the response of the converter system to the stimulus—applied externally or available internally during normal operation—is dependent on the device condition, and degradation can be detected by comparing the measured response to that predicted by a healthy model.

All of the possibilities have not been fully explored as CM of power electronics is still in the infant stage of development. This paper reviews the techniques experimented so far and comments on their characteristics and the need of further development. It has been attempted to capture the change of device ON-state voltage (V_{ON}) (measured through $V_{\mathrm{CE,sat}}$ or R_{ON}) to detect bond wire liftoff. It has also been attempted to capture the change of device internal thermal resistance R_{th} to indicate solder cracking; the temperature rise for a given set of power loss and ambient conditions can be used to extract R_{th} indirectly. These are the techniques currently under intensive development, while dedicated sensor-based and dynamic model-based techniques are also being actively studied.

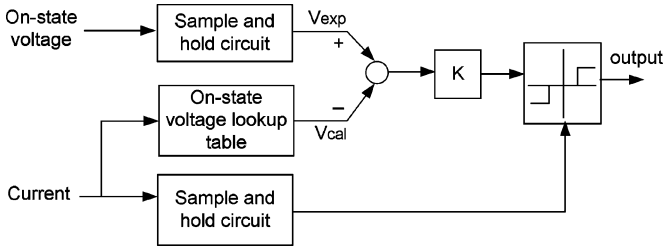


Fig. 14. On-state voltage monitoring [102].

A. On-State Voltage-Based CM for Bond Wire Liftoff Detection

Research has shown that there are detectable changes in R_{ON} or $V_{\mathrm{CE,sat}}$ of a device, IGBT or diode, after long-time power cycling and this has been related to the bond wire liftoff mode of packaging degradation [65], [101]–[103], [114].

In [102], a unit was used in an intelligent power module (IPM) to periodically monitor the device's ON-state voltage and current, which are sampled simultaneously, as shown in Fig. 14. For a given current value, the measured ON-state voltage is compared against a value saved in a look-up table. The deviation is used as an indication of the integrity of the bond wires and the level of deterioration due to power cycling.

A quasi real-time IGBT failure prognostic system based on monitoring the $V_{\mathrm{CE,sat}}$ variation at specific current and temperature was reported in [103], which was designed for application in an electric vehicle. An IGBT is considered to be seriously degraded if its measured $V_{\mathrm{CE,sat}}$ has increases by 15% or more of its normal reference value. While the ON-state voltage can be measured using additional specially designed sensing circuits [107], it was noted as very difficult to guarantee the accuracy because of the relatively small value of the ON-state voltage and the dramatic change of the measured voltage before and after switching transient. Moreover, practical issues need to be taken into account, including electrical isolation, cost, and the physical dimension of the sensing circuit integrated with device or converter. The method is applied only at the cold startup of the electric vehicle with a known starting current, in order to avoid additional current measurement and the effect of variable operating point. This gives the reason of the "quasi real-time" nature of the method. Effect of the ambient temperature is taken into account through temperature measurement.

A monitoring method was proposed in [114] by detecting the change of the ON-state resistance R_{ON} of a MOSFET in a digital-controlled forward converter switch-mode power supply (SMPS). Measurable operating parameters of the converter—the input and output voltages, switching duty ratio, and load current—were processed to derive R_{ON}. Although this is not generally applicable because in some systems, the output voltage signal may not be available, it gives an example of indirect monitoring of the ON-state resistance. Further work could be carried out to develop an online identification method for the ON-state voltage or resistance without measuring the high-frequency PWM voltage waveform. For example, in a PWM inverter induction motor drive, the equivalent resistance of an inverter-leg viewed by the machine can be comparable to the

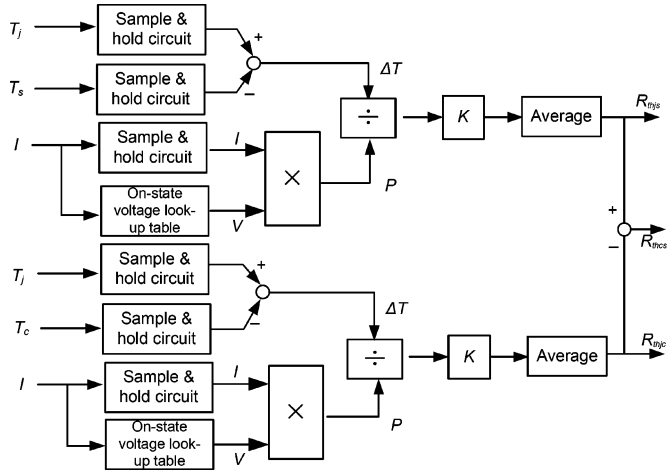


Fig. 15. Integrated power module monitoring unit [102].

stator resistance of the induction machine. The change of $R_{\rm ON}$ will affect the electromagnetic transients in the system, which can, in turn, be measured to detect the original change of resistance; the decaying time constant of a transient component in the stator flux linkage is dictated by the total resistance present on the stator side. It is likely to be necessary to further include the effect of temperature variation in the inverter and machine.

B. Thermal Resistance and Temperature-Based CM

Solder fatigue causes variation of thermal resistance value $R_{\rm th}$ of the device [104]. A thermal resistance-based technique is potentially suitable for monitoring solder fatigue inside the packaging of a power module. A criterion that has been used to define solder failures is a $+20\%$ increment of $R_{\rm th}$ [15], [68].

However, the challenge is to obtain the internal temperature information and correlate this with the device power dissipation in the module. Additional sensors are embedded in the power module and mounted on heat sink to measure the temperature over an extended period of time in [102]. The data, together with the corresponding load current recorded, are then postprocessed to calculate the thermal resistance associated with different parts of the package, achieving CM when change of thermal resistance is detected.

The proposed monitoring unit for an IPM is shown in Fig. 15, where the junction temperature T_j, case temperature T_c, heat sink temperature T_s, and device current I are measured periodically. The device voltage drop is obtained through a look-up table using the measured current, facilitating power loss calculation. The thermal resistances $R_{\rm thjc}$ (junction to case), $R_{\rm thjs}$ (junction to heat sink), and $R_{\rm thcs}$ (case to heat sink) are then calculated. The result data are stored to study the trend and determine the occurrence of solder interface degradation. In systems, where the switching frequency is high, a more accurate power loss calculation including device-switching losses will be necessary. Inclusion of scaling factor K allows calibration of the scheme in practical applications with instrumentation errors, e.g., $\pm 0.2\,^{\circ}$C for thermocouples.

As shown earlier, junction temperature T_j during operation is critical in monitoring the condition of a power device, but is most difficult to measure directly. Without using an integrated sensor in the device, techniques have been developed to measure the electrical quantities, which are sensitive to the junction temperature:

1) The junction temperature can be determined when the current is reduced to a low value, say 100 mA, by measuring the corresponding voltage drop. A linear relationship between the voltage drop and junction temperature is observed for a particular IGBT [65]
$$T_j = 0.595 \times V_{\rm CE} + 0.523 \tag{21}$$
where T_j is the junction temperature (in degree centigrade) and $V_{\rm CE}$ is the IGBT voltage drop (in volts) at 100 mA.
2) As temperature rises, the gate threshold voltage $V_{\rm GE,th}$ has been found to decrease at the rate of approximately 6–9 mV/K. This rule applies to both power MOSFETs and IGBTs at low and high temperatures [34], [105].
3) A technique is presented in [25] and [28], which uses dI_C/dt and the $dV_{\rm GE}/dt$ measurements to define a transconductance g_m (in mho) as a thermosensitive parameter, for the measurement of the static and of the transient average junction temperature in IGBT devices

$$\begin{aligned} g_m &= \frac{dI_C/dt}{dV_{\rm GE}/dt} \\ &= \frac{1}{1-\alpha_{\rm p\text{-}n\text{-}p}(T)}\left[\mu(T)C_{\rm OX}\frac{W}{L}\left(V_{\rm GE}-V_{\rm threshold}(T)\right)\right] \\ &= f(T) \end{aligned} \tag{22}$$

where $\alpha_{\rm p\text{-}n\text{-}p}(T)$ is the current gain of the p-n-p transistor structure within an IGBT, which is temperature dependent, $\mu(T)$ is the electron (channel) mobility (in centimeter square per volt per second), dependent on temperature: $\mu(T) = 1350 \times (T/300)^{-2.42}$ when $T \geq 200$ K [106], $C_{\rm OX}$ is the oxide capacitance (in farad per centimeter square), and W and L are the channel width and length, respectively (in centimeter). Note that the transconductance would typically be given as a function of temperature T in the form of a look-up table.

The first two techniques are simple with proven accuracy in laboratory experiments, but they may not be easily implemented in practical converters. The third is more suitable for online application. However, dI_C/dt could be affected by the presence of temperature-compensated gate resistors, which are used in some cases to improve the current sharing between paralleled IGBTs. Measurements are usually affected by noise, so several readings must be averaged to reduce the experimental error to an acceptable level.

It has been indeed crucial to obtain junction temperature to derive the internal thermal resistance; the error needs to be limited within $1\,^{\circ}$C because the maximum junction temperature rise due to solder fatigue targeted by CM would only be about $10\,^{\circ}$C. Given the limitations of the aforementioned indirect techniques, there is obviously room for improvement and the necessity for new methods. However, the change of external characteristics, e.g., case or heat sink temperature, could be used to monitor

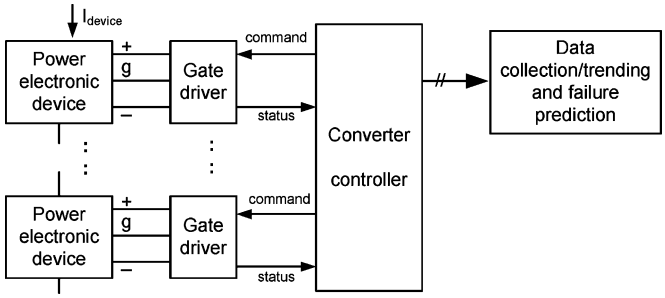


Fig. 16. CM technique based on switching time [108].

solder fatigue because the rise of junction temperature is to increase the total power dissipation, and hence, increase the overall temperature. The external temperature can be easily measured, but the difficulty lies in understanding the electrothermal interaction, and the masking effects of a variable operation and other mechanisms of degradation, such as bond wire liftoff.

One other method worthy of mention involves that of estimating the device temperature rise in real time using measurements of the inverter conditions, e.g., rms current, rms voltage, and base plate temperature [124]. Power losses are estimated in real time, and in conjunction with compact thermal models, used to estimate the junction temperature of devices in real time. Cycle counting methods, as in Section III-B1 [89] are then used to estimate the accumulated damage and provide a suitable signal indicating the health of the converter. However, this relies upon the device power loss and thermal models giving sufficiently accurate estimates of the chip temperatures.

C. Switch-Time-Based CM for the Power Device and its Gate Driver

Switch-time degradation is a known problem of IPMs, which if detected can signify several failure mechanisms [108].

1) Partial failure of a multichip device can result in longer switching times for a given current, due to the increases in current density, and consequently, stored charge.
2) Higher T_j can also cause prolonged switching, resulting from factors related to degradation, such as increased leakage current, elevated $V_{\mathrm{CE,sat}}$ due to bond wire liftoff, and higher R_{th} due to solder fatigue or loss of cooling.
3) Gate driver circuit degradation can extend the switching time, since it may be affected by more than one power supply incorporating capacitors and electronic components, which may degrade with time.

A monitoring technique, shown in Fig. 16, uses the switch time [108]. During normal operation of a converter, thousands of switching events can be measured every second. The regression of these measurements can produce a very high-resolution, time-averaged, and noise immune signature for each power device and gate driver pair.

The technique was initially applied in a GTO converter, where the GTO has long switch times, around 10 μs. In an IGBT or MOSFET converter, the direct measurement of switching time, often in the range of 10–500 ns, is not practical. However, an indirect technique of switch-time measurement could broaden the application. For example, it is known that the device switching characteristics will largely dictate the level of high-frequency electromagnetic interference emissions in a converter system [109], [110]. Techniques may be developed to provide adequate sensitivity to enable CM. A change in the *dv/dt* by 100% during the switching transient will cause a variation of some high-frequency signals in the system by 6 dB, which can be practically detected, taking background noise into account.

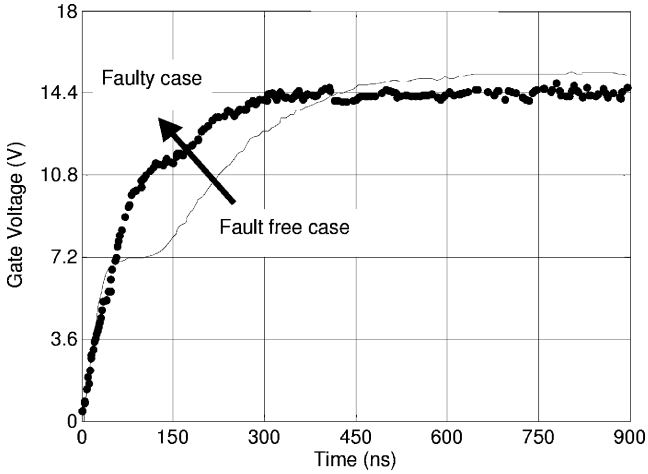


Fig. 17. Fault detection based on gate voltage monitoring [111].

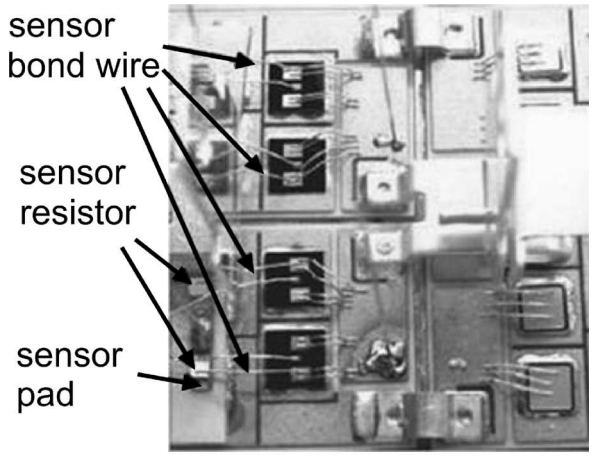
D. Gate-Signal-Based CM for Gate Degradation

A method to detect a short-circuit fault in an IGBT was recently proposed in [111] and was based on the gate voltage waveform during turn ON. It is assumed that the degradation of device modifies the gate charge distribution. Experimental results reproduced in Fig. 17 indicate the significant variation of the gate signal profile in the presence of IGBT short-circuit fault. It is not clear yet how to detect the difference between the gate signals in a fault free and a faulty device, but the two traces are distinctively different in terms of the level and duration of the Miller gate plateau. It was considered possible to set thresholds to discriminate natural aging from a short-circuit fault, implying that the method may also be developed for CM purposes. However, the aging effects need to be further understood.

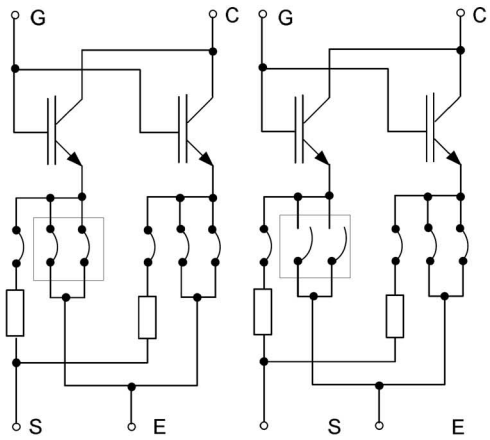
A limitation of this technique is that the gate voltage signal is required by additional measurement, which must provide high-sampling resolution in order to capture the Miller Plateau. For CM, where immediate shutdown of the converter is not necessary, it is envisaged possible and more suitable to convert the gate voltage waveform using analog electronics, such as an integrator into a charge signal that changes with the operating point and the device degradation condition. Although each switching event is brief and contribute only a little to the result, a number of consecutive switching events accumulate resulting in a noticeable signature.

E. Sensor-Based CM for Bond Wire Liftoff

Semikron presented a sensor-based approach in 2003 to detect bond wire liftoff in an operating IPM [65]. As shown in Fig. 18,



(a)



(b)

Fig. 18. Emitter bond wire liftoff detection for IGBTs in parallel [65]. (a) Modified IGBT module. (b) Equivalent circuits without (left) and with (right) emitter bond liftoff.

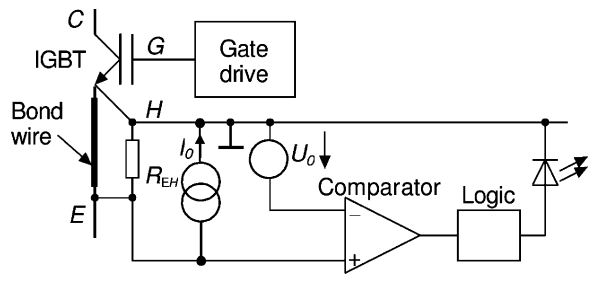


Fig. 19. Sensor-based CM technology [112].

the emitter bonding arrangement is tailored to allow the insertion of a subcircuit for instrumentation. The resistance between S and E is monitored and an increase signifies the occurrence of a bond wire liftoff.

A technique for early detection of bond wire liftoff in an IPM is shown in Fig. 19, which employs a resistor $R_{\rm EH}$ connected in parallel to the emitter bond wires to sense any increased voltage drop across the primary bond wires [112]. The physical spacing between E and H is typically 0.1 mm. A constant current I_0, e.g., 100 mA is applied to the resistor $R_{\rm EH}$. The voltage drop across $R_{\rm EH}$ is a function of the bond degradation. If the voltage drop exceeds a value U_0, a warning will be flagged.

Sensor-based CM technology for power electronics is reliable and accurate. However, there is no doubt that the modification of the assembly and of the direct-bonded copper substrate (DBC) layout, the additional sensors and monitoring circuits will increase the complexity and the cost of the power device chip or module. In practice, its applicability needs to be carefully evaluated by taking many factors into account, such as physical dimension, power dissipation, cost, and system reliability.

F. System-Identification-Based CM

In theory, degradation of a power device will affect the system response. Therefore, it is possible to monitor device condition based on system identification techniques [113], [114].

A technique was outlined in [113] for detecting the failure of precursors in the optical isolators in SMPS. The isolator is a two-port device that provides feedback for voltage regulation with gain governed by its transfer characteristics. The current transfer ratio (CTR)—the quotient of the output voltage and the input current—is used to monitor the degradation of the optical isolator. When the CTR falls below a critical threshold value, the circuit ceases to regulate and the output voltage begins to drift upward.

Before the failure point, the health of the optical isolator can be monitored from the observation of the crossover frequency, which will decrease as CTR is reduced, as shown in Fig. 20. This technique is confirmed with oscilloscope traces showing output voltage transients with a load current spike of 5 A [113].

It has recently been shown that CM is indeed possible in switching power converters with the aid of system identification [114]. In this example, the health condition of the capacitors was monitored. The monitoring system was experimentally validated on a 90 W, 50–15 V forward converter with field-programmable gate array (FPGA) control, in which the output filter capacitance was adjusted to vary the stability margin, indicating the degradation or failure of the capacitors. The shift of the frequency response can be used to monitor the degradation of converter stability margins, which may lead to a system level failure. Apart from the degradation of the output filter capacitor, other parametric variations that can result in potential system instability can be used to provide an early warning to local or system level controllers.

System-identification-based CM can be implemented without additional sensing points and with minimal additional digital hardware. However, the following are critical to the success of this technique.

1) Correlation between some specific failure modes and the system characteristic changes must be demonstrated.
2) Advanced signal processing algorithms are usually required, increasing the demand on computing hardware.
3) High-frequency noise attenuation is necessary.

Finally, neural networks have been proposed as a means of CM. In [125], such a neural network was applied to a diode rectifier. The rectifier was simulated, with changes made to

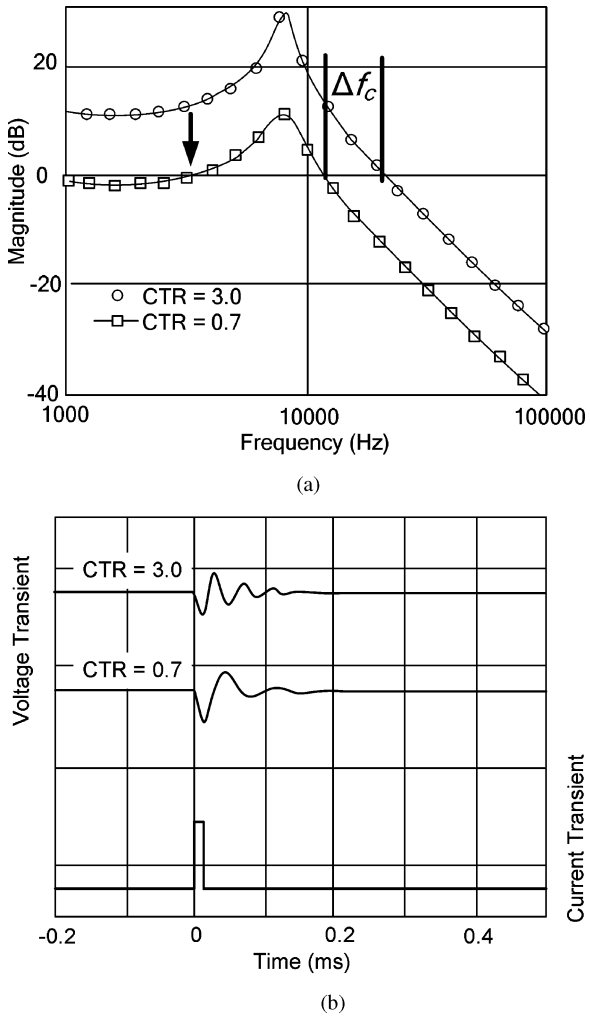


Fig. 20. CTR CM for optoisolator [113]. (a) Shift in crossover frequency due to a decreased CTR. (b) Voltage response to current impulse with two different CTRs.

capacitor ESR, diode knee (turn-ON) voltage, diode resistance and diode reverse recovery time, and the response of the neural network observed. It could clearly detect all the component changes, with the exception of a low sensitivity to the diode resistance. The method does, however, require suitable training data. This paper appears to be at an early stage, but could be a promising method of CM.

V. Discussion on Reliability and CM

Power electronics reliability is clearly an area with much active research. Semiconductor devices are, as shown in Fig. 3, significant triggers of system failures. A fault often results from the combined effects of interrelated failure mechanisms. With the evolution of semiconductor technology, the relative importance of failure mechanisms may also change. For example, lead-free technology has given rise to new issues that were not important in the past [115], [116]. The exploration of failure mechanisms is a long-term task that will inform the development of CM techniques.

A. Device Reliability

Device reliability is a main concern in power electronic converters. Those in traction applications suffer some of the greatest thermal stresses, and also require high reliability. This is borne out by the number of projects, discussed in Section II-B. The fact that IGBT modules are now used throughout the rail and automotive traction industries shows that these projects have been successful in addressing much of the original concern.

The chip-related failure mechanisms are largely irrelevant to CM. They generally involve random failures or external triggers—including overload conditions—and cannot be predicted, although CM techniques may be used to "trap" the failure events as they occur if its response is fast enough. The packaging-related failure mechanisms are, however, critically important for power devices. Although modern device packages may now be considered reliable, the modeling of packaging reliability is still an embryonic area of research. The individual failure mechanisms of bond wire liftoff and solder fatigue have thermomechanical models developed for them, as discussed in Section III, but these require further work in the following areas.

1) *Nonlinearity:* The interaction of wear-out mechanisms and the nonlinearity of damage accumulation are still not modeled by any of the existing packaging models. The results presented in [101] are a clear example of what needs to be modeled.
2) *Simple packaging models:* The models developed to date require a large quantity of information, such as the variation of the number of cycles to failure with temperature swing and peak–peak temperature for the packaging being modeled, the solder characteristics, the packaging dimensions, etc. Engineers designing power electronic converters will not want—nor need—to know such information, and the goal is for manufacturers to offer a few parameters from which a reliability model can realistically be built. This would allow engineers to predict the reliability at the design stage given the thermal behavior of the converter during use.
3) *Combined thermal models:* Obtaining the thermal behavior of the converter during use is another hurdle. Converter models of the type outlined in [85] and [117]—albeit with a range of accuracy—would be ideal to simulate such device temperatures. Integration of electrothermal converter models with the reliability models would create a package for converter designers to examine, where the tradeoffs in converter design could be improved.

B. CM Techniques

Apart from power device modeling techniques, the development of practical CM techniques is also necessary. Table I lists the advantages and disadvantages of the CM techniques discussed in Section IV. They can be roughly classified into internal sensor based and model based: the former ones may imply hardware requirement and the latter ones may have enormous calculation burden [118].

The limitations of existing techniques are significant and have largely prevented the wide application of CM for power

TABLE I
COMPARISON OF DIFFERENT CM TECHNIQUES

Methods	Advantages & Disadvantages
$V_{CE,sat}$, R_{on}	pros: highly related to degradations cons: difficult to measure small variations
R_{th}	pros: solder degradation detectable cons: difficult to measure T_j
Gate signal	pros: electrical fault detectable cons: high real-time requirement
Switch-time	pros: gate drive failure detectable cons: short switch time measurement needed
Sensor-based	pros: reliable and accurate cons: *DBC* layout modification
System identification	pros: no additional hardware modification cons: difficult correlation & complicated algorithm

electronics reliability. Considerable further research is needed to improve the techniques, particularly to increase their sensitivity and to reduce their cost. Because of the very tight space available in a module, the fast-switching transient and the relatively insignificant change of device characteristics due to degradation, the research has to address a series of challenges regarding sensor techniques and signal processing.

Measurement of electrical variables, such as $V_{\mathrm{CE,sat}}$ and R_{ON}, can be carried out externally, but the sensitivity needs to be very high because they are extremely small as compared to the OFF-state voltage and resistance. In practical conditions, the period during which such quantities and other electrical variables, such as gating signal and switch time, is very short. Special circuits are required to carry out the measurement. As reviewed earlier, efforts have been traditionally orientated in this direction. It is perhaps also worthy trying to capture the collective effect of such variations over a significant period of time, for example, the effect on converter efficiency and level of harmonics or electromagnetic (EM) emissions. Such ideas have been known and attractive to some researchers, but little research has been performed to prove or disprove them. However, effort on the measurement of thermal variables has mainly targeted the challenge of capturing T_j and internal temperature distribution in the module. While this is important because most devices are eventually damaged by excessive junction temperature, the root cause of a failure may not be effectively detected at an early stage and internal measurement is likely to be costly.

CM techniques without using internal sensors are indeed highly desirable. However, derivation of internal information from external measurements requires understanding of the relationship between the device condition and measurable system performance. The variable operating condition of a converter system makes it difficult to achieve CM using system identification. The electrical and thermal time constants in the system extend from microseconds to many minutes, adding to the difficulty of a model-based approach. Furthermore, the measurement environment for CM is usually noisy, requiring careful arrangement of external instrumentation and a large amount data acquisition for the purpose of error reduction. Very little research has been carried out in this respect. This approach would be particularly suitable for capturing the long-term effect of device degradation instead of information contained in an individual switching state. The efficiency effect and harmonic or EM emission signatures are apparently ideal for such an approach, but the changes in load or environmental conditions must be adequately represented in the model. The review of power device aging to failures and progress in device reliability modeling indicate that such an approach would be possible.

To improve sensitivity and credibility of CM, a common practice is to combine different techniques and adapt to the response of the CM system in the early period of its operation. Knowledge of the relationship between the parameters required by different methods and the various device failure mechanisms is important to eventually guarantee the effectiveness of such a combined approach.

C. Complete Condition and Reliability Monitoring

The developments in reliability modeling and CM techniques are so far currently not integrated. The reliability models are not directly applied to inform CM, since they address the prediction of reliability at the design stage, not in actual converter use. The CM techniques are reactive, in that they simply measure the condition of the packaging, and do not indicate the health—they simply flag whether a variable has exceeded a predetermined threshold. What is required here is a combined approach, i.e., predictive CM employing both CM and measurement techniques with reliability prediction.

The reason this is required is due to the nature of mission-critical systems. If a CM system identifies that a measurement variable exceeds its threshold, there is no indication of how imminent the actual failure may be. In some systems, the converter could run at reduced power or—in a multiple-converter system, such as distributed rail traction—switch OFF to give a "limp home" function. However, in other applications, running at anything below full power is not allowed until the next maintenance period. What is required, therefore, is a system for estimating whether the converter (i.e., device packaging) will survive until the next maintenance period, and this requires an integrated reliability model. This model would need to be of the same accuracy as those for design, but with the added proviso that it effectively observes the damage accumulation indirectly detected by the CM system. This would give a powerful method for guaranteeing the operational reliability of critical converter-based systems.

VI. CONCLUSION

CM is becoming increasingly important for power electronics, and has attracted much interest. As reviewed in this paper, efforts have been made in the following relevant areas: power device failure mechanisms, reliability modeling, and CM. Some key points are summarized as follows.

1) Power semiconductor devices are critical components to examine when considering power electronic converter reliability.
2) Thermomechanical fatigue is the dominant wear-out mechanism in modern IGBT-based power converters.

3) Electrothermal converter and packaging reliability modeling approaches are being developed, giving a solid foundation for design; however, they require significant further work to be used directly by converter design engineers.
4) CM techniques have been developed in earlier work, using a variety of techniques. However, further efforts should be made to improve their performance. First, the understanding of the failure mechanisms and effects should be enhanced. This work should be extended from the level of power electronics device itself to the system level. With the knowledge of system terminal characteristics degradation, CM without using sensors which have to be embedded in the module might be a realistic and promising approach in the future if it could provide adequate performance regarding sensitivity and self-adaptability.

Ultimately, a combined approach to reliability and CM will be beneficial. This combines CM and measurement techniques with reliability modeling to give reliability prediction and prognosis for systems in service. The potential application of such a system could deliver a step change in guaranteeing the reliability of mission-critical systems.

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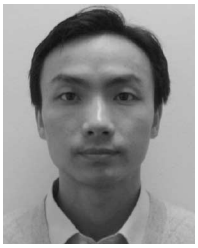

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