A Fast Voltage Clamp Circuit for the Accurate Measurement of the Dynamic ON-Resistance of Power Transistors

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***Abstract*—For determining the dynamic ON-resistance $R_{\mathrm{dyn,on}}$ of a power transistor, the voltage and current waveforms have to be measured during the switching operation. The novel heterostructure wide-bandgap (e.g., AlGaN/GaN) transistors inherently suffer from the current collapse phenomenon, causing the dynamic ON-resistance to be different from the static. Measuring voltage waveforms using an oscilloscope distorts the characteristics of an amplifier inside the oscilloscope when the range of the measurement channel is not set wide enough to measure both ON-state and OFF-state voltage levels, resulting in failure to accurately measure the voltage waveforms. A novel voltage clamp circuit improving the accuracy of the transistor's ON-state voltage measurement is presented. Unlike the traditional clamping circuit, the presented voltage clamp circuit does not introduce delay caused by RC time constants, keeping the voltage waveform clear, even during state transitions of the device under test. The performance of the presented circuit is illustrated by measurements on a 2-MHz inverted buck converter.**

***Index Terms*—Accuracy improvement, charge trapping, current collapse, dynamic ON-resistance, heterostructure wide-bandgap transistors, measurements, voltage clamping.**

I. Introduction

THE reduction of losses in power converters is indisputably one of the most important issues in the field of power electronics. Next to the optimization of the efficiency of a power switching converter, cost minimization is also of great importance [1]–[4]. The losses in a power switching converter are present both in the passive and in the active elements. In [5] and [6], the losses in a high-power dc/dc converter are reduced by an optimal design of the planar transformer. In [7]–[9], the switching losses are reduced by a soft-switching strategy. Despite previous efficiency-enhancing techniques, the conduction losses still represent a large part of the total losses. In particular, the ON-resistance of the transistor, which is directly linked to the conduction losses, needs to be as low as possible [10], [11]. Therefore, accurate measurement of the ON-resistance is indispensable. Recently developed high-voltage semiconductor switching devices frequently perform high-speed switching operations, and the static ON-resistance calculated from dc measurements is not sufficient as a guideline to predict the conduction losses. The reason for this is that the ON-resistance is determined by the junction temperature, which is unknown. In addition, heterostructure wide-bandgap semiconductor transistors [12] (e.g., AlGaN/GaN devices) are subject to a phenomenon known as current collapse, which is also called charge trapping [13]–[16], and this causes the ON-resistance to be dependent on the voltage that the transistor has to withstand during its OFF-state.

The ON-resistance of a transistor after applying high-voltage swings to the drain of the device under test (DUT) in its OFF-state is further referred to as the dynamic ON-resistance $R_{\mathrm{dyn,on}}$. It can be obtained by dividing the voltage and current waveforms during the ON-state.

When measuring the voltage waveform, the measurement range on the oscilloscope must be set wide enough, in order to measure both ON-state and OFF-state voltage levels. If this is not the case, then the characteristics of amplifiers inside the oscilloscope are distorted, due to a phenomenon known as "Oscilloscope Overdrive" and the lack of recovery thereof, resulting in failure to accurately measure the ON-state voltage [17, Ch. 24]. An 8-bit analog-to-digital converter in an oscilloscope provides $2^8 = 256$ quantization levels to discrete an analog signal. If the transistor switches between 0.1 and 400 V, then this gives a resolution of about $400/256 = 1.56$ V, resulting in completely inaccurate values of the ON-state voltage, which may even be perceived as negative because of the large quantization error. In recently developed GaN heterostructure semiconductor devices, this problem is even more pronounced because these devices exhibit a much lower ON-resistance for the same blocking voltage than silicon devices, and can therefore be downscaled with respect to traditional components, allowing them to switch faster [18]–[21]. This means that, for wide-bandgap devices, an even higher measurement resolution is required and that measurements should be performed with faster circuitry.

Conventional circuits partially solve this problem by clamping the OFF-state voltage to a lower value [22]. However, they introduce problems such as voltage peaks, measurement offset, and delays due to RC time constants. These problems get worse with increasing switching frequency and decreasing switching times, resulting in failure to accurately measure the voltage waveform.

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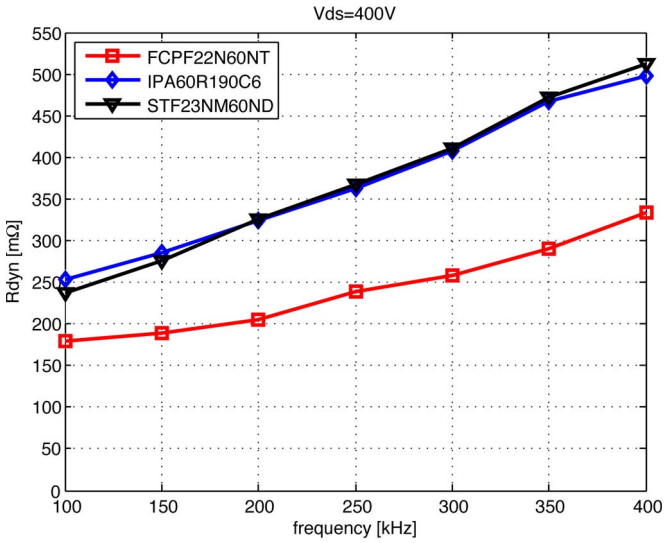

Fig. 1. Dynamic ON-resistance of different superjunction MOSFETs versus switching frequency ($V_{DS} = 400$ V, $I_{DS} = 4$ A, $V_{GS} = 12$ V).

To address these problems, a novel voltage clamp circuit is proposed, which improves the accuracy of the ON-state voltage waveform measurements. Unlike traditional clamping circuits, the presented voltage clamp circuit does not introduce delay caused by RC time constants, keeping the voltage waveform clear, even during state transitions of the DUT. The circuit is presented in [23], but in this paper, the parameters influencing the performance and operation of the circuit are thoroughly investigated. Recommendations are given for the selection of high-voltage diodes. A new power converter is built to test the circuit performance at higher switching frequency (2 MHz). A new state-of-the-art circuit has been found in the literature and is investigated in this paper. The state-of-the-art circuits are built and measured to confirm their advantages and disadvantages.

The circuit presented in this work is, in the first place, intended to measure the dynamic ON-resistance of heterostructure wide-bandgap semiconductor switches. Due to the charge-trapping effect, as mentioned earlier, the ON-resistance is dependent on the OFF-state voltage, and therefore might differ a lot from the static ON-resistance. However, there is also a second application, in which the circuit of this work is useful. Fig. 1 shows measurement results performed with the presented voltage clamp circuit for different superjunction MOSFETs not suffering from the charge-trapping effect, in function of the switching frequency. The higher the switching frequency, the higher the switching losses and thus the temperature increase of the measured device. This results in an increase of the ON-resistance. Since the junction temperature is unknown, the static ON-resistance listed in the components' datasheets cannot be used to determine the conduction losses. The presented voltage clamp circuit is capable of measuring the ON-resistance of a device while switching at high frequencies, and therefore, allowing one to determine its conduction loss. Furthermore, in all applications where the voltage has a pulsation behavior and where only the low voltage level should be measured accurately, and it is of no importance that the high level is clipped to a lower value, the circuit of this work can be applied. In all cases, the measured devices are treated as a black box, with the device parasitics accounted for in the measurements.

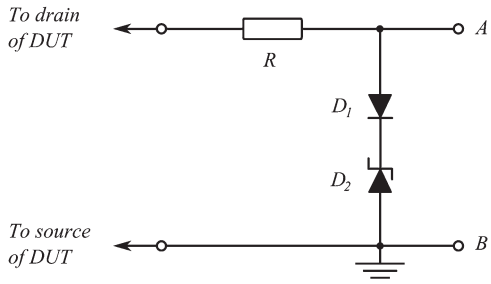

Fig. 2. State-of-the-art circuit I.

In literature, there are only a few references [16], [22], [24], [25] that have extracted the dynamic $R_{\mathrm{dyn,on}}$ of transistors. Moreover, clear illustrations of both the applied measurement method and the circuit are rarely given. Therefore, the authors conducted this work and deemed that a paper dedicated to this subject would be of value. The proposed circuit can be built inside oscilloscopes or measurement units, meaning the circuit has immediate industrial or scientific value.

This paper is organized as follows: three conventional circuits, which are also employing the voltage clamping principle, are first explained and discussed to illustrate their disadvantages with respect to the novel measurement circuit of this work. Then, the novel circuit is presented and assessed using simulations and measurements. The measurement accuracy is determined, both analytically and through simulations. Next, the most important factors for mitigating voltage peaks in the clamped voltage are experimentally evaluated. Finally, the influence of temperature on the measurement accuracy is evaluated.

II. State-of-the-Art Voltage Clamp Circuits

A. State-of-the-Art Circuit I: Based on a Zener Diode

The first voltage clamp circuit is shown in Fig. 2. The circuit is connected to the drain and source terminals of the DUT. The measurement of the drain-to-source voltage waveform is performed with an oscilloscope by placing a voltage probe between output nodes A and B. During the OFF-state, the drain voltage of the DUT is high (e.g., 400 V) and the voltage between the output nodes A and B (V_{out}) is clamped to a level equal to the sum of the voltage drop across diode D_1 and the Zener voltage across Zener diode D_2. The sum of these voltage drops is called the clamping voltage. The main reason for using diode D_1 is to reduce the total series parasitic capacitance of diodes D_1 and D_2.

The value of the clamping voltage must be chosen greater than the ON-state voltage of the DUT. Hence, diodes D_1 and D_2 will not clamp the drain-to-source voltage during the ON-state, and the measured voltage V_{out} between points A and B will be equal to the ON-state voltage of the DUT.

Note that the highest measured voltage V_{out} is the clamping voltage. Consequently, the measurement range of the oscilloscope may be set to a value wide enough to measure the

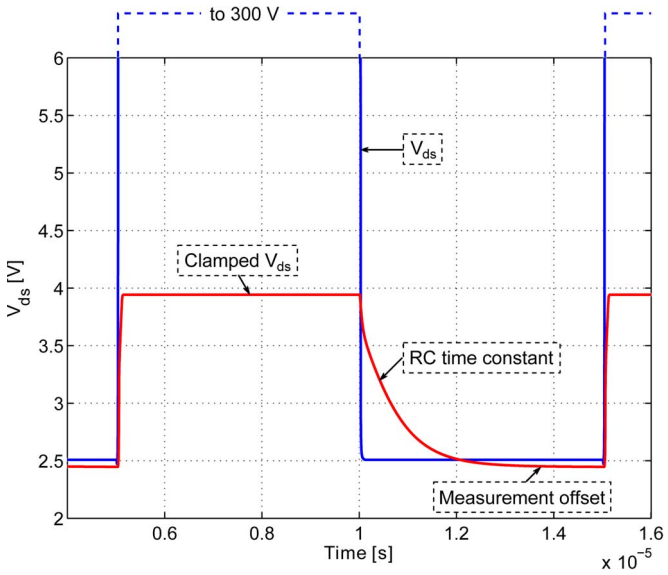

Fig. 3. Simulation results of circuit I (100 kHz), $D_1 = 1N4148$, $D_2 = BZV85C3V6$, $R = 200$ kΩ, switch = IRF840, 2.97 A, 300 V.

clamping voltage instead of the high OFF-state drain-to-source voltage. This results in an increase of the measurement resolution, with respect to a direct measurement with a factor, as follows:

$$\text{Resolution improvement} = \frac{V_{\text{pp,off}}}{V_{\text{pp,clamped}}} \tag{1}$$

where $V_{\text{pp,off}}$ is the peak-to-peak value of the drain-to-source voltage during the OFF-state, and $V_{\text{pp,clamped}}$ is the peak-to-peak value of the clamped drain-to-source voltage.

However, this circuit has some disadvantages. Fig. 3 shows that, during the ON-state, there is a current flowing through the resistor R, resulting in a voltage drop across it. This current is the sum of the leakage currents through the clamping diode and the measurement probe. Although the leakage currents are small, the high resistance value will lead to a significant voltage drop across R. Therefore, the measured voltage at the output of the circuit, between the points A and B, will be the ON-state voltage minus a voltage drop across R. The measurements, performed under the same conditions as for the presented circuit, show a voltage drop across the resistor R of a few hundred millivolts, depending on the value of R.

There is also an RC time constant caused by the resistor R and the parasitic capacitances of diodes D_1 and D_2, and of the measurement probe. Due to this time constant, the output voltage of the clamping circuit will only gradually decrease to the real ON-state voltage, causing a measurement delay. To counter this problem, the resistance value of R could be reduced, or probes and diodes with a low capacitance could be employed. However, to limit the power dissipation of R, which shows a maximum during the OFF-state of the device and is then equal to $(V_{ds} - V_{\text{clamped}})^2/R$, the resistance value should not be chosen too low.

Furthermore, the value of R also depends on the current, which has to flow through D_2 in order to achieve correct Zener operation. Typically, for many Zener diodes, a current of a couple of milliamperes is required. Due to these disadvantages, this circuit cannot be used to measure the ON-resistance during high-speed switching operation. The circuit can only serve for low frequencies, typically a few tens of kilohertz up to 100 kHz.

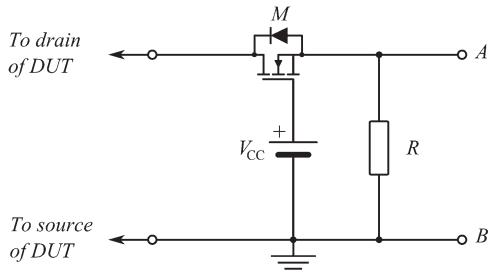

Fig. 4. State-of-the-art circuit II.

B. State-of-the-Art Circuit II: Based on a Transistor

A second voltage clamp circuit is described in the U.S. patent application 2008/0309355 A1 and depicted in Fig. 4. It is connected to the drain and source terminals of the DUT. The output voltage (V_{out}) of the circuit is measured between the nodes A and B using a voltage probe. Transistor M is a normally-on-type field-effect transistor with a negative threshold voltage (e.g., -2 V). In the patent, transistor M is a wide-bandgap normally-on-type transistor. The gate of transistor M is connected to a positive dc voltage supply V_{cc}.

During the OFF-state of the DUT, a current flowing through the resistance R will cause a voltage increase at the source terminal of transistor M. When the gate-to-source voltage of transistor M decreases below its threshold voltage (e.g., $V_{\text{th}} = -2$ V), transistor M is turned off. At this point, a voltage equilibrium will be established, and the output voltage V_{out} will be clamped to the clamping voltage $V_{\text{clamp}} = V_g - V_{\text{th}} = 4$ V. This allows the range of the oscilloscope to be zoomed in to a range wide enough to measure V_{clamp}, thus increasing the measurement resolution. When the DUT is turned on, the source voltage of transistor M decreases, causing the gate-to-source voltage of transistor M to become higher than its threshold voltage, bringing the transistor into conduction. As a result, the ON-state voltage of the DUT is measured at the output of the circuit. For a clamping voltage of, e.g., 4 V, the measurement accuracy is $4\text{ V}/2^8 = 0.0156$ V, using an 8-bit resolution oscilloscope. For an ON-state voltage of 0.1 V, this allows a sufficiently accurate measurement.

This circuit has a few disadvantages. First, the simulations in Fig. 5 show that, when the DUT switches off, the output voltage V_{out} is increased above V_{clamp} (V_{out} peaks) due to the parasitic drain-to-source capacitance of transistor M. These voltage peaks increase with the value of the resistance R and can be several times the clamping voltage V_{clamp}. Consequently, this will cause the oscilloscope overdrive phenomenon, resulting in failure to accurately measure the voltage waveforms. To prevent this, the range of the oscilloscope has to be set to a range wide enough to capture the voltage peaks, which decrease the measurement resolution. Moreover, the voltage peaks at the source of transistor M (also equal to V_{out}) will cause its gate-to-source voltage V_{gs} to become more negative than allowed (V_{gs}

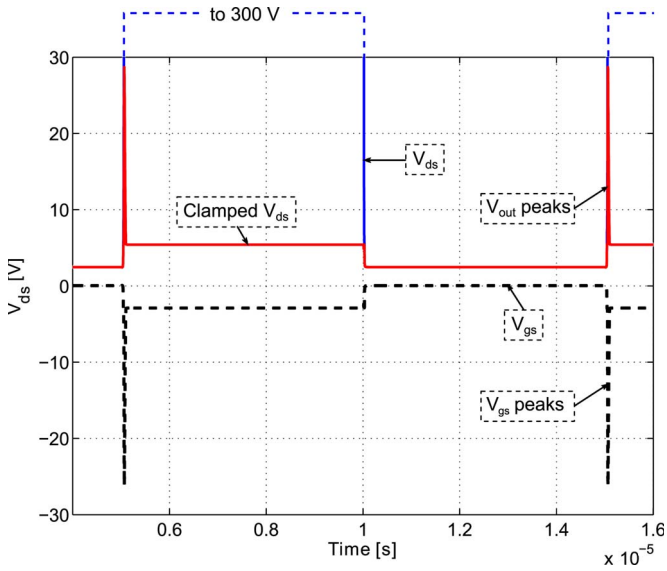

Fig. 5. Simulation results of circuit II (100 kHz), M = GaN [26], $R = 50\ \Omega$, $V_{cc} = 2.5$ V, switch = IRF840, 2.97 A, 300 V.

peaks), which might lead to its destruction. However, this can be solved by putting a series of fast switching diodes, between the source and the gate of transistor M, with a total forward voltage drop larger than the threshold voltage.

Second, to reduce the voltage peaks, the value of the resistance R has to be taken as small as possible. However, during the ON-state of the DUT, transistor M is turned on, and due to the resistance R, a small current flows through M, causing a voltage drop across it. This will introduce an error on the measurement. The error can be significant if the value of the resistance is taken too small. Additionally, there is a power dissipation in the resistance R, which can be up to 1 W.

Third, during the transition to the OFF-state of the DUT, there is a large dv/dt across its capacitance C_{gd}. Therefore, a large current will be flowing through the voltage supply V_{cc}, which might lead to its destruction.

The transistor used in the patent 2008/0309355 A1 is a wide-gap normally-on-type field-effect transistor (see Fig. 4). However, the circuit can also operate if a regular normally-off-type field-effect transistor is used. This is achieved by increasing the supply voltage V_{cc} by a few volts (e.g., $V_{cc} = 8$ V). For a threshold voltage of $V_{th} = 4$ V, this gives a clamping voltage of $V_{clamp} = V_{cc} - V_{th} = 4$ V.

C. State-of-the-Art Circuit III: Combination of I and II

In [22], another voltage clamp circuit is described, which can be seen as a combination of the first two circuits. It is shown in Fig. 6. It is connected to the drain and source terminals of the DUT, and the output of the circuit is the voltage between the nodes A and B. Basically, the circuit consists of a normally-off-type field-effect transistor M (IRF620 in [22]) connected to a Zener diode D_3 (5.1 V) in series with a resistor R_2 with a low resistance value (10 Ω). The transistor is biased at a constant voltage V_{cc} of between 6 and 8 V. The exact value of this voltage is chosen, so that the voltage peaks in the clamped

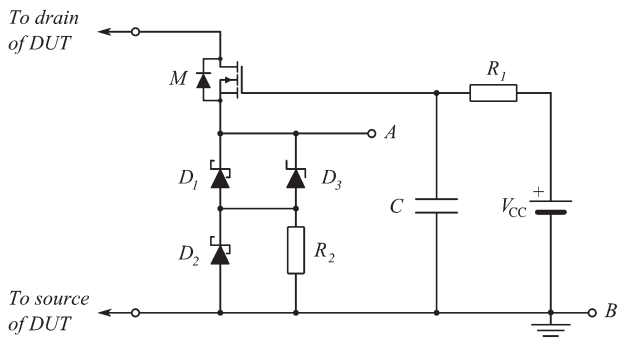

Fig. 6. State-of-the-art circuit III: combination of I and II.

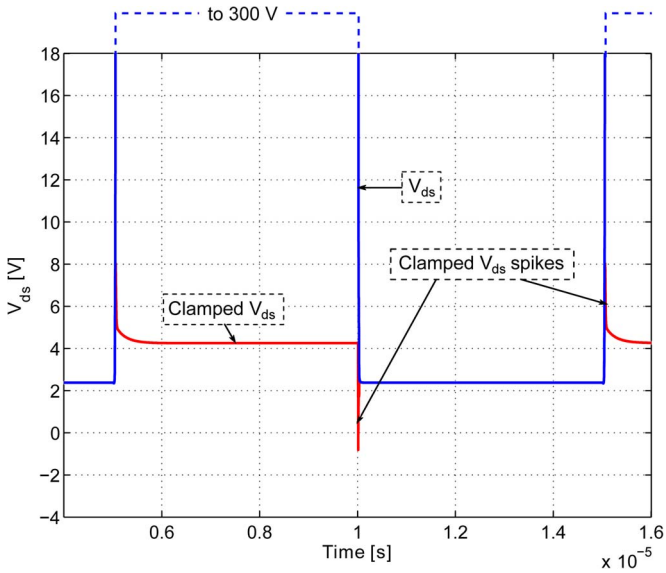

Fig. 7. Simulation results of circuit III (100 kHz), $D_1 = D_2 =$ 1N4148, $D_3 =$ 1N4733, $R_1 = 20\ \Omega$, $R_2 = 10\ \Omega$, switch = IRF840, 2.82 A, 200 V, $V_{cc} = 8$ V, T = IRF620, $C = 10$ nF.

voltage are minimal. If the DUT is off, the potential at node A is clamped, according to the same operating principle as circuit II, to a voltage $V_G - V_{th}$ because of the presence of the Zener diode D_3, where V_G is the potential at which the gate of M is biased and V_{th} is the threshold voltage of M. If the DUT is on, then M is also on, and the ON-state voltage appears across points A and B.

In Fig. 7, simulation results at 100-kHz switching frequency are shown. It can be also shown that the circuit performs well at 2 MHz.

However, this circuit has disadvantages. The large drain-to-source parasitic capacitance of transistor M leads to high voltage peaks at the node A, during the switching transitions of the DUT. The Schottky diodes D_1, D_2 and the Zener D_3 together with the resistor R_2 are used to reduce these voltage peaks. However, these components introduce a leakage current leading to a voltage drop across transistor M. The measurements, performed under the same conditions as for the presented circuit, show a voltage drop across transistor M up to 160 mV.

Transistor M should carry the high voltage that the DUT also carries, and thus has a large size, implicating that the parasitic

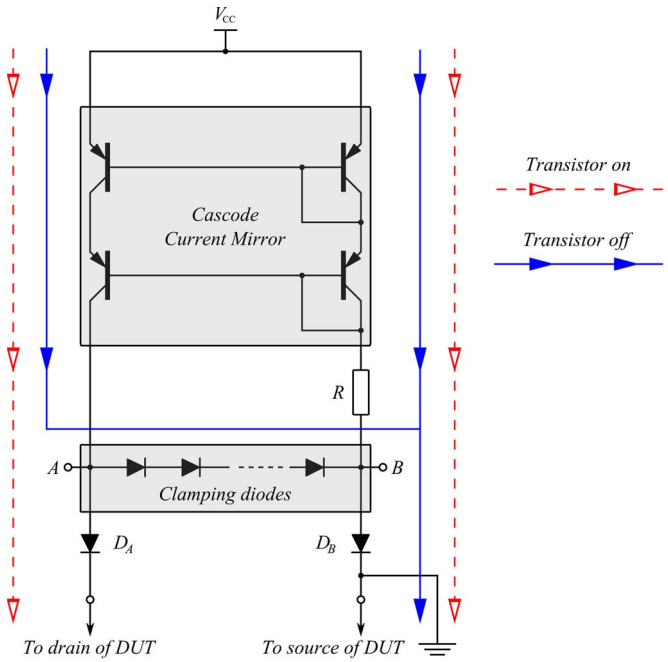

Fig. 8. Presented voltage clamp circuit with current flows during the ON- and OFF-states of the transistor.

drain-to-source capacitance has a large value. In the circuit presented in this work, i.e., the novel voltage clamp circuit, no MOSFETs are used in the clamping circuit, i.e., only diodes, having a lower parasitic capacitance. This is beneficial for the voltage spikes in the clamped voltage. Therefore, there is no need to use extra components that lead to leakage current and voltage offset. To give a numerical example, with data available in the components' datasheets, compare the parasitic diode capacitance of the BAS21J diode, i.e., $C_{\text{parasitic}} \approx 2$ pF at 0 V, with the drain-to-source capacitance of the IRF620 MOSFET: $C_{ds} \approx 70$ pF at $V_{gs} = 0$ V and $V_{ds} = 25$ V. Circuit III does not suffer from an RC-delay, but it introduces a voltage offset, which is not the case for the proposed circuit of this work.

Moreover, during the transition to the OFF-state of the DUT, there is a large dv/dt across the gate-to-drain capacitance C_{gd} of M. Consequently, if C_{gd} is large, a large current will be flowing through the voltage supply V_{cc}, which might lead to its destruction, as is the case in circuit II.

Nevertheless, circuit III has the advantage that no differential voltage probe should be used to measure the output voltage, unlike the novel proposed circuit of this paper.

III. Novel Voltage Clamp Circuit

In Fig. 8, the voltage clamping circuit of this work is presented. It consists of a current mirror circuit, two high-voltage diodes D_A and D_B having the same I–V characteristic, and a series connection of one or more clamping diodes connected between the points A and B. The circuit is connected via the high-voltage diodes to the drain and source terminals of the transistor of which the ON-state voltage or the dynamic ON-resistance is to be evaluated. The mirror circuit provides two equal currents, hereafter referred to as mirror currents. The value of these currents is determined by the resistance R, the supply voltage V_{cc}, and the forward voltage drops across the current mirror transistors, as shown in Fig. 8. The mirror circuit can have any kind of topology, for instance, a Wilson current mirror, but in the figure, a cascode mirror is shown. Wilson or cascode current mirrors have the advantage that the Early effect of the two upper bipolar junction transistors (BJTs) is avoided and that the output resistance has a very high value. The output of the voltage clamp circuit is the voltage V_{out} between the points A and B. Therefore, the voltage should be measured with a differential probe and an oscilloscope.

During the ON-state of the DUT, the drain-to-source voltage is low, and the mirror currents flow through the high-voltage diodes, as shown in Fig. 8 with the dashed lines. They do not flow through the clamping diodes. The potential at node A is then the sum of the voltage drops across D_A and the drain-to-source voltage of the DUT. The potential at node B is the voltage drop across diode D_B. Due to the fact that the mirror currents are equal and the diodes D_A and D_B have equal I–V characteristics, the voltage drops across D_A and D_B are the same, and the voltage between A and B is equal to the ON-state voltage of the DUT.

During the OFF-state of the DUT, the left mirror current cannot flow through diode D_A anymore because the drain-to-source voltage of the DUT is high. Therefore, the left mirror current is forced to flow through the series connection of clamping diodes, as indicated by the solid line in Fig. 8. The output voltage is thus the clamping voltage V_{clamp}. In the design of the circuit, the clamping diodes or their number should be chosen, so that the clamping voltage is higher than the ON-state voltage of the DUT. Since the output voltage V_{out} is limited to at most the clamping voltage V_{clamp}, the range of the oscilloscope may be set to one wide enough to measure V_{clamp}, therefore improving the measurement resolution.

Note that reversely connected Zener diodes can be also used as clamping diodes. They usually have more internal capacitance than forward-conducting Schottky diodes or small-signal diodes and hence are not preferred.

The presented voltage clamp circuit has a high measurement accuracy. Current mirrors typically exhibit a high current accuracy of $\pm 0.5\%$ (see, for example, the REF200 current mirror from Texas Instruments). When the mirror currents have, for example, a nominal value of 60 mA, in the worst case situation, the real mirror currents are 60.3 mA and 59.7 mA. In case two high-voltage BAS21J diodes are used, a PSpice simulation reveals that this will result in a difference between the voltage drops across the high-voltage diodes D_A and D_B of about 0.983 mV. When the ON-state voltage of the DUT is, for example, 1 V, this means that the measurement error is at most 0.1%.

Fig. 9 shows simulation results of the presented circuit. The simulation is done at a switching frequency of the DUT of 100 kHz, with a cascode mirror circuit of BC557C BJTs, a V_{CC} of 10 V, a series connection of five BAV3004W clamping diodes and the same high-voltage diodes, and $R = 100\,\Omega$. In the simulation, there are no voltage peaks at the output, during the transition to the ON-state. However, during the transition to the OFF-state, a voltage peak of about 6.53 V can be observed, which is still much less than the voltage peaks observed in

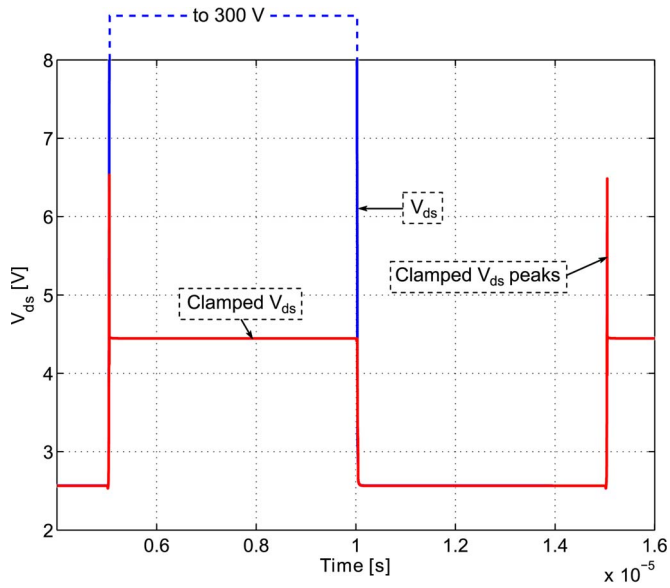

Fig. 9. Simulation results of the presented circuit (100 kHz), $D_A = \mathrm{BAV3004W} = D_B$ = clamping diodes, series connection of five clamping diodes, $V_{cc} = 10$ V, $R = 100\ \Omega$, switch = IRF840, 2.974 A, 300 V.

the state-of-the-art circuit II. This voltage peak is caused by the parasitic capacitance of diode D_A and can be minimized by choosing a better diode. For the best performance, a diode should be chosen with the lowest parasitic capacitance and limited reverse recovery.

The main advantage of the presented voltage clamp circuit is that it does not introduce delay caused by RC time constants, keeping the voltage waveform clear, even during state transitions of the DUT. In addition, there is no offset in the output voltage V_{out}, due to a voltage drop across a resistor or MOSFET in the clamping circuit, as was the case in state-of-the-art circuits I, II, and III.

IV. Quantifying the Accuracy of the Measuring Circuit

In a previous paragraph, a numerical example illustrated the accuracy of the voltage clamp circuit. Making use of the relationships between voltage and current of diodes, an expression for the absolute and relative errors can be derived. Referring to Fig. 8, it is assumed that diode D_A is a p-n diode, conducting a current of I and having a junction at temperature T. Diode D_B is a p-n diode, conducting a current of $I + \Delta I$, having a junction at temperature $T + \Delta T$. Suppose that the saturation currents I_0 of both diodes are the same. The absolute error ϵ of the ON-state voltage is then the difference of the two p-to-n voltages of the diodes, as follows:

$$\epsilon = V_{\mathrm{pn},A} - V_{\mathrm{pn},B}.$$

For p-n diodes, the relationship between p-to-n voltage and diode current is

$$I = I_0(e^{V_{\mathrm{pn},A}/(nV_{t,A})} - 1) \tag{2}$$

$$I + \Delta I = I_0(e^{V_{\mathrm{pn},B}/(nV_{t,B})} - 1) \tag{3}$$

with $V_{t,A} = kT/q$ and $V_{t,B} = k(T + \Delta T)/q$. Therefore, the error is

$$\begin{aligned}\epsilon &= V_{\mathrm{pn},A} - V_{\mathrm{pn},B} \\ &= \frac{nkT}{q}\ln\left(\frac{I}{I_0} + 1\right) - \frac{nkT}{q}\ln\left(\frac{I + \Delta I}{I_0} + 1\right) \\ &\quad - \ldots \frac{nk\Delta T}{q}\ln\left(\frac{I + \Delta I}{I_0} + 1\right) \\ &= \frac{nkT}{q}\ln\left(\frac{\frac{I+I_0}{I_0}}{\frac{I+\Delta I+I_0}{I_0}}\right) - \frac{nk\Delta T}{q}\ln\left(\frac{I + \Delta I}{I_0} + 1\right).\end{aligned}$$

Neglecting I_0 with respect to I, we find

$$\epsilon \approx -\frac{nkT}{q}\ln\left(1 + \frac{\Delta I}{I}\right) - \frac{nk\Delta T}{q}\ln\left(\frac{I + \Delta I}{I_0} + 1\right).$$

Making use of the Maclaurin series of the natural logarithm $\ln(1 + x) \approx x,\ x \to 0$, we have

$$\begin{aligned}\epsilon &\approx -\frac{nkT}{q}\frac{\Delta I}{I} - \frac{nk\Delta T}{q}\frac{V_{\mathrm{pn},B}}{nkT/q} \\ &\approx -\frac{nkT}{q}\frac{\Delta I}{I} - \frac{\Delta T}{T}V_{\mathrm{pn},B}.\end{aligned} \tag{4}$$

At 300 K, with $\Delta I = 0.6$ mA, $I = 59.7$ mA, and for two BAV21 diodes that are held at the same temperature and have an emission coefficient of $n = 2.854$,[1] we find an absolute error of

$$\epsilon \approx -\frac{2.584 \cdot 1.38065 \cdot 10^{-23} \cdot 300}{1.602 \cdot 10^{-19}}\frac{0.6}{59.7} = -0.671\ \mathrm{mV}$$

approximating the value simulated by PSpice, stated earlier, well.

V. Measurement Results

As mentioned earlier, the measurement of the ON-state voltage waveform is necessary to determine the dynamic ON-resistance $R_{\mathrm{dyn,on}}$. The following measurements were performed using a Tektronix TDS 5054 500-MHz oscilloscope, a Tektronix P5100A 500-MHz voltage probe, a Tektronix P6251 1-GHz differential probe, and a LEM PR50 Universal 50-MHz current probe.

The measurements are done on an inverted buck converter [27], [28] and the presented voltage clamp circuit (see Fig. 10). The circuit is built very compactly to reduce the parasitics in it. The voltage clamp circuit consists of a cascode current mirror built with two BCV62B components in series. The provided current is adjusted through the supply voltage and the resistance R (see Fig. 8). For the high-voltage diodes, BAS21J, BYV26C, and ES1G are used. For the clamping diodes, it is advised to use fast Schottky diodes. For the subsequent measurements, 20 1PS76SB10 Schottky diodes in series are used. Fig. 11 shows the voltage waveform measurement conducted on a Fairchild MOSFET FDPF5N60NZ with an OFF-state drain-to-source voltage of 300 V, an average current of 1 A, frequency $f = 2$ MHz, V_{GS} from -2 to 12 V, and duty cycle $D = 0.5$.

[1] The emission coefficient is obtained from the Spice model of the diode.

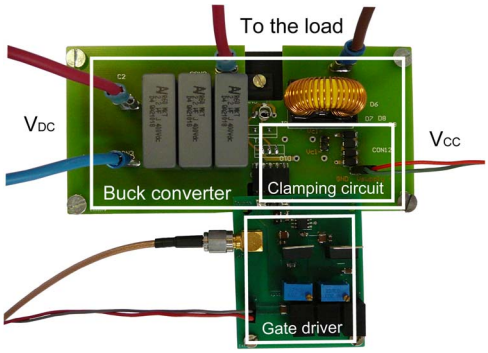

Fig. 10. Test circuit.

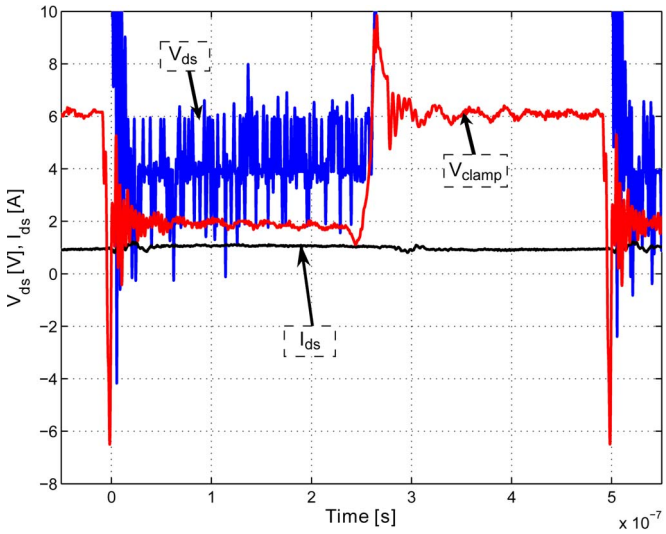

Fig. 11. Measurement with the presented voltage clamp circuit with BAS21J diodes (2 MHz).

The OFF-state drain-to-source voltage is clamped from 300 V to approximately 6.1 V.

As shown in Fig. 11, the ON-state drain-to-source voltage waveform V_{ds}, measured without the voltage clamp circuit, is completely unreliable as it contains a significant amount of noise. However, the presented voltage clamp circuit provides an accurate and clear measurement of the ON-state drain-to-source voltage waveform V_{ds} that can be used to determine the dynamic ON-resistance $R_{\mathrm{dyn,on}}$. For the voltage measurement with the clamping circuit, the Tektronix differential probe P6251 is used. The drain-to-source voltage is measured with the Tektronix high-voltage probe P5100A.

Fig. 12 shows the results for the dynamic ON-resistance $R_{\mathrm{dyn,on}}$, during the ON-state, with and without the use of the presented voltage clamp circuit. The dynamic ON-resistance determined without the voltage clamp circuit contains a significant amount of noise throughout the whole ON-period of the DUT. The quantization levels can be clearly distinguished in the measurement, due to the limited measurement resolution. The result for the dynamic ON-resistance obtained using the presented voltage clamp circuit contains much less noise and gives a very accurate measurement.

In high-electron mobility transistor devices based on heterostructures such as AlGaN/GaN, the value of the dynamic ON-resistance can change during the ON-state, due to the current collapse phenomenon [13], [14]. Therefore, to obtain a representative value of the dynamic ON-resistance, its average value should be calculated. This can, for example, be done on an energy basis, using the following equation:

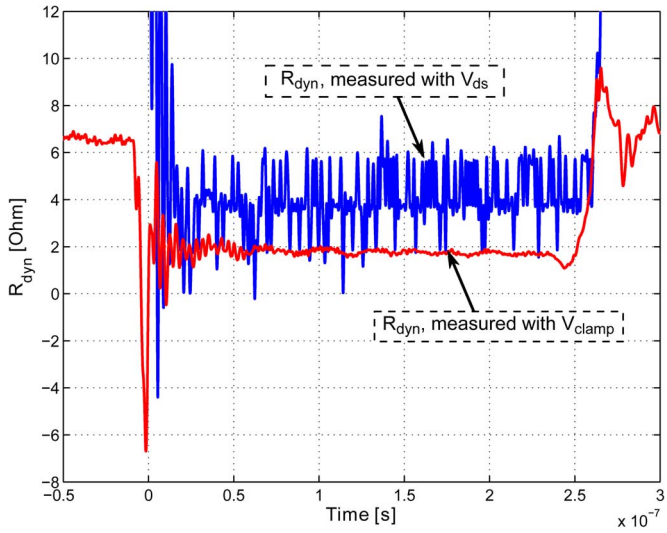

Fig. 12. Dynamic ON-resistance with and without the proposed clamping circuit (2 MHz).

$$R_{\mathrm{dyn,on}} = \frac{1}{I^2 \cdot \tau_{\mathrm{on}}} \int_0^{\tau_{\mathrm{on}}} R_{\mathrm{dyn}}(t) \cdot i^2(t) dt \tag{5}$$

with

$$I = \frac{1}{\tau} \int_0^{\tau} i(t) dt$$

where $i(t)$ is the current through the DUT, τ is the period of the waveform, and τ_{on} is the ON time of the DUT.

VI. Influencing Factors on the Voltage Peaks in the Clamped Voltage at the Switching Instants

As stated before, the voltage peaks in the clamped voltage can be observed during the switching transitions. The values of these peaks depend on the high-voltage diodes used and on the switching times of the measured device. The peaks are higher if the parasitic capacitance of the high-voltage diodes is larger or when the dv/dt of the switching transitions of the DUT is larger. The first influencing factor, i.e., the parasitic capacitance, is because capacitances tend to keep the voltage across them constant. The larger the parasitic capacitance, the higher the peaks in the clamped voltage. However, the capacitance of diodes is voltage dependent, and the relationship between the voltage peaks and the used high-voltage diodes is therefore not obvious.

In Fig. 13, it is shown that for a mirror current of 10 mA, for a transistor switching at 300 V, the BAS21J diode performs best, both for the positive peak and for the negative peak. A proper choice of the high-voltage diodes is thus of the utmost importance because the voltage peaks in the clamped voltage decrease the measurement resolution. The BYV26C and the

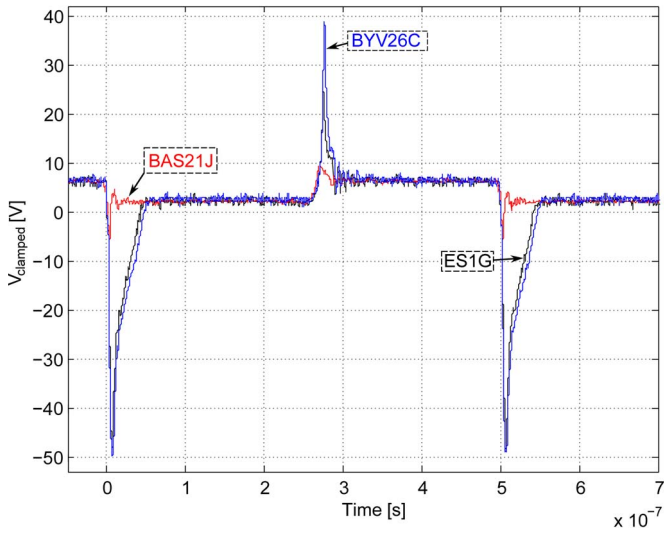

Fig. 13. Clamped voltage, for different high-voltage diodes (300 V). Peaks can be observed at the switching instants. They decrease the measurement accuracy.

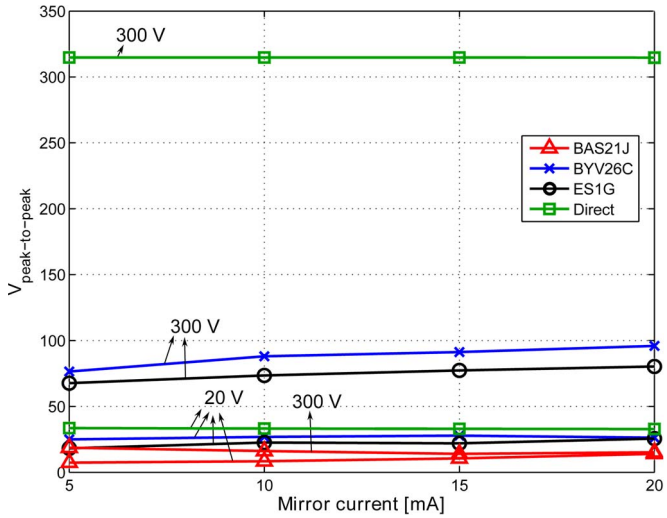

Fig. 14. Peak-to-peak value of the clamped voltage versus the mirror current, for different high-voltage diodes.

ES1G diodes have a similar performance with respect to the negative voltage peak, but of the two, the ES1G performs slightly better when the transistor switches off.

A second factor, i.e., the large dv/dt, is due to the limitation of the current needed to charge/discharge the parasitic capacitance of the high-voltage diode D_A in a short time.

The resolution improvement calculated by (1) is different for all measured diodes, as shown in Fig. 14. The higher the peak-to-peak voltage, the lower the resolution improvement. The scale of the oscilloscope should be set to make the measured waveform fit in the screen. There are two measurements performed, i.e., for drain-to-source voltages of 20 V and 300 V, for different high-voltage diodes and mirror currents. For the drain-to-source voltage of 20 V, all diodes have a very low peak-to-peak voltage, resulting in a high measurement resolution. However, for the drain-to-source voltage of 300 V, only the BAS21J has a low enough peak-to-peak voltage (16.4 V) to still accurately measure the ON-voltage. This is shown in Fig. 15,

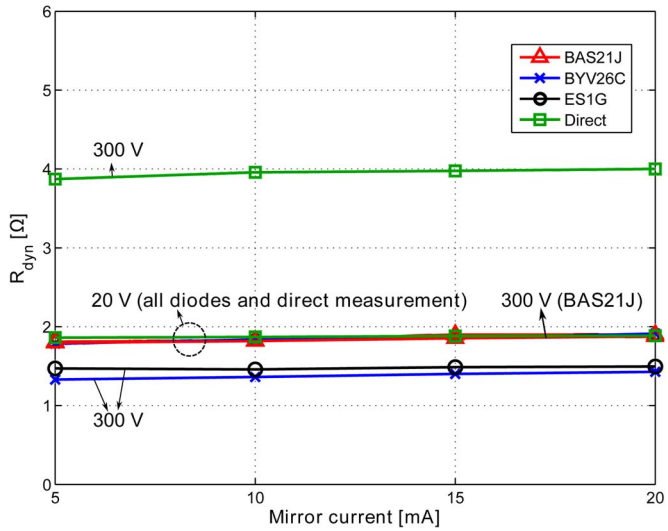

Fig. 15. Dynamic ON-resistance versus the mirror current, for different high-voltage diodes.

where the measurements of the BAS21J at 300 V coincide with the measurements at low voltage (20 V). The latter suffer less from the decreased accuracy, due to the limited voltage peaks in the clamped voltage, and therefore can be considered as approximating the dynamic ON-resistance well.

In Fig. 14, the peak-to-peak voltage of the directly measured drain-to-source voltage is 314.8 V. This results in a resolution improvement of $314.8/16.4 = 19.2$. Furthermore, in Fig. 14, one can also observe that the peak-to-peak values of the clamped voltages are fairly independent of the mirror current, on the condition that the mirror current is large enough to bring the high-voltage diodes fully into conduction.

Furthermore, in Fig. 15, the obtained resistance is more or less the same for all diodes at 20 V and for the BAS21J diode at 300 V. It can be also seen that the dynamic ON-resistance is not influenced by the choice of the mirror current. This proves that the presented measurement circuit is robust with respect to the concrete choice of the mirror current. It is only of importance that the voltage peaks in the clamped voltage are not too high, so that the measurement accuracy is not compromised.

VII. Further Remarks on Error Analysis

In Section IV, a calculation example was given to determine the magnitude of the error of the proposed measurement circuit. Formula (4) shows that the error consists of two terms. In the calculation example in Section IV, it was assumed that the two high-voltage diodes were at the same temperature. Now, we would like to see how the error is influenced by temperature differences. Taking the same current mirror and high-voltage diodes as in Section IV, the first term in the error is, at 25 °C, as follows:

$$\epsilon_1 = -\frac{nkT}{q}\frac{\Delta I}{I} \tag{6}$$

$$= -\frac{2.584 \cdot 1.38065 \cdot 10^{-23} \cdot 298.15}{1.602 \cdot 10^{-19}}\frac{0.6}{59.7} \tag{7}$$

$$= -6.6697 \cdot 10^{-4}\ \text{V}. \tag{8}$$

The second term is, for a temperature difference of 1°, as follows:

$$\begin{aligned}\epsilon_2 &= -\frac{\Delta T}{T} V_{\mathrm{pn},B} \\ &= -\frac{1}{298.15} 0.44 \\ &= -0.0015 \text{ V}\end{aligned}$$

where 440 mV is the forward voltage drop at 60 mA; this value can be found in the datasheet of the BAV21 diode. That means that per degree temperature difference, the second term has $0.0015/0.00066697 = 2.21$ times more influence. Temperature difference has, therefore, the most significant effect on the error. We now quantify their influence. For the BAV21 diode, the thermal resistance between junction and ambient can be found in the datasheet and is 300 K/W. A transient thermal impedance is not given; hence, the results discussed below will be the worst case. Assume that the DUT transistor switches with a duty cycle of 50%. In this case, the diode A (see Fig. 8) is conducting a current of 59.7 mA half the time. The temperature increase of diode A is

$$0.5 \cdot 300 \cdot 59.7 \cdot 10^{-3} \cdot 0.44 = 3.9402 \text{ K}.$$

The temperature increase of diode B, which alternately has to conduct 60.3 mA and $60.3 + 59.7 = 120$ mA, is

$$\begin{aligned}&0.5 \cdot 300 \cdot 60.3 \cdot 10^{-3} \cdot 0.44 \\ &+ 0.5 \cdot 300 \cdot 120 \cdot 10^{-3} \cdot 0.455 \\ &= 12.2 \text{ K}.\end{aligned}$$

This means that the temperature difference between the two transistors is $12.2 - 3.904 = 8.26$ K. This temperature difference leads to errors in the measured voltage of

$$\begin{aligned}\epsilon_2 &= -\frac{8.26}{298.15} 0.44 \\ &= -12.2 \text{ mV}.\end{aligned}$$

For ON-state voltages of 1800 mV (cf. Fig. 15), the error is $12.2/1800 = 0.68\%$ and is negligible. However, also smaller ON-state voltages can be measured. Fig. 1 shows that sometimes resistances as small as 200 mΩ at 1 A should be measured. This corresponds to a voltage of 200 mV. The error in this case is $12.2/200 = 6.1\%$. This error is significant, and in such a case, an appropriate calibration procedure is needed for accurate results. Therefore, it is recommended to use monolithically integrated diodes to eliminate temperature differences between the diodes.

VIII. Conclusion

Conventional circuits for measuring the ON-state voltage waveform of a transistor exhibit a number of problems, such as an RC time constant, measurement offset, limited dynamic range, spikes as a result of high parasitic capacitances, etc. As a result, the measured ON-state voltage waveform contains a measurement error and is not suited for megahertz switching frequencies. To address these problems, a novel voltage clamp circuit, improving the accuracy of the ON-state voltage waveform measurement, has been proposed. The presented voltage clamp circuit does not introduce any delay caused by RC time constants, keeping the voltage waveform clear, even during state transitions of the DUT. The performance of the presented circuit is illustrated by measurements on a 2-MHz inverted buck converter. The dynamic range can be increased by using a power converter that switches at higher frequencies and integrating the measurement circuit on a chip.

Simulations and practical measurements show that the presented voltage clamp circuit drastically improves the measurement resolution of the ON-state voltage waveform. The accuracy of the measurement circuit is assessed, both analytically and with simulations. In addition, it is observed that the clamped voltage exhibits sharp peaks at the switching transitions. Due to the fact these peaks decrease the accuracy of the measurement circuit, their influencing factors are investigated. The peaks occur due to the parasitic capacitance of the high-voltage diodes. They can be reduced by choosing diodes with a low capacitance. The mirror current has slight influence on the voltage peaks.

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