Test Setup for Long Term Reliability Investigation of Silicon Carbide MOSFETs

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Silicon Carbide (SiC), MOSFET, Reliability, Aging

Abstract

Silicon Carbide MOSFETs are now widely available and have frequently been demonstrated to offer numerous advantages over Silicon based devices. However, reliability issues remain a significant concern in their realisation in commercial power electronic systems. In this paper, a test bench is designed that enables an accelerated power cycling test to be performed on packaged Silicon Carbide MOSFETs (TO-247) under realistic operating conditions. An accelerated power cycling test is then performed, with on-state resistance selected as the observed parameter to detect degradation. On-state resistance is routinely monitored online through the use of an innovative voltage measurement system. The packaged Silicon Carbide MOSFET is shown to exhibit a 25% increase in on-state resistance as the device ages throughout its lifetime, with the test still on-going.

Introduction

Silicon Carbide (SiC) MOSFETs have reached a level of maturity where they can be considered as a substitute to Silicon devices. The primary benefits of SiC material are well documented [1] and include improved blocking voltage capabilities and specific on-resistance, faster switching speeds, and higher temperature tolerance. As such, SiC devices have potential to be employed in commercial power electronic systems applications operating at high efficiency, high frequency, or high temperature.

Nevertheless, little information on the reliability of these devices is available in comparison to the wealth of literature addressing the capabilities identified above. An index term search within IEEE Xplore for *'Silicon Carbide + Efficiency'* reveals 204 results for publications between the years 2006 – 2012 under the topic of 'Power, Energy & Industrial Applications'. Conversely, an index term search for *'Silicon Carbide + Reliability'* shows just 87 results over the same time period. More specifically, it is literature concerning the reliability of fully packaged devices in realistic operating conditions that appears particularly scarce.

The majority of SiC reliability research to date has been conducted independent of packaging, and primarily concerned with issues in the die and substrate material itself. Indeed, early experimental results displayed significant issues concerning the long term operation of SiC MOSFET die – particularly at high temperatures [2]. For example, several studies demonstrated underwhelming lifetimes for the gate oxide, with acceptable failure rates only achievable during operation below 150C [3], and lifetimes as low as 1000 seconds at 350C [4]. These would have perhaps excluded SiC from the high temperature applications where it is expected to find a niche. Nevertheless, gate-oxide lifetimes have seen substantial improvement in recent years. At 350C, projected lifetimes of several

hundred years were seen in 2008 – up from 3 years in 2006 [5]. SiC MOSFETs currently manufactured by Cree are asserted to have achieved gate oxide lifetimes of millions of years [6].

The substantial improvement in these types of failure modes has allowed numerous demonstration converters with SiC devices [7-10]. However, commercial power converters using these devices do not appear to be available at present. The long term reliability of these packaged devices clearly remains an issue – especially since packaging technologies still largely follow Silicon based designs [11]. In fact, there are several teams currently investigating alternative packaging techniques for SiC [12-14].

This paper therefore presents what is believed to be one of the first preliminary investigations on the reliability and wear out of commercial SiC MOSFETs under realistic operating conditions. At present just one study can be found that concerns the long term operation of SiC MOSFETs [15]. This involves a prototype massively paralleled module which is run for 500 hours in a realistic mission profile.

This study however, follows a path similar in vein to the type of accelerated power cycling tests that have traditionally been performed on devices such as Silicon based power modules: A test bench is constructed that allows Cree SiC MOSFETs (TO-247) to be tested under an accelerated working point. The on-state resistance is selected as the parameter to be monitored to detect degradation. An innovative voltage measurement system [16] is used to enable online measurement of drain-source voltage and hence allow online calculation of the on-state resistance characteristic as the device ages until the end of its lifetime.

Test Bench Description

The basis of the test setup is displayed in Figure 1. The basic premise of the test setup is to allow the emulation of the operating conditions seen in a full scale inverter – but without the required complexity of a complete converter. A single phase half bridge inverter is therefore constructed. With only open loop control, it is possible for this configuration to generate a sinusoidal output current at any desired amplitude and frequency.

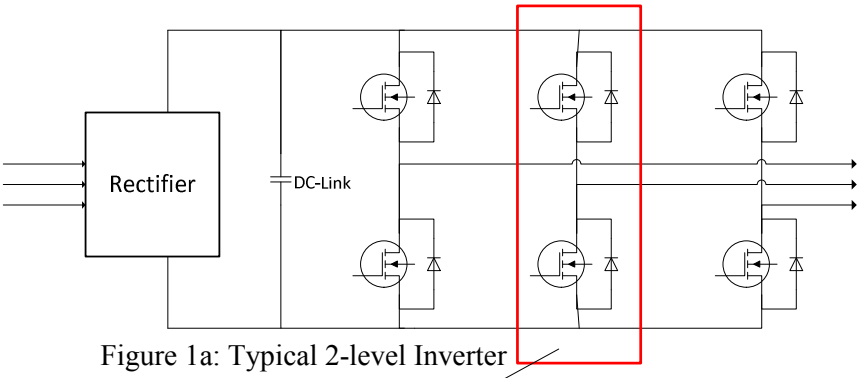

Figure 1a: Typical 2-level Inverter

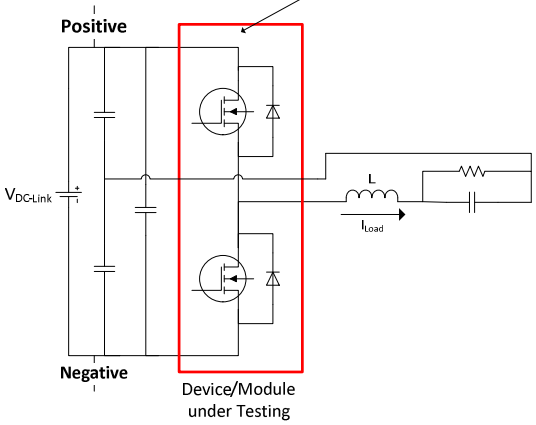

Figure 1b: Basic test setup – Single Phase Half-Bridge DC-AC Inverter

This sinusoidal current induces temperatures swings in the device, consequently stimulating degradation due to mismatches in the Coefficients-of-Thermal Expansion of differing materials used in the construction of the device. This process is considered to be one of the dominant failure causalities in power electronic devices [17].

Because a like-for-like test under actual operating conditions seen in an inverter may consist of perhaps billions of power cycles in an entire lifetime, a more stressful operating point can be selected in order to provoke degradation at an accelerated rate. Previous studies have used lifetime models from the manufacturer or derivations of the Coffin-Manson model in order to specify a suitable work point that will allow meaningful data to be extracted within a reasonable time period [18].

The device under test in this investigation is Cree's CMF10120D SiC MOSFET. Rated at 1200V and 13A, the working point parameters for the accelerated test are given in Table 1.

Table I: Accelerated Working Point

Parameter	Value
DC-Link Voltage	625V
Output Current	13A Peak
Frequency (Output)	3Hz
Frequency (Switching)	10kHz
Heatsink Temperature	75C

Forward Voltage Measurement

The forward voltage drop is regarded as a dominant monitoring parameter to detect degradation in power electronic modules [19]. Typically, this is measured 'offline' – that is, normal operation of the converter is halted momentarily to allow the measurement to be taken. This is due to demands placed on the measurement circuit which require highly accurate measurements at low voltage, while maintaining protection from the high voltage input range seen in many converters. There can also be time constraint issues when the measurement is being taken during a switching cycle, and whether there is interference in the operation of the converter.

In this investigation, a voltage measurement system is used that allows forward voltage drop to be measured during actual operation of the converter [16]. The system has an accuracy of around 1mV and is temperature compensated. The voltage is sampled, along with the current, in the middle of the PWM pulse. Figure 2 displays sample voltage and current waveforms in the MOSFET for one half period, measured during actual operation of the converter.

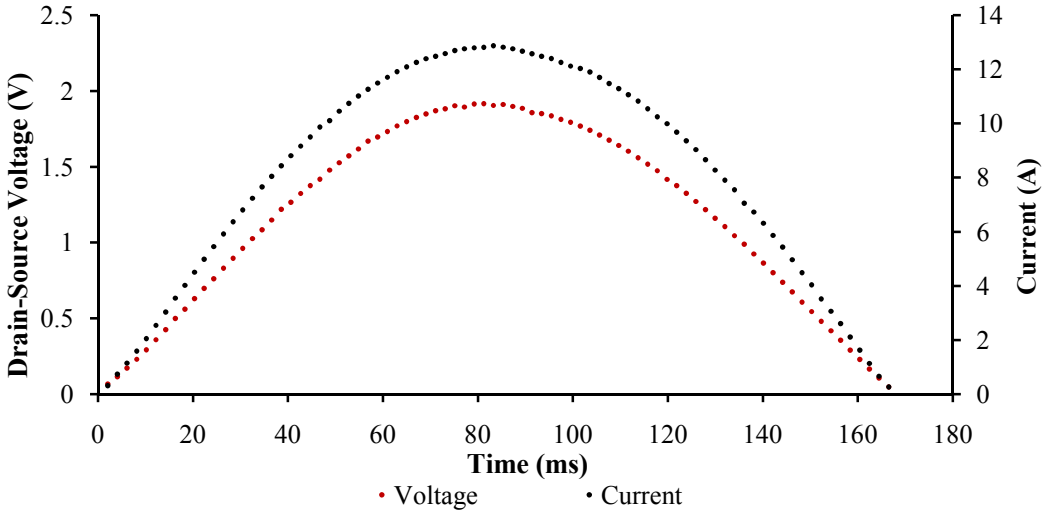

Figure 2: Measured current and measured voltage with voltage measuring system during actual operation

Test Bench Design Considerations

Gate Driver

A custom made gate driver is used, the design of which is heavily influenced by CREE's recommendations [20]. A gate resistance of 6.8Ω was used corresponding to CREE's suggestions – although this is a lower value than what has been used in some previous studies [9]. The gate voltage swings from -2V to 20V, and attention was paid in both the design of the gate driver circuit and converter to minimise the distance between the gate drive IC and the gate leg on the MOSFET.

Busbar Design

The faster switching speeds and improved characteristics of SiC compared to Silicon present a number of challenges in converter design. Most notably, there is an augmented concern regarding the influence of parasitic elements in the circuit; even highly optimised switching test circuits for SiC have displayed unwanted oscillations in switching transitions [21].

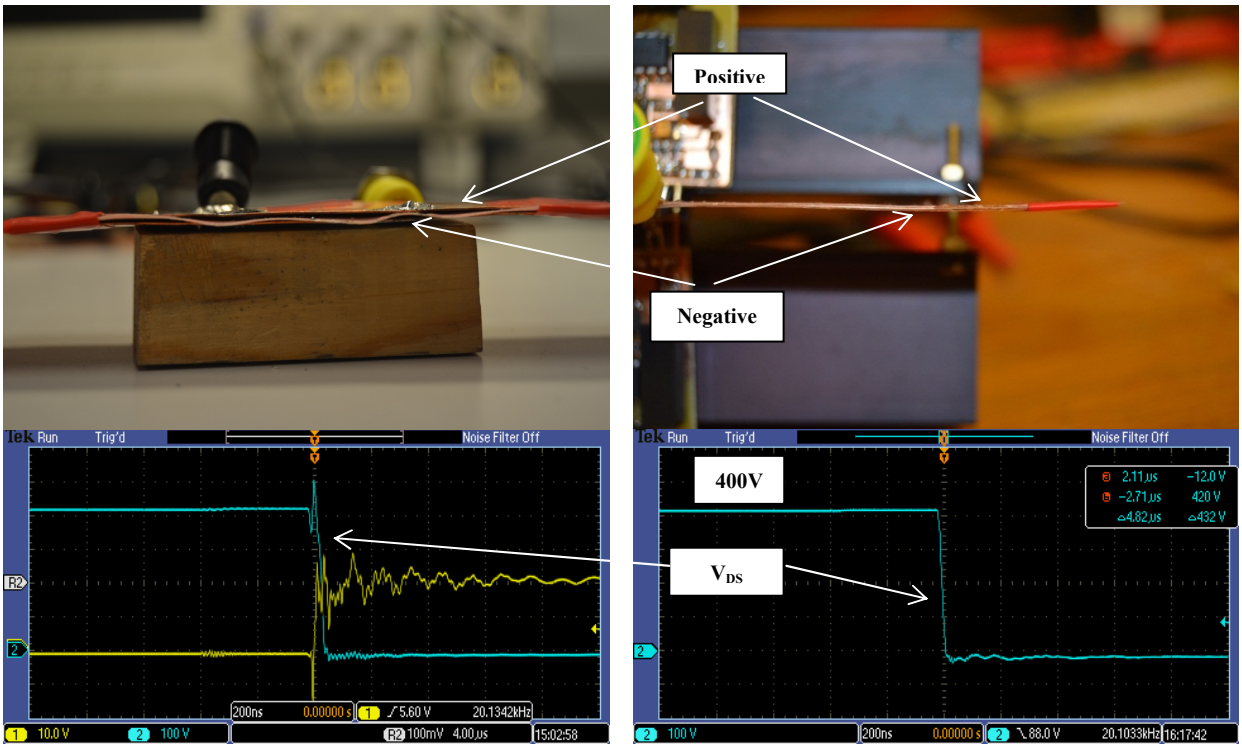

Figure 3: (Left) first busbar, and (Right) new busbar and removal of voltage overshoot on MOSFET turn-on

These unwanted oscillation conditions are unacceptable as they can cause over-voltage transients on the gate, higher switching losses, noise emission and perhaps even lead to uncontrolled and sustained oscillation with potential to cause the destruction of one or more devices.

Past literature on SiC has often made use of increased gate resistance values in order to eliminate the problem of parasitic oscillation. However, this strategy can lead to increased switching times similar to that of Silicon – negating one of the major advantages of SiC. It could therefore be hypothesised that new power circuit design techniques will emerge to facilitate clean switching [22].

Early experimental observations of CREE's SiC MOSFET operating standard 2-layer printed circuit board demonstrated excessive ringing. A copper busbar based design was then decided upon. A busbar

based design allows for closer positioning of the MOSFETs to the DC-link capacitor, in line with recommendations in [23][24]. There are many different texts describing techniques to decrease stray inductance in busbars, particularly regarding the superior performance achieved by minimising the distance between paralleled positive and negative busbars, as well as minimising the thickness/width ratio in the copper [25]. Copper busbars have also been used successfully in SiC converters – achieving very high efficiency in some instances [26].

In the original prototype of the test bench, a busbar with copper sheet dimensions: 36mm x 0.4mm was used, with insulation material of 0.25mm thickness separating the positive and negative sheets. Figure 3 displays the busbar, along with the drain-source voltage waveform at turn-on with the converter tested at a fixed duty cycle: A clear overshoot in the drain-source voltage can be seen.

A second busbar was manufactured with improved characteristics. The copper sheet dimensions of 43mm x 0.3mm reduced the thickness/width ratio, and finer insulation material of 0.1mm used. In addition the busbar was glued together and flattened as much as possible. These small improvements lead to a complete removal of this voltage overshoot, as can be seen in Figure 3.

Results and Discussion

Figure 4 displays the development of the on-resistance of the lower MOSFET in the half-bridge as the power cycling test progresses. Figure 5 displays forward characteristics of the MOSFET at 200k cycle intervals, as measured during operation with the voltage measurement system.

At the time of publication, the MOSFET has been subjected to around 600k temperature cycles with the test still on-going – the MOSFET has not yet failed. Voltage and current measurements in the manner as seen in Figure 2 were performed during converter operation every 1000 cycles. Calculation of the on-resistance at each interval was made between current values of 10,5A – 12,5A.

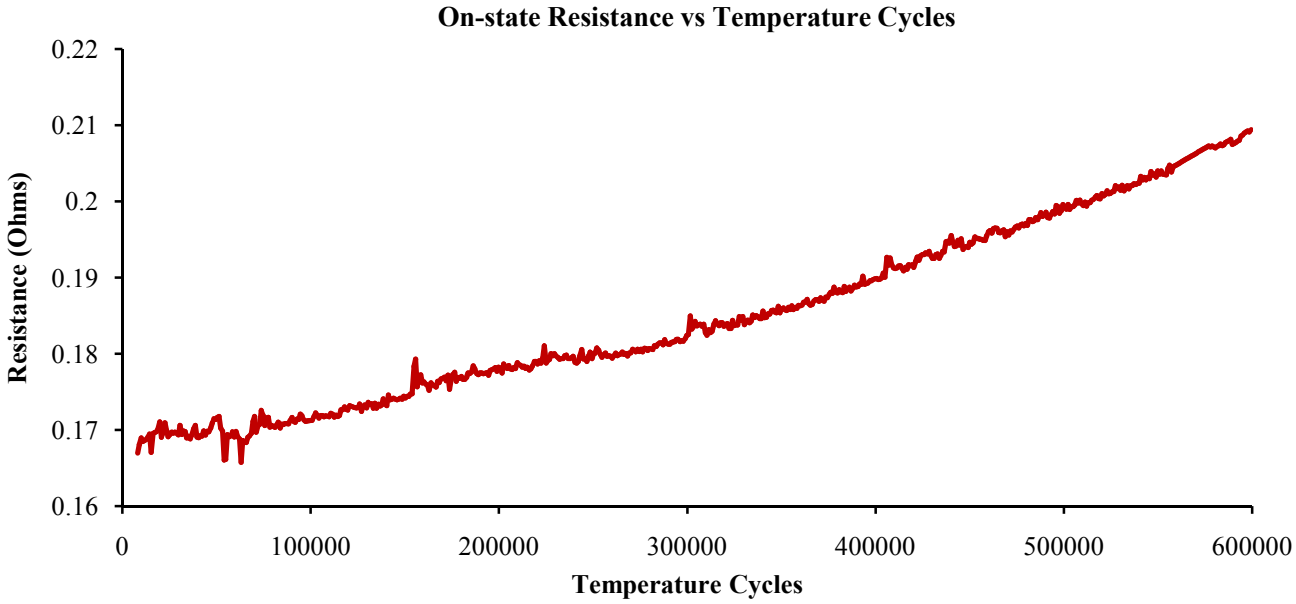

Figure 4: On-resistance evolution throughout accelerated test

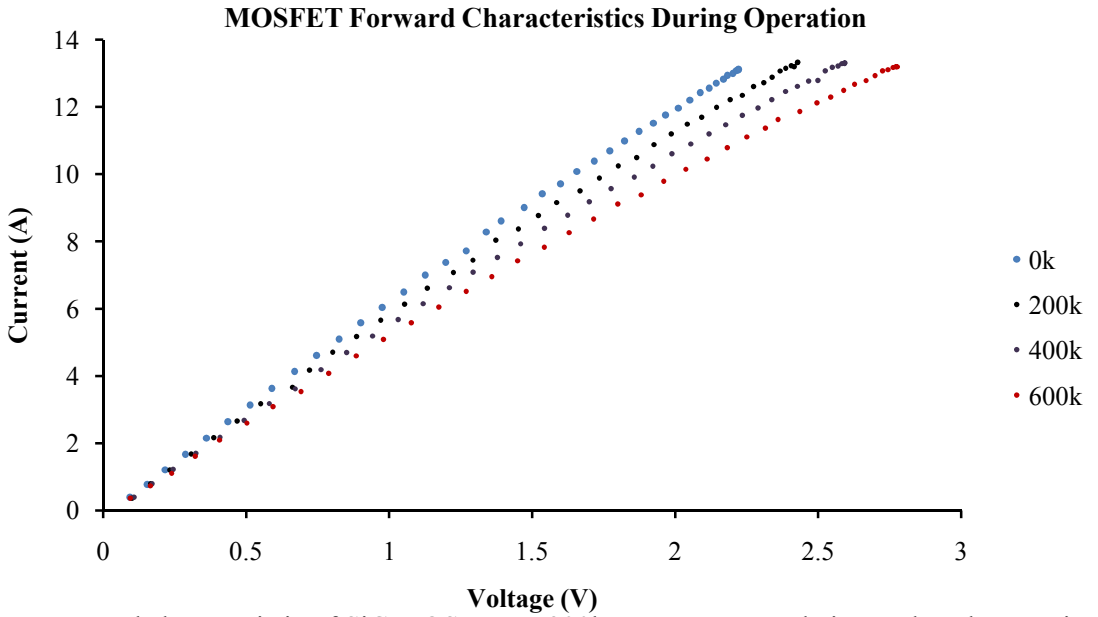

Figure 5: Forward characteristic of SiC MOSFET at 200k temperature cycle intervals - characterised during operation.

Although the MOSFET has not degraded to failure, there is a steady evolution in on-resistance. In fact, an increase of over 25% can be observed from start to finish. In addition, there is a notable increase in the rate of change as the test progresses. The first 500k cycles saw approximately a 4% increase in on-resistance per 100k cycles, however from 500k – 600k the resistance changed over 10% in its value. No sudden large increases were seen, which could have indicated bond-wire lift off [18].

Although with a different device, power level and test procedure, these results appear to contrast what is observed in the only other SiC MOSFET long term operation study [15]. Here, evolution in on-resistance for the whole study was substantially smaller (around 7%), in addition to the largest changes occurring in the first 100 hours of the test, after which the characteristic remained stable in comparison.

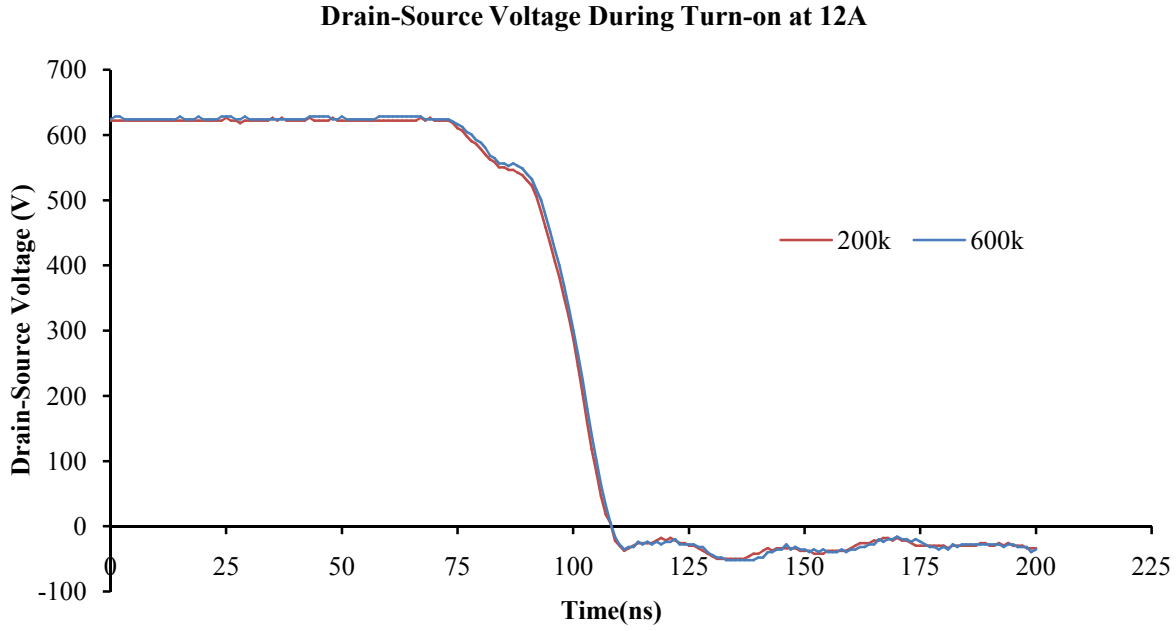

Figure 6: Evolution of Drain-Source Voltage turn-on waveform at 12A, 200k vs. 600k temperature cycles

Figure 6 displays the turn off voltage waveform at 200k cycles and 600k cycles at 12A. Little change can be seen. This appears to be consistent with [15].

Future Work

One shortcoming of the test bench is that although the heatsink temperature is kept constant at 75C throughout the test, there is no compensation for the junction temperature in the results. Coupled with the inability to view inside the TO-247 packaging without destroying the device, establishing the cause of continual rise in on-resistance is difficult. An increase in on-resistance could be caused by an increase in junction temperature, bond wire or solder degradation, or through another mechanism. A temperature sensitive electrical parameter [27] could be employed in order to estimate the temperature of the junction online.

While the turn off voltage waveforms in Figure 6 show almost identical behaviour after 200k and 600k temperature cycles, it has been noted in silicon IGBTs that the transient switching behaviour and oscillations are altered as the device ages [28]. Given the prominence of these kinds of oscillations in SiC devices, this is an area that perhaps could be investigated with more thorough precision. Furthermore, the influence of these parasitic oscillations on the reliability and aging of the device appears to be unknown. This test setup allows for the MOSFETs to be positioned further down the busbar away from the DC-link capacitor (inducing parasitic oscillations) and then tested under identical conditions as seen in this study. A comparison could then be made on whether the degradation rate is significantly altered due to the parasitic oscillations.

Conclusion

A test setup capable of performing an accelerated power cycling test on SiC MOSFETs is constructed. An accelerated power cycling test is performed and the on-resistance characteristic is chosen as the parameter to monitor degradation, which is measured and calculated during actual converter operation. The test is still on-going after 600k temperature cycles, at which point the on-resistance characteristic of the device has seen an increase of over 25% from its starting value. Little change however is observed in switching behaviour in device, contrary to what has been identified previously in some Silicon devices. Improvements to the test bench to increase validity and significance of results are identified, most notably: the inclusion of a junction temperature measurement system, and more meticulous investigation into any changes in parasitic oscillations during switching as the device ages, as well as the effect they may have on the rate of degradation itself.

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