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Introductory Invited Paper

Revisiting power cycling test for better life-time prediction in traction

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Abstract

This paper discusses the commonly accepted method for life-time prediction for power converters in traction. The method is based on junction temperature estimation and thermal cycles on a given duty cycle. The predicted numbers of thermal cycles are compared to the curves giving the number of cycles to failure versus temperature cycles. These curves are extrapolated from power cycling tests. Power cycling tests and extrapolation method will be discussed, particularly under the aspect of failure mechanisms that are induced. In order to generate the same failure mechanisms in power cycling than in the real applications, a new power cycling approach is presented.

1. Introduction

The actual generation of traction power converters is based on the use of high voltage IGBT modules or packs, available on the market. These modules or packs are single or multichip devices (IGBTs and diodes) integrated in the same packaged, which cover a large range of voltage (1700 V, 3300 V, 6500 V) and nominal currents (1600–2400 A, 1200 A, 600 A). The structure of the power converter is a mechanical assembly of different functional parts:

- IGBT modules.
- Cooling device.
- High power connections of bus-bar.
- Close control command or drivers.
- Low voltage connections.
- Capacitors (decoupling or filter).
- Mechanical parts for support and connectors.
- Control board and current sensors can be integrated in the power module.

The design of power converters for rail application is made with looking at the main following aspects:

- Safe operating area: the voltage and current must stay within the limits given by the component manufacturer in operating conditions.
- Dielectric: the high voltage operation imposes minimum distance in the materials and at the surface of the materials to avoid dielectric breakdown and partial discharges.
- Thermal limits: the designer verifies for the train duty cycle that the temperature do not exceed absolute limit values (125 °C for IGBT modules, 95 °C for co-laminated bus-bars, 85 °C for capacitors) and also verify that the temperature cycle in IGBT do not exceed limit value (35 °C 40 °C to allow several million cycles of traction-braking during the whole life of the train).

This last point requires an accurate estimation of train duty cycles, IGBT and diode junction temperatures, and the behavior of IGBT module under thermal cycles. The latter issue has been extensively studied in the nineties, particularly through LESIT (1994–1996) and RAPSDRA (1996–1998) programs. They leaded to the definition of power cycling tests and life-time prediction method of IGBT modules for traction applications.

In the next sections, we will describe the life-time prediction method currently followed, the power cycling tests commonly used, IGBT and diode temperature estimation methods, thermal cycle counting procedures, and finally, we will propose an alternative to power cycling tests.

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2. Life-time prediction method

The starting point for life-time prediction is determining the duty cycle or mission profile of the train during its whole life. Several approaches are possible:

- For train with a well known duty like metros or tramways, we consider the total duty cycle on a given service line assuming maximum load conditions.
- For train without well defined mission profile, we define a reference duty cycle. It is generally the most stressed course for the train.
- For high speed train and locomotives, it is very difficult to define a reference cycle.

The key aspect in the above approach is that we only consider traction-braking cycles. Long cycles like day and season cycles are not considered. In the same way, very short cycles are not accounted for. This is the case of statoric cycles at very low speed in locomotives, for instance.

In order to calculate the thermal cycles seen by the IGBT modules, a series of calculation is needed. Starting from the cinematic of the train, currents in the motors are estimated. Subsequently, in accordance to the control strategy applied on the converter, current and voltage seen by the IGBT modules are inferred. At this stage, with the static and dynamic characteristics of IGBT modules, IGBTs and diodes losses for the pack are estimated.

These losses are the input data for temperature cycle estimation, but another key parameter of the power converter is required: its equivalent thermal model of the whole chain of cooling from the junction to the external air. Generally, this equivalent model is extrapolated from thermal measurements and is presented under the form of a thermal RC stacking. These equivalent models are used to calculate the virtual junction temperature (T_{vj}) of the IGBT module and the temperature of the module base-plate (T_c). The concept of T_{vj} is the average temperature seen by all the chips inside the pack. In a 3.3 kV – 1200 A standard pack, T_{vj} for IGBT is the average temperature for 24 chips. At this point, we obtain the curve T_{vj} versus time for both IGBT and diode dice, T_c versus time for the pack, and a rule to translate these curves to a histogram of cycles, as shown in Fig. 1. A theoretical approach of life-time modelling is done in [1], but it has been simplified in our case for being operational.

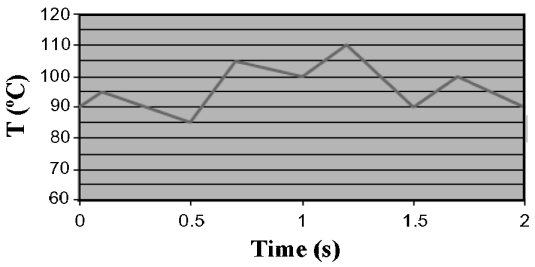

Fig. 1a. Thermal cycles versus time.

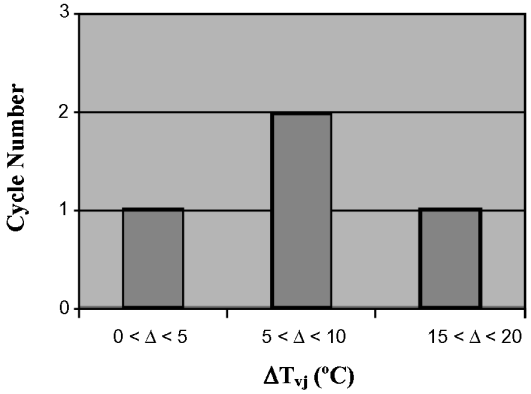

Fig. 1b. Histogram of thermal cycles.

The final step is to compare the histogram of cumulated cycles for the whole life of the train with reference curves. The reference curves shown in Fig. 2 are the number of cycles to failures versus the amplitude of thermal cycles. The reference curve number of cycles to failure (N) versus ΔT_{vj} is worked out from power cycling test results and an extrapolation law based on plastic deformation fatigue (coffin-Manson-like approximation). This law assumes that when ΔT_{vj} ranges from 5 to 80 °C, N may be expressed as:

$$N = N_0 \times (\Delta T_{vj})^{-\alpha} \quad (1)$$

Test result statistical treatment is carried out to take into account distribution of the end of life (Weibull distribution) and this curve gives the number of cycles after which 10% of modules have reached the end of life. The main criterion for the end of life is the evolution of saturation voltage of the IGBT (or forward voltage for diodes). A commonly accepted limit is 5%. The reference curve N versus ΔT_c follows the same basis, but the main criterion is defined as 20% increase of junction to case thermal resistance. The discussion on power cycling tests is made in the next section.

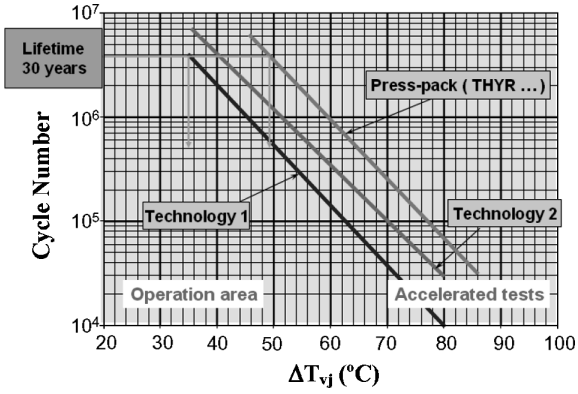

Fig. 2. Reference curves N cycles to failure versus virtual junction temperature cycles for various where N_0 and α are fitting constants depending on the material mechanical properties, where α ranges from 5 to 6.

In order to place the thermal cycles from the histogram on the reference curves, we define an equivalent point $(N_e, \Delta T_e)$ defined as:

$$N_e = \sum_{i-0}^{n} N_i \times \left(\Delta T_e / \Delta T_{i,avg}\right) \quad (2)$$

where i is a subindex which varies for all the range of temperature of the histogram, and $\Delta T_{i,avg}$ represents the center of the range. The criterion to know if we meet the life-time requirement is made by placing the equivalent point with respect to the considered reference curve. This approach is the simplest one; however alternative methods but more complex are possible and will be described in Section 5.

3. Power cycling tests

Power cycling tests (PCT) for high voltage IGBT modules based on wire-bonding technology have been widely studied by different IGBT modules manufacturers and final users in the nineties [2–6,8]. Particularly, RAPSDRA program proposed the sketch of reliability tests1 called Active power cycling tests [9]. Two types of tests were proposed: active power cycling with short duration cycles (on the second range) and active power cycling with long duration cycles (on the minute timescale). The first test is designed to stress the wire-bond and accelerate the wire-bond lift-off mechanism as shown in Fig. 3. The second one is designed to stress the solder between substrate and base-plate and accelerate its delamination as depicted in Fig. 4.

Both tests are run with IGBT packs mounted on a water plate. In order to simplify the test set-up, the IGBT pack is heated by putting the module at on-state with low voltage supply. The temperature swing is adjusted with the device conduction time and the used current level. This means that during PCT, the stress conditions are completely different from real conditions: no switching, no high voltage, no dynamic losses are considered.

Another aspect is that we do not provoke the same failure mechanisms than in real conditions and we only observe indicators of the following failure mechanisms:

Fig. 3. Wire-bond lift-off after thermal cycles.

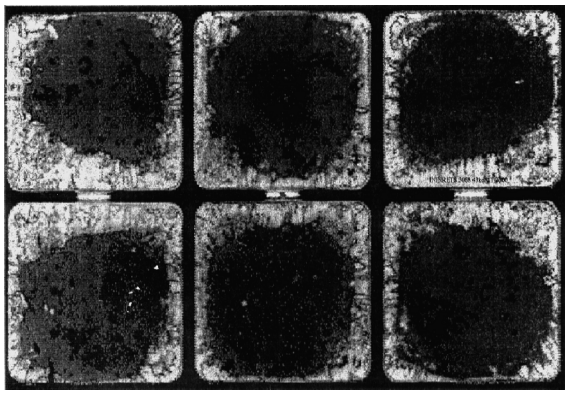

Fig. 4. Solder delamination inside IGBT 3300 V – 1200 A with copper base-plate after 40 kilocycles.

- Collector–emitter saturation voltage for IGBT.
- Forward voltage for diode.
- Collector–emitter leakage current.
- Loss of control of the gate.
- Loss of power connections.

There is no clear relation between the evolution of these indicators and the failure mechanisms in the field.

A first conclusion on PCT is that these tests are well adapted to compare durability of wire-bonds and soldering technology, but the extrapolation of PCT tests for life-time estimation is not so straight-forward. In the developed PCTs, the saturation voltage evolution usually is supposed to monitor the evolution of bonding degradation during time. However, in real applications, one may find a phenomenon not taken into account in such PCTs derived from a simple calculation. The saturation voltage (V_{cesat}) may be roughly approached as:

$$V_{cesat} = V_0 + R_d \times I \quad (3)$$

where V_0 is the knee voltage (2.13 V in this case) and Rd is the device on-resistance (2.16 mΩ at 125 °C). Inside the pack, 24 IGBT chips are connected with eight aluminium wires of 380 μm diameter with an average length of 1.5 cm (typical values for 3300 V – 1200 A IGBT modules). The intrinsic resistance of these wire-bonds is 3.6 mΩ. Therefore the total equivalent resistance of the 192 wire-bonds is 0.019 mΩ. Considering an increase of 5% of V_{cesat} at nominal current, each wire can increase its resistance from 3.6 mΩ to 41.4 mΩ. This increase is local and located under the wire-bond foot where the aluminium structure is changing (aluminium reconstruction). As a consequence, local heating due to wire-bonds will be very high close to the IGBT cells, which may induce the die failure. At this stage, we can propose a scenario of failure mechanism due to evolution of packaging structure:

- Evolution of cracks in the wire-bonds due to aluminium reconstruction at the foot of wire-bond inducing local heating of the wire-bond.

– Increase of average junction temperature due to delamination, this increase is higher under the delaminated area.
– Unbalancing of current in these wire-bonds.
– This ageing phenomenon continues up to the point when locally the maximum temperature under a wire-bond exceeds the limit for static or dynamic overrun.

4. IGBT and diode junction temperature measurement and module thermal distribution

In this framework, there is one misleading point related to the real temperature measurement of the devices inside the pack. For an individual die, such issue can be easily tackled by means of different temperature measurement techniques, such as described in literature [10], mainly based on device thermo-sensitive electrical parameters (TSPs), temperature sensors monolithically integrated in the device, or the use of optical methods. Depending on the spatial resolution, one may define the junction temperature concept, which consists in the temperature average inside the device. However, dice packaging introduces an apparent limitation on temperature local monitoring (temperature spatial resolution problems). Consequently, an average spatial temperature measurement is always performed [11], being the generalisation of the aforementioned quantity at package level, as already explained. Since any sensing method inside the package has not been envisaged by the manufacturers, usually TSPs are used for power cycling purposes, such as the $V_{CE,sat}$ at low current level.

It has been evidenced that an uneven temperature distribution inside the module is induced due to different factors always related to the thermal management strategy. Three main factors have been observed to justify the final thermal map inside a power module: module-cooling system interface, the chips placement inside the module, and the module mechanical mounting procedure. This fact may establish a huge temperature dispersion, which may thermally stress certain devices depending on its location inside the module. Thus, determining such temperature distribution at chip level inside the module becomes essential when facing reliability studies. Fig. 5 depicts this dependence on the employed heat exchange system for cooling down the converter. In this case, one force-cooled heat pipe-based thermosyphon (a) and one water-based cooling system (b) are compared, in which the air and inlet water temperatures are 25 °C and 60 °C, respectively. In both measurements, the contribution due to thermal interaction with the other modules is also taken into account. The thermal maps have been derived in two steps. The thermal maps referred to each device type are firstly acquired by using 60 s long power pulses (1.8 kW in IGBTs and 0.6 kW in diodes), and afterwards, they are synchronised and added, according to the sources superposition principle [12]. From these thermal maps, it is clearly evidenced that the commonly followed way to tackle the thermal design of a converter only considering the virtual junction is not the most reliable approach. In addition, from the combination of a non-uniform temperature field inside the module and possible abnormal events produced during a real application, such as short-circuit, could force the premature device failure, fact which never will be predicted by the conventional or traditional PCT previously described.

5. Thermal cycle counting

In Section 1, we propose a simple way of for calculating the thermal cycles: a temperature cycle of ΔT is a rise or a fall of $\Delta T(N_{+\Delta T}, N_{-\Delta T})$ and for a given application, the number of cycles of amplitude $\Delta T(N_{\mathrm{cyc}\Delta T})$ is evaluated from the temperature profile versus time as:

$$N_{\mathrm{cyc}\Delta T} = (N_{+\Delta T} + N_{-\Delta T})/2 \tag{4}$$

This simple definition can be easily computed but is not very accurate to take into account all their characteristics.

Focusing on the mechanical evolution of the structure, the duration and ramp-up of the cycles play a key role in the life-time evolution and an alternate counting method is required [14]. Another method inferred from the mechanical evaluation of cumulated fatigue is used for this purpose: the Rainflow Method [15]. This is an algorithm that

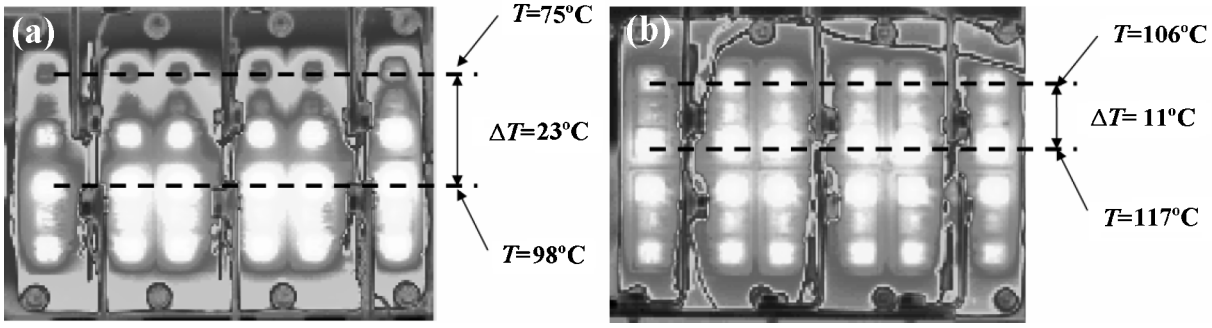

Fig. 5. Infrared thermal maps corresponding to the same module when cooled down by a heatpipe-based thermosyphon (a) or a water cooled-based system (b) obtained from power pulse excitation of IGBTs and diodes separately (1.8 kW in IGBTs and 0.6 kW in diodes) and finally applying the superposition principle.

transforms the stress (or temperature) curves versus time into a frequency histogram of cycles number versus stress amplitude (or temperature) cycle and stress average value (or temperature) for the cycle.

Whatever is the counting method, the limitations are:

- We count step by step and the large cycles are not taken into account.
- We always suppose that there is a cumulative effect of cycles, i.e., two cycles of $\Delta T = 20$ K have the same effect than one cycle of $\Delta T = 40$ K.
- Except for Rainflow method, the average temperature of the cycle is not taken into account.

6. Endurance power cycling tests

The Power cycling test has to be redesigned on the basis of the following principles:

- Acceleration tests must induce the same failure mechanisms than in real service.
- Most likely, ageing of packaging structure induces thermal failure mechanisms linked with high voltage and/or switching.
- Ageing of packaging is mainly activated by active and passive thermal cycles, and
- "Distribution of temperature between chips inside the pack is a key factor for generating failure.

Moreover, not only the thermal stress induced by temperature cycling should be kept, but also the IGBT module should be stressed under real operational conditions (high voltage and switching). On the other hand, if we want to estimate the life-time by extrapolating the results of accelerated tests, the cooling conditions for the IGBT power module must be the same than in real service operation to respect the temperature distribution inside the pack.

This new test called Endurance power cycling test will be carried out with inverter legs mounted back to back and driven by control boards (PWM pattern) modulating the modules heating time in order to adjust ΔT_{vj} at 80 °C and 60 °C. The cooling conditions will be the same than in real operation.

In order to exactly know the context of the generated failures, current and voltage tracking will be made. These tests will be carried out with 10 IGBT packs in order get a good estimation of the Weibull shape factor of the failure distribution at a given ΔT_{vj}. Then, acceleration factor will be calculated between different ΔT_{vj} under the condition that we keep the same range of Weibull shape factor whatever is ΔT_{vj}.

7. Conclusion

After reviewing the present methods for life-time estimation of traction IGBT modules, it appears that all the considered assumptions lead to a high level of uncertainty on the observed failures from the field.

From all the existing methods, the main approximation is that the failure mechanism is mixed with its failure indicator. They are representative for the manufacturer interest to improve its product, but not for the final user. Several times, the harsh environmental conditions or the real working conditions, both electrical and thermal, could induce a device failure before to the predictions given by only considering an ageing process.

As a result from the limitations shown for the conventional thermal cycling procedures, an alternative test (Endurance power cycling test) is proposed with the main objective to stimulate the same failure mechanisms than in real operating conditions. In them, the thermal non-homogeneities inside the power module and non-controlled parameters, as for instance abnormal events, may be taken into account all together, being possible to study such a complex issue. Furthermore, the real module wear-out process could be reproduced, which may induce another thermal fatigue effect in comparison to the conventional PCTs.

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