A Method for Online Ageing Detection in SiC MOSFETs

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***Abstract*—This paper presents a comprehensive study on degradation monitoring of SiC MOSFETs and propose a method to detect incipient faults for early warning in power converters and smart gate drivers. During the accelerated ageing tests (power cycling) several electrical parameters are measured to analyze critical signatures and precursors for early fault detection. Among those, gate leakage current is identified as one of the most practical precursor which exhibit consistent changes throughout the aging and relatively easy to monitor. The proposed method is experimentally justified which can be integrated to a gate driver to monitor the condition of the MOSFETs. This method naturally fits to the applications which cannot tolerate interrupts caused by unpredicted failures. Due to its simple scheme and low cost, it can potentially be embedded into commercial gate drivers featuring improved reliability options.**

***Index Terms*—Gate leakage current, gate oxide, online ageing detection, reliability, SiC MOSFET**

I. Introduction

SILICON carbide (SiC) technology has been gaining importance in power converters due to its higher efficiency, reduction in filtering and/or cooling requirements. Despite relatively higher SiC semiconductor price, manufacturers claim overall cost savings thanks to the reduced cost of the filter elements and the heatsink [1]. On the other hand, this promising technology is relatively new compared to its silicon (Si) counterpart. Therefore, reliability studies are required to minimize the potential uncertainties and problems in the practical applications.

In [2], high-reliability design of SiC MOSFET power modules for extended temperatures is discussed. It analyzes the SiC power modules through extensive tests and proposes improvements in the module design. Limitations and reliability issues of gate oxide in SiC MOS devices are studied in [3] which points out the fundamental shortcomings of SiO_2 dielectric in SiC MOS gates and the trade-off between reliability and on-state resistance. In addition, [4] discusses the short circuit effects on gate oxide reliability. It is shown that Si MOSFETs are more resistant to short circuits than SiC counterparts but different gate structures may improve performance of SiC devices. In [5], the instability mechanisms of threshold voltage in SiC MOSFETs are presented. Reliability performances at higher temperatures are described in [6] and [7]. [6] remarks the continued improvements in SiO_2 based in SiC MOS gates which opens the doors to fully utilize SiC capabilities such as high temperature operation.

By filling the gap in the literature, this paper approaches to the reliability issue of SiC MOSFET from converter designer and end user perspective. As such, it proposes an method for online aging detection. It aims to provide an overall summary of electrical parameter changes in SiC MOSFETs throughout their aging and proposes a new online incipient fault detection method.

The paper is organized as follows. The power cycle test setup and the test method are described briefly in the following section. In section III, the experimental results showing the variations in the certain electrical parameters under thermal stress are shown and analyzed in detail. In section IV, possible aging precursors are identified and compared in order to find the most practical precursor for real-time ageing detection in practical applications. Accordingly, gate leakage current is identified as one of the consistently changing precursor in all aged devices. In section V, an online ageing detection method based on variations in this parameter is proposed and it is experimentally demonstrated that the proposed method can successfully distinguish the healthy and aged devices. Also, practical considerations for implementation are also discussed.

II. Ageing Test and Its Setup

In general, the ageing tests seek for weakest points in device structure and possible signatures for online monitoring of degradation. In practical applications, among all, the power devices are stressed mostly by thermal effects [8]. Hence, in this study, a power cycling test scheme is developed in order to apply thermal stress to four devices simultaneously within safe operating area (SOA).

The test system is composed of three parts; high-bandwidth current source, measurement, and control. The current source includes a half-bridge structure switching at high frequency and inductor to filter switching-frequency ripple in the current. Voltage and current are sensed through signal conditioning part on the tested SiC MOSFETs so that we can regulate current, deduce $R_{ds,on}$ and then decide when to supply and cut the heating current. Control part is, on the other hand, responsible from current regulation. Also, it cyclically changes the tested switches when they reach the junction temperature limit.

The test setup supplies the rated current to the turned-on devices under test (DUT) until maximum junction temperature allowed is reached. The supply current is regulated through high-bandwidth current controller according to the commands of the test algorithm. Junction temperature is estimated through the sensed voltage and current of the DUT by using its correlation with $R_{ds,on}$ [9]. As shown in Fig. 2, DUTs are placed on a temperature-controlled cold plate. This way, the junction is rapidly heated from around 25 °C to 150 °C. After the junction temperature hits the maximum limit, the current is immediately regulated to zero and then the DUT is turned off and left for cooling. In the meantime, the power cycle for the next MOSFET begins so that the test method uses time and hardware resources more effectively. When one MOSFET is in cooling phase, others are tested. With one test setup and cycle time, the testing of four switches is achieved.

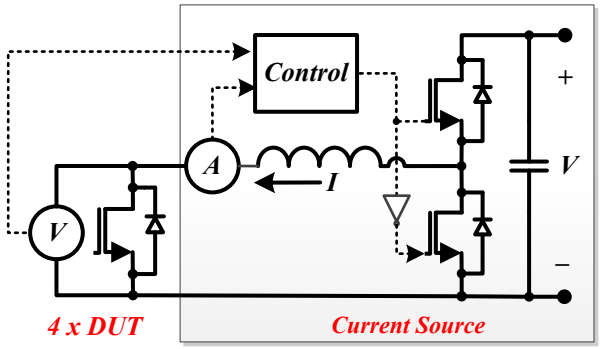

Fig. 1. Block diagram of the ageing test setup.

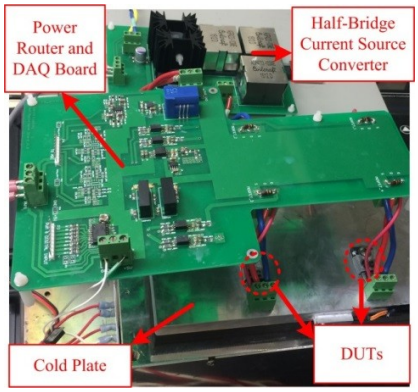

Fig. 2. Accelerated ageing test setup for power cycling.

In this study, a 1200 V, 40 A SiC MOSFET [10] is used as test device. The on-state resistance $R_{ds,on}$, drain-source leakage current I_{dss}, gate-source leakage current I_{gss}, threshold voltage V_{th} and device capacitances of the SiC MOSFETs are periodically recorded with a Keysight B1506A curve tracer, once per 50 thousand power cycles throughout the test.

III. Variations in Electrical Parameters

A. On-state Resistance: $R_{ds,on}$

$R_{ds,on}$ measurement results are presented in Fig. 4 and Fig. 5 for two sample devices as a function of drain current for 13 consecutive periodic measurements. $R_{ds,on}$ is used as a failure precursor for conventional Si MOSFETs [11]. In SiC MOSFETs, it turns out to be applicable, yet there is relatively less change in $R_{ds,on}$ until the end of useful lifetime. After certain power cycles, $R_{ds,on}$ starts increasing which are classified as 'Aged' in the figures. Both device 1 and 2 show similar $R_{ds,on}$ increase as they age.

Fig. 3. Keysight B1506A curve tracer.

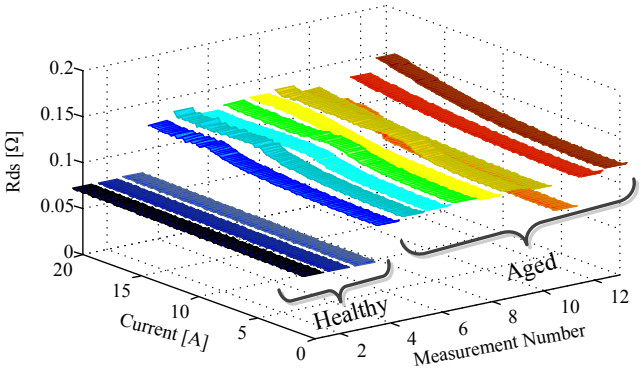

Fig. 4. $R_{ds,on}$ variation during ageing test – Device 1.

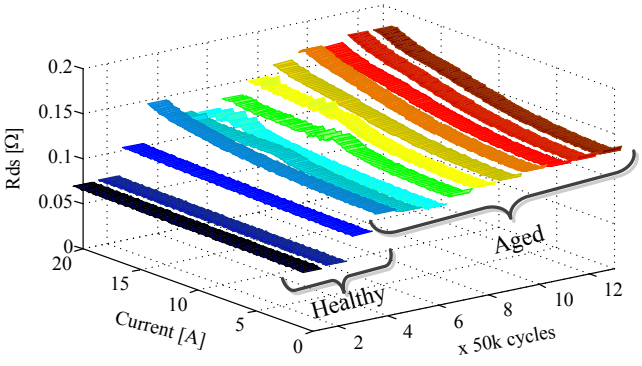

Fig. 5. $R_{ds,on}$ variation during ageing test – Device 2.

B. Drain-Source Leakage Current: I_{dss}

In general, I_{dss} level should be very low in a healthy device; i.e. maximum 100 µA for the tested device [10]. At the beginning of each test, I_{dss} is practically zero as shown in Fig. 6 and Fig. 7 and hence there is no ageing sign. As the devices start aging, they begin to leak drain current, whose magnitude exceeds the maximum allowed datasheet value. Both devices show similar I_{dss} increase as they age. For these two sample

devices, the leaked drain-current can reach 0.5 mA after ageing or more.

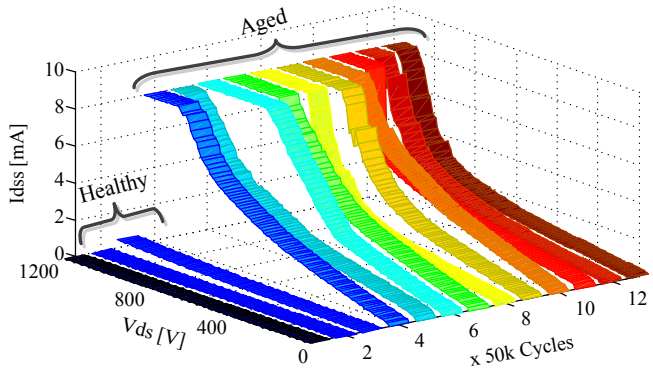

Fig. 6. I_{dss} variation during ageing test – Device 1.

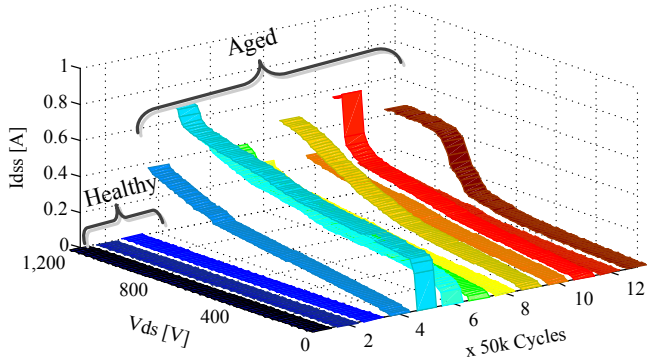

Fig. 7. I_{dss} variation during ageing test – Device 2.

C. Gate-Source Leakage Current: I_{gss}

I_{gss} is typically very low in any healthy devices i.e. maximum 250 nA for the tested devices [10]. Before ageing becomes remarkable, switches have practically no leakage current as shown in Fig. 8 and Fig. 9. After certain degradation in the switches, I_{gss} increase to values way more than the allowed limits. The results show that this increase can be detected quite easily since I_{gss} in healthy and aged cases show very diverse results.

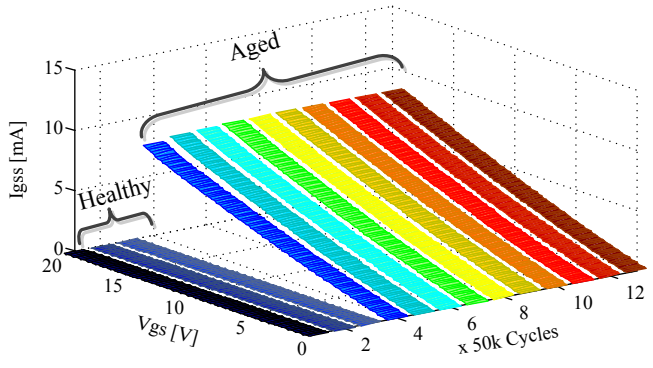

Fig. 8. I_{gss} variation during ageing test – Device 1.

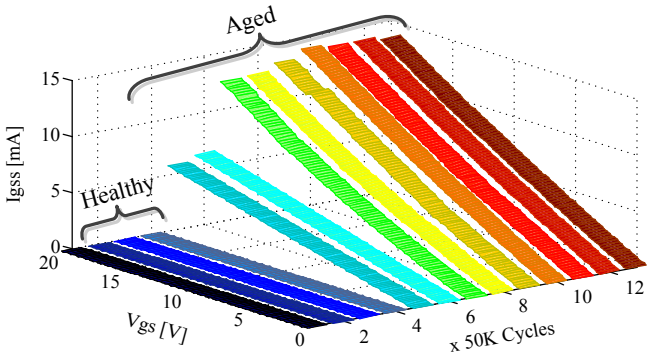

Fig. 9. Igss variation during ageing test – Device 2.

D. Threshold Voltage: V_{th}

In the device datasheet, threshold voltage is defined as the gate-source voltage that causes 5 mA drain current I_{dss} under 10 V drain-source voltage V_{ds} [10]. Considering this definition, it can be concluded that there is a small decrease in the threshold voltage V_{th}, as the devices age. As shown in Fig. 10 and Fig. 11, devices do not conduct any current until V_{gs} reaches 1.5 V in the healthy case. However, this significantly changes through the degradation and the devices conduct noticeable current for any positive voltage V_{gs}.

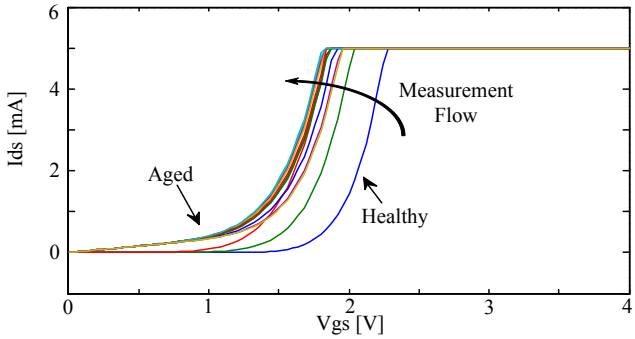

Fig. 10. V_{th} variation during ageing test - Device 1.

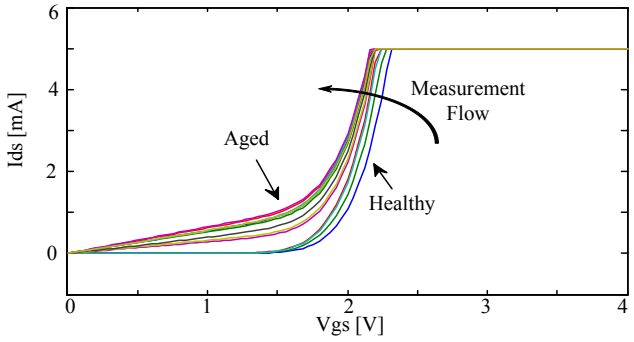

Fig. 11. V_{th} variation during ageing test - Device 2.

E. Device Capacitances: C_{iss}, C_{oss}, Crss

The input C_{iss}, output C_{oss}, and reverse transfer C_{rss} capacitances of the SiC devices are presented in Fig. 12 and Fig. 13. All measurements taken throughout the test are plotted in same graph and no meaningful change in any of the capacitances is observed.

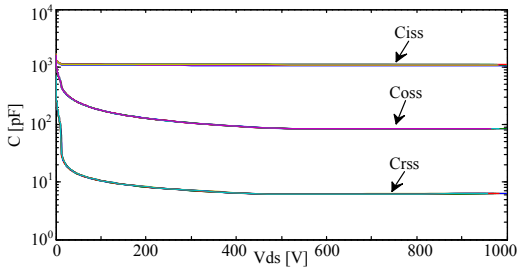

Fig. 12. Capacitance variation during ageing test - Device 1.

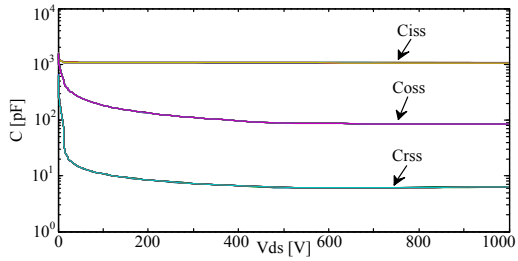

Fig. 13. Capacitance variation during ageing test - Device 2.

IV. Evaluation of Ageing Precursors

Previously presented test results show that I_{gss}, I_{dss}, V_{th}, and $R_{ds,on}$ of SiC MOSFETs change as the device ages. Moreover, the variations in I_{dss}, I_{gss}, and V_{th} indicate that gate-oxide is the most affected component in SiC MOSFETs and the gate-oxide related problems is prominent as predicted in previous literature [3-7]. Next, utilization of these findings to detect the ageing in SiC MOSFETs is discussed.

A. On-state Resistance

It shows valuable information about impending failure. However, in practice, obtaining reliable $R_{ds,on}$ information online in the commercial converters is a challenging task. First, the rise in $R_{ds,on}$ may be due to either temperature or ageing. Reliably distinguishing these in practical applications is not easy if not impossible. Second, measuring $R_{ds,on}$ in a converter is complicated. The measurement circuit should be very precise at very low voltage ranges such as 1-2 V to measure $R_{ds,on}$ and also able to block DC-link voltage. The DC-link voltage protection in $R_{ds,on}$ measurement circuits may impair the precise measurement [12]. As a result, usage of $R_{ds,on}$ in online tracking of ageing in SiC MOSFETs has some practical limitations.

B. Drain-Source Leakage Current and Threshold Voltage

Drain-source leakage current flows through the main high-current path. Therefore, I_{dss} measurement should be precise in mA-region, tolerate nominal switch current, and not cause extra leakage inductance which can severely limit overall converter performance. As a result, I_{dss} and V_{th} based online incipient fault detection is not practical to realize due to these contradicting requirements.

C. Gate-Source Leakage Current

In this work, detecting the ageing in SiC MOSFETs using I_{gss} is suggested to be most practical among other precursors for several reasons. First, this current can be measured with minimal interference to the other circuitry. It does not use any signal from high-current or high-voltage parts of the power stage for monitoring device ageing. Second, the gate-source leakage current has very distinct values for healthy and aged cases. Therefore, we propose to track I_{gss} online as an aging signature for SiC MOSFETs.

V. Proposed Online Ageing Detection Method

The proposed method is summarized in block diagram shown in the Fig. 14. The gate resistance is used to measure the gate leakage current. The voltage drop on the gate turn-on resistance is sensed with a difference amplifier, and then the amplified differential voltage is compared to a limit voltage, which functions as a threshold for detecting the ageing. For healthy switch, there will be practically no current and comparator will output logic-0 indicating the switch is healthy. On the other hand, aged switch will leak some gate current in range of a few mA and the comparator will output logic-1 once the voltage drop on the gate resistor exceeds the limit voltage. This warning represents that the switch is aged, a failure may happen in the near future.

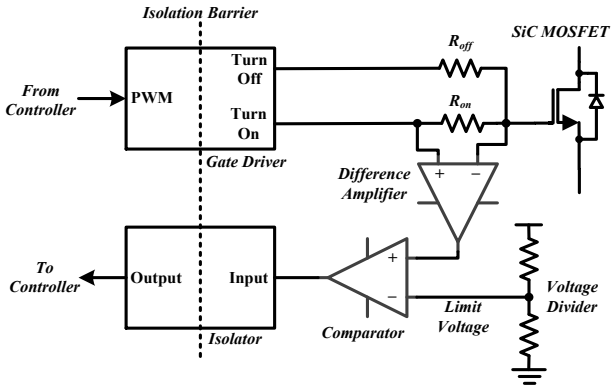

Fig. 14. Block diagram of the proposed method.

A. Discussion on Practical Implementation

Accuracy of voltage measurement on the gate resistance is of paramount importance for the proposed method. The requirements for the measurement circuit can be listed as follows:

- Gate driver power supply can be used to feed the ageing detection circuitry by adding simple low-cost linear regulator.
- The amplifier should have a wide common-mode (CM) voltage capability and include gate voltages in the CM range because the amplifier will experience positive and negative gate voltages as CM voltage and amplifier should handle it. On the other hand, with a simple modification in amplifier's power supply arrangement, negative CM voltage capability requirement can be decreased. If the amplifier uses the negative gate voltage as its ground reference, then the amplifier would not experience meaningful negative CM voltage. Hence, an amplifier with less negative CM voltage range can be used. In addition,

CM rejection ratio in high frequency region such as switching frequency should also be high enough.

- The amplifier should have enough bandwidth to properly operate in the high frequency range, i.e. a few multiple of SiC MOSFET switching frequency.
- Input bias current of the amplifier should be at least one order of magnitude less than the target gate leakage current.
- Input offset voltage of the amplifier should be at least one order of magnitude smaller than the minimum threshold voltage on the resistor.
- In practical gate drivers, there can be gate bleeding resistor and protection Zener diode just next to the gates of the power semiconductors. These can cause a small current flow over the gate resistance in any time and hence false alarm by contaminating the I_{gss} measurement. Therefore, the bleeding resistor should be place just at the turn-on output of gate driver chip and before turn-on gate resistor. Zener diode with a very low leakage current at gate voltages should be preferred.
- In different converter designs, different gate resistances are used. Thus, the measured voltage on the turn-on gate resistor will be different for different designs. The resistor divider, producing the limit voltage for the comparator, can be tuned so that one design can easily be adapted to many different applications.
- In healthy switches, certain amount of current flows over the gate resistor to charge gate during turn-on. However, in SiC MOSFETs, this is the order of tens of nanoseconds; hence, limited bandwidth of the difference amplifier will filter out this short-time voltage drop. Thus, false alarms due to normal switching are not expected and this is verified in the experiment.

B. *Experimental Results*

To verify the proposed method, a test circuit, shown in Fig. 15, is build considering the practical suggestions above. As the difference amplifier, LT1999-50 with 50-gain and AD8417 with 60-gain are selected. The amplifier output has 2.5 V bias due to the single supply operation. The gate driver is driven by a 100 kHz square wave with a 50% duty cycle. Comparator is tuned for 1 mA gate leakage-current limit. Turn-on gate resistance is 5 Ω.

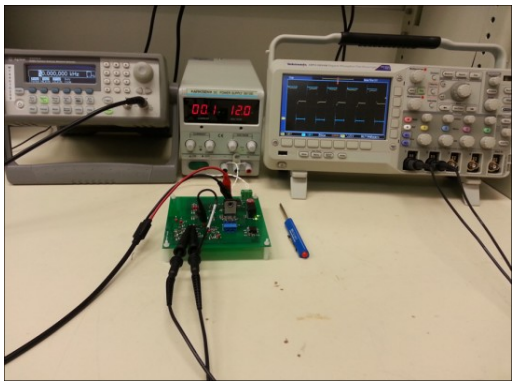

Fig. 15. Test setup for gate leakage current detection

As shown in Fig. 16, for healthy device, amplifier output is around 2.6-2.7 V. The excess is due to the input offset voltage and bias current. In this case, comparator correctly outputs logic-0. For the aged device (Device-1), amplifier output is reaches to 4.8-5.0 V when the switch is turned on and then decreases to the normal value of 2.6-2.7 V after the switch is turned off as show in Fig. 17. Comparator truly outputs logic-1 indicating that the device is aged and a failure is approaching.

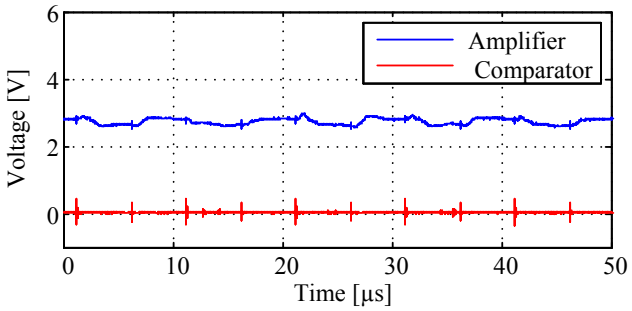

Fig. 16. Healthy device experimental result: Amplifier (blue) and Comparator (red) outputs.

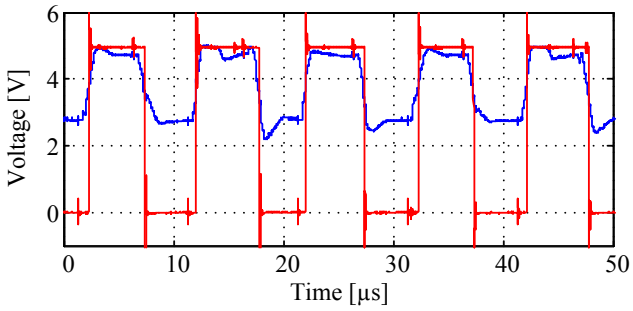

Fig. 17. Aged device experimental result: Amplifier (blue) and Comparator (red) outputs.

VI. Conclusion

This paper extensively analyzes the failure signatures of SiC MOSFETs and proposes a method to detect ageing. A detailed ageing test procedure is proposed and applied. Ageing test results indicate that most of the tracked electrical parameters change through ageing process. If the emerging degradation is anticipated by tracking a suitable precursor, power converter failures and related problems can be prevented. The gate leakage current is proposed as a ageing tracking signature. If the gate leakage current goes beyond a specific limit, the converter controller will warn the user about a possible failure. The proposed idea is implemented and experimentally verified. The considerations for practical design are also provided. The presented method is a powerful ageing detection tool, which can be integrated into an existing gate driver chip as an extra protection feature or can also be implemented discretely with the off-the-shelf components.

Acknowledgement

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REFERENCES

[1] U. Schwarzer, S. Buschhorn, and Klaus Vogel, "System Benefits for Solar Inverters using SiC Semiconductor Modules," in *Proc. PCIM Europe*, pp. 1-8, 2014.

[2] J. D. Scofield, J. N. Merrett, J. Richmond, A. Agarwal, and S. Leslie, "Performance and Reliability Characteristics of 1200 V MOSFET Module," in *Proc. International Conference on High Temperature Electronics,* 2010.

[3] R. Singh and A. R. Hefner, " Reliability of SiC MOS devices," *Solid-State Electronics*, vol. 48, pp. 1717–1720, 2004.

[4] T.-T. Nguyen, A. Ahmed, and T. V. Thang, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2445 - 2455, May 2015.

[5] A. J. Lelis, R. Green, D. B. Habersat, and M. El, "Basic Mechanisms of Threshold-Voltage Instability and Implications for Reliability Testing of SiC MOSFETs," *IEEE Transactions on Electron Devices*, vol. 62, no. 2, pp. 316 - 323, Feb. 2015.

[6] L. C. Yu, G. T. Dunne, K. S. Matocha, P. Cheung, J. S. Suehle, and K. Sheng, " Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments," *IEEE Trans. Device and Materials Reliability*, vol. 10, no. 4, pp. 418-426, Dec. 2010.

[7] W. Zhou, X. Zhong, and K. Sheng, "High Temperature Stability and the Performance Degradation of SiC MOSFETs," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2329 - 2337, May 2014.

[8] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M. H. Poech, "Fast power cycling test for IGBT modules in traction application," in *Proc. IEEE Int. Conf. Power Electron. Drive Syst.*, vol. 1, pp. 425–430, May 1997.

[9] X. Perpiñà, J. F. Serviere, J. Saiz, D. Barlini, M. Mermet-Guyennet, and J. Millán, "Temperature Measurement on Series Resistance and Devices in Power Packs based on On-state Voltage Drop Monitoring at High Current," *Microelectronic Reliability*, vol.46, pp.1834-1839, 2006.

[10] Cree, C2M0080120D Datasheet, [Online]. Available: http://www.wolfspeed.com/downloads/dl/file/id/167/product/10/c2m0080120d.pdf

[11] J. R. Celaya, A. Saxena, V. Vashchenko, S. Saha, and K. Goebel, "Prognostics of Power MOSFET," in *Proc. IEEE International Symposium on Power Semiconductor Devices and ICs*, pp. 160 - 163, 2011.

[12] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, P. B. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of IGBT," in *Proc. IEEE Power Electron and Appl. Conf.*, pp. 1–10, 2013.