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Fast power cycling protocols implemented in an automated test bench dedicated to IGBT module ageing

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ABSTRACT

This paper presents fast test protocols for ageing IGBT modules in power cycling conditions, and a monitoring device that tracks the on-state voltage V_{CE} and junction temperature T_J of IGBTs during ageing test operations. This device is implemented in an ageing test bench described in previous papers, but which has since been modified to perform fast power cycling tests.

The fast test protocols described here use the thermal variations imposed on IGBT modules by a test bench operating under Pulse Width Modulation conditions. This test bench reaches the maximal values of power cycling frequencies attainable with a given module packaging in order to optimize test duration.

The measurement device monitors V_{CE} throughout the ageing test that is needed to detect possible degradations of wire bonds and/or emitter metallization. This requires identifying small V_{CE} variations (a few dozen mV). In addition, the thermal swing amplitude of power cycling must be adjusted to achieve a given ageing protocol. This requires measuring junction temperature evolution on a power cycle, which is carried out by means of V_{CE} measurement at a low current level (100 mA).

Experimental results demonstrate the flexibility of this test bench with respect to various power cycling conditions, as well as the feasibility of the proposed on-line monitoring methods.

1. Introduction

Power devices in numerous applications suffer from thermo-mechanical stress resulting from power cycling, thus inducing ageing mechanisms. The improvement of power electronics systems requires increasing their operating safety [1–5], which itself depends on knowledge concerning ageing mechanisms and the failure causes in power semiconductor devices such as IGBT modules.

To move forward in this area, physical analysis, modeling, and multi-physics simulations must be achieved [6–8], but they must also be supplied and completed by application results and data collected in laboratory tests [9–19]. The latter issue is the subject of this article, which presents a test bench able to stress IGBT under power cycling conditions with a high repetition frequency, accompanied by the corresponding measurement methods and a system developed to acquire values of the junction temperature and on-state voltage V_{CE} during tests. These tests focus on studying ageing of the wire bond and emitter metallization, the other parts not being stressed by the few-second thermal swing because of their higher time constants.

The V_{CE} parameter is used as an ageing indicator of the bond wires and emitter metallization [15,18,22,29]. It must be monitored to evaluate the degradation state of the device during the test and to stop the test before failure. The junction temperature is needed to control the thermal swing amplitude as well as for the V_{CE} measurement that must be performed with given die temperature and current conditions.

Section 2 of this article provides an overview of the experimental test bench, which places IGBT power modules under operating conditions close to those found in the real world (PWM operations). The presentation then focuses on thermal module operating conditions.

A general analysis based on a simplified thermal model enables identification of the thermal swing maximal frequency that can be used in power cycling tests. It is shown how the test bench can be configured to provide various test conditions, from low cycling frequencies (a few dozen seconds) to the highest cycling frequencies attainable with a given IGBT module, with this latter configuration being the most appropriate to minimize test duration in case of low thermal swing amplitudes. Lastly, the experimental maximal frequency range obtained with the tested IGBT modules is shown, with the results confirming the trends of the previous analysis.

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Automated monitoring is required to preserve the benefit of high frequency tests in terms of duration. Section 3 presents the principle of on-line measurement and the corresponding hardware system that was implemented to monitor V_{CE} evolution and to adjust and control junction temperature swings. Both tasks are based on V_{CE} measurement: the first performed at fixed current and temperature values (100 A, 125 °C); the second performed at a low fixed current value (100 mA), which constitutes a classical method for measuring junction temperature indirectly [23,26]. Then follows a description of the V_{CE} measurement stage that uses an original and simple floating circuit connected to a 16-bit acquisition board, along with the power stage modifications required to introduce automated V_{CE} (100 A, 125 °C) measurement throughout the ageing test. Experimental results concerning both measurements are presented and commented.

Lastly, Section 4 presents the results of ageing tests obtained on a group of twenty-seven samples using the high frequency protocols defined in Section 2. They confirm that unusually low temperature swing values can be reached with short test durations, while the applicability of the fast test compared to the classical test is demonstrated in the studied domain.

2. Ageing test bench and power cycling conditions

2.1. Tested devices

The tested devices are IGBT modules with one inverter leg and 600 V–200 A trench gate chips (Fig. 1). This is typical of current technology that uses mainly Aluminum Nitride Direct Bond Copper and wire bonds to interconnect the upper part of IGBT dies. The overall aim of this work is to collect quantitative data concerning metallization and wire bond degradations under variable power cycling conditions.

2.2. Test bench power stage

The samples are aged in a test bench operating under switching conditions. A general view and selected details are shown Fig. 2. This test bench uses two modules to constitute a PWM Bridge (Fig. 3(a)) that operates as a drive inverter with respect to the electrical stress applied to IGBT dies. Closed-loop Sinusoidal Pulse Width Modulation is applied to generate a controlled current in the IGBTs. A more detailed description of this test bench can be found in [20–22].

The dies are thus placed under conditions very similar to those found in the real world, conversely to classical test benches [9–19]. The switching frequency can be adjusted between 10 kHz and 30 kHz.

Fig. 3(b) shows a simulation (using PSIM software) in which a simplified thermal equivalent circuit (see Section 2.3.1) is used to estimate junction temperature (Fig. 3(c)).

The Controlled Current Source (CCS), corresponding to IGBT losses, is driven by the simulated IGBT current (taking PWM modulation into account) multiplied by a constant value for the on-state voltage. To better show the electrical current shapes, a low (but not realistic) switching frequency value was chosen for the simulation. This induces a high frequency temperature ripple that does not exist in real operation. The main aim of this simulation is to recall the shape of temperature ripple induced by the modulation itself, whose amplitude depends on the electrical stress and on the modulation frequency. In the following part of this section, it will be shown how this thermal behavior can be used to impose controlled power cycling.

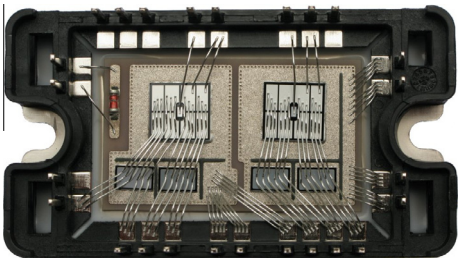

Fig. 1. View of the tested IGBT module.

The main advantages of the test bench's operation are the following:

- Ageing tests are performed under realistic electrical conditions compared to tests that use only current injection under low voltage.
- As switching losses constitute a significant part of IGBT losses, they can be adjusted by the switching frequency to control thermal swing amplitude. This allows performing most parametric tests with normal and constant electrical conditions, and therefore to avoid overload conditions when high temperature swings are required.
- PWM operation makes it easy to control all of the thermal swing's amplitude and periodic conditions.
- It is possible to apply an opposition method [21] that drastically reduces electrical power consumption.

2.3. Power cycling conditions

2.3.1. General considerations regarding power cycling tests

Power cycling tests have long been applied to semiconductor devices. The purpose of these tests is to partially reconstitute, in the laboratory, the operating conditions encountered in different applications, especially in transport-embedded systems [9–19]. In such systems, the junction temperature can vary over a wide range (up to 60 °C) throughout the mission, with cycle periods from a few seconds to a few dozen seconds, and with case temperatures in the 50–80 °C range. Therefore, to be relevant in this context, the amplitudes of power cycling on the junction must be held within a range of 30–60 °C.

For the lowest thermal cycle in this range (ΔT_J = 30 °C), the lifetime is typically higher than 10^7 cycles [10]. Therefore, the test duration is a critical issue. For example, a power cycle period of 10 s leads to a test duration of 40 months for a lifetime of 10^7 cycles. Even this brief analysis shows that it is of great interest to minimize the power cycle period.

The device itself is actually a limiting factor for test speed and it is not possible to select just any test period. The next part of this article highlights the trends of this limitation. Such an analysis first needs a thermal model. Fig. 4(a) proposes a discrete and simplified model describing module thermal behavior from the junction to the case, derived from the geometrical and thermal characteristics of the successive layers. The thermal time constant of the die (a few 10^{-5} s) is ignored and the case temperature T_{Case} is assumed to be imposed by a regulated thermal exchanger (the case of the present test bench).

A simplified analysis can be performed by considering an ideal shape for the die losses (square losses, Fig. 5(a)). This shape is defined by two parameters: maximal losses P_{DieM} and duty cycle D. Therefore, the average die losses are $P_{DieAv} = D\,P_{DieM}$. In the test, this latter value must be compatible with module characteristics and the thermal exchanger's capability. Theoretical limits can be now identified:

- If the cycling period is higher than the highest time constant of the thermal model, the heat flux flows directly trough the stack and $\Delta T_J \approx \Sigma\, R_{TH}\, P_{DieM}$, power cycling is maximal.

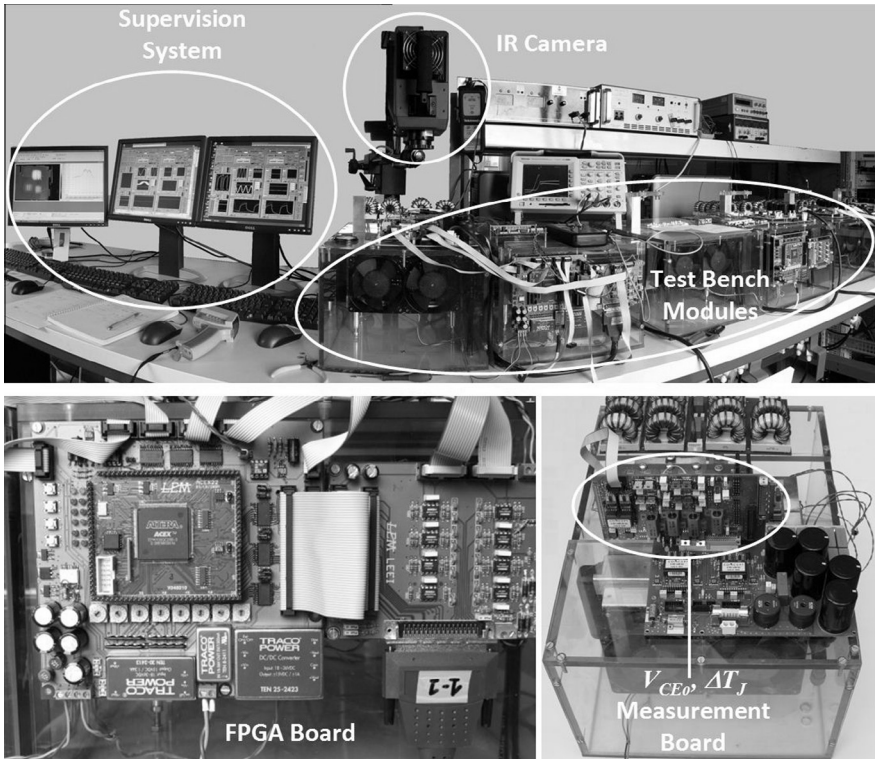

Fig. 2. Views of the test bench.

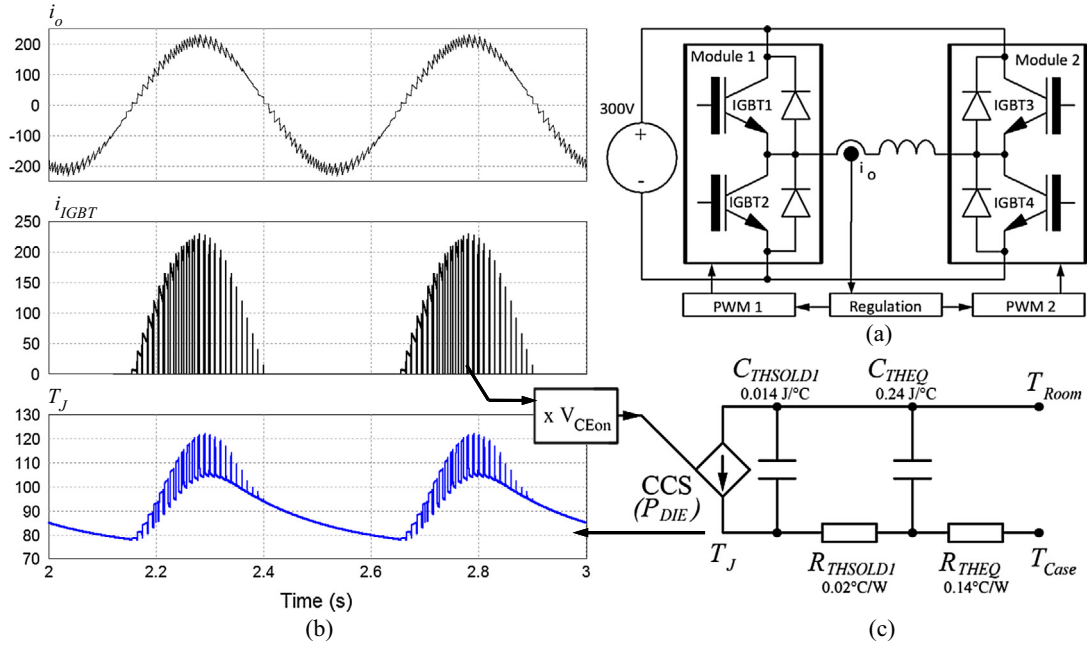

Fig. 3. PWM test bench principle. (a) Bridge power stage, (b) simulated waveforms and (c) simplified thermal model for simulations.

– Conversely, if the cycling period is lower than the lowest time constant, there is no power cycling and $\Delta T_J \approx \Sigma\, R_{TH}\, P_{DieAv}$.

The model in Fig. 4(a) can be simplified as shown in Fig. 4(b), a reduction that has been validated through simulation. In addition, the first time constant is 100 times lower than the second, enabling the assumption to be made that time t_A, response time of the first stage, is negligible compared to time t_B (Fig. 5(a)) and that the temperature variation $\Delta T_{J1} = R_{THSOLD1}\, P_{DieM}$ is reached immediately. In that case, the part ΔT_{J2} is mainly due to the response of network R_{THEQ}, C_{THEQ} and an analytic calculation is possible:

$$T_{Case} = \frac{1 - e^{-\frac{1-D}{F_{PC}\cdot\tau_{EQ}}}}{1 - e^{-\frac{1}{F_{PC}\cdot\tau_{EQ}}}} T_{Ref} + (T_{Ref} - R_{THEQ} P_{DieM}) \frac{e^{\frac{D}{F_{PC}\cdot\tau_{EQ}}} - 1}{e^{\frac{1}{F_{PC}\cdot\tau_{EQ}}} - 1} \quad (1)$$

where T_{Ref} is the minimal value of T_J on a cycle

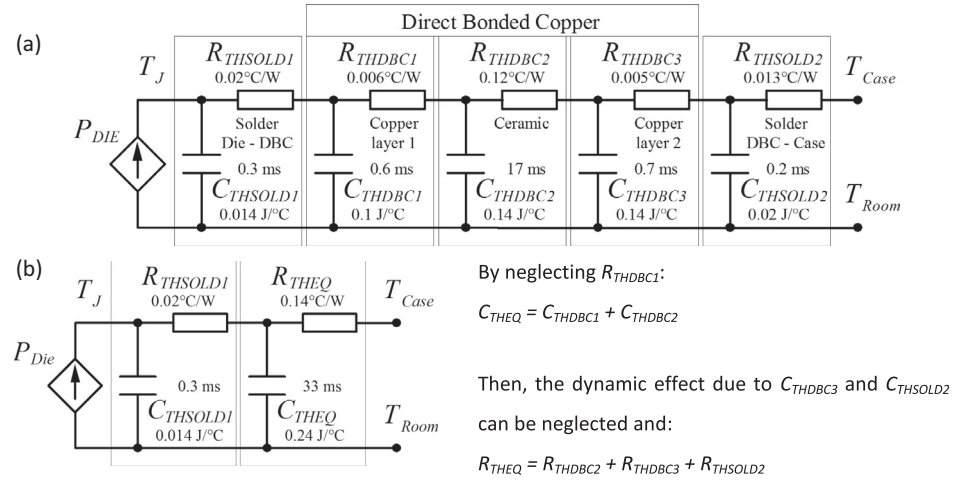

Fig. 4. Thermal equivalent circuits of the considered module. (a) Complete circuit and (b) reduced circuit.

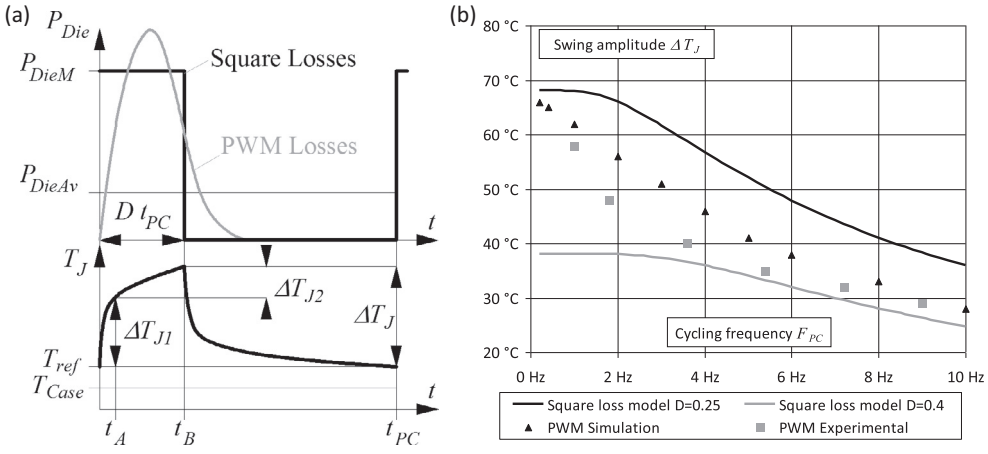

Fig. 5. Power cycling frequency. (a) Simplified representation of power cycling conditions. (b) Range of the possible cycling frequency.

$$\Delta T_J = R_{THSOLD1} P_{DieM} + (T_{Ref} - T_{Case} - R_{THEQ} P_{DieM}) \left(e^{-\frac{D}{F_{PC} \cdot \tau_{EQ}}} - 1 \right) \qquad (2)$$

with F_{PC}, cycling frequency, $\tau_{EQ} = R_{THEQ} \cdot C_{THEQ}$, $D = t_B/t_{PC}$.

Eq. (1) shows that T_{Case} must be adjusted (thermal exchanger) to obtain a fixed temperature T_{ref} with fixed values of P_{DieM}, and F_{PC}. Then ΔT_J is determined by these values and the module's thermal behavior (Eq. (2)).

The curve "Square loss model" in Fig. 5(b) shows the evolution $\Delta T_J(F_{PC})$ obtained with this simplified modeling. In both cases, the average losses P_{LossAv} are equal to 100 W, a typical acceptable value for the modules in question. It appears that decreasing duty cycle and increasing power pulse magnitude at the same time is a means to increase the temperature swing without increasing average losses. The shape of the real die losses due to modulation is clearly different, as shown by the qualitative representation (PWM losses) in Fig. 5(a). To verify that previous results are relevant, simulations using the configuration in Fig. 3 were performed by adjusting a value of average die losses always equal to 100 W. The result is given in Fig. 5(b) ("PWM simulation"), confirming that the trend obtained with simplified modeling is correct.

The experimental curve $\Delta T_J(F_{PC})$ obtained with the considered IGBT modules in the test bench operating in high frequency mode, with average losses of 100 W in each IGBT die, is given Fig. 5(b). This curve presents good consistency with calculated and simulated curves and confirms the capability of the test bench to perform power cycling tests using the highest cycling frequencies attainable.

In addition, it can be observed that the PWM mode is a good means for providing power cycling due to its high shape factor P_{LossM}/P_{LossAv}.

The limitation on cycling frequency is the main observation resulting from this analysis. Whatever the principle of the test bench may be, cycling frequency values higher than 10 Hz lead to swing amplitude lower than 30 °C if reasonable values of average die losses are used.

The thermal characteristics of the tested module being representative of this device family, the trends observed in the present analysis can be generalized to various IGBT modules. It can be concluded that the frequency range of 1–10 Hz gives a good indication regarding faster power cycling protocols that can be applied to this kind of power device.

Publications on that subject mention mainly test benches operating in on–off mode under low voltage [9–19]. Cycling frequencies vary between 1 Hz for the fastest and 0.01 Hz for the slowest. None of them reaches the maximum frequency identified previously. In most cases, ΔT_J is higher than 50 °C and the data concerning lower swing amplitudes are very rare [10].

The test bench presented here operates modules under real conditions and is able to generate different cycling modes, from a few 0.01 Hz to a few dozen Hertz, implementing the means described in the next paragraph.

2.3.2. Low frequency protocols in the present test bench

This method has been applied successfully for many years [22] in projects imposing low frequency power cycling protocols. Power cycling is generated by a low-frequency on–off operating mode of the PWM inverter (around a few 0.01 Hz).

During the on-phase, the inverter operates as described in Fig. 3, with a maximum value of the sinusoidal current adjustable up to 200 A and a high modulation frequency (100 Hz). During the off-phase, the inverter is simply stopped, the current i_o is null. This operation corresponds approximately to the generation of square losses (Fig. 5(a)) at a low cycling frequency.

Fig. 6 shows a simulation of this mode. There, the on–off mode is the main cause of temperature variation, and the contribution due to the modulation frequency (zoom window) is negligible.

In that case, the power cycling period is realistic with respect to applications, but the technique involves high intrinsic test durations that can be only reduced by using high temperature swings.

2.3.3. High frequency protocols in the present test bench

These protocols were evaluated to reduce test duration, especially for low thermal swing amplitudes. The method simply benefits from temperature variation due to PWM modulation, as was demonstrated in the previous section. The on–off mode is no longer used and the modulation frequency is reduced in the range identified above (1–10 Hz) to increase temperature variations up to values compatible with the desired tests.

Fig. 7 shows the experimental temperature swing measured with an infrared camera under the test condition with 2 Hz PWM modulation. Measurement is obtained by acquiring a few dozen thermal frames over the modulation period and by averaging the die surface temperature on each frame after extracting the data corresponding to the wire bond zones. Here, the amplitude variation is close to 40 °C.

To be efficient, the fast ageing protocols have to be completed by fast measurement of the ageing parameters. Therefore, this part must be automated and the solutions chosen to perform this task are presented in Section 3.

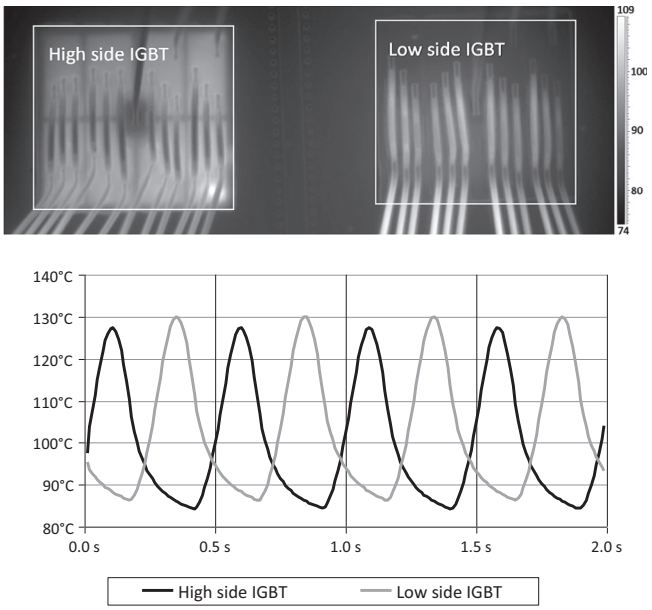

Fig. 7. Experimental junction temperature in fast power cycling.

3. On-line [T_J, V_{CEo}] measurements

3.1. Principle and hardware

To carry out ageing tests under the power cycling conditions described above, ageing indicators must first be identified and then measured regularly throughout the test [4,23–30]. The most

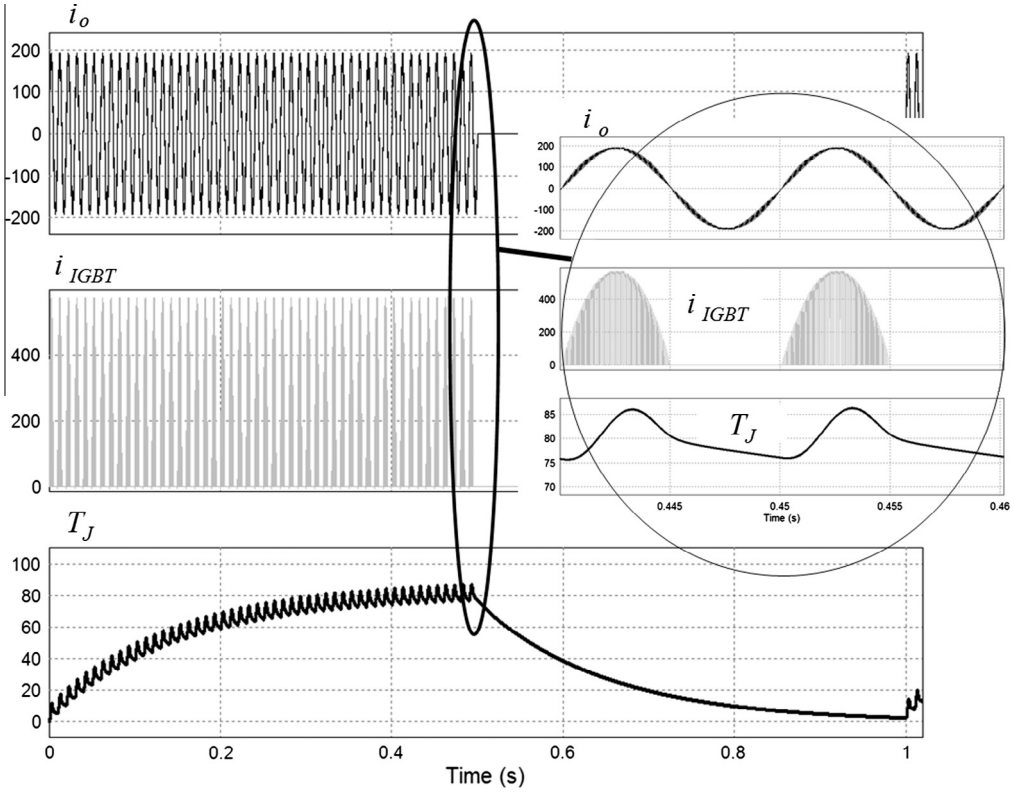

Fig. 6. Low frequency protocol using on–off mode.

frequently-used indicator is the on-state voltage across the IGBT that enables detection of wire bond and metallization degradations. This indicator is retained in the tests considered here, chosen to measure values on-line and thus drastically reduce the manpower required to oversee tests.

This on-line V_{CE} measurement is critical. It must be carried out under strictly-controlled temperature and current conditions (125 °C and 100 A in the present tests; value referred as V_{CEo} to monitor the same operating point regularly. Measurement must be extremely accurate (uncertainty lower than 1%) to detect very low V_{CEo} variations at this operating point, thus revealing the degradations mentioned above. A major difficulty is the insertion of instrumentation devices able to provide that accuracy in power stages supplied by high voltage, and in which currents and temperatures vary periodically. In the considered test bench, it is possible to modify the PWM control to insert the measurement process, as the changes introduced in the time scale of some switching periods have no significant effect on the thermal stress generated by the test bench.

Therefore, repetitive V_{CEo} measurements must be made under constant current and temperature conditions. The first choice for this issue is to measure temperature indirectly via V_{CE} [10,17]. This requires preliminary characterization of each die as shown Fig. 8, which is relatively easy to achieve, performed under a low current level (100 mA in the present case) to eliminate the voltage drop due to the connections, and under a constant voltage V_{GS} (15 V). This current value is then used for all indirect temperature measurements performed during the test, to make them independent from connection ageing.

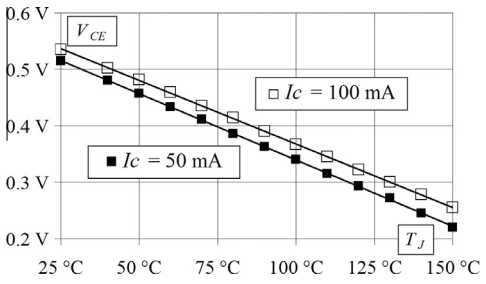

Fig. 8. V_{CE} thermal sensitivity curves.

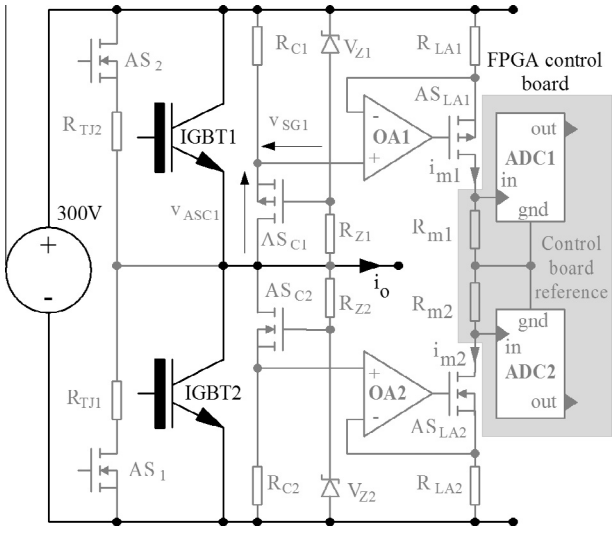

Fig. 9. V_{CE} measurement schematic.

On that basis, the proposed instrumentation structure is shown in Fig. 9. For simplification of the schematic parallel diodes are not drawn. This structure uses two stages, one for the high side IGBT and one for the low side IGBT.

Each stage includes a V_{CE} clamp (V_{Z1}, R_{Z1}, AS_{C1}, R_{C1} and V_{Z2}, R_{Z2}, AS_{C2}, R_{C2}) to limit the measured voltage when IGBTs are in an off-state, a 100 mA current sink for indirect temperature measurement (AS_1, R_{TJ1} and AS_2, R_{TJ2}), and a voltage-level shifter ($OA1$, AS_{LA1}, R_{LA1}, R_{m1} and $OA2$, AS_{LA2}, R_{LA2}, R_{m2}). All these devices are implemented near the IGBT power module. Another identical measurement board is associated with the two other IGBTs.

Voltage clamp. The principle can be deduced (example of the high stage) from the following equations:

$$V_{RC1} = V_{CE} - v_{ASC1} = V_{Z1} - V_{SG1} \tag{3}$$

$$V_{SG1} = V_{Z1} - V_{CE} + v_{ASC1} \tag{4}$$

If AS_{C1} is in an on-state, voltage V_{RC1} is equal to V_{CEo} (3), the AS_{C1} R_{DSON} being widely lower than R_{C1} (3 Ω versus 10 kΩ). AS_{C1} is in an on-state if $V_{Z1} - V_{CE} + v_{ASC1} \geqslant V_{SGTH1}$ (4), i.e. when V_{CE} is low, V_{SGTH1} being the threshold voltage of AS_{C1}. When V_{CE} increases, and then reaches the value $V_{Z1} - V_{SGTH1}$, AS_{C1} begins to operate in linear mode, the clamping mode is active and the high voltage is then applied to A_{SC1} and R_{Z1}. Therefore, the voltage clamp value is close to $V_{Z1} - V_{SGTH1}$ (10 V here) and the voltage across R_{C1}, A_{O1} (referenced to the DC positive rail) and R_{LA1} is limited to this value.

This clamp circuit avoids any threshold diode voltage.

100 mA Current sink. With the 300 V DC voltage being provided by a regulated voltage power supply (0.1%), the 100 mA current is simply determined by fixing the value of resistors R_{TJ1} and R_{TJ2} (3 k, tolerance 1%). The current injection into IGBT1 or IGBT2 is performed by turning on A_{S1} or A_{S2} respectively. The consumption of the stage V_{Z1}, R_{Z1} is lower than 1 mA and does not introduce significant error.

300 V voltage-to-current converter. The use of a simple 300 V voltage-to-current converter enables providing signal transmission while solving the connection problem between the power stage and the control board.

Through the amplifier $OA1$, voltage V_{RC1} (V_{CEo} clamped) is reproduced on the resistor R_{LA1}, which generates a current i_{m1} equal to V_{RC1}/R_{LA1} and conveyed by AS_{LA1}. AS_{LA1} also absorbs the high voltage variations.

The principle allows transmitting the V_{CEo} voltage information through high current values (i_{m1} and i_{m2}, a few dozen mA) to the FPGA control board's analog-to-digital converters, with the benefit of a high immunity transmission.

In addition, they avoid introducing galvanic insulation stages, the electrical reference thus being that of the FPGA control board, floating with respect to the power stage. This floating control board reference imposes an inverted signal on the ADC2 input, which is easily solved by setting the correct ADC configuration.

To perform measurements, the IGBTs must be disconnected from the load, therefore the current flowing through both legs must be deviated. Additional MOSFETs (S_1) and IGBTs (S_2) introduced in the load line allow these operations to be performed (Fig. 10) respectively in a very short period of time (<1 μs) in order to avoid die temperature decrease. The switch S_1 is made of MOSFETs because the low voltage switching function requires a very low voltage-drop (conduction of the load current in normal operation).

The switch S_2 uses the IGBT because it is subject to the inverter voltage (±300 V) in normal operation, while it has to conduct the load current during the transient free-wheeling phase.

3.2. V_{CEo} (I_C, T_J) measurement strategy

3.2.1. Objective

This measurement is needed to track IGBT state evolution with respect to ageing [22,29]. It does not need to be made at each thermal cycle. Its periodicity can be adjusted during the test, from a low value (for example, 1000 cycles) at the beginning to a higher value (for example, 100 cycles) when degradation appears.

This periodic V_{CE} measurement must always be made for the same fixed I_C current (here, 100 A) and the same fixed junction temperature (here, 125 °C) in order to obtain an ageing indicator.

3.2.2. Accuracy requirements and corresponding achievements

To detect wire bond degradations (crack or lift-off), V_{CEo} (100 A, 125 °C) variation around 10 mV must be detected, ideally. The V_{CE} value obtained for the 100 A collector current being included into a [1.2–1.4 V] range, the required relative uncertainty is close to 1%.

In addition, the accuracy of temperature measurement (125 °C) must be considered. For a current value of 100 A, a temperature variation of 38 °C leads to a V_{CE} variation of 25 mV (Fig. 8), i.e. a sensitivity of 0.7 mV/°C. Therefore, an error of a few degrees Celsius on the junction temperature creates an error on V_{CEo} (100 A, 125 °C) measurement significantly lower than the expected 10 mV detection level.

Lastly, respecting 1% and 5% relative uncertainties respectively on V_{CE} measurement and on temperature measurement should enable this coupled measurement to be performed correctly. Actually, the acquisition chain used in the present system is more efficient. It is based on a multiplexed 16 bit −1 MHz ADC offering $a \pm 10$ V input voltage range. In the measurement schematic in Fig. 9, each side uses a half voltage range, 0/10 V for the high side, 0/−10 V for the low side. Therefore, the theoretical resolution is 0.15 mV, i.e. a relative uncertainty of 0.015% with respect to the V_{CE} value close to 1 V. The main limitation of the chain is due to the 0.1% tolerance of resistors $R_{LA1,2}$ and $R_{m1,2}$ that leads to a relative uncertainty of 0.2% on V_{CE} measurement.

The accuracy of temperature measurement depends mainly on the previous accuracy, but the influence of the low current (100 mA) required for indirect measurement must also be considered. From the curves in Fig. 8, it can first be deduced that the thermal sensitivity is close to −2 mV/°C and then, that the sensitivity with respect to the current is close to 0.5 mV/mA, by comparing both curves.

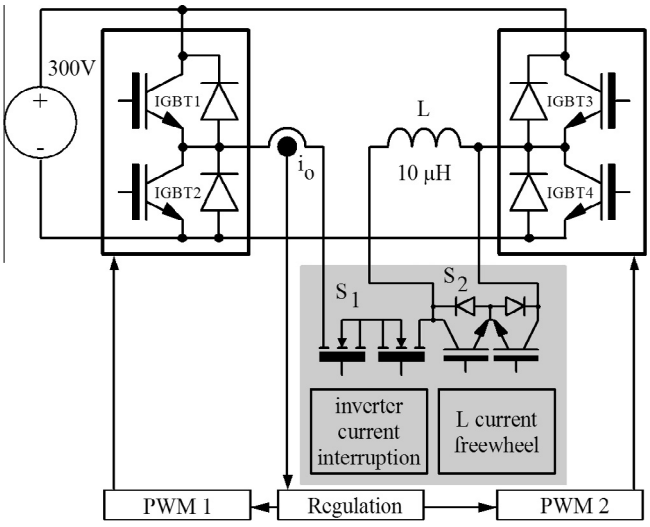

Fig. 10. Power stage arrangement.

Considering the −2 mV/°C sensitivity, V_{CE} measurement accuracy and resolution are sufficient to detect a variation lower than 1 °C. Therefore, it is the control of the low current level that could limit accuracy. As indicated in the previous circuit description, the characteristic of the DC power supply and the resistor tolerance lead to a relative uncertainty close to 1% (1 mA), therefore to an uncertainty of 0.5 mV on V_{CE} measurement, which is negligible.

3.2.3. Operation

To reach the objective, the measurement process in Fig. 11 is performed. Normal test operation is stopped and a particular switching sequence is introduced (buck operation) to make the switch current and junction temperature vary around the fixed values. Indeed, it is not possible to impose the right operating point directly. For example, to make the measurement on IGBT1, IGBT1 is maintained in an on-state while IGBT4 switches (20 kHz) to create a current variation around 100 A.

A few dozen values of $V_{CE}(I_C, T_J)$ are acquired and stored. IGBT4 switching is then stopped; S_2 is switched on; S_1 is switched off; and an indirect temperature reading is taken immediately, available for all the acquired values because the case temperature does not vary significantly (0.1 °C/ms) during the acquisition sequence. The latter yields a first $V_{CE}(I_C, T_{J1})$ characteristic for a given temperature T_{J1}. It is important to emphasize that, by the means of S_1, S_2, IGBT1 can be maintained in an on-state during this entire sequence, its gate voltage state remains constant, and 100 A/100 mA switching can be very fast, if the 100 mA injection is anticipated.

The buck operation is then restarted for a few dozen ms to increase the case temperature, and a second acquisition sequence is carried out, providing a second characteristic for a second temperature T_{J2}. Lastly, three characteristics are built successively. The desired value is extracted from this family by interpolation made in parallel after restarting normal operation.

The duration of the complete measurement cycle is around 0.5 s if the initial case temperature is greater than 70 °C, i.e. if the test bench was in steady-state operation immediately prior.

Fig. 12 shows an example of a measurement series made around 100 A and 125 °C. The point V_{CEo} (100 A–125 °C) is extrapolated from the nearest results, corresponding here to junction temperature values of 117 °C and 133 °C.

3.3. T_J measurement strategy in operation

3.3.1. Objective

In this case, the target is the measurement of the thermal swing generated by the modulation (a few Hz) to initially adjust and verify power cycling conditions regularly. Therefore, several indirect measurements of the junction temperature must be made over the modulation period. In the case of a steady-state, a sub-sampling strategy can also be applied by making one indirect measurement on several modulation periods with a different sampling time for each period.

3.3.2. Accuracy requirements and corresponding achievements

To adjust the amplitude of the thermal swing for a given protocol, varying between 30 °C and 50 °C, an uncertainty of 1 °C is broad enough. Such accuracy is compatible with the characteristics of the acquisition chain described above, used again to provide this temperature measurement.

3.3.3. Operation

Indirect measurement is achieved by stopping normal operation for a short time (a few switching periods) to inject the 100 mA current into the chosen IGBT.

To generate this acquisition window, the control sequence for the different IGBTs and switches is identical to that described in

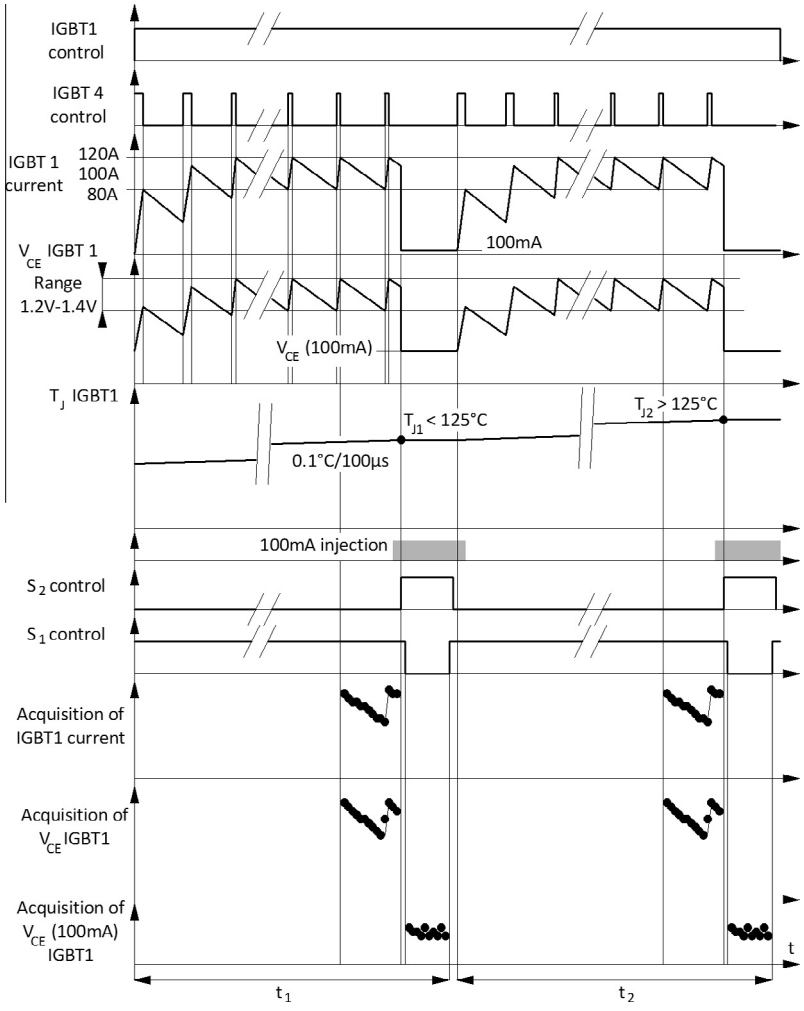

Fig. 11. V_{CEo} measurement sequence.

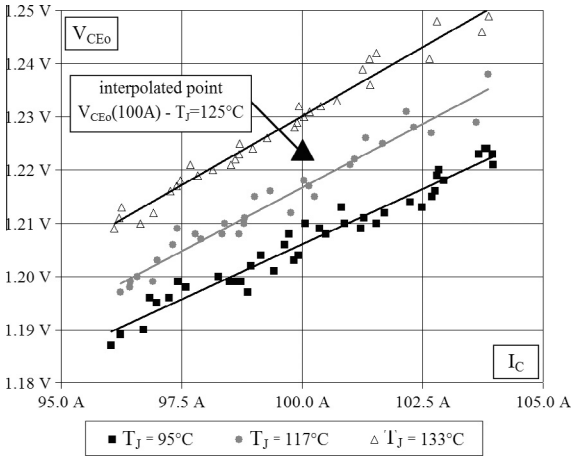

Fig. 12. On-line measurements of $V_{CEo}(I_c)$ on IGBT for three temperatures.

the previous section. During the window, 20 values of V_{CE} (100 mA) are acquired and stored at the sampling frequency of 500 kHz. The acquisition is delayed from 100 µS after the interruption to allow the IGBT to reaching electrical equilibrium (carrier recombination) for the 100 mA current. This delay does not generate a significant error on the measured temperature ($\leqslant$0.5 °C).

These values are then used to generate one sample by averaging, in the end converted into a temperature value by using the intrinsic thermal characteristics of the considered IGBT.

The proposed approach is applied to the test bench operating with two variants. The first variant, direct sampling mode, corresponds to the simulation in Fig. 13. Ten groups of twenty V_{CE} samples are acquired on one modulation period. Fig. 13 shows that the interruption effect on the junction temperature is weak (variations of a few degrees), and therefore that the variant is applicable (in case of low-frequency modulation) and does not require steady-state operation. Fig. 14(a) presents a Labview window showing the raw temperature reconstructed from V_{CE} measurements over the modulation period.

Fig. 14(b) offers a comparison between the temperature measurements obtained with the infrared camera and with direct V_{CE} sampling mode, after data processing. The results exhibit good consistency.

The second variant, limited to steady-state conditions, uses a sub-sampling method. The ten previous groups of twenty samples are acquired on ten successive modulation periods to reconstruct the junction temperature profile. This sub-sampling mode allows measuring the temperature swing generated by higher modulation frequencies (>5 Hz), while avoiding any influence of the interruption on the temperature swing period.

To verify the assumption concerning the low impact of direct sampling mode on the temperature swing, the results obtained

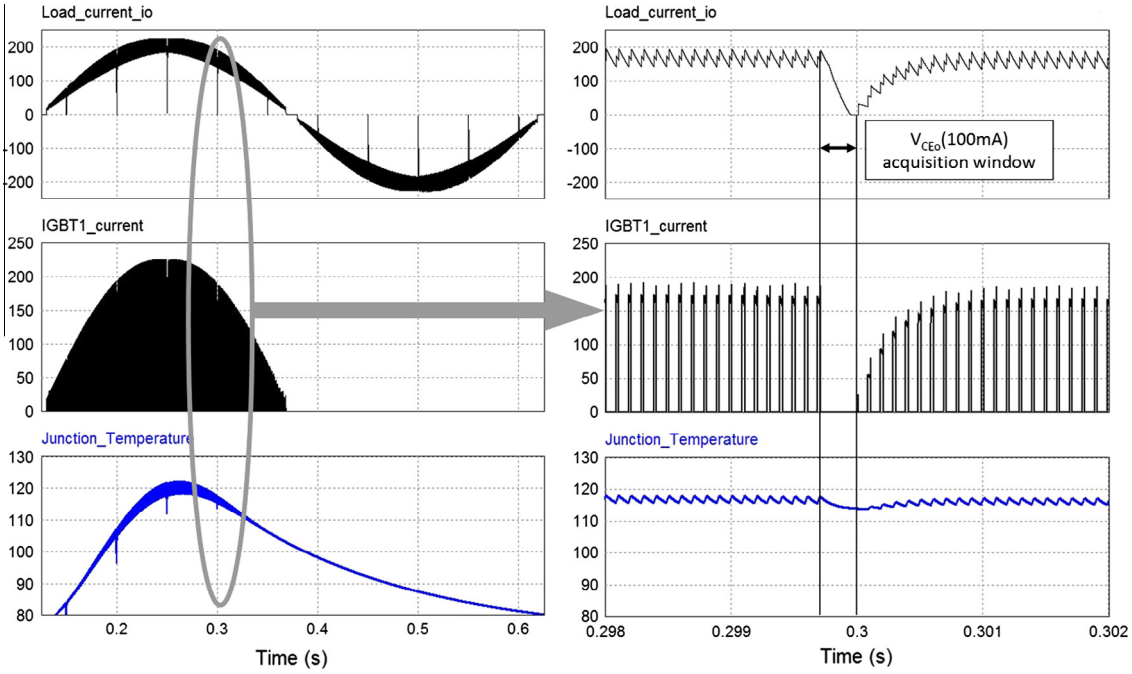

Fig. 13. Simulated effect of measurement interruptions on the junction temperature.

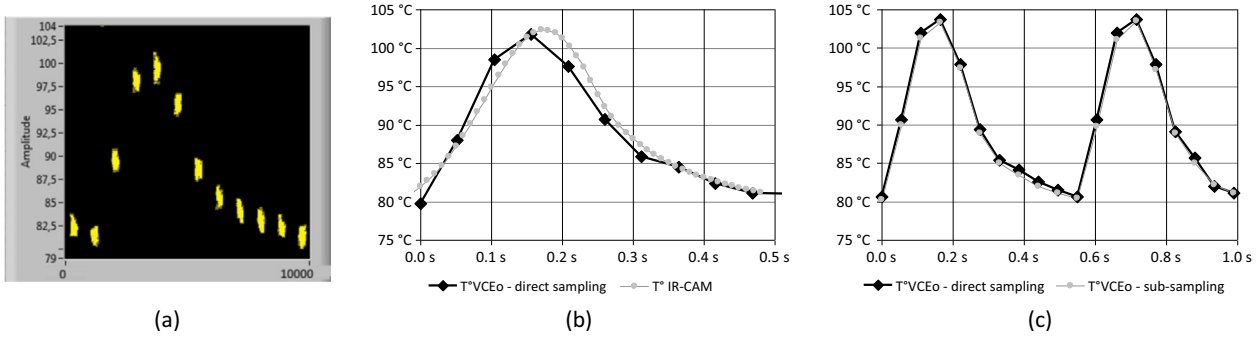

Fig. 14. Temperature swing measurement. (a) Raw measurement, (b) comparison of direct sampling mode and IR camera measurement and (c) comparison of direct sampling and sub-sampling modes.

in both cases were compared, for the same operating conditions [T_{Case} = 80 °C, I_{CMax} = 140 A, V_{DC} = 300 V, F_{mod} = 2 Hz].

Fig. 14(c) shows the comparison. Values are very similar in both configurations, confirming the previous assumption.

4. Experimental results

Currently, four test blocks equipped with the automated measurement system are available, allowing eight modules to be tested simultaneously. Fifty modules were tested for approximately one year.

4.1. Result presentation

Table 1 contains a list of twenty-seven aged module samples with the main information concerning the tests, i.e. thermal condition, lifetime, and the reason for the test stop.

In accordance with test bench abilities, the junction thermal swings are included in the range [30–52 °C], adjusted by current amplitude and switching frequency, while most of the tests were made with a modulation frequency of 2 Hz and a reference temperature of 80 °C. The test stop is determined by a V_{CEo} increase of a few percent. The last column in Table 1 gives the percentage value increase for each IGBT in the module. Sometimes only one is mentioned if the degradation concerns only one IGBT die of the two mounted in the module. An example of V_{CEo} drift illustrates measurement robustness.

The first observations that can be made by looking at these results are as follows:

- The fast testing method shows promise, with lifetime values being consistent. In addition, results are highly reproducible.
- Higher lifetime values are close to 10,000,000 cycles. Such results would be very difficult to obtain with classical tests because of their duration. With the fast testing method, combined with the automated measurement system, a sample reaches this lifetime in only three weeks.
- For the lower values of ΔT_J, lifetime is very sensitive with respect to the thermal swing amplitude that is consistent with the trend generally observed (exponential lifetime model).
- For the higher temperature swings, in some case, the device is destroyed before any detection of significant V_{CEo} evolution. This effect corresponds to an acceleration of degradation that occurs between two V_{CEo} monitoring sequences.

Table 1
Test results on twenty-seven samples.

	Sample	ΔT_J (°C)	Lifetime	Stop reason
1	SAMP004	52.0	713,906	V_{CE} Increase, 4%
2	SAMP005	52.0	797,198	V_{CEo} increase, 4% and 2%
3	SAMP006	52.0	746,942	V_{CEo} increase, 1.5% and 2%
4	SAMP007	52.0	663,650	V_{CEo} increase, 4% and 2.5%
5	SAMP008	52.0	621,128	V_{CEo} increase, 2.5%
6	SAMP009	52.0	621,128	V_{CEo} increase, 4.5%
7	SAMP010	52.0	598,516	Die destruction
8	SAMP011	52.0	570,000	Die destruction
9	SAMP012	52.0	620,000	Die destruction
10	SAMP018	41.0	1,548,000	V_{CEo} increase, 4% and 2.5%
11	SAMP025	41.0	1,402,000	V_{CEo} increase, 1% and 6.5%
12	SAMP024	40.0	1,752,971	V_{CEo} increase, 5.5% and 2.5%
13	SAMP026	40.0	1,634,589	V_{CEo} increase, 1% and 4%
14	SAMP021	39.5	1,646,231	V_{CEo} increase, 3.5% and 5%
15	SAMP027	39.5	1,816,490	V_{CEo} increase, 5% and 1%
16	SAMP028	39.5	1,917,049	V_{CEo} increase, 2.5% and 3%
17	SAMP029	39.0	2,467,261	V_{CEo} increase, 5% and 10%
18	SAMP016	38.5	3,033,662	V_{CEo} increase, 5% and 5%
19	SAMP019	38.0	3,455,658	V_{CEo} increase, 5% and 2.5%
22	SAMP031	35.0	5,763,256	Die destruction
23	SAMP032	35.5	5,763,256	V_{CE} increase, 5–1.5%
24	SAMP036	31.5	9,140,000	V_{CE} increase, 4%
25	SAMP037	32.0	9,140,000	V_{CE} increase, 3.5–2.5%
26	SAMP044	52.0	550,000	V_{CE} increase, 5–6%
27	SAMP045	52.0	550,000	V_{CE} increase, 5–6%

These modules were opened and analyzed with an SEM. Degradations are identical for all modules and concern only the wire bonds. The views in Fig. 15 show the typical damage suffered by the devices that focus on wire bond attaches and eventually generate lift-off. No degradation of emitter metallization was observed. To be sure that this behavior is not due to module technology, one sample from another manufacturer, using the same IGBT dies, was tested (SAMP010). The result is identical.

4.2. Comparison with previous tests

In previous projects, of which the main results are presented in [22,29], a few dozen samples were aged with higher thermal swings (between 60 °C and 90 °C) and with lower cycling frequencies (around 0.02 Hz), by using the test bench in on/off mode. These results cannot be detailed here again, but two significant points of comparison can be established.

The first point concerns the difference of degradations observed in both testing phases. In the previous projects, four degradation modes occurred, namely metallization degradations and wire bond foot cracks/heel cracks/liftoff cracks (Fig. 16). These modes coexisted with a combination depending on the thermal swing. As mentioned above, only the liftoff mode was observed in the present testing phase. For now, it is not possible to draw definitive conclusions because of the difference in thermal swing amplitudes.

The second point is the respective positions of the different samples in a lifetime graph. From the results obtained in the previous testing phase at low cycling frequency, a modified Coffin-Manson model [10] was established as follows:

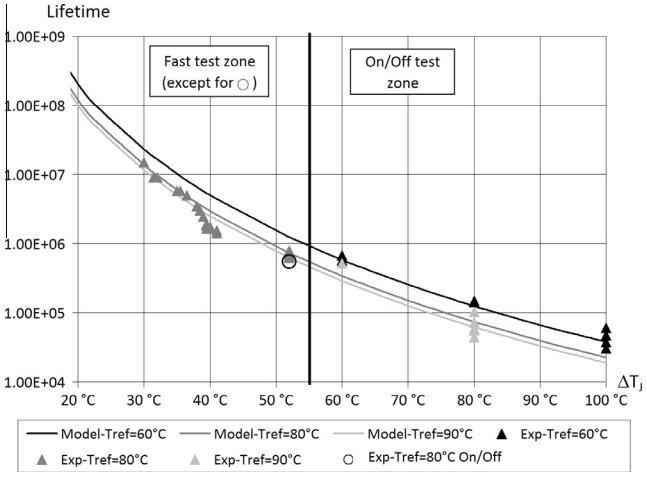

Fig. 17. Lifetime graph.

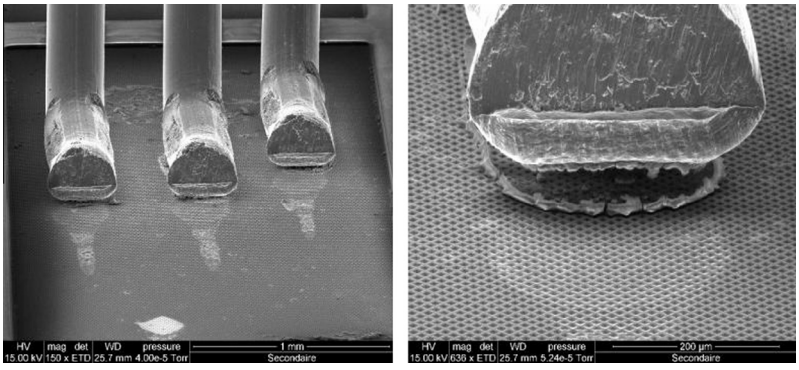

Fig. 15. Wire bond degradations.

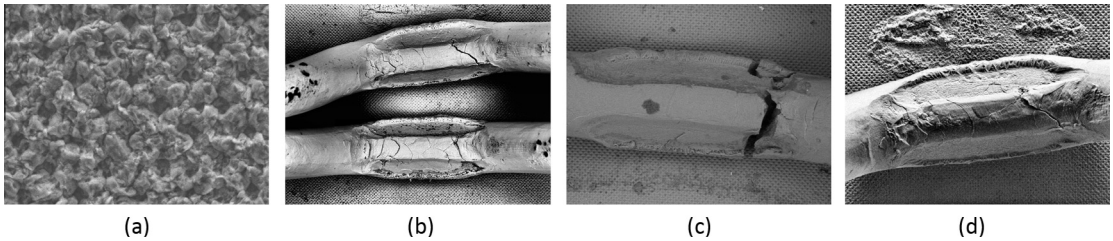

Fig. 16. Modes of degradations observed in previous tests, (a) metallization, (b) foot crack, (c) heel crack and (d) liftoff.

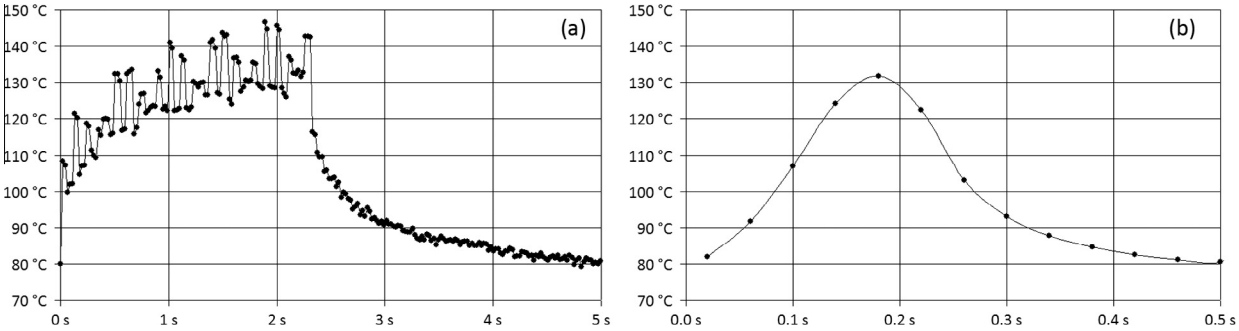

Fig. 18. Compared Junction temperatures, (a) low frequency test −0.2 Hz and (b) high frequency test −2 Hz.

$$N = \frac{K}{\Delta T_J^{v}} exp\left(\frac{T_a}{T_{ref}}\right), \quad \text{with } K = 2.13 \times 10^{14},\ v = 5.33,\ T_a = 126°C \tag{5}$$

The corresponding lifetime curves versus ΔT_J and T_{ref} are shown Fig. 17. The experimental points from which the model parameters were extracted are localized in the right-hand part of the graph, where the temperature swing amplitudes are higher or equal to 60 °C. The experimental results of the present testing phase were added to the same graph and are localized in the left-hand part.

Despite differences observed on the degradation modes, and the difference in cycling frequencies, the new results are very close to the model elaborated before they had been obtained. It is a good but paradoxical sign concerning the consistence of these new results, but once again, a definitive conclusion cannot be drawn from this observation.

4.3. Impact of power cycling frequency

The impact of the cycling frequency is a critical issue regarding the consistency of faster test protocols. If degradation modes and lifetimes are not preserved while the cycling frequency increases, the test applicability is not demonstrated. As mentioned above, the results given by the two testing phases cannot be compared. Therefore, a new test was used to perform a comparison between both methods (on/off mode and PWM modulation mode). Two samples (SAMP044 and SAMP045) were aged with the same parameters (current, voltage, thermal swing amplitude, reference temperature) as SAMP004–SAMP012, but with the on/off mode implemented with a 0.2 Hz cycling frequency (ten times lower). The compared shapes of thermal swings generated in both cases are shown Fig. 18.

As it can be observed in Table 1, the lifetimes are very close in both cases. The average lifetime calculated from SAMP004 to SAMP012 is around 660,000 cycles and the lifetime of SAMP44 and SAMP45 is 550,000 cycles. In addition, the degradations observed by SEM are very similar (wire bond attach degradation and liftoff). This result does not confirm the observations made in previous publications [7,31], in which lifetime increases when cycling frequency increases. The test conditions being strongly different, it is necessary to be careful about premature conclusions. Additional investigation on this issue must be a priority for future works, and the present test bench is a good tool to do that. If the trend identified here is confirmed, the interest of results provided by this fast testing method will be fully demonstrated.

5. Conclusion

This paper presents two complementary developments in the field of power cycling tests dedicated to IGBT devices.

The first is the implementation of fast testing protocols based on junction temperature variations induced by Pulse Width Modulation operation in an inverter bridge built with two samples. By using this technique, the IGBT modules are placed in realistic operating conditions and a wide range of test parameters can be covered, while minimizing test duration.

The second development is the automation of the measurement system to fully benefit from the fast testing method by avoiding test stops in order to measure the indicator V_{CEo}. The acquisition chain, based on a floating V_{CE} measurement stage using an active clamp without threshold, a current signal transmission and a 16-bit analog-to-digital conversion, performs the measurements with an accuracy in accordance with test requirements. As a consequence, the monitoring system can automatically perform the periodic characterizations needed to detect possible IGBT module degradations while the test bench continues to operate.

The combination of the fast testing method and automated measurement offers an opportunity to obtain significant numbers of ageing samples in a short period of time and with a stress range unattainable with classical methods.

This ability has been used to test several dozen samples over a few months in a [30–52 °C] range of temperature swing amplitude. A first analysis, supported by a comparison between fast and classical ageing modes, shows a good consistency of these results.

References

[1] Xiong Y, Cheng X, Shen ZJ, Mi C, Wu H, Garg VK. Prognostic and warning system for power-electronic modules in electric, hybrid electric, and fuel-cell vehicles. IEEE Trans Ind Electron 2008;55(6):2268–76.
[2] Lezana P, Pou J, Meynard TA, Rodriguez J, Ceballos S, Richardeau F. Survey on fault operation on multilevel inverters. IEEE Trans Ind Electron 2010;57(7):2207–18.
[3] Ceballos S, Pou J, Robles E, Gabiola I, Zaragoza J, Villate JL, et al. Three-level converter topologies with switch breakdown fault-tolerance capability. IEEE Trans Ind Electron 2008;55(3):982–95.
[4] Rodríguez-Blanco MA, Claudio-Sánchez A, Theilliol D, Vela-Valdés LG, Sibaja-Terán P, Hernández-González L, et al. A Failure-detection strategy for IGBT based on gate-voltage behavior applied to a motor drive system. IEEE Trans Ind Electron 2011;58(5):1625–33.
[5] Wagenitz D, Westerholz A, Erdmann E, Hambrecht A. Power cycling test bench for IGBT power modules used in wind applications. In: Proceedings of the 14th european conference on power electronics and applications (EPE 2011), 2011. p 1–10.
[6] Ciappa M. Selected failure mechanisms of modern power modules. Microelectron Reliab 2002;42(4–5):653–67.
[7] Bayerer R, Licht T, Herrmann T, Lutz J, Feller M. Model for power cycling lifetime of IGBT modules – various factors influencing lifetime. In: Proceedings of 5th international conference on integrated power electronics systems, November 2008. p. 37–42.
[8] Khatir Z, Lefebvre S. Boundary element analysis of thermal fatigue effects on high IGBT power modules. Microelectron Reliab 2004;44:929–38.
[9] Wu W, Gao G, Dong L, Wang Z, Held M, Jacob P, Scacco P. Thermal reliability of power insulated gate bipolar transistor (IGBT) modules. In: Proceedings of the 12th IEEE SEMI-THERM symposium, 1996. p. 136–41.
[10] Held M, Jacob P, Nicoletti G, Scacco P, Poech M-H. Fast power cycling test for IGBT modules in traction application. In: Proceedings of conference on power electronics and drive systems confer, May 1997; vol. 1. p. 425–30.

[11] Auerbach F, Lenniger A. Power-cycling stability of IGBT-modules. In: Proceedings of the IEEE industry applications annual meeting, 1997. p. 1248–52.
[12] Hamidi A, Coquery G, Lallemand R. Reliability of high power IGBT modules testing on thermal fatigue effects due to traction cycles. In: Proceedings of the 7th european conference on power electronics and applications, 1997; vol. 3. p. 118–23.
[13] Hamidi A, Beck N, Thomas K, Herr E. Reliability and lifetime evaluation of different wire bonding technologies for high power IGBT modules. Microelectron Reliab 1999;39:1153–8.
[14] Hamidi A, Coquery G. Effects of current density and chip temperature distribution on lifetime of high power IGBT modules in traction working conditions. Microelectron Reliab 1997;37(10/11):1755–8.
[15] Coquery G, Lallemand R. Failure criteria for long term accelerated power cycling test linked to electrical turn off SOA on IGBT module. A 4000 h test on 1200 A–3300 V module with AlSiC base plate. Microelectron Reliab 2000;40(8-10):1665–70.
[16] Morozumi A, Yamada K, Miyasaka T, Seki Y. Reliability of power cycling for igbt power semiconductor modules. IEEE Trans Ind Appl 2003;39(3):665–70.
[17] Coquery G, Lefranc G, Licht T, Lallemand R, Seliger N, Berg H. High temperature reliability of automotive power modules verified by power cycling tests up to 150 C. Microelectron Reliab 2003;43:1871–6.
[18] Khatir Z, Ousten JP, Badel F, Dupont L, Lefebvre S, Bouarroud M. Degradation behavior of 600 V–200 A IGBT modules under power cycling and high temperature environment conditions. Microelectron Reliab 2007;47:1719–24.
[19] Bouarroud M, Khatir Z, Ousten J-P, Lefebvre S. Temperature-level effect on solder lifetime during thermal cycling of power modules. IEEE Trans Dev Mater Reliab 2008;8(3):471–7.
[20] Vallon J, Richardeau F, Feral H, Cheron Y, Forest F, Huselstein J-J, Joubert C. Converter topology for reliability test bench dedicated to PWM inverters. In: Proceedings of 10th EPE conference (EPE2003), 2003. p. 1–10.
[21] Forest F, Huselstein J-J, Faucher S, Elghazouani M, Ladoux P, Meynard T, et al. Use of the opposition method in the test of high power electronics converters. IEEE Trans Ind Electron 2006;53(2):530–41.
[22] Smet V, Forest F, Huselstein J-J, Richardeau F, Khatir Z, Lefebvre S, et al. Ageing and failure modes of IGBT modules in high temperature power cycling. IEEE Trans Ind Electron 2011;58(10):4931–41.
[23] Kim YS, Sul SK. On-line estimation of IGBT junction temperature using on-state voltage drop. Proc Ind Appl Conf 1998;2:853–9.
[24] Brückner T, Bernet S. Estimation and measurement of junction temperatures in a three-level voltage source converter. IEEE Trans Power Electron 2007;22(1):3–12.
[25] Barlini D, Ciappa M, Mermet-Guyennet M, Fichtner W. Measurement of the transient junction temperature in MOSFET devices under operating conditions. Microelectron Reliab 2007;47(9–11):1707–12.
[26] Koenig A, Plum T, Fidler P, De Doncker RW. Junction temperature measurement of COOLMOS devices. Power Electron Drive Syst 2007:90–5.
[27] Yang S, Xiang D, Bryant A, Mawby P, Ran L, Tavner P. Condition monitoring for device reliability in power electronic converters: a review. IEEE Trans Power Electron 2010;25(11):2734–52.
[28] Patil N, Celaya J, Das D, Goebel K, Pecht M. Parameter identification for insulated gate bipolar transistor (IGBT) prognostics. IEEE Trans Reliab 2009;58(2):271–6.
[29] Smet V, Forest F, Huselstein J-J, Rashed A, Richardeau F. Evaluation of V_{CE} monitoring as a real-time method to estimate aging of bond wire-IGBT modules stressed by power cycling. IEEE Trans Ind Electron 2013;60(7). 2760–2270.
[30] Beczkowski S, Ghimre S, de Vega ARP, Munk-Nielsen S, Rannestad B, Thogersen P. Online V_{CE} measurement method for wear-out monitoring of high power IGBT modules. 15th Eur Conf Power Electron Appl (EPE2013) 2013:1–7.
[31] Scheuermann U, Schmidt R. Impact of load pulse duration on power cycling lifetime of Al wire bonds. Microelectron Reliab 2013;53:1687–91.