Reliability issues in GaN and SiC power devices

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***Abstract*— GaN and SiC have been widely investigated for future power switching systems with high efficiencies. So far, prototypes of working transistors using these wide bandgap materials have demonstrated the superior performances suggesting the great potential. Remaining tasks for the commercialization include finding niche applications as entry ones with the well-established reliability. In this paper, recent progress of the GaN and SiC power devices developed at Panasonic is reviewed. After reviewing the reliability issues in the conventional transistors, normally-off GaN Gate Injection Transistors (GITs) and SiC Diode-integrated MOSFET (DioMOS) free from the degradations are presented. These state-of-the-art GaN and SiC devices are very promising for practical applications.**

Keywords; Gallium Nitride (GaN), Silicon Carbide (SiC), Current collapse, Gate Injection Transistor (GIT), Diode-integrated MOS (DioMOS)

I. INTRODUCTION

Gallium Nitride (GaN) and Silicon Carbide (SiC) are very promising wide bandgap semiconductors suitable for power switching applications. The superior properties of the materials would make the switching systems highly efficient and very compact. So far, working transistors with low on-state resistances and high breakdown voltages by these materials have been demonstrated together with highly efficient switching systems with them. This implies that maturity of the device technologies are reaching to the level of their commercialization and the remaining tasks should be finding niche applications as the entry ones accepting the inherent uncertainties and high costs of the new devices. Figure 1 shows how the future markets of the wide bandgap semiconductors are shared by GaN and SiC. Since the increase of the breakdown voltage of GaN transistors is limited up to 1000V by the existing epitaxial growth technology of GaN on Si substrates, medium range of the output power with relatively high operating frequencies is the target for GaN. SiC should cover rather higher output power taking advantages of the SiC's high breakdown voltages and better thermal conductivity. Challenges to persuade the system designers include better understanding of the switching behavior, the thermal management to overcome high power density, and the reliability. In particular, the reliability needs to be well understood and established to extend the market of the promising wide bandgap semiconductors.

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In this paper, the basic structures and the reliability issues of GaN and SiC transistors are discussed. GaN Gate Injection Transistor (GIT) and SiC DioMOS (Diode integrated MOSFET) developed at Panasonic are shown as unique examples of the structures. Current collapse in GaN and degradation of SiC MOSFET are explained as the issues followed by results of the reliability study for the above GaN GITs and SiC DioMOS free from the above degradations.

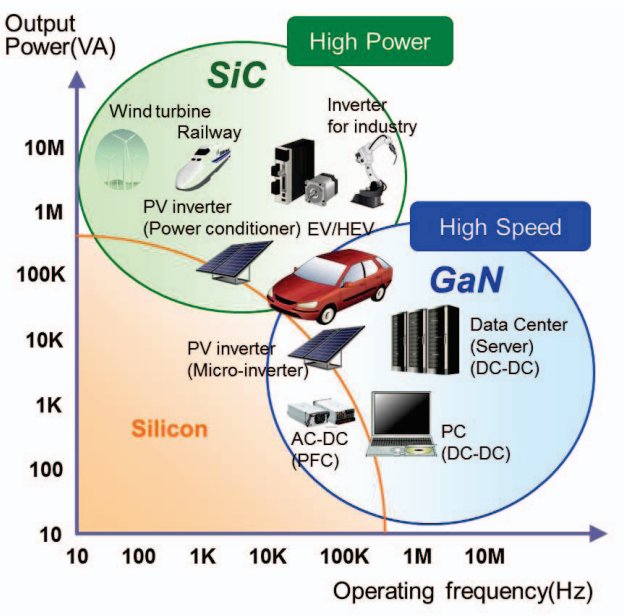

Fig.1 Potential applications of GaN and SiC power switching transistors.

II. GAN POWER DEVICES AND RELIABILITY

A. Structures and Issues of GaN Transistors

GaN transistors, in general, utilize the AlGaN/GaN hetero structures where two dimensional electron gas (2DEG) with high carrier density and high electron mobility is formed [1,2]. The devices have lateral configurations on the insulating buffer enabling high speed switching taking advantages of the low parasitic capacitances. Recently, most of the reported GaN powers switching transistors are formed on Si substrates since the fabrication cost can be dramatically reduced [3-6]. A schematic cross section of the epitaxial structure shown in Fig.2 is an example to relax the strain in the film caused by the lattice and the thermal mismatches. The wafer diameter has been extended up to 8 inch at largest, so far [6]. The structure of a conventional AlGaN/GaN heterojunction field effect transistor (HFET) with a Schottky-metal gate is shown in Fig.3.

The figure also shows a possible origin of the degradations. The degradation appears as the change of the current and resistances occasionally with the failure of the passivation films and/or electrodes. The dominant origins of the degradation have been damaging at the gate edge, leading gate leakage increase, electron trapping in the GaN/AlGaN layers and/or in the passivation films and hot electrons related trap generation [7,8]. The most serious technical issue especially at high drain voltages has been "current collapse" in which the drain current is decreased after applying high drain voltages [9]. The phenomenon is described in Fig.4. The elimination of the above-mentioned trapping with the relief of the electric fields has been solving the collapse resulting in available GaN samples for the examination of the switching systems. In addition, a notable achievement for the GaN transistors is the commercialization of high frequency power transistors to be used for cellular base stations. Although the applied drain voltage has been up to 50V, the devices are free from the above degradations demonstrating the possibility for the failure-free GaN transistors at further high voltages.

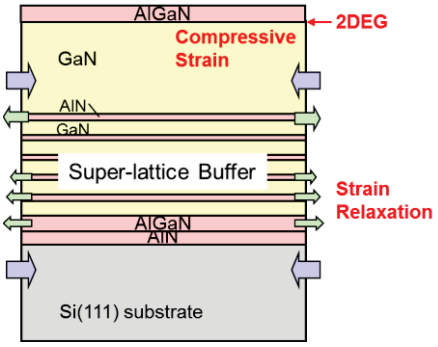

Fig.2 A schematic cross section of AlGaN/GaN hetero-structure grown on a Si substrates.

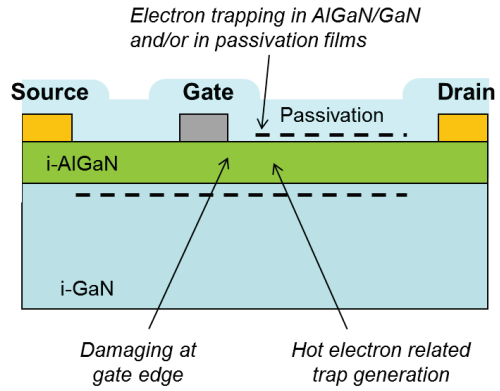

Fig.3 Structure of a conventional AlGaN/GaN HFET in which possible origins of the degradations are also shown.

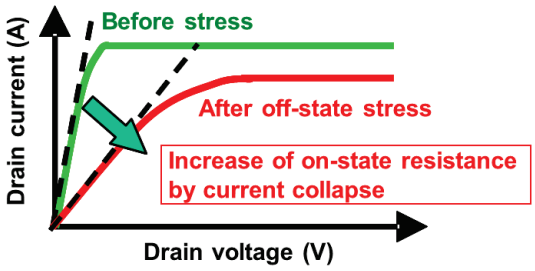

Fig.4 Current collapse observed in GaN transistors.

B. *Gate Injection Transistors (GITs) and Reliability*

Inherent high carrier concentration in the AlGaN/GaN has been making the normally-off operation of the GaN transistor very difficult. The normally-off operation is a mandatory requisite for power switching transistors to ensure the safe operation of the switching systems. Gate Injection Transistors (GITs) solve the issue by placing a p-type AlGaN gate over the heterojunction, which fully depletes the channel under the gate [4]. Injection of holes from the p-gate enhances the formation of the electrons at the channel, which can be called as conductivity modulation, resulting in low on-state resistance and high drain current even in the normally-off transistors. A schematic cross section of the GIT with the operating principle is shown in Fig.5. The DC characteristics of the GIT working samples are summarized in Table 1. The notable characteristics are the low $R_{on}Q_g$ (R_{on}: on-state resistance, Q_g: gate charge) of 700mΩnC which is one thirteenth smaller than that of state-of-the-art superjunction Si MOS indicating far better potential for the high speed switching. The current collapse of the GIT on a Si substrate is characterized by so-called pulsed current-voltage (I-V) measurements. Very short pulses of the drain and the gate voltages from both the zero-bias state and the off-state are applied. Identical I-V characteristics for both with and without bias stress as shown in Fig.6 imply that the GITs are free from the current collapse. The on-state resistances after the off-state stress are measured for various drain voltages up to 600V as

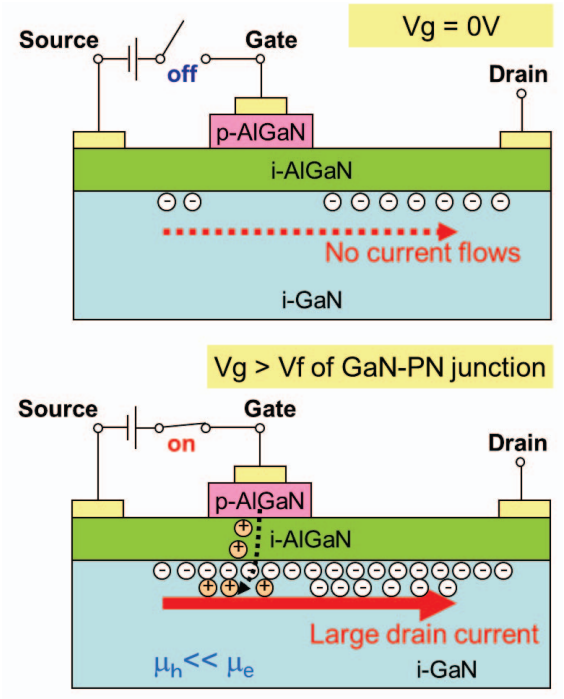

Fig.5 A schematic cross section of a GIT with the operating principle.

summarized in Fig.7. No apparent change of the on-state resistances in the figure implies that the fabricated GITs are free from the current collapse owing to the improved device structure and the processing to eliminate the trapping effects. Note that the slight increase of the dynamic on-state resistances is presumably due to the increase of the temperature by the given multi-pulses. Among the various test of the reliability, the results of high temperature reverse bias tests are summarized in Fig.8. The leakage current and the threshold voltage are stable over 1000 hours which is a good indication of the maturity of the device technologies. So far, standard reliability tests based on the JEDEC standards are qualified for the GITs. Progress of the GIT devices with the improved reliability would be able to find a niche application as an entry one, which would be followed by the wide-spread use of GaN transistors in the near future.

Table 1 Summary of DC characteristics of GaN GITs on Si substrates.

Threshold voltage V_{th}	1.2V (Normally-off)
Blocking voltage BV_{ds}	600V
Raiting current (continuous) I_d	15A
On-state resistance R_{on}	65mΩ
Gate charge Q_g	11nC

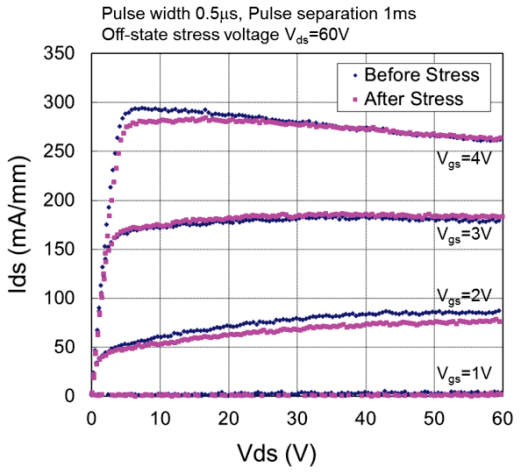

Fig.6 Pulsed I-V characteristics for the fabricated GITs on Si.

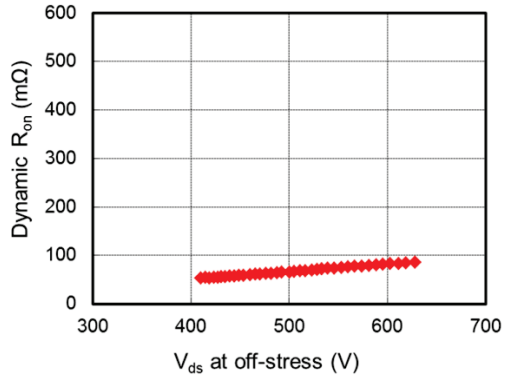

Fig.7 On-state resistances of GITs on Si after pulsed off-state stress by various drain voltages.

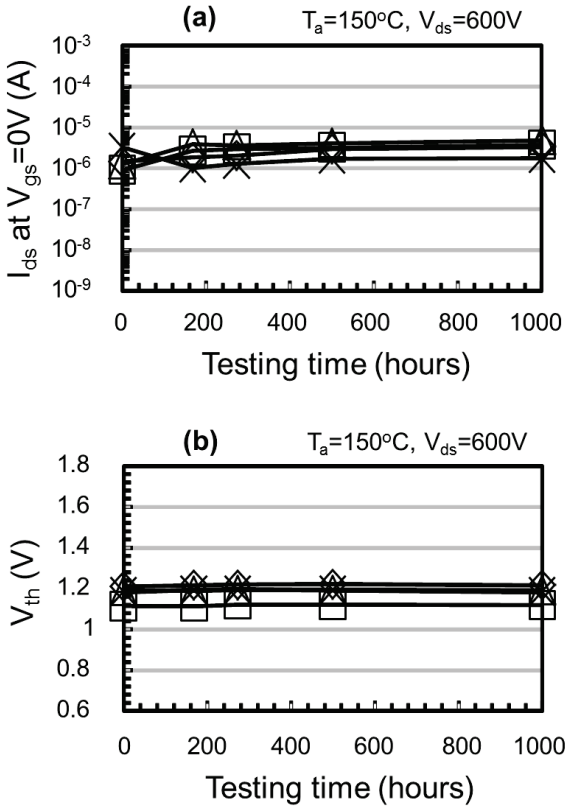

Fig.8 Results of high temperature reverse bias tests for (a) off-state leakage current, (b) threshold voltage of GIT on Si.

III. SiC Power Devices and Reliability

A. Structures and Issues of SiC Transistors

SiC devices are formed on SiC substrate taking advantages of the improved quality of the bulk crystal and the epitaxially grown SiC film on the off-axis substrates [10-12]. The material properties of SiC depend on the poly-type and the choice for the power transistors has been 4H-SiC since it serves higher electron mobility with good bulk quality. The device configuration developed for the mass production so far has been double-diffused MOSFET (DMOS) which has been commonly employed for existing Si power MOSFET. MOS-gate structures and their processing have been investigated for working SiC transistors together with the ion implantation techniques to enable the planar structure. A typical structure of the SiC DMOS and the reliability issues studied so far are summarized in Fig.10. In addition to the improvement of the interfacial properties at the thermal oxide over SiC, suppression of the shift of the threshold gate voltages after applying high positive or negative voltages has been a critical issue for the reliability [13,14]. Typical data of the shifts are shown in Fig.11. High gate voltage presumably causes the trapped electrons or holes dependent on the polarity of the gate voltages resulting in the shift of the threshold voltages. Additional issue for the reliability is the degradation of body diode based on pn junction as shown in Fig.12. The origin is believed to be a formation of the basal-plane dislocations and the improvement of the epitaxial quality would be necessary to solve it [15,16]. So far, in order to avoid the degradation of the body diode and

to flow fly-wheel current with smaller reverse conduction loss and fast recovery, SiC Schottky barrier diodes (SBDs) are connect in parallel with the MOSFET. The introduction of the SBDs has doubled the total chip cost in the SiC-based power circuits, although it enables the operation free from the degradation of the body diodes.

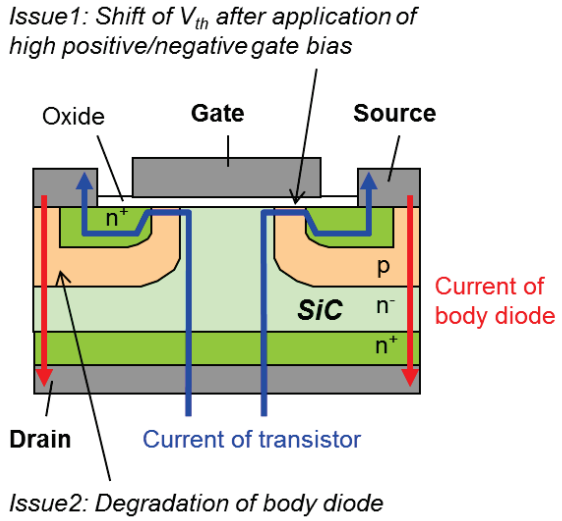

Fig.10 A schematic cross section of the conventional SiC DMOS with the reliability issues.

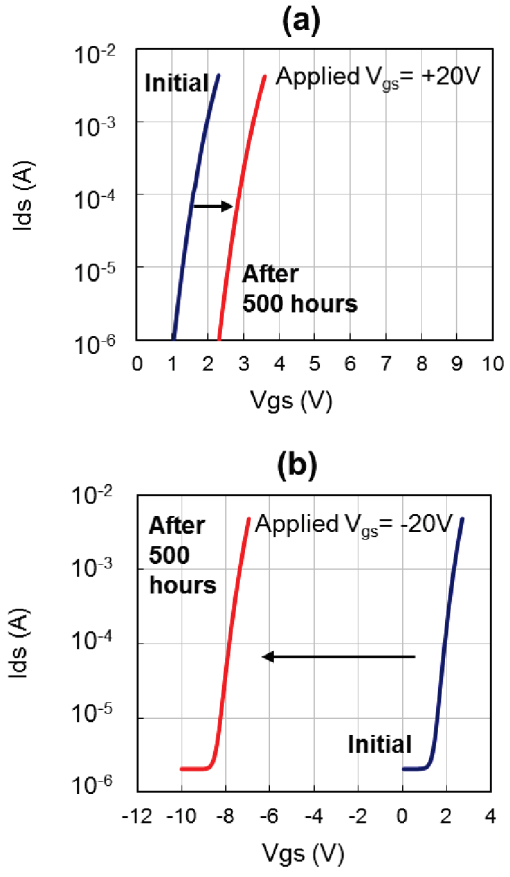

Fig.11 Shift of the threshold voltages of conventional SiC MOSFETs after applying high (a) positive and (b) negative gate voltages.

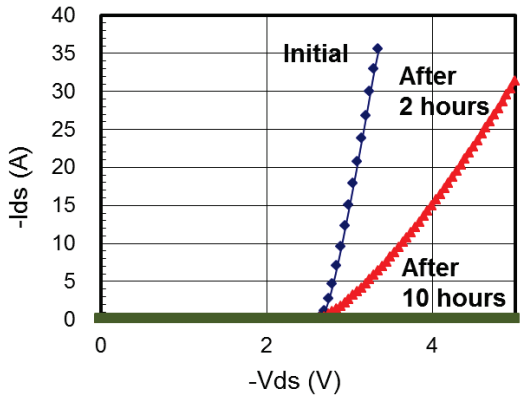

Fig.12 Degradation of the body diode in a conventional SiC DMOS

B. Diode-integrated MOSFET (DioMOS) and Reliability

A Diode-integrated MOS (DioMOS) structure has been proposed to reduce the total chip cost in the SiC-based switching system [17,18]. Figure 13 shows the schematic cross section in which additional channel epitaxial layer is formed under the gate insulator. This channel layer serves the path for the reverse diode current so that the reverse current does not flow at the integrated body diode. The basic operation of the DioMOS is that the potential barrier for the electrons at the reverse conduction is lowered down to 0.8eV underneath the gate by the thin channel epitaxial layer with heavy n-type doping. The change of the potential diagram at the MOS gate depending on the doping profile of the channel is shown in Fig.14. The lowered barrier height corresponds to the build-in voltage of the reverse diode in the DioMOS. Typical I-V characteristics of the SiC DioMOS are shown in Fig.15, where low built-in voltage of the reverse diode is confirmed. Table 2 summarizes the DC characteristics of the fabricated DioMOS with the breakdown voltages are over 1200V and the high drain current over 25A by a single chip. No shift of the threshold voltages is confirmed for both positive gate bias up to 15V and negative value to -15V. The DioMOS is inherently free from the degradation of the body diode since the forward current

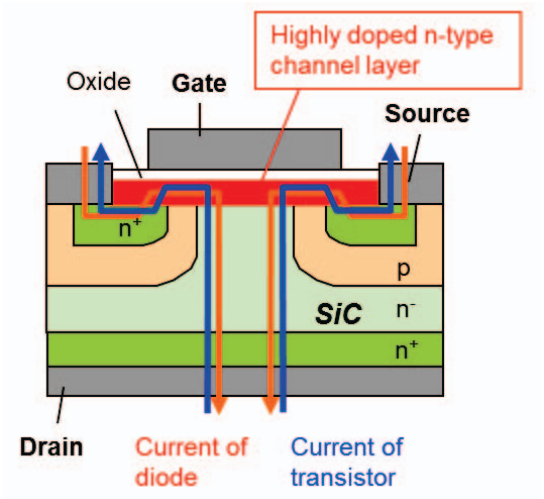

Fig.13 A schematic cross section of SiC DioMOS.

does not flow at the pn junction. High temperature reverse bias tests for the SiC DioMOS are conducted, of which the typical results are shown in Fig.16. The stable characteristics up to 1000 hours indicate that the demonstrated DioMOS with sufficient reliability is applicable to practical switching applications.

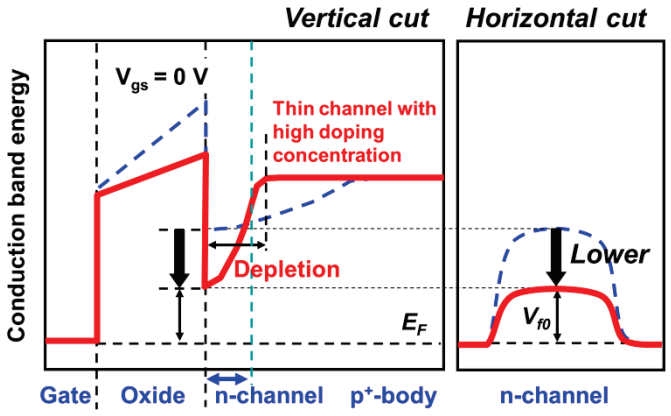

Fig.14 Potential diagrams of SiC DioMOS at the gate, in which thinner channel with higher doping concentration lowers the potential barrier along to the channel.

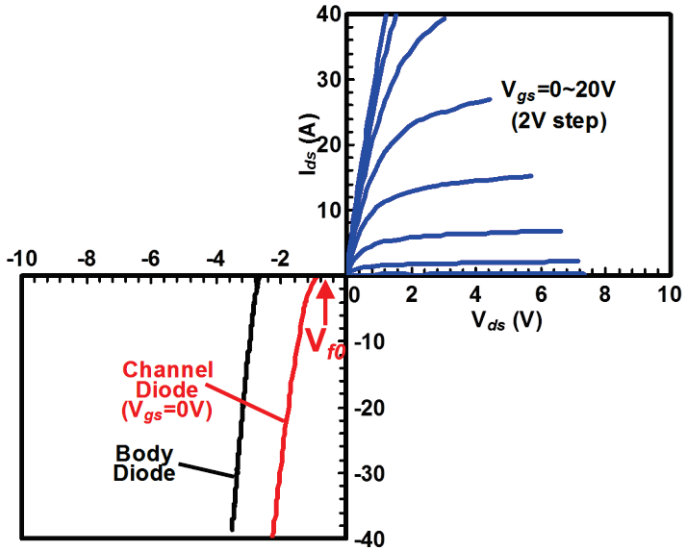

Fig.15 Forward and reverse I-V characteristics of the fabricated SiC DioMOS.

Table 2 Summary of DC characteristics of SiC DioMOS.

Threshold voltage V_{th}	4.5V (Normally-off)
Blocking voltage BV_{ds}	1700V
Raiting current (continuous) I_d	25A
On-state resistance R_{on}	40mΩ
Built-in voltage of diode V_{f0}	0.8V

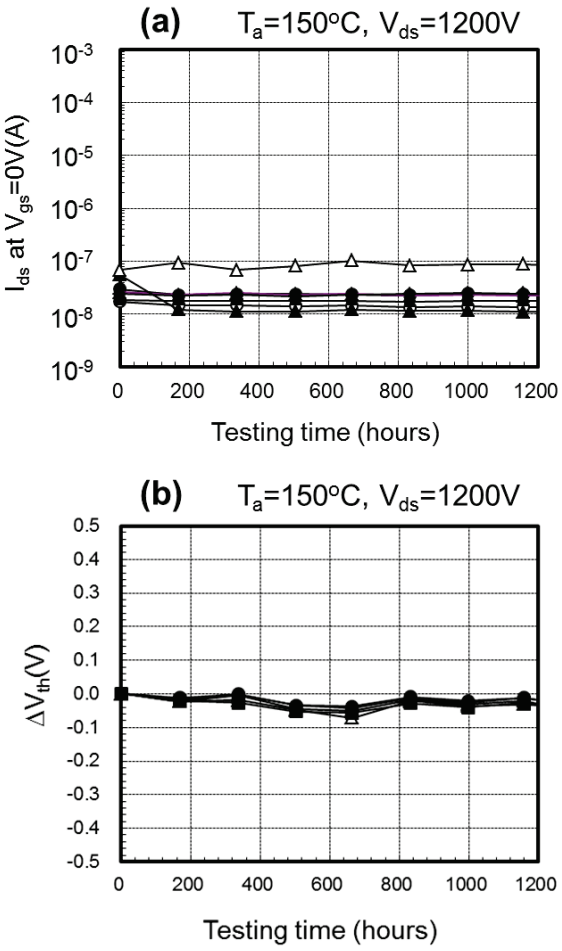

Fig.16 Results of high temperature reverse bias tests for (a) off-state leakagae current and (b) variation of threshold voltages of SiC DioMOS.

IV. Conclusions

State-of-the-art GaN and SiC power switching devices developed at Panasonic are reviewed after summarizing the conventional devices and the reliability issues for them. Normally-off GaN GITs on Si substrates are free from current collapse up to 600V which is sufficiently good for the practical switching applications. SiC DioMOS, which integrates the reverse diode, can reduce the total chip cost in the system. It shows stable operation free from the shift of the threshold voltages after the application of high gate bias and the degradation of the body diodes. The presented GaN and SiC power devices have passed the high temperature reverse bias tests over 1000 hours and thus very promising for highly efficient power switching systems in the future.

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