Gate Oxide Degradation of SiC MOSFET in Switching Conditions

Rémy Ouaida, Maxime Berthou, Javier León, Xavier Perpiñà, Sebastien Oge, Pierre Brosselard, and Charles Joubert

***Abstract*— Under realistic switching conditions, SiC MOSFETs reliability issues remain as a challenge that requires further investigation. In this letter, a specific aging test has been developed to monitor and characterize the electrical parameters of the SiC MOSFET. This allows estimations of the health state and predictions of the remaining lifetime prior to its failure. The gate leakage current seems to be a relevant runaway parameter just before failure. This leakage indicates deterioration of the gate structure. This hypothesis has been validated through analysis of scanning electron microscopy pictures, with a focused ion beam cut showing cracks within the polysilicon.**

***Index Terms*— Silicon carbide, power MOSFET, aging test, reliability, failure mechanism, switching, oxide degradation.**

I. Introduction

SILICON Carbide (SiC) power semiconductors are believed to be one ideal choice for future power electronic converters. This is thanks to their performances, which cannot be reached by conventional silicon (Si) semiconductors, especially at high temperatures.

Due to its simple drive requirement and the advantage of safe, normally-off operations, SiC MOSFET is becoming a promising device that could replace conventional Si MOSFETs and Si IGBTs. Previous works have revealed the achievable electrical performances of high temperature inverters using SiC MOSFETs [1]. However, studies presented in [2] and [3] have demonstrated that the threshold voltage is not stable due to electron injection into gate oxide traps. More recent works ([4] and [5]) demonstrate a satisfying lifetime and improved reliability. Reliability issues are not yet well understood, and in contrast to DC testing ([6] and [7]), understanding SiC MOSFET reliability under realistic switching conditions remains a challenge that requires further investigation.

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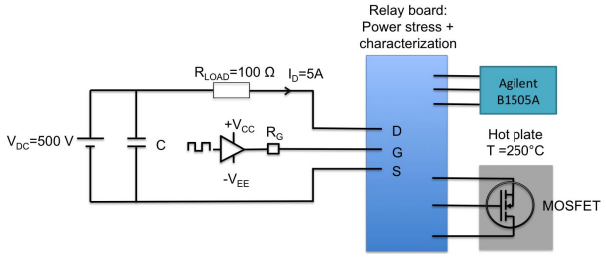


Fig. 1. Schematic of one section of the aging test setup.

A specific aging test has been developed in order to monitor and characterize the electrical parameters of the SiC MOSFET's switching conditions. This allows for estimations of the health state and predictions of the remaining lifetime before failure. Moreover, the defects have been localized in the device using an infrared lock-in thermography. Cracks in the Poly-Silicon (Poly-Si) gate, causing the failure of the MOSFET, have been observed using FIB and SEM imagery.

II. Aging Setup

Figure 1 presents the aging setup. The SiC MOSFETs used include $1200\,V/80\,m\Omega/16\,mm^2$ dice. To use them at 250 °C, the dice were packaged using the following materials: Active Metal Brazed Si_3N_4 substrate with silver sintering die attachments/TO-254 metallic packaging/hermetical seals in N_2 atmosphere. Three test vehicles were fixed on a heating baseplate to maintain their case temperature at 250 °C. The fixed temperature avoids thermal cycles that generate package related failures. To insure a constant thermal stress setup, a relay card was used to stop the switching test and proceed to static characterization. Upon setup, this characterization was performed using an Agilent B1505A. Each MOSFET switched a 5 A drain current at 10 kHz under 500 V bus with $V_{GS} = -5\,V/+20\,V$. During the test, the aging indicators of the MOSFETs were monitored at regular intervals of time. Due to the sensitive nature of the gate oxide interface, the first indicator's threshold voltage was defined as the value of the gate voltage corresponding to a DC drain current (I_D) of $100\,\mu A$. The degradation of the oxide could initiate leakage in the gate, so the leakage current was measured for $V_{GS} = 5\,V$. Degradations, such as channel drift mobility or ohmic contacts, could change the on-resistance of the device. $R_{DS,ON}$ was monitored using $V_{GS} = 20$ V and $I_D = 5$ A. Other mechanisms, such as the gate-induced drain leakage

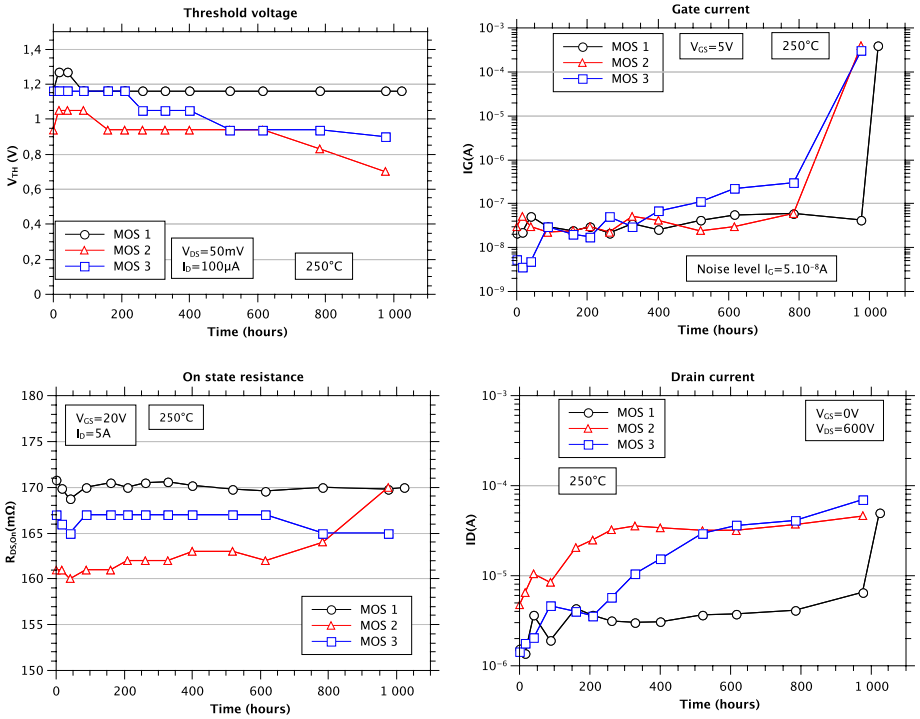


Fig. 2. Evolution of threshold voltage, gate current, on state resistance and drain current versus time for aging test with T_{case} of 250 °C

current [8], defect evolution, or thermal runaway, can weaken the structure of the device and create leakage paths between the drain and the source. Therefore, the drain leakage current was monitored with $V_{GS} = 0\,\text{V}$ and $V_{DS} = 600\,\text{V}$.

III. Experimental Results

A. Evolution of Electrical Parameters During Aging Test

The stress, with a case temperature of 250 °C, was performed on three devices, all of which failed after approximately 1000 hours of stress. The monitored parameters were sampled 13 times. Figure 2 depicts the evolution of these parameters along the stress. The three devices show inconclusive aging behaviors for all parameters except for the gate leakage current. The gate threshold voltage decreased slightly in 2 of the 3 devices. However, V_{TH} does not shift significantly as the gate is switching between a positive and negative voltage. This is in contrast to the DC gate stress tests [3]. Concerning $R_{DS,ON}$, only one device shows notable degradation. We can therefore determine a correlation between the rate of gate threshold voltage degradation and $R_{DS,ON}$. Taking MOSFET operation into account, the on-resistance should decrease when V_{TH} decreases, as well. This means that the measured evolution must come from a degradation that results from an increased instability of the gate threshold voltage. Upon observing the drain leakage current, it can be discerned that the devices evolve differently. For SiC MOFSET, there is generally a correlation between threshold voltage and drain leakage. A comparison of the evolution of V_{TH} and I_D on figure 2 reveals that the increase in drain leakage current with time is likely due to a local threshold decrease with time. Finally, the gate leakage current is the only indicator that informs failure; indeed, I_G increases just before failure. The relay card was used to characterize the MOSFET. Unfortunately, this also introduced parasitic leakage. The first values of I_G are abnormally high. However, the large shift noted at close to 1000 hours of operation is real, and so the lifetime estimation based on this particular failure is valid.

B. Temperature Dependence of the Lifetime at a High Temperature

To study the temperature dependence of the lifetime, the aging test has been performed for two other temperatures: $T_C = 260$ °C and $T_C = 300$ °C. The TTF (Time to Failure, defined as the +100% upper specification limit of gate leakage current: $I_{Glimit} = 5{\cdot}10^{-7}$A) was measured for three MOSFETs at each temperature. The aging indicators have been monitored for each temperature, with the gate leakage current behaving as depicted previously. This validates that the parameters for failure do not change. The gate leakage is the most relevant health state indicator. For each temperature, evolution of the threshold voltage decreases with the increase of temperature. However, MOSFET are still normally-off devices, with $V_{TH} = 0.2\,V; 0.5\,V; 0.7\,V$ at 300 °C. Figure 3 shows each component placed in terms of time to failure, in function of 1000/T (temperature of stress in Kelvin). At $T_C =$ 250 °C (523K), the device's lifetime is grouped around 900 hours, 700 hours for $T_C = 260$ °C (533K), and 250 hours, with $T_C = 300$ °C (573K). The lifetime estimation at 200 °C (473K and 1000/T = 2,114) is evaluated at 5000 hours. The TTF globally decreases with the temperature, which identifies the temperature as an accelerating factor. The applied electric field is calculated with an oxide thickness of 50 nm

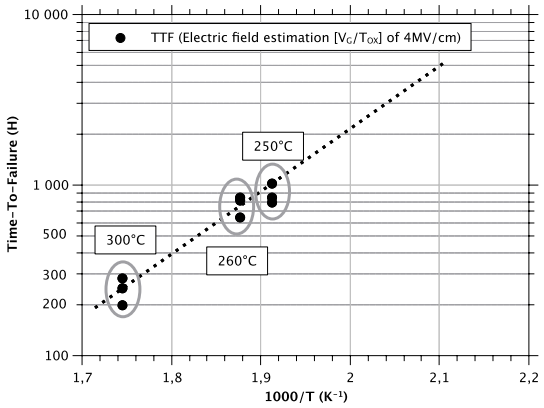
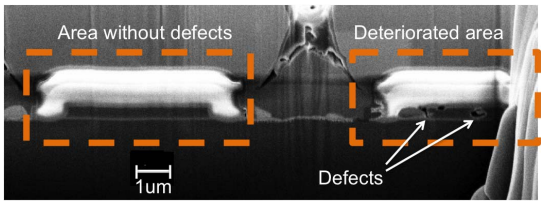
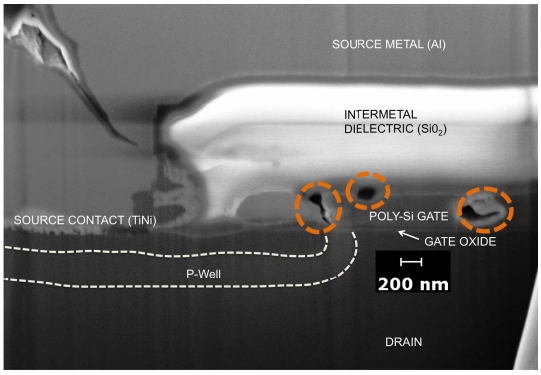


Fig. 3. Temperature dependance of the lifetime for three case temperature.



(a)



(b)

Fig. 4. SEM micrograph of the FIB cut of (a) the defect localized by infrared lock-in thermography. (b) Zoom of the deteriorated area.

and it is estimated to 4 MV/cm. In [7], Figure 6 describes the temperature acceleration with an Arrhenius dependence. It seems that the MOSFETs present the same dependence, and this validates our results.

C. Microscopic Analysis of the Gate Oxide's Degradation

Presented results show a runaway of the gate leakage current just before failure. This evolution could be linked to the gate's degradation. To validate this hypothesis, the physical defect has been localized using an infrared lock-in thermography technic [9]. Once the failure was localized, it was imaged using Scanning Electron Microscopy (SEM) with a Focused Ion Beam (FIB) cut. Figure 4a shows the picture of the FIB cut with elementary structures of MOSFET. The structure on the left does not present defects. However, cracks do show around the gate area on the right. Figure 4b is a magnified shot of the physical defect on the right cell where the gate was destroyed. The intermetal dielectric appears in bright contrast and the Poly-Silicon gate metal appears in darker gray. The gate oxide is approximately 50 nm thick, which is very difficult to see on the image. Defects appear as cracks in the Poly-Silicon gate metal. The increase of the gate leakage current could be explained by the following assumption: the Poly-Silicon voids were formed from localized heat (high electric field and high temperature), leading to the gate oxide breakdown. Thus, the gate oxide can no longer be considered an insulator in this region. Additionally, a current flows through this crack between the source and the gate. The cracks within the Poly-Silicon might be a valuable indicator that the gate oxide failed.

IV. Discussion and Conclusion

Our work proposes an accelerated aging test system that allows for an analysis of the gate oxide degradation mechanism in SiC MOSFET. Based on the evolution of electrical parameters during aging tests, gate current leakage has been identified as a valuable health indicator. The SEM micrographs of FIB cut might validate this hypothesis with the presence of cracks in the Poly-Silicon gate, which would indicate that the gate oxide failed. A higher magnification image showing cracks within the gate oxide could be physical proof of this failure. Such a measure is not straight forward. Therefore, further investigations are required. Nevertheless, the failure signature has been identified through the gate leakage current.

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