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Advanced power cycler with intelligent monitoring strategy of IGBT module under test

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ABSTRACT

Power cycling (PC) test is one of the important test methods to assess the reliability performance of power device modules related to packaging technology, in respect to temperature stress. In this paper, an advanced power cycler with a real-time V_{CE_ON} and V_F measurement circuit for the IGBT and diode, which for the wear-out condition monitoring are presented. This advanced power cycler allows to perform power cycling test cost-effectively under conditions close to real power converter applications. In addition, an intelligent monitoring strategy for the separation of package-related wear-out failure mechanisms has been proposed. By means of the proposed method, the wear-out failure mechanisms of an IGBT module can be separated without any additional efforts during the power cycling tests. The validity and effectiveness of the proposed monitoring strategy are also verified by experiments.

1. Introduction

Power device modules are one of the reliability critical components in power electronic systems and thus, its reliability assessment, prediction and improvement are becoming important issues in power electronics field [1].

There are many test methods for reliability assessment of power device modules [2]. Among them, the power cycling (PC) test is one of the major test methods to assess the reliability performance related to packaging technology, in respect to temperature stress [3]. Furthermore, a lifetime model can be developed based on the PC test results [4,5] and it can be used for Design For Reliability by estimating the lifetime of power device modules under given mission profiles of real converter applications [6].

Increasing efforts are being done to perform the reliability assessment of power electronic products under more realistic conditions of real applications as close as possible in order to obtain better results. As a part of that, in recent PC test, some advanced features are demanded such as realistic operation of the Device Under Test (DUT) and online monitoring of wear-out status of the DUT in order to avoid catastrophic failure [7,8].

In this paper, an advanced power cycler with intelligent monitoring strategy is presented to further improve the existing methods. In the first section of this paper, the configuration and control methods of advanced power cycler are presented, which allow cost-effectively to perform the PC test under more realistic electrical condition compared with PC test under real loads. Then, an on-state collector-emitter voltage (V_{CE_ON}) and forward voltage (V_F) measurement circuit for real-time condition monitoring of the IGBT modules is proposed. In addition, an intelligent monitoring strategy is proposed, which can separate package-related wear-out failure modes without any efforts during PC test. The validity and effectiveness of the proposed strategies are verified by experiments.

2. Advanced power cycler

2.1. The number of power cycling test bench

In the reliability studies, the statistical data analysis is an essential part in order to deal with uncertainties because the reliability is influenced by variability such as in manufacturing process, environment and other factors. However, there is a limitation in sample size due to the cost and time for reliability tests. In such a situation, the data ranking is a useful method for the compensation of small sample sizes. Median Ranking is one of the most used methods for probability plotting in reliability engineering such as Weibull analysis. It is defined as the cumulative percentage of the population represented by a particular sample with 50% confidence level and can be calculated simply by the Benard's approximation [9] as

$$\text{Median Rank}(\%) = \left(\frac{j-0.3}{N+0.4}\right) \times 100 \quad (1)$$

where j = failure order number and N = sample size. For example, Median Rank (MR) of 3*rd* order sample out of six samples represents 41.28% of the total population with 50% confidence.

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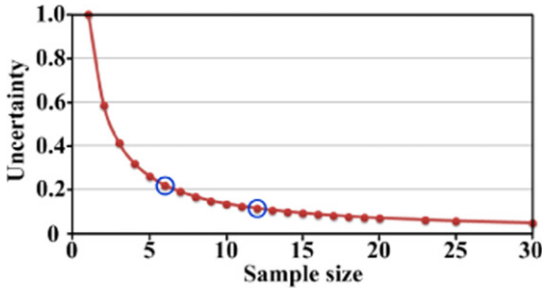

Fig. 1. Uncertainty vs. sample size.

From the *MR*, the uncertainty in the probability plot can be calculated as

$$\text{Uncertainty} = 1-(MR_{\_higest}-MR_{\_lowest}) \quad (2)$$

where $MR_{\_highest}$ and $MR_{\_lowest}$ are the highest and lowest median ranks for a given sample size.

Fig. 1 shows the uncertainty depending on the sample size. A sample size of six is down in the knee of the curve and the sample size of twelve is beyond the knee of the curve. It can be seen that six to twelve samples would be appropriate for the test and thus at least six samples are required per test.

2.2. Configuration of advanced power cycler

Fig. 2 shows the configuration of advanced power cycler. According to the discussion in the previous section, it has been designed with six identical test benches so that the test results of six samples can be obtained at the same time for the reduction of test time. They are mounted on heat exchangers with water cooling systems where the temperature of the heat exchanger for the IGBT module under test can be varied depending on desired test conditions. The temperature of the heat exchanger for the load IGBT module is kept low about 20 °C and individual test bench is protected by each electric fuse.

Each test bench is mainly composed of three boards, test converter board, load converter board and control board. The outputs of IGBT module under test of the test converter are connected with the outputs of the IGBT module of the load converter through small load inductors and they are sharing a common DC source. In the load converter, an IGBT module which has a higher rated power than an IGBT module under test is used so that the load IGBT module has a smaller temperature stress during power cycling tests. Thus, the load converter can run for a long time even though several IGBT modules under test are replaced after power cycling tests. The on-state collector-emitter voltages (V_{CE_ON}) of the IGBTs and forward voltages (V_F) of the diodes are measured in real time in order to determine the wear-out condition of the IGBT module under test. Both converters are controlled by the control board using a Digital Signal Processor (DSP) and a Labview interface communicates with the DSP in order to manage the overall system and also to save the monitoring parameters.

2.3. Control of advanced power cycler

In this system, both converters are controlled as a single-phase half-bridge converter as shown in Fig. 3. The output voltage of the test converter ($V_{A\_ref\_test}$) is controlled by an open loop voltage controller under a defined switching frequency (f_{sw}), output frequency (f_{out}) and modulation index. The output phase current of the converter (I_A) is considered as the current in the d-axis in the stationary frame when it is controlled. The q-axis current in the stationary frame is obtained by shifting the d-axis current in the stationary frame by 90° using an all-pass filter as shown in Fig. 3. The d- and q-axis currents in the stationary frame are converted to the currents in the synchronous frame with a phase angle. The real power is aligned to the d-axis and the imaginary power is aligned to the q-axis in the synchronous frame. Then, they become the input to Proportional-Integral (PI) current controllers, separately. The output of each current controller becomes the reference output voltages (V_{de_ref} and V_{qe_ref}) in the synchronous frame. By inverse transformation, V_{de_ref} and V_{qe_ref} are converted to voltages in the stationary frame (V_{ds_ref} and V_{qs_ref}), where the V_{ds_ref} becomes the reference voltage of the load converter ($V_{A\_ref\_load}$). The controls for the other phases are the same. There are only phase shift by 120 and 240°, respectively in order to emulate a 3-phase converter system. In this system, there is only small power consumption by two IGBT modules and small inductors because the power is circulated between two converters. Therefore, the power cycling test can be performed under realistic operating conditions of DUT cost-effectively compared with power cycling test under real loads such as in [10].

Typically, in power cycling tests, high junction temperature swing ΔT_j (40 °C–100 °C) and mean junction temperature T_{jm} (60 °C–120 °C) are applied to the DUT in order to obtain test results in a reasonable test time [3]. There are two ways to apply the temperature stress to DUT in the advanced power cycler. AC current leads to ΔT_j in DUT but it is

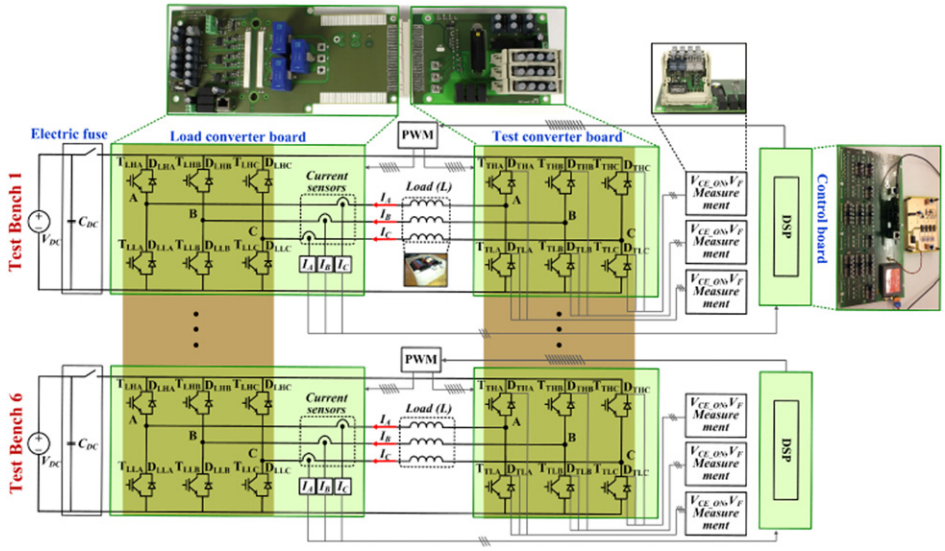

Fig. 2. Configuration of proposed advanced power cycler.

difficult to get a high ΔT_j with high f_{out}. Therefore, AC current with low f_{out}, less than ten hertz is applied to DUT as shown in Fig. 4 (a). In this way, high ΔT_j can be obtained in a relatively short cycle period. The other way is that the regulated AC current with high f_{out} such as 100 Hz is applied to DUT. If the junction temperature is reached to the maximum temperature for desired ΔT_j, the injection of output current is stopped as the conventional DC power cycling test. Then, the junction temperature is decreased by the external cooling system as shown in Fig. 4 (b). In this way, high ΔT_j can be obtained in a relatively long cycle period. Between them, a proper method can be chosen depending on the desired test conditions and target applications.

2.4. Real time V_{CE_ON} and V_F measurement circuit

Fig. 5 shows the real-time V_{CE_ON} and V_F measurement circuit based on a depletion mode MOSFET (M_{D1}) where the magnitude of clamping voltage (V_{CC}) should be larger than that of V_{CE_ON} and V_F and the input impedance (Z_{in}) of the next stage should be high enough. Considering the T_{HA} as an example, when T_{HA} is tuned-on, the current I_D does not flow through the M_{D1} because the collector voltage $V_C = V_{CE\_ON} < V_{CC}$ and Z_{in} is high. Thus $V_{GS} = 0$. Consequently, the M_{D1} is turned on because it has a negative threshold voltage ($V_T < V_{GS} = 0$) and $V_{out\_HA} = V_{CE\_ON}$. When V_C increases above the V_{CC} as T_{HA} is turned off, I_D starts to flow and makes a voltage drop in R. As I_D increases, V_{GS} becomes a negative value and then M_{D1} is turned off when $V_{GS} < V_T$. Therefore, the V_{CC} is measured at the output during this period [11].

3. Intelligent monitoring strategy for power cycling test

3.1. Monitoring parameter for both bond-wire and solder joint fatigues

There are mainly two dominant package-related failure mechanisms in standard IGBT modules, bond-wire fatigue and solder joint [12]. Bond-wire fatigue leads to the increase of electrical resistance and thus results in the increase of V_{CE_ON}. Solder joint fatigue leads to the increase of thermal impedance, which causes the increase of junction temperature and thus it bring about the changes in V_{CE_ON} because it is Temperature Sensitive Electrical Parameter (TSEP). Therefore, both failure modes can be detected by monitoring the variation of V_{CE_ON}.

3.2. Conventional real-time monitoring strategy for failure mechanism distinction

The V_{CE_ON} can be used for the monitoring of the bond-wire fatigue and the junction temperature (T_j) estimation for the monitoring of the solder joint fatigue. However, in order to use V_{CE_ON} for monitoring of both failure modes, it is needed to eliminate the influence from one failure mode on the monitoring of the other failure mode. For example, if the bond-wire fatigue occurs, the V_{CE_ON} increases and it results in a wrong estimation value of T_j, which is estimated by using V_{CE_ON} based on initial I-V characterization curves [13]. Therefore, an I-V re-characterization is required in order to eliminate the effect of electrical degradation on the T_j estimation and to determine the V_{CE_ON} increase due to either bond-wire fatigue or solder joint fatigue.

Fig. 6 shows the V_{CE_ON} during power cycling test and estimated T_j using V_{CE_ON} and load current with I-V characterization curves. It can be seen that the estimated T_j increases as V_{CE_ON} increases. The estimated T_j decreases to initial value after the I-V re-characterizations and thus it can be determined that the increase of V_{CE_ON} is not due to the solder joint fatigue but due to the bond-wire fatigue. However, multiple I-V re-characterizations during the PC test are very inconvenient and time-consuming.

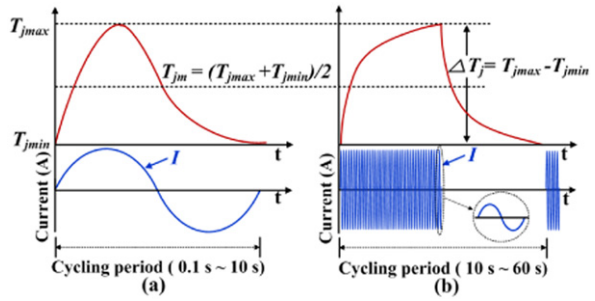

Fig. 4. Strategies to apply temperature stress to DUT (a) low frequency AC current (b) high frequency AC current.

3.3. Intelligent real-time monitoring strategy for failure mechanism distinction

Two preliminary characterizations of the IGBT modules are required in order to separate the failure modes using V_{CE_ON} without additional efforts during the PC test. The first one is a conventional I-V characterization to find an intersection point, which is independent on the temperature variation as shown in Fig. 7 (a). Therefore, the increase of electrical resistance (ΔR_{int}) can be obtained from the variation of $V_{CE\_ON(inter)}$ at an intersection point when the bond-wire fatigue occurs. The second one is the V-T characterization under the power cycling test condition as shown in Fig. 7 (b), where V is the V_{CE_ON} at the peak current ($V_{CE\_ON(peak)}$) and T is the heat-sink temperature (T_H). From this, the dependency of V_{CE_ON} on T_j, the K-factor can be obtained indirectly, which is used to determine the end-of-life in the case of solder joint fatigue. Of course, the increment in T_H does not imply exactly the same

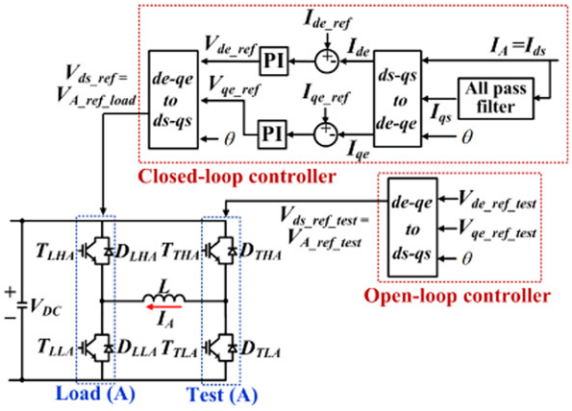

Fig. 3. Control block diagram of advanced power cycler.

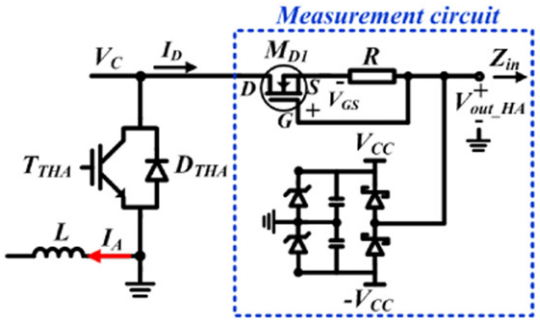

Fig. 5. Real-time V_{CE_ON} and V_F measurement circuit [11].

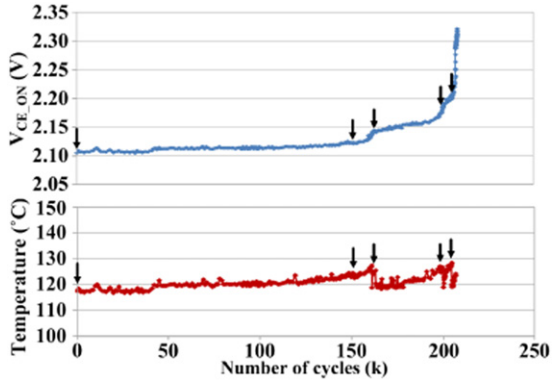

Fig. 6. Variation of V_{CE_ON} due to bond-wire fatigue and estimated T_j using V_{CE_ON}; arrow: re-characterization points.

increment in T_j. However, a few degree differences in T_j are not significant to determine the end-of-life of the IGBT module in the power cycling test.

$$\begin{aligned}
&\text{Case 1}: \text{if } \Delta V_{CE_ON(\ inter)} = 0, \Delta V_{CE_ON(peak)} = 0, && \text{Normal condition}\\
&\text{Case 2}: \text{if } \Delta V_{CE_ON(\ inter)} > 0, \Delta V_{CE_ON(peak)} = \Delta V_{CE_ON(peak_ref)}, && \text{Bond-wire fatigue}\\
&\text{Case 3}: \text{if } \Delta V_{CE_ON(\ inter)} = 0, \Delta V_{CE_ON(peak)} > \Delta V_{CE_ON(peak_ref)}, && \text{Solder joint fatigue}\\
&\text{Case 4}: \text{if } \Delta V_{CE_ON(\ inter)} > 0, \Delta V_{CE_ON(peak)} > \Delta V_{CE_ON(peak_ref)}, && \text{Bond-wire and solder joint fatigues}
\end{aligned} \tag{3}$$

The failure modes during the power cycling test can be determined as Eq. (3) where the reference variation value of $\Delta V_{CE\_ON(peak)}$ ($\Delta V_{CE\_ON(peak\_ref)}$) can be obtained from the ΔR_{int} as

$$\begin{aligned}
\Delta R_{int} &= \Delta V_{CE_ON(inter)} / I_{inter}\\
\Delta V_{CE_ON(peak_ref)} &= \Delta R_{int} \cdot I_{peak}
\end{aligned} \tag{4}$$

where $\Delta V_{CE\_ON(inter)}$ is variation of $V_{CE\_ON(inter)}$, I_{inter} is the current value at intersection point and I_{peak} is the peak current value. Typically, the end-of-life criteria are 5%–20% increase in V_{CE_ON} for the bond-wire fatigue and 20% increase in thermal impedance for the solder joint fatigue [2].

4. Experimental results

Experiments have been performed in order to validate the proposed method. The PC test condition is $V_{DC} = 400$ V, $I = 25$ A_{peak}, $V_{X\_ref\_test(X\ =\ A,B,C)} = 120$ V, $f_{sw} = 10$ kHz, $f_{out} = 1$ Hz, $T_H = 40$ °C, $\Delta T_j = 60$ °C, $T_{jm} = 90$ °C. Furthermore, the $V_{CE\_ON(inter)}$, I_{inter} and K-factor are obtained from the preliminary characterizations (see Fig. 7) as 1.062 V, 5 A and 0.34 (°C/mV), respectively. In the experiments, the bond-wire fatigue is simulated by cutting the bond-wires of an open

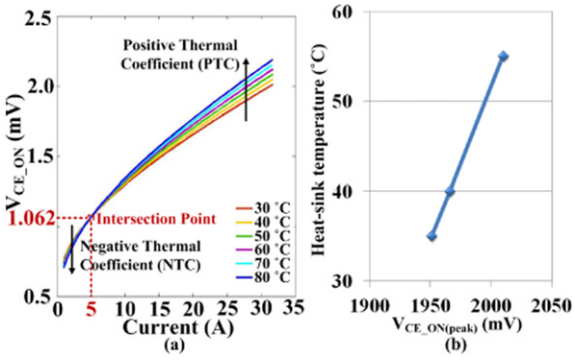

Fig. 7. Preliminary characterizations (a) I-V characterization (b) V-T characterization at peak of load current (25 A).

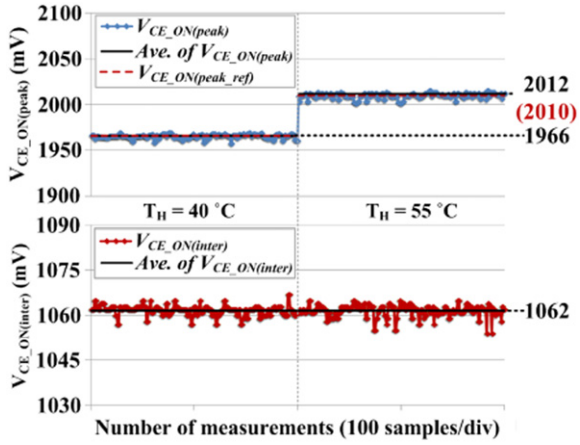

Fig. 8. Experimental result under the virtual solder joint fatigue; Black: measured value, Red: reference value.

IGBT module and the solder joint fatigue is emulated by changing T_H. Furthermore, averages of 100 V_{CE_ON} measurements at both intersection and peak current points are used in order to improve the accuracy of failure monitoring.

Fig. 8 shows the experimental result, which is simulating the solder joint fatigue (Case 3). The measured $V_{CE\_ON(inter)}$ is 1.062 V which is the same as the value of the initial I-V characterization and the initial $V_{CE\_ON(peak)}$ is 1.966 V. Then, T_H increases to 55 °C in order to simulate the virtual solder joint fatigue. It is worth to note that T_H is kept constant during the power cycling test. It can be seen that there is no variation in $V_{CE\_ON(inter)}$ but the $V_{CE\_ON(peak)}$ increases from 1.966 to 2.012. This result satisfies the condition of Case 3 in Eq. (3). $\Delta V_{CE\_ON(peak)}$ is 46 mV and thus the increment of T_j is about 15.6 °C (46 mV ∗ 0.34 (°C/mV)). This result agrees well with the variation of the T_H and thus the T_j increase due to real solder joint fatigue can be determined.

Fig. 9 shows the experimental result where Case 2 and Case 4 are emulated. First, the bond-wire fatigue is simulated by cutting 2 bond-wires out of 5. $V_{CE\_ON(inter)}$ increases by 9 mV and thus ΔR_{int} is 1.8 mΩ. From this, $\Delta V_{CE\_ON(peak\_ref)}$ is obtained as 45 mV form Eq. (4). Due to the bond-wire fatigue, $V_{CE\_ON(peak)}$ rises by 46 mV and it is almost the same with $\Delta V_{CE\_ON(peak\_ref)}$. It can be seen that this result corresponds to Case 2 in Eq. (3). Then, T_H is changed from 40 °C to 53 °C in order to emulate the virtual solder joint fatigue at the same time. The $V_{CE\_ON(inter)}$ is kept to 1.071 V, which increase due to the bond-wire fatigue. On the other hand, $V_{CE\_ON(peak)}$ increases from 2.012 V to 2.054 V. $\Delta V_{CE\_ON(peak)}$ of 42 mV means 14 °C increase in T_j.

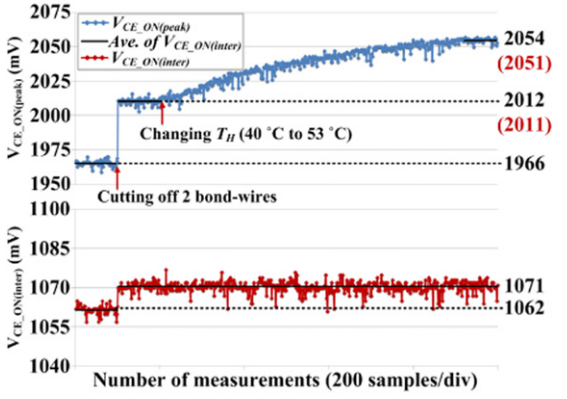

Fig. 9. Experimental result under bond-wire and virtual solder joint fatigues; Black: measured value, Red: reference value.

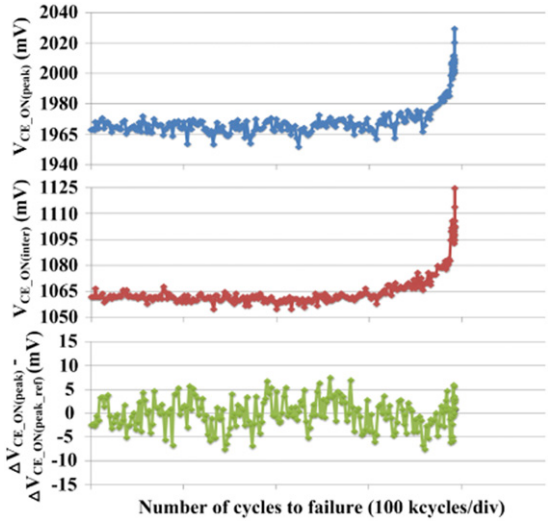

Fig. 10. Experimental result of power cycling test.

This result agrees with the variation of T_H. It results in only 1 °C error. Compared with initial $V_{CE\_ON(peak)}$, the $V_{CE\_ON(peak)}$ increases by 88 mV and it is possible to determine that a 46 mV increase is due to the bond-wire fatigue and a 42 mV increase is caused by the solder joint fatigue. This result is good agreement with Case 4 in Eq. (4). Furthermore, in the case of the solder joint fatigue, the amount of T_j increase can be obtained indirectly in order to decide if it is reached to the end-of-life criterion.

Finally, the proposed monitoring strategy is validated under the power cycling test. $V_{CE\_ON(inter)}$ and $V_{CE\_ON(peak)}$ are measured in real time as shown in Fig. 10. As $V_{CE\_ON(inter)}$ increases, $V_{CE\_ON(peak)}$ also increases and $\Delta V_{CE\_ON(peak)}$ is almost the same with $\Delta V_{CE\_ON(peak\_ref)}$. The difference is less than around 7 mV, which leads to only 2.5 °C. This result is in agreement with Case 2 in Eq. (3). Thus, it can be expected that bond-wire fatigue occurs.

5. Conclusion

In this paper, an advanced power cycler with an intelligent monitoring strategy is proposed. The detailed explanations of configuration, features and control method of the power cycler are presented. By this, the PC test can be performed cost-effectively under more realistic electrical conditions. In addition, an intelligent monitoring strategy for the separation of wear-out failure mechanisms is proposed. It can be achieved by monitoring two V_{CE_ON}s at the intersection and peak current points with two preliminary characterizations. This strategy with real-time V_{CE_ON} measurement circuit gives some advantages to perform the power cycling test. First of all, power cycling test does not need to be stopped in order to measure the failure indicators and also for re-characterization. Furthermore, the power cycling test can be finished properly before the catastrophic failure occurs, which enables to perform a physical failure analysis of DUT. Finally, it helps to better understand wear-out characteristics and also to define wear-out failure mechanisms before the failure analysis of DUT.

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