On-Line [T_J, V_{ce}] Monitoring of IGBTs Stressed by Fast Power Cycling Tests

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Abstract

This paper describes a part of a larger supervision system able to monitor the on-state voltage V_{CE} and the junction temperature T_J of IGBT in operation. That system is associated to an ageing test bench stressing IGBT modules by power cycling. All along the ageing test, it is necessary to supervise V_{CE}, always measured in the same conditions of junction temperature and collector current, in order to detect possible degradations of wire bonds and/or emitter metallization.
In addition, the thermal swing amplitude of the power cycling must be adjusted to realize a given ageing protocol. That requires measuring the junction temperature evolution on a power cycle to choose the initial electrical conditions providing the wished temperature swing and then, to regularly verify the stability of this thermal stress during the ageing test.
The temperature measurement needed for both monitoring is carried out by means of V_{CE} measurement at low current level (100mA), that intrinsic on-stage voltage being a well-known thermo sensitive parameter.
The first section describes briefly the ageing test bench, that places the power IGBT modules in operating conditions close to those of real world (PWM operations), and presents the thermal stress protocol applied to the devices, the aim being to define the context in which the measurements have to be made.
The second section presents, on the one hand, the principle of an automated measurement of V_{CE}(100A-125°C), made in steady-state, to detect a possible degradation of the top part of IGBT dies, on the other hand, the dynamic measurement of the junction temperature in operation, i.e. in power cycling conditions generated by the PWM modulation. In both cases, experimental results are shown that demonstrate the feasibility and the good accuracy of these monitoring methods.

I. Introduction

In numerous applications, power devices suffered from thermo mechanical stresses resulting from power cycling and which induce ageing mechanisms [1]-[9]. In IGBT power modules, all components are concerned. The proposed paper will present on the one hand a test bench able to stress IGBT under power cycling conditions with a high repetition period and, on the other hand, the measurement method and system that has been developed to acquire values of the junction temperature and of the on-state voltage V_{CE} during the tests.
The V_{CE} parameter is used as an ageing indicator of the bond wires and emitter metallization [10][11]. It must be monitored to evaluate the degradation level of the device during the test and to stop the test before the failure. The junction temperature is needed to control the thermal swing amplitude but also for the V_{CE} measurement that must be achieved with given conditions of die temperature and current.
The first section provides a brief overview of the main features of the experimental test bench with a focus on the module's thermal operating conditions. The second section presents the principle of the on-line measurements and the corresponding hardware system that has been implemented.

II. Ageing test bench and power cycling conditions

A. Tested devices

The tested devices are IGBT modules including one inverter leg and using 600V-200A trench gate chips (Figure 1). There are representative of the current technology using mainly A/N DBC and wire bonds to interconnect the top part of the IGBT dies. The global aim of the work is to collect quantitative data concerning metallization and wire bond degradations under variable conditions of power cycling.

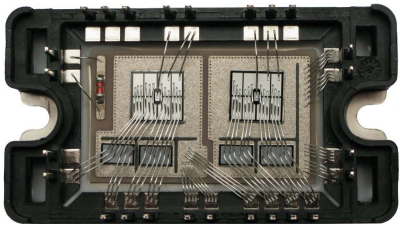

Figure 1 : View of the tested IGBT module

B. Power stage of the test benches and power cycling conditions

The samples are aged in a test bench operating in switching conditions (PWM control, Figure 2).
This test bench uses two modules to constitute a PWM Bridge that operates as a drive inverter with respect to the electrical stresses applied to IGBT dies (PWM switching, sinusoidal modulation, [12]). Therefore, the dies are placed in conditions very similar to real-world conditions. The switching frequency can be adjusted between 10 and 30 kHz.

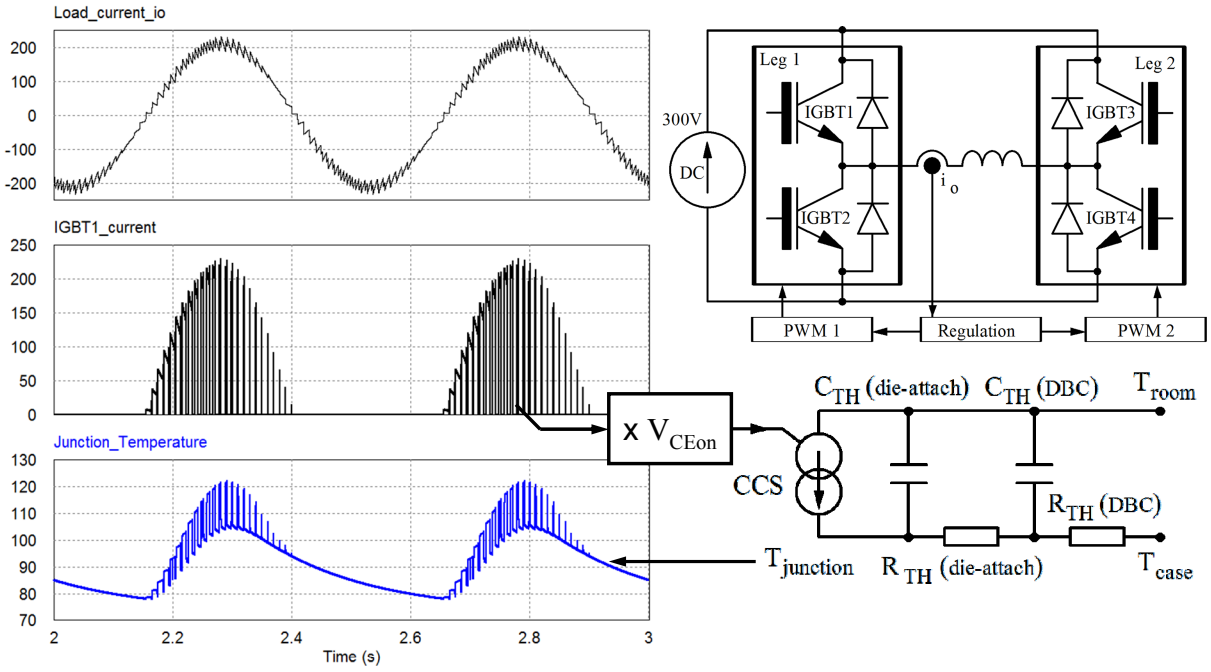

Figure 2 : PWM test bench principle

One of the test originalities is the generation of the junction thermal swing by the use of a low frequency modulation (few hertz). It is the losses variations in IGBT due to the current variations during a half modulation period that creates the temperature variations. The Figure 2 shows a simulation (PSIM software) in which a simplified thermal equivalent circuit (die + DBC) is used to estimate the temperature swing. The equivalent current source (CCS) corresponding to IGBT losses is driven by the simulated IGBT current (taking into account the PWM modulation) multiplied by an constant value of the on-state voltage. To make better appear the electrical current shapes, a low value of the switching frequency has been chosen in the simulation: it induces a high frequency temperature ripple that does not exist in real operation. The result is purely qualitative but illustrates the power cycling conditions imposed in the test bench.
That situation could be compared to thus observed in a drive inverter at low-speed operations. In regard with the thermal swing frequency used in classical power cycling test (0.02 to 0.1Hz), such values are twenty to fifty times higher, that allows drastically reducing the test durations.
The Figure 3 shows the experimental temperature swing measured with a infrared camera in that test

conditions for a 2Hz PWM modulation.

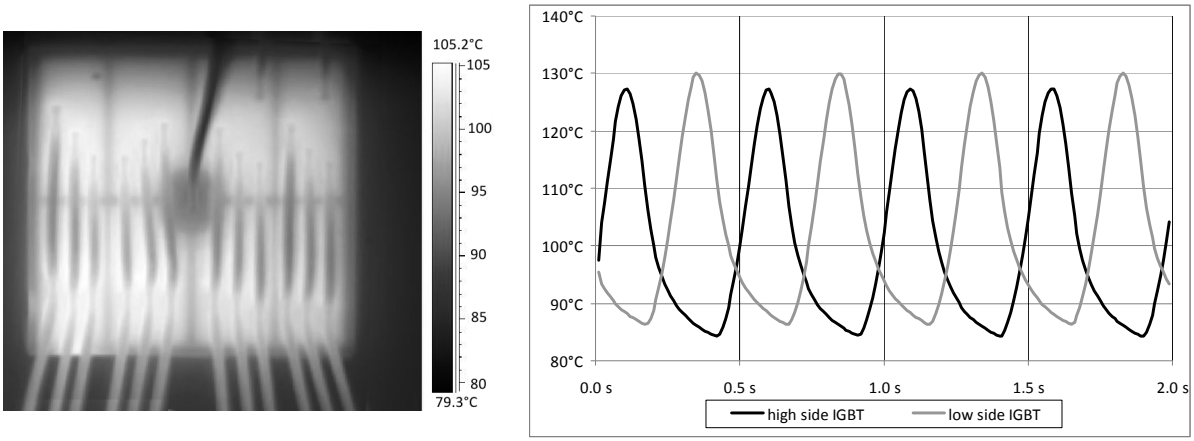

Figure 3 : Experimental jonction temperature in fast power cycling

C. Control part

The test bench supervision system includes two parts [12]. The first is a group of FPGA boards dedicated to PWM control and to protection management for power stages. The second is a group of PC and acquisition boards that manage the power cycling, handle the regulation and acquire and store all the test data (namely temperatures, voltages, currents). Figure 4 gives some views of the system.

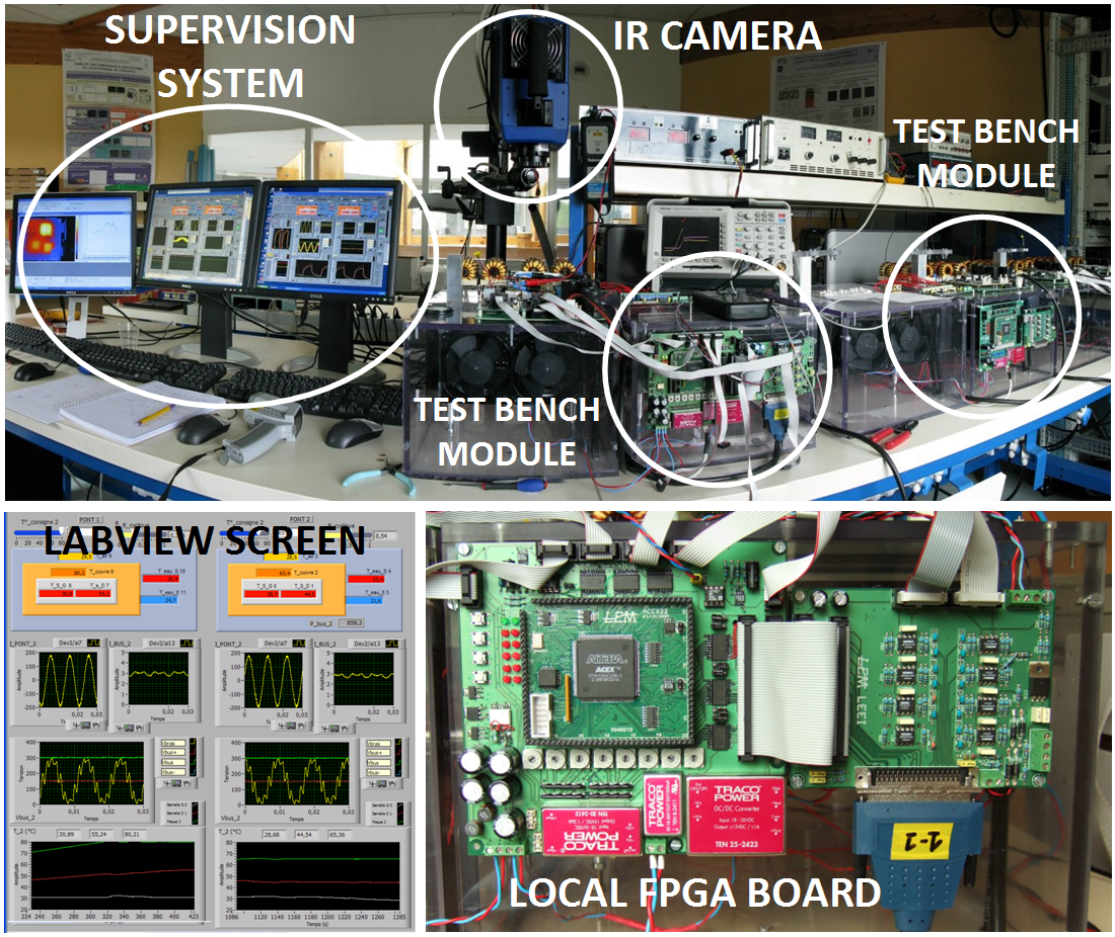

Figure 4: Views of the complete system

III.On-line [T_J, V_{CEo}] measurement

A. Principle and hardware

To carry out ageing tests under power cycling conditions, ageing indicators have to be identified and then, regularly measured all along the test. The more usually used is the on-state voltage across the IGBT that allows detecting wire bond and metallization degradations. It is retained in the considered tests and it has been chosen to make an on-line measurement to reduce drastically the manpower assigned to the test supervision.

This on-line V_{CEo} measurement is very critical. Indeed, it must be carried out under strictly controlled temperature and current conditions (125°C and 100A in the present tests) to monitor always the same operating point and must be extremely accurate (uncertainty lower than 1%) to detect very low V_{CEo} variations at this operating point, that should reveal the degradations mentioned above. A major difficulty is the insertion of instrumentation devices able to provide that accuracy in power stages supplied by high voltage and in which the currents and temperatures vary periodically. In the considerate test bench, it is possible to modify the PWM control to insert the measurement process, the changes introduced in the time scale of some switching periods having no significant effect on the thermal stresses generated by the test bench.

Therefore, repetitive V_{CEo} measurements have to be made under constant temperature and current conditions. The first choice for the strategy is to carry out an indirect temperature measurement via V_{CEo} [3][9]. This requires a preliminary characterization of each die as shown Figure 5, which is easy to achieve. It must be performed under a low current level in order to eliminate the voltage drop due to the connections. On that basis, the proposed instrumentation structure is shown in Figure 6. To simplify the schematic parallel diodes are not drawn.

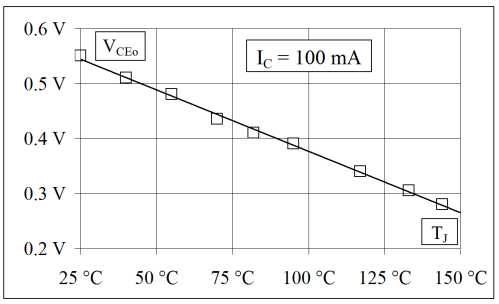

Figure 5 : Curve of V_{CEo} thermal sensibility

This structure uses two stages, one for the high side IGBT and one for the low side IGBT. Each stage includes a V_{CEo} clamp (V_{C1}, AS_{C1}, R_{C1} and V_{C2}, AS_{C2}, R_{C2}) to limit the measured voltage when IGBTs are in off-state, a 100 mA current sink for the indirect temperature measurement (AS_1, R_{TJ1} and AS_2, R_{TJ2}) and a voltage-level shifter (OA1, AS_{LA1}, R_{LA1}, R_{m1} and OA2, AS_{LA2}, R_{LA2}, R_{m2}). All these devices are implemented near the IGBT power module. Another identical measurement board is associated with the two other IGBT.

To carry out the measurements, the IGBTs have to be disconnected from the load and the current flowing between both legs has to be derived. Additional MOSFETs (S1) and IGBTs (S2) introduced in the load line allow respectively realizing these operations (Figure 7) in a very short time (< 1µs) in order to avoid die temperature decrease.

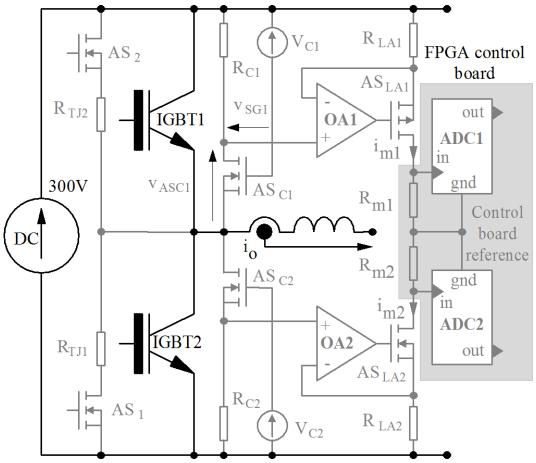

Figure 6 : V_{CEo} measurement scheme

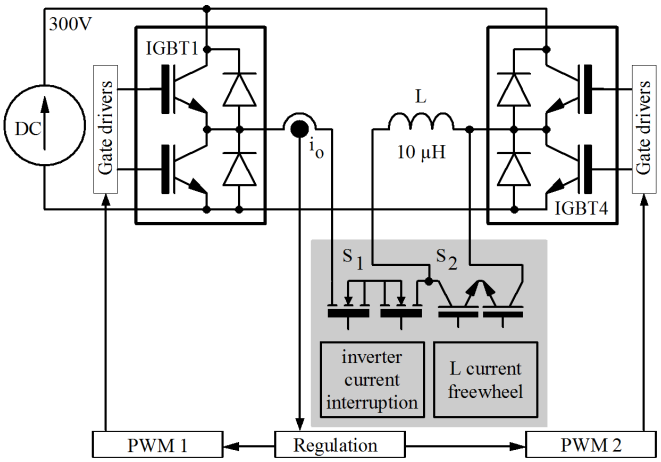

Figure 7 : Power stage arrangement

B. The different measurement strategies and results

1) V_{CEo} (I_C, T_J) measurement strategy

This measurement is needed to follow the evolution of IGBT state in regard with ageing [10][11]. It does not require to be made at each thermal cycle. Its periodicity can be adjusted along the test, from a low value (for example 1000 cycles) at the beginning and a higher value (for example 100 cycles) when a degradation appears.

This periodic V_{CE} measurement has always to be made for the same fixed I_C current (here 100A) and the same fixed junction temperature (here 125°C) in order to obtain an ageing indicator. To reach this aim, the normal test operation is stopped and a particular switching sequence is introduced (buck operation) to make the switch current and the junction temperature vary around the fixed values. Indeed, it is not possible to impose directly the right operating point. For example, to make the measurement on IGBT1, this one is maintained in on-state while IGBT4 is switching (20kHz) to create a current variation around 100A. Few ten values of $V_{CE}(I_C, T_J)$ are acquired and stored, then the IGBT1-IGBT4 are stopped, S2 is switched-on, S1 is switched-off and an immediate indirect temperature measurement is made, available for all the acquired values because the case temperature does not significantly vary (0.1°C/ms) during the acquisition sequence. The latter allows obtaining a first V_{CEo} (I_C, T_{J1}) characteristic for a given temperature T_{J1}.

The buck operation is then restarted during few ten ms to increase the case temperature and a second acquisition sequence is carried out, providing a second characteristic for a second temperature T_{J2}. Finally, three characteristics are successively built. The researched value is extracted from this family by an interpolation that can be made in parallel after the restart of the normal operation. The duration of the complete measurement cycle is around 0.5 s if the initial case temperature is greater than 70°C, i.e. if the test bench was in steady-state operation just before.

The Figure 8 shows an example of measurements series made around 100A and 125°C. The point V_{CEo}(100 A)-125°C is extrapolated from the closest results, corresponding here to junction temperature values of 117°C and 133°C.

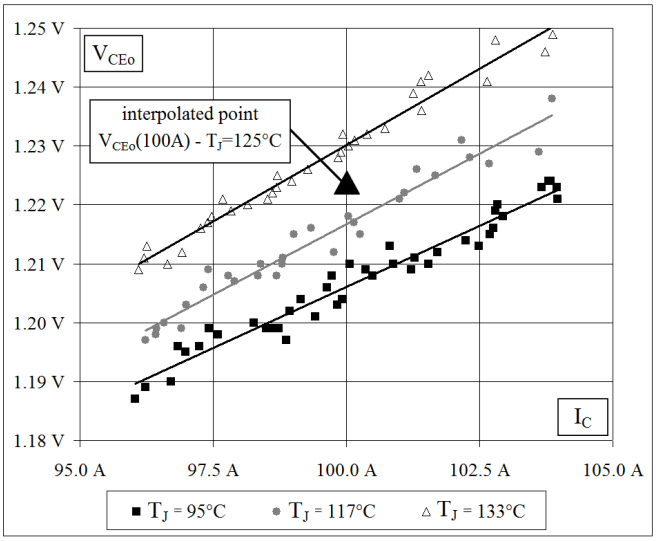

Figure 8: On-line measurements of V_{CEo}(Ic) on IGBT for three temperatures

C. T_J measurement strategy in operation

In that case, it is the measurement of the thermal swing generated by the modulation (few Hz) that is aimed to initially adjust and to regularly verify the power cycling conditions. Therefore, several indirect measurements of the junction temperature must be made on the modulation period. In case of steady-state, a sub-sampling strategy can also be applied by making one indirect measurement on several modulation periods with a different sampling time for each period.

The indirect measurement is achieved by stopping the normal operation during a short time (few switching periods) used to inject the 100mA current in the chosen IGBT. To generate that acquisition window, the control sequence of the different IGBT and switches is identical to thus described in the previous section.

During that window, few ten values of V_{CEo}(100mA) are acquired and stored. They will be used later to generate a more accurate final value by averaging, finally converted in a temperature value by using the intrinsic thermal characteristic of the considered IGBT. The Figure 9 shows a simulation of the interruption effect on the junction temperature, based on the approach described in section II.B (Figure 2-b). In that case, all the values are sampled on the same modulation period. A few degree variation can be observed for each measurement but the accuracy stays correct.

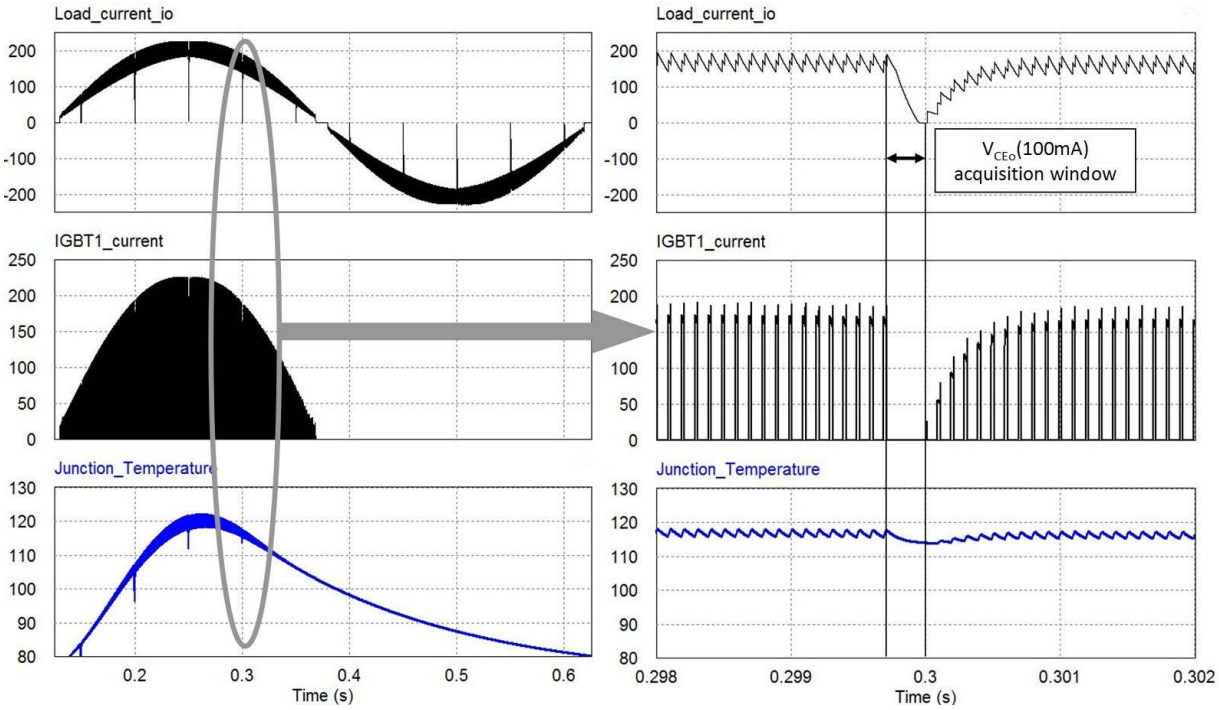

Figure 9 : Simulated effect of measurement interruptions on the junction temperature

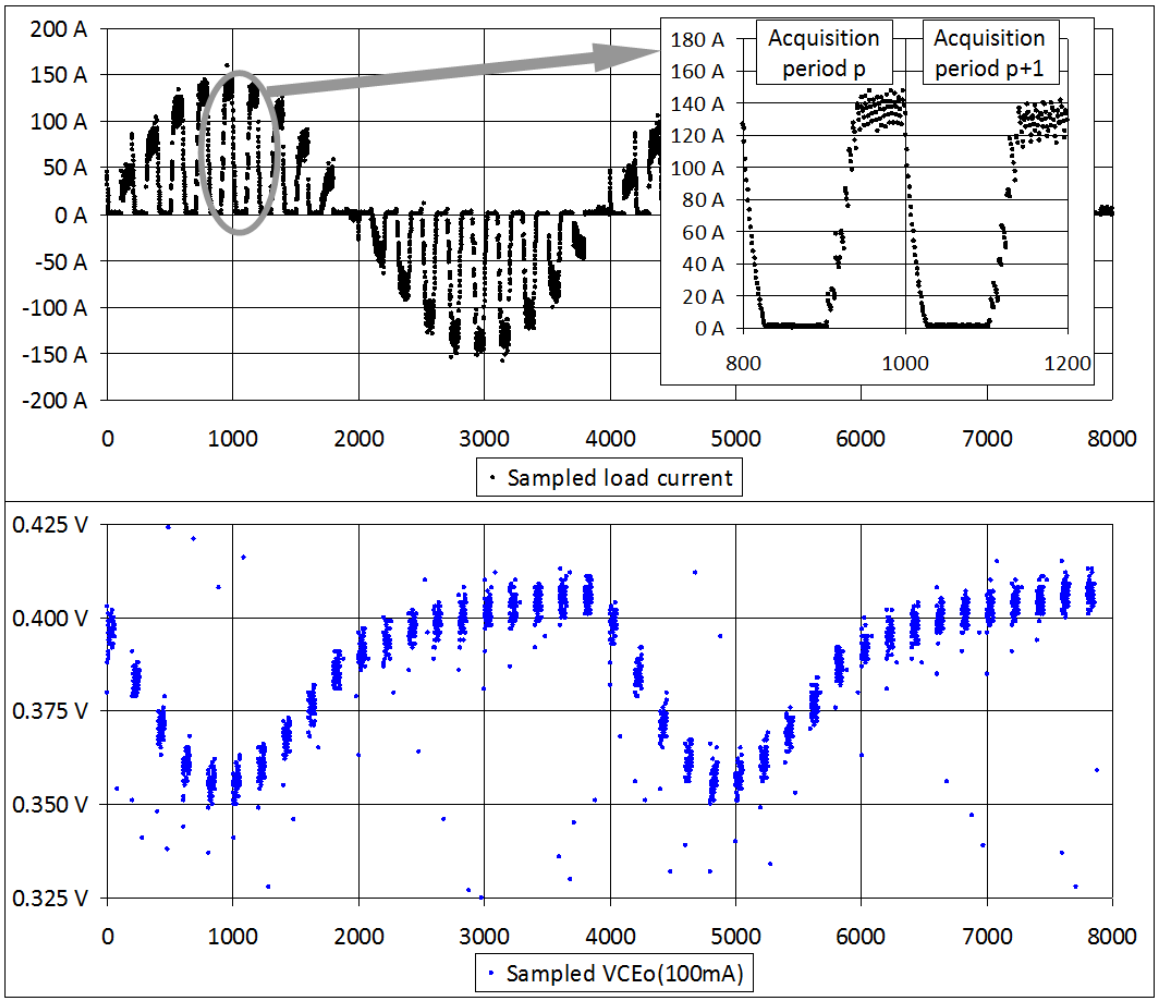

Figure 10: Stored samples in sub-sampling mode

The proposed approach is now successfully applied to the test bench in operation. Two variants are currently tested.

The first variant, limited to steady-state conditions, uses a sub-sampling method. Twenty temperature measures are made on twenty successive modulation periods to reconstitute the junction temperature profile. The sampling frequency is 500kHz (period of 2µs). Figure 10 shows an example of acquisition realized at the operating point [T_{case} = 80°C, I_{CMax} = 140A, V_{DC} = 300V, F_{mod} = 2Hz]. The graphs represent the successive samples of load current i_o and V_{CEo}(100mA) stored in memory along forty modulation periods. In that case, the acquisition window is larger than the current interruption phase imposed by S_1 and S_2 in order to show the current value corresponding to each measure. Therefore, two-hundred samples are stored here for each measure. In the final process, the window will be reduced (few ten samples) to minimize the data file size.
The V_{CEo} graph reveals partially the future shape of the temperature swing, V_{CEo} decreasing linearly with the temperature. In addition, it emphasizes the good reproducibility of the measures. Figure 11 shows the temperature reconstituted from the V_{CEo} measurements on the modulation period. It is compared with the temperature measurement given by the infrared camera. The results have a good coherence.
The sub-sampling method is not necessary for the two Hz ageing test but other tests using higher modulation frequency could require that method, now validated.

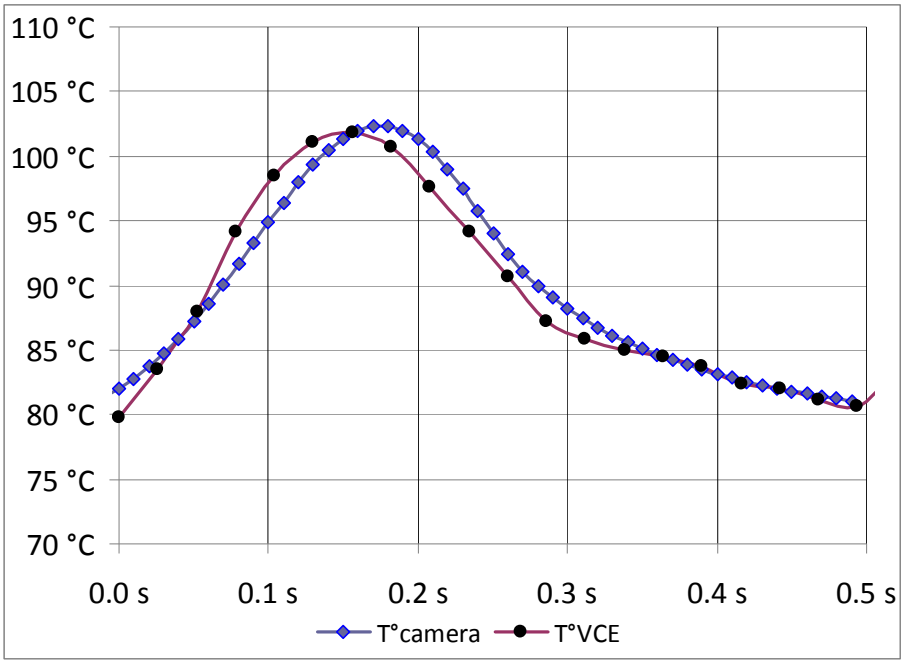

Figure 11: Comparison of temperature variations measured via V_{CEo} and by IR camera

The second variant is in accordance with the simulation presented Figure 9. Ten V_{CEo} samples are directly acquired on the modulation period without sub-sampling. The sampling frequency is always 500 kHz. This variant is applicable in case of low-frequency modulation and does not require steady-state operation. In order to verify the assumption of a low impact on the temperature swing if a direct sampling is used, the result obtained in this case has been compared to the result obtained in sub-sampling mode with ten modulation periods, for the same operating conditions [T_{case} = 80°C, I_{CMax} = 140A, V_{DC} = 300V, F_{mod} = 2Hz]. The Figure 12 shows the comparison. Values are very similar in both configurations, confirming that ten samples can be acquired on a modulation period (with ten interruption windows) without any influence on the temperature evolution. That sample number is enough to provide an accuracy in accordance with the aims of temperature swing measurement, i.e. operation control and adjustment of test protocol conditions.

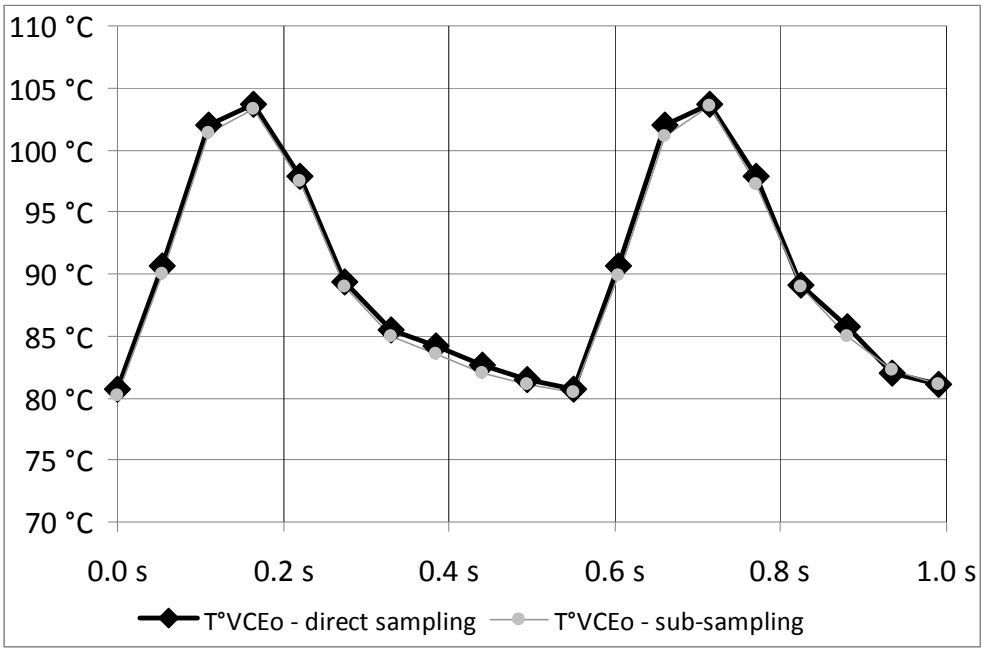

Figure 12 : Comparison of direct sampling mode and sub-sampling mode

IV. Conclusion

The on-line measurement system described in this paper has been developed to monitor different parameters in ageing test benches dedicated to the test of power IGBT modules. The main parameter considered here is the on-stage voltage V_{CEo}, measured for fixed conditions of junction temperature and collector current, and well known as a relevant indicator of degradations that can hit wire bonds and/or emitter metallization. Therefore, the V_{CEo} measurement requires the junction temperature measurement that is another challenge to take up.

The implementation of the instrumentation hardware able to reach that aims requires measuring very low voltage variations while the power stage switches the high DC voltage. The solutions proposed here allow solving that technological difficulty and carrying out measurements enough accurate to provide the function, as it is demonstrated by the experimental results. Therefore, the supervision system can realize automatically the periodic characterizations needed to detect possible IGBT module degradations while the test bench is maintained in operation. As a drawback, the principle described here uses additional power switches to generate the measurement windows and cannot be directly applied to real converters in operation. Nevertheless, it can be considered by using possible standby states of these converters to introduce a specific measurement sequence. That can constitute a way to provide advanced real-time diagnostic on semi-conductor power devices in real power electronic systems.

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