A 15 kV SiC MOSFET Gate Drive with Power over Fiber based Isolated Power Supply and Comprehensive Protection Functions

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***Abstract*—This paper presents a 15 kV SiC MOSFET gate drive circuit, which features high common-mode (CM) noise immunity, small size, light weight, and robust yet flexible protection functions. To enhance the gate-drive power reliability, a power over fiber (PoF) based isolated power supply is designed to replace the traditional design based on isolation transformer. It delivers the gate-drive power by laser light via optical fiber over a long distance (>1 m), so a high isolation voltage (>20 kV) is achieved, and the circuit size and weight are reduced. More importantly, it eliminates the parasitic CM capacitance coupling the power stage and control stage, and thus eradicates the control signal distortion caused by high *dv/dt* in switching transients of the high-voltage SiC devices. In addition, the gate drive circuit design integrates comprehensive protection functions, including the over-current protection, under/over-voltage lockout, gate-clamping, soft turn-off, and fault report. The over-current protection responds within 400 ns. Experimental results from a 15 kV double pulse tester are presented to validate the design.**

Keywords— common-mode noise immunity; gate drive; high voltage SiC device; isolated power supply; laser power; over current protection; protection functions; power over fiber

I. INTRODUCTION

In recent years, there has been a significantly growing interest in the high-voltage (HV) Silicon Carbide (SiC) based semiconductor power devices and their applications. To date, 10 kV and 15 kV SiC MOSFETs [1-3], 13 kV p-i-n diode [4], 15 kV SiC IGBTs [5-13], and 16 kV n-channel IGBT [4] have been developed and demonstrated. 10 kV SiC MOSFET power modules have already been applied in power electronics building blocks [14-16]. Applications of these HV SiC power devices include medium voltage drives and circuit breakers, power converters for renewable energy integration, STATCOM, active power filters, FACTS devices, and solid-state transformers [1-18].

The gate drive circuit of the HV SiC power devices is critical to ensure fast and reliable switching operation. It is comprised of four major subsystems: 1) an isolated power supply, 2) an isolated signal transfer circuit, 3) the driving circuit, and 4) protection circuits against faults such as over-current/short-circuit, over/under-voltage, over temperature, and etc.

The isolated power supply of the gate drive circuit must be able to sustain high isolation voltage (>15 kV) and achieve high common-mode (CM) *dv/dt* (>110 kV/μs) rejection [19-20]. In traditional designs, the isolation is implemented with transformers [3], [9], [20-24]. To achieve the high isolation voltage, the transformer requires a large magnetic core to separate the primary and secondary windings and create sufficient creepage distance. This results in a large and heavy gate drive circuit. Moreover, there is inevitable CM parasitic capacitance coupling the windings of the transformer, which makes the gate drive circuit sensitive to high CM *dv/dt,* causing distortion in the gate-drive input signals, cross talk between gate drives, and malfunction in upstream control circuits [19-20]. As an alternative solution for the isolated gate-drive power supply, wireless power transfer using separated coils has been studied in [25-27]. However, this solution is also sensitive to EMI, and it requires large space for isolation and shielding.

To achieve reliable yet compact design of the gate drive circuit, in this paper a power over fiber (PoF) based isolated power supply is proposed. It delivers sufficient gate-drive power by laser light via optical fiber over a long distance (>1 m), so a >20-kV isolation voltage is achieved. It eliminates the parasitic CM capacitance coupling the power stage and control stage, and achieves significant size and weight reduction of the gate drive circuit. Although the laser emitter, which can be placed far away from the main power stage, may offset the overall system volume reduction, the main power stage layout can be optimized with smaller gate drive circuits.

To ensure safe operation, the gate drive circuit must integrate fast and reliable protection functions against faults such as over-current/short-circuit. Compared to Si devices, SiC devices tend to have lower short circuit withstand capability, and the high *dv/dt* and *di/dt* noises also make fault detection more challenging [28-30]. Although over-current protection schemes for 1.2 kV SiC MOSFETs have been discussed in

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[30], the over-current protection for the HV SiC devices is more challenging because of much higher isolation voltage and higher *dv/dt* [1], [10], [19]. This paper presents the design of comprehensive protection functions for the 15 kV SiC MOSFET, including over-current protection, gate-drive power under/over-voltage lockout, gate-clamping, and soft turn-off.

II. Design of the Isolated Gate-drive Power Supply

A. Power over Fiber based Laser Receiver

Power over fiber (PoF) is a technology in which a fiber optic cable carries optical power, which is used as an energy source rather than, or as well as, carrying data [31-32]. This allows a device to be remotely powered, while providing electrical isolation between the device and the power supply. *MH GoPower Co., Ltd.* offers a PoF laser receiver YCH-0.5-6V, which is shown in Fig. 1. The major specifications of this laser receiver are as follows:

- Optimized for 915 nm, 940 nm, or 975 nm laser sources.
- Conversion efficiency at 1 W input: Typical ~24%.
- Max electrical output power: ~0.5 W.

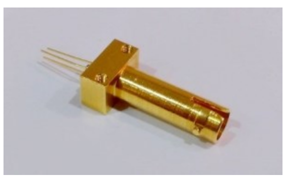
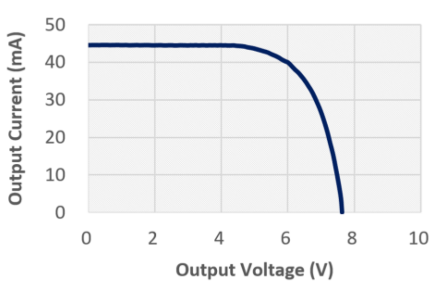


Fig. 1. The 0.5 W PoF laser receiver YCH-0.5-6V from *MH GoPower Co., Ltd.*

Fig. 2 shows the output I-V curve and P-V curve of the PoF laser receiver YCH-0.5-6V at 1 W input optical power.



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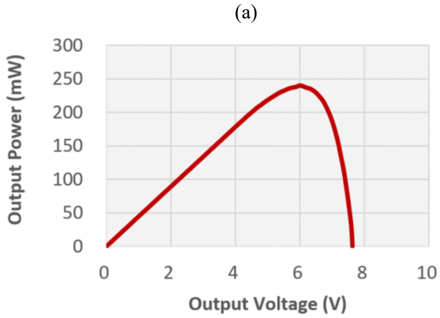

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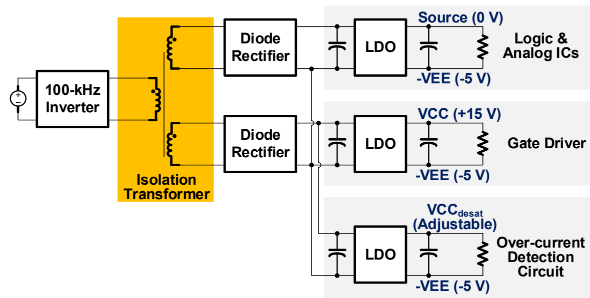
Fig. 2. The output (a) I-V curve and (b) P-V curve of the 0.5 W PoF laser receiver YCH-0.5-6V at 1 W input optical power.

The maximum electrical power supplied by this PoF laser receiver is 0.5 W. It is low but sufficient for driving the 15 kV, 10 A SiC MOSFET switching at 10 kHz, given the measured device input capacitance is around 4.24 nF.

B. Transformer-based and PoF-based Isolated Gate-drive Power Supply

To demonstrate the CM noise immunity improvement and circuit size reduction of the PoF-based isolated gate-drive power supply, two designs of the isolated gate-drive power supply are presented, including a traditional transformer-based design and a proposed PoF-based design. The schematics of the two designs are shown in Fig. 3.



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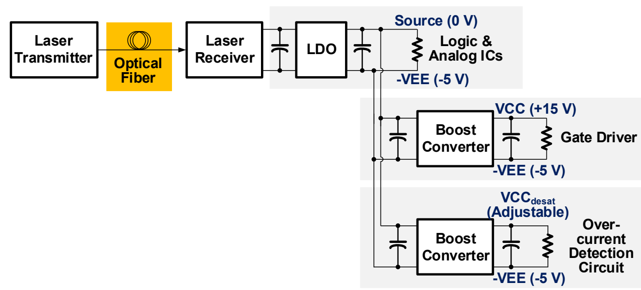


(b)

Fig. 3. Schematics of the two designs of the isolated gate-drive power supply, including (a) a transformer-based design, and (b) a PoF-based design.

It can be seen from Fig. 2 that the laser receiver is indeed a photovoltaic cell, which features a maximum power point in operation. Thus, there exists a minimum input laser irradiance that matches the maximum output power of the laser receiver with the required gate-drive power, and the operation at such a sweet spot minimizes the gate-drive power loss. However, power converters built upon the 15 kV SiC devices are typically operated at 5~10 kHz because of the device thermal limitation [1-16], so the gate-drive power loss is negligible compared to the main power stage loss. Therefore, for simplification of the design, the matching between the input laser light irradiance and required gate-drive power is not implemented.

Based on the two different designs of the isolated gate-drive power supply presented in Fig. 3, two prototypes of the gate drive circuit for the 15 kV SiC MOSFET are built and presented side by side for comparison, as shown in Fig. 4.

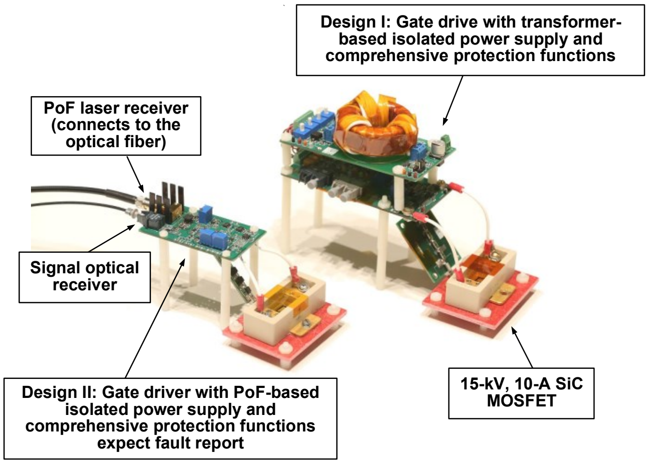


Fig. 4. Two prototypes of the gate drive circuit for the 15 kV SiC MOSFET. They are with two different designs of the isolated gate-drive power supply, including a transformer-based design and a PoF-based design.

The transformer-based isolated gate-drive power supply suffers inevitable parasitic CM capacitance coupling the isolated transformer windings. The measured results of this capacitance are shown in Tab. I. In the PoF-based design, this parasitic CM capacitance is eliminated, as a result of the long-distance (>1 m) laser transmission via fiber optics.

TABLE I. MEASURED PARASITIC CM CAPACITANCE COUPLING THE ISOLATED TRANSFORMER WINDINGS

Frequency	1 kHz	10 kHz	50 kHz	100 kHz
CM capacitance	3.5 pF	3.47 pF	3.48 pF	3.49 pF

Compared to the transformer-based isolated power supply, the PoF-based design has the following advantages:

- Higher insulation voltage (>20 kV).
- Reduced size and weight.
- Higher CM transient rejection (>200 kV/µs) because of the elimination of parasitic CM capacitance.

III. DESIGN OF COMPREHENSIVE PROTECTION FUNCTIONS

The gate drive design integrates comprehensive protection functions, including the over-current protection, under/over-voltage lockout, gate-clamping, soft turn-off, fault report, and protection mode selection to allow either single or multiple faults. Fig. 5 shows the schematic for the protection circuits, where the under/over-voltage lockout function is not included as it is implemented with voltage monitoring ICs.

A. *Over-current Detection*

For the over-current protection design, the "desaturation detection" method used for IGBTs-based power circuits is employed. This method is generally applicable for HV MOSFETs given that their output characteristics are similar to IGBTs in the active region. It is also already demoed in the over-current protection for 1.2 kV SiC MOSFETs [30]. For the 15 kV SiC MOSFETs, the challenges to implement this method have been the high voltage bias and high *dv/dt* on the device drain terminal.

To sense the drain-to-source voltage drop across the switch in the ON state and block the high drain voltage bias in the OFF state, five 3.3 kV SiC Schottky diodes (D_{ss1}-D_{ss5}) are connected in series to the switch's drain terminal. This is not only to achieve sufficient reverse-bias blocking voltage (>15 kV), but also to greatly reduce the equivalent sensing diode junction capacitance. In the presence of high *dv/dt* at the switch's drain terminal, lower junction capacitance of the sensing diodes causes less displacement current flowing from the switch drain terminal to the sensing analog circuits, and thus reduces the risk of false trigger of the protection.

However, the series connection of the five sensing diodes causes an equivalent diode forward voltage five times higher, which results in a large offset in the sensed voltage and thus lower the sensing resolution. In the design, a high-speed, 5 V analog comparator is chosen to achieve fast response time. To match the comparator's input voltage range, the sensed voltage is scaled down with a resistive voltage divider (R_{div1} and R_{div2}). Also, the voltage level (VCC_{desat}) of the PWM buffer output needs to be adjusted accordingly.

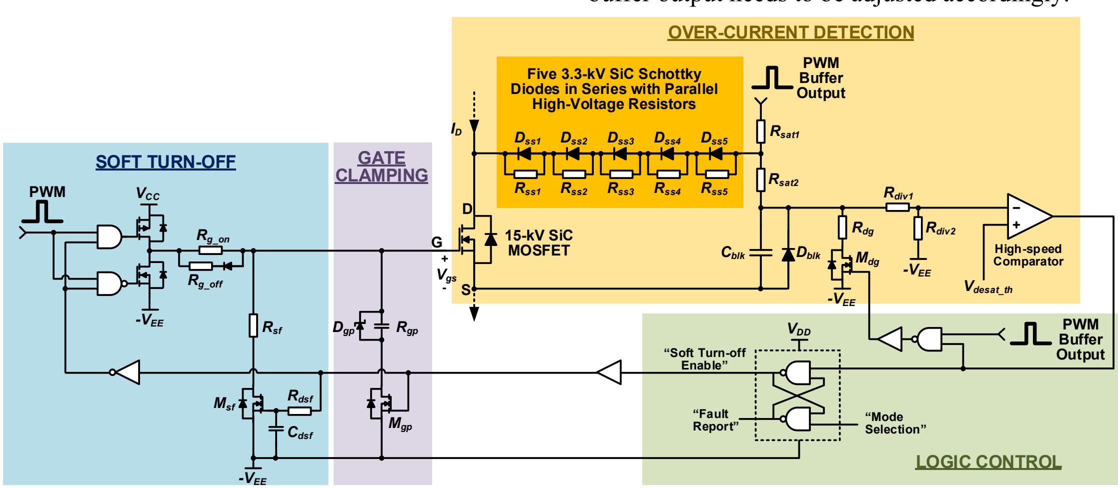


Fig. 5. Schematics of the protection functions including over-current protection, gate-clamping, soft turn-off, fault report, and protection mode selection to allow either single or multiple faults.

Another problem of the series connection of the sensing diodes is the non-uniform voltage distribution across those diodes when reverse-biased, which would cause breakdown failure of those diodes. To solve this problem, HV rated resistors (R_{ss1}-R_{ss5}) are added in parallel with each sensing diode to balance the voltage distribution.

The over-current protection for the 15 kV SiC MOSFET is currently designed to be triggered in the device triode region rather than the saturation region. This is because the behaviors of 15 kV SiC MOSFETs in the saturation region are not yet experimentally investigated due to the limited testing samples. However, the over-current protection in the device triode region allows the triggering at a much lower device current, which enables a safer device operation.

B. Over-current Protection Response Time

The response time of the over-current protection circuit relies heavily on the blanking time delay, which is required to bypass the device turn-on transient current to avoid false triggering. As shown in [1] and also in the section V of this paper, the normal turn-on transient current of the 15 kV SiC MOSFET could surge to a very high value during the blanking time. The blanking time is set by the blanking capacitance (C_{blk}) and oscillation damping resistor (R_{sat1}). The selection of these parameters are discussed in [30]. Another resistor R_{sat2} increases the blanking time when the over-current protection is triggered when the sensing diodes D_{ss1}-D_{ss5} are reverse biased. To prevent false triggering of the protection during the device turn-off transient, an auxiliary switch M_{dg} and a current limiting resistor R_{dg} discharges the C_{blk} after the device is turned off. The designed over-current protection total response time under hard-switching fault (HSL) is presented in Tab. II.

TABLE II. OVER-CURRENT FAULT RESPONSE TIME

Detection Delay	Comparator Delay	Logic Control Delay	Total Delay
330 ns	4.5 ns	45 ns	379.5 ns

IV. DESIGN OF A 15 KV DOUBLE PULSE TESTER

A 15 kV double pulse tester is built to verify the designed gate drive circuit for the 15 kV SiC MOSFET. The schematic of the double pulse tester is shown in Fig. 6, and the prototype and setup are shown in Fig. 7.

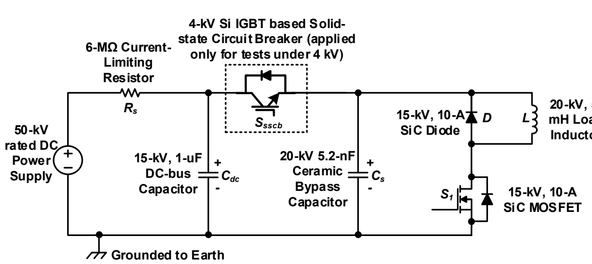


Fig. 6. Schematic of the 15 kV double pulse tester.

The gate drive circuit over-current protection is debugged in the tests with dc-bus voltage applied under 4 kV. During the debugging test, a designed 4 kV Si IGBT based solid-state circuit breaker is applied in the test connections for additional short-circuit protection, as shown in Fig. 6.

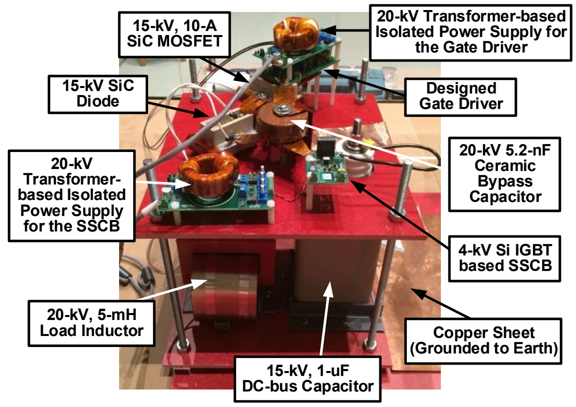


Fig. 7. Prototype of the 15 kV double pulse tester.

The design of the 20-kV, 5-mH inductor is presented in [21]. To enhance the insulation capability, the inductor winding cables are upgraded to the 20 kV rated cable ETN 2022 from *Wiremax*. This cable is also used to make connections between the power stage components of the 15 kV double pulse tester.

V. EXPERIMENTAL VERIFICATIONS

A. PoF-based Gate Drive Circuit Test

To verify the driving power capability, the designed PoF-based gate drive circuit is tested to drive a 12 nF load capacitor, at a 0.5 duty ratio and a 10 kHz switching frequency. The experimental waveforms are shown in Fig. 8. The 12 nF load capacitance is 3 times larger than the input capacitance (4.24 nF) of the 15 kV SiC MOSFET, so it is verified that the designed PoF-based gate drive circuit can supply sufficient driving power.

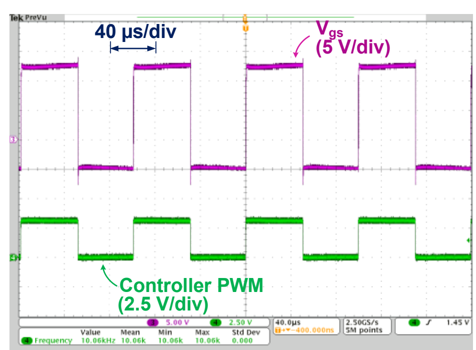


Fig. 8. The experimental results of the designed PoF-based gate drive circuit driving a 12 nF load capacitor, at a 0.5 duty ratio and a 10 kHz switching frequency.

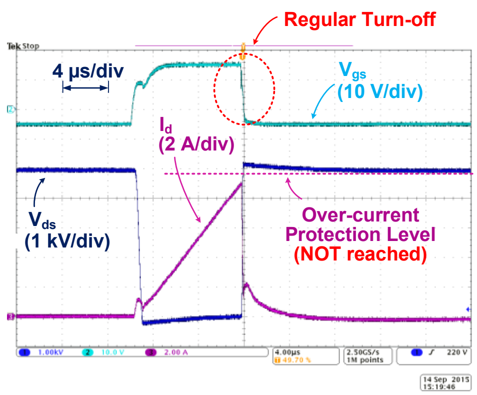
B. Protection Functions Test

To verify the designed comprehensive protection functions, a single pulse test of the 15 kV SiC MOSFET is conducted on the designed 15 kV double pulse tester. The test setup is shown in Fig. 6 and Fig. 7. Before the test, the insulation between critical electrical points of the setup is verified, with 8 kV dc voltage applied for 10 minutes. Insulation tests at higher voltage will be continued in future work. In the single pulse test, the turn-on gate resistance is 66 Ω, and the turn-off gate resistance is 10 Ω. Tab. III shows the measurement equipment.

TABLE III. MEASUREMENT EQUIPMENT SPECIFICATIONS

Equipment	P. N.	Bandwidth	Measurement
Oscilloscope	DPO4054B	500 MHz	
20 kV single-ended probe	P6015A	75 MHz	V_{ds}
300 V passive probe	TPP1000	1 GHz	V_{gs}
30 A current probe	TCP0030A	120 MHz	I_d

Fig. 9 shows the experimental waveforms before and after triggering the over-current protection, which is set at 9.6 A. It can be seen that the designed over-current protection, gate clamping, and soft turn-off are all verified. The device drain current (I_d) after turn-off shows a tail which damps out slowly. Similar test result can be seen in [1]. This could be caused by the resonance between the load inductor and the device output capacitance, which needs further study to confirm.



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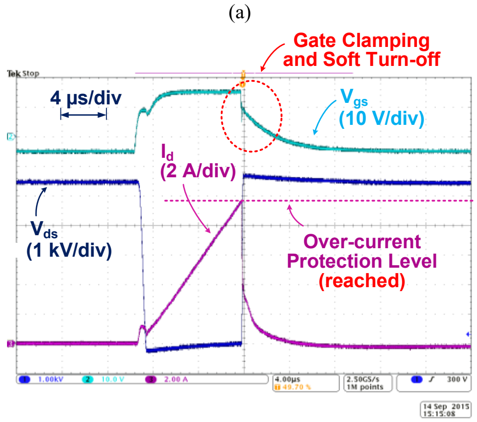


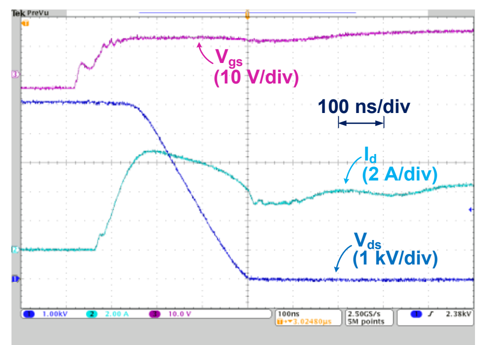
(b)

Fig. 9. The experimental results (a) before and (b) after triggering the designed protection functions including the over-current protection, gate clamping, and soft turn-off.

C. Double Pulse Test of the 15 kV SiC MOSFET

After the protection functions are verified, the experiments with gate drive circuit are continued to a preliminary 6 kV double pulse test of the 15 kV SiC MOSFETs. The test setup is shown in Fig. 6 and Fig. 7. In the test, in order to increase the device switching speed, the turn-on gate resistance is reduced to 10 Ω, and the turn-off gate resistance is reduced to 2 Ω. The measurement equipment are kept the same as specified in Tab. III.

The experimental waveforms are shown in Fig. 10. It can be seen that the device *dv/dt* only reached about 30 kV/µs, which is much less than the results presented in [1]. This is because: 1) the tested I_d is low, which slows down the charge transfer between the MOSFET and the diode in switching transients, 2) the applied gate voltage (+15 V) is low, which limits the device transconductance, 3) the applied gate resistance is still relatively large, and 4) the main power loop has excessive stray inductance because of the large loop length and non-optimized loop layout.



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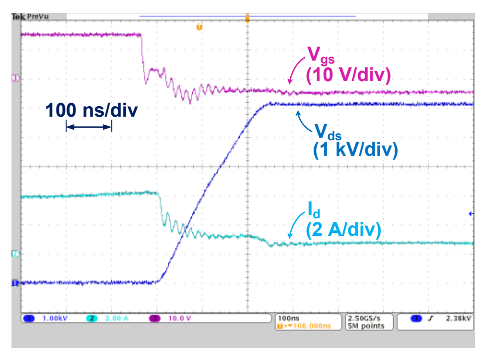

(b)

Fig. 10. Experimental waveforms of the preliminary 6 kV double pulse test of the 15 kV SiC MOSFET in the (a) turn-on and (b) turn-off events, under the test conditions R_{g_on} = 10 Ω, R_{g_off} = 2 Ω, and V_{gs} = +15 V/-5 V.

VI. CONCLUSIONS

This paper propose a PoF-based gate drive circuit for the 15 kV SiC MOSFET. Compared to the traditional transformer-based isolated gate-drive power supply, the PoF-based design features higher insulation voltage (>20 kV), reduced circuit volume and weight, and higher CM transient rejection (>200 kV/µs) due to the elimination of parasitic CM capacitance.

The PoF-based gate drive circuit has sufficient driving power for the 15 kV SiC MOSFET, which is experimentally verified.

The gate-drive circuit design also integrates comprehensive protection functions, including the over-current protection, under/over-voltage lockout, gate-clamping, soft turn-off, and fault report. The over-current protection for the 15 kV SiC MOSFET is currently designed to be triggered in the device triode region. It enable the protection at a low device current. The designed over-current protection total response time under HSL fault is within 400 ns.

A 15 kV double pulse tester is built to verify the designed gate drive circuit. Experimental results of a preliminary 6 kV double pulse test of the 15 kV SiC MOSFET are presented. Further study will be continued to raise the switching speed and test the designed gate drive under harsher *dv/dt* conditions.

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REFERENCES

[1] V. Pala, E. V. Brunt, L. Cheng, M. O'Loughlin, J. Richmond, A. Burk, S. T. Allen, D. Grider, J. W. Palmour, and C. J. Scozzie, "10 kV and 15 kV silicon carbide power MOSFETs for next-generation energy conversion and transmission systems," *Proc. IEEE ECCE 2014*, pp. 449-454, Sept. 2014.

[2] M. K. Das, C. Capell, D. E. Grider, R. Raju, M. Schutten, J. Nasadoski, S. Leslie, J. Ostop, and A. Hefner, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," *Proc. IEEE ECCE* 2011, pp. 2689-2692, Sept. 2011.

[3] S. Madhusoodhanan, A. Tripathi, D. Patel, K. Mainali, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Solid-State Transformer and MV Grid Tie Applications Enabled by 15 kV SiC IGBTs and 10 kV SiC MOSFETs Based Multilevel Converters," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3343-3360, July-Aug. 2015.

[4] F. Fukuda, D. Okamoto, M. Okamoto, T. Deguchi, T. Mizushima, K. Takenaka, H. Fujisawa, S. Harada, Y. Tanaka, Y. Yonezawa, T. Kato, S. Katakami, M. Arai, M. Takei, S. Matsunaga, K. Takao, T. Shinohe, T. Izumi, T. Hayashi, S. Ogata, K. Asano, H. Okumura, and T. Kimoto, "Development of Ultrahigh-Voltage SiC Devices," *IEEE Transactions on Electron Devices,* , vol. 62, no. 2, pp. 396-404, Feb. 2015.

[5] A. Kadavelugu, S. Bhattacharya, S.-H. Ryu, E. V. Brunt, D. Grider, A. Agarwal, and S. Leslie, "Characterization of 15 kV SiC n-IGBT and its Application Considerations for High Power Converters," *Proc. IEEE ECCE 2013*, pp. 2528-2535, Sept. 2013.

[6] D. Rothmund, G. Ortiz, T. Guillod, and J. W. Kolar, "10 kV SiC-based isolated DC-DC converter for medium voltage-connected Solid-State Transformers," in *Proc. IEEE APEC 2015*, pp. 1096-1103, Mar. 2015.

[7] A. Kadavelugu, K. Mainali, D. Patel, S. Madhusoodhanan, A. Tripathi, K. Hatua, S. Bhattacharya, S.-H. Ryu, D. Grider, and S. Leslie, "Medium voltage power converter design and demonstration using 15 kV SiC N-IGBTs," *Proc. IEEE APEC 2015,* pp. 1396-1403, Mar. 2015.

[8] A. K. Tripathi, K. Mainali, D. C. Patel, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "Design Considerations of a 15-kV SiC IGBT-Based Medium-Voltage High-Frequency Isolated DC–DC Converter," *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3284-3294, July-Aug. 2015.

[9] K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A Transformerless Intelligent Power Substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electronics Magazine*, vol. 2, no. 3, pp. 31-43, Sept. 2015.

[10] S. Madhusoodhanan, K. Mainali, A. Tripathi, D. Patel, A. Kadavelugu, S. Bhattacharya, and K. Hatua, "Performance Evaluation of 15 kV SiC IGBT based Medium Voltage Grid Connected Three-Phase Three-Level NPC Converter," *Proc. IEEE ECCE 2015* (to be published).

[11] K. Vechalapu, A. Tripathi, K. Mainali, B. J. Baliga, and S. Bhattacharya, "Soft Switching Characterization of 15 kV SiC n- IGBT and Performance Evaluation for High Power Converter Applications," *Proc. IEEE ECCE 2015* (to be published).

[12] A. Tripathi, K. Mainali, S. Madhusoodhanan, D. Patel, A. Kadavelugu, S. Hazra, S. Bhattacharya, and K. Hatua, "MVDC Microgrids enabled by 15kV SiC IGBT based Flexible Three Phase Dual Active Bridge Isolated DC-DC Converter," *Proc. IEEE ECCE 2015* (to be published).

[13] S. Madhusoodhanan, A. Tripathi, K. Mainali, A. Kadavelugu, D. Patel, S. Bhattacharya, and K. Hatua, "Three-Phase 4.16 kV Medium Voltage Grid Tied AC-DC Converter based on 15 kV/40 A SiC IGBTs," *Proc. IEEE ECCE 2015* (to be published).

[14] D. Grider, M. Das, R. Raju, M. Schutten, S. Leslie, J. Ostop, A. Hefner, "10 kV/120 A SiC DMOSFET half H-bridge power modules for 1 MVA solid state power substation," *IEEE ESTS*, pp. 131-134, 2011.

[15] C. DiMarino, I. Cvetkovic, Z. Shen, R. Burgos, and D. Boroyevich, "10 kV, 120 a SiC MOSFET modules for a power electronics building block (PEBB)," *Proc. 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications (WiPDA),* pp. 55-58, Oct. 2014.

[16] I. Cvetkovic, Z. Shen, M. Jaksic, C. DiMarino, F. Chen, D. Boroyevich, and R. Burgos, "Modular scalable medium-voltage impedance measurement unit using 10 kV SiC MOSFET PEBBs," *Proc. 2015 IEEE Electric Ship Technologies Symposium (ESTS),* pp. 326-331, June 2015.

[17] C. Peng, A. Q. Huang, and X. Song. "Current commutation in a medium voltage hybrid DC circuit breaker using 15 kV vacuum switch and SiC devices." in *Proc. IEEE APEC 2015*, pp. 2244-2250, Mar. 2015.

[18] C. Peng, I. Husain, A. Q. Huang, B. Lequesne, and R. Briggs, "Design and Experimental Investigations of a Medium Voltage Ultra-Fast Mechanical Switch for Hybrid AC and DC Circuit Breakers", *Proc. IEEE ECCE* 2015, Sep. 2015.

[19] K. Vechalapu, S. Bhattacharya, E. V. Brunt, S.-H. Ryu, D. Grider, and J. W. Palmour, "Comparative Evaluation of 15 kV SiC MOSFET and 15 kV SiC IGBT for Medium Voltage Converter under Same dv/dt Conditions," *Proc. IEEE ECCE 2015* (to be published).

[20] A. Kadavelugu, and S. Bhattacharya, "Design considerations and development of gate driver for 15 kV SiC IGBT," *Proc. IEEE APEC 2014*, pp. 1494-1501, Mar. 2014.

[21] L. Fu, X. Zhang, H. Li, X. Lu, and J. Wang, "The development of a high-voltage power device evaluation platform", *in Proc. IEE WiPDA 2014*, pp. 13-17, Oct. 2014.

[22] L. Fu, H. Li, X. Lu, and J. Wang, "Overview and evaluation methodologies of high voltage power devices", *in Proc. IEEE IPMHVC 2014*, pp. 546-549, Jun. 2015.

[23] CONCEPT, "2015 Product Catalog," [Online], Available: https://igbt-driver.power.com/products/product-documents/2015-product-catalog/

[24] M. N. Nguyen, et al., "Compact, intelligent, digitally controlled IGBT gate drivers for a PEBB-based ILC Marx modulator," IPAC'10, pp. 1-3, May 2010.

[25] K. Kusaka, K. Orikawa, J.-I. Itoh, K. Morita, and K. Hirao, "Isolation system with wireless power transfer for multiple gate driver supplies of a medium voltage inverter," *Proc. IPEC-Hiroshima 2014 - ECCE-ASIA 2014*, pp. 191-198, May 2014.

[26] K. Kusaka, M. Kato, K. Orikawa, J.-i. Itoh, I. Hasegawa, K. Morita, and T. Kondo, "Galvanic Isolation System for Multiple Gate Drivers with Inductive Power Transfer Drive of Three-phase Inverter," *Proc. IEEE ECCE 2015* (to be published).

[27] S. Brehaut and F. Costa, "Gate driving of high power IGBT by wireless transmission," *Proc. CES/IEEE 5th International Power Electronics and Motion Control Conference, 2006 (IPEMC 2006)*, pp. 1-5, Aug. 2006.

[28] D. Othman, M. Berkani, S. Lefebvre, A. Ibrahim, Z. Khatir, and A. Bouzourene, "Comparison study on performances and robustness between SiC MOSFET & JFET devices–Abilities for aeronautics application," *Proc. Eur. Symp. Reliab. Electron Devices, Failure Phys. Anal.*, vol. 52, no. 9, pp. 1859–1964, Sep. 2012.

[29] M. K. Dasa, S. Haney, J. Richmond, A. Olmedo, J. Zhang, and Z. Ring, "SiC MOSFET reliability update," *Mater. Sci. Forum*, vol. 717–720, pp. 1073–1076, May 2012.

[30] Z. Wang, X. Shi, Y. Xue, L. M. Tolbert, F. Wang, and B. J. Blalock, "Design and Performance Evaluation of Overcurrent Protection Schemes for Silicon Carbide (SiC) Power MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 10, pp. 5570-5581, Oct. 2014.

[31] Fraunhofer ISE, "Power-by-Light," [Online], Available: https://www.ise.fraunhofer.de/en/business-areas/iii-v-and-concentrator-photovoltaics/research-topics/power-by-light

[32] J.-G. Werthen, "Powering Next Generation Networks by Laser Light over Fiber," in *Proc. Conference on Optical Fiber communication /National Fiber Optic Engineers Conference 2008. (OFC/NFOEC 2008)*, pp.1-3, Feb. 2008.