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An Agile Accelerated Aging, Characterization and Scenario Simulation System for Gate Controlled Power Transistors

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Abstract - *To advance the field of electronics prognostics, the study of transistor fault modes and their precursors is essential. This paper reports on a platform for the aging, characterization, and scenario simulation of gate controlled power transistors. The platform supports thermal cycling, dielectric over-voltage, acute/chronic thermal stress, current overstress and application specific scenario simulation. In addition, the platform supports in-situ transistor state monitoring, including measurements of the steady-state voltages and currents, measurements of electrical transient response, measurement of thermal transients, and extrapolated semiconductor impedances, all conducted at varying gate and drain voltage levels. The aging and characterization platform consists of an acquisition and aging hardware system, an agile software architecture for experiment control and a collection of industry developed test equipment.*

Keywords *– prognostics, aging, characterization, damage progression, semiconductor test systems, degradation, electronics, remaining useful life, IGBT and MOSFET.*

I. INTRODUCTION

Generally, an understanding of intrinsic and extrinsic degradation mechanisms of component level devices is crucial for the adoption and application of health management to systems. Within the field of electronics, knowledge of semiconductor degradation under various system and environmental scenarios may be coupled with prognostic algorithms to predict future state and time–to–failure of semiconductor components.

The existence of measurable extrinsic degradation precursors, pertaining to device packaging, has been well established in literature for power transistor devices [1][2][3][4]. In recent literature intrinsic degradation precursors, related to the physical properties of the semiconductor, have also been observed [5][6][7]. However, it is not widely known how degradation mechanisms propagate as a function of environmental conditions and various stressors. The attainment of such knowledge is critical for advancements in the field of power electronics health management and prognostics. Therefore, the ability to perform large scale experiments on semiconductor devices for characterization of degradation precursors under various scenarios is of great interest. This paper presents the design of a transistor test platform that assists in the stimulation and characterization of such features. Additionally, the first phase of system implementation and its initial application to Insulated Gate Bipolar Transistors (IGBTs) in a thermal overstress scenario is presented.

Fault diagnosis has traditionally been applied to safety-critical mechanical systems or to those systems for which downtime leads to considerable financial loss. Typically, sensors monitor environmental and loading conditions in the application environment. Algorithms are then designed to extract information from the sensor readings, and compare them against a baseline to determine whether abnormal conditions exist and, if yes, what the root cause might be. While this technology has matured to some degree for mechanical and structural systems, what has been ignored until recently is that most of today's complex systems contain significant amount of electronics. There exists *a priori* reliability evidence that electronics may fail earlier than mechanical components.

In the aerospace domain, flight and ground crews require health state awareness and prediction technologies across all systems (including structures, propulsion, and various subsystems) that can accurately diagnose faults, anticipate failures, and predict remaining life. This includes those from avionics. Indeed, electronic components have an increasingly critical role in on-board, autonomous functions for vehicle controls, communications, navigation, radar systems, etc. Future aircraft systems, such as the electric aircraft or the Next Generation Air Traffic System (NGATS) will certainly

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rely on more electric and electronic components. The assumption of new functionality will also increase the number of electronics faults with perhaps unanticipated fault modes. In addition, the move toward lead-free electronics and microelectromechanical devices (MEMS) will further result in unknown behaviors. To improve aircraft reliability, assure in-flight performance, and reduce maintenance costs, it is therefore imperative to provide system health awareness for electronics. To that end, an understanding of the behavior of deteriorated components is needed to develop the capability to anticipate failures and predict the remaining life of embedded electronics.

II. FAULT MECHANISMS

The following is a brief review of common fault mechanisms prevalent in power transistors. It should be noted that many faults exist and this list is by no means exhaustive. Some major intrinsic faults, relevant to the transistor physics, include dielectric breakdown, hot carrier injection, and electromigration [8][9]. Some major extrinsic faults, relevant to the transistor packaging, include contact migration, wire lift, die solder degradation and package delamination [1][8].

Dielectric breakdown occurs when a strong electric field induces a current channel through a previously insulated medium. In FETs (Field Effect Transistor) this can be formed through the device's gate-emitter junction, gate-collector junction or, when the gate is off, across the drain-source junction. Acute dielectric breakdown is typically the result of electrostatic discharge (ESD) and junction over-voltage. Time Dependent Dielectric Breakdown (TDDB) refers to the break down of gate oxide caused by chronic defect accumulation in the SiO2 insulator during standard operation. For thick gate oxides, dominant in power transistors, this breakdown is the result of hole trapping and impact ionization. Theses are caused by high field strengths or caused by the "trap creation process" attributed to hydrogen-induced defect creation which occurs during normal operating conditions [10]. TDDB is shown to be advanced by increases in electric field strength [9]. It has also been observed that time-to-failure has logarithmic temperature dependence [10].

A strong electric field may impart energy into an electron or a hole which then becomes a so-called "hot carrier" due to the high kinetic energy [8]. Hot carriers have sufficient energy to tunnel and become trapped in gate oxide. These injected electrons and holes build up in insulator layers changing device characteristics such as the gate threshold voltage (V_{gth}) and transconductance (g_m). Hot carriers are a primary cause of TDDB and contribute to device failures under normal operating conditions.

Electromigration is a result of high current densities in silicon interconnects causing migration of metals. Formation of metal voids on interconnects can cause open circuits or high resistive paths, which in turn can result in poor performance or circuit malfunction [9]. A related mechanism, contact migration, forms metal voids between external contact metals and the silicon. As metal voids grow, the aluminum or other metals can diffuse down to the silicon. This in turn can cause metal spikes to form deep in the silicon region which results in shorting the p-n junctions [11].

Wire lift occurs when the bond between the package wires connecting to the silicon die fail and the wire "lifts" from the silicon. Wire lift is predominantly caused by thermal expansion mismatch between the bond solder and the attachment point, causing a thermo-mechanical cracking and bond failure. Wire lift has been identified as a dominant failure mode in high power IGBTs [1].

Die solder degradation is another prominent package related fault. Solder attaching the silicon die and package heatsink develop cracks and voids due to thermal expansion mismatch between materials during expansion and contraction [1][2]. These cracks increase the junction-case thermal impedance, contributing to increased internal operating temperatures. This creates a positive feedback loop, increasing the magnitude of temperature swing, in turn causing greater solder degradation. Package delamination occurs similarly, creating voids between case material and the silicon die [8].

III. ACCELERATED AGING METHODS

Thermal stress and electrical stress are the most common aging methodologies. Thermal cycling and chronic temperature overstress are prevalent thermal stress methods, with thermal cycling among the most prevalent accelerated aging methodology in electronics. Thermal cycling subjects devices to rapid changes in temperature differentials causing thermal expansion and contraction. Die solder degradation and wire lift are associated strongly with this aging method. Previous experiments on Metal-Oxide-Semiconductor FETs (MOSFETs) cycled 7000 times from -50^{o}C to 100^{o}C resulted in void formation in over 30% of the die solder attachment [4]. Similar results were demonstrated in IGBTs under power cycling with wire lift also occurring [1][2][3]. It should be noted that this effect is solder dependent, with lead-free packages showing better resistance to solder degradation [3]. Thermal overstress, another prevalent method, subjects devices to high temperatures for extended periods of time. TDDB is accelerated under high temperatures [10] and transistors have exhibited temperature dependant lifetimes accelerated by this mechanism [12]. IGBTs aged with self heating have shown changes in current ringing characteristics during switching [5].

Electrical overstress can be induced though transient and steady-state methods. Transient methods include electro static discharge (ESD), inductive switching and electromagnetic pulses. ESD is a leading cause of gate oxide failure [13] and hard switching of inductive loads, causes voltage spikes which can cause significant damage to drain-source junctions [14]. One can distinguish between thermally induced failure mechanisms (contact metal burnout, fused metallization), and electric field induced damage. Steady-state methods include chronic over-voltage and over-current. Applying high gate

voltages [6], setting gate voltage (V_g) to maximize drain current [7], and applying current overstress across the drain [15] have been shown to induce hot carrier and TBBD [10]. Fault precursors that could be monitored, amongst others, appear as collector-emitter leakage, gate leakage, changes in g_m and shifts in V_{gth}.

IV. SYSTEM REQUIREMENTS AND DESIGN CONSIDERATIONS

A. System requirements

This section describes the design and implementation of a system capable of performing accelerated aging tests, application simulations and device characterization on gate controlled power transistors to induce and analyze fault precursors. The proposed system should have the ability to act as test bed for the validation of prognostic algorithms for power transistors. System requirements relevant to these goals are:

1. Accommodate gate controlled power transistors by operating on standard and commercially available MOSFETs and IGBTs with currents capabilities ranging from 1A to 50A in typical 3 pin packages.
2. Accelerate aging of transistors, wherein electrical signals and environments can be carefully controlled to laboratory standards.
3. Simulate various application specific scenarios, including scenarios with extreme environmental conditions.
4. Measure and record electrical signals and environmental properties associated with test scenarios. In addition, the system must perform tests to extract transistors physical and electrical characteristics.
5. Have the ability to interface with prognostic algorithms such that real-time prognostics can be achieved.
6. Incorporate flexibility such that new instrumentation or software modules can be added with minimal effort. The system should be scalable, allowing multiple transistors to be tested in parallel. The software must be agile, such that new requirements can be incorporated without significant software redesign.
7. Perform aging and characterization tasks autonomously. User intervention should only be required to design, configure or initiate a test sequence.

B. Design considerations

Transistor Gate Hardware - Arbitrary signal generation is required over the full voltage range of a transistor gate for the support of robust scenario simulation and characterization. A review of industry datasheets yields rise and fall times on the order of 10ns and 50ns, for the specified class of MOSFETS and IGBTs. Gate voltages are limited to a 20V maximum for both transistors. A driver that exceeds this maximum would be useful for hot carrier injection and TDDB aging scenarios. Slew rates in excess of 2V/ns are desired for fast large signal swings. Gate capacitances for specified transistors are typically in the range of 500pF for MOSFETs and 6nF for IGBTs, requiring a powerful gate driver. The necessity for arbitrary signal generation at the transistor gate suggests the use of a linear amplifier. A driver bandwidth in excess of 100MHz is desired. Additional equipment with higher performance or special functionality may need access to the transistor gate. Therefore, the gate circuit should incorporate a switching mechanism between various instruments. A switching network for the electrical isolation of the gate should also be implemented where leakage or high voltages may cause problems.

Load and Power Supply Hardware - It is desirable to accommodate load currents from 10A up to 100A. Contacts and Printed Circuit Board (PCB) components must be rated for high amperages. Power supplies voltages should be programmable to accommodate dynamic scenarios. Power conditioning is desired to reduce interference from power supply feedback circuits or power cable inductance. Dynamic loads are desirable for the emulation of rich system scenarios.

Hardware Electrical Signal Acquisition - The transient response of voltage and current signals corresponding to the gate-emitter and the collector-emitter nodes should be measured in-situ. Transient acquisition rates greater than 1ns are desirable and bandwidths in excess of 300MHz are required to measure rise and fall times. PCB design must take transients into consideration. Overlap between collector and emitter traces should be minimized to reduce parasitic capacitance that may change transient characteristics. Traces should be kept very short or be impedance matched to prevent signal reflection. If possible, instrumentation amplifiers should be used for isolation and common mode rejection. Low-pass filtered transistor signals should also be measured. These averaged signals are especially important for SMPS (Switch Mode Power Supply) applications. Power management ICs (Integrated Circuits) in SMPS already implements voltage monitors, making them an ideal candidate for future prognostic implementations.

Hardware Thermal Environment - Controlling thermal environment is important for transistor characterization as their characteristics are heavily temperature dependant. Datasheets reveal V_{gth} shifts on the order of -10mV/°C. Collector-emitter resistances will often change by an order of magnitude over a 100°C differential. Such shifts must not be attributed to changes in the intrinsic characteristics of the transistor. In addition, aging and simulation scenarios involve extreme environmental conditions. The system should allow temperatures ranging from far below 0°C to above 300°C, where IGBTs have shown short-term operability [5]. Internal junction temperature measurements, often measured using V_{gth}, can be problematic as hot carrier effect also acts on V_{gth}. Special effort should be taken to measure silicon die, package epoxy and package heat sink temperatures using thermal methods, in order to enable accurate temperature control and thermal impedance degradation measurements.

Software Control and Data Acquisition - The chosen software development environment must support

communication with multiple hardware devices, act as an in-the-loop feedback controller, and save gigabytes of data collected over long test runs. The test software must perform a multitude of different experiments related to scenario generation and transistor characteristics. It should interact easily with the user and display results in real-time.

Software Architecture - The software framework controlling the system should enable a dynamic and scalable development environment. Scientific software development is usually iterative [16], where results dictate new and novel experiments. Equipment upgrades will require system adaptation. A thorough consideration of software engineering principles is crucial to the development of a successful software package.

V. IMPLEMENTATION

System Implementation has been broken into several stages to manage project complexity. The system implementation consists of a set of commercially available instrumentation attached to a custom built hardware system under the control of an agile software framework developed in LabVIEW.

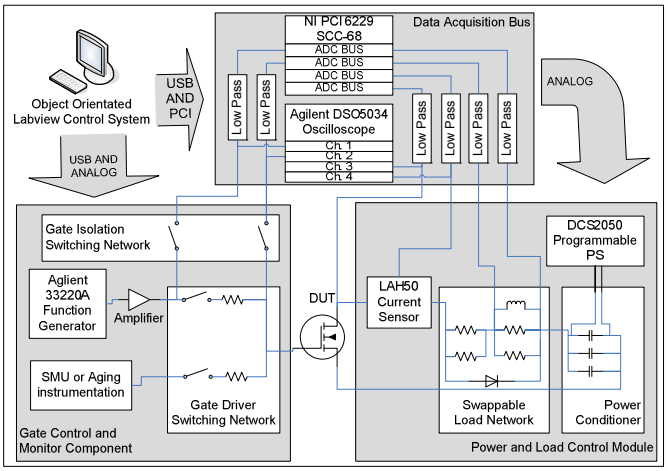

Figure 1: Overview of the electrical system.

A. Commercial Instrumentation

The industrial hardware consists of a 300MHz Agilent DSO5034A oscilloscope with a 1ns sample rate and 1Mpts memory for large transient acquisition, a 20 MHz Agilent 33220A function generator for gate signal control, a National Instruments PCI-6229 data acquisition card with a SCC-68 breakout containing three SCC-TC02 thermocouple measurement modules and one SCC-RTD01 resistance temperature detector, a DCS2050A analog programmable power supply capable of sourcing 20V and 50A, three thermocouple modules, a Raytek RACI3A infrared sensor, a Tenney T5STR environmental chamber capable of temperature, humidity and pressure control, and a computer running LabVIEW and Matlab.

B. Transistor Test Board

Custom hardware was developed to compliment the commercial instrumentation and serve as the physical test bed for the transistor under test. This hardware includes a primary test board with a built in 200KHz current sensor with a 100A maximum current, an infrared temperature sensor port, BNC transient output ports connected to the DSO5024A oscilloscope, and a bank of 30Hz low-pass filtered output ports connected to the PCI-6229 data acquisition card. An onboard gate driver switching network allows for the in-situ swapping of two separate gate signal sources. A gate isolation switching network is also implemented to remove unnecessary instrumentation when performing current leakage measurements or tests involving high voltage.

C. Power conditioner and Load Board

A power conditioner and load board was also constructed. It includes a power conditioning stage with three parallel capacitors with staggered capacitance values of 120mF, 4700uF and 47uF. This filtering system removes cable inductance and power supply interference from most transient measurements. The board also provides a two port swappable load network, allowing 3 parallel loads across node 1 and two parallel loads across node 2. A freewheeling diode port is also provided. Board voltages are low pass filtered and acquired by the PCI-6229.

D. Gate Driver Board

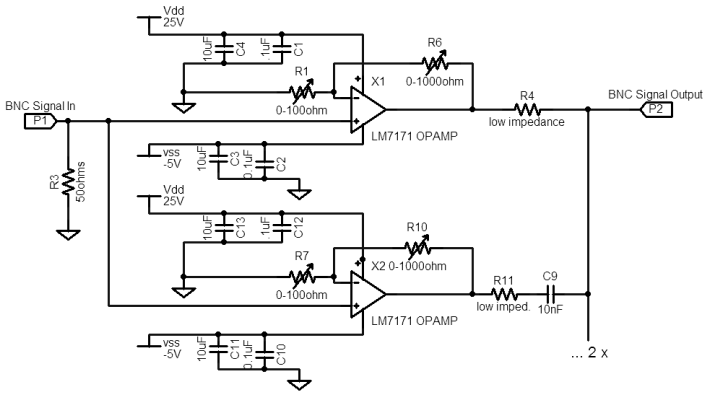

Figure 2: Schematic for the linear gate driver with only one of three capacitively coupled operational amplifiers displayed.

The gate driver board consists of four parallel LM7171 linear voltage feedback operational amplifiers (op-amps) operating in a non-inverting configuration with input coupled to an Agilent 33220A waveform generator. The gate driver board has an approximate bandwidth of 100MHz, rail to rail voltages from -2V to 23V and can achieve slew rates of 0.5V/ns into a 50Ω load. The design of the driver, shown in Figure 2, consists of a single op-amp directly connected to the driver board output for DC operation and three additional op-amps capacitively coupled to the driver board output to

assist in driving the largely capacitive loads associated with power transistor gates. The capacitive coupling prevents damage to op-amps in the event of gain mismatch during steady-state operation. The driver board additionally contains adjustable feedback resistors used in gain calibration to ensure stable operation.

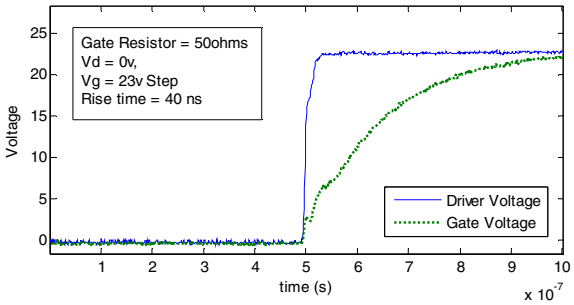

Figure 3: Large signal step response of the gate driver into the IGBT gate.

Figure 3 show a 23V step through a 50Ω resistor across the gate of an IGBT. Rise time is 40ns. Figure 4 shows an impedance test of an IGBT gate. A 0.25V RMS sine wave is coupled with a 5V DC bias. Voltage is measured with an ac coupled oscilloscope across a 50Ω resistor connected in series with the gate.

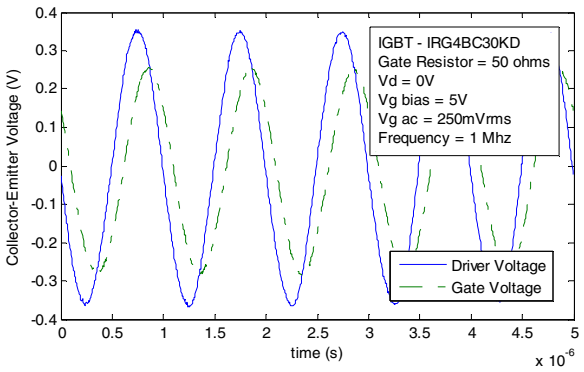

Figure 4: Small Signal response of the IGBT gate used for impedance characterization.

E. Thermal Test System

A custom thermal control unit is also under development to attach thermocouples to fixed positions on the transistor package and utilize a Peltier unit capable of 60°C temperature swings in both negative and positive directions for use in rapid thermal cycling. The Peltier unit is driven by a 15A linear amplifier and attached to a large heat sink for that acts as a reservoir for heat dissipation. An infrared sensor is also included for applications requiring contactless measurements, though infrared sensors have exhibited large temperature errors in our applications due to emissivity and beam localization considerations.

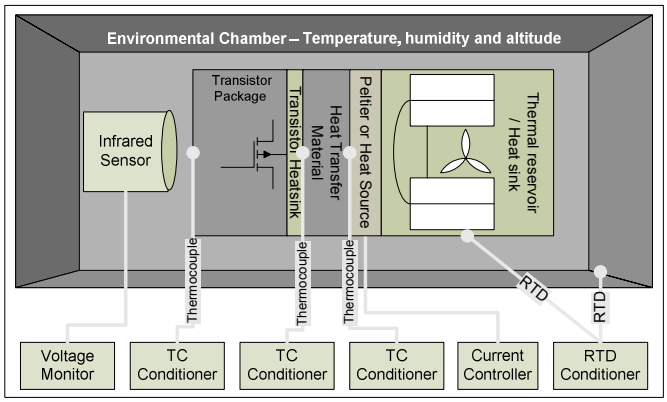

Figure 5: Overview of the thermal test system.

F. Agile Software Framework

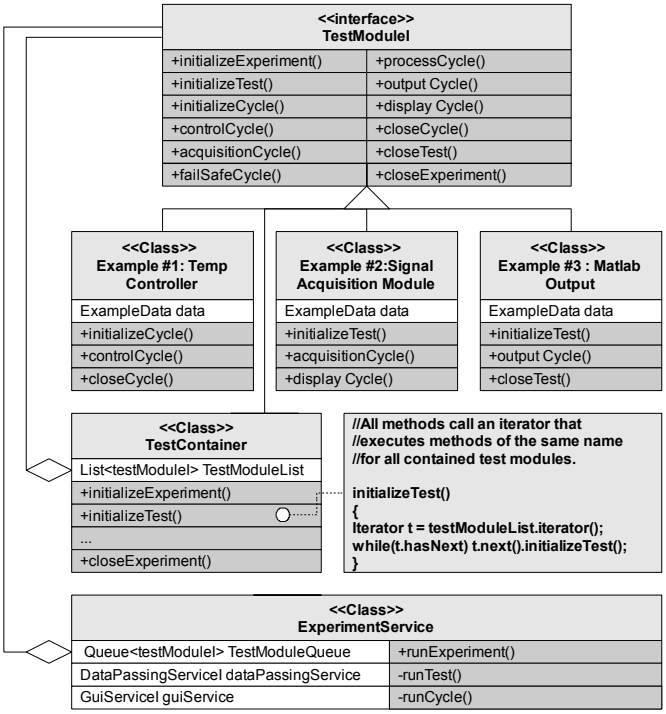

Figure 6: Class relation diagram for core experiment components.

An agile software architecture has been developed for use as a framework in the coding and execution of tests and experiments. It employs object oriented programming, makes heavy use of design patterns, and supports the agile coding methodology [17], valuable to the iterative development found in scientific programming [16]. Such methodologies enable flexibility in system design and allows for adaptation to changing requirements. The framework was implemented in the LabVIEW development environment, though the design is portable to most object oriented languages. It embodies an experiment execution package, a test builder package, several graphical user interface (GUI) services and an assortment of miscellaneous classes. This paper describes only the core framework, consisting of those services relevant to the execution of an experiment. This core consists of

components shown in Figure 6. These include the test module interface, the test container class, the experiment service, and concrete implementations of the test module interface.

The experiment service is responsible for the overall execution of the experiment. It contains a queue of test containers or modules, a data passing service, and a GUI service. All such services and modules are coded using interfaces (also referred to as virtual classes or dynamic VIs) rather than concrete classes. The use of interfaces in the design has a subtle but far reaching impact. The experiment service is not bound to any specific test, so it may run any class implementing the test module interface. The data passing service, responsible for passing data between objects, can be as simple as an array or provide an interface to a SQL server when data is large or reliability is paramount. The GUI service can be changed as needed without breaking the underlying process. All of these objects can be swapped at runtime and can be applied without breaking code in other modules. This design structure embodies elements of both the *strategy pattern* and the *template method pattern* [18].

The experiment service is started via the runExperiment() method. Tests objects placed on its queue are executed in series as shown in Figure 7.

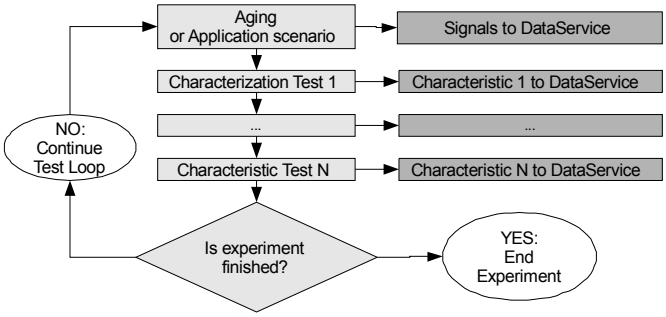

Figure 7: A flow diagram representing a typical experiment.

Data are communicated between different test modules and the experiment service using a data passing object. Once the test queue is iterated, the experiment will either end, or loop for another round of testing, depending on state flags present in the data passing service. Individual tests are executed by passing the test object to the runTest() method. A test module has an initialization method, a sequence of cycle methods called at each time step, and a closing method called at the end as shown in Figure 8.

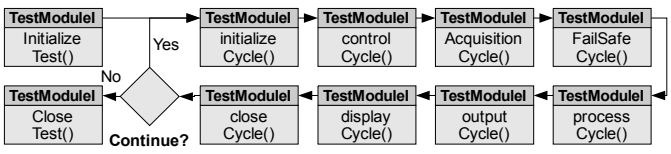

Figure 8: Flow diagram of Experiment.runTest() template method.

A test object, which defines a test, is constructed by placing a set of test modules into a test container as shown in Figure 9. The Concrete test module class usually implements some discrete functionality such as control logic, data processing or signal display. When many test modules are coupled together into a test container they define a complete test object.

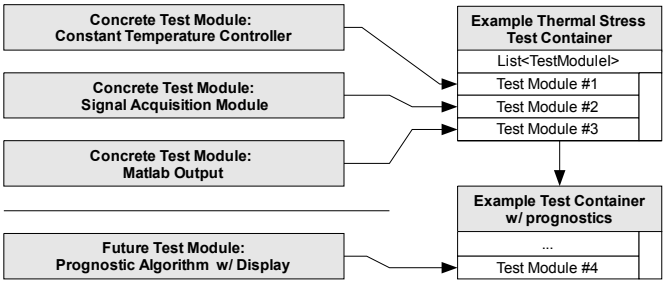

Figure 9: Construction of an example test object which can be extended to include prognostic algorithms as they become available.

Using this design, many different tests can be constructed using the same base module classes. The Test object functionality can also be easily extended with additional test modules. Similar to the experiment class, this component orientated approach allows for test construction and modification during runtime. All test container methods delegate method calls to those methods of the same name in contained test modules, as noted in the code snippet on Figure 6. It is worth discussing that a test container is also a test module. Complex test containers may have an object hierarchy several layers deep forming a multi-node tree, the order of leaf method execution is dictated by a preorder traversal sequence. A call to a method within a test container iterates through all children test modules' methods in series, but when run in a sequence, as shown in Figure 8, they are considered to run in pseudo-parallel, similar to procedural coding. This deterministic execution has some advantages over true parallelism, as one avoids challenges associated with multi-threading and race conditions.

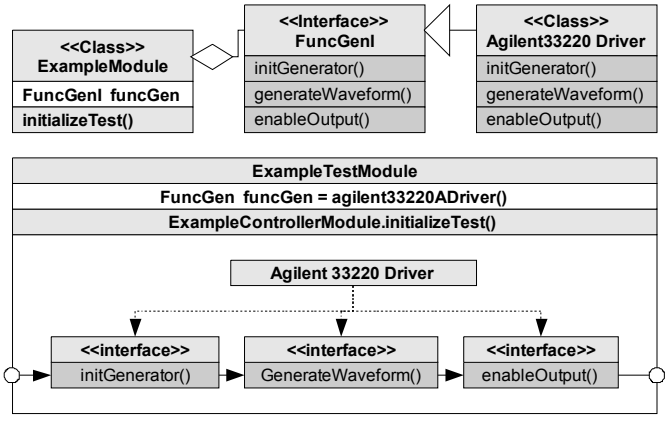

Figure 10: An example test module utilizing the strategy pattern to assign device drivers dynamically.

Concrete test modules, which implement discrete functionality, also utilize the *strategy pattern*. Test logic for experiment control is constructed using generic device interfaces, rather than vendor specific device drivers. At

runtime, any device driver that implements the respective interface can be passed into the module. Methods will be called from the implementing class, rather than the generic interface. Most drivers can be wrapped in an *adapter* [18], allowing a great deal of compatibility. An example of this pattern is shown in Figure 10. This pattern enables separation of test logic from vendor specific equipment, limiting dependency on aging legacy devices and poorly performing instrumentation and can encourage software collaboration between researchers.

G. Custom aging and characterization test software

Two test objects have been thoroughly developed in the LabVIEW development environment and others are under refinement. The first test object performs a thermal degradation scenario which self-heats a transistor to a specified temperature and holds it within a temperature boundary by gate switching. All transient, thermal and steady-state signals are acquired and recorded. In the event of a failure, the experiment is ended quickly to preserve the transistor. The second test object performs thermal impedance characterization of transistor package. Transistors are self-heated to a constant temperature with a known power setting. The transistor is then switched OFF, and its temperature decay is measured and thermal impedance shifts extracted. Additional aging software under refinement performs thermal cycling, injects hot carriers and induces electrical overstress. Additional characterization software under refinement measures gate impedance, perform pulsed I-V curve measurements and extracts switching characteristics.

VI. IGBT THERMAL OVERSTRESS EXPERIMENT

Preliminary thermal overstress tests were conducted on IGBTs during system development. An International Rectifier IRG4BC30KD IGBT with a 600V/15A current rating in a TO220 package was attached to the transistor test board with no external heatsink. The collector-emitter junction was connected in series with a load power supply and a 0.2Ω load resistor. A 50Ω resistor was placed between the gate driver and the IGBT gate for current measurement. A thermocouple was attached to the IGBT case for temperature measurement. The gate signal was chosen to be a Pulse Width Modulated (PWM) signal with amplitude of 10V, a frequency of 10 KHz and a duty cycle of 40%, similar to a slow SMPS. A hysteresis temperature controller with set points of 329°C and 330°C was connected to the system, switching the gate voltage for its control mechanism. The load power supply voltage was increased from 0V to 4V over the course of several minutes until the heat sink temperature reached 330°C and the temperature controller began cycling. An additional temperature threshold controller, with a set point of 340°C, was programmed to turn off the load power supply and end the experiment in the event of thermal runaway and latching failures. IGBTs tested with this process were found to fail early in the test, within the first several minutes, or survived 1 to 4 hours before loss of gate control and thermal runaway was observed.

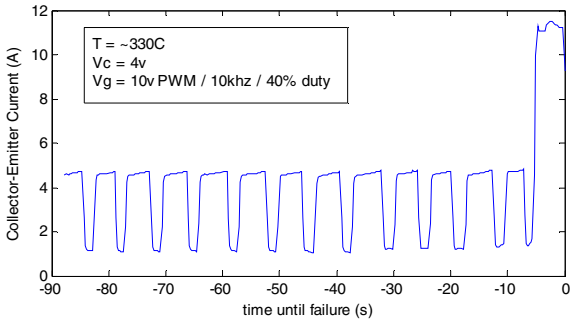

Figure 11: Latch up failure of an IGBT during thermal overstress.

Figure 11 shows the averaged collector-emitter current during a failure. The average ON-state current increases from approximately 4A to 10A indicating a transition from a 40% PWM duty cycle to a latched ON-state, resulting from a loss of gate control. This behavior may be attributed to the temperature-stimulated parasitic Silicon Control Rectifier (SCR) found within the IGBT. The experiment was ended quickly after the failure and the IGBT was found to be functional when returned to room temperature of 24°C. Characteristics of the degraded IGBT are currently being examined.

Both steady state and transient switching signals recorded during the test were analyzed. Steady-state voltages and currents showed minimal change throughout the test. Transient gate voltage and current also remained constant. Changes to collector-emitter voltage transient characteristics during turn-ON were also minimal. The collector-emitter current characteristics were not collected during this stage of development.

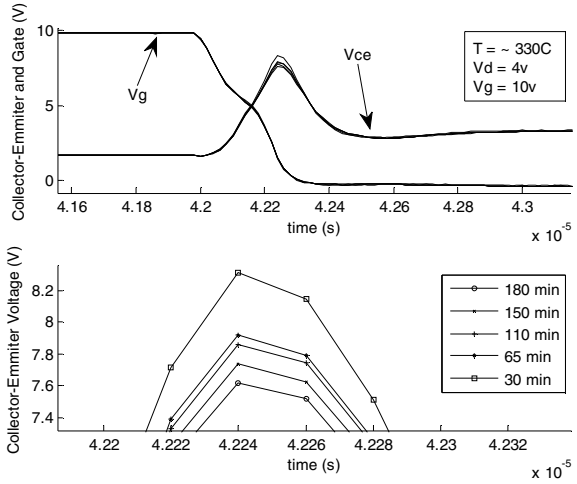

Figure 12: a) A voltage transient is generated across the collector-emitter junction. This peak decreases as the device degrades. b) A close-up of the transient peak.

A strong degradation indicator was observed when viewing the collector-emitter voltage turn-OFF transient. The peak voltage of this transient decreased significantly with both

increases in temperature and thermal overstress degradation. Figure 12 displays the switching transient voltage, measured near 330°C, at different degradation stages.

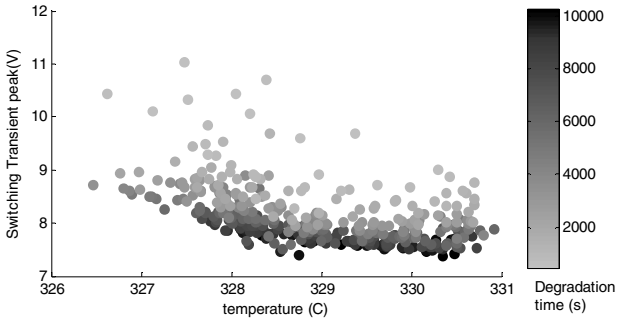

Figure 13: A scatter plot of the package temperature vs. switching transient peak voltage for a single IGBT under degradation.

Figure 13 shows a scatter plot of transient peak voltage versus heatsink temperature with grayscale indicating aging state. A degradation trend can be clearly seen with transient peaks in similar temperature ranges decreasing over 10% during the course of the experiment. An indicator of semiconductor degradation under severe conditions is clearly observed. The root-cause is of course in question. This indicator could be intrinsic degradation; however, a more likely cause is thermal impedance degradation of the package causing increases in internal temperatures. Further investigation of this failure precursor's cause is planned.

VII. FUTURE CONSIDERATIONS AND CONCLUSION

The design and initial implementation of an accelerated aging, scenario simulation and characterization system has been presented. A successful preliminary investigation of in-situ degradation indicators using the system has also been demonstrated, wherein thermal overstress of an IGBT caused shifts in the peaks of switch-OFF voltage transient.

Future work will consider the expansion of the system for testing multiple transistor in parallel, adding an on-board system controller, the addition of a microcontroller based gate signal generator and switch controller, addition of an impedance matched multiplexing board to scale oscilloscope applicability, adding instrumentation amplifiers to board signals for increased signal isolation, addition of high-voltage switches for damage prevention during IGBT collector overstress and leakage tests, addition of source measurement units for leakage current and threshold voltage measurement, and addition of a switching network to allow multiple loads to the main board.

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