A new generation of high voltage MOSFETs breaks the limit line of silicon

G. Deboy, M. März, J.-P. Stengl, H. Strack, J. Tihanyi and H. Weber
Siemens AG, Semiconductor Division, Balanstr. 73, 81541 München, Germany

Abstract

For the first time a new device concept for high voltage power devices has been realized in silicon. Our 600 V-COOLMOS™ reaches an area specific on-resistance of typically 3.5 Ω·mm^2. Our technology thus offers a shrink factor of 5 versus the actual state of the art in power MOSFETs. The device concept is based on charge compensation in the drift region of the transistor (1-3). We increase the doping of the vertical drift region roughly by one order of magnitude and counterbalance this additional charge by the implementation of fine structured columns of the opposite doping type. The blocking voltage of the transistor remains thus unaltered. The charge compensating columns do not contribute to the current conduction during the turn-on state. Nevertheless the drastically increased doping of the drift region allows the above mentioned reduction of the on-resistance.

Basic principle

The most important contribution to the on-resistance of high voltage MOSFETs arises from the epitaxial drift region. Fig. 1 shows a cross section of a standard 600 V-power MOSFET.

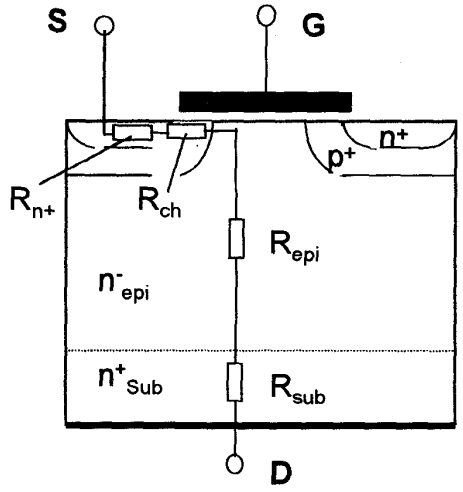

Fig. 1: State of the art–600 V-MOSFET (RDS_{on}·A≈18 Ω·mm²): Typical values of the individual series resistances are: R_{n+}: 0.5%, R_{ch}: 2%, R_{epi}: 97%, R_{sub}: 0.5%.

A high blocking voltage V_{br} of the transistor requires a relative thick and low doped epitaxial layer leading to the well known law $RDS_{on} \approx V_{br}^{2.4-2.6}$(4). This limitation can be overcome if columns of the opposite doping type are implemented into the drift region in a way that the doping integral along a line perpendicular to the current flow remains smaller than the material specific breakthrough charge, which is for silicon about $2 \cdot 10^{12}$ cm^{-2} (see Fig. 2).

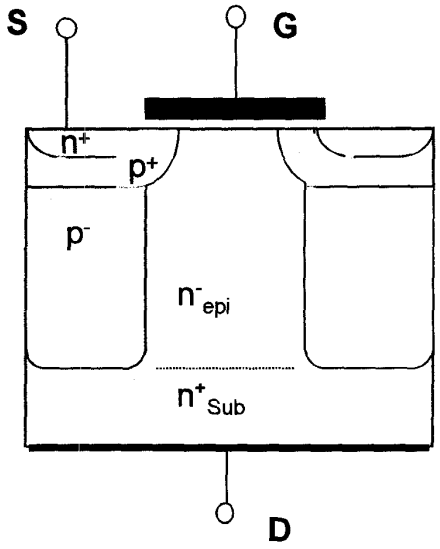

Fig. 2: Cross section of a 600 V-COOLMOS™.

Thus the doping of the current conducting n-regions can be enhanced inverse proportional to their width (5,6). The electric field inside the structure is fixed by the net charge of the two opposite doped columns. Thus a nearly horizontal field distribution can be achieved if both regions counterbalance each other perfectly. For higher blocking voltages only the depth of the columns has to be increased without the necessity to alter the doping. This leads to a linear relationship between blocking voltage and on-resistance (see Fig. 3). Using this technique our 1000 V COOLMOS™ will offer a RDS_{on}-reduction in the range of one order of magnitude versus conventional technologies.

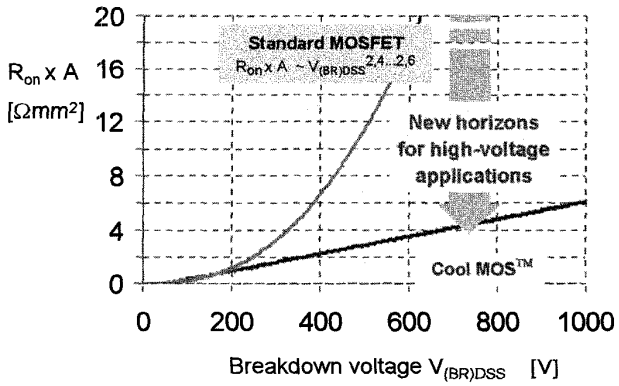

Fig. 3: COOLMOS™ technology offers a linear relationship between blocking voltage and on-resistance.

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Technology

The devices are manufactured by multiple deposition of epitaxial layers and subsequent implantation steps on a highly doped n^+-substrate. We used masked boron and phosphor implantations on undoped epitaxy, masked boron and unmasked phosphor implantations on undoped epitaxy, masked phosphor and unmasked boron implantations on undoped epitaxy and masked boron implantaions on n-doped epitaxy. The device termination has to be optimized individually for each technology version. A diffusion process is subsequently used to form vertically coherent p- and n-columns. The cell pitch is adjusted to the structure in a way that each p-column is connected by a p-well and a contact hole within the active device area.

Device performance

The internal structure of the new MOSFET generation has a strong impact on the device behaviour. In the blocking state the space charge layer expands from the p^+-well to the n^+-substrate. As the p- and n-columns are connected to the p-well and n^+-substrate, respectively, the space charge is removed in the same way as in a standard MOSFET, that is by the electron drift current and by diffusion of holes. If the space charge in some part of the p-column is not entirely removed, the device will not turn on properly due to the formation of a lateral JFET effect.

During turn off the space charge layer starts to expand along the lateral pn-junctions, which form a large internal surface; therefore at low voltages a very large drain-source capacitance is observed. This capacitance drops to extremely low values as soon as the space charge layer has spread over the whole columns (see Fig. 4).

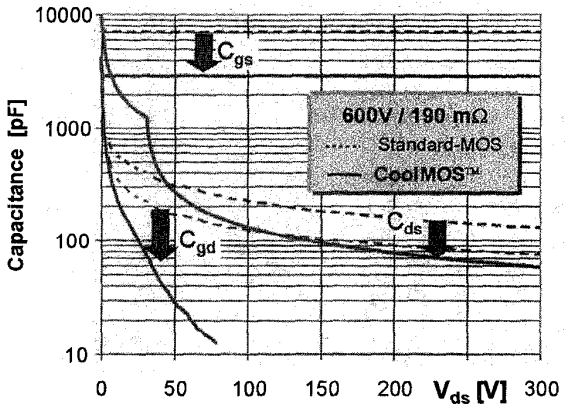

Fig. 4: COOLMOS™ offers a substantial reduction of gate-source and Miller capacitance, C_{gs} and C_{gd} respectively, as well as a very favourable nonlinear behaviour of the drain-source capacitance C_{ds}.

The energy E_{oss}

$$E_{oss} = \int_0^{Uds.max} C_{oss}(U) \cdot U \cdot dU$$

stored in the output capacitance C_{oss}

$$C_{oss} = C_{DS} + C_{GD}$$

during switching is thus substantially lower than in conventional MOSFETs with equal chip area. The extreme nonlinear characteristic of the output capacitance leads to a very favourable switching behaviour: during turn-off an external current driven by parasitic stray inductances loads the output capacitance instead of forcing this current through the channel of the transistor. The miller plateau can be run through in a drastically reduced time. During turn on the stored energy E_{oss} is converted into heat and adds to the overall switching losses of the device. It is therefore of primary importance to keep this energy very small. COOLMOS™ improves this term by a factor of two versus the state of the art as shown in Fig. 5. Due to the drastically improved area specific RDS_{on} our technology also offers a substantially reduced Miller capacitance C_{rss} and input capacitance C_{iss}, which leads to a very small gate charge. Typical characteristics for all device capacitances are plotted in Fig. 4, whereas Fig. 5 shows a comparison of the output energy stored in a COOLMOS™ versus different standard MOSFETs.

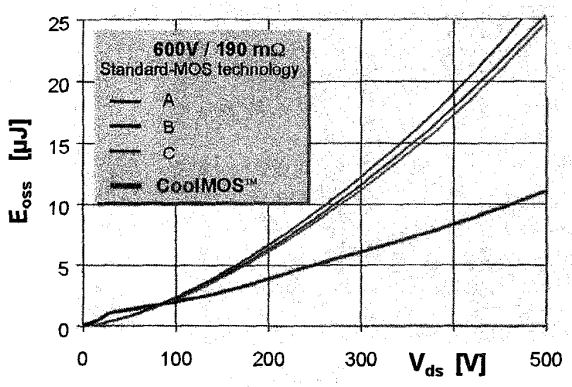

Fig. 5: COOLMOS™ cuts the energy stored in the output capacitance C_{oss} by a factor of two versus state of the art MOSFETs.

The switching behaviour of COOLMOS™ is absolutely like a MOSFET. There is no bipolar component like the well known tail current in IGBTs. The mobile carriers stored in the adherent columns are swept out at very low voltages without carrier flow through the space charge layer. Combined with very low internal capacitances the dynamic losses can be reduced to an hitherto unknown extent.

Device ruggedness

From the customers viewpoint device ruggedness is an essential criterion. COOLMOS™ transistors offer an avalanche energy per chip area which is very close to the thermal limit of zener clamped devices. We used a self aligned spacer technology to reduce the base length of the DMOS-inherent parasitic bipolar structure to the outermost extent. Thus no latch-up phenomena will occur within the specified safe operating area of the transistor. Fig. 6 shows experimental results of our best-in class-transistor offering a resistance of 190 mΩ in the TO220-package. The device is

driven with an unclamped inductive load at its nominal current.

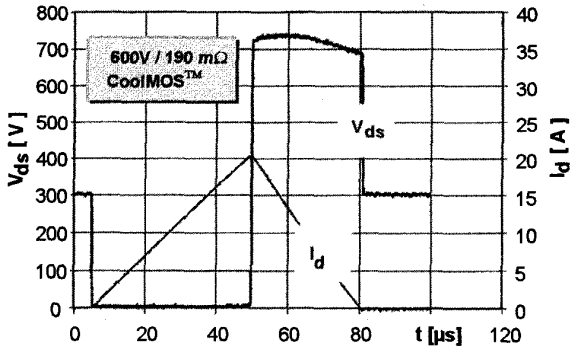

Fig. 6: COOLMOS™ shows an avalanche ruggedness close to the thermal limit of zener clamped devices.

Due to the enormous shrink potential offered by COOLMOS™ special attention has to be paid to high current density effects. For the replacement of a state of the art transistor with a given RDS_{on} and nominal current we recommend a transistor with a five times smaller chip area. Our device has therefore to cope with a corresponding higher current density. As the shrink potential of our technology, however, scales at the same factor as the doping of the n-regions (and respectively the conductivity of the drift region, which is the main contribution to the on-resistance) the ratio between current density and effective doping is not altered. The current capability therefore increases linearly with the conductivity gain. However, a very fine cell pitch, chosen to supply each p-column of the internal structure with a transistor cell, results in a significantly increased total channel width of the device. Measures has therefore to be taken to limit the short circuit current to a reasonable level.

Fig. 7 shows our 190 mΩ-transistor (TO220 package) in an application as a serial switch for a 220 V AC power supply. During short circuit the current reaches a maximum of more than 100 A. This current exceeds the rated nominal current and thus the specified safe operating area (SOA) by more than a factor 5. Nevertheless the device can be turned off safely within a period of 10 µs, which is sufficient for an over current detection. Our COOLMOS™ technology is specified with full SOA range as rated in conventional state of the art transistors.

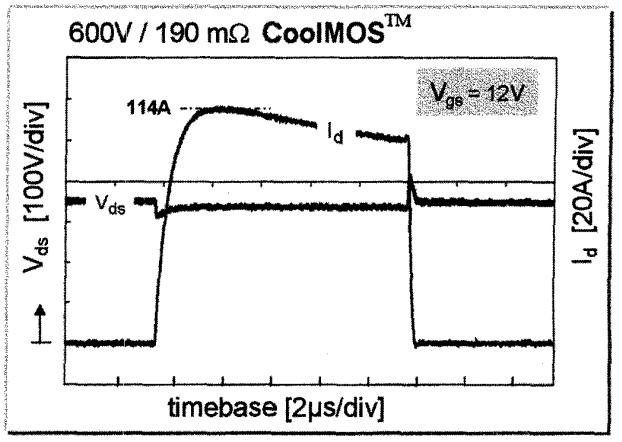

Fig. 7: COOLMOS™ offers short circuit ruggedness and the full safe operating area known from standard MOSFETs.

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