Comprehensive Parametric Analyses of Thermally Aged Power MOSFETs for Failure Precursor Identification and Lifetime Estimation Based on Gate Threshold Voltage

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***Abstract*— Thermal/power cycles are widely acknowledged methods to accelerate the package related extrinsic failures. Many studies have focused on particular failure precursor at a time and continuously monitored it using custom-built circuits. Due to the difficulties in taking sensitive measurements, the reported findings are more on the quantities requiring less sensitive measurements such as on-state resistance. In this paper, a custom-designed test bed is used to age a number of power MOSFETs and an automated curve tracer is utilized to capture parametric variations in I-V curves, transfer capacitances and gate charges at certain time intervals throughout the aging. The results suggest that the failure precursors which exhibit continuously increasing trend are the on-state resistance, body diode voltage drop, parasitic capacitances and threshold voltage. Based on the results, an exponential empirical model for the gate threshold voltage that fits successfully with the experimental data is proposed. Furthermore, Kalman Filter is employed to filter out the measurement noise and model uncertainties, which is also used to estimate the remaining useful lifetime of the degraded switches.**

Keywords—failure diagnosis, power MOSFET, on-state resistance, gate threshold voltage, health monitoring, remaining useful lifetime.

I. INTRODUCTION

Reliability of power semiconductor devices is of great importance particularly for mission critical systems, and has been exhaustively investigated in recent literature [1]-[7]. Researchers have focused on the identification of failure precursors that can be evaluated to engage on protective circuitry, prevent costly shutdowns, and bring down maintenance costs. To accelerate the time duration of the reliability tests, custom test-beds that are capable of applying thermal/power cycling have been designed [4],[6]-[8]. Auxiliary circuits are employed to continuously monitor the failure precursors. Majority of the work has been devoted to the reliability of IGBT modules where multiple active chips are paralleled through multiple bond-wires [1],[3]-[5],[7]. The reported findings in the literature are; variations in saturation voltage [4],[6],[9], thermal impedance [10], turn off time [11], change in phase and amplitude of ringing during turn-off [12], input, output and reverse transfer capacitances [3], threshold voltage [6], [14]. On the other hand, a few studies have investigated the failure precursors observed in power MOSFETs [8], [15]-[17]. The failure precursors identified for power MOSFETs are the on state-resistance and gate threshold voltage.

Although some of the failure precursors of thermal aging have been identified in literature, the effects on the MOSFET's current/voltage characteristics have not been fully explored comprehensively in a single study. One important reason is the necessity of high resolution source and measurement units for these tests. For instance, the gate current or drain-source leakage currents are in the order of several pA which can easily be interfered by the noise present in the circuit, if the measurement interface board is not well designed.

In this work, 400V/11A power MOSFETs are thermally aged on a custom-designed test-bed presented in [8]. It is aimed to stress the gate oxide and solder joints by applying thermal cycle. At certain time intervals (50 or 200 thermal cycles), the switches are removed from the test-bed and placed on the Keysight B1506A automated curve tracer as shown in Fig. 1. The following parameters are analyzed in this work; 1) threshold voltage, 2) breakdown voltage, 3) leakage current, 4) body diode avalanche voltage, 5) gate charge, 6) parasitic capacitances, 7) on-state resistance, 8) body diode voltage drop. In earlier studies, on-state resistance variation has been continuously monitored and identified as a failure precursor and evaluated to estimate the remaining useful lifetime [17]. In this study, all parametric changes in the thermally aged power switches are investigated based on the data collected in the laboratory environment. Furthermore, as a result of the findings, the threshold voltage is identified as a feasible failure precursor that increases consistently throughout aging, which can be used to assess the state of health of the switches.

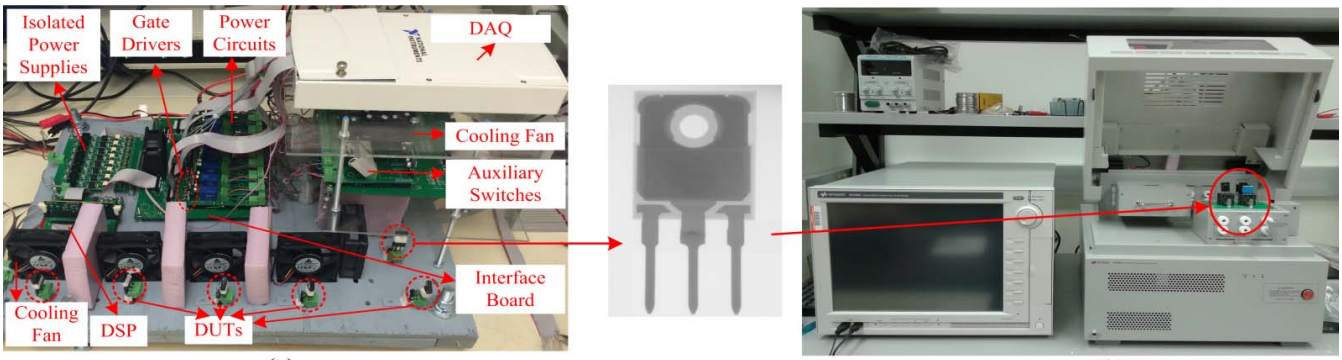


Fig. 1. Illustration of the test-bed; (a) custom designed aging setup, (b) curve tracer.

Based on the experimental data, an empirical model in the form of an exponential function is established and Kalman Filter (KF) is used to filter out the noise and deal with the model uncertainties.

II. Parametric Analysis of Thermally Aged Power MOSFETs

The conducted thermal aging tests intend to cycle the power MOSFETs with a junction temperature swing between 40°C and 180°C, at a constant drain current of 5.2A, where rated continuous drain current of the switch at room temperature is 11A. At every 200 thermal cycles, the devices are removed from the setup shown in Fig. 1(a), and then plugged into the curve tracer for parametric analyses, as shown in Fig. 1(b). The tests have been performed on multiple samples, but only results of two samples that can represent the general behavior of the power MOSFETs have been shown here. There are two failure modes observed during the tests. Most commonly, the gate control was lost. Secondly, the drain-source terminal was shorted. Basically, there are three package related degradation mechanisms taking place in a semiconductor power device.

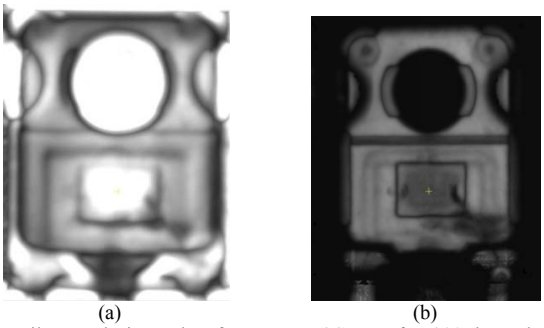
The first degradation mechanism is the aluminum reconstruction, which happens at relatively high junction temperatures. The thermal cycles at high temperatures result in tensile stresses on the upper metallization layer due to mismatch of the coefficients of the thermal expansions (CTE) of Al (22.2) and Si (3), where unit of CTE is $10^{-6}m/(mK)$. This induced stress can be much higher than the elastic limit, which results in extrusion of the aluminum grains at the grain boundaries. This causes the sheet resistance to increase, which increases the on-state resistance measured between drain to source terminals, and also degrades the gate-oxide layer as the increased sheet resistance of a cell increases the current densities at adjacent cells [18].

Another degradation/damage is typically observed at the wire-bonds. Being close to the active Si chip area, particularly the bond pad is exposed to the full thermal swing under power cycling. In addition, due to the skin effect becoming more dominant at higher switching frequencies, the current distribution or in other words power dissipation is not homogeneous. Most commonly, a crack is forming up at the tail of the bond, which then propagates towards the Al surface where the bond-wire gradually lifts off [18]. The root of this failure is again mismatch of the CTE between Al and Si. Bond-wires experience thermal swings larger than the ones experienced by the die.

Thirdly, the solder joint between Cu base plate and Direct Bounded Copper (DBC) substrate degrades with respect to thermal swings. Typically, the solder material is lead-tin alloy bonded to the base copper plate with large lateral dimension. When this interface experiences thermal cycles, the cracks are formed at the border of the joint on the copper plate side as maximum shear stress occurs at the border [18]-[19]. The degradation on this layer affects the thermal impedance as heat flow within the device is from Si to the base plate.

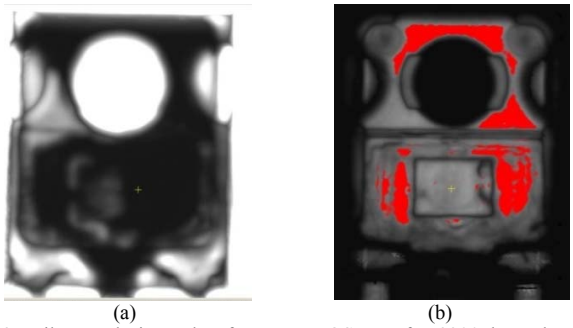
The DBC layer mostly helps reducing the shear stress on the die attach solder as CTE of DBC ranges from 4 to 7.1 while it is 3 for Si. However, DBC layer is not preferred in discrete packages due its high cost. Moreover, isolation between base plate and drain/source plate is not required in discrete switches. When die is attached to a Cu base plate, the CTE mismatch of die and base plate becomes considerably large with relatively larger lateral dimension in comparison to bond-wires. In addition, the thermal time constant of a discrete package is significantly less than that of the power module. Because of this reason, it is likely that die attach solder joint degrades in discrete packages at lower frequencies faster than the bond-wires. Die attach degradation increases both the electrical resistance and thermal impedance.

In accelerated tests, these three failure mechanisms occur simultaneously. Some studies have also tried to trigger only one type of failure. For instance, in the bond-wire failure tests, the time duration of the applied thermal swing is less than a couple of seconds with a maximum junction temperature not exceeding 110°C, where the switches are driven with PWM under rated load. The purpose is to only increase the junction temperature through heat generated as a result of power loss, but meantime not heating the case temperature too much so that solder joints or DCB substrate do not experience significant temperature swing. This type of test reflects a real condition where the operation frequency is higher than 1-10Hz



(a) (b)

Fig. 2. Failure analysis results of a power MOSFET after 300 thermal cycles; (a) T-SAM, (b) C-SAM.



(a) (b)

Fig. 3. Failure analysis results of a power MOSFET after 3300 thermal cycles; (a) T-SAM, (b) C-SAM.

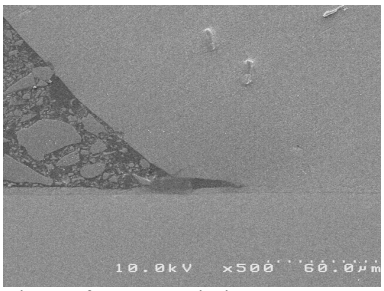


Fig. 4. Bond wire image after cross-sectioning.

and it is more suitable for power modules where there is a significant thermal capacity difference between the die and DBC substrate. In discrete packages, it is more likely to observe die attach degradation under 60Hz as CTE mismatch of Cu and Si is large, the lateral dimension of die attach is larger than bond-pad, and thermal time constants of a discrete device is much smaller than power modules.

In our custom-designed test bed, the devices are actively heated without attaching a heat-sink and cooled down by forced air-cooling through fans. Thus, the junction temperature is increased up to very high degrees (180°C which triggers all three failure mechanisms. Yet, as pointed out earlier, the large thermal swings together with long relaxation and heating times in fact stress the die attach solder joints, and gate oxide more than the bond-wires due to the larger lateral dimensions. In our tests, one thermal cycle lasts for approximately one minute (20 sec heating, 40 sec cooling). Thus, we observed the consequences of these two aging mechanisms before there was any damage on the bond-wires.

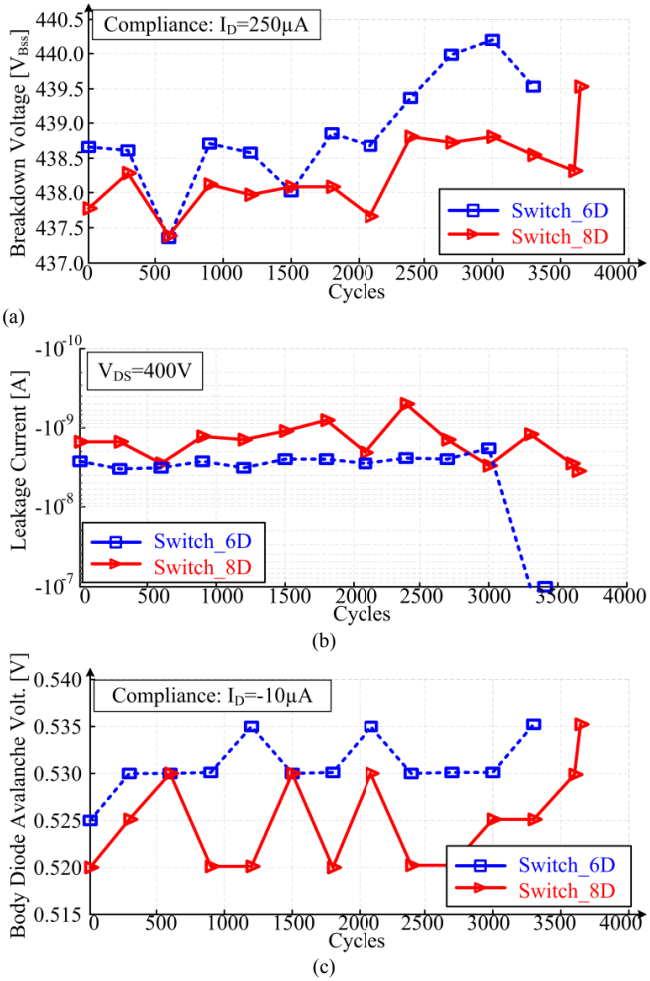
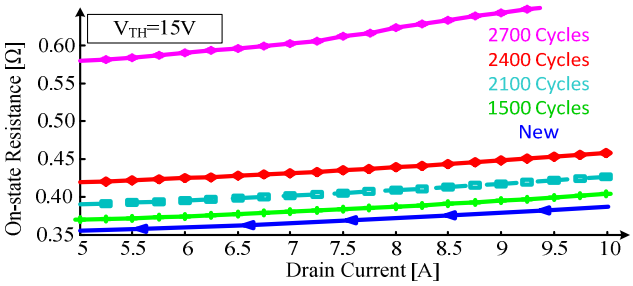


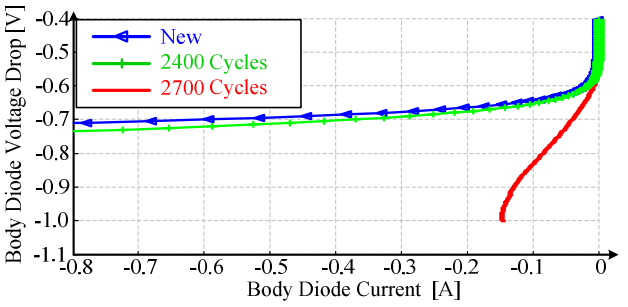
Fig. 5. Parameter variations according to the thermal cycles; (a) Breakdown voltage, (b) Leakage current, (c) Body diode forward avalanche voltage.

The T-SAM and C-SAM analyses are conducted to observe possible delamination and voids on the surfaces. The dark spots in T-SAM and the red spots in C-SAM reveal possible delamination. The C-SAM and T-SAM results of a power MOSFET cycled for 300 thermal cycles shown in Fig. 2. It is seen that the images are clear and shows no sign of voids/delamination. The failure analyses of the same sample after 3300 thermal swings are shown in Fig. 3. The T-SAM result suggests possible delamination on the die attach, and C-SAM results indicate voids on several spots. The device has been cross-sectioned and bond-wire has been analyzed as shown in Fig. 4. As it can be seen, there is no significant damage on the bond-wire.

Some of the I-V curves under the aforementioned aging conditions are given in Fig. 5-7. The breakdown voltage has been measured as shown in Fig. 5(a) under the compliance of I_{DS}=250µA. It is seen that it increases by 2V at the end of the aging cycles; however, the increase is relatively small and does not exhibit a consistently increasing trend. As seen from Fig. 5(b), the leakage currents do not change significantly till the complete failure. The sample 6D has failed under short-

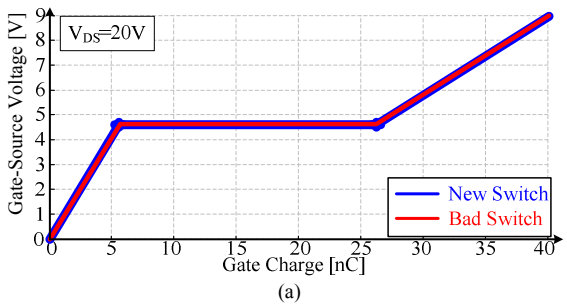


(a)

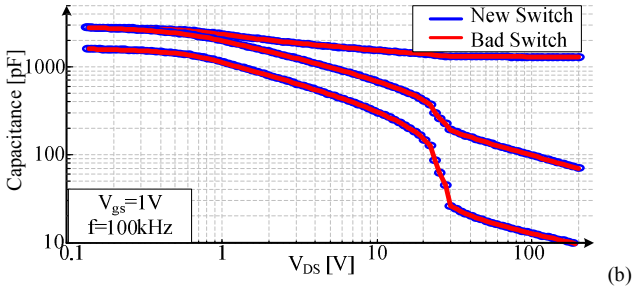


(b)

Fig. 6. Switch characteristics with respect to aging; (a) On-state resistance, (b) body diode voltage drop.



(a)



(b)

Fig. 7. Switch characteristics with respect to aging; (a) Gate charge, (b) Parasitic capacitances.

circuit fault. This failure can be observed from the increased leakage current around 3300 cycles. Fig. 5(c) shows the body diode forward avalanche voltages of the two samples. As it is seen, the p-n junction characteristics do not change which suggests that the failure is rather extrinsic

Fig. 6 presents the on-state resistance and body diode voltage drop at different aging intervals. As expected, the on-state resistance increases while the increase in the body diode voltage drop verifies the increased resistance between drain to source terminals. From electrical point of view, the body diode voltage drop of a switch is expressed as

$$V_{SD} = V_F + r_L I_{SD} \tag{1}$$

where, V_{SD} is the voltage drop between source and drain terminals, r_L is the internal resistance between source to drain terminals, V_F is the forward voltage drop of the p-n junction, and I_{SD} is the current passing through the body diode. As it has been shown in Fig. 5(c), V_F does not change throughout the aging, which suggests that the increase in V_{SD} is due to the increased r_L. It is found out that the increment in the r_L is in fact equal to increment in the on-state resistance, $R_{ds,on}$.

In Fig 7, the gate charge and parasitic capacitances variations have been plotted for healthy and aged states. The curves suggest very small change in these characteristics. As shown in Fig. 8, the threshold voltage increases correspondingly. It has been reported in literature that the bond-wire liftoffs in a power module reduces the overlap surface of the gate polysilicon with doped N and P regions, which decreases the gate-source capacitance [3]. However, the device under test is in a discrete package with only one drain-to-source bond-wire. The solder degradation is not expected to have an effect on the voltage threshold, as thermal impedance degradation at the joints does not have any physical interference with Si chip. Considering that compliance for threshold voltage test is 250µA, the junction would not be heating up. In fact, threshold voltage is used to correct the thermal impedance model of a degraded switch in [20], as it is not affected by the solder joint degradation.

One of the anticipated reasons for this change is the gate oxide degradation due to damaged source metallization and trapped electrons and holes in the gate-oxide. The devices had been decapsulated after the failure, which revealed source metallization damage. This partially degraded gate-oxide layer causes the changes in the gate oxide capacitance, which has the following relations with gate-source and gate-to-drain capacitances [3].

$$C_{gs} = \frac{C_{oxs} C_s}{C_{oxs} + C_s} + \frac{C_{oxc} C_c}{C_{oxc} + C_c} \tag{2}$$

$$C_{gd} = \frac{C_{ox} C_{dep}}{C_{ox} + C_{dep}} \tag{3}$$

where C_{oxs} and C_{oxc}, are the capacitances between gate oxide and N+ region, gate oxide and P+ region, respectively. C_s and C_c represent the capacitances of the depletion regions for N+ and P+ regions, and C_{dep} denotes the capacitance of the depletion region under the gate oxide. It is clear that decrease of gate oxide capacitances reduces both C_{gs} and C_{gd}. This decrease can also be observed in the gate threshold voltage variation as plotted in Fig. 8. The threshold voltage value has shifted by around 55mV at the end of the aging period. The threshold voltage is expressed as [21]

$$V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{4\varepsilon_s q N_a \phi_F}}{C_{ox}} \tag{4}$$

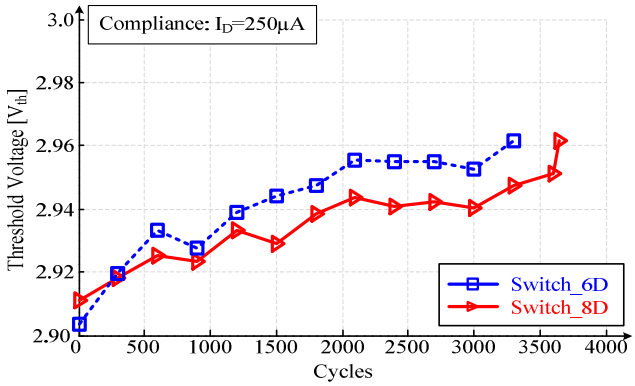


Fig. 8. Gate threshold voltage variation captured from the first set of test sampled at every 200 thermal cycles.

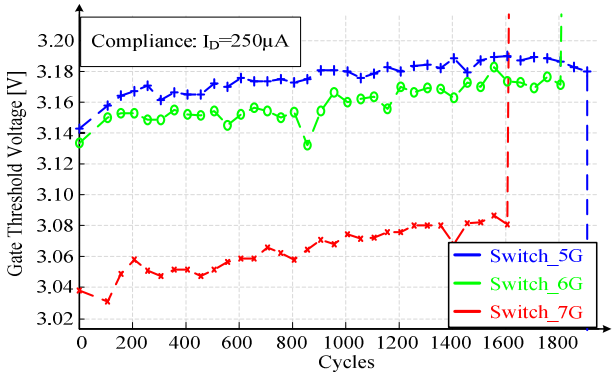


Fig. 9. Gate threshold voltage variation captured from the second set of test sampled at every 50 thermal cycles.

where, V_{FB} is the flatband voltage, $\square_F$ is the half contact potential, q is the charge of an electron, N_a is the doping density, ε_s is the dielectric constant of silicon. As Eq. (4) dictates, reduced gate oxide capacitance increases the threshold voltage value. Since the degradation of gate oxide is not severe in these samples, both the parasitic capacitances and threshold voltage variations are rather small. Yet, it is pertinent that threshold voltage steadily increases during aging, which makes it a potential failure precursor for remaining useful lifetime estimation.

To confirm this conclusion, another set of experiments were carried out and the results are presented in Fig. 9. The data is captured at every 50 thermal cycles rather than 200 thermal cycles to obtain more data points for evaluation. The resultant experimental data can be modeled empirically through exponential fit function. Based on the data, the threshold voltage can be expressed as in Eq. (5).

$$V_{Th}(t) = \alpha\left(1 - e^{-\beta t}\right) + V_{Th,init} \tag{5}$$

For constant α and β, Eq. (5) can be written in state-space form as

$$\dot{V}_{Th}(t) = -\beta V_{Th}(t) + \beta\left(\alpha + V_{Th,init}\right) \tag{6}$$

Discretizing the system yields

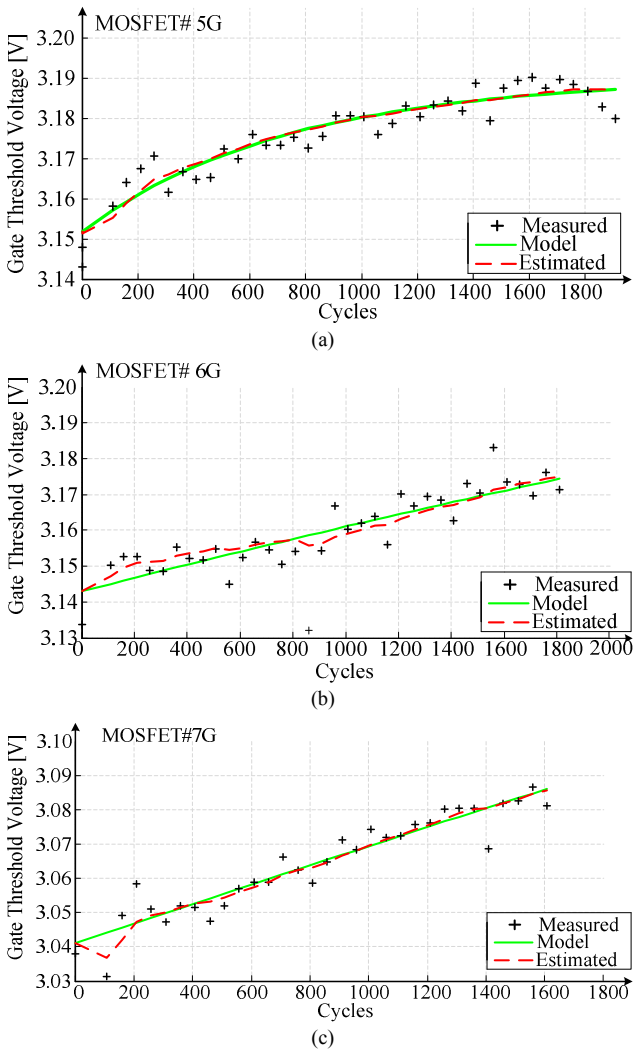


Fig. 10. State estimation with Kalman Filter for samples (a) MOSFET #5G, (b) MOSFET #6G, (c) MOSFET #7G.

$$V_{Th}(k+1) = V_{Th}(k)\cdot(1 - \Delta t\beta) + \beta\Delta t\left(V_{Th,init} + \alpha\right) \tag{7}$$

It is possible to estimate the posterior state by applying KF to the empirical model given in Eq. (7). The implementation steps of the KF is similar to [17], in which on-state resistance variation had been identified as a failure precursor and the empirical model is filtered with KF. At every time step, the new state is estimated in a recursive manner using the previous posterior estimate that is found through the time and measurement updates. The estimated state obtained from the KF is compared with the actual measurement data in Fig. 10. Normal prediction horizon of EK is one step. However, EK can also be used for predicting n steps ahead, with current error covariance. As the real measurements are taken, the error covariance is updated and trajectory converges to the one obtained from the model. Fig. 11 presents the estimated trajectory of the state estimate after 200 and 400 thermal cycles for device 5G.

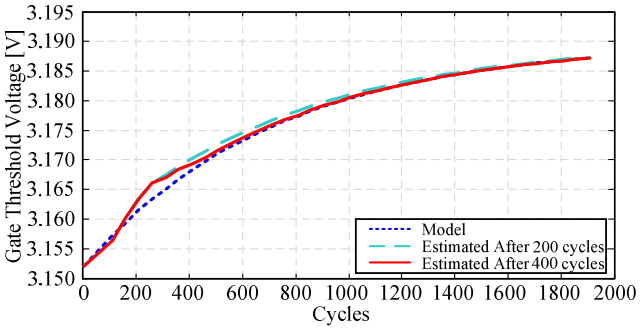


Fig. 11. RUL prediction for MOSFET #5G.

III. CONCLUSION

In this paper, comprehensive analyses of thermally aged power MOSFETs based on parametric current/voltage, parasitic capacitances, and gate charge variations with respect to aging cycles are presented. The power switches are exposed to thermal cycling, and the parametric variations are captured using an automated curve tracer at every determined number of cycles. It has been shown that on-state resistance, body diode voltage drop, parasitic capacitances and gate threshold voltage are the only viable failure precursors for die attach solder joint and gate oxide degradation mechanisms. The other parameters either do not consistently change or exhibit sudden change before failure, which can be used for instantaneous failure detection. Based on the findings, the variation in the gate threshold voltage is modeled with an exponential function, and Kalman Filter is used to filter out the measurement noise and model errors, and estimate the remaining useful lifetime. The experimental results on more than 20 samples suggest that threshold voltage variation is a feasible precursor to monitor.

IV. ACKNOWLEDGEMENT

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REFERENCES

[1] K. Li, G.Y. Tian, L. Cheng, A. Yin, W. Cao, and S. Crichton, "State Detection of Bond Wires in IGBT Modules Using Eddy Current Pulsed Thermography," *IEEE Trans on Power Electron*., vol. 29, no. 9, pp. 5000-5009, Sept. 2014.

[2] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Trans on Power Electron*., vol. 25, no. 11, pp. 2734-2752, Nov. 2010.

[3] W. Kexin, D. Mingxing, X. Linlin, and L. Jian, "Study of Bonding Wire Failure Effects on External Measurable Signals of IGBT Module," *IEEE Trans on Device and Materials Reliability,* vol. 14, no. 1, pp. 83-89, March 2014.

[4] V. Smet, F. Forest, J,-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, "Ageing and Failure Modes of IGBT Modules in High-Temperature Power Cycling," *IEEE Trans on Ind. Electron.*, vol. 58, no. 10, pp. 4931-4941, Oct. 2011.

[5] H. Oh, B. Han, P. McCluskey, C. Han, and B.D. Youn, "Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review," *IEEE Trans on Power Electron*., vol. 30, no. 5, pp. 2413-2426, May 2015.

[6] N. Patil, J. Celaya, D. Das, K. Goebel, and M. Pecht, "Precursor Parameter Identification for Insulated Gate Bipolar Transistor (IGBT) Prognostics," *IEEE Trans on Reliability,* vol. 58, no. 2, pp. 271-276, June 2009.

[7] B. Ji, V. Pickert, W. Cao, and B. Zahawi, "In Situ Diagnostics and Prognostics of Wire Bonding Faults in IGBT Modules for Electric Vehicle Drives," *IEEE Trans on Power Electron*., vol. 28, no. 12, pp. 5568-5577, Dec. 2013.

[8] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance", in *Proc. IEEE International Electric Machines and Drives Conference (IEMDC)*, pp. 1-6, 10-13 May 2015.

[9] M. Held, P. Jacob, G. Nicoletti, P. Scacco, M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Proc. Power Electronics and Drive Systems*, pp. 425-430, 26-29 May 1997.

[10] W. Sleszynski, J. Nieznanski, A. Cichowski, J. Luszcz, A. Wojewodka, "Evaluation of selected diagnostic variables for the purpose of assessing the ageing effects in high-power IGBTs," in *Proc. IEEE International Symposium on Industrial Electronics (ISIE),* pp. 821-825, 4-7 July 2010.

[11] Brown, D., M. Abbas, A. Ginart, I. Ali, P. Kalgren, and G. Vachtsevanos, "Turn-off Time as a Precursor for Gate Bipolar Transistor Latch-up Faults in Electric Motor Drives," in *Proc. Annual Conference of the Prognostics and Health Management Society*, pp. 1-8, 2010.

[12] Sonnenfeld, G., K. Goebel, and J.R. Celaya, "An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors," in *Proc. IEEE AUTOTESTCON*, pp. 205-215, 2008. Turn-Off Time as an Early Indicator of Insulated Gate Bipolar Transistor Latch-up.

[13] A. Ginart, M. J. Roemer, P. W. Kalgren, and K. Goebel, "Modeling aging effects of IGBTs in power drives by ringing characterization," in Proc. Annual Conference of the Prognostics and Health Management Society, pp. 1-7, 2008.

[14] Celaya, J.R., P. Wysocki, V.Vashchenko, S. Saha, and K. Goebel, "Accelerated aging system for prognostics of power semiconductor devices," in *Proc. IEEE AUTOTESTCON*, pp. 1-6, 2010.

[15] Celaya, J., A. Saxena, P. Wysocki, S. Saha, and K. Goebel, "Towards Prognostics of Power MOSFETs: Accelerated Aging and Precursors of Failure", in *Proc. Annual Conference of the Prognostics and Health Management Society*, pp. 1-10, 2010.

[16] Celaya, J.R., N. Patil, S. Saha, P. Wysocki, and K. Goebel, "Towards Accelerated Aging Methodologies and Health Management of Power MOSFETs (Technical Brief)", in *Proc. Annual Conference of the Prognostics and Health Management Society*, pp. 1-8, 2009.

[17] S. Dusmez, and B. Akin, "Remaining Useful Lifetime Estimation For Degraded Power MOSFETs Under Cyclic Thermal Stress", in *Proc. IEEE Energy Conversion Conference & Expo.*, pp. 3846-3851, 2015.

[18] M. Ciappa, "Selected Failure Mechanisms of Modern Power Modules," Microelectronics Reliability, vol. 42, no. 4–5, pp. 653-667, 2002.

[19] J.-M. Thebaud, E. Woirgard, C. Zardini, S. Azzopardi, O. Briat, J.-M. Vinassa, "Strategy for designing accelerated aging tests to evaluate IGBT power modules lifetime in real operation mode," *IEEE Trans on Components and Packaging Technologies*, vol. 26, no. 2, pp. 429-438, June 2003.

[20] H. Chen, B. Ji, V. Pickert, W. Cao, "Real-Time Temperature Estimation for Power MOSFETs Considering Thermal Aging Effects," *IEEE Trans on Device and Materials Reliability*, vol. 14, no. 1, pp. 220-228, March 2014.

[21] Bart Van Zeghbroeck, *Principles of Semiconductor Devices and Heterojunctions*. Prentice Hall , 2007.