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Reliability of power transistors against application driven temperature swings

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Abstract

This report presents the results of the investigations undertaken to study the robustness of MV-NDMOS power transistors in SOI against fast internal temperature swings. The heating effects are studied for various frequencies and amplitudes of the square wave power dissipation. The temperature in the device is continuously measured with an integrated temperature sensor. The conditions necessary to obtain various peak temperatures are established and reliability studies are performed. No failures were observed in devices with T_{peak}~220°C and ΔT~100°C while the higher T_{peak}~300°C with ΔT~200°C showed early failures only in samples with silicon nitride used as the intermetal dielectric. The source of these early failures could be due to the enhanced conduction (of Frenkel-Pool type) of the nitride at elevated temperatures. The present investigations indicate power transistors to be more robust for high temperature applications when oxide is used as the intermetal dielectric in stead of nitride. Samples (both nitride and oxide) at end of life showed signs of combined electro- and thermo-migration of the metal layers and cracking of the passivation layer. © 2002 Elsevier Science Ltd. All rights reserved.

1. Introduction

It is conjectured that the peak temperature is a limiting factor in the design of power transistors in general and especially in SOI where the buried oxide significantly influences the thermal behavior and ultimately the robustness of the devices. Currently, power transistors are sized based on simulation data [1]. However, it is not clear how well these simulations compare with reality [2]. If the design peak temperature used to calculate the device area is very high it may lead to combined thermo-migration and electro-migration and subsequently damage the metallization layer leading to device failures. On the other hand, if the modeled peak temperature is much higher than what is observed in application, the calculated power area is larger than required, leading to unnecessary high cost for the product. Thus it is important to determine experimentally the reliability aspects of devices with different peak temperatures, thereby arriving at an optimum design area for a given peak temperature desired in application. This is aimed in the present study and the results obtained here can be taken as calibration for simulations.

2. Device structure

The device investigated here is the MV-NDMOS power transistor with an area of 0.75mm^2 in the A-BCD-2 [3] process using SOI technology. The thickness of the buried oxide (BOX) is 1μm and the SOI layer is 1.5μm thick. The thickness of the gate

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oxide is 37nm. The device is connected with double metal interconnect. The thickness of the first metal (IN1) is 0.6μm while the second metal (IN2) is 2,5μm thick. The standard interlayer dielectric (ILD) between the two metal layers is a 0.9μm thick silicon nitride. The standard passivation layer is also silicon nitride of thickness 1.8μm. Devices with different ILDs and passivation layers have also been studied and the results are presented below. Some device parameters at room temperature are BV_{ds}=30V,and R_{on} (at V_{gs}=12V and with power sense measurement)=55mΩ.

3. The measurement method

The measurement set-up is shown in Fig. 1(a). The supply voltage V_{sup}, V_{gs}, and the load R_L are all varied and the heating of the power transistor can be monitored continuously from the readings of the diodes integrated in the transistor at the locations shown schematically in Fig. 1(b). The diode in the center of the transistor has an area of about 0.004 mm^2 and is junction isolated, while the diodes outside the Silicon Island are oxide isolated. In order to translate the

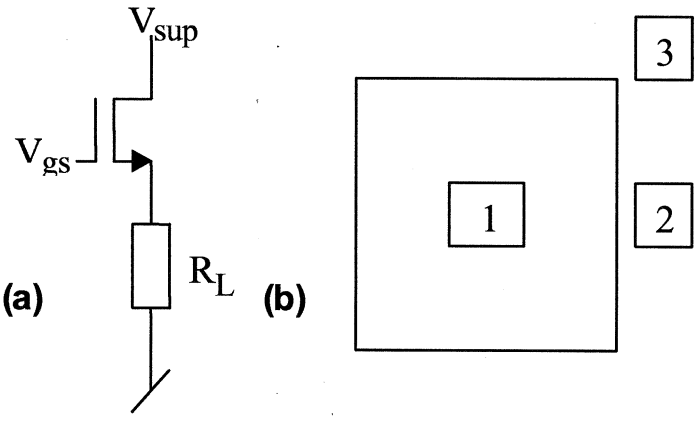

Fig. 1. The circuit (a) used to study the heating effects of the MV-NDMOS transistor. The diodes used as temperature sensors are integrated in the power transistor in the locations shown in (b). The diode numbered 1 is junction isolated while the diodes numbered 2 and 3 are oxide isolated

voltages of these diodes to actual temperatures, the diodes were first calibrated in a furnace up to 250°C. The diode voltages were found to drop linearly with increasing temperatures for constant currents. A linear temperature coefficient of -1.687mV/K was obtained for a constant biasing current of 10μA.

The heating effects at different locations of the transistor (shown in Fig. 1(b)) are plotted in Fig. 2 in one power cycle. As expected, most heating occurs in

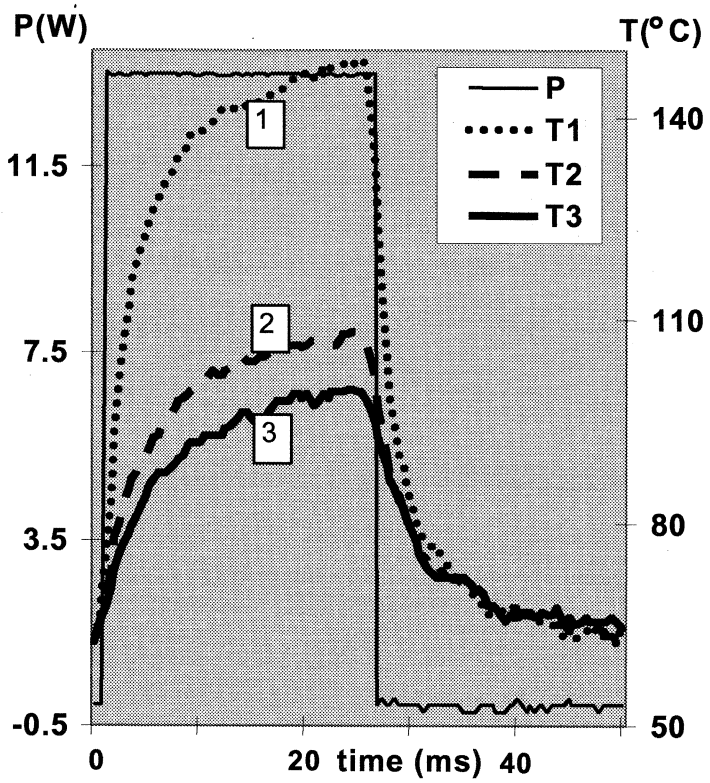

Fig. 2. The heating (right axis) as measured by the three diodes (see Fig. 1(b)) of the power transistor under the conditions V_{sup}=15V, R_L=4Ω and a square wave V_{gs} of amplitude 2.5V, frequency 20Hz and duty cycle 50%. The dissipated power (P) is also shown (left axis).

the central region (labeled 1) of the transistor and the corner diode (labeled 3) registers less heating than the side one (labeled 2). These differences are due to the different boundary conditions, and the thermal de-coupling of dielectric isolated devices.

By tuning V_{sup}, V_{gs} and using a load of R_L=2Ω different peak temperatures could be obtained. For doing further life test experiments the standard average junction temperature of 150°C was desired. This was obtained as shown in Fig. 3 with a V_{sup}=18V and a square wave V_{gs} of amplitude 2.25V and duty cycle 50%. Different peak temperatures with different ΔT's (the difference between the maximum and the minimum temperature attained) were obtained by varying the frequency as shown in Fig. 4.

It is observed that the temperature peaks (and ΔT's) are higher for lower frequencies but for higher frequencies the number of swings in a given time increases, although with lower temperature peaks. It has to be established by life tests, which of these factors is worse for the device. These effects arise in applications such as audio amplifiers with widely varying input signals. Such devices have been normally qualified at high frequencies (~1kHz) without problems

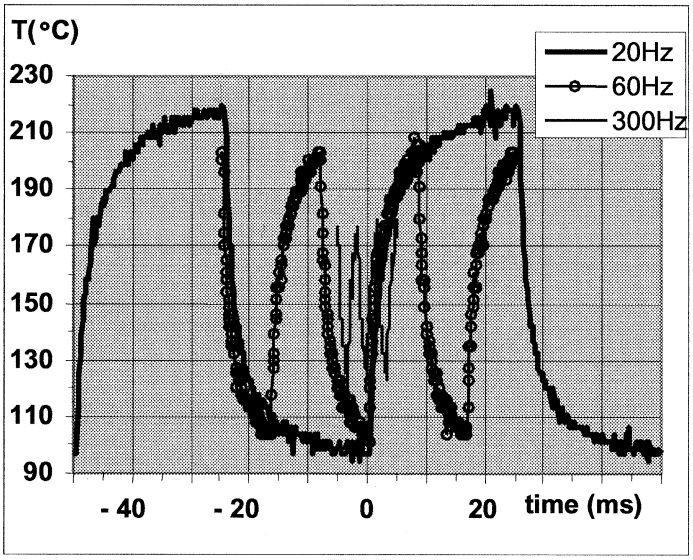

Fig. 3. The heating effect of the power transistor with V_{sup}=18V, R_L=2Ω and for different frequencies of a square wave V_{gs} of amplitude 2.25V and duty cycle 50%.

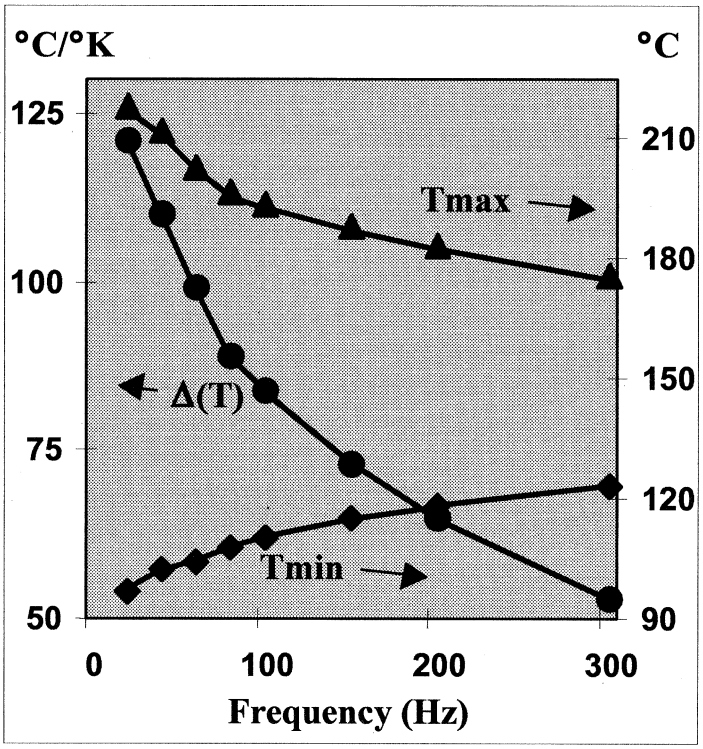

Fig. 4. The minimum (T_{min}) and maximum (T_{max}) temperatures with the associated ΔT's in the central region of the power transistor under the conditions of Fig. 3.

and failures. Hence it is thought that high peak temperatures play a greater role in the degradation and eventually failures of power devices. In the present investigation the effect of high peak temperatures will be only considered and hence the input frequency is limited to 20Hz.

4. Thermal simulation

It should be noted that although the area of the central diode is negligible in comparison to the total power area there is no power dissipation in this central region and therefore the central diode records neither the highest nor the lowest temperature in the power transistor. Thermal simulations have therefore been performed to check how big this dip is in the site of the central diode. As input for the simulation of the temperature distribution in the power transistor a test chip mounted in a Philips DBS-17 power package shown schematically in fig. 5 was used. Reflecting boundary conditions were used along the symmetry line in the middle of the power transistor, at the side edges of the chip, and at the top of the chip, so all heat energy flows through the bottom surface to the copper block

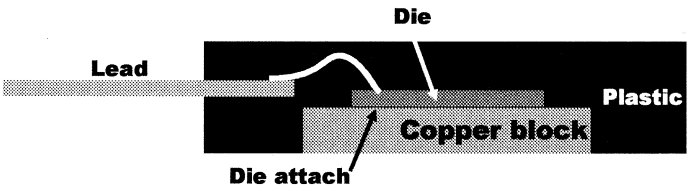

Fig. 5. Schematic cross-section of the power package used in the thermal simulation.

(heat spreader) and the external heat sink. So, the die, the die-attach and the copper block were all included in the thermal simulation. The heat sink temperature was considered constant. For both Silicon and SiO_2 temperature dependent thermal conductivity was used. The structures of the Silicon On Insulator (SOI) layers and the double metal interconnect described in sec. 2 were included in the thermal model since these significantly influence the thermal behaviour for fast power pulses [4]. It was found from the simulations that the difference between the maximum temperature in the device and that in the region of the central sensor is larger for smaller pulse widths and saturates to a value of ~12.5% for pulse widths larger than 10ms. The simulated temperature distribution in the power area with the central diode is presented in Fig. 6 at t=15ms for a square wave dissipation of amplitude 30W, frequency 20Hz with a duty cycle of 30% and a constant heat sink temperature of 90°C (found from measurements). The maximum temperature in this case is found to be 330°C while in the central point the temperature is simulated to be 290°C. Thus it should be

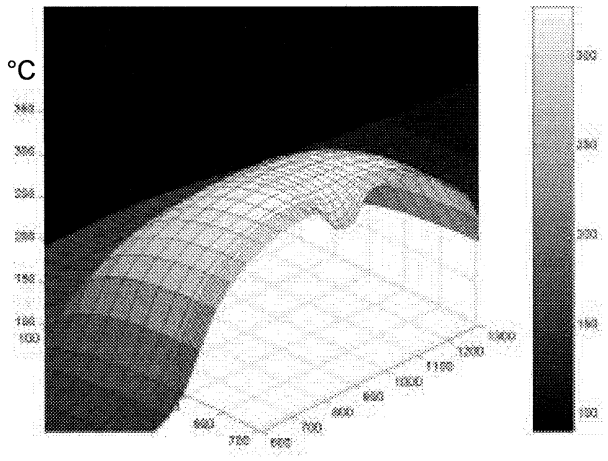

Fig. 6. Simulated temperature rise distribution (in °C) in the power transistor with the central diode at t=15ms for a power dissipation of amplitude 30W, frequency 20Hz and a duty cycle of 30%. The co-ordinates of the power area are in μm.

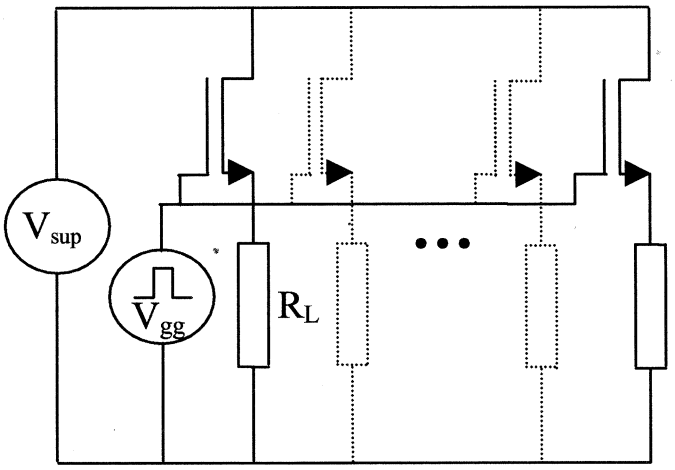

Fig. 7. The set up used for life test.

noted that the actual peak temperatures in the devices are even larger (by ~10%) than those presented here from the readings of the diodes placed in the center of the devices. Power transistors without the integrated temperature sensors were also made and life tested. Testing devices without the temperature sensor controls the design of the temperature sensors integrated in the power transistors.

5. Life test results

5.1. Peak temperature of 220°C and ΔT~100°C

Devices were stressed under the conditions shown in Fig. 3 and with a frequency of 20Hz. The life test set-up used is shown in Fig. 7. The maximum power dissipated under these conditions is P≈17.5W and the peak current in the device is $I_d \approx 1.1$A giving peak current density values of 3.2e4 A/cm^2 and 4.7e4 A/cm^2 in IN1 and IN2 respectively. These current densities values lie well within the design rules. The life tests were done at room temperature and heat sinks were used. In every hour of life test the device goes through 72000 internal thermal cycles with a ΔT=110°C and a T_{max}=220°C. The temperature of the power transistors was monitored regularly and no failures were observed during the whole life test lasting 1080hours (with 78e6 thermal cycles). Two samples were de-capped after the whole life test and signs of metal migration could be seen in the power areas and on the bond pads. In some places the IN2 was seen to ooze out creating cracks in the passivation layer.

5.2. Peak temperature of 300°C and ΔT~200°C

The power in the devices was further increased to a $P_{max} \approx 30$W by a V_{sup}=24V and V_{gg}=5.5V. A peak temperature of ~300°C with ΔT ~200°C was obtained with a duty cycle of 30% of the 20Hz signal. The average junction temperature was maintained at 150°C. A peak current of 1.5A was found in this case giving current density values of 4.8e4A/cm^2 in IN1 and 6.9e4A/ cm^2 in IN2. Devices without the central temperature sensor were also tested. Failures were found in both types of devices with more failures in devices with the central diode. The slight design modification and the junction isolation of the central diode can explain this difference. The electrical parameters were measured after 1080 hours of stressing and the R_{on} (at V_{gs}=12V) was found to increase by 27% and 18% respectively in devices with and without the central diode indicating degradation of the metal lines. The Kelvin set up used in the measurement rules out contributions from Au-Al inter diffusion (Kirkendall voiding) in the degradation of R_{on}. Good samples were de-capped after life test and a FIB cross-section taken in some places show (see Fig. 8) strong metal voiding (mostly in IN2) and extrusions of the IN2 due to cracking of the passivation layer. Pure Electromigration experiment [5] done at 220°C on 16μm broad IN2 lines (of AlSi(1%)Cu(0.5%)-kind as used here) with a current density 1e6A/cm^2 give a t(50%)=276hours. This would translate to a t(50%) ~8000hours in the present case assuming the IN2 line is constantly maintained at 300°C. Thus the strong voiding seen in Fig. 8 can only be explained by thermomigration (movement of Al driven by the large temperature gradients) and stress voiding.

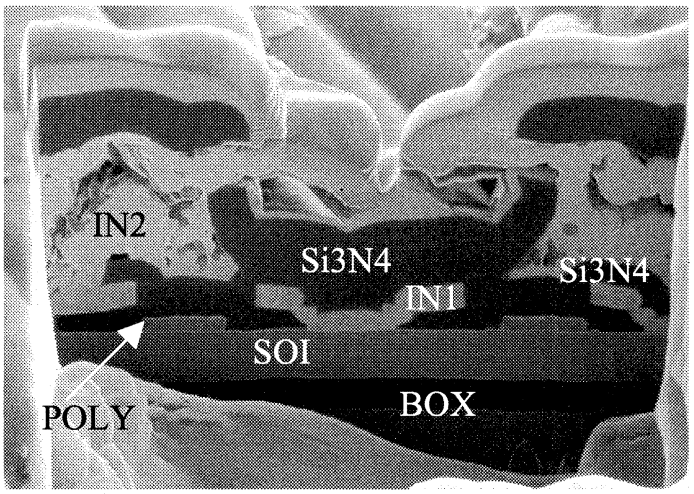

Fig. 8. A FIB cross-section through the power device structure after ~500hours of life test with T_{max}~300°C and ΔT ~200°C. Metal (mostly IN2) voiding and extrusions of IN2 through the passivation layer can be seen.

5.3. Power devices with different ILDs and passivation layers

It was thought during the studies that standard silicon nitride used as the ILD between the two metal lines could cause problems due to cracking since nitride layers are known to exert very high compressive stresses. A batch of devices with different ILDs and passivation layers were therefore assembled and life tested under the conditions presented in the previous section 5.2 (with a T_{max} ~ 300°C and ΔT~ 200°C). The results of the life test are summarized in Table 1.

The oxide ILD was a PECVD oxide of thickness 0.655μm (maintaining the same dielectric thickness as the nitride samples). The low stress nitride is a variation of the standard nitride producing lower bowing of the wafer which simplifies sawing. The thickness of the low stress nitride layers were the same as the standard nitride layers. Clearly the devices with oxide as the ILD are found to be the most robust for these applications with high peak temperatures. All devices presented in Table 1 that did not fail were further tested till ~2000hours and no further failures were found. Some of these good samples with different ILDs and passivation layers were de-capped and analyzed. They all showed similar behavior of Fig. 8, namely strong IN2 voiding and cracking of the passivation layer.

The source of the early failures in devices with nitride as the ILD is not completely understood yet. However it is conjectured that the increased conduction, dominated by the Frenkel-Pool conduction

Table 1
Lifetime test results from power MV-NDMOS transistors with the different ILDs and passivation layers.

ILD	Passivation layer	Early failures (≤168 hours)
Nitride	Nitride	9/10
Nitride	Low-stress nitride	9/10
Oxide	Nitride	0/10
Oxide	Low-stress nitride	0/10
Low-stress nitride	Nitride	7/10
Low-stress nitride	Low-stress nitride	3/10

(bulk-controlled mechanism), in Nitride [6,7] at elevated temperatures (T ≥ 150°C) could be the source of the early failures seen only in the Nitride devices. Compressive stresses in Nitride dielectrics could also play a role but not a major one as devices with low-stress nitrides also show failures. Electromigration studies [8] with different dielectric layers have shown that the lifetimes of metal lines are dependent on the characteristics of the dielectric layers deposited on them.

Single devices were finally tested till failure. The supply voltage was fixed at 23.5V and the frequency and duty cycle of the gate voltage were also fixed at 20Hz and 28% respectively. The amplitude of the gate voltage was increased till failure was observed and the failed products were de-capped and inspected. The failures from the nitride and the oxide samples (without the central diode) are presented in Figs. 9 and 10 respectively. The nitride sample failed at V_{gg}=8.9V with an open while the oxide sample failed at V_{gg}=9.1V with a short. The peak powers at these failures are ~60W. The samples with the central diode were also tested and the failures were found at V_{gg}=7.2V for the nitride sample and at V_{gg}=8.9V for the oxide sample. As seen in Fig. 9 the nitride sample is seen to have become very hot possibly due to thermal runaway, with molten metal spread in the device. These same types of failures were also found in the life test products. In contrast the IN2 layer in the oxide sample shown in Fig. 10 is intact. These point towards a difference in the failure mechanism between the nitride and the oxide samples. The oxide ILD is seen to be able to better handle the high peak temperatures in the power device.

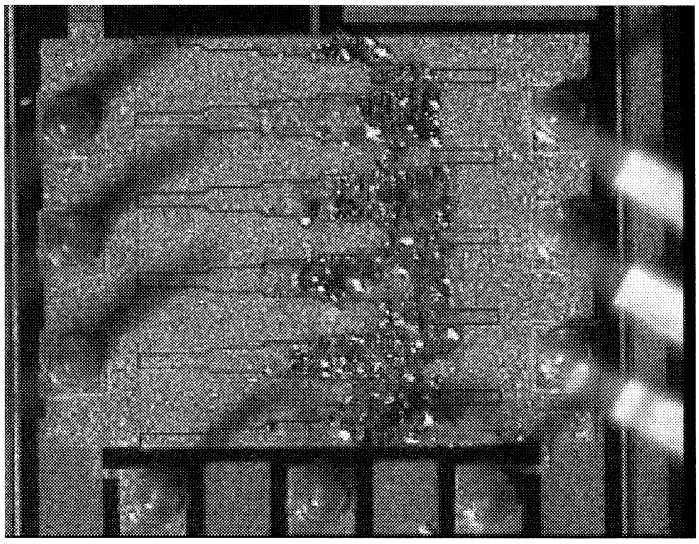

Fig. 9. A typical failure found in the power device with nitride as the ILD.

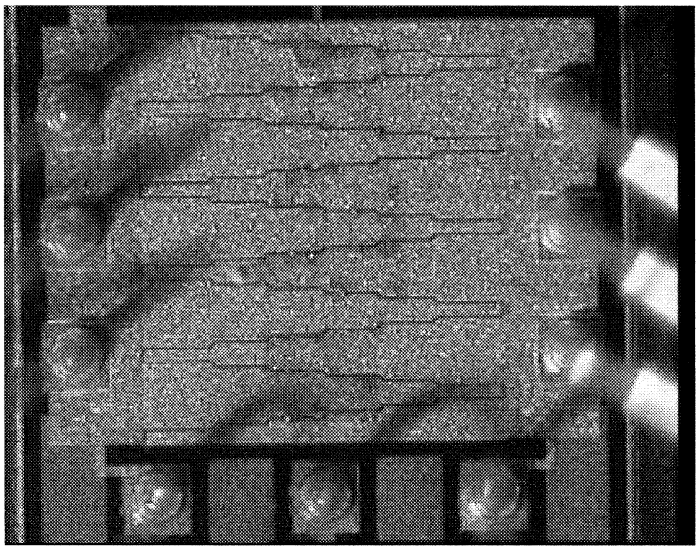

Fig. 10. The failure found in the power device with oxide as the ILD.

6. Conclusions

In conclusion, the reliability of MV-NDMOS power transistors in SOI has been investigated under application induced temperature swings. A T_{max} ~ 200°C and ΔT~ 100°C did not produce failures in life test. However a higher T_{max} ~ 300°C with ΔT ~ 200°C showed early failures only in devices with nitride as the ILD. Samples that did not fail showed strong degradation of the metal lines that can only be explained by the large temperature swings. The source of the early failures could be due to the enhanced conduction (of Frenkel-Pool type) of the nitride at elevated temperatures. Special test structures are being considered to check this further. In addition more devices are presently tested to gather statistical information. These studies indicate power transistors with oxide, used in place of nitride as the intermetal dielectric, are more robust especially in applications with high peak temperatures and this has to be taken into account in the area optimization of power transistors.

Acknowledgements

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