

Active cycling reliability of power devices: Expectations and limitations

W. Kanert*

Infineon Technologies, Am Campeon 1-12, 85579 Neubiberg, Germany

ARTICLE INFO

Article history:

Received 30 May 2012

Received in revised form 15 June 2012

Accepted 15 June 2012

Available online 20 July 2012

ABSTRACT

Active cycling of power devices, i.e. exposure to repetitive voltage and current pulses, causes power dissipation, resulting in thermo-mechanical loads that can cause different failure mechanisms. This paper focuses on degradation of the metallization. Requirements and customer expectations, using examples from automotive applications, are discussed, contrasting these with the procedures for reliability assessment and their limitations.

© 2012 Elsevier Ltd. All rights reserved.

1. Introduction

Power devices have found wide ranges of applicability. From the light-weight battery charger of your mobile phone to real heavy, multi-chip, high voltage power modules in traction, power devices are used either as discrete components or integrated together with CMOS and bipolar devices in so called Smart Power technologies. Voltages range from a few tens of volts to kilovolts, currents from a few to hundreds of amperes.

Power dissipation and thermal management are key issues in the application and the reliability of the devices. Reliability of these devices is of paramount importance, either because of economical reasons or because of safety reasons. Breakdown of an offshore windmill may serve as illustration of the first and fail to trigger an airbag as illustration for the second point. This paper has a focus on automotive applications, but the issues raised may apply in an equal manner to other, e.g. industrial, applications.

Recently, the implications of the pulsed load conditions on the reliability of power devices have received increasing attention. Active cycling is the exposure of the power stage to repetitive voltage and current pulses. This causes different degradation mechanisms of the devices, such as bond degradation, die attach degradation, thermal runaway or latch-up of the DMOS. The failure mechanisms depend not only on the load conditions, but also on the technology, materials and the design. System boundary conditions play a major role, too. Active cycling can cause severe power dissipation that leads to heating of the device and thermo-mechanical stress and fatigue. This fatigue can result in failures of the device [1]. This paper looks at degradation of the chip metallization and its effect on device reliability. It also discusses the difference between customer expectations and what reliability assessment is able to deliver.

1.1. Providing a common basis

As experience shows, notions of reliability are often diverging and blurred. It is, therefore, advantageous to give a definition of reliability as a common starting point:

Reliability is the probability of an item to perform a required function under given conditions for a given time interval.

Reliability is not an inherent property of the product but is related to the application requirements, i.e. the “given conditions”. “Time interval” corresponds to the lifetime requirements of the component.

Assessing the reliability is trying to answer the basic question:

Is our product sufficiently reliable in the application?

The term “sufficiently” is used deliberately. Sufficiently means fulfilling the customer’s requirements. These requirements can be substantially different, so there is no general definition of “sufficient”.

1.2. Customer expectations

Customers expect components to operate reliably under their application conditions. Due to the multitude of devices in a complex system like a car, failure probabilities in the range of single digit ppm (parts per million) or even below are required for the car to have an acceptable probability of defective behavior overall.

Application requirements are harsh with increasing tendency. Power devices are used in many critical applications, e.g. lighting, motor management, braking systems, electronic power steering and airbag firing. Table 1 gives an example of requirements for a smart power device used as valve drive in motor management. These devices are also prone to be exposed to transients that are transported via the power net of the car, while they themselves need their switching behavior be tuned to meet electromagnetic interference requirements.

* Tel.: +49 171 5531318; fax: +49 89 234 9553585.

E-mail address: Werner.Kanert@infineon.com

Table 1

Example of customer requirements a smart power device for valve drive in motor management.^a

Mode of operation	Max. pulse energy (mJ)	Number of pulses
Normal operation	15	6×10^8
Jump start	50	1×10^4
Load dump	100	5

^a Numbers are fictitious but give order of magnitude.

Safety related applications require special care, as a fail of such a device may cause harm to a person or even loss of life. Functional safety imposes constraints on the development and fit rates are required for the component. And customers expect the components to sustain not only “normal operation” conditions, but also error conditions such as short circuits.

2. Power devices – a short description

Power devices come in a large variety. They cover a wide range of voltages, from a few tens of volts up to several kilovolts. They can be discrete or integrated, depending on the technological needs and functional requirements, and economic considerations. Current and voltage capability, on-resistance and switching characteristics are among the relevant performance parameters. Integrated power devices typically have on-chip protection circuits, e.g. overvoltage and overtemperature protection.

3. Application requirements and boundary conditions

As stated in the definition of reliability above, reliability has always to be related to some specified application conditions. The most prominent parameters concerning active cycling are voltage and current, both as a function of time, and, of course, the number of pulses. There are two extremes of requirements, as can be seen from Table 1. On the one hand, pulses with high energy and a low number of cycles, and on the other hand, pulses with low energy and a high number of cycles. There are different kinds of operational modes that have to be taken into account, and it has to be emphasized that the requirements for normal operation include a very high number of pulses on the order of several hundred millions of cycles. Similar requirements on the order of 1 billion cycles exist for discrete PowerMOSFETs. Such requirements imply the ensuing question of how high the temperature swing for each pulse is allowed to be to fulfil the reliability requirements. Pulse duration and duty cycle are parameters that have to be considered, and in addition the thermal boundary conditions and temperature mission profiles. These requirements constitute a multiparameter space. The problem is exacerbated by the requirement to combine different operation conditions.

Driving inductive loads leads to high voltages simultaneously to high currents during turn-off. This is illustrated in Fig. 1. The voltage is limited by a series of Zener diodes, preventing the device to enter an avalanche condition. Nevertheless, the temperature swing resulting from the power dissipation can be quite substantial.

For discrete PowerMOSFETs no such integrated voltage limitation is available. Therefore, the PowerMOSFET can enter an avalanche state under certain turn-off conditions. This corresponds to repetitive unclamped inductive switching (UIS), similar to the standard single pulse UIS test. The essential question here is, what the limitations on the pulse conditions are for the device to sustain a certain number of pulses.

Beyond the operation conditions that can be classified as functional requirements under normal operation, devices are required to sustain certain error conditions that may occur in the field.

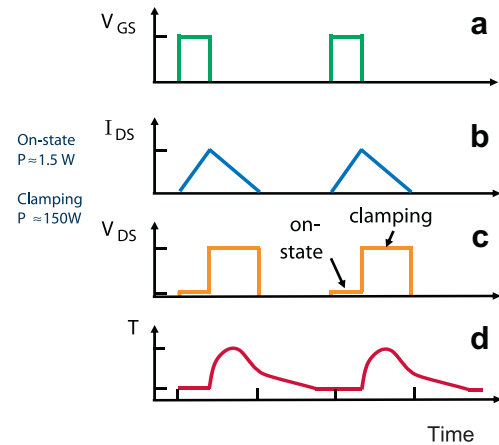


Fig. 1. Smart power device under repetitive clamping conditions. Schematic illustration of the time dependence of gate voltage (a), drain current (b), drain voltage (c), and temperature (d). Power dissipation during clamping is two orders of magnitude higher than in the on-state.

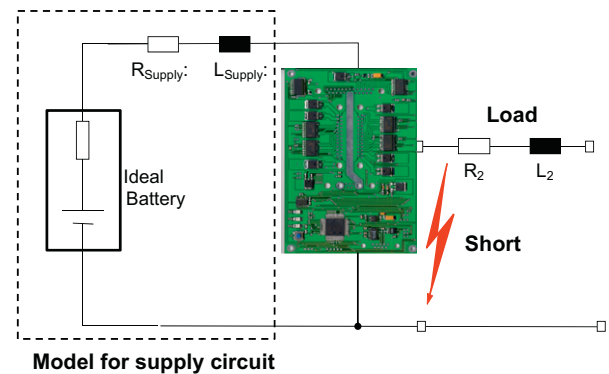


Fig. 2. Schematic outline of a short circuit configuration for a high side switch.

One of the most important of these error conditions is a short circuit. Especially for high side drivers, these short circuit requirements impose severe constraints on the technology. The case of a short circuit in a high side driver configuration is illustrated in Fig. 2. The number of pulses the device is required to withstand can be on the order of hundred thousand, meaning a high stress on the device.

4. From application conditions to device loads

Load conditions from the application have to be converted into technologically and physically meaningful data for the technology. Power dissipation leads to temperature increase in the device. Temperature is a central parameter for the reliability of the device. The usual practice of specifying a simple “junction temperature” is insufficient to deal with the problem in hand. The dynamic behavior is essential. The time scales of pulse duration and duty cycle are essential to the thermal loads of the device. As the load is dynamic, the temperature of the device is not static and usually far from being homogeneous. Rather, it is both spatially and time dependent. This fact is not captured by the simple notion of a junction temperature (as an aside, in consequence the very notion of a junction temperature has to be questioned.). And, of course, thermal boundary conditions have to be known, as they significantly influence the device temperature and, therefore, its reliability.

The first question that arises then is: considering specific application conditions, how much do different time scales matter? The second question is: if they matter, how can information on the relevant temperature be obtained?

The problem is to determine the temperature distribution on a device that may have an area of several square millimeters, for pulses that may range between a few tens of microseconds to several milliseconds.

Although integrated power devices typically have temperature sensors, these have an offset to the hottest spot by design. And they can only give information at one location, not on the spatial distribution, and usually they cannot even be read out via an output pin.

Infrared spectroscopy in different variations is a very useful tool, but also here the time and spatial resolution is not suitable for all purposes. It is also typically applied to at least partially opened devices, thereby changing the thermal boundary conditions, although also signal detection through the package has been demonstrated [2].

A useful tool is electro-thermal simulation. It gives information on the temperature distribution in the device. However, the feedback loop of temperature on the device parameters has to be implemented correctly. And calibration is mandatory [3]. If done properly, simulation provides information on the physical behavior of the device in a manner that is not accessible by measurement.

5. Standard qualification procedures for power devices

Standard product qualification procedures include some tests that require the device be subjected to active loads. The most popular of these tests, the High Temperature Operating Life Test (HTOL) [4–6] addresses integrated circuits, but not specifically power devices. Power Temperature Cycling (PTC) [6,7] is required for devices exceeding a certain power dissipation, but again does not specifically address power devices. Intermittent Operating Life (IOL) [8,9] applies to discrete devices. Neither of these tests is suited to obtain relevant information on the reliability of power devices under real application conditions.

Short circuit is addressed with AEC Q100-012 [10] and with AEC Q101-006 [11], which is identical to the former one. This standard has been issued some years ago to provide a procedure for testing short circuit capability of integrated smart power devices, and also contains a definition of short circuit, which was not available before its publication. In Fig. 2, which illustrates the short circuit of a high side switch, a short circuit may occur anywhere from the output of the power device to the load along the cable. The standard gives loads and test conditions.

Power cycling [12] is used for qualification of power modules. Together with information on the mission profile, simulation and end-of-life data, these procedures provide a means to estimate the reliability of the modules under application conditions [13].

Also, standard tests for silicon wafer technologies used to evaluate the reliability of the chip metallization, i.e. electromigration and stressmigration, are not suitable to address the problem.

6. Testing

Subjecting power devices to active cycling requires special test equipment [14]. For instance, short circuit testing of smart power switches may require currents of more than 100 A per device. Also, normal HTOL equipment is not suitable to test repetitive clamping of smart power devices for a larger number of samples, e.g. 32, simultaneously. Special detection circuitry is necessary to detect a fail of the device on-line and record the corresponding number of cycles.

The wide range of application conditions – loads and pulse conditions – cannot be covered by testing. Rather, specific conditions for reliability tests have to be chosen. Other parameters like different base temperatures or design variants extend the parameter range that has to be considered.

Many devices, especially discretes, are sold as commodity devices, for which the loads and pulse conditions may vary widely, without the supplier knowing the application conditions.

7. Failure modes and mechanisms

The basic failure mechanism considered in this paper is metal degradation due to active cycling. Active cycling results in power dissipation and a non-homogeneous, time-dependent temperature distribution on the device. The difference in coefficients of thermal expansion results in mechanical stress. If this stress is beyond the yield strength of the material, plastic deformation of the metallization is generated. Repeated cycling can cause heavily disrupted metal layers. This effect was observed by Ciappa and Malberti [15] on IGBTs subjected to short circuit loads and in that paper denoted as “metal reconstruction”. Similar short circuit effects on the metallization of high side smart power devices have recently received increased attention [16,17]. Typical failure modes of the devices are bond lift-offs or shorts due to melt-up of the device triggered either by latch-up of the DMOS or thermal runaway.

The metal degradation can be observed on discrete PowerMOSFETs exposed to repetitive unclamped inductive switching. This can be seen in Fig. 3. The metallization of a PowerMOSFET after repetitive unclamped inductive switch with a temperature swing

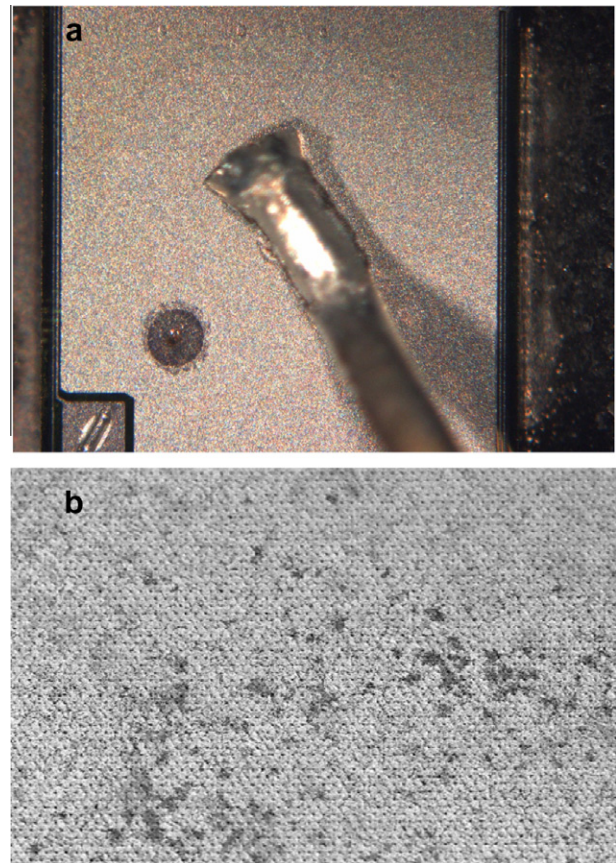


Fig. 3. PowerMOSFET exposed to repetitive unclamped inductive switching with a $\Delta T = 160$ K, showing (a) a burn mark in the source field and (b) degradation of the metallization.

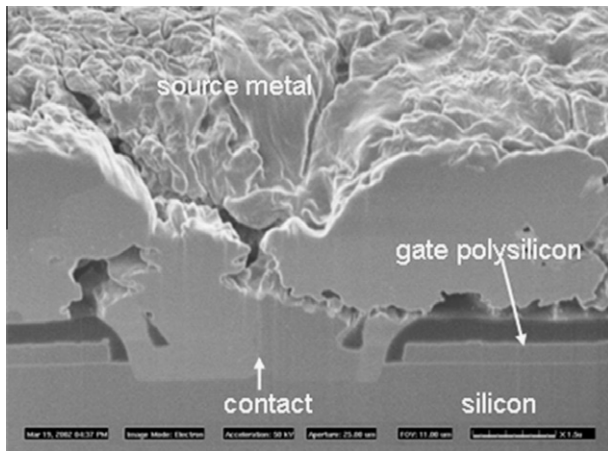


Fig. 4. Metal degradation of a high side smart power switch after repetitive short circuit.

of 160 °C shows a burn mark in the source field (a) and a closer inspection reveals degradation of the metal layer (b) with a roughened surface (dark spots).

This degradation is also illustrated in Fig. 4. Here, the source metallization of a high side switch after repetitive short circuit clearly shows the metal degradation with cracks in the metal and voids at the interface of the metal to the underlying dielectric layer.

As components are increasingly used in harsh applications, this failure mechanism has been investigated recently [18,19].

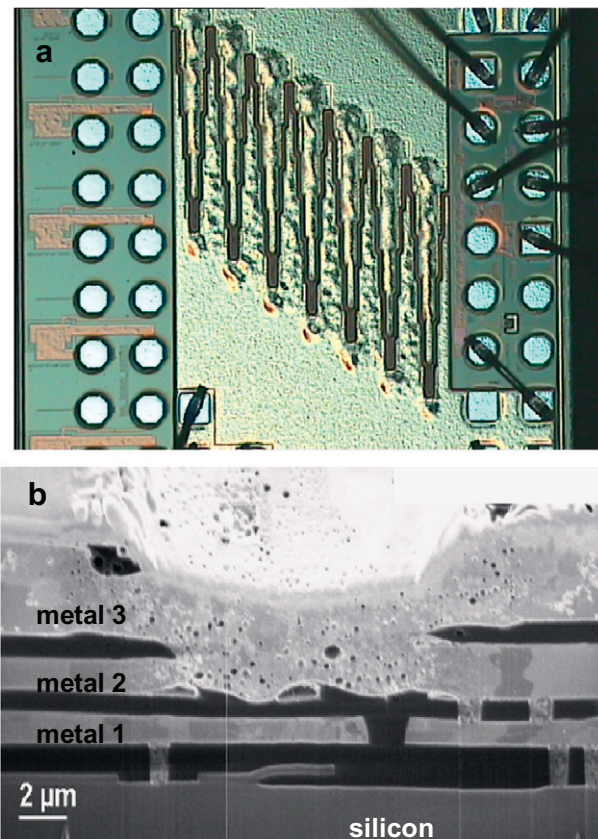


Fig. 5. Metal degradation on a smart power device after repetitive clamping with 10^9 cycles with $\Delta T \sim 100$ °C.

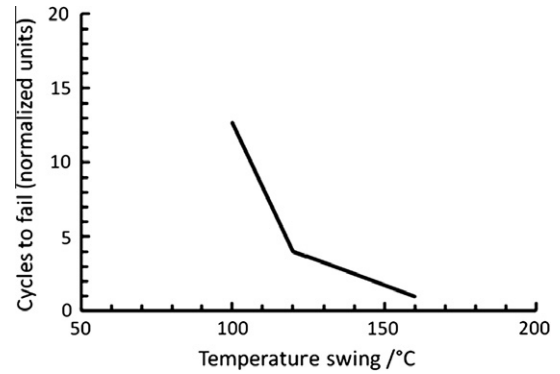


Fig. 6. Dependence of cycles to fail as a function of temperature swing for a PowerMOSFET under repetitive unclamped inductive switching conditions.

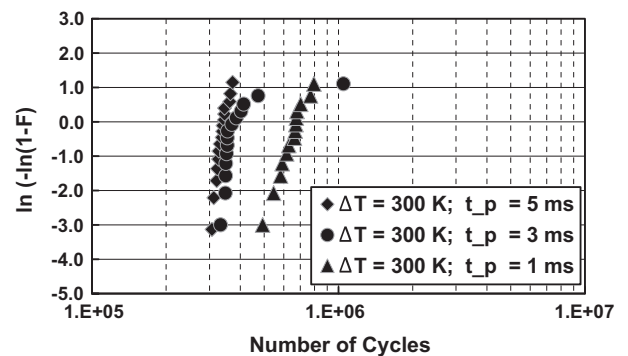


Fig. 7. Pulse length dependence of fail distributions on a dedicated test structure.

It might be assumed that this metal degradation is readily observed by measuring the on-resistance of the device. However, experiments show that the increase in on-resistance can usually only be observed at a rather late stage of the degradation.

Power stages in highly integrated smart power technologies with typically two or three wiring layers fail in a different manner under normal operation. Here metal degradation occurs, too, but it is not the thick power metal layer that eventually fails. Rather, build-up of mechanical stress in the wiring layers leads to a crack in the intermetal dielectric layer, which is subsequently filled with metal resulting in a short in the device. Fig. 5a shows the

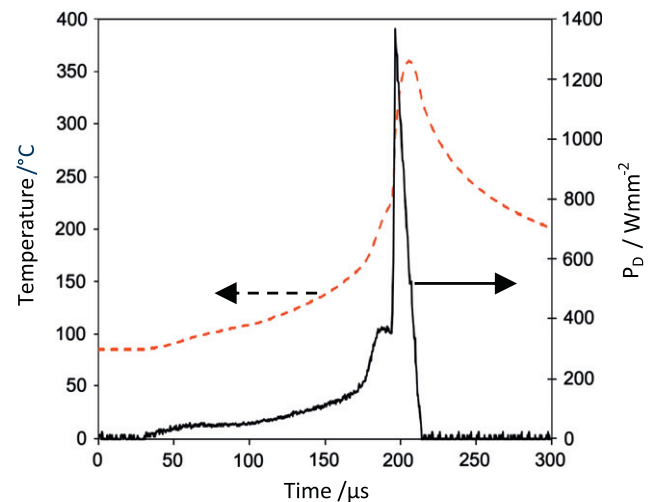


Fig. 8. Power dissipation P_D and temperature as a function of time for a smart power high side switch under short circuit conditions [17].

degradation of the metallization and Fig. 5b the local melt-up caused by a short between the source and drain metal.

Temperature swing ΔT is probably the most prominent factor influencing the degradation. This dependence is depicted in Fig. 6. Number of cycles to fail of a PowerMOSFET under repetitive unclamped inductive switching is shown as a function of ΔT . Lower temperature swing means higher number of cycles. A change in behavior can be observed below a ΔT of 120 °C. The reason lies in the temperature dependence of the yield strength of the metal.

Cycles to fail are also dependent on the pulse length, as can be observed from Fig. 7. Data were obtained from stress of a dedicated test structure, which has been described elsewhere [20]. The test structure has a poly heater, so that no current is flowing through the metal layer itself.

Short circuit of high side switches is among the harshest stress conditions that devices can experience. Fig. 8 illustrates the high power dissipation due to the short circuit event and the high peak temperatures that is caused by this power dissipation [17].

8. Lifetime modeling

The most obvious factor causing degradation is the temperature swing ΔT , caused by the current/voltage pulse. The lifetime is then modeled with a Coffin-Manson type of equation.

$$N_f = A \cdot (\Delta T)^c, \quad (1)$$

where N_f is the number of cycles to fail, A is a constant, ΔT is the temperature swing and c is a constant that is somehow related to the material properties [21]. This approach or some extensions of it (e.g. Norris-Landzberg type of models [22]) have been commonly used.

Bayerer et al. [23] have published an analytical model for lifetime calculation of power cycling of IGBTs that includes several factors. This model has been fitted to a large amount of data. However, the factors used are not independent. For instance, current and temperature are connected. This model needs a database over a wide range of conditions to allow for interpolation.

Ciappa has proposed a method to calculate the lifetime of a device starting from a mission profile [24].

There are several factors besides temperature swing that have an influence on the degradation. One rather obvious factor is the base temperature. As the yield strength of metals is temperature dependent, it is clear that the temperature excursions can cause the mechanical stress to exceed the yield strength, thereby inducing plastic deformation.

It is well known that plastic deformation is quite complex. Work hardening and Bauschinger effect [25] have to be taken into account for modeling cycle fatigue behavior. Also pulse duration has been observed to have an influence and the role of strain rate dependencies is not fully understood.

None of the published models so far fully captures the physics of the failure mechanism. The basic problem of a lifetime model for active cycling is the predictive capability for different types of stress conditions, including cumulative effects of different loads. What one would wish for is a damage accumulation model for the metal degradation taking into account the relevant factors. This is a really daunting task. It implies an electro-thermal simulation to obtain the time-dependent temperature distribution on the power device, a coupling of the electro-thermal simulation to a thermo-mechanical simulation to obtain the distribution of the mechanical stress, and a thorough knowledge of the behavior of the different materials involved (constitutive models). The simulation has to be calibrated to experimental data. These data are not only end-of-life distribution, but parameters that characterize the time-dependent damage accumulation of the system.

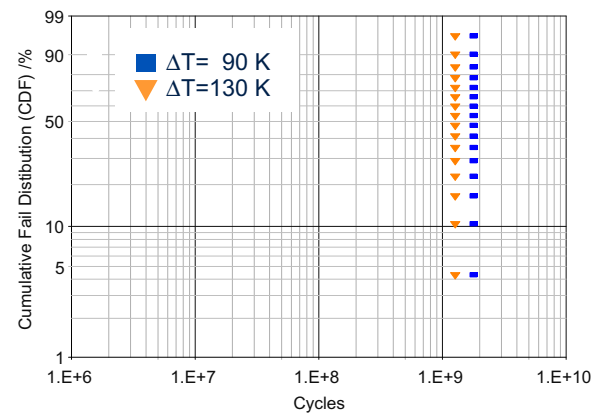


Fig. 9. Repetitive clamping of a smart power device with more than 1 billion cycles.

Accelerated testing is a well-established way to obtain lifetime assessments by extrapolating from time to fail distributions under stress conditions to time to fail distributions under use conditions. One fundamental boundary condition of accelerated testing is that the failure mechanism must not change. Fig. 9 shows data of an integrated power device under mildly accelerated stress conditions. More than 1 billion of cycles were tested without any fails (naturally on a limited number of samples). Two specific pulse conditions were applied, one with a temperature swing of 90 K and a second one with a temperature swing of 130 K. Both had a pulse duration of 0.5 ms. It has to be emphasized that each of the test groups took more than 4 months test time. Significantly higher acceleration will induce a different failure mechanism. This sets limits to the acceleration that one can obtain. Although application conditions may vary substantially, it is obvious that testing a wide parameter range of these conditions is not feasible.

The problem is further exacerbated by the requirement of different load conditions even in one specific application, implying that one has to deal with cumulative effects of varying cycling conditions. The Palmgren–Miner rule is widely applied to sum the effects of different cycling conditions. It is based on the assumption of linear damage accumulation, meaning that the sequence of loads does not affect the overall result. This is an assumption that awaits experimental and theoretical justification.

9. Conclusions

Reliability assessment of power devices is a challenging task. Although the underlying failure mechanism of metal degradation can be clearly related to plastic deformation of the metal, modeling of the lifetime is impeded by a lack of detailed physical understanding of the failure mechanism and the multitude of parameters that influence the degradation behavior.

Reliability testing itself is a complex task requiring dedicated equipment. Testing of a high number of cycles requires long test times of the order of several months. This implies that testing of a wide range of application conditions is not feasible.

Lifetime models are empirical, but end-of-life data are needed as a foundation of these models. A physical damage model is what one would wish for but a tremendous amount of work is needed to achieve this end. Improvement of empirical and semi-empirical models is needed for better reliability assessment, but meets with substantial difficulties, among them being the need to generate a comprehensive base of test data.

Active cycling of power devices remains a challenge for reliability assessment that needs substantial effort of the semiconductor industry and scientific institutes.

Acknowledgements

The author wants to express his special thanks to Dr. Michael Nelhiebel, Dr. Reinhard Pufall, and Dr. Andreas Spitzer for many intensive discussions on the subject.

References

- [1] Kanert W. Reliability challenges for power devices under active cycling. In: Proc 47th IRPS; 2009. p. 409–15.
- [2] Schlangen R et al. Dynamic lock-in thermography for operation-mode dependent thermally active fault localization. *Microelectron Reliab* 2010;50:1454–8.
- [3] Pfost M, et al. Measurement and simulation of self-heating in DMOS transistors up to very high temperatures. In: Proc ISPSD; 2008. p. 209–12.
- [4] JEDEC JESD22-A108. Temperature, bias, and operating life.
- [5] JEDEC JESD47. Stress-test-driven qualification of integrated circuits.
- [6] Automotive Electronic Council (AEC) Q100. Failure mechanism based stress test qualification for integrated circuits.
- [7] JEDEC JESD22-A105. Power and temperature cycling.
- [8] MIL-STD-750. Method 1037.
- [9] Automotive Electronic Council (AEC) Q101. Stress test qualification for automotive grade discrete semiconductors.
- [10] Automotive Electronic Council (AEC) Q100-012. Short circuit reliability characterization of smart power devices for 12 V systems.
- [11] Automotive Electronic Council (AEC) Q101-006. Short circuit reliability characterization of smart power devices for 12 V systems.
- [12] IEC 60747-2, 9.
- [13] Hensler A, et al. Power Cycling Tests at High Temperatures with IGBT Power Modules for Hybrid Electrical Vehicle Applications. In: ESTC; 2010.
- [14] Glavanovics M et al. Flexible active cycling stress testing of smart power switches. *Microelectron Reliab* 2007;47:1800–4.
- [15] Ciappa M, Malberti P. Plastic-strain of aluminium interconnections during pulsed operation of IGBT multichip modules. *Qual Rel Eng Int* 1996;12:297–303.
- [16] Russo S et al. Fast thermal fatigue on top metal layer of power devices. *Microelectron Reliab* 2002;42:1617–22.
- [17] Nelhiebel M et al. A reliable technology concept for active power cycling to extreme temperatures. *Microelectron Reliab* 2011;51:1927–32.
- [18] Pietranico S et al. A study of the effect of degradation of the aluminium layer in the case of power semiconductor devices. *Microelectron Reliab* 2011;51:1824–9.
- [19] Azoui T et al. 3D Electro-thermal modeling of bonding and metallization ageing effects for reliability improvement of power MOSFETs. *Microelectron Reliab* 2011;51:1943–7.
- [20] Smorodin T. Modellierung von Schädigungsmechanismen in Metallisierungsschichten unter schneller Temperaturwechselbelastung. Ph.D. thesis. Freiburg, Germany; 2008.
- [21] JEDEC JEP122. Failure mechanisms and models for semiconductor devices.
- [22] Norris KC, Landzberg AH. Reliability of controlled collapse interconnections. *IBM J Res Dev* 1969;266–71.
- [23] Bayerer R, et al. Model for Power Cycling lifetime of IGBT Modules – various factors influencing lifetime. In: CIPS; 2008.
- [24] Ciappa M. Lifetime prediction on the base of mission profiles. *Microelectron Reliab* 2005;45:1293–8.
- [25] Xiang Y, Vlassak IJ. Bauschinger and size effects in thin-film plasticity. *Acta Mater* 2006;54:5449–60.