Method for Electrical Detection of Bond Wire Lift-Off for Power Semiconductors

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Abstract. A novel approach is presented for detecting bond wire lift-off in power semiconductor devices while they are in operation. The aim is to improve the reliability of power electronic systems. The method comprises a specific bond assembly and an integrated subcircuit as part of the gate driver [1], and serves to detect bond wire lift-off in parallel switched power devices, a typical end-of-life phenomenon encountered in modules, which results in loss of contact and therefore of controllability. The former is detected and the system is prevented from going abruptly into failure mode, so that the destruction of devices is safely avoided.

INTRODUCTION

The beginning of the end-of-life stage is marked by an increase in the failure rate. Fig.1 shows the typical reliability bathtub curve with its three characteristic sections. The *early-life failure* characteristic depends on the actual design, materials, devices and technology. It can also be influenced by quality assurance activity such as stress testing, burn-in, and measurement under harsh conditions. *Statistical failures* in the middle phase of the lifetime can be managed by intelligent control and monitoring concepts. A great problem, still not solved by the known protection concepts, is the loss of electrical contact to the power devices during the *end-of-life* phase, which will inevitably result in loss of controllability. Predictions about reliability parameters such as failure mechanisms, failure modes and estimated lifetime can be made by extracting data from accelerated lifetime tests. These typically reveal damage to the chip assembly in power devices or modules entering the end-of-life stage – damage caused by mechanical stress imposed on the module by temperature cycles. Moreover, power semiconductor modules subjected to these accelerated lifetime tests show a visible alteration of certain parameters (drift indicators), examples being an increase in thermal resistance or increased collector emitter saturation voltage [2]. Fig. 2 shows the results of an active power cycling test of a SKiiP3 IGBT module with 14 IGBT chips in parallel per switch. Such tests also allow categorization of failure mechanisms and failure modes.

The steady increase of maximum junction temperature $T_{j,max}$ in Fig.2 is due to a rise in thermal resistance due to degradation of soldering.

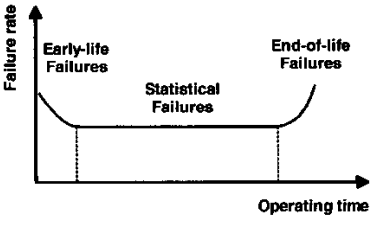

Fig.1 Reliability bathtub curve

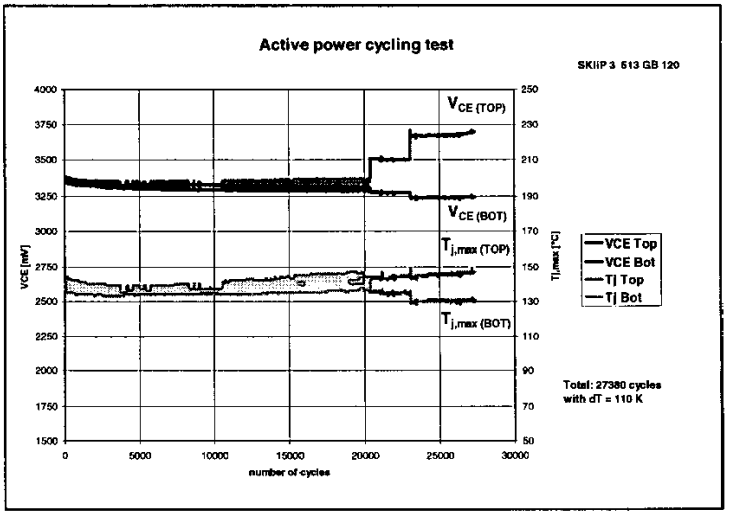

Fig.2 End-of-life indicator V_{CEsat} and $T_{j,max}$ and failure mode - bond wire lift-off

In contrast, the jump-up of the collector-emitter saturation voltage V_{CEsat} in Fig.2, is caused by bond wire contact loss in one or more of the parallel switched IGBT chips.

For end-of-life failures, both damage to the chip solder and bond wire lift-off are characteristic. Fig.3 shows an IGBT chip with lifted-off emitter bond wires after the active power cycling test.

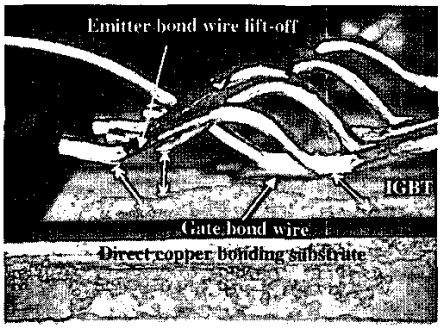

Fig.3 End-of-life failure mode – bond wire lift-off

DETECTION METHOD: ASSEMBLY TECHNIQUE AND SENSOR SIGNAL DERIVATION

It is difficult to process the well-known failure indicators, R_{th} and V_{Cesat}, in real-life power converter applications. Therefore, we followed the approach of taking bond wire lift-off as an indicator that the end of lifetime is approaching.

For the practical implementation of the diagnostic strategy here described, redundant structures are crucial because they still allow the system to operate, even if an individual unit actually fails. In the case of a high power IGBT module, active redundancy will be automatically implemented during assembly because of parallel emitter bond wires and/or parallelisation of chips. Detection of bond lifting does call for the modification of the assembly and of the DCB layout.

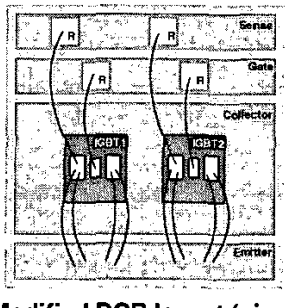

Fig.4 Modified DCB layout (simplified)

As can be seen in Fig.4, the IGBT collector is conventionally contacted by soldering; both emitter and gate are contacted by bond wires to the DCB substrate. What is new is the use of an additional bond wire which connects the emitter pad of every parallel IGBT through a resistance to an additional contact area (labelled Sense) on the DCB substrate. This bond wire does not conduct the emitter current in normal operation because of its higher impedance, but it does make sure the chip retains some controllability and is not damaged even if all the standard emitter-bonds lift off. The extra bond wires to all the IGBT emitters are grouped together by means of low ohmic resistors either placed on DCB or integrated monolithically into the IGBT. The midpoint of the resistor sub networks (Sense) is fed into control circuitry which can be part of the gate driver. Fig.5 shows a practical implementation of this assembly structure for a module with four IGBTs in parallel. The equivalent electrical network is represented in Fig. 6a (only two IGBTs drawn).

If the bond wire contact to the IGBT emitter is lost as a result of bond wire lift-off (in the equivalent network shown in Fig.6b this is IGBT1), controllability of the affected chip will nevertheless be maintained, as the resistor network implemented will take over the role of ensuring a low ohmic coupling between the IGBT emitter and the controlling gate driver.

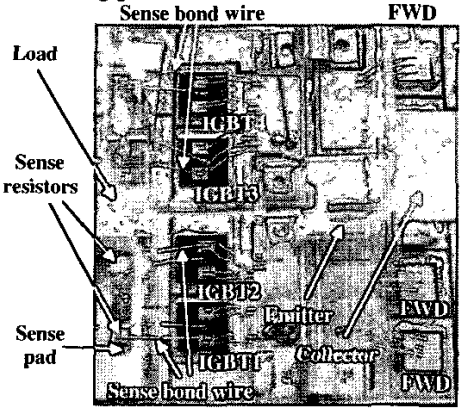

Fig.5 Modified IGBT module (Semitrans 3)

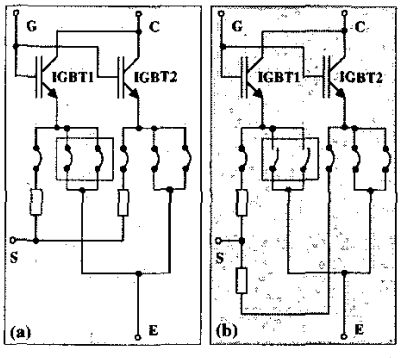

Fig.6 Equivalent circuit (a) without and (b) with emitter bond lift-off at IGBT1

The resulting feedback in the emitter branch is advantageous because it automatically means that IGBT1 has a considerably reduced collector on-state current. The midpoint of the resistor network (Sense) carries a sensor signal which, being strong enough and close to the emitter potential, is analysable.

Fig.7 indicates the different characteristics of the sense emitter voltage V_{SE} with and without bond wire lift-off. The signal is about 0.7V and relatively independent of the values of actual sense resistances and of the collector current. Integrated comparators can be used by the monitoring circuitry to evaluate this sensor signal.

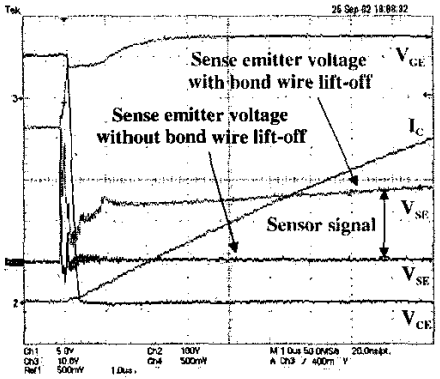

Fig.7 Measurement results – Sense signal

MONITORING CIRCUIT

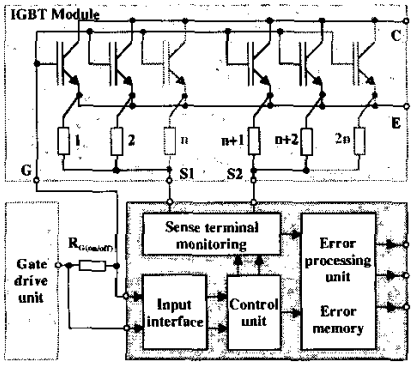

Fig.8 Block diagram of the bond wire lift-off detection system

A block diagram of the resulting detection system is shown in Fig.8. The IGBT switch consists of several parallel-switched IGBTs which are separated into two groups, each of which needs only one Sense contact (here S1 or S2), connected to the monitoring circuit.

Fig.9 shows a block diagram of the monitoring circuit. The main functionality is that two of four comparators monitor a terminal each, "SENSE1" (S1) and "SENSE2" (S2). The comparators detect a conductivity loss if all emitter bond wires of a particular chip lift off. Furthermore, the system also monitors the integrity of the sense bond wire. Here, any sense bond wire is checked separately, ensuring the diagnostic function is also guaranteed if the sense bond wires should lift-off first.

Depending on whether the system checks for emitter bond failures or sense bond failures, the signals V_{SE} (see Fig.7) or V_{S1S2} (see Fig.8) respectively are evaluated by dedicated hysteresis-comparators. The monitoring of emitter bond wire failures is enabled only during the on-state of the IGBT, because only then does a current flow through the emitter connections and make generation of a bond wire lift-off sensor signal possible. The monitoring of sense bond wires, in contrast, will be enabled only when the IGBTs are in the off state. To check the sense connection, a current source (labelled CS in Fig.9) will be turned on and the values of the resistances in each branch SENSE1 and SENSE2 will be compared. Both branches in combination form a Wheatstone bridge. The output signal is close to zero as long as both branches are symmetrical and no sense bond wire has lifted off. In order to limit the extra power dissipation due to CS, the current source is operated in pulsed mode. The pulse width and thus the average current may be made adjustable by an external capacitor at the Pin CTCS.

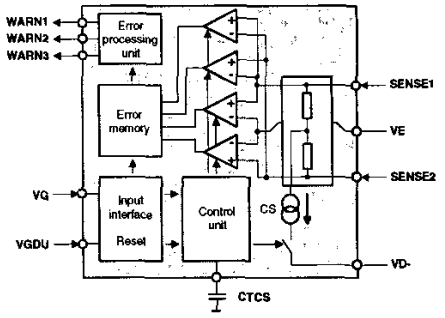

Fig.9 Block diagram of the bond wire lift-off monitoring circuit

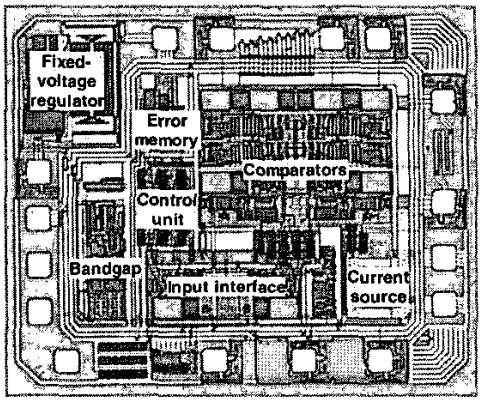

Fig.10 Chip photography of the bond wire lift-off monitoring circuit

A dedicated timing control for the comparators is mandatory to achieve high EMI immunity. The timing control and the generation of a reset-signal are based on the timing of the gate emitter voltage VG and the digital output signal of the gate drive unit GDU. With these data is it possible to disable the comparators during the switching transients of the IGBTs. This is beneficial for detection precision because of the exclusion of IGBT switching noise from the sensor

signals. If a bond failure is detected, an error signal will first be sent to the gate driver, which turns off the IGBT, and then on to the microcontroller. The error processing unit generates a specific error pattern at the external outputs (WARN1, WARN2 and WARN3) for any failure detected. Thus the origin of any bond wire failures (emitter or sense connection) is transparent to the user.

The lift-off detection topology described above can be implemented as an integrated circuit which is part of a gate driver IC [3]. Fig.10 shows the chip photography of the detection system realised in a high voltage CMOS technology (V_{BREAK} approx. 50V, feature size 1µm, 12 masks, double metal).

MEASUREMENT RESULTS

Fig.11 and 12 show sample measurements of a bond wire lift-off monitoring circuit realised as an IC.

In Fig.11, the correct behaviour is shown of the monitoring circuit in the case of a conductivity loss of all emitter bond wires to one IGBT chip at the terminal SENSE2. With the beginning of the turn-on process of the IGBT, as can be seen from the rising edge of V_{GE}, an internally generated reset-signal sets all error flags WARN1, WARN2 and WARN3 to logic low level (pattern 000). As soon as the IGBT turn-on process is completed, the monitoring function will be enabled and thus the comparators can detect a potential emitter bond wire lift-off failure at terminal SENSE2. The error processing unit generates error signal patterns at the external outputs. The Figure illustrates a case of all the external error flags, WARN1, WARN2 and WARN3, changing from low to high levels (pattern 111). When the IGBT is in the off-state, the error signals are stored and held until a reset signal is initiated at the next V_{GE} turn-on edge.

While Fig.11 showed the behaviour of the monitoring system in the case of an emitter bond wire failure, Fig.12 depicts measurement results of detection of sense wire lift-off. A contact loss is present for the SENSE1 terminal in the measurement setup.

The described method for checking the conductivity of the sense bond wires by analogy with a Wheatstone bridge requires a relatively high test current through the sense bond wires. The detection of a sense wire conductivity loss is challenging because of the low-ohmic conditions in each sense branch. For this reason, as mentioned before, the on-state duration of the current source should be restricted. The sample of Fig.12 shows an on-state duration of approximately 15µs, derived from the controlling voltage V_{CTCS} rising from zero to a predefined threshold. During this interval the current through CS is nearly constant. The turn-off of the current source, caused by the falling edge of V_{CTCS}, resets an internal counter and subsequent sense bond testing will be enabled only at every 240th IGBT turn-on process in order to decrease the average current consumption of CS even further.

A detected sense bond wire failure will be stored, independently of the turn-off of the current source CS and can be transferred to the error memory of the gate driver [4]. The detection unit will be reset by the next turn-on edge at V_{GE}.

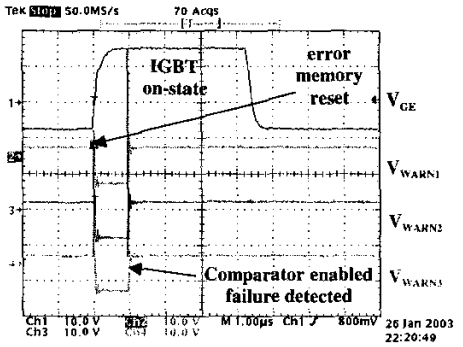

Fig.11 Measurement results – error flags after emitter bond wire lift-off at SENSE2

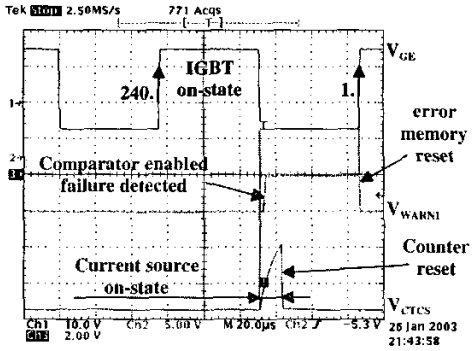

Fig.12 Measurement results – detection of sense bond wire lift-off at SENSE1

CONCLUSION

The topology for detecting bond wire lift-off, and the implementation of the diagnostic system into an integrated circuit, as presented here, provide an opportunity to detect end-of-life failures in power semiconductor devices in advance. This enables system designers to implement diagnostic functionality as an integral part of power semiconductor solutions.

REFERENCES

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