GaN-on-Si Failure Mechanisms and Reliability Improvements

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Abstract

The degradation of 36mm AlGaN/GaN HFETs-on-Si under DC stress conditions has been studied on a large number of nominally identical devices that were chosen randomly across a production process. A common and primary degradation phenomenon was observed in the devices. A combination of electrical and physical analysis was used to identify a possible failure mechanism related to the Ni/Au Schottky gate diode that appears to explain the degradation of the FET. Based on the analysis, a gate anneal step was added into the fabrication process of AlGaN/GaN HFETs-on-Si. Nominal devices processed using a gate anneal showed (a) a modified gate metal-semiconductor interface (b) forward diode characteristics that are unchanged upon stress and (c) improvement in overall reliability relative to control devices.
Keywords - AlGaN/GaN HFETs, GaN high electron mobility transistors (HEMTs), RF power transistors, reliability, failure analysis.

Introduction

GaN has been the focus of a number of recent results benchmarking the capability of GaN for high power RF applications [1, 2, 3]. The unique attributes of GaN-based devices are highly suited for a number of commercial and military markets, including cellular infrastructure, broadband wireless access, radar and communications applications. Now that the performance of the devices are reaching the required levels for some of the applications, a key remaining question for both markets is the reliability of the technology and the understanding of key failure mechanisms. Only recently are results for GaN device reliability being reported [4, 5, 6].

GaN-on-Si HEMTs, in particular, have seen rapid progress towards commercial readiness. The highlights include: high power densities on small-periphery devices [7]; repeatable high total power on large-periphery devices [8]; and complete characterization of large-periphery device reliability [9]. The availability of reliable large periphery GaN-on-Si devices has lead to the introduction of this technology into commercial applications. However, as part of the continuing effort to understand and improve reliability, failure analysis is preformed on these process-nominal GaN devices. In this paper, we report on one of the failure mechanisms along with a modified gate processes to further improve reliability of GaN-on-Si power devices.

Device Overview

Devices reported in this work are based on AlGaN/GaN heterostructures grown on high resistivity Si (111) substrates by metal organic chemical vapor deposition (MOCVD). A stress mitigating transition layer is used to grown a crack-free GaN buffer layer on the Si substrate [10]. Subsequently, an $Al_{0.26}Ga_{0.74}N$ device layer and thin GaN cap layer are grown. The gate structure is a 0.7µm dielectrically defined T-gate consisting of Ni/Au metallization. Ohmic contacts are Ti/Al/Ni/Au and are annealed at ~850°C. Source and drain fingers are subsequently plated with Au during which the source fingers are airbridged. Devices are passivated and encapsulated with PECVD deposited SiN_x. All devices in this study have a gate-to-source spacing of 1µm and gate-to-drain spacing of 3µm. Detailed descriptions of the process have been provided elsewhere [11,12].

Reliability Background

The reliability performance of the current baseline technology has been extensively characterized by sampling six wafers randomly from a 150-wafer baseline distribution and subjecting them to a complete battery of tests [9]. The test vehicle consisted of a transistor die attached to high–thermal-conductivity CuW single-ended, ceramic packages using AuSi eutectic process. The package was lidded with a non-hermetic epoxy sealed lid. The sources were grounded to the package base by way of substrate vias in the 150µm-thick silicon wafer. Internal matching networks were used to transform both the input and output to higher impedances. These devices typically deliver 60-70W of CW saturated output power along with 60-65% efficiency at an operating voltage of 28V and frequency of 2.14GHz [8].

Building on the findings thus far, this work focuses on the DC stress data and subsequent failure analysis to assess the root cause for parametric degradation under stress. Key DC results include 3-temperature (260°C, 285°C & 310°C) data showing an exponential relationship between current drift and junction temperature (T_j). High temperature operating life (HTOL) data from a fourth T_j of 200°C is also overlaid and exhibits consistent behavior with the 3-temperature data. In all cases, devices were stressed at Vds of 28V and Ids of 2.3A with the ambient temperature adjusted to achieve the desired T_j. Fig. 1 shows the Arrhenius plot from which (a) an activation energy (Ea) of 1.7eV and (b) a mean time to failure (MTTF) > 10^7 hours when operated at T_j of 150°C, were extracted.

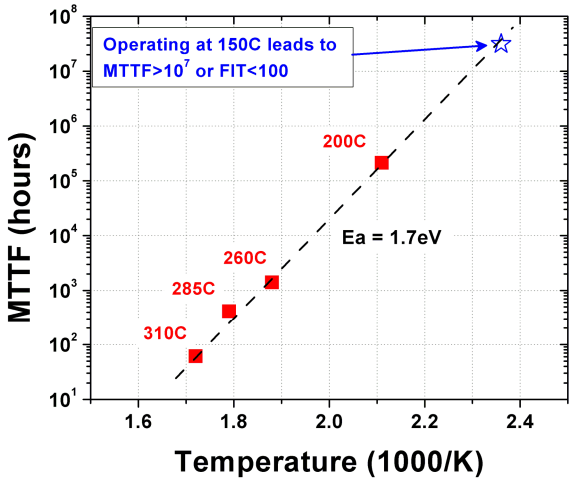

Fig. 1: Arrhenius Plot showing Ea=1.7eV and MTTF > 10^7 hours at 150°C.

Fig. 2 shows the median saturated drain current (Idss) for 30 HTOL samples measured at multiple test intervals from which an extrapolated 20-year degradation of 15% at a Tj of 200°C was predicted. Application of an acceleration factor (Ea=1.7eV) results in an expected 20-year Idss drift of ~5% at a Tj of 150°C. The DC stress tests not only demonstrate low drift rates, but also show consistent drift characteristics, which are helpful in determining failure mechanisms.

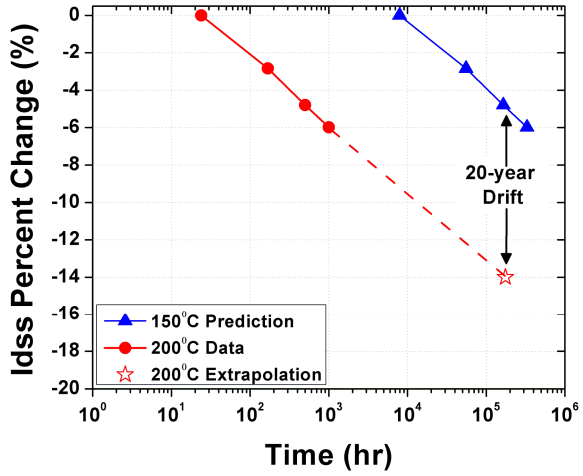

FIG. 2: IDSS EXTRAPOLATION OUT TO 20 YEARS.

FAILURE ANALYSIS

The 30 HTOL samples previously described created an excellent set of devices on which to perform failure analysis. The failure analysis plan consisted of both electrical and physical characterization. The first step entailed taking a closer look at the I-V FET transfer curves. This electrical analysis revealed an increase in pinch-off voltage (Vp) with time of stress that seemed to be consistent with the Idss degradation. This phenomenon is illustrated in Fig. 3, which shows the magnitude of Vp increasing after stress. A proposed explanation for this Vp shift was a permanent Schottky barrier height (SBH) increase.

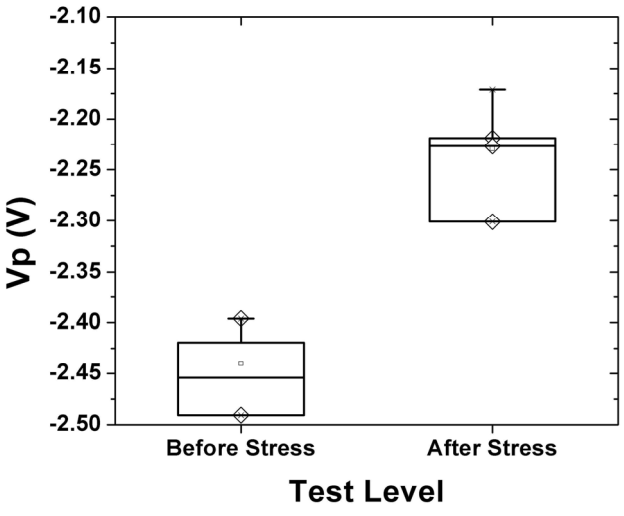

FIG. 3: VP SHIFT DURING HTOL STRESS

Physical analysis was performed on both unstressed and stressed (1000 hours, HTOL) devices using FIB (focused ion beam) and STEM (scanning tunneling electron microscopy) techniques. Upon close examination of the images, it was discovered that there was an interfacial layer between the gate and the semi-conductor on unstressed samples, which seemed to be modified on the stressed samples as seen in Fig. 4. It is quite possible that the modification of this interfacial layer due to stress may have caused the SBH to increase, thereby resulting in a corresponding shift in Vp and hence, Idss.

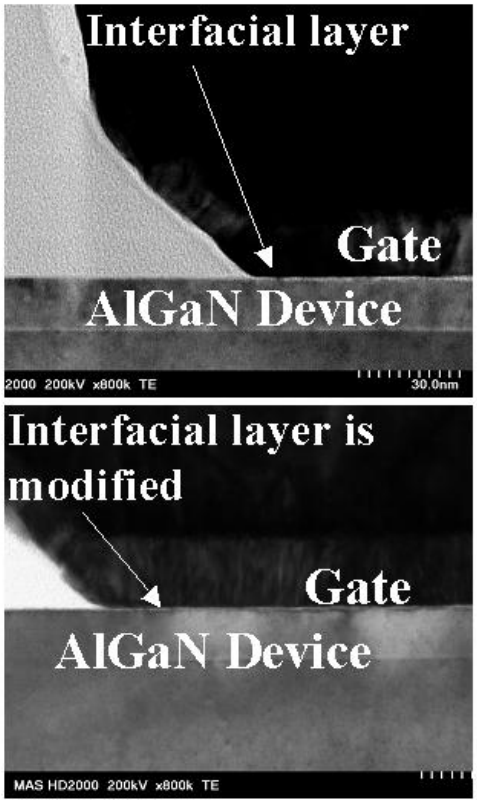

FIG. 4: STEM PICTURES OF UNSTRESSED (TOP) AND STRESSED (BOTTOM) SAMPLE SHOWING CHANGE IN INTERFACIAL LAYER AFTER STRESS.

Automated DC test plans were designed to study this phenomenon and provide feedback for potential process improvements. In this test, the forward diode characteristics for several single-finger 100µm devices were obtained on-wafer. These devices were then stressed for an hour under conditions similar to the HTOL test (28V with Ids adjusted to provide T_j of 200°C). The forward diode curves were then re-measured. Through such a sequence, it was confirmed that the SBH did indeed increase after stress as shown in Fig. 5.

The stress due to device operation leads to a positive shift in SBH and a corresponding negative shift in Idss. In fact, after the stress the interfacial layer is reduced leading to a more ideal diode with a higher SBH, both of which are positive attributes of any Schottky diode. While the positive shift in SBH is a positive attribute of the gate in general, the corresponding change in Idss of the FET due to stress is undesirable. The preferred scenario is to remove the interfacial layer during fabrication (i.e., stabilize and idealize the Schottky diode) and induce the SBH shift during the wafer fabrication process and not during device operation.

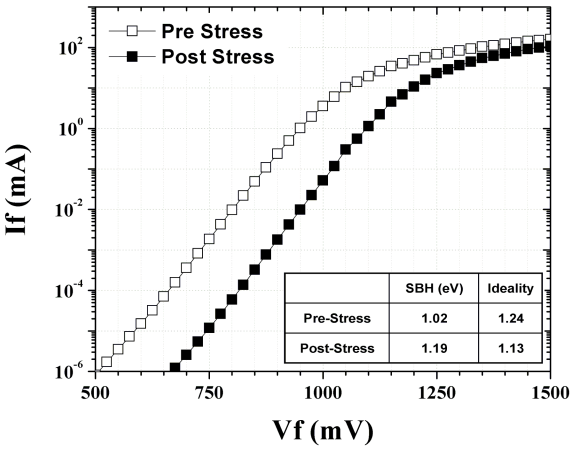

FIG. 5: PCM FORWARD DIODE MEASUREMENT ON UNANNEALED GATE SHOWING SIGNIFICANT SHIFT AFTER STRESS.

PROCESS IMPROVEMENTS

In order to reduce the effect of the interfacial layer, an annealing step was added to the gate fabrication process. This creates a more ideal semiconductor-metal interface under the gate before device operation and stress. FIB and STEM images were used to confirm the improved interface. In the experiment a wafer was chosen and FIB cuts were taken on three gates from different areas on the wafer before gate anneal. Then, following the gate anneal, three more FIB cuts were taken from the same area on the wafer. STEM images of a typical device before and after gate anneal are shown below in Fig. 6 and reveal a similar modification to the interfacial layer as seen during HTOL stress.

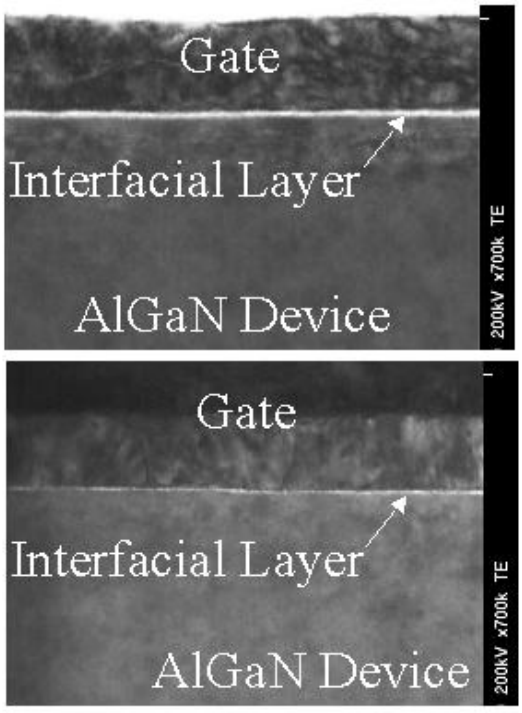

FIG. 6: STEM PICTURES OF DEVICE BEFORE (TOP) AND AFTER (BOTTOM) GATE ANNEAL SHOWING CHANGE IN INTERFACIAL LAYER WITH ANNEAL.

Electrical confirmation was provided by using the same automated DC test plan, previously discussed, on single-finger 100µm devices fabricated with this new process and those results are shown in Fig. 7. From Fig. 7, two observations can be made: (1) the SBH value is greater in magnitude with the modified gate process and (2) the diode is stable with stress.

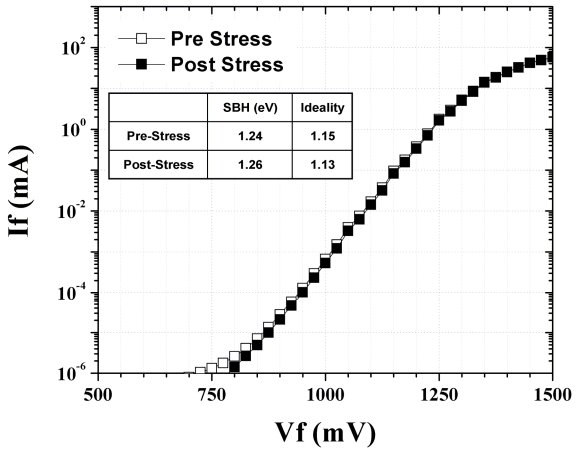

FIG. 7: PCM FORWARD DIODE MEASUREMENT ON ANNEALED GATE SHOWING NO CHANGE AFTER STRESS.

INITIAL RELIABILITY RESULTS

The new gate process was added to the fabrication process of 36mm packaged die in order to determine the Idss drift under HTOL test conditions described previously (T_j=200°C, Vds=28V, Ids=2.3A). A controlled experiment was set up where one wafer was processed with no anneal and one wafer received the gate anneal. Ten devices were selected from each wafer with the different gate processes and were packaged and stressed. The comparative results are plotted in Fig. 8 and show a dramatic reduction in Idss change over time relative to the old gate process. Specifically, devices with the gate anneal degraded 50% less during the first 24 hours relative to the devices without the anneal.

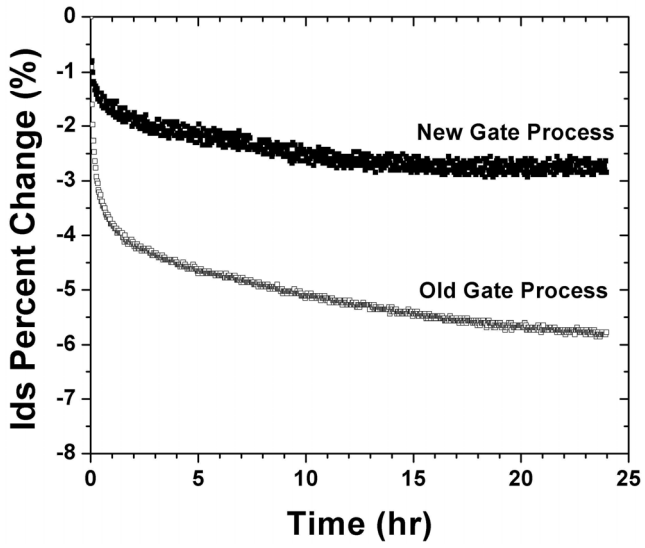

FIG. 8: RESULTS FROM 24-HOUR HTOL TEST SHOWING IMPROVED PERFORMANCE WITH GATE ANNEAL PROCESS.

In Fig. 9 the data is re-plotted on a log scale and shows that both degradation trends follow a logarithmic drift model. Extrapolating the results reveals 20 year operating lifetime drift at 200°C of just 6% for gate annealed devices versus 12% for un-annealed devices. These initial reliability results look very promising and more statistical, longer-term HTOL and three-temperature testing will be performed and the results will be reported elsewhere.

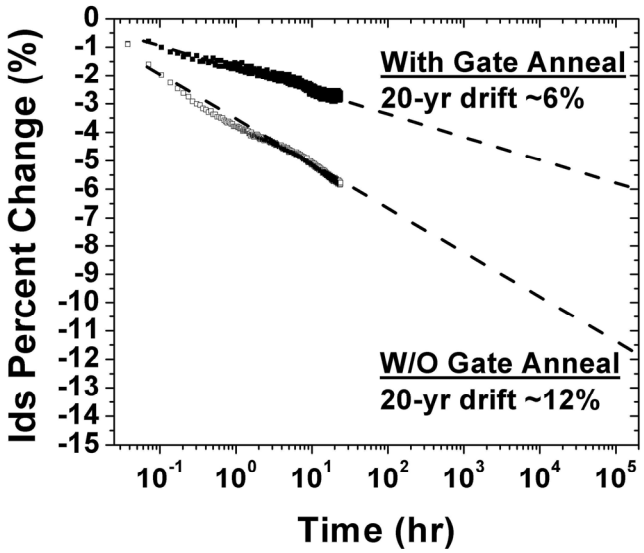

FIG. 9: LIFETIME PREDICATION FROM 24-HOUR HTOL TEST SHOWING DRIFT OVER 20 YEARS OPERATION AT V_{DS}=28V AND T_J=200°C.

CONCLUSION

In summary, failure analysis was performed on DC stressed samples by a combination of electrical (IV curves) and physical (FIB, STEM) techniques. The failure analysis effort led to the discovery of a thin interfacial layer under the gate. This interfacial layer was diminished with stress causing a SBH shift. A new gate process was inserted into the fabrication flow and results show negligible SBH shift and a dramatic improvement in the large-periphery HTOL results. This is believed to be the first example of a failure analysis effort and subsequent reliability improvement on GaN devices.

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