# A Literature Review of IGBT Fault Diagnostic and Protection Methods for Power Inverters

Bin Lu, *Senior Member, IEEE*, and Santosh K. Sharma

***Abstract*—This paper presents a survey on existing methods for fault diagnosis and protection of insulated gate bipolar transistors with special focus on those used in three-phase power inverters. Twenty-one methods for open-circuit faults and ten methods for short-circuit faults are evaluated and summarized, based on their performance and implementation efforts. The gate-misfiring faults and their diagnostic methods are also briefly discussed. Finally, the promising methods are recommended for future work.**

***Index Terms*—Fault diagnosis, gate-misfiring fault, insulated gate bipolar transistor (IGBT), open-circuit fault, power inverter, short-circuit fault.**

## I. Introduction

VOLTAGE-SOURCE inverters (VSIs) are widely used in motor drive and power quality applications. It is estimated that about 38% of the faults in variable-speed ac drives in industry are due to failures of power devices [1]. Most of these inverters use insulated gate bipolar transistors (IGBTs) as the power device because of their high voltage and current ratings and ability to handle short-circuit currents for periods exceeding 10 $\mu$s. Although IGBTs are rugged, they suffer failures due to excess electrical and thermal stress that are experienced in many applications. IGBT failures can be broadly categorized as open-circuit faults, short-circuit faults, and intermittent gate-misfiring faults. Various IGBT fault diagnostic and protection methods have been developed during the last decade. The main purpose of this paper is to conduct a comprehensive review of these works.

## II. Gate-Drive Open-Circuit Fault

A gate-drive open-circuit fault may happen due to lifting of bonding wires caused by thermic cycling. It may be caused by a driver fault or a short-circuit-fault-induced IGBT rupture. Open-circuit faults lead to dc current offset in both the faulty and healthy phase. The interaction between the dc component and the field generates a pulsating torque at the stator current frequency, which may substantially reduce the maximum average torque available to the drive [2]. The dc currents also generate unequal stress in the upper and lower transistors. These effects may cause secondary faults in the inverter, motor, or load. The voltages and currents carry the fault signatures and hence can be analyzed to detect and locate the fault. Open-circuit faults generally do not cause system shutdown, but degrade its performance. Therefore, these diagnostic methods can be used in device-fault-tolerant systems.

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B. Lu is with the Innovation Center, Eaton Corporation, Milwaukee, WI 53216 USA (e-mail: binlu@ieee.org).

S. K. Sharma is with the India Engineering Center, Eaton Corporation, Pune 411014, India (e-mail: santoshkrsharma@eaton.com).

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TABLE I
Defect Transistor Localization by Park's Vector Method

| Transistor | Avg. Current Magnitude | Current Phase Angle (degree) |
|---|---|---|
| T1 | Exceeds Threshold | 150-210 |
| T2 | Exceeds Threshold | 210-270 |
| T3 | Exceeds Threshold | 270-330 |
| T4 | Exceeds Threshold | 330-30 |
| T5 | Exceeds Threshold | 30-90 |
| T6 | Exceeds Threshold | 90-150 |

### A. Detection Methods

*1) Park's Vector Method [3]:* In this method, open-circuit fault detection and defect transistor localization are accomplished by calculating the position of the current trajectory's midpoint, which is the mean value of the ac current space vector over one period.

First, the three-phase average currents are calculated. Then, Park's vector transformation is applied to obtain the magnitude and phase angle of the ac currents in the complex domain. For a normal system, the mean (magnitude) value is zero and the space vector trajectory is a circle. If a fault occurs, the magnitude of the space vector is nonzero and greater than a threshold. The defect transistor is identified by the phase angle, as shown in Table I.

*2) Normalized DC Current Method [4], [5]:* This is an improvement over the Park's Vector Method, which has a major drawback of being load dependent. To make the fault detection independent of load, normalized dc current is used and is given by

$$\gamma_{a,b,c} = \frac{I_{a,b,c_{\mathrm{av}}}}{\sqrt{\left(a^2_{1,(a,b,c)} + b^2_{1,(a,b,c)}\right)}} \tag{1}$$

where $I_{a,b,c_{\mathrm{av}}}$ is the average phase current, and $a_{1,(\mathrm{a,b,c})}$ and $b_{1,(\mathrm{a,b,c})}$ are the fundamental coefficients of the three-phase currents. This normalized value is calculated for each phase. To identify the faulty IGBT, the resulting residual, $\gamma_{\mathrm{a,b,c}}$ is compared with a threshold 0.45, reported to be a universal value derived from experience.

*3) Modified Normalized DC Current Method [4], [5]:* The normalized dc current method has some drawbacks when implemented in a closed-loop control scheme. The modified normalized dc current method uses the same algorithm and, however, employs a less restrictive way to localize the faulty switch. To prevent multiple satisfying conditions, only the largest absolute value among $\gamma_{\mathrm{a}}$, $\gamma_{\mathrm{b}}$, and $\gamma_{\mathrm{c}}$ is compared with the threshold 0.45.

*4) Slope Method [6]:* For fault detection, the slope $\Psi$ of the diameter of the current space vector trajectory is used and is defined as

$$\Psi = \frac{i_{d_k} - i_{d_{(k-1)}}}{i_{q_k} - i_{q_{(k-1)}}} \tag{2}$$

where $i_{d_k}$ and $i_{q_k}$ are the sampled $d$-axis and $q$-axis current components, respectively. The trajectory is calculated by the Park's vector transformation of the currents. Its slope is used to identify the faulty leg and the missing half-cycle of the current waveform is used to localize the faulty switch.

*5) Simple Direct Current Method [4], [5]:* This uses the mean phase current value for fault detection. The largest of the three-phase dc current values (absolute) is compared with a threshold to identify the faulty leg. The faulty switch is localized by the polarity of the mean value.

*6) AC Current Space Vector Instantaneous Frequency Method [6]:* This diagnostic method for open-circuit faults is based on the instantaneous frequency. During open-circuit fault, the frequency of the current space vector is zero on the diameter of the semicircle. To detect the fault, it is sufficient to test whether $f_{\mathrm{i}}$ is lower than a threshold. This method detects an open-circuit fault but does not isolate the faulty transistor.

*7) Comparison of AC Voltage Actual and Reference Quantity Approach in Time Domain [1], [7]:* This method uses techniques that require the measurement of the voltages and are based on the analytical model of the VSI. The technique is developed to minimize the time between the fault occurrence and diagnosis. The analysis is based on the fact that fault occurrence introduces errors in the phase voltages in comparison to its normal operation. The detection techniques employ a direct comparison of the measured values with their reference voltages obtained from the pulse-width modulation (PWM) reference signals. The techniques are classified based on the measured parameters, such as the inverter pole voltage, machine phase voltage, system line voltage, and machine neutral voltage. The error between the reference voltage and the measured value is used to detect the fault and identify the faulty switch. Detection times of one-fourth of a period have been reported achieved.

*8) Diagnosis by Sensing Voltage Across Lower Switch [8]:* This method is based on the fact that during open-circuit fault the voltage across the lower switch is around half the bus voltage. Normally, this voltage is either zero or full bus voltage. The detection scheme contains op-amp based voltage conditioning circuit and fault detector using flip-flops. Detection times of around 2.7 ms have been reported achieved in simulation.

*9) Centroid-Based Fault Detection [9]:* In this method, fault location and type are identified by determination of the centroid. The algorithms use pattern symmetry across the positive and negative $\alpha-\beta$ axes after the three-phase currents are transformed from abc to $\alpha\beta$ plane using Concordia transform. An open-switch fault is declared if a nonabsolute value of the centroid is not at the origin.

*10) Current Pattern Recognition Method in Time Domain [10]:* In this method, the fault modes of the inverter system are completely characterized by the patterns of the current waveform in time domain. The pattern characteristic is defined by parameters, such as the dc value, the polarity of the average current value in the first quarter of a complete period and in the second period. Each one can be equal to, greater, or lower than zero. In case of a semiconductor fault, 9 out of 27 parameters, called flags, are set in a special way to detect the fault.

*11) Converter Behavior Rules Diagnosis in Time Domain [11]:* This method is based on the measured dc bus current in each leg, the ac currents, and voltages. As the dc current of each leg is difficult to measure, its virtual quantity is calculated by using Kirchhoff's laws for the currents for all possible switching states. This knowledge base of behavior rules has been proven in an offline mode. However, defining the complete switching behavior of the power converter needs extensive computational efforts and additional sensors.

*12) Spectrum Analysis Method [12]:* In this method, the current spectrum is analyzed for detecting the characteristics of an open transistor. A fast Fourier transform is used for the spectrum analysis. It requires relatively high computing power.

*13) Current Deviation Method [13]:* In this method, normalized value of the inverter output current is used. If the inverter is connected to a motor drive, then the machine state variables are evaluated. The deviation $c$ of the measured current $i_{\mathrm{s,meas}}$ from the reference current $i_{\mathrm{s,ref}}$ is used to detect a transistor open-circuit fault, as

$$c = i_{s,\mathrm{ref}} - i_{s,\mathrm{meas}}. \tag{3}$$

By applying a discrete Fourier transform, the mean value $c^0$ and the fundamental component $c^1$ of the deviation are calculated. A fault indicator $f$ is calculated as

$$f = \frac{c^1}{c^0}. \tag{4}$$

This indicator reduces the influence of load conditions and leads to a torque-independent fault detection. The magnitude of the fault indicator is compared against a threshold to identify fault condition. Its argument is used to detect the faulty transistor. Detection time of around two cycles is reported.

*14) Wavelet-Fuzzy Algorithm [14]:* This is a real-time condition-monitoring algorithm that uses three-phase currents. Wavelet analysis is used to identify changes or events in currents. Upon detecting a change, the dc offset of current is calculated. The polarity and value of the dc offset are fed to a fuzzy logic system to determine an open circuit or a misfiring fault. To differentiate between these faults, the duration for which the offset exists is considered.

*15) Wavelet-Neural Network Method [15]:* In this method, the three-phase currents are used for fault detection and classification. Wavelet transform is applied to obtain information

about the fault signatures. The variation in decomposition coefficients contains this information. Normalized approximation coefficients are fed into a back propagation artificial neural network (ANN) model to identify the faulty and healthy mode. Through simulation, a diagnosis error of less than 5% is reported.

*16) Wavelet-ANFI System [16]:* In this method, the drive dc-link current is monitored over one cycle for diagnosis. Continuous wavelet transform is applied on the fault characteristic signal and indices are derived to train the adaptive neurofuzzy inference (ANFI) system. The fuzzy logic renders ability to build knowledge bases and the parameter adaptation enables learning of nonlinear behavior.

*17) Clustering-ANFI System [17]:* In this method, the inverter three-phase currents are transformed to $d$–$q$ axis first. Then, these components are fed to the Clustering-ANFI System to recognize various vague fault patterns. It is shown that the clustering technique has reduced the dimension of the fuzzy model and training time compared to other methods. Worst-case error of 2.26% is reported.

*18) Subtractive Clustering-Based Mean Current Vector Method [18]:* This method is based on subtractive clustering analysis of the stator mean current vector. First, the stator three-phase currents are transformed from abc to $\alpha\beta$ axes using Concordia transformation. Then, the mean current vector is calculated and used as the fault signature. The trajectories of the mean $\alpha\beta$ current vector are calculated by using subtractive clustering method. Magnitude and phase of the mean current are used for fault identification and fault localization.

*19) Model-Based ANN Diagnostic Method [19]:* In this method, model of a closed-loop motor drive is developed. It provides three-phase voltages, currents, and electromagnetic torque for training a multiclass ANN. The ANN is trained to detect single-switch open-circuit faults and leg open faults in a three-phase inverter. Prediction rates of around 75% for single switch open-circuit faults and above 90% for leg open faults are reported.

*20) Diagnosis by Rule-Based Expert Systems [20], [21]:* This is an offline interactive method for diagnosis of ac drives. Basing on the input of the operator, the method advices possible causes and remedies.

*21) Using Bond Graph Model [22]:* In this method, the inverter system along with IGBT is modeled using Bond Graph methodology. The mean values of the voltages across the switches are used for fault detection.

### B. Performance Evaluation

To evaluate and compare the performance of the methods studied in the previous section, a list of evaluation indices are selected and used later in Section V. The details are explained as follows.

*1) Effectiveness:* A method is effective if it successfully indicates the faulty switch. Simulation results, from [4] and [5], showing the effectiveness of some methods discussed above, as shown in Table II.

*2) Resistivity Against False Alarms:* False alarms may occur during light-load and transient conditions, due to increased noise, i.e., low signal-to-noise ratio. Resistivity against transients can be improved by providing a dead time during transients. However, this approach has the drawback of slower detection. The necessary dead time is an indicator of resistivity against false alarms and is shown in Table III for a few methods [5]. Resistivity against noise can be improved by having higher threshold. However, it leads to false alarms during light loads. This can be handled by making a method independent of load. A comparison of the resistivity among a few methods is shown in Table IV.

TABLE II
EFFECTIVENESS OF SOME DISCUSSED METHODS FROM SIMULATION [4], [5]

| Methods | RMS Current ($I_{rms}$) | | |
|---|---|---|---|
| | 30 Amps | 6 Amps | 1.2 Amps |
| Park's Vector Method | Detected | Detected | Ambiguous |
| Slope Method | Detected | Detected | Failed |
| Normalized DC Current Method | Detected | Detected | Detected |
| Modified Normalized DC Current Method | Detected | Detected | Detected |
| Simple DC Current Method | Detected | Detected | Failed |

TABLE III
REQUIRED DEAD TIME FOR FALSE ALARM RESISTIVITY FROM SIMULATION [5]

| Detection Methods | Dead Time (ms) |
|---|---|
| Park's Vector Method | 5 |
| Slope Method | 10 |
| Normalized DC Current Method | 3 |
| Modified Normalized DC Current Method | 5 |
| Simple DC Current Method | 6 |

TABLE IV
COMPARISON OF RESISTIVITY FROM EXPERIMENTAL RESULTS [5]

| Detection Methods | Required dead time due to transients | Minimum current due to noise | Minimum current due to threshold |
|---|---|---|---|
| Slope Method | None | 2.6 $A_{rms}$ | – |
| Simple DC Method | 10 ms | – | 2.7 $A_{rms}$ |
| Modified Normalised DC Current Method | 3 ms | 2.1 $A_{rms}$ | – |

TABLE V
DETECTION TIME MEASUREMENTS FROM EXPERIMENTAL RESULTS [4], [5]

| Detection Methods | Detection Time (ms) | | |
|---|---|---|---|
| | Avg. | Min. | Max. |
| Slope Method | 38.3 | 23.6 | 58 |
| Modified Normalised DC Current Method | 18.4 | 8.0 | 35.1 |
| Simple DC Current Method at 3.2 $A_{rms}$ | 18.0 | 8.0 | 26.2 |
| Simple DC Current Method at 7.3 $A_{rms}$ | 11.9 | 4.8 | 18.0 |
| Simple DC Current Method at 10.3 $A_{rms}$ | 9.6 | 3.2 | 17.2 |

*3) Detection Time:* Detection time is dependent on the complexity of the detection method and its resistivity to noise, as the threshold is determined according to that. The detection times for different methods are shown in Table V, as reported in [4] and [5].

*4) Implementation Effort:* The efforts required to implement an algorithm dependents on the easy of sensing the detection parameter, on the mathematical operations involved and the decision-making process.

*5) Tuning Effort:* To have a universally usable method, it is advantageous to have as few thresholds and tolerances to be set as possible.

## III. Transistor Short-Circuit Fault

An IGBT short-circuit fault may happen due to either of the following reasons:

1) a wrong gate voltage, which may be caused by driver circuit malfunction, auxiliary power supply failure, or $dv/dt$ disturbance;
2) an intrinsic failure, which may be caused by overvoltage/ avalanche stress or temperature overshoot.

The short-circuit faults are difficult to deal with because the time between the fault initiation and failure is very small. Therefore, most of the existing IGBT short-circuit detection and protection methods are hardware circuit based. Very few are algorithm based.

### A. IGBT Rupture Phenomenon [23]

*1) Bond Wire Rupture:* As the device current rises to the point of bond wire rupture, the bond wire releases large energy raising the temperature of the soft gel, which, in plasma state, produces high internal pressure on the case of the module. If the device current is uninterrupted, all bond wires will fail with no module rupture, otherwise, the module case will fail.

*2) Impact Ionization [24], [25]:* Impact ionization and current crowding cause excess heat generation and eventually lead to device breakdown [26]. This may also happen due to device latch-up.

*3) Gate Circuit Degradation:* Electrical parameter degradation, due to the rupture in the isolated gate zone, affects the IGBT gate-source capacitance $C_{\rm GS}$ and the gate-drain capacitance $C_{\rm GD}$.

*4) Over Current [27], [28]:* Over current due to fault-under-load or switching into short circuit (or hard switching fault) causes high collector currents and device failure eventually.

### B. Detection, Protection, and Current Limiting Methods

A transistor short circuit in the motor drive system causes a nonzero dc component current flow in the stator winding and the machine experiences dynamic braking with other base-drives disabled. In many short-circuit failure conditions, the time between the fault initiation and the device failure is very short. The IGBTs can withstand abnormal currents up to around 10 $\mu$s. Therefore, detection and protection should happen dynamically with the changing conditions. Detection methods based on mathematical transformations can detect the damaged device, but they are not fast enough to cause any protective action. Other methods that are based on voltage level change are fast but need too many measurements for fault localization [23]. Detection methods that have shown better effectiveness in terms of detection or dynamic action or both are discussed in the following.

*1) De-Saturation Detection [29]:* In case of a fault, the increase in the collector voltage from the low saturation value to the bus voltage level, with the gate drive high, is detected. Then, a control signal is generated causing the gate pulses to be suppressed. This method uses only a simple sensing diode. However, it is not suitable for high-speed IGBT switching, because it requires a blanking time of around 1 to 5 $\mu$s and provides no dynamic feedback information.

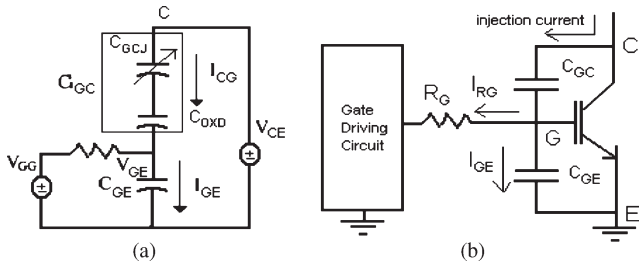



Fig. 1. (a) Equivalent circuit of IGBT gate. (b) Miller capacitance injection current during fault.

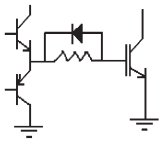
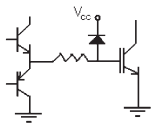
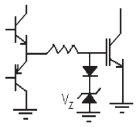
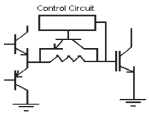
*2) Current Mirror Method [29]:* The collector current is sensed by a current mirror circuit, which is obtained by integrating a second IGBT into the main IGBT. The second IGBT carries a scaled-down current of the main IGBT. This current, through a known resistor, can be used for fault current detection. Implementation of the method is simple. However, it is very expensive due to the requirement of a special device with a current mirror circuit.

*3) Gate Voltage Sensing [23]:* In the equivalent circuit of the IGBT gate, shown in Fig. 1(a), $C_{\rm GCJ}$ constitutes the variable capacitances formed by the depletion region and is a function of many electrical parameters that change during fault conditions. This affects the gate current and leads to a significant change in the gate voltage. Therefore, the changes in the gate voltage are analyzed to identify a faulty condition. IGBT failures due to rupture in the isolated gate zone can be detected and proactive action can be taken to avoid major damages in the inverter. This method is simple, but it requires complicated protection circuitry.

*4) $di/dt$ Feedback Control [29]:* In this method, the induced voltage across the stray inductance between the Kelvin emitter and the power emitter is used to estimate the device current. The measured voltage, which reflects the device current, is compared with a preset value. When a fault is detected, a feedback control is introduced to dynamically control the fault current change rate $di/dt$. Once the fault current is contained at a predetermined level, by controlling the gate voltage, a slower turnoff mechanism is employed. This method does not require any blanking time and provides dynamic control of the gate voltage.

*5) Protection by Gate Voltage Limiting [30]:* These are peak current limiting circuits that are developed to protect IGBTs against fault-under-load conditions. In such conditions, while the collector voltage increases, current injection through the Miller capacitance from the load side to gate side increases the gate-emitter voltage, as shown in Fig. 1(b). This consequently increases the collector current from initial ON-state current to high peak values. When the collector voltage reaches the bus voltage, the current through the Miller capacitance vanishes and gate voltage falls down to the ON-state value. Subsequently, collector current falls to the saturation value

TABLE VI
GATE VOLTAGE LIMITING SCHEMES [30]

| Protection Schemes | Comments ("+": Advantage; "-": Disadvantage) |
|---|---|
|  (a) | (+) The diode provides a low-impedance path for the injected current, when a fault-under-load transient occurs. (-) The safe operating area is decreased due to high *di/dt*. |
|  (b) | (+) Gate voltage is clamped to the driver supply voltage. (-) The parasitic capacitance of the clamping diode affects the switching performance of the IGBT. |
|  (c) | (+) Gate voltage is clamped at $V_Z$ through a zener diode. (-) Parasitic capacitance of the diodes can affect the switching characteristic of the IGBT. |
|  (d) | (+) Limits the collector current peak by means of dynamic reduction of the gate resistance, using active components, during the fault transient. (-) Needs proper selection of the protection components. |

corresponding to the ON-state gate voltage and remains at this value as long as the device is gated.

As the gate resistance increases, the peak values of the gate voltage and the collector current increase, since a major part of the injected current flows into $C_{\rm GE}$, i.e., if $I_{\rm RG} \ll I_{\rm GE}$, then

$$V_{\rm GE} = \frac{C_{\rm GC}}{C_{\rm GC} + C_{\rm GE}} V_{\rm CE}. \tag{5}$$

From (5), the gate voltage increases with the collector voltage. To decrease this effect, either an IGBT of low Miller capacitance should be used or the gate resistance is decreased to reduce $I_{\rm GE}$. However, this leads to a high $di/dt$ and creates EMI issues. Some hardware methods to limit the gate voltage increase in literature are summarized in Table VI.

*6) Protection by Snubbers and Clamp Circuits [31]:* In hard switching applications, the trapped energy in the circuit stray inductance caused by abrupt interruptions of the device current appear as a voltage overshoot across the device. Snubbers and clamp circuits offer optimized protection against these transients. However, the use of these circuits for protection against turnoff transients caused by rapid suppression of the gate drive is not optimal, because it requires high-capacity high-voltage snubber capacitors that are bulky and costly.

*7) Protection by Slow Turnoff of IGBT Using Additional Passive Components [31]:* The issues with snubbers and clamp circuits in fault conditions are addressed by slowing down the turnoff of the IGBT using additional components. Through electronic gate control, the falling rate of the gate voltage is reduced only when a fault current is detected. This is accomplished either by a resistive method or a capacitive method. In a resistive method, a high value gate resistance is switched in series with the IGBT gate. In a capacitive method, a high value of external capacitor is switched in parallel with the IGBT gate input capacitance.

TABLE VII
DEFECT TRANSISTOR LOCATION SCHEME IN PARK'S VECTOR METHOD [3]

| Faulty Transistor | Current Phase Angle (degree) |
|---|---|
| T1 | 330-360 or 0-30 |
| T2 | 30-90 |
| T3 | 90-150 |
| T4 | 150-210 |
| T5 | 210-270 |
| T6 | 270-330 |

*8) Protection by Two-Step Gate Pulse [32]:* In hard switched fault, the device current ramps up very rapidly until it saturates, forcing the IGBT voltage to rise to the dc clamp. In desaturation condition, the voltage across the IGBT rises above 5 to 15 V with the gate voltage high, indicating abnormal switch currents. After fault detection, depending on the point, at which the fast turnoff pulse is applied, different levels of hole current flow under the $n^+$ source region. Due to impact ionization and rising temperature, a local maximum occurs at the curvature of the p-base n-drift junction and very small fraction of the total current flows through the channel. Hence, the device does not turnoff even after the gate voltage is removed. Eventually, the device breaks down due to thermal instability. To tackle this problem, a two-step gate pulse method is used. In this method, after fault detection, the gate voltage is reduced from its normal value to a lower value, causing the device current to decrease. The gate is held at this value long enough to ensure that the device voltage has climbed to the full clamp level. The gate voltage is then decreased to zero at a slow time constant. The slow gate discharge limits the $di/dt$ during the final turnoff.

*9) Average Current Park's Vector Approach [3]:* In this method, the fault occurrence is related to the average current Park's Vector modulus. The faulty device is determined by the corresponding phase angle. For a normal system, the mean of the current magnitude is zero and its space vector trajectory is a circle. If a fault occurs, the magnitude of the current space vector is nonzero and greater than a threshold. The defect transistor is located by the current phase angle, as shown in Table VII.

*10) Vector Composition of Inverter Output Voltage [33]:* This method uses the inverter output voltage vector harmonic composition at the fundamental frequency, assuming a significant component at the switching frequency appears in the output voltage upon the short-circuit failure. The output voltage is filtered by an analog circuit, which is tuned at the switching frequency. The filtered voltage is sampled at three times of the switching frequency. A linear transformation is applied to these values to obtain an instantaneous vector diagram of the switching frequency component. The magnitude of the vector is compared with a failure level and the phase shift of the component is used to determine the faulty switch. The remedial strategies employed here include a rapid and safe turnoff of the IGBTs and a fail-safe reconfigured operation

TABLE VIII
COMPARISON OF IGBT OPEN-CIRCUIT FAULT DIAGNOSTIC METHODS

| Methods | Effectiveness | Resistivity | Detection Time | Implementation Effort | Tuning Effort | Detection Parameter | Threshold Dependence on Detection Variable |
|---|---|---|---|---|---|---|---|
| Park's Vector Method [3] | Ambiguous at small currents | Poor at small currents | >20 ms | Medium | High | 3-phase currents | High |
| Normalized DC Current Method [4], [5] | Poor at small currents | Poor as multiple conditions may satisfy | 18.4 ms[4] | Low | Low | 3-phase currents | Independent |
| Modified Normalized DC Current Method [4], [5] | Good | Good | 18.4 ms[4] | Low | Low | 3-phase currents | Independent |
| Slope Method [6] | Poor at small currents | Poor | 38.3 ms [5] | Low | High | 3-phase currents | High |
| Simple DC Method [4], [5] | Poor at small currents | Medium | Load dependent [4] | Low | Medium | 3-phase currents | High |
| AC Instantaneous Frequency Method [6] | Cannot locate faulty transistor | Medium | 20 ms [6] | Low | Low | 3-phase currents | Low |
| Comparison of Actual and Reference Quantity Method [1], [7] | Needs 2-4 sensors for effective detection | Good | 5 ms [7] | High | Medium | Inverter pole voltage, phase voltages and neutral voltage | Independent |
| Sensing Voltage across the Lower Switch [8] | Good | Good | 2.7 ms[8] | Medium | –‡ | Lower switch voltages | Low |
| Centroid Based Fault Detection [9] | Good | Good | – | Medium | – | 3-phase currents | N/A |
| Current Pattern Recognition Method [10] | Many parameters to consider | Medium | 10 ms [1] | High | Medium | 3-phase currents | High |
| Converter Behavior Rules [11] | Not yet proven on-line | Good | – | High | None | Bus currents, 3-phase currents and voltages | Independent |
| Spectrum Analysis Method [12] | – | – | – | Medium | High | 3-phase currents | High |
| Current Deviation Method [13] | Good | Medium | 2 cycles [23] | High (Requires change in inverter control algorithm) | Low | Normalized 3-phase currents | Independent |
| Wavelet-Fuzzy Method [14] | Good if the fuzzy rules are carefully designed | Good | 5 cycles[14] | High | Medium | 3-phase currents | Low |
| Wavelet-Neural Network Method [15] | Diagnosis error < 5%[15] | Good if NN is thoroughly trained | – | High due to NN training | Low | 3-phase currents | N/A |
| Wavelet-ANFI Method [16] | – | Good as the NN is trained for noisy conditions | – | High due to NN training | Low | Dc link current | N/A |
| Clustering-ANFI System [17] | Worst-error of 2.26%[17] | – | – | High | Low | 3-phase currents | N/A |
| Subtractive Clustering Based Mean Current Vector Method [18] | Good | – | ¼ cycle[18] | Medium | Low | 3-phase currents | N/A |
| Model Based ANN Method [19] | Prediction rate of around 75%[19] | – | – | High | – | 3-phase voltages, currents and torque | N/A |
| Rule Based Expert Systems [20], [21] | Offline diagnosis tool | – | – | High | – | User input | N/A |
| Bond Graph Method [22] | – | – | – | High | – | Switch voltages | High |

†: "N/A" means "Not Applicable"
‡: "–" means "Not Available"

to avoid catastrophic failures. In a three-phase system, if one leg is isolated due to a short-circuit fault, the other two legs are reconfigured to work as a single-phase inverter, allowing continued operation at reduced load.

## IV. INTERMITTENT GATE-MISFIRING FAULT

IGBT gate-misfiring faults can cause catastrophic breakdown of the device, if the faults remain undetected. It may be caused by driver circuit open circuit, control circuit element deterioration, degraded electromagnetic compatibility, etc. Inverters can operate for a considerable period of time even with sustained gate misfiring. However, this is accompanied by degraded output voltage and overstress on other switching devices and dc bus capacitors. Gate misfiring may also lead to a short-circuit fault of a device. This may happen when the device fails to turnoff causing shoot-through. In most cases, gate misfiring is intermittent in nature. Online monitoring is important in

TABLE IX
COMPARISON OF IGBT SHORT-CIRCUIT FAULT DIAGNOSTIC METHODS

| Methods | Parameters Required | Turn-off | Dynamic Protection | Implementation Effort | Reliability | Comments |
|---|---|---|---|---|---|---|
| De-saturation Detection Method [29] | Collector Voltage | Abrupt | No | Low | Medium | Device turn-off not assured |
| Current Mirror Method [29] | Device Current | Abrupt | No | Low | Medium | Very expensive |
| Gate Voltage Sensing Method [23] | Gate Voltage | Abrupt | No | Low | Low | Requires complicated protection circuitry |
| *di/dt* Feedback Control Method [29] | Device Current | Soft | Yes | High | Medium | Stray inductance hard to control |
| Protection by Gate Voltage Limiting [30] | Gate Voltage | Soft | Yes | Medium | Low | Interfere with normal operation |
| Protection by Snubbers and Clamp Circuits [31] | Device Voltage | N/A† | Yes | High | Low | Very expensive for fault protection |
| Protection by Slow Turn-off Using Additional Parameters [31] | Gate Voltage | Soft | Yes | High | Low | Require complex circuitry |
| Protection by Two-Step Gate Pulse [32] | Gate Voltage | Soft | No | High | High | Reliable shutdown of the device, low *di/dt* |
| Average Current Park's Vector Approach [3] | Phase currents | N/A | N/A | Medium | High | Reliable detection but offer no protection |
| Vector Composition of the Inverter Output Voltage [33] | Inverter output voltage | N/A | N/A | Medium | Low | Slow response as it uses filters |

safety-critical applications. Detection methods in frequency domain are not suitable for intermittent faults, since the steady-state measurements do not contain information about the fault after the system has recovered. Therefore, time-domain techniques are desirable. Intermittent gate-misfiring fault has not been extensively studied in the previous literature. A few detection methods are discussed in the below section.

### A. Detection Methods

*1) Detection by Output Current Trajectory [34]:* A real-time condition-monitoring algorithm for PWM inverter induction motor drives is discussed in [34]. The monitoring principle of the algorithm is summarized as follows. When a gate-misfiring fault occurs in one of the inverter switching devices, the voltage disturbance will cause an increment to the stator current space vector. The incremental current happens toward a unique direction that is determined distinctively by the failed device. An incremental system model is used to provide compensation to the measured current response, so that the modified incremental current signal will decay in the opposite direction to the initial offset caused by the voltage disturbance. The trajectory of the current response can be used to detect the fault and locate the defect switch.

*2) Pattern Recognition Approach [35], [36]:* This is a fuzzy-based technique and uses inverter output current to detect the intermittent loss of firing pulses. A fuzzy fault detection and diagnosis block compares the stator Concordia current vector with that in the rule base. By this process, the method can detect a fault, locate the faulty device and can also find the fault severity. The method is discussed more in [35] and [36].

## V. CONCLUSION AND RECOMMENDATIONS

This paper has presented a comparative literature review on the existing methods for IGBT diagnostics and protection, including open-circuit, short-circuit, and gate-misfiring faults. More than 20 methods for open-circuit fault and 10 methods for short-circuit fault diagnosis have been evaluated and compared in Tables VIII and IX.

Among the open-circuit fault methods, the modified normalized dc current method is found to be very effective in detecting faults with high resistivity to false alarms. In addition, it is independent of load variations. The Current Deviation Method, which is embedded in the inverter control algorithm, has the advantage that it can take remedial measures and keep the inverter operate under a fail-safe mode, even with an open-circuit fault in one of the devices. Wavelet, fuzzy, and neural network-based methods render additional intelligence for smart diagnosis but at the cost of higher implementation effort.

When an IGBT short-circuit fault occurs, a controlled turnoff of the device during faults is effective in protecting the device, e.g., the protection method using two-step gate pulse. It also keeps the $di/dt$ low and avoids interference issues. The methods that propose dynamic control using the stray inductance are difficult to implement in practice, because the accurate stray inductance is difficult to obtain.

Gate-misfiring faults usually do not cause immediate system failures. The rapid advances in digital controls and electronics have also greatly remedied these problems. Therefore, these faults have not been extensively studied in literature. However, in critical applications, gate misfiring should still be taken care of as early as possible, since it expedites the inverter circuit deterioration and often causes more catastrophic faults.

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**Bin Lu** (S'00–M'06–SM'09) received the B.Eng. degree in automation from Tsinghua University, Beijing, China, in 2001, the M.S. degree in electrical engineering from the University of South Carolina, Columbia, in 2003, and the Ph.D. degree in electrical engineering from Georgia Institute of Technology, Atlanta, in 2006.

From 2001 to 2003, he was with the Virtual Test Bed Group, University of South Carolina, where his master thesis work built the foundation of a real-time virtual test bed for the hardware-in-the-loop testing of dynamic power systems. From 2003 to 2006, he was a Graduate Research Assistant with the Power Electronics and Motor Diagnostics Group, Georgia Institute of Technology, working on the energy evaluation and condition monitoring of electric machines. In the summer of 2006, he was with the Manufacturing Research Laboratory, General Motors R&D Center, Warren, MI, as a graduate summer intern. Since October 2006, he has been with the Innovation Center, Eaton Corporation, Milwaukee, WI, where he is currently an Engineering Specialist and Program Manager. His research interests include controls and diagnostics of electric machines and power electronics, computational intelligence applied to energy systems, integration and protection of renewable energy sources, modeling and simulation, and wireless sensor networks applied in electric power areas. He has published over 50 papers in refereed international journals and conference proceedings and has nine U.S. patent applications in these areas.

**Santosh K. Sharma** received the B.Tech. degree in electrical and electronics engineering from Jawaharlal Nehru Technological University, Hyderabad, India, in 2003, and the M.Tech. degree in machine drives and power electronics from Indian Institute of Technology, Kharagpur, India, in 2005.

From 2005 to 2007, he was with the Research Division, TVS Electronics, Bangalore, India, where he was working on development of uninterruptible power system, inverters, and low-power dc–dc converters. Since May 2007, he has been with the India Engineering Center, Eaton Corporation, Pune, India, working on condition monitoring and fault diagnostics of induction machines and drives. His research areas include electric motor drives and diagnostics, power converters, and flexible ac transmission systems.