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Introductory Invited Paper

Reliability methods and standards

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Abstract

This tutorial focuses on three aspects of standardization: existing standards and organizations, evolution of standards and creation of new standards, new developments.

An overview of existing standards and involved organizations is given. The main standardization institutes and forums for semiconductor reliability are described.

The process of introducing new standards and changes is described. New and changed standards are needed when technologies change and when increased knowledge leads to better methods. Also, new application areas and changed customer requirements may lead to changed or new methods.

Advantages and disadvantages of standards are discussed, with emphasis on standards for qualification. Development and use of knowledge-based methods is addressed.

1. Introduction

Reliability methods for semiconductor devices have been standardized by several organizations. In Section 2 a summary is given of the most important standardization organizations, and the organizations influencing the standardization process. Section 3 explains the way of working of in international standardization in the creation of new standards and the evolution of existing standards. New directions in reliability methods and standards are described in Section 4.

The tutorial focuses on standardization of reliability of electron devices. The tutorial will not address quality standards, e.g. ISO/TS 16949 [1], and other standards related to system certification.

2. Reliability standards and organizations

This section provides an overview of standards and specifications related to the reliability of semiconductor devices. These standards can be classified as shown in Table 1. Reliability methods are often subject of standardization in several organizations. In those cases the standards were usually derived from a common source, e.g. MILSTD-883 [2], and only minor differences exist between different standards.

2.1. MIL standards

The MIL standards were developed by the United States Department of Defence (DOD) in the mid twentieth century as product procurement specifications because of bad reliability experience during WW II. The MIL standards have been used as industry standards for a many years, and also today many companies still refer to the MIL standards. With the advent of new technologies other standards have become more important.

MIL-STD-883 [2] establishes test methods and other procedures for integrated circuits. It provides general requirements, mechanical, environmental, durability and electrical test methods, and quality assurance methods and procedures for procurement by the US military. The

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Table 1
Classification of standards

Class	Example
International standards	IEC
National standards	USA (ANSI)
Governmental standards	MIL
Industrial standards	EIA/JEDEC
Standards by expert groups	ESDA
Standards by semiconductor users	AEC Q100

test methods described in MIL-STD-883 include environmental test methods (standard numbers 1000–1999), mechanical test methods (2000–2999), digital electrical test methods (3000–3999), linear electrical test methods (4000–4999), and test procedures (5000–5999).

MIL-STD-750 [3] specifies mechanical, environmental and electrical test methods and conditions for discrete semiconductor devices.

MIL-STD-202 [4] specifies mechanical and environmental test methods for electronic and electrical components.

MIL-HDBK-217 [5] is a US Military handbook for reliability prediction of electronic equipment. This handbook introduces methods for calculating the predicted failure rate for each category of parts ion electronic equipment, including e.g. mechanical, components, lamps, and advanced semiconductor devices such as microprocessors.

2.2. IEC standards

The IEC (International Electrotechnical Commission) was founded in 1908, and is the leading global organization that prepares and publishes international standards for electrical, electronic and related technologies. IEC's goal is to facilitate world trade by removing technical barriers, and to promote international cooperation on electrotechnical standardization and related matters. IEC standards serve as a basis for national standardization and as references when drafting international tenders and contracts.

At present, the IEC has 51 member countries. Only one representative organization per country (the National Committee) is qualified for IEC membership. Membership of the National Committees may include manufacturers, providers, distributors and vendors, consumers and users, governmental agencies, professional societies and trade associations, and standards developers.

The IEC organization diagram is shown in Fig. 1.

IEC publishes a.o. International standards (IS), Technical specifications (TS), Technical reports (TR), and guides.

Examples of reliability related IEC standards:

- IEC 60068: environmental testing [6]. This standard contains fundamental information on environmental testing procedures and severities of tests. It is primarily intended for electrotechnical products.
- IEC 60749 series [7]: Mechanical and climatic test methods. These standards are applicable to semiconductor devices (discrete devices and integrated circuits).

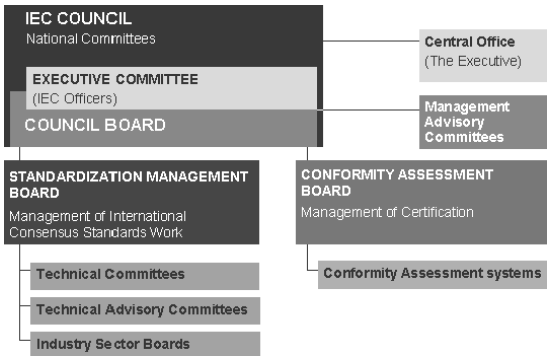

Fig. 1. IEC organization.

- IEC 62047 [8]: Micro-electromechanical devices.
- IEC 62373/74 [9]: Wafer level reliability.
- IEC/TR 62380 [10]: Reliability data handbook – Universal model for reliability prediction of electronics components, PCBs and equipment.

2.3. JEDEC standards

JEDEC Solid state technology association (formerly Joint Electron Device Engineering Council) is the semiconductor engineering standardization division of the Electronic Industries Alliance (EIA), a US-based trade association that represents all areas of the electronics industry. JEDEC was originally created in 1960 to cover the standardization of discrete semiconductor devices and later expanded in 1970 to include integrated circuits.

JEDEC does its work through its 50 committees and subcommittees. Members are both manufacturers and users of semiconductor components and others allied to the field. Presently there are about 290 member companies.

JEDEC spans a wide range of standards related to reliability. These standards are among the most referenced by semiconductor companies in the USA and Europe. The JEDEC committees for reliability standardization are:

- JC-14 Committee: Quality and reliability of solid state Products.
- JC-14.1 Subcommittee: Reliability test methods for packaged devices.
- JC-14.2 Subcommittee: Wafer level reliability.
- JC-14.3 Subcommittee: Silicon devices reliability qualification and monitoring.
- JC-14.4 Subcommittee: Quality processes and methods.
- JC-14.6 Subcommittee: Failure analysis.
- JC-14.7 Subcommittee: Gallium arsenide reliability and quality standards.

JEDEC publishes standards, publications, guidelines, standard outlines, specifications, ANSI and EIA standards.

The online JEDEC catalogue gives a complete overview of the JEDEC documents. The JESD 22 [11] series contains

most reliability related standards. Other reliability related standards include Wafer level reliability methods, qualification and monitoring methods as well as remaining reliability related methods, e.g. latchup test. JESD 47 [12] is a well-known industry standard for stress-test driven qualification of semiconductor products. Furthermore, the JEDEC documents include joint publications (JP), e.g. the Foundry Qualification Guidelines [13] developed together with the fabless semiconductor association (FSA), and joint standards (J-STD), e.g. the joint IPC/JEDEC standard [14] for Moisture sensitivity classification method for SMD devices. In addition, the catalogue contains JEDEC Publications (JEP) and EIA standards, some of which are related to reliability as well. The catalogue also lists standards by subcommittee, which gives the fastest way of finding all relevant standards.

Since 1998 JEDEC has provided its standards and publications on the JEDEC website at no charge.

2.4. JEITA

Japan Electronics and Information Technology Industries Association (JEITA) was formed in 2000 from a merge of The Electronic Industries Association of Japan (EIAJ) and Japan Electronic Industry Development Association (JEIDA). It's objective is to promote the healthy manufacturing, international trade and consumption of electronics products.

JEITA's main activities are supporting new technological fields, developing international cooperation, and promoting standardization. Principal product areas covered by JEITA are digital home appliances, computers, industrial electronic equipment, electronic components and electronic devices (e.g. discrete semiconductor devices and ICs).

JEITA standards related to semiconductor reliability are

- ED4701 [15], containing environmental and endurance test methods.
- ED4702 [16], mechanical tests.
- ED4704 [17], failure mode driven tests (WLR).
- EDR4704 [18], guideline for accelerated testing.
- EDR4705 [19], SER.
- EDR4706 [20], FLASH reliability JEITA standards are available online.

2.5. Other

The most relevant standards for semiconductor reliability have been described above. However, there are many other standards as indicated in Table 1. Sometimes standards are developed by semiconductor user groups or expert groups with a limited scope. The Automotive Electronics Council and the ESD association are the most important examples of user groups and expert groups, respectively.

2.5.1. AEC

The Automotive Electronics Council (AEC) was originally established by Chrysler, Ford, and General Motors for the purpose of establishing common partqualification and quality-system standards.

Currently, the sustaining members are Delphi Corporation, Siemens VDO Corporation and Visteon Corporation. The scope is limited to automotive applications.

The AEC Q100 [21], stress test qualification for integrated circuits describes the qualification requirements for IC's in automotive applications. Other AEC standards included in Q100 are for example:

- AEC – Q100-001 – Rev-C: Wire bond shear test.
- AEC – Q100-002 – Rev-D: Human body model (HBM) electrostatic discharge test.
- AEC – Q100-003 – Rev-E: Machine model (MM) electrostatic discharge test.
- AEC – Q100-004 – Rev-C: IC latch-up test.
- AEC – Q100-005 – Rev-B: Non-volatile memory program/erase endurance, data retention, and operational life test.
- AEC – Q100-006 – Rev-D: Electro-thermally induced parasitic gate leakage test (GL).
- AEC – Q100-008 – Rev-A: Early life failure rate (ELFR).
- AEC – Q100-010 – Rev-A: Solder ball shear test.
- AEC – Q100-011 – Rev-B: Charged device model (CDM) electrostatic discharge Test.

2.5.2. Electrostatic discharge association

The ESD association is a professional voluntary association dedicated to advancing the theory and practice of electrostatic discharge (ESD) avoidance. The association has more than 2000 members from more than 30 countries throughout the world. The scope includes effects of ESD on electronic components, and areas such as textiles, plastics, web processing, clean rooms, and graphic arts.

The association has published more than thirty documents covering electrostatic discharge in the electronics environment. These include standards, standard test methods, standard practices, technical reports, and informational advisory documents.

Examples of standards:

- ANSI/ESD STM5.1-2001 [22] Electrostatic discharge sensitivity testing-human body model (HBM) component level.
- ANSI/ESD STM5.2-1999 [23] Electrostatic discharge sensitivity testing-machine model (MM) component level.
- ANSI/ESD STM5.3.1-1999 [24] Charged device model (cdm)-component level.
- ANSI/ESD SP5.3.2-2004 [25] Sensitivity testing socketed device (SDM) component level.

- ANSI/ESD SP5.4-2004 [26] Transient latchup testing-component level supply transient stimulation.
- ANSI/ESD SP5.5.1-2004 [27] Electrostatic discharge sensitivity testing transmission line pulse (TLP) component level.

3. Evolution of standard, creation of new standards

3.1. New and changed standards

New standards or changes are needed when new technologies emerge, e.g. Cu/Low-K, when new knowledge becomes available or when changes occur in application areas, use conditions or legislation (Pb-free). Most standardization organizations have a mandatory review scheme. For IEC standards the maintenance cycle ranges typically between 3 and 5 years. IEC publishes changes to standards as amendments with a maximum of 2 amendments per standard. The process of introducing new or changed standards is shown for IEC and JEDEC.

3.2. The process of introducing new standards and changes

3.2.1. IEC

The standards are developed by Technical Committees (TC's), Sub Committees (SC's) and Working Groups (WG's) for each technical field. IEC standards are based on consensus. Any member (country) of the IEC may participate in the preparatory work.

The technical committees prepare technical documents, which are submitted to the member National Committees for voting. For International Standards full consensus is needed. If consensus cannot be reached a Technical Specifications may be produced. Technical Reports are informative and based on a simple majority of votes.

Table 2 shows the development stages of IEC standards. The revision of an existing standard starts at the committee draft stage.

Subjects not yet ready for standardization may start in the preliminary stage. Proposals for new work are submitted by a National Committee. A simple majority vote of members and a minimum of four nominated experts are needed to start the work. The document enters the committee stage when it is submitted to the National Committees as a committee draft (CD) for comment. The next stage is the enquiry stage, when the document is submitted as a Committee Draft for Vote (CDV) to all National Committees for a five-month voting period. It is the last stage at which technical comments can be taken into consideration. In the Approval stage the Final Draft International Standard (FDIS) is circulated to the National Committees. A 2/3 majority of positive votes is needed for approval.

3.2.2. JEDEC

JEDEC members ballot proposals for new standards. Proposal can also result from surveys among members on important areas. Standardization work takes place at the regular committee meetings. The members vote via the JEDEC voting machine prior to meetings. Voting is then reported at the meetings and modifications to the proposals are made in response to comments that are made during balloting.

After a ballot passes and comments are resolved and incorporated, the proposal goes to the JEDEC Board of Directors for final approval before publishing.

The review cycle is done by issuing a regular ballot in which the entire standard, publication, registration, guideline, or specification is open for comment (see Fig. 2).

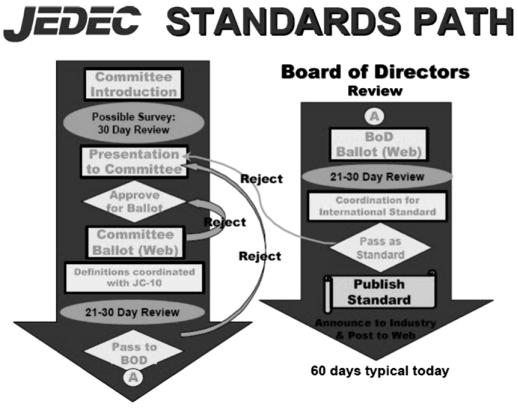

Fig. 2. Development of standards in JEDEC.

Table 2
Classification of standards

Project stage	Associated document	
	Name	Abbreviation
Preliminary stage	Preliminary work item	PWI
Proposal stage	New work item proposal	NP
Preparatory stage	Working draft(s)[a]	WD
Committee stage	Committee draft(s)[a]	CD
Enquiry stage	Enquiry draft[b]	ISO/DIS IEC/CDV
Approval stage	Final draft international standard[c]	FDIS
Publication stage	International standard	ISO, IEC or ISO/IEC

[a] These stages may be omitted, as described in Annex F.
[b] Draft International Standard in ISO, committee draft for vote in IEC.
[c] May be omitted (see 2.6.4).

4. New developments

Standardization in semiconductor reliability focuses mainly on reliability test methods like HAST, ESD tests, etc. Several of these tests have been unchanged for many years, e.g. High Temperature Storage Test. On the other hand, new test methods have been developed driven by technology changes, e.g. the Tin Whisker Growth measurement after the introduction of Pb-free soldering. Another broad field in semiconductor reliability subject to standardization is reliability qualification. Usually the requirements for qualification are described in terms of required test methods, sample sizes, and test conditions (JESD 47, AEC Q100).

The main advantage of the use of standards for reliability is the common language used in different parts of the world, by suppliers and their customers, and as a consequence the elimination of a barrier for international trade. Other advantages are the use of an industry practice, which worked rather well for decades, the acceptance by customers, and the little effort needed to write a qualification plan. However, there are also disadvantages of using standard methods. Disadvantages are the rigid requirements, which are sometimes much more severe than needed for the application, sometimes not severe enough, and sometimes not applicable for a new technology. The result is that stress test times are too long, relevant failures are not found, or that massive failures occur because a product is overstressed. In other words, the qualification plan is not tailored to the specific technology and application, which may lead to waste of time and money, or to the risk of failures in the field.

These disadvantages are especially important for the use of standards for qualification. Dissatisfaction with stress test driven qualification programs based on JESD 47 has led to several initiatives for improved qualification standards in the past.

4.1. Development of knowledge-based methods

To accommodate the disadvantages of the stress-test driven qualification approach a number of initiatives have been taken, which can be classified as programs for knowledge-based qualification.

The difference between the stress-test driven qualification test methods and knowledge-based qualification is mainly in the way the qualification plan is set up and the test conditions and duration are determined. The stress-test driven approach uses a standard list of stress tests, along with standard conditions, durations, and sample sizes. Such a list represents industry practice and/or customer requirements, and is determined from experience, often using LTPD-based sampling plans [28]. The stress-test driven approach is well documented and standardized with JEDEC 47 and AEC Q100. It should be mentioned that the approach is only well described for product qualification, not for wafer fab process or assembly qualification.

Knowledge-based qualification uses physics of failure and customer requirements in terms of mission profiles and failure rates. The qualification plan translates the customer needs to a program of stress tests.

There are no standards yet for knowledge-based qualifications, but some important publications lead the way to the new approach. Some of these are discussed in more detail below.

4.2. Publications and standards

International Sematech published a white paper with the title "Knowledge-based reliability qualification of silicon devices" in 2000 [29] and "Understanding and developing knowledge-based qualification of silicon device" in 2004 [30]. Both publications describe knowledge-based qualification. The differences between stress-test driven qualification [12] and knowledge-based or failure mechanism driven qualification [31–33] are addressed. In the knowledge-based approach it is key to have a link between reliability of the test vehicle and the real product. Knowledge-based qualification may use specific test structures or complete products. For new technologies it is critical to verify known failure mechanisms and models and to investigate new failure mechanisms. The latter can be done by using known stress tests, and stressing to failure. The reader is also warned that the qualification is as good as the knowledge that is used. Knowledge-based qualifications may include the use of simulations, e.g. thermomechanical simulation of package stress and resulting cracking of layers on the die. For instance, simulations may indicate that a certain package type generates more stress than related packages, and consequently the worst-case package may be used for qualification, covering also the other packages.

An other initiative was from the Semiconductor Quality Management Council (SQMC) workshop headed by Infineon. This methodology contains a detailed description how to set up a knowledge-based qualification. Customer requirements form the basis for qualification. Parameters are defined which characterize the reliability performance and target values for these parameters are derived from the requirements. The difference between known values and targets triggers actions, which lead to a qualified product (see Fig. 3). The method has been published in [34].

Other publications describing knowledge-based qualification are e.g.:

- JESD 94, Application specific qualification using knowledge-based test methodology [32].
- SEMATECH White Paper #99083810AXFR, use condition based reliability evaluation of new semiconductor technologies [35].
- JEP148, Reliability qualification of semiconductor devices based on physics of failure and risk and opportunity assessment [35].

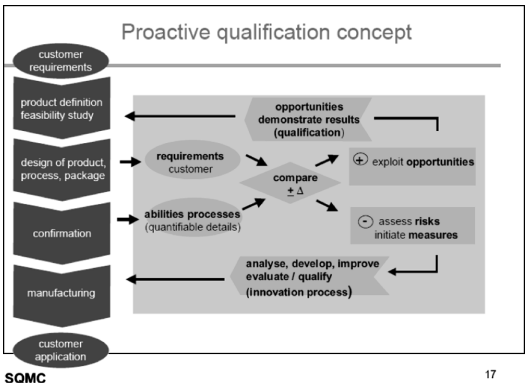

Fig. 3. SQMC knowledge-based qualification method.

The most recent activity related to knowledge-based qualification is the joint development of a Robustness Validation Handbook, by ZVEI and SAE [36], AEC. The handbook uses a knowledge-based approach, and describes a detailed assessment of the robustness of semiconductor devices. The new element is the relation with a Zero Defects strategy.

5. Conclusions

Reliability standardization is necessary and helps to achieve a uniform approach to reliability across the world. Several organizations are active in reliability standardization, and the efforts are in most cases coordinated to avoid duplication of work.

New methods are being developed to make better use of existing knowledge, to avoid unnecessary long qualification times and waste of resources, and above all, to have better coverage of all relevant failure mechanisms in semiconductor device qualification.

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