The Smart Power High-Side Switch: Description of a Specific Technology, Its Basic Devices, and Monitoring Circuitries

ABDELLATIF ELMOZNINE, JEAN BUXO, MARISE BAFLEUR, AND PIERRE ROSSEL, MEMBER, IEEE

Abstract—**This paper details the choice of a processing technology and of a design methodology adapted to the realization of a monolithic solid-state, high-side power switch for automotive applications and describes the devices, circuits, and functions made possible by this technology.**

I. Choice of a Smart Power High-Side Switch Technology

In order to reduce the chip area, an n-channel vertical DMOS power transistor will be chosen as the power switch. The device's backside drain will have to be connected to the battery voltage supply V_{BAT} so as to meet the requirements of the automotive field and will therefore perform a high-side switch function.

For this moderate voltage application, the VDMOS sits on an n^- epilayer whose thickness is related to the device's voltage handling capability (10 μm for 60 V) and has a multicellular configuration aimed at reducing its on-resistance value and at increasing its current capability.

A substantial requirement for the chosen technology is that it should lend itself to mass production as a result of its low cost and high fabrication yield. To reach this goal, a reduced mask sequence is proposed involving only highly mature and well-experienced MOS processing steps of low complexity. Two interconnecting levels, polysilicon and metal, will be used to increase the integration density further.

Finally, it is worth recalling that given the very harsh automotive environment, i.e., temperature ranging between -40 and $+125$°C, very low power dissipation in the switch during turn-on and turn-off is required, consistent with a low-cost package. Thus, it will be necessary to turn on strongly and rapidly the high-side switch. For this, a CMOS level-shifting capability usually performed by a charge-pump circuit is necessary.

In this VDMOS-compatible CMOS process, the n-channel transistors outside the power device also sit on the common n^- epilayer. They are embedded in a p^- well that will provide them with the necessary static isolation and that, endowed with MOS field-plate termination [1] (Fig. 1), will permit the withstanding of large voltage values.

For the sake of simplicity and in accordance with the previous low-cost requirements for the technology, a single p^- well will be diffused before polysilicon deposition and will be used as both the p^- body in the VDMOS and the p^- substrate in the NMOS transistor logic device. Although this is not consistent with a double-diffused, self-aligned gate in the VDMOS, it appears that, in most cases, the channel length of this device is not a limiting factor. Proper and complete integration of the VDMOS also requires including a p^+ deep diffusion aimed at shorting the p^- body to its n^+ source diffusion. This latter diffusion will also be used to make up the n^+ source and drain of the logic self-aligned n-channel MOS devices.

High-voltage n-channel devices are also necessary to sustain the high-voltage situation created, in particular, in the charge-pump circuitry. As shown later in Section II-A, these transistors incorporate a supplementary n-type implanted region (n-dep) with sufficiently low doping such that, combined with n^+ source–drain, they will make up a lightly doped drain structure so as to better accommodate high voltages [2].

The charge-pump circuit driven at a frequency $f_{\text{pump}} \approx 1/\tau$ will progressively raise the gate voltage of the VDMOS to a value higher than V_{BAT} thanks to the bootstrapping action of a large-value capacitor C_{pump} that is sequentially charged up and discharged into the VDMOS gate every τ seconds. Consequently, the technology will have to incorporate an n^+ implant (n^+ cap) that, located under an MOS capacitor, will provide sufficiently fast, high-value capacitors [3].

Introducing a LOCOS processing step for field oxides can deteriorate the needed balance between cost and performance. Indeed, LOCOS will only introduce savings in real estate in the logic area. It is worth noticing that the n^+ source–drain self-alignment with the p^+-field implant, which implies using the LOCOS process, will also bring about lower breakdown voltage values of the logic n-channel transistor [4]. Therefore, a "thick-oxide" process will be advocated.

This "thick-oxide" process, shown in Fig. 2, only requires nine masking steps (p^- well, deep p^+, n dep, n^+ cap, thin oxide, polysilicon, n^+ source–drain, contact,

Manuscript received August 2, 1989; revised December 11, 1989. The review of this paper was arranged by Associate Editor B. J. Baliga.

The authors are with the Laboratoire d'Automatique et d'Analyse des Systèmes, Centre National de la Recherche Scientifique (CNRS), 31077 Toulouse Cedex, France.

IEEE Log Number 9034212.

0018-9383/90/0400-1154$01.00 © 1990 IEEE

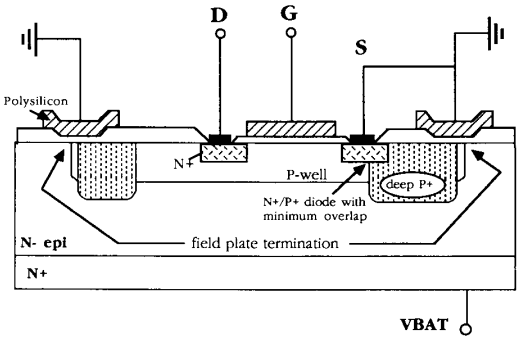


Fig. 1. Cross section of the silicon implementation of a LV NMOS transistor with its static and dynamic shielding.

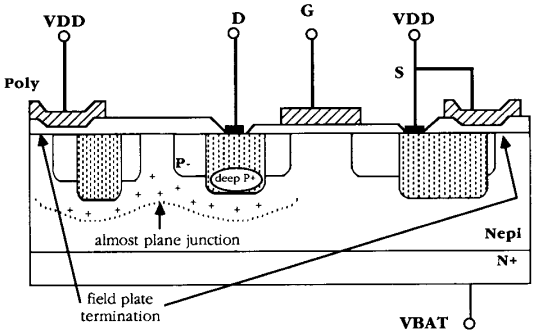


Fig. 3. Cross section of the silicon implementation of a LV PMOS transistor with its static shielding.

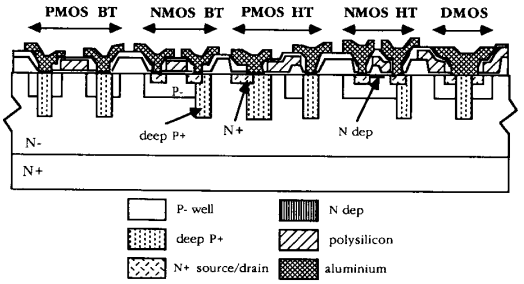


Fig. 2. Cross section of the chosen smart power technology.

aluminum), thus complying with the previous cost-saving and ruggedness characteristics required for this technology.

II. Static and Dynamic Isolation

Five main devices are made available in this technology:

1) low-voltage (LV) p- and n-channel devices,
2) high-voltage (HV) p- and n-channel devices,
3) VDMOS switch,
4) Zener diode, and
5) MOS capacitor.

Their basic implementation, within the framework of the previous technology, will be described hereafter.

A. Static Isolation

1) Proper operation of both n- and p-channel LV MOS logic devices in the logic section of the circuit makes it necessary to use an intermediate voltage supply V_{DD} with $V_{DD} < V_{BAT}$.

It will be possible to include a number of LV n-channel MOS devices within a single p^- well. This p^--well diffusion will then be terminated with a deep p^+ ring that will ensure proper channel stopping at its edge. However, this termination, if not protected, is prone to early breakdown. Therefore, in order to reduce the lateral fringing field value, a tapered diffusion termination can be achieved by letting the p^--well diffusion laterally overlap the deep p^+ ring. This termination, conveniently capped with a grounded MOS field plate, will help reach the largest breakdown voltage value [1] (Fig. 1).

The LV p-channel device (Fig. 3), exposed to the high-voltage supply in the epilayer, will be protected by lightly doped drain–source structures [2] based on using the deep p^+- and p^--well diffusions in both the source and drain. In order to ensure proper termination of this device, a guard ring is used. This ring is obtained by stretching the source diffusion all around the PMOS device in such a way that the space-charge regions around the drain and guard ring merge so as to develop an almost planar junction configuration for the space charge layer [5]. This arrangement provides the largest possible breakdown voltage when a V_{DD}-biased MOS field plate protection is used for its termination. It should be stressed that, in contrast with the LV n-channel device, the LV p-channel is not a self-aligned gate transistor.

2) In order to obtain HV p-channel devices, the same guidelines will be followed with the addition of a tapered oxide step at the drain edge aimed at further reducing the electric field at its vicinity. This is compatible with the chosen thick-oxide process since it does not require any additional masking step.

HV n-channel devices (Fig. 4) are achieved when the lightly doped drain structure, based on using the n-dep implant, is conveniently associated with the previous tapered oxide step. This implant is called n-dep since its doping level is such that it can also help produce logic n-channel depletion-mode devices.

3) The self-protected multicellular VDMOS device will be conveniently protected, in this medium-voltage application, by the previously described MOS field-plate termination structure.

4) This technology can also provide conveniently protected Zener diode devices (Fig. 5). To this end n^+ source–drain and deep p^+ diffusions will be used. The same termination technique is used here again.

5) Fig. 6 shows the arrangement leading to an isolated capacitor that uses n^+ cap and deep p^+ diffusions in its substrate. It should be emphasized that positive dc bias should always be applied to polysilicon (plate *B*) so that

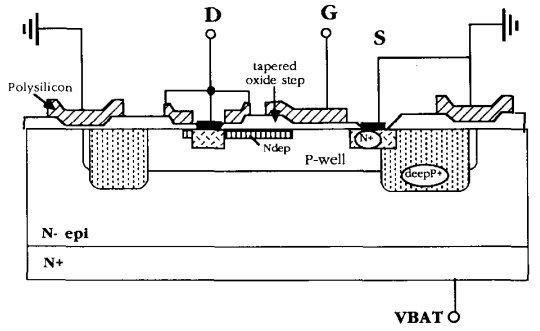


Fig. 4. Cross section of the silicon implementation of a HV NMOS transistor with its static and dynamic shielding.

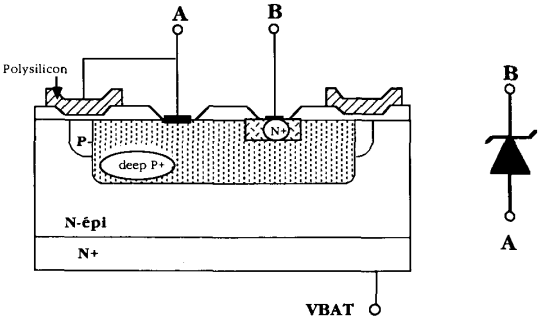


Fig. 5. Cross section of the silicon implementation of a Zener diode with its static shielding.

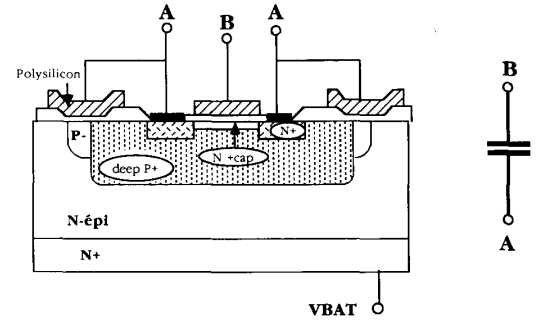


Fig. 6. Cross section of the silicon implementation of an MOS capacitor with its static shielding.

maximum conductivity is achieved throughout the n^+-cap RC distributed circuit in the lower electrode (plate A). As discussed below, this is most important in the charge-pump circuit since we expect the capacitor C_{pump} to respond fully at the highest possible frequency $f_{\text{pump}} \approx 1/\tau$.

B. Dynamic Isolation: The Floating-Well Approach

During turn-on and turn-off of the VDMOS, the highly resistive epilayer will probably propagate parasitic transients across the entire chip that can reach, through capacitive coupling, the transistors in the logic area. It appears that, since no buried isolating film is introduced in this very simple technology, such capacitive coupling is capable of generating a latchup situation.

Although a sanitary layout can reduce this effect, it appears that silicon area can be saved by using the shielding methodology based on the floating p^--well concept developed below.

The n-p-n parasitic vertical bipolar (PVB) transistor, associated with the NMOS transistor source diffusion, is most responsible for initiating latchup [6]. Therefore, in the case of a VDMOS-compatible CMOS process with grounded p^- well, the available deep p^+ diffusion can be used to completely eliminate the source-related PVB transistor [6]. Indeed, this is achieved by properly undercovering the n^+ source with deep p^+, as shown in Fig. 7. However, this configuration does not prevent transistor PVB2, whose emitter is the transistor drain, from turning on and initiating latchup. Indeed, as shown in Fig. 7, when the negative-going voltage parasitic transient ΔV in the epilayer is capacitively coupled into the NMOS drain through the drain-to-substrate capacitance of the PMOS transistor, PVB2 can be set on.

In this configuration, PVB2 will stay on as long as transient ΔV stays low. Therefore, if the latchup regeneration time τ_{regen} [7] is shorter than the length of the transient, latchup will occur and the parasitic thyristor will remain triggered even after ΔV ceases, which brings about possible destruction of the circuit.

The new idea [8] consists, then, in replacing the previous grounded well by a floating well and introducing, through layout, proper control on the time τ_0 during which the base current I can flow into PVB2. This control is achieved by making current I be supplied by the (RP^-, C_j) circuit described in Fig. 8. This is possible since the p^- well is free to change its voltage. However, PVB2 will still be turned on by the transient $\Delta V < 0$ in this configuration, but the time during which it will stay on is now not longer than τ_0, which is given by

$$\tau_0 = RP^- \cdot C_j \ll \tau_{regen}. \tag{1}$$

Equation (1) also states that τ_0 should be made to be much lower than τ_{regen}. Indeed, by so doing, it is possible to guarantee that the circuit will be latchup free despite the presence of transients and no matter how long these transients last.

In order to gain the necessary control of the product $RP^- \cdot C_j$, both the layout and the electrical parameters will be relevant in defining it. Therefore, it must be stressed that layout is important here in order to achieve a floating-well-based, latchup-free circuit.

It appears, however, that the floating-well configuration should also provide the requested immunity of the source-related transistor, PVB1. Indeed, the generous undercovering, depicted in Fig. 7, between the n^+ and the deep p^+ is now prohibited because the large capacitance values C_j associated with this n^+/p^+ junction would tend to make τ_0 too large.

The solution depicted in Fig. 9 consists of implement-

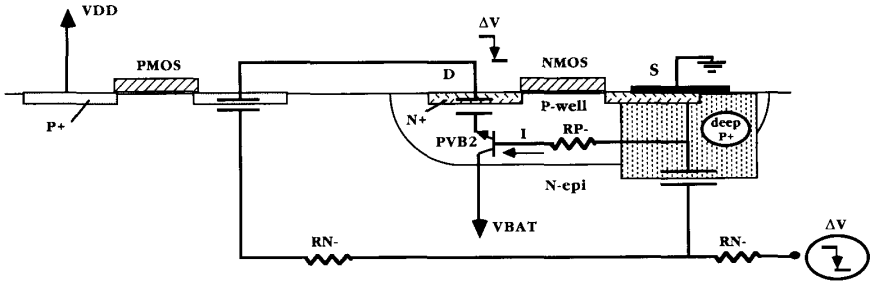


Fig. 7. CMOS technology with grounded well: case of a negative dV/dt transient.

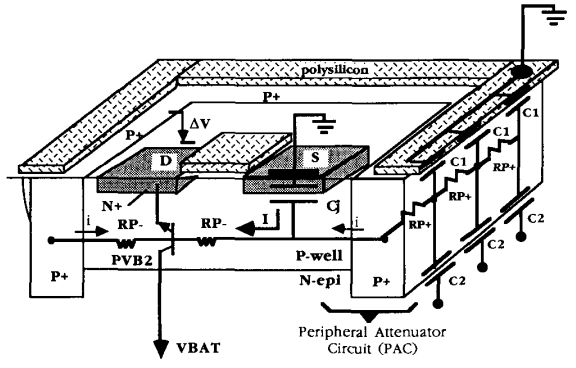


Fig. 8. Silicon implementation of an NMOS transistor in a floating well surrounded by a peripheral attenuator circuit (PAC) and equivalent electrical schematic in case of a negative dV/dt transient.

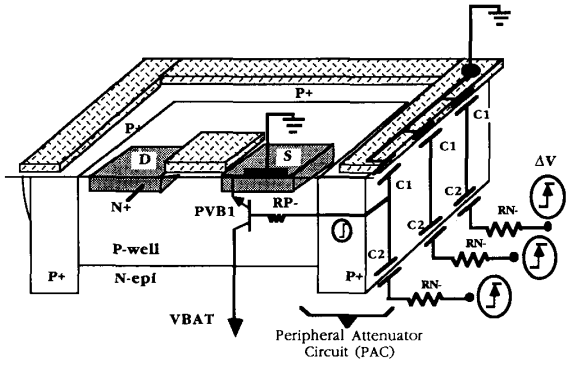


Fig. 9. Silicon implementation of an NMOS transistor in a floating well surrounded by a PAC and equivalent electric schematic in case of a positive dV/dt transient.

ing a thin-oxide-based MOS capacitor ($C1$), on top of the deep p^+ diffusion and completely surrounding the p^--well edge of the NMOS transistor by the resulting ($C1$, $C2$) capacitor attenuator circuit.

It can be shown that the ratio between $C1$ and $C2$ can be controlled and made large enough so that the voltage disturbance coupled through it into the p^- well should remain lower than 0.5 V. This limitation will hence prevent latchup initiation from originating in PVB1, under a positive-going ΔV voltage parasitic transient.

It should be pointed out that the device termination, shown in Fig. 1, provides both static and dynamic isolation since it is coincident with the peripheral attenuator circuit (PAC) described above.

It should also be noticed that letting the p^--well float can, in principle, reduce the voltage-handling capability of the PVB transistor since a BV_{CEO} situation is created. However, a small overlap between the n^+-source and deep p^+ will significantly decrease the gain h_{FE} of bipolar transistor PVB1 in such a way that $BV_{CEO} \approx BV_{CBO}$. The reduction of h_{FE} is due to the n^+/p^+ diode (Fig. 1), with very short diffusion length L_p, which practically inhibits the amplifying action of transistor PVB1 by shorting its emitter–base junction.

A numerical application of the previous ideas is now carried out, leading up to the definition of a dynamically shielded minimum-size transistor.

The dynamic behavior of latchup initiation has already been experimentally studied by forcing a transient current across the p^- well [7]. Measurements were made, at a given pulse current level, of the minimum pulse width sufficient to cause latchup. This width is, by definition, the latchup regeneration time τ_{regen}. A minimum trigger current of the order of 2.65 mA was detected with sharply declining regeneration time above it. Furthermore, a slow rate of decrease of τ_{regen} was detected at high-level currents (5.2 mA) and τ_{regen} appears not to decrease below 50 ns for currents above 6 mA. Both these two asymptotic behaviors were given proper physical explanation [7].

It will now be shown that a minimum-size transistor, on a floating p^- well, is compatible with the shielding criterion given in (1).

The value of RP^- is related to the NMOS transistor channel length L_N and the sheet resistivity of the p^- well. Typical values are in the range of 1 kΩ. A conservative maximum value for C_j of 2 pF will be adopted. Indeed, the dominant contribution to C_j is not due to the source/p^--well junction depicted in Fig. 8 but to the n^+/deep-p^+ junction resulting from the previously mentioned necessary n^+/p^+ diode, shown in Fig. 1, whose capacitance is not greater than 2 pF if the overlap between n^+ and deep p^+ is limited to 10 μm. This latter value largely fits within the possibilities of a photolithography controlled overlap.

As a result, minimum-size transistors with L_N in the range of a few micrometers can be realized, with no risk of latchup initiation, on a floating p^--well substrate. Since, for a given L_N, τ_0 is constant ($\tau_0 \approx 2$ ns $\ll 50$ ns), regardless of the width W_N of the transistor, the previous design methodology will also permit designing transistors with large W_N.

III. Basic Functions

A. The Charge Pump

Implementing such a basic function, aimed at quickly shifting the gate voltage of the VDMOS above V_{BAT}, basically calls for a high-value pumping capacitor C_{pump} as well as an ideal switching device that should allow transport of charges from C_{pump} onto the VDMOS gate on one phase (φ_1) and act as an open circuit on the next phase (φ_2) so that when C_{pump} charges up, the switch will prevent the VDMOS gate from discharging.

P-N junction based diodes would be useful to implement the switching device, however, they are not compatible with the isolation possibilities of the previous simple technology. A diode-like NMOS device, $T1$ in Fig. 10, is then generally used [9] in classical implementations of MOS charge-pump circuits, with the drawback that its nonideal switching behavior brings about an offset in $T1$ which leads to slowly charging the VDMOS gate on φ_1. Transistor $T2$ is aimed at charging up C_{pump} on φ_2 when the level shifter is low and is also responsible for the overall speed performance of this circuit. Another important concern is that, since grounded p^- wells are used to properly isolate the NMOS from the substrate, a problem arises when the level shifter goes to zero and the VDMOS gate is still low. Indeed, node N then swings negative, a situation that will bring about latchup [10], since an n^+-p^- junction is being forwardly biased.

The circuit in Fig. 11 is compatible with the previously detailed VDMOS–CMOS technology and brings about a solution to each and every problem related with Gupta's earlier circuit [9].

Indeed, the switch transistor $T1$ is now replaced by a depletion-mode MOS transistor $ND2$ with floating p^--substrate so that it operates as an almost ideal switch, since the p^--well voltage will be able to follow the VDMOS gate voltage V_{DG} and no offset occurs during phase φ_1.

The charging action of transistor T_2 in Fig. 10 is now replaced, in Fig. 11, by the emitter current of two parasitic vertical bipolar transistors, T_{b1} and T_{b2}, which are sought to perform intensively during a short period of time.

T_{b1} has its emitter coincident with the diffusion n^+ of $ND2$ at node D and its base is the floating p^--substrate of $ND2$ (node B). T_{b2} has its emitter coincident with diffusion n^+ of transistor $ND2$ at node N.

The rapid voltage variation of V_{DG} moving up to V_{BAT} and beyond will be achieved in two steps.

During the first step ($S1$), V_{DG} moves up to $V_{BAT} - 0.6$ V, driven by the strongly turned on transistor T_{b1}, which

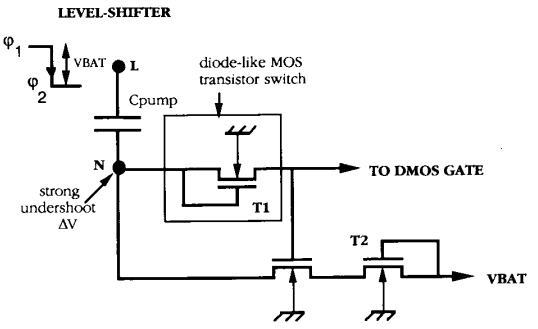


Fig. 10. Electrical schematic of an MOS charge-pump circuit [9].

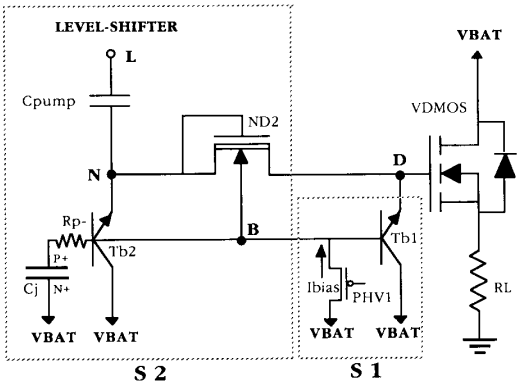


Fig. 11. Electrical schematic of a floating-well-based charge-pump circuit.

is possible since the p^--well substrate is allowed to float. In order to turn on T_{b1}, a controlled current source I_{bias}, flowing across the p^- well, is implemented, with the aid of a HV strongly biased p-channel device (PHV1). By the end of $S1$, the p^- well reaches its maximum value, V_{BAT}, and PHV1 is disabled.

During $S2$, since I_{bias} is no longer available, the only active device that may contribute to further increasing V_{DG} above $V_{BAT} - 0.6$ V is T_{b2}. Indeed, the level-shifter action is such that C_{pump} is sequentially charged up by T_{b2} to $V_{BAT} - 0.6$ V (φ_2: level shifter low). When the level shifter goes high (φ_1), C_{pump} can go up to $2V_{BAT} - 0.6$ V and $ND2$ will transmit the previously stored charge from C_{pump} onto the VDMOS gate.

It is important to emphasize that although the already mentioned undershoot (negative voltage) on node N will also occur in this case, it will not bring about any latchup originating situation since T_{b2} does not only provide fast charging of C_{pump} but also introduces the necessary feedback between N and B (floating V_{pwell}) so that no uncontrolled current is injected into the epilayer (n^- substrate).

For the charge pump to be efficient, it is important that C_{pump} be fully charged up on the low-going transition (φ_2) of the level shifter. This is achieved when the driving capability of T_{b2} is much larger than the output conductance of the pull-down transistor in the level-shifter circuitry

(not shown). It appears that, by including a n^+-p^+ junction (C_j) with sufficiently large area within the peripheral deep p^+ ring that surrounds $ND2$ (Fig. 1), it is possible to provide T_{b2} with sufficiently large base current transients, originating from C_j, so that the requested large driving capability is obtained for the emitter of T_{b2} on φ_2.

The frequency at which the level-shifter can be exercised will have to be such that C_{pump} is fully charged on φ_2. Indeed, the larger C_{pump} is designed, the larger its internal time constant τ will be. There is a trade-off, therefore, between the size of C_{pump} and the level-shifter frequency. For the circuit to work properly, it is most important that the cutoff frequency of the circuit supplying base current to T_{b2} be made much larger than $1/\tau$, which is achieved by making RP^- as small as possible.

The physical behavior of this circuit can then be numerically estimated. In particular, the turn-on time T_{ON}, which is the single most important feature of this high-side circuitry, can be roughly computed as follows. Given the internal resistance of C_{pump}, R_{n^+cap}, contributed by the underlying n^+ cap conductive electrode, it is possible to estimate τ by

$$\tau \approx R_{n^+cap} \cdot C_{pump} \tag{2}$$

which computes the maximum frequency of the oscillator that will have to be implemented in order to produce the level-shifter signal. By taking, $C_{pump} = 50$ pF and a typical value for $R_{n^+cap} = 10$ kΩ, we obtain $\tau = 500$ ns. Turn-on time is then given by

$$T_{ON} \approx \frac{C_{VDMOS}}{C_{pump}} \cdot \tau. \tag{3}$$

The design of this circuit has been carried out and the result of the SPICE simulation given in Fig. 12 shows a turn-on time of 20 μs, which is in good agreement with the value obtained from (3). Fig. 13 describes the cross section of a silicon implementation, used for this simulation, that includes most of the previously described devices, conveniently packed and sufficiently close to one another so that they make up a single block embedded in the p^--well substrate that is surrounded by the PAC protective termination.

The largest useful value of C_{pump} that has been used in the previous simulation is given by [11]

$$C_{pump} = h_{FE}(T_{b2}) \cdot C_j \tag{4}$$

where h_{FE} is the dc current gain of the PVB T_{b2}.

Equation (4) will now be deduced. If node N undergoes a negative voltage variation δV_N during the transient, the integrating current I_{cp} on C_{pump} during δ_t is given by

$$I_{cp} = \frac{C_{pump}}{\delta_t}(\delta V_L - \delta V_N) \tag{5}$$

where δV_L is the incremental negative voltage swing on the level-shifter side of C_{pump}.

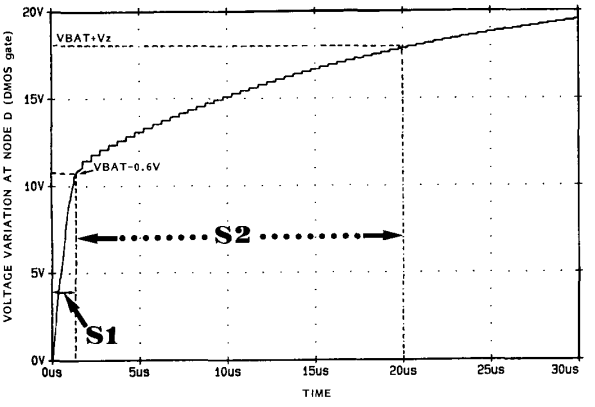


Fig. 12. Result of a SPICE simulation of the charge-pump circuit given in Fig. 11. The main parameters used are: $C_{VDMOS} = 2$ nF, $C_{pump} = 50$ pF, $C_j = 5$ pF, $f_{pump} = 2$ MHz, and $h_{FE} = 10$.

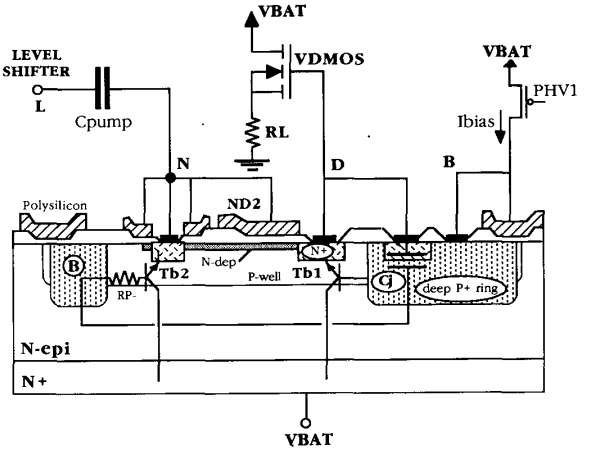


Fig. 13. Cross section of the silicon implementation of the main devices involved in the charge-pump circuit given in Fig. 11.

The instantaneous emitter current I_E of T_{b2} is given by

$$I_E = C_j \cdot h_{FE} \cdot \frac{\delta V_B}{\delta_t} \tag{6}$$

where δV_B is the base voltage variation of T_{b2}.

Assuming $\delta V_N = \delta V_B$, in agreement with the assumption that T_{b2} has a sufficiently large driving capability, we obtain, after equating I_E and I_{cp}:

$$\delta V_N = \frac{\delta V_L}{1 + C_j \dfrac{h_{FE}}{C_{pump}}}. \tag{7}$$

The amount of charges, Q_{int}, integrated on C_{pump} over the phase φ_2 is then

$$Q_{int} = C_{pump} \int_0^{\varphi_2} (\delta V_L - \delta V_N)\, dt. \tag{8}$$

On introducing (7), we get

$$Q_{int} = C_{\text{pump}} \int_0^{-V_{BAT}} \left(1 - \frac{C_{\text{pump}}}{C_{\text{pump}} + C_j \cdot h_{FE}}\right) \delta V_L \quad (9)$$

since when φ_2 is completed, the voltage variation on node L is $-V_{BAT}$. We then obtain

$$Q_{int} = C_{\text{pump}} V_{BAT} \left(1 - \frac{C_{\text{pump}}}{C_{\text{pump}} + C_j \cdot h_{FE}}\right) \quad (10)$$

which shows that C_{pump} values in excess of $C_j \cdot h_{FE}$ do not contribute a significant increase in Q_{int} for a given V_{BAT}, which is in agreement with (4).

It should be noticed that obtaining the requested large driving capability of T_{b2} amounts to reducing the negative swing of V_N, during φ_2, to a minimum value. During this phase (φ_2), however, there is a tendency for the gate of the VDMOS (node D) to leak current back on to C_{pump} through $ND2$.

The amount of this leakage is proportional to $[V_{DG} - (V_{BAT} - 0.6\text{ V}) + V_N]$, where V_{DG} is the current voltage on node D. This leakage will discharge D only during the transient (φ_2). Therefore, only the largest values of V_{DG}, taking place at the end of T_{ON}, will begin producing significant leakage. In addition, the requested high frequency of the charge-pump circuit also contributes to reducing this deleterious effect on the turn-on time of the VDMOS switch.

B. Other Functions

Of course, a smart power switch is not complete without at least the following additional circuits: a discharging device compatible with inductive loads, short-circuit detection and protection, overvoltage and gate protection, as well as a temperature detection device [12].

The logic section of the circuit will be mainly devoted to generating switching signals that will make up the status messages aimed at interfacing the central microprocessing unit external to the chip.

It can be shown that the previous functions are compatible with the preceding processing technology [13]. The corresponding circuits make extensive use of the floating-well concept, which, at this stage, appears to be not only related to dynamic shielding but also to lending itself to obtaining active devices.

IV. Conclusion

A simple processing technology leading to a low-cost, high-performance, power high-side switch is described. This technology is basically an MOS one on a high-resistance epilayer and therefore does not contain built-in junction isolation walls. Instead, it is shown that convenient, both static and dynamic, isolation is achieved by introducing a floating-well concept.

A floating well, if conveniently protected by a peripheral attenuator circuit, will decouple the well voltage from voltage fluctuations in the epilayer that result from turning on and off the VDMOS device, thereby isolating the logic section of the device from the power one.

The floating-well technique also lends itself to producing isolated capacitors, Zener devices, and a controlled vertical bipolar transistor, which prove to be useful in producing a reliable, low-consumption, fast-switching smart power high-side switch.

Indeed, the vertical bipolar transistor inherent to the n-channel MOS in a p^- well can be shown to be monitored in such a way that only controlled currents are driven into it. Therefore, by properly biasing the floating p^- well, it can be made to switch in such a way that it is possible to obtain the necessary fast charge-pumping circuitry.

Finally, we believe that this technology is properly suited to handle particularly high current values. Indeed, given its simplicity, the expected economically possible die size is likely to be amenable to large values.

References

[1] F. Conti and M. Conti, "Surface breakdown in silicon planar diodes equipped with field plates," *Solid-State Electron.*, vol. 15, pp. 93–105, 1972.

[2] S. Ogura *et al.*, "Elimination of hot electron gate current by the lightly doped drain-source structure," in *IEDM Tech. Dig.*, 1981, pp. 611–618.

[3] L. A. Glasser and D. W. Dobberpuhl, *The Design and Analysis of VLSI Circuits*. Reading, MA: Addison-Wesley, 1985, pp. 305–306.

[4] L. Wofford, "Silicon gates spur linear CMOS to bipolar speeds, holds offsets stable," *Electronics*, pp. 137–140, Mar. 24, 1982.

[5] Y. C. Kao and E. D. Wolley, "High voltage planar p-n junctions," *Proc. IEEE*, vol. 55, pp. 1409–1414, 1967.

[6] H. Wakaumi, T. Suzuki, M. Saito, and H. Sakuma, "A highly reliable 16 output high voltage NMOS/CMOS logic IC with shielded source structure," in *IEDM Tech. Dig.*, 1983, pp. 416–419.

[7] R. D. Rung and H. Momose, "DC holding and dynamic triggering characteristics of bulk CMOS latch-up," *IEEE Trans. Electron Devices*, vol. ED-30, pp. 1647–1655, Dec. 1983.

[8] M. Bafleur *et al.*, "Capacitive coupling of the floating body well to sensitive nodes prevents high resistance CMOS circuit from latching-up," *Electron. Lett.*, vol. 25, no. 13, pp. 860–861, June 22, 1989.

[9] A. Gupta *et al.*, "A 5V-only 16K EEPROM utilizing oxynitride dielectrics and EPROM redundancy," in *ISSCC Dig. Tech. Papers*, Feb. 1982, pp. 184–185.

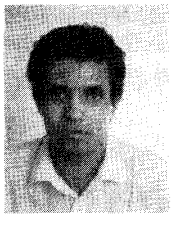
[10] Y. Yatsuda *et al.*, "Hi-NMOS II technology for a 64-kbit byte-erasable 5V only EEPROM," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 1, pp. 144–151, Feb. 1985.

[11] A. Elmoznine, "Définition d'une méthodologie de conception et étude des fonctions de contrôle et de protection d'un commutateur de puissance intelligent," Ph.D. dissertation, Univ. Paul Sabatier, Toulouse, France, no. 522, Oct. 2, 1989.

[12] M. Bafleur *et al.*, "CMOS compatible, self-biased bipolar transistor aimed at detecting maximum temperature in a silicon integrated circuit," *Electron. Lett.*, vol. 24, no. 16, pp. 1022–1024, Aug. 4, 1988.

[13] A. Elmoznine *et al.*, "The smart power switch: Description of a specific technology, its basic devices and monitoring circuitries," presented at the Symp. High Voltage and Smart Power ICs, 175th Meeting Electrochem. Soc., Los Angeles, CA, May 7–12, 1989.

*



Abdellatif Elmoznine was born in 1961 in Eljadida, Morocco. He received the Master's Science degree in electronics engineering from the Paul Sabatier University, Toulouse, France, in 1986, and the Ph.D. degree from the Laboratoire d'Automatique et d'Analyse des Systèmes (LAAS), Centre National de la Recherche Scientifique (CNRS) in Toulouse, France, in October 1989.

His dissertation dealt with the design of the monitoring circuitry of a smart power high-side switch.

Jean Buxo was born in Sabadell, Spain, in April 1941. He received the Docteur ès-Science degree in 1972 from the Paul Sabatier University in Toulouse, France.

He is employed by the Centre National de la Recherche Scientifique (CNRS) at the Laboratoire d'Automatique et d'Analyse des Systèmes (LAAS) in Toulouse, France. His research activities has been devoted to device physics and particularly to the theoretical and electrical characterization of electrically erasable programmable memories relying on Fowler-Nordheim tunneling. In relation with this field, he developed a EEPROM memory prototype at Harris Semiconductor, Melbourne, FL. From 1981 to 1985, he was involved in custom and semi-custom CMOS design. Now he is Director of Research, and since 1986, his research work has been focused on smart power integrated circuit design in collaboration with European and American manufacturers and Universities. He has published as author or co-author a number of papers on semiconductor devices (MIS, MISS), CMOS design, and smart power integrated circuit design.

*

Marise Bafleur was born in June 1956 in Gimont, France. She received the Engineer Degree in solid state physics in 1979 from the Institut National des Sciences Appliquées, Toulouse, France, and the Docteur-Ingénieur degree and Docteur ès-Science degree in 1982 and 1987, respectively, from the Paul Sabatier University, Toulouse, France.

Since 1983, she has been employed by the Centre National de la Recherche Scientifique (CNRS) at the Laboratoire d'Automatique et d'Analyse des Systèmes (LAAS) in Toulouse, France. From 1979 to 1982, she was working on defect characterization of molecular-beam-epitaxy (MBE) grown GaAs layers. She spent one year at IBM-COMPEC, Bordeaux, France, working on integrated circuits' characterization via reverse engineering techniques. From 1983 to 1987, her research activities was devoted to CMOS digital integrated circuit design and modeling of their dynamic behavior. Since 1987, she has been involved in smart power IC design and technology. She has published as author or co-author a number of papers on MBE GaAs layers characterization, CMOS design, and smart power integrated circuit design.

*

Pierre Rossel (M'75) was born in Banyuls-sur-Mer, France, on March 31, 1943. He received the Ingenieur Degree in Electrotechnics in 1965 from the Ecole Nationale Superieure d'Electrotechnique, Electronique et Hydraulique of Toulouse, France, and the Docteur Ingenieur degree and the Docteur ès-Sciences degree in 1968 and 1973, respectively, from the University Paul Sabatier, Toulouse, France.

From 1965 to 1967, he was an Assistant Professor at the University Paul Sabatier, and since 1968 he has been employed by the Centre National de la Recherche Scientifique (CNRS) at the Laboratorie d'Automatique et d'Analyse des Systèmes (LAAS), Toulouse. From 1973 to 1985, he was the head of the research team on field-effect devices at the LAAS. Now he is Director of Research, and he is managing a research group of about 35 scientists in the area of MOSFET devices and circuit design. Since 1976, his research activities have been devoted to studies on power MOS devices, including technology, integration, and dc and dynamic properties. He has published as author or co-author a number of papers on semiconductor devices (MOSFET and GaAs FET), design, analysis, and modeling.

Dr. Rossel is a member of the Société Francaise de Physique.