Modeling and improvement of a metallization system subjected to fast temperature cycle stress

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Abstract

The device failure of DMOS transistors under repetitive inductive load switching is dominated by the thermomechanical deformation of the metallization. The failure evolution is thus experimentally studied with special test structures and highlighted by thermomechanical FEM-simulation. Based on these findings a novel metallization concept is shown, which improves the fast temperature cycle reliability.

1. Introduction

For a broad field of automotive applications, electronic units are supported by integrated low-side switches [1]. An example for a transistor broadly used in this field is the quasi-vertical double-diffused-MOS (VDMOS) introduced with the first BCD technology [2][3][4]. These power transistors are applied to drive the inductive loads with applications like Engine Management or the Anti-Lock-Braking System (ABS).

The inductive load opposes to the current change by an increase of its terminal voltage when the gate is switched-off (Fig. 1). A zener-clamp between the drain and the gate prevents the VDMOS from avalanche and the current decays with the adjusted clamping voltage. Therefore the Drain-Source voltage in the off-state is approximately 100 times higher than in the on-state. This causes a high initial power dissipation for the VDMOS and leads to a sharp temperature rise within a fraction of milliseconds (see schematic drawing in Fig. 1).

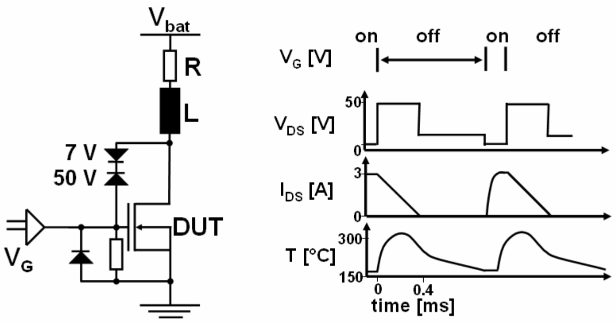

Figure 1: Circuit-diagram of a low-side switch driving an inductive load. The relationship between V_{DS}, I_{DS} and temperature T is schematically shown on the right.

During lifetime the VDMOS switches are subjected to a large number of these temperature pulses (10^4 – 10^9). As the metallization has a higher coefficient of thermal expansion (CTE) than the underlying silicon substrate, a thermomechanical stress is introduced with the fast temperature cycling. The stress in the metallization is beyond its yield point and therefore causes a viscoplastic deformation of the aluminum, whereat an additional amount of viscoplastic deformation is accumulated with each switching cycle. This finally results in cracking of the passivation and the interlayer dielectric (ILD), with the consequence of extruding aluminum causing short-circuits and device failure (Fig. 2).

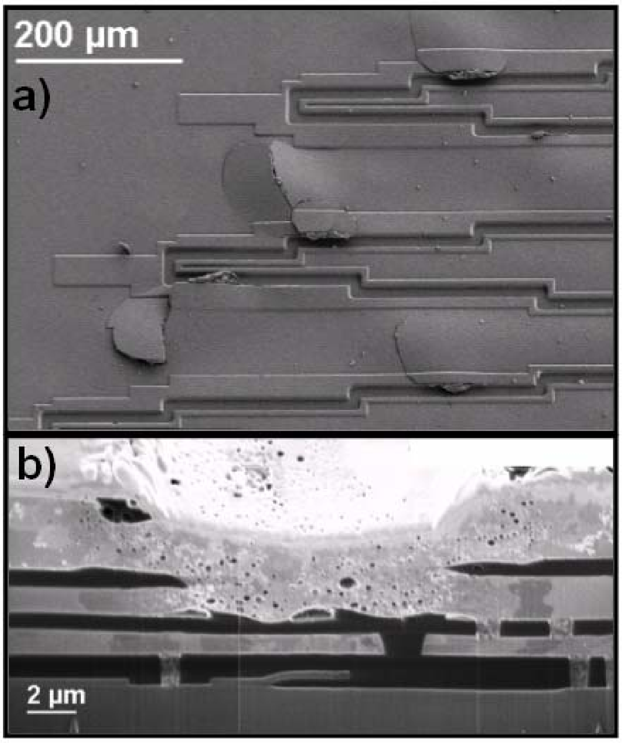

Figure 2: a) SEM-image of a DMOS-switch after exposure to fast temperature-cycle stress. Massive buckling of the metallization and passivation cracks are visible, from which aluminum extrudes.
a) FIB-cross section of a failure spot: A power overshoot results from the short-circuit and leads to a local melting & evaporation of the aluminum.

2. Thermomechanical Test Structures

Experimental. Special thermomechanical test structures are applied to investigate the fast temperature cycle reliability of a metallization system. These test structures consist of square plates of poly-silicon (600 µm x 600 µm), which are electrically contacted from two sides. By applying a voltage pulse on these resistors, they

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can be used as heating plates. A meandering aluminum line is located above the plate. The meander is traversed from both sides by conductor lines, which allow the detection of lateral short circuits (Fig 3). The meander and the extrusion monitors have the same line width and are separated by 0.8-µm-wide oxide walls. Furthermore, the meandering line and the extrusion monitors are covered by a stack of oxide and aluminum, which allows for the detection of vertical short circuits (see inset Fig. 3). Those can occur either from the meander to the plate or from the extrusion monitor to the plate.

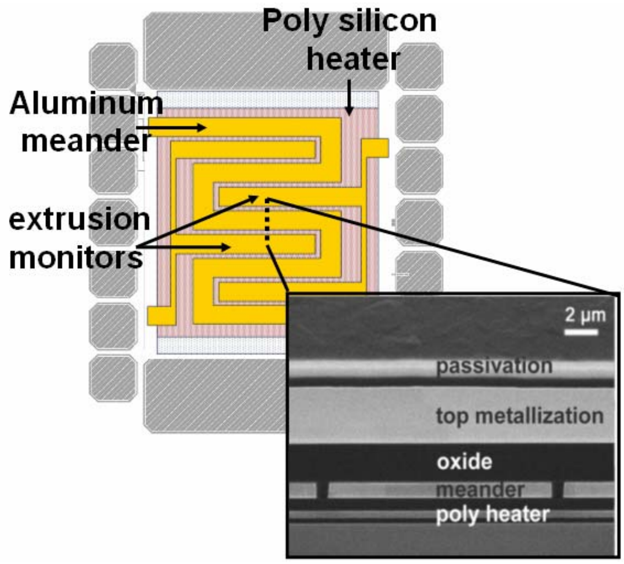

Figure 3: Schematic top view of the test structure: By using the poly-silicon heating plate, fast temperature cycling (10 - 100 Hz) of the metallization is possible without having current flow in the metallization. The inset shows a FIB cross-section of the test structure.

Failure Modeling. The time-to-failure data obtained with the thermomechanical test structures shows an increasing lifetime with decreasing temperature rise (ΔT) [5]. Differential interference contrast microscopy (DICM)-images of stressed devices (ΔT = 300 K, $1 \cdot 10^6$ cycles) reveal a strong deformation of the covering aluminum plate, whereat the thickness of the aluminum layer increased in the center of the structure (Fig. 4). Additionally buckling of the layer evolved. The ring-shaped structure of the deformation is caused by the temperature distribution across the device, in particular the gradient in temperature [5]. A change in the direction of the shear stress acting on the film is observed at the location of the maximum gradient in temperature (see draft in Fig. 4). The shear stress biases the fast temperature cycling and causes one-directional shifting of the metallization [6]. This ratcheting-like deformation of the film accumulates with every temperature cycle, as known for passive temperature cycle tests [7].

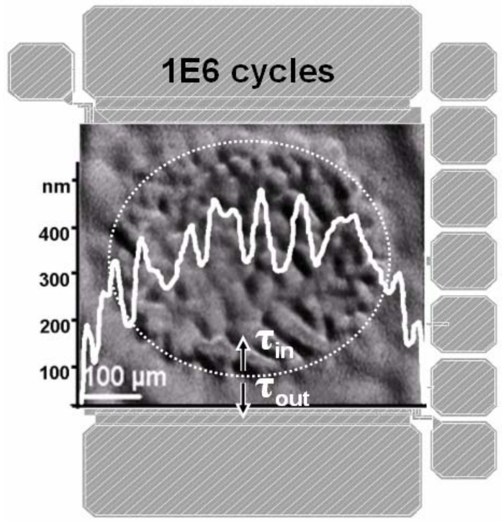

Figure 4: DICM-image of the covering aluminum plate after $1 \cdot 10^6$ cycles. The profile measurement illustrates the evolution of inhomogenities in the film thickness.

Electrical probing shows that the device failure is caused by a short-circuit between the conductor lines of the meandering layer. To investigate the impact of the fast temperature cycle stress on the conductor lines, the covering aluminum plate is removed by polishing. A DICM-image of an as-prepared device (ΔT = 300 K, $1 \cdot 10^6$ cycles) is shown in Fig. 5. The deformation of the lines is maximum in the center of the structure, as observed with the covering plate. Failure mapping for 12 devices shows that all short-circuits occur in the center of the structure where the maximum deformation of the lines is observed.

The FIB-cross-section of a failure spot shows a crack, which has propagated from the edge of one conductor line to the neighbouring one (see inset Fig. 5). Energy dispersive X-ray spectroscopy (EDX) reveals that the crack is filled with aluminum, which accounts for the short-circuit. Distance measurements on as-obtained FIB-images show an increase in the thickness of the conductor lines by up to 10%.

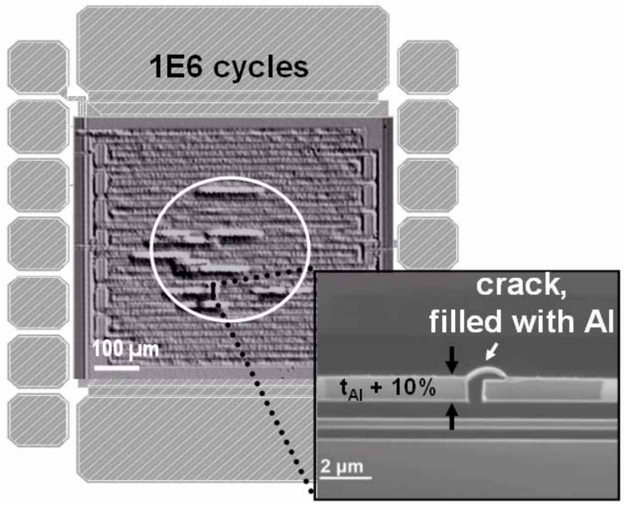

Figure 5: DICM-image of the conductor lines after 1•10^6 cycles. The covering aluminum plate was preliminarily removed. The inset shows a FIB-cross-section of the short circuit between two neighbouring conductor lines.

Simulation. The viscoplastic deformation of the aluminum lines is the root-cause for the failure evolution, as the locally increasing layer thickness causes an increasing stress on the interlayer dielectric. This failure evolution was assessed by thermomechanical simulations carried out using the FEM-code ANSYS. For the thermal and subsequent mechanical analysis a two-dimensional model of the test structure has been set (thermal: *plane55*; mechanical: *plane182*, plane strain). As the temperature distribution is decisive, a temperature profile is generated with the thermal analysis (Fig. 6). With the mechanical analysis the model is then cycled between the as-generated profile (= on-state) and a homogenous temperature of 125°C (= off-state). For the mechanical simulation the aluminum is modeled with a non-linear kinematic hardening model (Chaboche) [8][9].

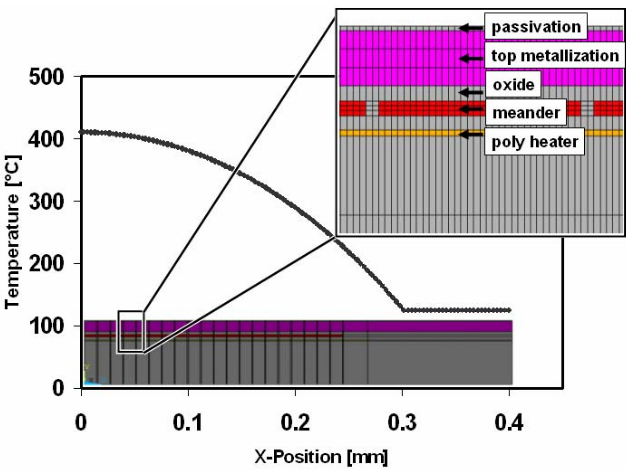

Figure 6: FEM-model of the thermomechanical test structure and the applied temperature profile.

The accumulated plastic deformation in the aluminum metallization after 2000-simulated-temperature-cycles is shown in Fig. 7. The highest amount of deformation is observed within the covering aluminum plate in the center of the structure. However, the device failure is observed to be an electric short-circuit between to the neighbouring conductor lines (see Fig. 5). Therefore the progression of the accumulated plastic deformation is evaluated for the cross-section of a conductor line in the center of the structure (Fig. 7a). It is noticed that it rises linearly with increasing number of loading cycles.

Additionally, the impact of the plastic deformation of the conductor lines on the stress level within the ILD is evaluated from the simulation. For this purpose, the progression of the first principal stress is analyzed within the ILD (Fig 7b). This shows an increasing stress level, whereat the amplitude between on- and off-state stays almost unchanged after 500 loading cycles. A tensile-only loading is observed from approximately 1000 cycles on, while the maximum stress value continuosly increases. This finally results in ILD cracking and the device failure beyond a critical stress level. In the next section mechanical measurements are performed to assess a criterium for the oxide fracture.

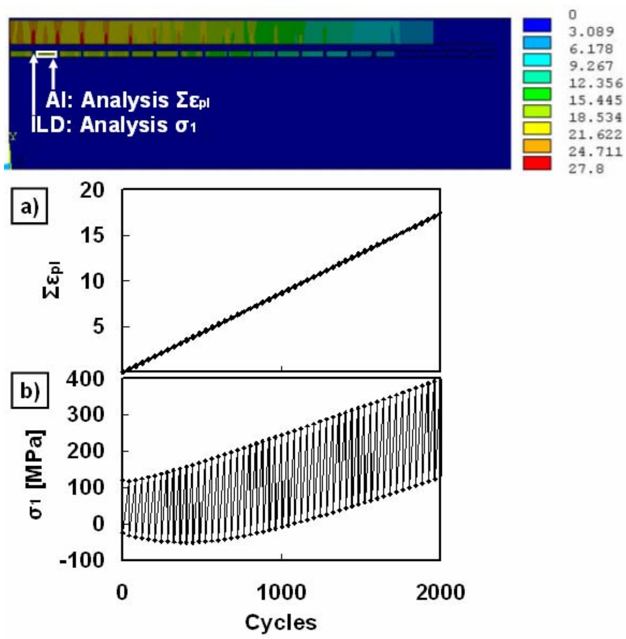

Figure 7: Accumulated plastic deformation after 2000 simulated temperature cycles. a) The plastic deformation accumulated in the cross-section of a conductor line increases linearly. b) The first principal stress within the ILD increases with increasing number of loading cycles.

3. Mechanical measurements ILD

Both elastic and fracture properties of the ILD layers have been extracted from bulge tests, that is the measurement of the deflection profiles of diaphragms resulting from applied uniform pressure loads. Membranes made of silicon oxide deposited by PECVD have been processed from the bulk micromachining of silicon wafers and characterized. Properties extracted from these films included the plane-strain modulus E_{ps}, pre-stress σ_0 and Weibull parameters (mean fracture strength μ and modulus m). The bulge test uses a setup where up to 80 membranes on a silicon wafer can be characterized in a single series of sequential measurements [10,11]. This enables the efficient acquisition of large data sets necessary, e.g., for the determination of reliable fracture data. The membrane profiles resulting from pressure loads are measured with an auto-focus sensor integrated with automated position tables for scanning purposes. A peculiarity of these bulge experiments is the use of diaphragms with large side length aspect ratios. This makes it possible to formulate and apply an accurate, analytical model of the diaphragm mechanics including multilayers with individual prestress and mechanical constants, and the support stiffness, as explained in detail elsewhere [10,11]. The membranes are bulged until failure and the stress distribution at fracture is used to extract the brittle material strength through Weibull distributions [10,11]. Figure 8 shows the probability of failure of 400-nm-thick silicon oxide films deposited by PECVD at 300°C as a function of the fracture strength thus obtained. The Weibull distribution function is fitted to the experimental data from which a mean fracture strength of 540 MPa and a Weibull modulus of 5.8 are extracted. From the measured load-deflection dependences, not shown here, a plane-strain modulus of 72 GPa and prestress of −312 MPa are obtained.

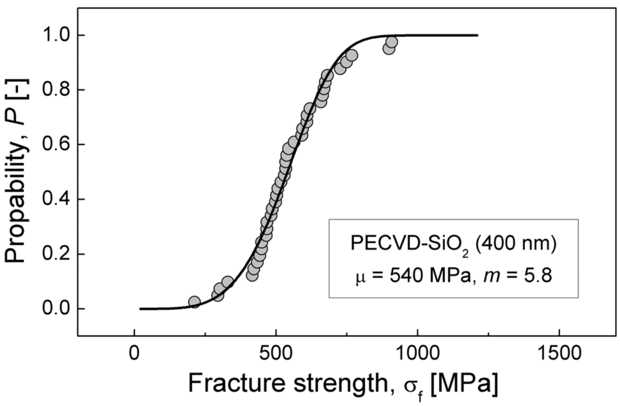

Figure 8: Pooled Weibull data and fit obtained from the bulge test of silicon oxide thin-film membranes. A mean fracture strength of 550 Mpa and a Weibull modulus of 5.8 are extracted.

4. Improvement of the metallization system

The failure of the devices is observed to be ILD fracture with the consequence of an electric short-circuit. However, the experimental investigations as well as the simulation results of section 2 demonstrate, that the deformation of the conductor lines is the root cause for the failure evolution. Therefore, a novel metallization system is introduced in this section which is supposed to improve the fast temperature cycle reliability. The alteration of the aluminum metallization is based on the investigations about the failure evolution: The starting point for the deviec failure is the deformation of the conductor lines. Hence, its reduction is the aim.

To realize this, we make use of the mechanical properties of thin metal films. The yield stress (σ_{yield}) of a thin metal layer is dependant on the film thickness: It increases with decreasing layer thickness [12,13]. We have shown in a previous publication that halving the layer thickness leads to an extension of the lifetime of conductor lines under fast temperature cycle stress [5]. However, this solution is not applicable as a DMOS metallization from a practical point of view. The reason is that by halving the layer thickness the current density is doubled and therefore the risk of electromigration failures is increased. To overcome this challenge we suggest a novel metallization concept. With this multi layer metallization, several thin aluminum layers are deposited consecutively, instead of the film deposition with one processing step. (Fig. 9).

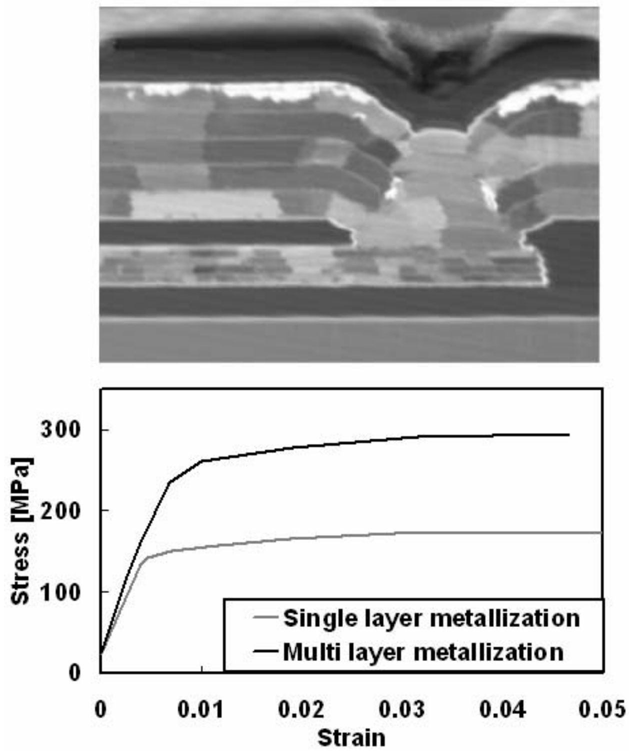

Figure 9: FIB-image of the novel metallization concept. The aluminum layers are deposited consecutively and are separated by thin TiN layers. The stress-strain curve is obtained via microcompression measurement and shows an increase in yield stress by approximately 70% for the multi layer metallization.

The resulting overal thickness of the stack is identical to the film thickness in case of the single layer deposition.

The difference is that the aluminum layers are separated each by a thin TiN layer (Fig. 9). Therefore the mechanical properties of the resulting multi layer film are more related to those of the individual thin films, than to those of a film with the total thickness. The stress-strain curve in Fig. 9 is obtained from microcompression measurements on ion-milled columns. It shows an increase in yield stress by approximately 70% for the multi layer metallization in comparison to the single layer.

The increase in yield stress should decrease the amount of plastic deformation, which is introduced to the conductor lines with each temperature cycle. Therefore an additional simulation is performed to evaluate this. The FEM-model is identical to the one shown in figure 6. As with the previous simulation the Chaboche material model is assumed for the aluminum. The only difference is found for the yield stress, which is adjusted according to the measurement shown in figure 9.

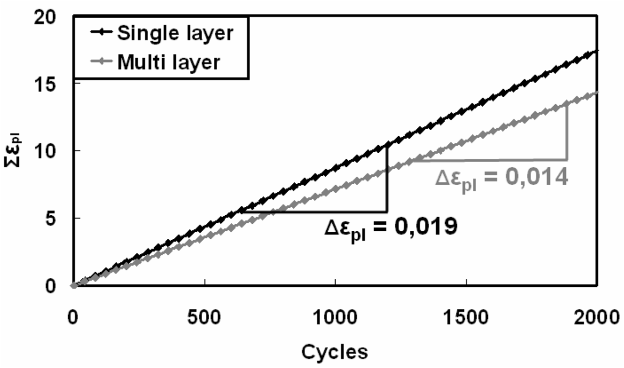

Figure 10: Weibull-plot of the time-to-failure data for test structures with single layer (black) and multi layer (grey) metallization.

The evolution of the accumulated plastic deformation within the cross-section of one conductor line (see figure 7) is shown in figure 10. It rises linearly with increasing number of loading cycles. For comparison the result of the simulation with the material model for the single layer is displayed additionaly. The plastic deformation per cycle can be evaluated from the slope of the two graphs (single layer: 0.019; multi layer: 0.014). This shows, that due to the increased yield stress the deformation per cycle is reduced by 26%.

According to the failure hypothesis shown in section 2, the reduction of the plastic deformation per cycle should increase the number of cycles to the device failure. To evaluate this experimentally, the thermomechanical test structures shown in figure 3 are fabriacted with a single and a multi layer metallization respectively. The two types of metallization are then loaded with identical stress conditions (ΔT = 300 K, T_{start} = 125°C) and the time-to-failure is monitored.

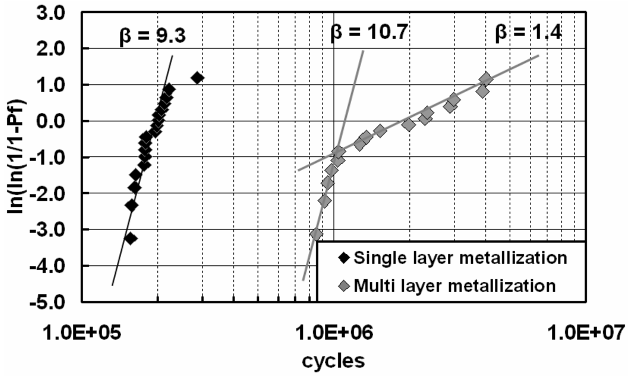

Figure 11: Weibull-plots of the time-to-failure data for test structures with single (black) and multi layer (grey) metallizations.

A Weibull-plot of the time-to-failure data is shown in Fig. 11. A bimodal distribution is observed in case of the multi layer metallization, whereat the first branch has a comparable slope as observed with the single layer metallization (β_{single} = 9.3; β_{multi_1} = 10.7). The second branch of the failure distribution has a lower slope (β_{multi_2} = 1.4). The evolution of a bimodal distribution in case of an extended endurance of the lifetest has already been discussed in a previous publication [5].

The appliance of the multi layer metallization shifts the mean time-to-failure by almost an order of magnitude. This shows the potential of the new metallization concept and substantiates the failure model for conductor lines under fast temperature cycle stress.

5. Summary

The failure evolution under fast temperature cycle stress is dominated by a thermomechanical deformation of the conductor lines, whereat an additional amount of deformation is introduced with each switching cycle. This leads to a rising stress level within the ILD with increasing number of loading cycles. The implementation of the multi layer metallization increases the yield stress of the conductor lines and therefore extends the lifetime as the amount of plastic deformation per cycle is reduced.

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