JEDEC STANDARD

Power and Temperature Cycling

JESD22-A105C

(Revision of JESD22-A105-B)

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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TEST METHOD A105C
POWER AND TEMPERATURE CYCLING

(From JEDEC Board Ballot JCB-03-70, formulated under the cognizance of the JC-14.1 Subcommittee on Reliability Test Methods for Packaged Devices.)

1 Scope

This test method applies to semiconductor devices that are subjected to temperature excursions and required to power on and off during all temperatures. The power and temperature cycling test is performed to determine the ability of a device to withstand alternate exposures at high and low temperature extremes with operating biases periodically applied and removed. It is intended to simulate worst case conditions encountered in typical applications.

The power and temperature cycling test is considered destructive. It is intended for device qualification.

2 Terms and definitions

2.1 Temperature cycle time

Time between one high temperature extreme to the next, or from one low temperature extreme to the next, for a given sample; see Figure 1.

2.2 Ramp rate

The rate of temperature increase or decrease per unit of time for the sample(s). Ramp rate should be measured for the linear portion of the profile curve, which is generally the range between 10% and 90% of the test condition temperature range; see Figure 1. Note: Ramp rate can be load dependent and should be verified for the load being tested.

2.3 Dwell time

The amount of time the sample temperature has exceeded the specified temperature, either the high or the low temperature; see Figure 1.

2.4 Power cycle time

Time between one power on to the next, or from one power off to the next, for a given sample; see Figure 1.

2 Terms and definitions (cont'd)

2.5 Duty cycle, power

The ratio of the power-on time duration per cycle to the total cycle time.

NOTE Power duty cycle is usually expressed as a percentage.

3 Apparatus

The apparatus required for this test shall consist of a controlled temperature chamber capable of producing the specified temperatures within the specified transition times. Sockets or other mounting means shall be provided within the chamber so that reliable electrical contact can be made to the device terminals in the specified circuit configuration. Power supplies and biasing networks shall be capable of maintaining the specified operating conditions throughout the testing period despite normal variations in line voltages or ambient temperatures. The test circuitry should also be designed so that existence of abnormal or failed devices does not alter the specified conditions for other units on test. Care should be taken to avoid possible damage from transient voltage spikes or other conditions that might result in electrical, thermal, or mechanical overstress.

4 Procedure

When special mounting or heat sinking is required, the details shall be specified in the applicable specification. The power should then be applied and suitable checks made to assure that all devices are properly biased. During the test, the power applied to the devices shall be alternately cycled 5 minutes on 5 minutes off unless otherwise specified in the applicable specification. The devices shall concurrently be cycled between temperature extremes for the specified number of cycles. The time at the high and low temperature extremes shall be sufficient to allow the total mass of each device under test to reach the specified temperature extremes with no power applied. The low temperature to high temperature transition or reverse sequence is acceptable.

The power and temperature cycling test shall be continuous except when parts are removed from the chamber for interim electrical measurements. If the test is interrupted as a result of power or equipment failure, the test may restart from the point of stoppage.

4 Procedure (cont'd)

4.1 Test conditions

The electrical bias circuit shall be specified in the applicable specification. The device shall be subjected to the test conditions derived from Table 1 as illustrated in Figure 1.

4.2 Precautions

Since case and junction temperatures of some devices can be significantly greater than ambient temperature, the circuit should be structured so that the maximum rated case or junction temperature shall not be exceeded. Precautions should be taken to avoid electrical damage and thermal runaway. Direct heat conduction to sample(s) shall be minimized. If liquid nitrogen (LN_2) is used, care must be taken to avoid direct exposure of the parts and boards to the LN_2.

The test setup should be monitored initially and at the conclusion of a test interval to establish that all devices are being stressed to the specified requirements. Deviations must be corrected prior to further cycling to assure the validity of the qualification data.

4.3 Solder interconnect considerations

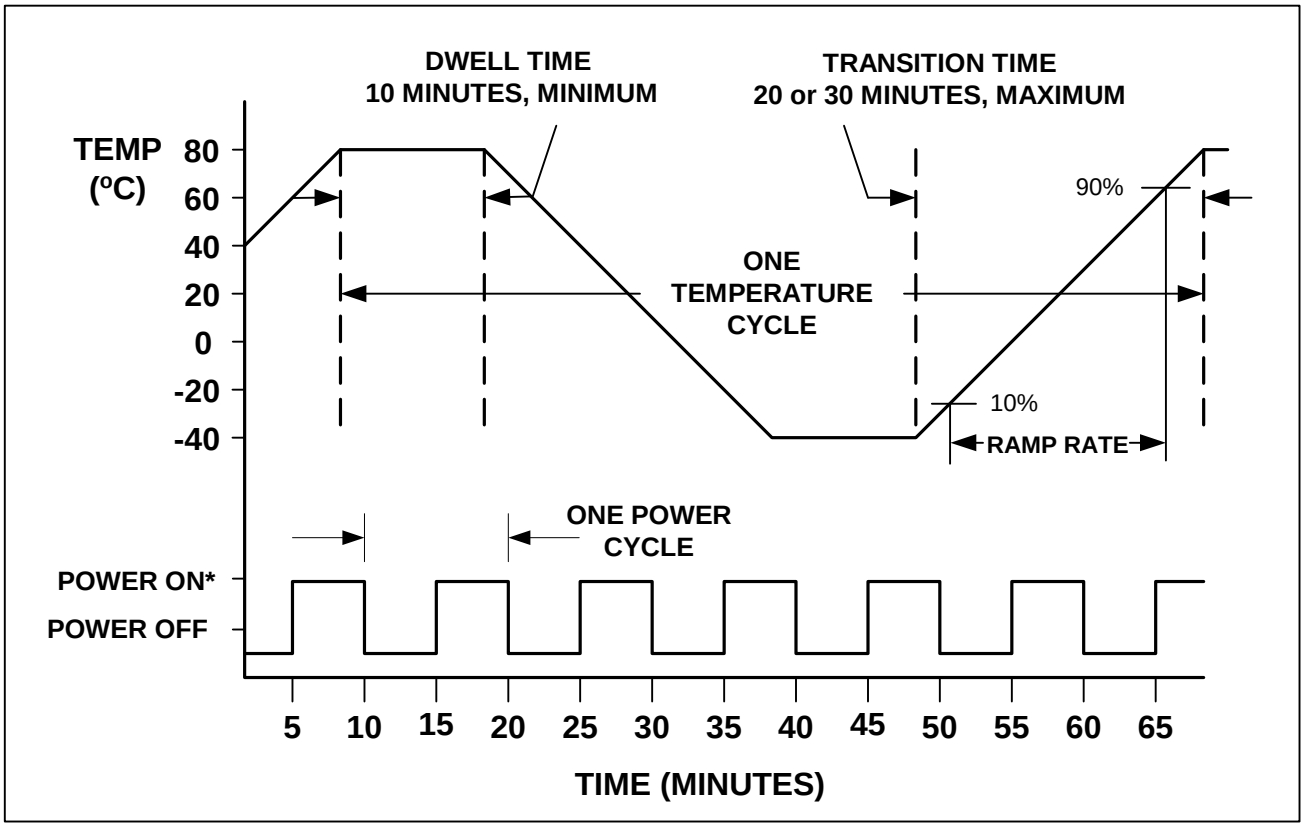
Devices with solder interconnects have cycle rates that are in the range of <1 to 2 cph. These include flip chip, ball grid array and stacked packages with solder interconnections. Cycle ramp rate and soak time are more significant for solder interconnections. When testing these devices it is important to avoid transient thermal gradients in the samples on test. Samples with large thermal mass and low heat transfer efficiency require ramp rates slow enough to compensate for the thermal mass. The temperature of the sample should be within a few degrees of the ambient temperature during the temperature ramps. Typical ramp rate for this situation is 15 °C/minute or less for any portion of the cycle. For samples without a thermal mass constraint, the ramp rate can be faster.

4 Procedure (cont'd)

4.3 Solder interconnect considerations (cont'd)

Table 1 — Typical Test Conditions

Test Condition	Temperature Extremes Degrees C.	Transition Time Between Temp Extreme, Max.	Dwell Time at Each Temp Extreme, Min.
A	-40(+0, -10) to +85(+10,-0)	20 minutes	10 minutes
B	-40(+0, -10) to + 125(+10, -0)	30 minutes	10 minutes



* Power cycle need not be synchronized with temperature cycle.

Figure 1 — Typical power and temperature cycle test condition

4 Procedure (cont'd)

4.4 Measurements

The electrical measurements shall be made at intervals per the applicable specification.

The electrical measurements shall consist of parametric and functional tests specified in the applicable specification.

5 Failure criteria

A device is defined as a failure if parametric limits are exceeded or if functionality cannot be demonstrated under nominal and worst case conditions specified in the applicable specification. Mechanical damage shall not include damage induced by fixturing or handling or the damage is not critical to the package performance in the specific application.

6 Summary

The following details shall be specified in the applicable specification:

a) Special mounting, if applicable.
b) Test conditions from Table 1.
c) Biasing conditions.
d) Power duty cycle, if other than specified in clause 4.
e) Test intervals.
f) Electrical measurements.
g) Sample size.
h) The number of temperature cycles.

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