A Gan Transistor based 90W AC/DC Adapter with a Buck-PFC Stage and an Isolated Quasi-Switched-Capacitor DC/DC Stage

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***Abstract*— This paper presents a GaN Transistor based 90W ac/dc adapter with a Buck-PFC stage and an isolated Quasi-Switched-Capacitor (QSC) dc/dc stage. In the dc/dc stage, two different QSC converters are proposed. Compared to Flyback and LLC resonant converters, the QSC converters feature: 1) reduced voltage stress on the primary-side switches to 2/3 of the input voltage; 2) reduced voltage stress on the transformer to 1/3 of the input voltage and a lower transformer turns ratio; 3) a wide range for soft-switching operation and high efficiency; 4) a simple control strategy. The operation principles and simulation results are presented. A 90 W, 85 V/19 V, 1 MHz QSC resonant converter is built, using 100 V EPC eGaN FETs for all switches. This prototype achieves: 1) a high power density of 10.5 W/cm^3; 2) wide-range soft switching and a peak efficiency of 92.8% at 900 kHz in preliminary test results. A Buck-PFC evaluation module from TI is tested with a GaN HEMT and a SiC Schottky diode. The peak efficiency reached 97.1%, and the experimental results are compared with those from the Si based version.**

I. INTRODUCTION

For portable electronics such as laptops, there exists an ever-increasing demand for high power-density and highly energy efficient power supplies. Fig. 1 shows the system structure of the ac/dc power adapter. The PFC stage regulates the input ac current to meet the current harmonic requirement such as the IEC61000-3-2 [1]. The isolated dc/dc stage steps down the dc-link voltage, and provides galvanic isolation for user safety.

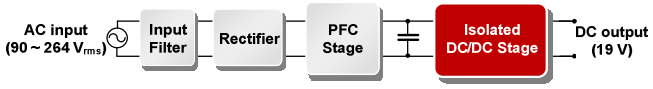


Fig. 1. System structure of the ac/dc power adapter.

For the isolated dc/dc stage, Flyback and Half-Bridge (HB) LLC resonant converters have been widely applied [2]-[7]. The Flyback converter features a simple structure and minimum switch count, but it requires a bulky transformer that is used for energy storing. HB LLC resonant converters can achieve both high efficiency and high power density. An isolated Quasi-Switched-Capacitor (QSC) dc/dc converter is proposed in [8]. Compared with Flyback and LLC resonant converters, it has the following features including: 1) the voltage stresses on the primary-side switches are reduced to 2/3 of the input voltage, which is friendlier to switches with low voltage rating; 2) the transformer turns ratio is reduce by 2/3, which enables less number of turns of the winding, lower winding loss and lower transformer leakage inductance; 3) a wide range for soft-switching operation and high efficiency; 4) a simple control strategy. [8]

For the PFC stage, the Boost-PFC circuit has been widely used [2]-[7]. It features very low THD and small hold-up capacitance. However, it has considerable drop in efficiency at low line voltage, and its output dc-link voltage is about 400 V, which requires switches with high voltage rating and a large transformer turns ratio in the downstream stage. Buck-PFC, on the other hand, is more efficient at low line voltage, and it provides a low output voltage of around 85 V, which enables lower common-mode (CM) noise, and more efficient design of the downstream dc/dc stage, using lower voltage switches with better figures of merit. [9] [10]

This paper presents a 90 W ac/dc adapter based on a Buck-PFC stage and an isolated QSC dc/dc stage. In the QSC dc/dc converter, a QSC dc/ac circuit with a 3:1 voltage step-down ratio is applied on the primary side, and 2 different rectifier circuits are applied on the secondary side to form 2 different topologies, including: 1) a QSC converter with a synchronous-rectifier, current-doubler (SRCD) circuit, and 2) a QSC resonant converter with a synchronous-rectifier, center-tapped (SRCT) circuit. The circuit descriptions, operation principles, and simulation results of the 2 topologies are presented herein.

GaN devices have the following benefits compared with Si devices: 1) they can operate at higher switching frequency,

which shrinks the size of the passive components; 2) they switch at faster speeds which lead to lower switching loss; 3) they have a lower figure of merit for the product of the on-resistance and the total gate charge, which leads to higher efficiency; 4) they have higher operating temperature which decrease the cooling requirement [11]-[13].

To verify the isolated QSC dc/dc stage, a GaN Transistor based 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit is built, serving downstream to a Boost-PFC stage. To pursue higher power density and higher efficiency, an eGaN FETs based 90 W, 85 V/19 V, 1 MHz QSC resonant converter with a SRCT circuit is built, serving downstream to a Buck-PFC stage. In this converter, low transformer leakage inductance and low stray inductance are achieved with a planar transformer that has interleaved windings and vias. Optimal PCB layout is conducted for the circuit to reduce the stray inductance. The prototype design and the experimental results are presented in this paper. To verify the Buck-PFC stage, a Buck-PFC evaluation module from TI is tested with a GaN HEMT and a SiC Schottky diode. Experimental results are provided and compared with those from the original Si based version herein.

II. The Isolated QSC DC/DC Stage

A. QSC Converter with a SRCD Circuit

The QSC converter with a SRCD circuit is shown in Fig. 2, and its waveforms are shown in Fig. 3 [8].

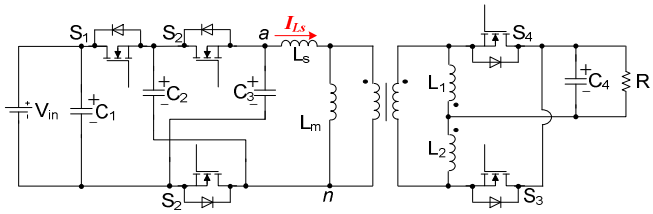


Fig. 2. The QSC converter with a SRCD circuit [8].

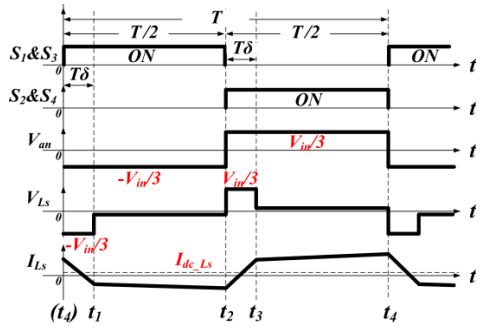


Fig. 3. Waveforms the QSC converter with a SRCD circuit [8].

Because of the steady-state volt-second balance of the transformer inductance and the inductors L_1, L_2 (L_1=L_2), in this converter: 1) the voltage stresses on S_1 and S_2 are reduced to $2V_{in}/3$; 2) the voltage stress on the transformer is reduced to $V_{in}/3$, and the transformer turns ratio is reduced. In addition, due to the steady-state ampere-second balance of C_2 and C_3 (C_2=C_3), the primary-side QSC dc/ac circuit generates a dc-offset current in the transformer. However, unlike in the Flyback converter, this dc-offset current doesn't result in a bulky core, nor does it require an air gap for the transformer. A secondary-side branch composed of L_1 and L_2 in series is connected in parallel with the transformer magnetizing inductance (L_m). Since the inductance of L_1 and L_2 are much smaller than L_m, a major part of the dc-offset current of L_m is shifted to L_1 and L_2. This prevents the transformer core from saturating and allows it to function without any air gap.

The transformer leakage inductance (L_s) causes current to freewheel through S_1 and S_2. This enables S_1 and S_2 to turn on under ZVS condition. The converter has a wide ZVS range. The output power of the converter is regulated by changing the switching frequency.

B. QSC Resonant Converter with a SRCT Circuit

The QSC resonant converter with a SRCT circuit is shown in Fig. 4 and its waveforms are shown in Fig. 5.

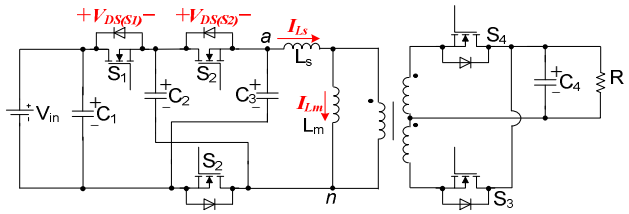


Fig. 4. The QSC resonant converter with a SRCT circuit.

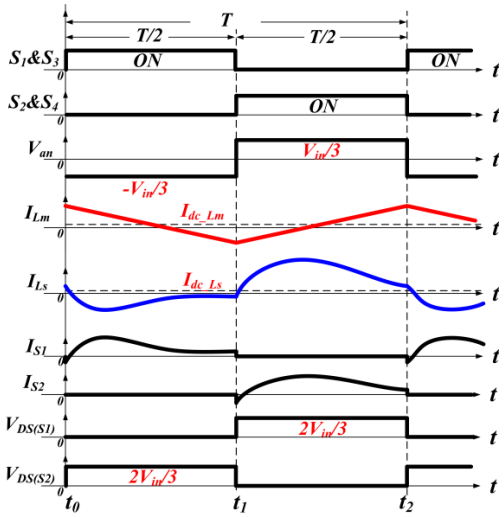


Fig. 5. Waveforms the QSC resonant converter with a SRCT circuit.

In this converter, soft-switching for all the switches can be achieved by generating resonant switch currents, as shown in Fig.5, utilizing the resonant tank composed of the switched capacitors C_2, C_3 (C_2=C_3), the transformer leakage inductance L_s, the output capacitor C_4 and the load resistor R. With a high switching frequency applied, the secondary-side inductors are no longer needed for filtering. Even though the primary-side circuit is generating a dc-offset current in the transformer, there is no need to add secondary-side inductors to sink the dc-offset current. This is because in resonance, the impedance of the output branch composed of L_s, C_4 and R is much smaller than that of L_m, and the major part of the dc-offset current of L_m is shifted to the output branch. As a result, the output voltage ripple is unsymmetrical, and I_{s3} and I_{s4} are unbalanced.

In steady-state, the converter has 2 major switching modes in a switching cycle (T). Fig. 6 (a) shows the equivalent circuit of Mode 1 (t_0-t_1), and Fig. 6 (b) shows the equivalent circuit of Mode 2 (t_1-t_2). The red circles indicate the current loop of L_m, and the blue circles indicate the loop of the output current.

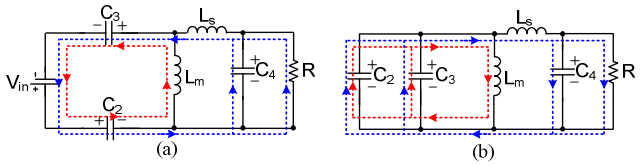


Fig. 6. (a) The equivalent circuit of Mode 1 (t_0-t_1), and (b) the equivalent circuit Mode 2 (t_1-t_2) of the QSC resonant converter with a SRCT circuit.

It can be inferred from the red circles that, because of the volt-second balance of L_m, the voltage of C_2 and C_3 (V_{C2} and V_{C3}) remain $V_{in}/3$ despite the small ripple caused by the resonance, and I_{Lm} changes linearly. As a result, in this converter: 1) the voltage stresses on S_1 and S_2 are reduced to $2V_{in}/3$; 2) the voltage stress on the transformer is reduced to $V_{in}/3$, and the transformer turns ratio is reduced.

To define the resonant frequency required for achieving soft switching, the output current loop as shown in the blue circles in Fig. 6 is studied. Although the current of L_m is also part of the switching currents, it is much smaller than the load current, so L_m is ignored to simplify the analysis. The circuit functions as two LCC resonant circuits in the two switching modes, where each mode has 2 different values for the resonant frequency. Depending on the loading, the circuit resonant frequency varies between the two values.

In Mode 1 (t_0-t_1), C_2 and C_3 are connected in series, so the two resonant frequencies are:

- When $R = 0$, which means a short-circuit output, C_4 is shorted. The resonant frequency is

$$F_{\min 1} = \frac{1}{2\pi\sqrt{L_s \cdot \frac{C_2}{2}}}$$

- When $R = \infty$, which means an open-circuit output, C_4 is in series with C_2 and C_3. The resonant frequency is

$$F_{\max 1} = \frac{1}{2\pi\sqrt{L_s \cdot \frac{C_2 C_4}{C_2 + 2C_4}}}$$

In Mode 2 (t_1-t_2), C_2 and C_3 are connected in parallel, so the two resonant frequencies are:

- When $R = 0$, which means a short-circuit output, C_4 is shorted. The resonant frequency is

$$F_{\min 2} = \frac{1}{2\pi\sqrt{L_s \cdot 2C_2}}$$

- When $R = \infty$, which means an open-circuit output, C_4 is in series with C_2 and C_3. The resonant frequency is

$$F_{\max 2} = \frac{1}{2\pi\sqrt{L_s \cdot \frac{2C_2 C_4}{2C_2 + C_4}}}$$

For both the 2 switching modes, as the load gets heavier, the resonant frequency will shift to higher frequency. Mode 1 has a higher resonant frequency compared with Mode 2. The switching frequency (f_s) has to be chosen according to the resonant frequency of Mode 1, so that: 1) both S_1 and S_2 have ZVS on and their turning-off loss is reduced; 2) the current of S_1 will not resonate to negative value. In soft switching, the switch current of S_3 and S_4 follow the similar pattern of the S_1 and S_2, leading to very low switching loss for S_3 and S_4.

III. The Buck-PFC Stage

The Buck-PFC based ac/dc stage circuit is shown in Fig. 7. The output dc-link voltage is set at around 85 V, less than the lowest ac line peak voltage. Similar to the Boost-PFC stage, the Buck-PFC is controlled using an outer voltage-control loop to regulate the dc-link voltage, with an inner current-control loop to control the average current shape. The average ac line current follows a pseudo-sinusoidal shape and essentially widens the conduction angle to deliver the required PF performance [9].

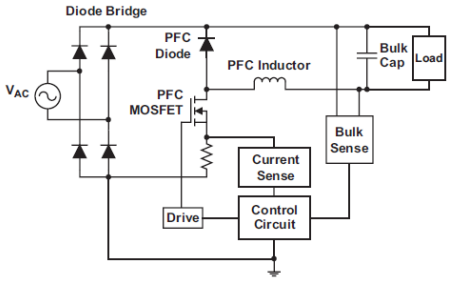


Fig. 7. Buck-PFC based ac/dc stage [9].

The Buck-PFC circuit can operate in the continuous-conduction mode (CCM) [14], discontinuous-conduction mode (DCM), and critical-conduction mode (CRM) [15]-[16]. CCM operation leads to small inductance of the PFC inductor but high reverse-recovery loss of the diode. DCM operation can provide good PF performance with simple control, but it causes high switching loss and high inductor current ripple which requires a big size of the PFC inductor. CRM operation can eliminate the reverse-recovery loss of the diode, and achieve ZVS ON for the switch, and therefore lead to high efficiency.

For moderate power levels up to approximately 150 W, the Buck-PFC can be designed to operate in DCM at high line voltages (>160 Vac) over the full load range, and in CCM at low line voltages, heavy load conditions. This allows a compact PFC inductor design and enables the usage of a low-cost ultrafast PFC diode [9].

IV. Simulation Verifications

A. Simulation Results of the QSC Converter with a SRCD Circuit

A simulation model of the QSC converter with a SRCD circuit is built in PSIM. The circuit parameters are as follows: V_{in}=400 V, V_{out}=19 V, N=3:1, L_m=4 mH, L_s=1.6 µH, L_1=L_2=2 µH, C_2=C_3=4.4 µF, C_4=5 µF. The simulation results at P_{out}=90 W, f_s=500 kHz are shown in Fig. 8.

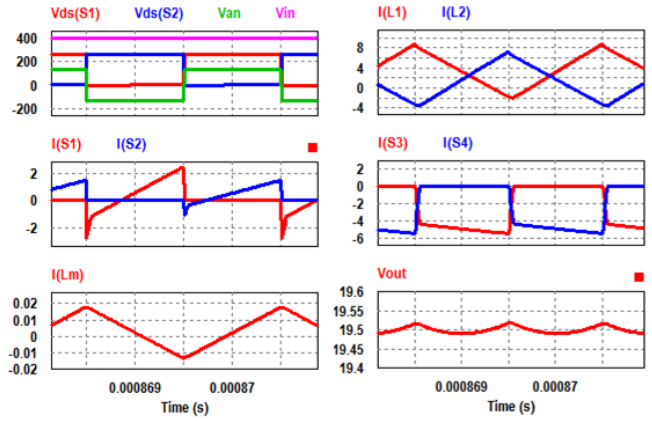


Fig. 8. Simulation results of the QSC converter with a SRCD circuit.

B. *Simulation Results of the QSC Resonant Converter with a SRCT Circuit*

A simulation model of the QSC resonant converter with a SRCT circuit is built in PSIM. The circuit parameters are as follows: V_{in}=85 V, V_{out}=19 V, N=3:2:2, L_m=16 µH, L_s=25 nH, C_2=C_3=2 µF, C_4=2 µF. The simulation results at P_{out}=90 W, f_s=1 MHz are shown in Fig. 9.

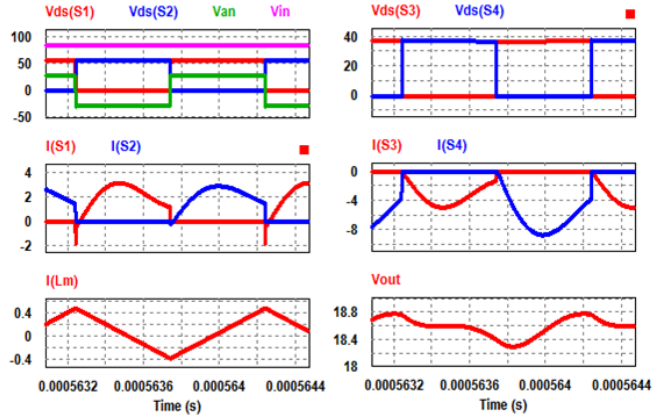


Fig. 9. Simulation results of the QSC resonant converter with a SRCT circuit.

It can be seen from Fig. 8 and Fig. 9 that: 1) the circuit features including the reduced voltage stresses on S_1, S_2, and the transformer, and the minimized dc-offset current in L_m are verified; 2) because of the low switching loss caused by the resonant switching currents, the QSC resonant converter with a SRCT circuit can lead to a higher efficiency; 3) in the QSC resonant converter with a SRCT circuit, since the input voltage supplied by the upstream Buck-PFC stage is 85 V, and the voltage stresses on S_1 and S_2 are reduced to about 57 V, the converter enables the use of 100 V EPC eGaN FETs such as the EPC2016 for all the switches, with sufficient margin reserved for voltage overshoot and ringing on the switches. This, in the meantime, can further improve the efficiency because of the low merit of figure of the device, and improve the power density because of the small size of the device and the elimination of heatsink.

V. Prototype Design

A. *Prototype Design of the QSC Converter with a SRCD Circuit*

A 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit is built, as shown in Fig. 10 (a), using 600 V Transphorm GaN HEMTs (TPH2006) for the S_1 and S_2, and 200 V EPC eGaN FETs (EPC2010) for the S_3 and S_4. Tab connections are implemented for the GaN HETMs as shown in Fig. 10 (b), in order to separate the main power loop and the gate loop, and therefore to achieve the Kelvin connection which provides the minimized common-source inductance. The circuit parameters are: N=33.5:11.5, L_m=4 mH, L_s=1.6 µH, L_1=L_2=2 µH, C_2=C_3=4.4 µF, C_4=60 µF. Litz wire is applied to cope with the skin effect. Ferrite material 3F35 from Ferroxcube is chosen for the magnetic components.

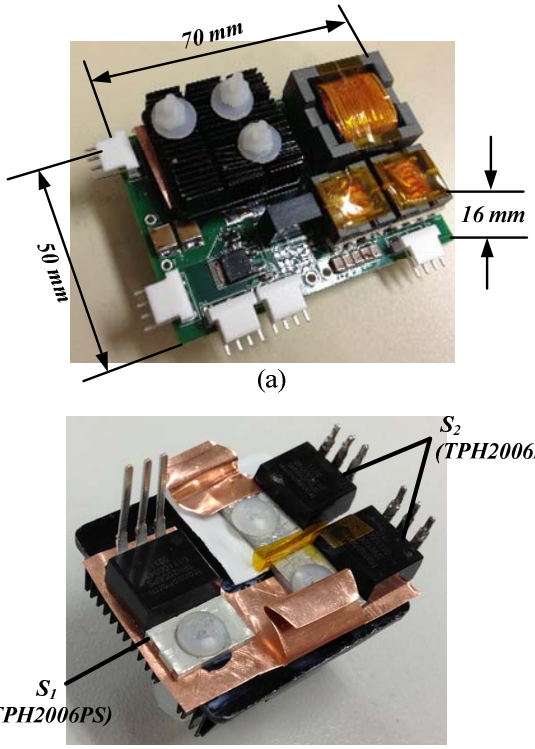


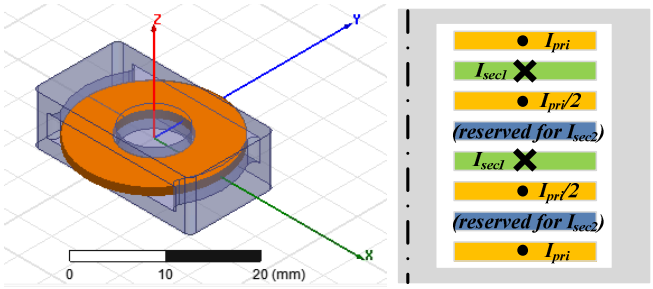
Fig. 10. (a) The 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit, and (b) Transphorm GaN HEMTs and its tab connections.

B. *Prototype Design of the QSC Resonant Converter with a SRCT Circuit*

To purse higher power density and higher efficiency, a 90 W, 85 V/19 V, 1 MHz QSC resonant converter with a SRCT circuit is built, using 100 V EPC eGaN FETs (EPC2016) for all switches. High switching frequency is preferred to shrink the passive components and increase power density, so a high circuit resonant frequency is required. To increase the resonant frequency, low transformer leakage inductance and minimized stray inductance in the main power loop layout are needed. To minimize the transformer leakage inductance and the stray inductance in the circuit layout, the Finite Element Analysis (FEA) tools Maxwell 3D and Q3D Extractor are applied to assist with the design.

1) Planar Transformer Design

A center-tapped planar transformer with an interleaving winding structure is designed. The turns ratio is N=3:2:2. The Ferrite material 3F45 from Ferroxcube is chosen for the magnetic core. As shown in Fig. 11, an ideal model without termination is firstly analyzed in Maxwell 3D. The simulation results are: L_m=19 μH, L_s=12 nH.



(a) (b)

Fig. 11. (a) Maxwell 3D simulation model of the ideal planar transformer without termination and (b) the interleaving winding structure.

Then, a detailed transformer model with vias connecting different layers, as shown in Fig. 12, is built in Maxwell 3D and Q3D Extractor for analysis with termination inductance considered. However, the model has too much detail that the simulation failed in Maxwell 3D because of running out of computing memory. The same model could successfully run in Q3D Extractor, but the results of L_m and L_s from the Q3D Extractor were not accurate. Therefore, the stray inductance of the vias connecting different layers of the winding, and the resulted extra winding strip between the vias are estimated respectively. These two parts of stray inductance are part of the total resonance inductance.

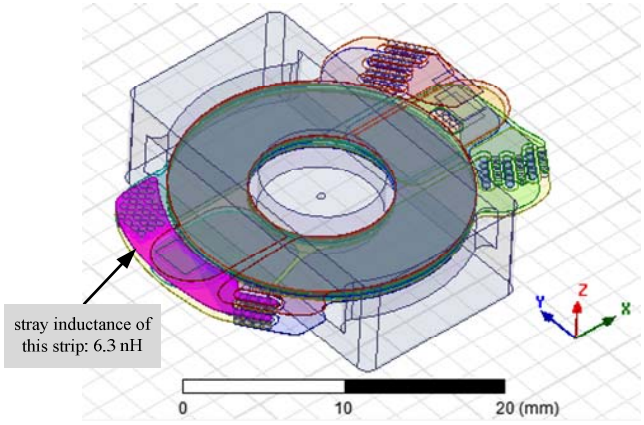


Fig. 12. Detailed simulation model in Maxwell 3D of the planar transformer with termination.

The stray inductance of the extra winding strip can be estimated by the following equation [17]

$$L_{stray} = 0.0002\,L[\ln\frac{2L}{W+H} + 0.2235\frac{W+H}{L} + 0.5]\ \ \mu H \qquad (1)$$

, where L is the length of the strip, W is the width of the strip, and H is the thickness of the strip. For example, the estimated stray inductance of the strip highlighted in purple in Fig. 12 is 6.3 nH.

In order to reduce the stray inductance caused by the vias connecting different layers of the transformer windings, an interleaving structure of the vias is applied, as shown in Fig. 13. For each transformer winding, at places where different layers of the winding connect, interleaving rows of vias carrying opposite currents are placed with enough clearance distance for breakdown prevention. The paralleled vias in a row provide reduced resistance and reduced conduction loss. The interleaved rows of vias allow for reduced eddy and proximity effects, reducing ac conduction losses.

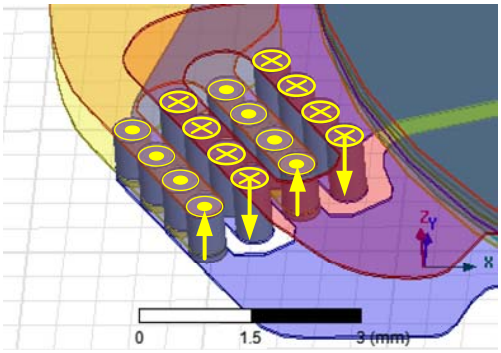


Fig. 13. Interleaving vias of the palanr transformer.

The stray inductance of the interleaving vias can be estimated by the following equation [18]

$$L_{via} = \frac{\mu_0}{2\pi}h[\frac{3}{2}\ln\frac{s}{r} + \frac{1}{2}\ln 2]\ \ \mu H \qquad (2)$$

where s is the distance between 2 adjacent rows of vias, r is the via-hole radius, and h is the via length. The estimated stray inductance of the vias shown in Fig. 11 is 0.6 nH.

2) PCB Layout

An 8-layer PCB is designed, where the main circuit traces and the planar transformer windings are integrated. The spacing between the internal layers must be selected to meet the isolation capability requirement of the ac/dc adapter. However, smaller spacing is preferred in order to reduce both the transformer leakage inductance and the stray inductance in PCB layout. According to the standard IPC-2221 [19], the electric strength of the FR4 material is 39.4 kV/mm, and according to the standard IEC60950-1 [20], the reinforced electric strength requirement for the aimed application is 2 kV. In the design, a 4 mil spacing is selected, which can withstand 4 kV for isolation.

The stray inductance in the main power loop is also part of the resonance inductance. Meanwhile, it slows down the dV/dt of the switches, causing more switching loss [13] [21]. So this part of stray inductance needs to be minimized. In the PCB layout, the idea of the optimal layout for reduced stray inductance and resistance, as proposed in [21], is followed.

Consider the layout of S_2, C_2 and C_3 for example, (shown in Fig. 14): 1) S_2, C_2 and C_3 are all placed on the top layer of the board, with minimal spacing between them; 2) The transformer primary-side winding starts from the top layer and ends at the 2nd layer; 3) The switch currents flow to the transformer on the top layer, with the overlapped return

current flowing on the 2nd layer. The current return path is located directly underneath the top layer's power loop, allowing for the smallest physical loop size combined with field self-cancellation.

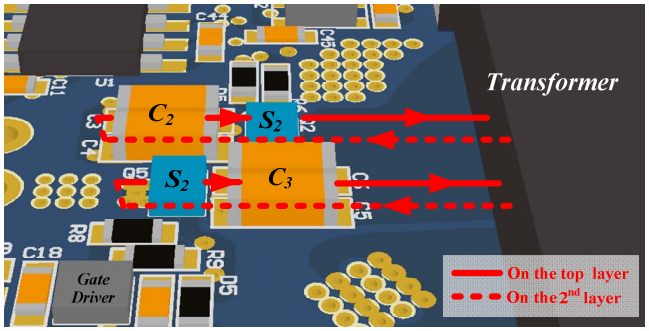


Fig. 14. Optimal PCB layout for EPC eGaN FETs for reduced high frequency parasitic inductance and resistance.

3) Output Rectifiers

S_3 and S_4 operate as synchronous rectifiers (SR) to reduce the conduction loss. However, due to the high source-drain forward voltage of eGaN FETs, the propagation delay before turning on the device would lead to high loss. Schottky diodes in parallel with the SR can minimize the conduction loss caused by the propagation delay [21] [22], therefore S_3 and S_4 are paralleled with Schottky diode PDS760.

The prototype of the QSC resonant converter is shown in Fig. 15. It contains the main circuit and gate drive circuits, but doesn't contain the controller and the isolated power supplies for the gate drive circuits, which however, could be integrated into an IC in future. The circuit parameters are: N=3:2:2, L_m=16 μH, C_2=C_3=2 μF, C_4=2 μF, f_s=1 MHz, the measured total resonance inductance, which includes the transformer leakage inductance and the main power loop stray inductance, is only 25 nH. Ferrite material 3F45 from Ferroxcube is chosen for the transformer. The power density of this prototype has reached 10.5 W/cm^3.

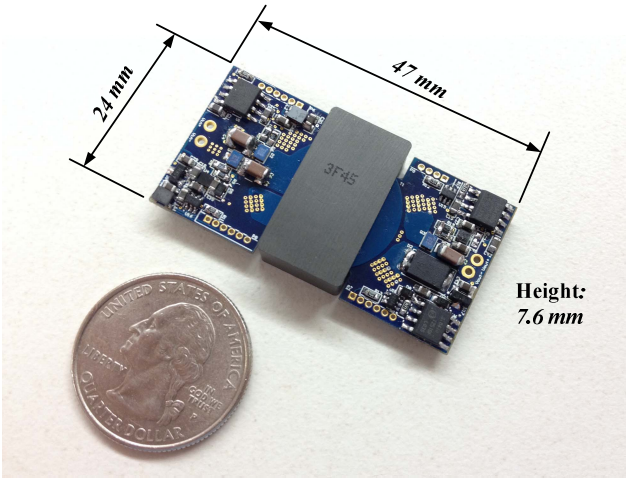


Fig. 15. The 90 W, 85 V/19 V, 1 MHz QSC resonant converter with a SRCT circuit.

VI. Experimental Verifications

A. Experimental Results of the QSC Converter with a SRCD Circuit

Fig. 16 shows the experimental waveforms of the 90 W, 400 V/19 V QSC converter with a SRCD circuit, operating at V_{in}=400 V, V_{out}=19.48 V, P_{out}=96.8 W, f_s=500 kHz. Fig. 17 shows the efficiency curve of the converter.

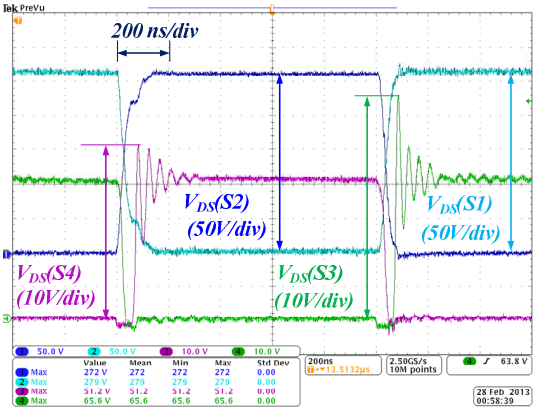


Fig. 16. Experimental waveforms of the 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit.

It can be seen from Fig. 16 that: 1) the voltage stresses on S_1 and S_2 are reduced to $2V_{in}/3$; 2) the dead time between the SR S_3 and S_4 is not minimized, which caused extra power loss; 3) before turning on S_1 or S_2, the drain-to-source voltage of that switch has resonated to zero because the transformer leakage inductance releasing its energy, so ZVS on is achieved for S_1 and S_2. It can be seen from Fig. 17 that the efficiency continues to increase with the output power and the peak efficiency hasn't been reached at the maximum power, which means the prototype is overdesigned for this power rating.

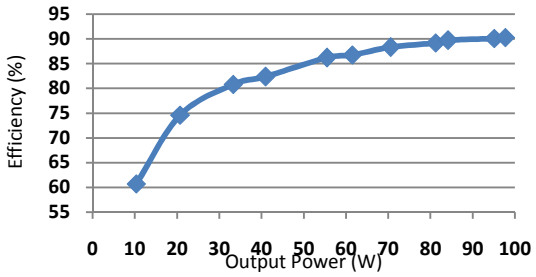


Fig. 17. Efficiency curve of the 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit.

The power loss distribution of the prototype at 90 W output power is shown in Fig. 18. It is shown in [13] that the 600 V GaN HEMT is oversized for this application because when it turns off at a low switch current which is about 1~2 A, the switching speed is significantly slower than the rated value, leading to high switching loss. It can be seen from Fig. 18 that the turn-off loss of the GaN HEMT takes a large portion of the total loss in this application, so the prototype is overdesigned, and the performance and efficiency are not optimized. The efficiency can be improved by selecting more appropriate switches and implementing a better design.

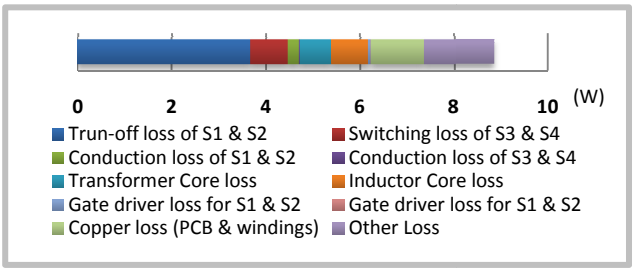


Fig. 18. Power loss distribution of the 90 W, 400 V/19 V, 500 kHz QSC converter with a SRCD circuit operating at 90 W output power.

B. *Experimental Results of the QSC Resonant Converter with a SRCT Circuit*

The testing of the 90 W, 85 V/19 V, 1 MHz QSC resonant converter with a SRCT circuit is in progress. The estimated efficiency of the converter at full load is 96%. The preliminary experimental results are presented herein. Fig. 19 shows the experimental waveforms of the converter operating at V_{in}=85 V, V_{out}=19 V, P_{out}=90 W, f_s=900 kHz. The efficiency curve operating at f_s=900 kHz is shown in Fig. 20.

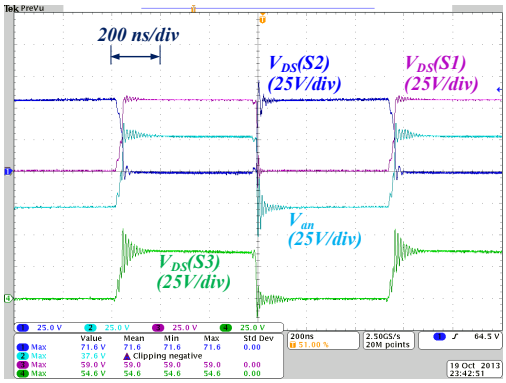


Fig. 19. Experimental waveforms of the QSC resonant converter with a SRCT circuit operating at V_{in}=85 V, V_{out}=19 V, P_{out}=90 W, f_s=900 kHz.

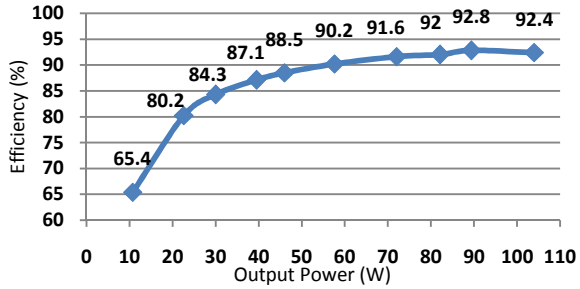


Fig. 20. Efficiency curve of the 90 W, 85 V/19 V QSC resonant converter with a SRCT circuit operating at f_s=900 kHz.

It can be seen from Fig. 19 that: 1) the voltage stresses on S_1 and S_2 are reduced to $2V_{in}/3$; 2) the voltage stresses on the transformer is reduced to $V_{in}/3$; 3) the experimental results matched the simulation results well. The resonant switching currents couldn't be monitored on the prototype because of the structure. However, they can be predicted from the simulation.

In this preliminary testing, for the sake of operation safety: 1) the applied turn-on external gate resistance is 10 Ohm, and the applied turn-off external gate resistance is 2 Ohm; 2) the gate drive voltage is 4.5 V and a 20 ns dead time is applied for the eGaN FETs. The conservative gate resistance, low gate drive voltage, and large dead time all contribute to higher power loss of the eGaN FETs [11]. With these parameters optimized, the efficiency can be further improved.

C. *Experimental Results of the Buck-PFC AC/DC stage*

A Si device based Buck-PFC evaluation module from TI is tested. It is based on the controller UCC29910A, which has a fixed switching frequency of 100 kHz. In order to evaluate the improvement of applying wide bandgap devices, the following modifications are made: 1) the Si CoolMOS is replaced with a GaN HEMT (TPH3006PD); 2) the Si Hyperfast diode is replaced with a SiC Schottky diode (C4D20120A), which has no reverse-recovery loss; 3) the gate drive voltage is raised to 15 V, to reduce the on-resistance of the GaN HEMT; 4) the RC snubber across the switch is removed. Fig. 21 shows the efficiency curves of both the original and modified module at V_{in}=115 V_{ac}. Fig. 22 shows the temperature profiles of the 2 versions after running at full load for 10 minutes.

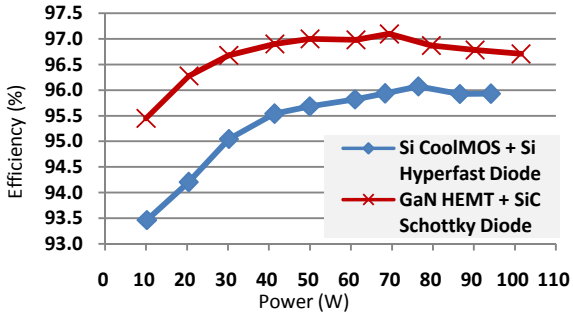


Fig. 21. Efficiency curves of the Si based and GaN/SiC based Buck-PFC evaluation modules at V_{in}=115 V_{ac} over the full load range.

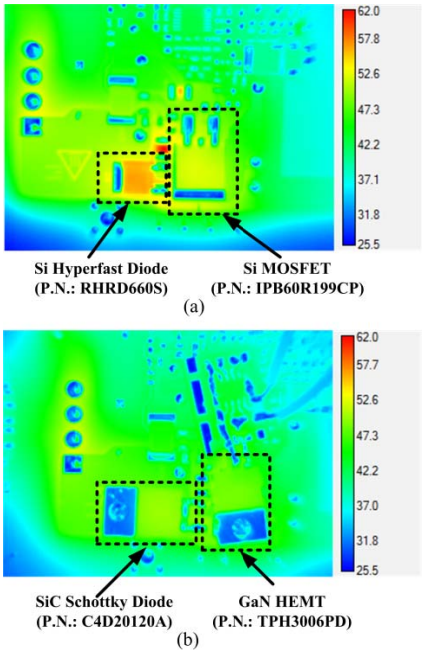


Fig. 22. Temperature profiles of the 2 versions of the Buck-PFC evaluation module after running at full load for 10 minutes.

Fig. 21 shows that, compared with the Si based version, the GaN based version improved the efficiency by 1~2% over the full load range. Fig. 22 shows that the temperature rise is lower in the GaN based version. The fixed 100 kHz switching frequency is not high enough to show the benefits of the low switching loss provided by the GaN HEMT and SiC Schottky diode. If a higher efficiency is applied, the power density can be significantly improved, while good efficiency performance can be maintained.

VII. CONCLUSIONS

This paper presents a GaN Transistor based 90W ac/dc adapter with a Buck-PFC stage and an isolated QSC dc/dc stage. Compared to Flyback and LLC resonant converters, the QSC converters feature: 1) reduced voltage stresses on the primary-side switches to 2/3 of the input voltage, which is friendlier to low voltage switches; 2) reduced voltage stress on the transformer to 1/3 of the input voltage and a lower transformer turns ratio, which enables lower winding loss and smaller leakage inductance; 3) a wide range for soft-switching operation and high efficiency; 4) a simple control strategy. Compared to the Boost-PFC stage, the Buck-PFC features better efficiency at low line voltage, and it provides a low output dc-link voltage, which enables lower CM noise, and more efficient design of the downstream stage, using lower voltage switches with better figures of merit.

GaN devices can lead to high efficiency and high power density for ac/dc adapters. A 90 W, 85 V/19 V, 1 MHz QSC resonant converter is built, using 100 V EPC eGaN FETs for all switches. This prototype achieves: 1) a high power density of 10.5 W/cm^3; 2) wide-range soft switching and a peak efficiency of 92.8% at 900 kHz in preliminary test results. A Buck-PFC evaluation module from TI is tested with a GaN HEMT and a SiC Schottky diode. The peak efficiency reached 97.1% at 100 kHz. The experiment results show an efficiency improvement by 1~2% over the full load range and a lower temperature rise, compared with the original Si based version. With higher switching frequency applied, the power density of the Buck-PFC can be significantly improved, while good efficiency performance can be maintained.

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