On-line Condition Monitoring for MOSFET and IGBT Switches in Digitally Controlled Drives

Jason M. Anderson and Robert W. Cox
Department of Electrical and Computer Engineering
UNC Charlotte
Charlotte, NC 28223
Email: jmander1@uncc.edu and Robert.Cox@uncc.edu

***Abstract*— The early detection of incipient faults is desirable in mission-critical applications such as shipboard propulsion drives. This paper presents an on-line condition-monitoring approach for detecting incipient faults in IGBTs and MOSFETs. The proposed algorithm extracts important device features (i.e $V_{CE,ON}$ and $R_{DS,ON}$) and compares them to healthy values recorded over a range of operating conditions. The algorithm is based on principal-components analysis (PCA). An experimental implementation in an IGBT-based drive is described. An on-line feature extraction scheme for MOSFETs is also proposed and demonstrated. This scheme exploits the nature of carrier-based PWM in order simplify the measurement process.**

I. Introduction

Power electronic drives are becoming increasingly common in mission-critical applications. High power, medium voltage examples include propulsion motors aboard all-electric ships [1], large industrial motors such as those driving recirculation pumps in nuclear power plants [2], and large multi-megawatt, grid-tied inverters for wind turbines and photovoltaics [3]. Lower voltage drives are also becoming common in vehicles and aircraft [4]. This increasing dependence on power electronics in mission-critical applications has created a need for real-time techniques that can detect *incipient* faults.

The two components most prone to failure in switch-mode drives are electrolytic filtering capacitors and power semiconductors [5]. Approaches for on-line monitoring of capacitor health have been described in the literature, and are relatively easy to implement in digitally controlled drives [5], [6]. In the case of MOSFET and IGBT switches, on the other hand, the focus has been to develop fault-detection schemes that allow one to detect complete device failures such as shorted or open transistors [7], [8], [9], [10], [11]. Once such faults occur, unplanned and inconvenient maintenance must be performed. In some cases, control can be modified to allow operation in a degraded mode until service can be performed [8], [9], [12].

Although post-fault detection will always be a necessary safety feature in any mission-critical drive, there is good reason to consider incipient fault detection and on-line condition monitoring. The most obvious motivation is the possibility that maintenance can be conveniently scheduled rather than forced. There are, however, other concerns. Consider, for instance, an IGBT that slowly wears over its lifetime because of thermal cycling. Ultimately, such a device will short circuit, which is desirable in a drive with $N+1$ components. Eventually, however, the bond wires burn away, leading to an indeterminate failure state that may cause an arc flash and subsequent collateral damage to the rest of the circuit or to nearby humans [13].

The literature includes a number of articles describing the physics of failure in MOSFETs and IGBTs [14], [15], [16], [17]. Authors have described and verified the relationships between device health and device parameters (i.e. $V_{CE,ON}$, $R_{DS,ON}$, V_T, etc.). Very few works, however, describe the use of such features for monitoring switch health in real-time in an operational circuit. Methods based on efficiency monitoring have been proposed [18], but these do not necessarily determine the source of degradation in multi-transistor drives. A major limiting factor in the development of condition-monitoring for switches has been the difficulty in obtaining the required signals, which are often very small and thus highly susceptible to corruption from switching noise [11]. Furthermore, acquisition of the appropriate information tends to require additional sensors and thus higher costs.

Many of the barriers to real-time health monitoring can be overcome through the use of advanced gate drives (AGDs). These next-generation components, which were originally proposed in [8], locally measure key switch variables such as collector current and collector-to-emitter voltage. In future applications, it is imagined that these signals will be communicated to a digital controller via fiber-optic cables. The authors of [8] use this concept to detect and recover from complete failures after they have occurred. With appropriate signal processing, however, one could use these signals to detect switch degradation prior to complete failure.

This paper presents an approach for monitoring the health of power switches in real-time using the advanced gate drive concept. Although AGDs are not necessary for any of the approaches proposed herein, they do provide a practical platform for implementation and are thus included. Section II provides background on key failure mechanisms in both MOSFETs and IGBTs. Section III then presents a smart drive architecture that enables real-time health monitoring. Section III also includes a health-monitoring algorithm based on concepts from the field of facial recognition. Section IV demonstrates the method in an IGBT-based drive, and Section V considers application with MOSFETs. The paper concludes in Section VI with a discussion of future work.

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II. A Review of Failure Mechanisms in Power Transistors

There are two different categories of failure mechanisms in power transistors. The first group includes intrinsic mechanisms related to the physics of the actual semiconductors. Some of the most prevalent examples are dielectric breakdown and electromigration [19], [20], [21]. The other group includes factors related to transistor packaging, such as contact migration, bond-wire lift, and die-solder degradation [22], [14], [23], [24].

A. Example Intrinsic Failure Mechanisms

Dielectric breakdown occurs when a strong electric field creates a current channel in an insulating medium [25]. During conduction, breakdown can occur between the gate and the drain/collector terminal or between the gate and the source/emitter terminal. Two different forms of breakdown are noted in the literature [19]. Catastrophic breakdown of the gate oxide typically results from severe thermal or electrical over-stress (i.e. electrostatic discharge, junction overvoltage, etc.). Time-dependent dielectric breakdown (TDDB), which occurs more gradually over time, refers to the natural breakdown of the gate oxide. TDDB is caused by chronic defect accumulation in the SiO_2 insulator during standard operation [26]. At least three defect-generation mechanisms have been identified [19]. These include impact ionization, hot-carrier injection, and so-called trap creation attributed to the redistribution of hydrogen within the device. Before causing a complete failure, these naturally-occurring phenomena affect various device parameters [19]. For instance, they can change the gate leakage current. Similarly, any charges that become trapped in the gate oxide affect important device parameters, such as the threshold voltage V_T and the transconductance g_m [19]. Note that breakdown can also occur between the drain and the source or between the collector and emitter when the device is in a blocking state.

Electromigration is another intrinsic failure phenomenon [20]. This mechanism results when high current densities within the silicon cause adjacent metal connections to migrate. If any voids form in the interconnects as a result of this process, then the connection may open-circuit or the overall device resistance may increase [20], [27].

B. Example Extrinsic Failure Mechanisms

Various extrinsic failure phenomena have also been observed. Bond-wire lift is one of the most commonly occurring examples [14]. This phenomenon is a failure in the bond between the package wire and the silicon die. Thermal expansion mismatch between the bond solder and the attachment point is the primary cause. Bond-wire lift leads to higher junction temperatures (T_j), and thus it impacts parameters such as $V_{CE,ON}$ and on-state resistance [28]. Changes in these parameters can increase power dissipation, thus cause further increases in T_j. The resulting positive feedback mechanism ultimately leads to a complete device failure [14].

Die-solder degradation is another extrinsic issue [23]. Solder attaching the silicon die to the package heat sink can develop cracks and voids due to dissimilar thermal expansion in the two materials [24]. The junction-to-case thermal impedance, θ_{jc}, thus increases, which leads to a higher T_j. A positive feedback mechanism is thus created once again. As in the case of bond-wire failures, this mechanism affects parameters such as the on-state resistance and $V_{CE,ON}$ [14].

A third extrinsic failure mechanism is contact migration. This phenomenon, which is related to electromigration, occurs when voids between external metal contacts and silicon cause metal to diffuse into the semiconductor. Ultimately, this diffused metal can short-circuit internal *pn* junctions. Before causing a complete failure, this mechanism impacts parameters such as $V_{CE,ON}$ and on-state resistance [14].

C. Challenges to Real-Time Health Monitoring

The above noted mechanisms and other similar effects ultimately cause complete device failures, including permanent short or open circuits between the drain and source and the collector and emitter. Techniques for detecting short or open-circuited devices have been developed and will always be needed as a safety precaution. The number of complete failures and subsequent unplanned maintenance calls can be significantly reduced, however, by continuously monitoring some of the indicators noted above (i.e. $V_{CE,ON}$, V_T, etc.). There are two main challenges to this approach. First, one must be able to determine the appropriate quantities during normal operation of the drive. Second, one must be able to distinguish between true fault conditions and changes associated with variations in temperature and operating conditions (i.e. loading, etc.). Methods for addressing these issues are presented below.

III. Smart Drive Architecture with Real-Time Switch Condition Monitoring

Real-time switch condition monitoring introduces new requirements into the design of the overall drive. First, one must obtain high-rate samples of switch terminal variables such as v_{CE} and i_C. Additionally, these signals must be processed and analyzed over time. This section considers a drive architecture that addresses these issues, and it presents an algorithm that can be included to track switch health. Note, however, that the proposed algorithm can be used in any drive capable of measuring the required quantities.

A. Drive Architecture

Figure 1 shows a three-phase full-bridge converter with the ability to sample all of the required terminal variables. The key feature is the advanced gate drive concept from [8]. It is anticipated that fully developed versions of these devices could sample terminal quantities locally at a very high rate, and then transmit appropriately down-sampled versions over a fiber-optic link to a digital signal processor (DSP) performing overall control.

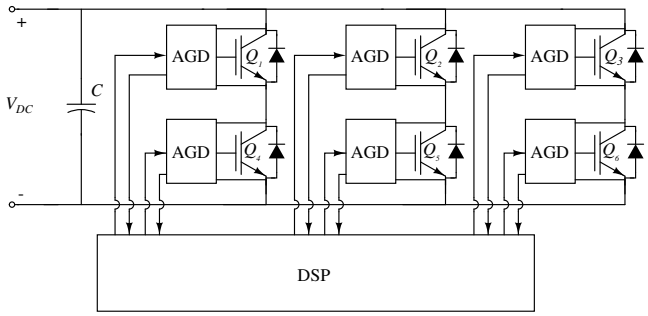

Fig. 1. A potential smart drive architecture including the advanced gate drives (AGDs) proposed in [8]. The AGDs provide the controller with measurements of terminal variables including i_C and v_{CE}. It is assumed that these connections would be fiber optic.

From a health monitoring perspective, it is critical to sample signals such as v_{CE} and i_C fast enough to be able to extract features such as $V_{CE,ON}$ and $R_{DS,ON}$. Sampling rate is one issue that must be addressed regardless of the actual circuit architecture. In general, sampling must be performed at a rate above the switching frequency. This may limit application in lower power drives with switching frequencies in excess of 10kHz. In high power, medium voltage (MV) drives, which are more likely to require condition monitoring, power-dissipation limits tend to cap switching frequencies at values on the order of 1kHz [29]. At these switching frequencies, it likely that device variables could be sampled fast enough to extract the relevant features. Note that the same AGD approach could be applied in typical MV architectures, such as neutral-point-clamped (NPC) inverters and cascaded H-bridges.

The AGD concept is included here simply because it provides a feasible approach for monitoring the key signals of interest. Example implementations presented in Sections IV and V are thus based on signals obtainable from gate drives. It should be noted, however, that such signals could be obtained without the use of AGDs and thus the techniques presented here are not contingent upon the use of this approach.

B. Generalized Health-Monitoring Algorithm for Switches

Figure 2 shows a generalized health-monitoring algorithm for power switches. This algorithm is designed to distinguish between the effects of true faults and other naturally occurring phenomena such as changes in temperature and operating conditions. Inputs to the algorithm include various raw device signals such as v_{CE} and i_C. The first step in the process is to extract relevant health indicators such as $V_{CE,ON}$. Various algorithms can be used. In general, multiple samples of the input data are needed to calculate any feature. As a result, indicators are extracted at a rate well below the sampling frequency. Sections IV and V present algorithms for estimating key IGBT and MOSFET parameters, respectively. As shown in Fig. 2, various feature estimates are ultimately combined with measurements of the case temperature and passed to the remainder of the algorithm.

Feature vectors computed at the time t_k are grouped into a column vector $\boldsymbol{x}_k$. In our current implementation in the IGBT-based drive, this vector includes $V_{CE,ON}$, R_{ON}, and T_C. Assuming that other parameters will be added, we make the general assumption that $\boldsymbol{x}_k$ has a length d. The basic approach of the principal-component-based algorithm is to compare each measurement $\boldsymbol{x}_k$ to an expectation. This expected vector is computed by projecting $\boldsymbol{x}_k$ onto a vector space created using "healthy" features. These healthy values are learned during a training phase in which the drive is new and presumably in good condition. During training, the healthy vectors are decomposed into a small set of characteristic vectors that best describes the distribution of the healthy parameters. During operation, each measured vector is projected onto this space. In the language of information theory, we are extracting the relevant information from the feature vector, encoding it efficiently, and then comparing the encoded result to a database of healthy features encoded in a similar manner. Any differences indicate that the device may be degrading. This approach is partially patterned after the facial recognition scheme presented in [30].

The training space includes features recorded over a range of expected operating conditions. In all, there are M such vectors and they are denoted as $\boldsymbol{\Gamma}_1, \boldsymbol{\Gamma}_2, \boldsymbol{\Gamma}_3, ..., \boldsymbol{\Gamma}_M$. These training vectors are subject to a principal-component analysis (PCA) in which one seeks a set of orthonormal vectors $\boldsymbol{e}_i$ that best describe the distribution of the data. The j-th training vector can thus be expressed as

$$\boldsymbol{\Gamma}_j = \boldsymbol{m} + \sum_{i=1}^{d'} a_{j,i}\, \boldsymbol{e}_i, \tag{1}$$

where $\boldsymbol{m}$ is the sample mean, i.e.

$$\boldsymbol{m} = \frac{1}{M} \sum_{j=1}^{M} \boldsymbol{\Gamma}_j. \tag{2}$$

Note that the distribution of the data is best described using $d' \leq d$ orthonormal vectors [31], [30]. During the training phase, one calculates these by minimizing the squared-error criterion function

$$J = \sum_{j=1}^{M} \left\| \left(\boldsymbol{m} + \sum_{i=1}^{d'} a_{j,i}\, \boldsymbol{e_i} \right) - \boldsymbol{\Gamma}_j \right\|^2. \tag{3}$$

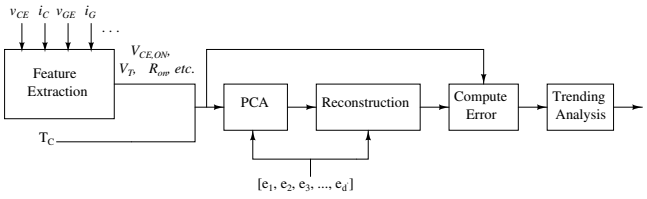

Fig. 2. Generalized condition-monitoring algorithm for an operational IGBT based on principal-components analysis (PCA). The $\boldsymbol{e}_i$ are based on healthy conditions. New input signals and parameters can be added as needed. A similar implementation would be used for a MOSFET.

References [31] and [30] show that the $\boldsymbol{e}_i$ correspond to the eigenvectors of the sample covariance matrix which is

$$\boldsymbol{S} = \sum_{j=1}^{M} (\boldsymbol{\Gamma}_j - \boldsymbol{m}) (\boldsymbol{\Gamma}_j - \boldsymbol{m})^T . \quad (4)$$

The actual $\boldsymbol{e}_i$ are the eigenvectors corresponding to the d' largest eigenvalues of $\boldsymbol{S}$ [31], [30]. Ultimately, this process yields a compact basis that efficiently encodes the relevant features of a healthy switch over a range of expected operating conditions.

During normal operation of the drive, the prognostic algorithm in Fig. 2 projects the features measured at time t_k onto the space spanned by the $\boldsymbol{e}_i$. This projection is performed by the block labeled PCA, which computes the set of coefficients

$$a_{k,i} = \boldsymbol{e}_i^T (\boldsymbol{x}_k - \boldsymbol{m}) . \quad (5)$$

The next block uses these coefficients to reconstruct an approximation of $\boldsymbol{x}_k$. The resulting estimate is thus denoted as

$$\hat{\boldsymbol{x}}_k = \boldsymbol{m} + \sum_{i=1}^{d'} a_{k,i}\, \boldsymbol{e}_i. \quad (6)$$

Following reconstruction, the algorithm calculates the two-norm of the residual vector $\boldsymbol{r} = \hat{\boldsymbol{x}}_k - \boldsymbol{x}_k$. This quantity represents the error between the measured features and their projection onto the healthy features. If the error is small, the switch is healthy; if the error grows, a problem may be developing. The final block monitors for such variations.

IV. Incipient Fault Detection in IGBTs

The condition-monitoring algorithm described in Section III has been tested using an IGBT-based drive of the form shown in Fig. 1. This custom-built system drives a 1hp induction motor and is controlled using a dsPIC30F6010A. The switching frequency is set to approximately 1kHz in order to mimic operation in a medium voltage drive. Although the full AGD concept is not employed, measurements are based on signals obtained locally in the gate drive.

A. Implementation Details

The two health indicators used in this example are $V_{CE,ON}$ and R_{ON}. Additional information could be obtained and included, but the use of these two parameters is sufficient for illustrating the basic concept of the algorithm. The use of these two features is reasonable given that they are indicators for several important incipient faults. Other features will be added in the future.

To determine $V_{CE,ON}$ and R_{ON} in real-time, one must measure both v_{CE} and i_C. The current is easily measured using a Hall-effect transducer. The collector-to-emitter voltage, on the other hand, is difficult to measure directly because the required amplifier would be exposed to large common-mode swings and the subsequent analog-to-digital converter would have difficulty measuring on-state voltage with appropriate resolution. To overcome this issue, v_{CE} is measured in the on-state using the desaturation detection circuit included in the gate drive. Figure 3 shows this circuit. The optical transmission circuit from [8] maintains appropriate isolation when measuring the voltage v_X, which is referred to the high voltage side of the drive. When the IGBT is conducting, this signal has the form

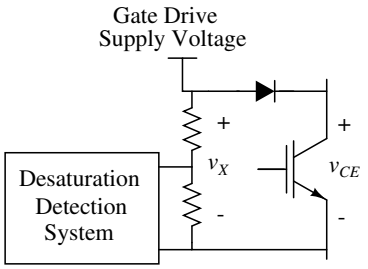

Fig. 3. A partial schematic of a desaturation circuit in a gate drive for an IGBT. The voltage v_X is sampled during the on state.

$$v_X = V_D + v_{CE}(i_c) , \quad (7)$$

where V_D is the forward voltage drop across the diode in the desaturation circuit.

Although the literature suggests that $V_{CE,ON}$ can be directly applied in fault detection, this is only true under carefully controlled conditions that do not necessarily apply in the field. In general, the circuit model for a conducting IGBT is a diode in series with a power MOSFET, meaning that

$$V_{CE,ON} = V_J + i_C R_{ON}, \quad (8)$$

where R_{ON} is the resistance of the MOSFET channel and V_J represents the combination of the voltage drops across the *pn* junction and the drift region [32]. Given that most incipient faults have only a small impact on $V_{CE,ON}$, this result suggests that it may difficult to distinguish between changes in i_C and true fault conditions. This problem is further compounded by the fact that both V_J and R_{ON} are affected by temperature [32]. Measurement is particularly problematic in variable-speed AC drives in which the current is subject to continuous variation.

Figure 4 illustrates the effect of Eq. 8 in an operational drive. Note that $V_{CE,ON}$ essentially follows the current when the IGBT is conducting. To isolate the effect of the current, we separately estimate the two parameters in Eq. 8 using a least-squares approach. During each conduction interval, successive samples of the current and voltage are averaged. Figure 5 shows these averages and the best-fit line corresponding to the data in Fig. 4. The estimated y-intercept (V_J) and the slope (R_{ON}) are ultimately extracted as features. These quantities are combined with low frequency samples of T_C to assemble each feature vector $\boldsymbol{x}_k$.

B. Experimental Demonstration

To illustrate the effectiveness of the proposed algorithm, one of the switches in the drive was removed and subjected to

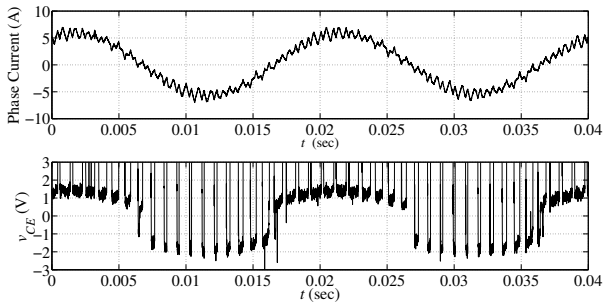

Fig. 4. Measured phase current and v_{CE} for one of the switches in the experimental drive. When v_{CE} is negative, the anti-parallel diode is conducting.

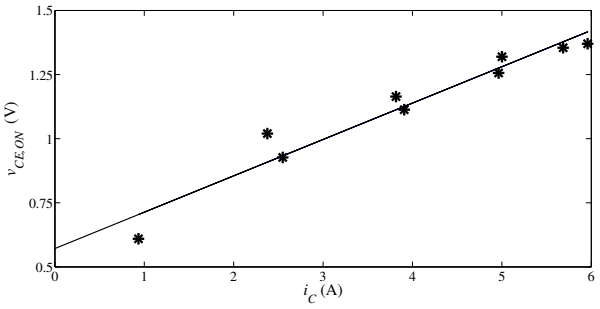

Fig. 5. Average $V_{CE,ON}$ versus average i_C during the conduction intervals between approximately 17ms and 26ms in Fig. 4. A best-fit line is also included.

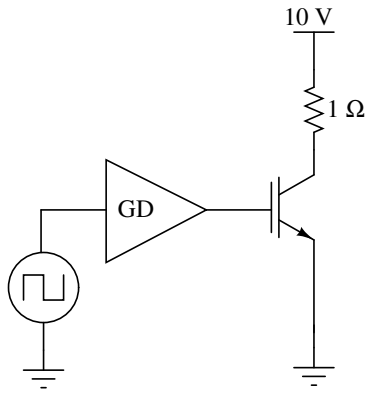

Fig. 6. Circuit used to age the IGBT. A 1kHz waveform with $D = 0.4$ drives the gate.

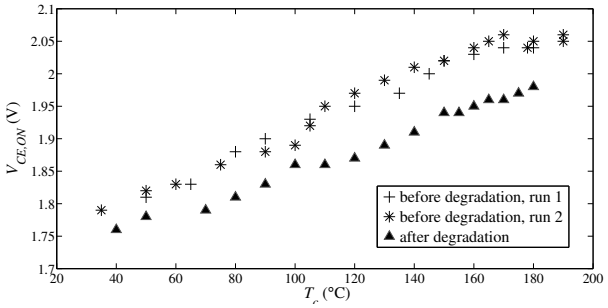

Fig. 7. $V_{CE,ON}$ versus temperature for the IGBT, both before and after aging.

an accelerated aging test. To perform ageing, the IGBT was placed in the circuit shown in Fig. 6. The gate signal in this circuit is a 1kHz square waveform with a 40% duty ratio. The average current recorded during testing was approximately 3A, which is rather high given that the part is only rated for 10A and no heat sink was used. Case temperature was measured during the test using an infrared camera. The test was stopped once T_c reached approximately 190°C. This test was repeated for a number of hours. A similar approach was used in [33] to develop die-attach faults.

Figure 7 shows results recorded during the ageing process. Note the positive temperature coefficient in both the new and degraded case. This result is expected for IGBTs [33]. Additionally, note that the component has a lower $V_{CE,ON}$ at all temperatures once it has degraded. This result was also obtained in [33]. It is believed that the drop occurred because the degraded die attach increased θ_{jc} and thus created a higher internal temperature at any given T_c. Since the *pn* junction has a negative temperature coefficient of resistance [34], an increase in the temperature of this junction would lower $V_{CE,ON}$.

Figure 8 shows results obtained using the proposed condition-monitoring algorithm. Note that the part was tested in both the healthy and degraded state over a range of temperatures. The figure shows the reconstruction errors for both conditions. Note that these errors are very low when the part is healthy and much higher (2to4X) when the part is degraded but still functional. Note that one should compare results obtained at similar temperatures.

V. Incipient Fault Detection in MOSFETs

A. Feature Extraction

The on-line monitoring approach shown in Fig. 2 can also be applied to MOSFETs. Figure 9 shows the schematic of the MOSFET-based drive constructed for testing purposes. Note that this system uses the same control board and motor as the IGBT-based drive.

Although various health indicators also exist for MOSFETs, we focus our attention here on the use of $R_{DS,ON}$. On-state resistance can be measured on-line in motor drives using naturally occurring ripple waveforms generated by the action of carrier-based PWM. The exact details depend upon the manner in which the drive is controlled.

Consider the motor drive shown in Fig. 9, and assume that it is driven using a digitally-implemented carrier-based PWM scheme. Specific instances of carrier-based PWM include space-vector modulation and regular sampling [35]. Typically, these schemes are implemented using capture-compare modules in microcontrollers. The most common technique is to use timers to align the switching instants with a fictitious carrier waveform as shown in Fig. 10. As a result, each phase

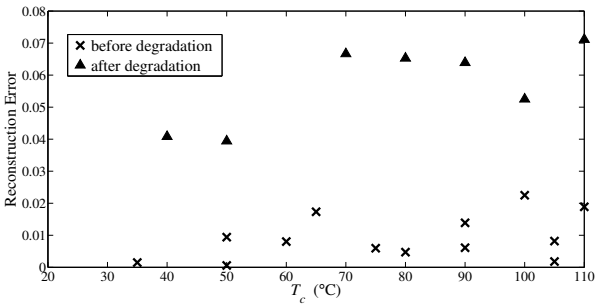

Fig. 8. The reconstruction error recorded by the health-monitoring algorithm. Data is included from tests performed before and after accelerated aging. Note that the error is significantly lower at any given temperature when the part is healthy.

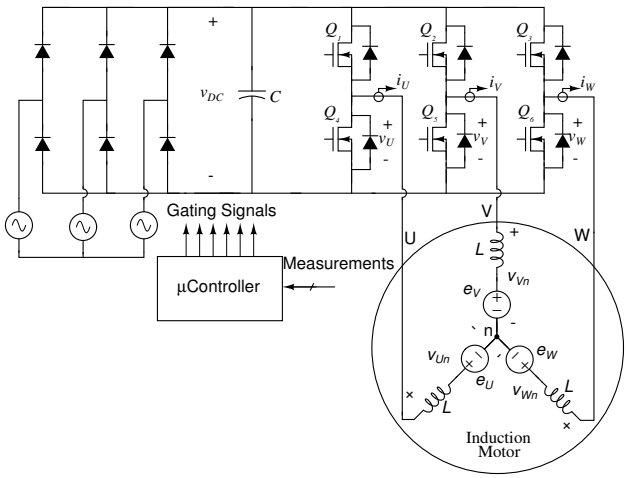

Fig. 9. Partial schematic of the experimental FET-based drive. The drain-to-source voltage, v_{DS}, is measured for each transistor and the motor phase currents i_U, i_V, and i_W are also measured.

voltage pulses once per switching period. The exact timing of switching depends upon the specifics of the microcontroller, but switching is often selected to be symmetrically aligned with the peaks of the carrier as shown in Fig. 10 [35]. The measurement approach described below does not depend on this symmetry, however. Symmetric regular sampling is used only for illustrative purposes, and other techniques could be considered.

The proposed measurement approach is based on the current ripple generated by the phase voltages shown in Fig. 10. These voltage waveforms can be written as the superposition of a fundamental frequency component and a ripple term. Using the simplified induction machine equivalent circuit in Fig. 9, note that all of the voltage ripple for a given phase appears across the inductance L. The resulting current is thus of the form [32]

$$i_{ripple} = \frac{1}{L}\int_0^t v_{ripple}\left(\tau\right) d\tau. \tag{9}$$

The term v_{ripple} can be written for any one of the three phases.

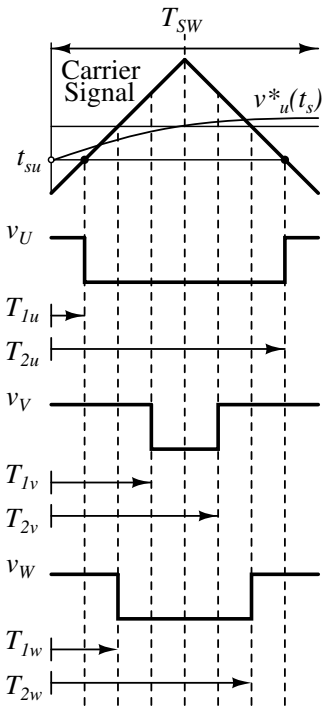

Fig. 10. Notional example of the voltages v_U, v_V, and v_W during a single switching period. Also shown is the fictitious triangular carrier signal and the reference waveform for phase U. The voltages are defined in Fig. 9. The switching time instants, T_1 and T_2, are also shown for each of the phases.

For phase U, for instance, it is

$$v_{U,ripple} = v_{Un} - v_{Un,1} \tag{10}$$

where v_{Un} is the voltage across phase U with respect to the motor neutral and $v_{Un,1}$ is the corresponding fundamental component of v_{Un}. In terms of the phase voltages shown in Fig. 10 [32],

$$v_{Un} = \frac{2}{3}v_U - \frac{1}{3}\left(v_V + v_W\right). \tag{11}$$

A careful analysis of Eqs. 9, 10, and 11 shows that the pulses in v_V and v_W affect the ripple current flowing in phase U. If one measures the voltage across Q_4 during an appropriate interval aligned with one of the pulses on the other two phase legs, then one can easily estimate the on-state resistance of Q_4 using the equation

$$R_{DS,4,ON} = \frac{\Delta v_U}{\Delta i_U}, \tag{12}$$

where Δi_U is the ripple current during the measurement interval and Δv_U is the corresponding voltage ripple. Figure 11 presents an experimental example showing how the ripple current changes as the MOSFETs change state. $R_{DS,4,ON}$ would be measured when v_V is low. The on-state resistance of the other FETs would be measured during similar intervals.

Timing is critical to the successful implementation of the measurement process described above. Figure 10, for instance,

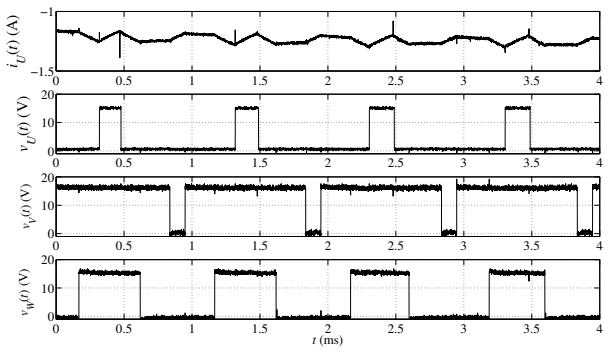

Fig. 11. The nature of i_U, v_U, v_V, and v_W (from top to bottom) in the example drive.

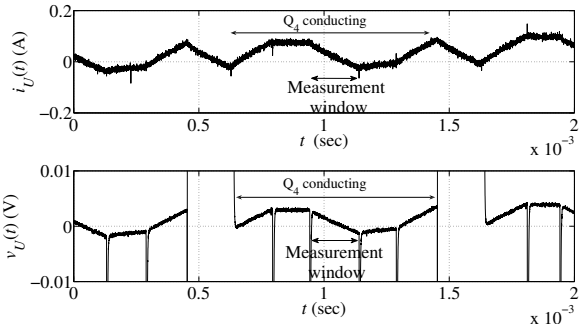

Fig. 12. Measured $i_U(t)$ and $v_U(t)$. The measurement window is indicated.

shows times during which Q_4, Q_5, and Q_6 are each conducting. Note that Q_4 is on for the longest time, and that its ripple current should exhibit 5 distinct states based on the action of the other phase legs. By comparison, the ripple current flowing through Q_5 only exhibits one distinct state. In this case, one can trigger high-speed sampling of the voltage and current for Q_4 using the same interrupts that control the switching of Q_5. Thus, one can exploit the nature of the PWM waveforms to obtain the best possible measurements of Δi and Δv. Measurements should be performed over a sufficiently long interval during which the current is approximately linear. The timing shown in Fig. 10, for instance, is ideal for the measurement of $R_{DS,4,ON}$ because the pulses on the two other phases are of a sufficient length and do not overlap. One can predetermine the appropriate measurement times by considering the nature of the symmetric, center-aligned PWM signals shown in Fig. 10. For any one phase, the switching time instants T_1 and T_2 can be computed in real time using the geometrical relationships [35]

$$T_1 = \frac{1}{4}T_{SW} \cdot (1 + v^*(t_s)) \tag{13}$$

$$T_2 = \frac{1}{2}T_{SW} + \frac{1}{4}T_{SW} \cdot (1 - v^*(t_s)) \tag{14}$$

where $v^*(t_s)$ is the most recent sample of the reference waveform for the given phase. When using regular sampling, these references are of the form

$$v_u^*(t_s) = M \sin(\omega_m t_s) \tag{15}$$

$$v_v^*(t_s) = M \sin\left(\omega_m t_s - \frac{2\pi}{3}\right) \tag{16}$$

$$v_w^*(t_s) = M \sin\left(\omega_m t_s + \frac{2\pi}{3}\right) \tag{17}$$

where M is the modulation depth and ω_m is the angular frequency of the modulating signal. The pulse widths for each phase are thus computed by taking the difference

$$\Delta T = T_2 - T_1 = \frac{1}{2}T_{SW} - \frac{1}{2}T_{SW} \cdot (v^*(t_s)). \tag{18}$$

These times are independent of ω_m and can thus be rewritten by substituting $\omega_m t_s = \theta$ into (15)-(18) to yield

$$\Delta T_u = \frac{1}{2}T_{SW} - \frac{1}{2}T_{SW} \cdot M \sin(\theta) \tag{19}$$

$$\Delta T_v = \frac{1}{2}T_{SW} - \frac{1}{2}T_{SW} \cdot M \sin\left(\theta - \frac{2\pi}{3}\right) \tag{20}$$

$$\Delta T_w = \frac{1}{2}T_{SW} - \frac{1}{2}T_{SW} \cdot M \sin\left(\theta + \frac{2\pi}{3}\right). \tag{21}$$

Equations (19)-(21) can be plotted to determine appropriate measurement times. Figure 10 corresponds to $M = 1$ and $\theta = -2\pi/3$. One can perform analysis to determine if the current will be approximately linear during the chosen measurement period. The measurement timing can be easily coordinated with switching.

B. Demonstration

The proposed measurement scheme has been demonstrated using a prototype drive of the form shown in Fig. 9. In this case, the motor is a 1hp induction machine, the microcontroller is a dsPIC30F6010A, and the MOSFETs are IRF540s. The microcontroller generates center-aligned PWM waveforms. Figure 12 shows the drain-to-source voltage across Q_4 and the phase U current. Δi_U and Δv_U are measured over the indicated window. As described above, the measurement is relatively straightforward to implement because the appropriate sampling window can be predetermined. Measurements are performed once every 100 periods of the modulating waveform. When applying the proposed approach with the waveforms shown in Fig. 12, the value of $R_{DS,ON}$ was found to be 40.2mΩ. For the given conditions (i.e. ambient temperature and current), the manufacturer datasheet predicts a value of 44mΩ [36]. Estimates of $R_{DS,ON}$ over a range of temperatures could be used to create the vector space needed for the condition-monitoring algorithm. The key implementation details are the same as for the IGBTs, with the need to perform a training step at the outset.

VI. Conclusion

Online methods for incipient fault detection will be essential as systems become more heavily dependent on power electronics. This paper has presented and demonstrated a health-

monitoring algorithm for power switches that can distinguish between true faults and changes in operating conditions. Ongoing work focuses on the inclusion of all appropriate features and the completion of an exhaustive battery of tests. Ultimately, we also seek to develop full prognostic capabilities (i.e. estimation of the time to failure).

VII. Acknowledgements

The authors would like to acknowledge comments and input from Adam Kabulski at Converteam Naval Systems.

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