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Experimental Study of 650V AlGaN/GaN HEMT Short-Circuit Safe Operating Area (SCSOA)

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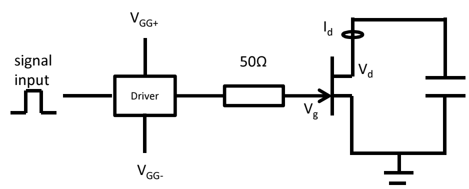
***Abstract*—The short-circuit reliability of power switches plays very important part in many applications, where a 10µs short-circuit duration at 400V is usually required for 650V switches. Although emerging high voltage AlGaN/GaN HEMT technologies have shown switching advantages, the short-circuit performance has not been thoroughly investigated. In this work, we present an experimental study and numerical simulation analysis of 650V AlGaN/GaN HEMTs short-circuit safe-operating-area (SCSOA), and provide a theory for the reduction in ruggedness at high voltage short circuit conditions.**

I. Introduction

Wide band gap (WBG) semiconductors, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), have been proven to be very efficient materials for power semiconductor devices [1] [2]. The adoption of WBG devices in power electronic applications generally leads to much higher switching frequency and higher power density than silicon solutions [3]–[5]. The reliability of SiC power devices have been well studied in the last decade and these device were reported to be able to handle large amount of energy under extreme conditions [6]–[8]. However, study of GaN devices in these conditions are rarely reported in the literature.

The short-circuit capability is an operational mode for which the limits must be characterized. It requires the switch to withstand the short-circuit connection to the DC bus for a couple of microseconds (usually 10µs) before the controller can detect and clear the fault. The huge amount of self-heating during the short-circuit event is usually regarded as the root cause of the failure and a critical temperature T_{cr} is usually used to describe the limitation for this operation [9]. For silicon switches, T_{cr} was reported to be around 650K and critical power density around 2000kW/cm^2 [10]. Significant improvement in short-circuit robustness can be achieved with better transient cooling method [11].

In previously published work, short durations under short-circuit operation have been reported on a commercial 200V normally-off AlGaN/GaN HEMT due to thermal instability and some of those devices only survived 2µs of short-circuit at 50% of nominal voltage [12]. Similar limitation has also been reported for 600V AlGaN/GaN HEMT that cannot withstand for 10µs of short-circuit at bus voltage beyond 200V [13]. However, the root cause for this weakness remains unknown. A systematical experimental study of GaN power device is due for better understanding of the failure mechanism.



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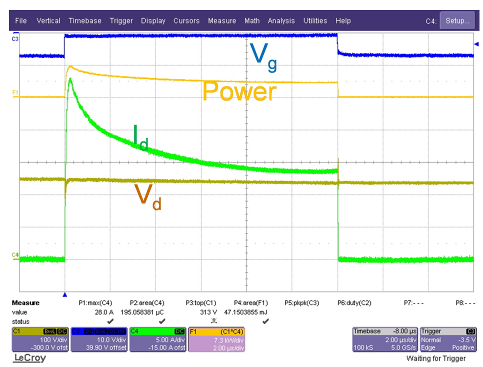

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Fig. 1. The set-up for short-circuit test.

In this paper, we present a comprehensive experimental study of the short-circuit SOA of the 650V depletion-mode AlGaN/GaN HEMT. Unlike conventional thermal failure of silicon or SiC devices at short-circuit operations, the root cause of the AlGaN/GaN HEMT, in this case, is not related to self-heating but some new electrical breakdown mechanism possibly related to the hole accumulation within the device.

II. Short-Circuit Experiment Setup

The 650V AlGaN/GaN depletion mode HEMTs with SiC substrates were fabricated at RFMD and were encapsulated in TO-220 packaging. The device has a typical on-resistance of 140mΩ and a thermally stable threshold voltage of -3V. In the short-circuit test, the drain of device under test (DUT) was directly connected to the DC bus and the gate was turned on for a short period to a preset on-state voltage V_{GG+}, as shown in Fig. 1(a). Due to the small gate charge (∼20nC), a relatively large gate resistance of 50Ω was used as external gate resistance to protect gate driver circuit from damages

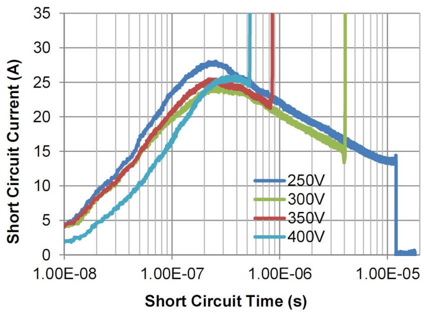


Fig. 2. The short-circuit current waveforms at various drain voltages.

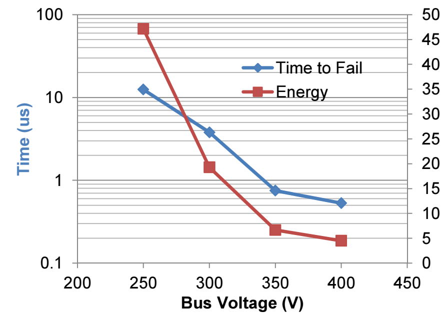


Fig. 3. The short-circuit duration and energy vs. bus voltage.

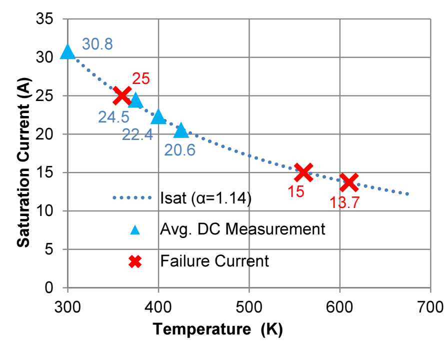


Fig. 4. I_{sat}-T_j model and estimation of failure temperature.

after failure of DUT. During the short-circuit operation, the device's gate voltage V_g, drain voltage V_d and drain current I_d were captured by probes. A typical survivable short-circuit waveform is shown in Fig. 1(b). The drain voltage stays the same with DC bus voltage and the saturation current becomes lower and lower due to self-heating and increased resistance at higher temperature. The dependence of short-circuit duration on V_d, was studied with on-state gate bias V_{GG+} fixed to ground and the dependence on V_{GG+} with fixed V_d at 400V.

III. Dependence on V_d

The short-circuit test started with the gate pulse width set to 1µs. The test was repeated with 1µs increment in pulse width until failure occurred or short-circuit duration exceeded 20µs. The test was done with DC bus voltages of 250, 300, 350 and 400V respectively. The last drain current waveform at each voltage level was plotted against the time in log scale (Fig. 2). The gate bias V_{GG+} during short-circuit was set to zero as the same as it is during normal operation. The short-circuit duration was found to decrease from more than 20µs at 250V DC bus to below 1µs at 400V. This negative correlation of drain bias against short-circuit duration and energy tolerance is plotted in Fig. 3.

Comparing the energies at different V_d, it is worthy being noticed that the absorbed energy at V_d=400V was only 4.5mJ or around 0.2J/cm^2, which is a very small amount of energy density compared with >5J/cm^2 of silicon parts [14] and >13.5J/cm^2 of SiC parts [8].

IV. Extraction of Failure Temperature

As the DUT operates at saturation region, one common way of extracting junction temperature is using the short-circuit current itself [15]. Because the threshold voltage is stable at elevated temperature and the biases at all the electrodes are fixed during the operation. Therefore, the major factor determining I_{sat} is the electron mobility in the channel that decreases with increasing junction temperature, T_j. Thus, we was able to be extracted based on the equation below:

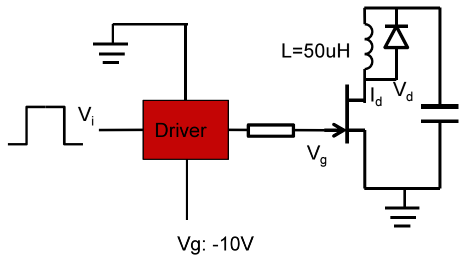
$$I_{sat} = I_{sat,300K}(T/300)^{-\alpha}$$

In Fig. 4, the blue points are the saturation current measured at various temperatures. The extracted temperature coefficient, α, was found to be around 1.14. In previous section, the failure current at 400, 300 and 250V were 25, 15 and 13.7A respectively and plotted with red marks in Fig. 4. Their corresponding failure junction temperatures, T_j, can be estimated from this I_{sat}-Temperature curve. It turned out that the failure temperature at drain bias higher than 300V does not exceed the 600K that is below silicon limit.

To further prove the low temperature at the 400V short-circuit failure, a light inductive load short-circuit test was carried out to compare the I-V trajectories at different temperatures (Fig. 5). The two samples tested at room temperature and 150 °C failed at 0.32µs and 0.39µs respectively after the drain bias reached DC bus voltage. Comparing the trajectories of the two temperature tests, the drain current at room temperature test never dropped below the corresponding I_{sat} at 150 °C. As the I_{sat} is only determined by temperature in this case, it proves that T_j is irrelevant to the failure at 400V. This excludes the thermal failure mechanisms for AlGaN/GaN HEMT power devices under short-circuit operation.

V. Dependence on V_{GG+}

The dependence of short-circuit performance on on-state gate bias, V_{GG+}, was tested with fixed drain bias of 400V and on-state gate bias varied from zero to -1.5V. As is shown in Fig. 7, the short-circuit ruggedness improved at lower gate



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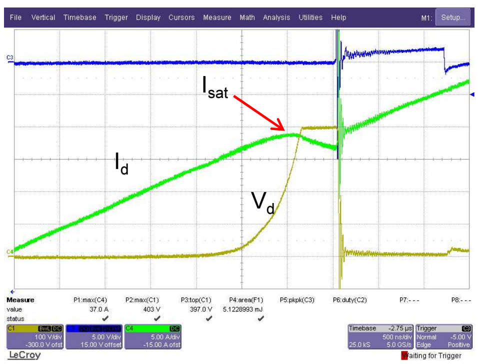

(b)

Fig. 5. The set-up for short-circuit test.

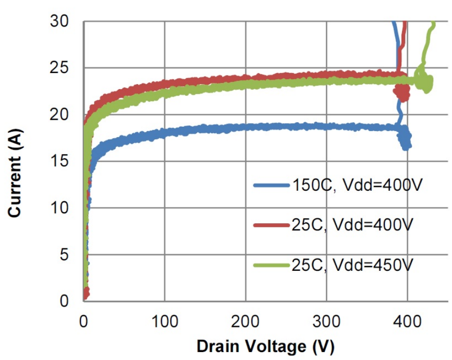

Fig. 6. I-V trajectories of short-circuit test with light inductive load.

bias. The energy tolerance of the device increased from 5mJ at V_{GG+}=0 to 85mJ at V_{GG+}=-1.5V. Similar influence of gate bias on short-circuit capability is known for silicon power MOSFETs due to suppressed second breakdown at lower gate voltage [16]. However, it is not likely to be the case of AlGaN/GaN HEMT due to lack of internal NPN transistors. A closer investigation on the gate voltage waveform shows a voltage tail at turn-off after long (>20µs) short-circuit operation (Fig. 8). The tail has a time constant of around 2µs and a peak current is more than 0.1A calculated from 50Ω gate resistance. As this gate waveform is not observed for shorter duration of short-circuit test and the integral of the charge is much higher than that of device gate charge, we believe extra charge was stored within the device during the operation.

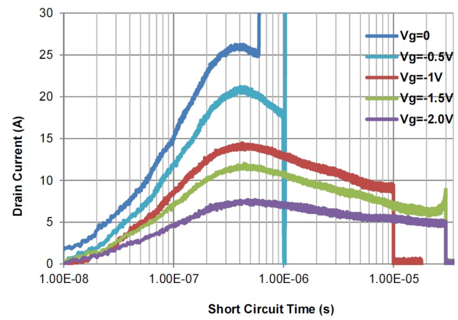

Fig. 7. I_{sat}-T_j model and estimation of failure temperature.

A steady-state numerical simulation was performed to explore a possible explanation of the stored charge. The avalanche generation at high field was calculated in lateral direction using the measured GaN impact ionization model given in the following equations [17]:

$$\alpha_n = 9.17 \times 10^5 e^{-\frac{1.72\times10^7}{E}}$$

$$\alpha_p = 8.7 \times 10^5 e^{-\frac{1.46\times10^7}{E}}$$

The TCAD simulation showed a very high density of holes ($>10^{18}$) located under the gate during the short-circuit operation(Fig. 9). The holes were generated at drift region due to severe impact ionization induced by high electron current injected from the channel.

These holes were then accumulated under the gate due to the valence band barrier of AlGaN/GaN heterojunction. Therefore, it comes to a speculation that, after turn-off, the diffusion of stored holes towards the source-side boundary of the depletion region could have caused the voltage tail in the gate (Fig. 10). According to the Poisson equation below, positively charged holes in depletion region are like the N-type doping ions and influences the shape of electric field in a similar way.

$$\frac{dE_x}{dx} + \frac{dE_y}{dy} = \frac{q(N_D^+ - N_A^- + p^+ - n^-)}{\varepsilon}$$

Therefore, the holes under the gate may introduce high field and cause premature breakdown in vertical direction or at source-gate region. This theory is consistent with the reported hole induced source-gate breakdown of AlGaN/GaN HEMT [18] [19]. In this case, the dependence of short-circuit reliability on V_d and V_{GG+} may be explained: at lower V_d, the avalanche multiplication is reduced due to lower field thus less holes are generated and better reliability was observed; at negative gate bias, the channel injects less electrons that induce avalanche generation of holes at high field, thus less stored charge can not disrupt the device.

VI. Conclusions

In summary, we have investigated the limited short-circuit capability of 650V rated AlGaN/GaN HEMT. The failure at

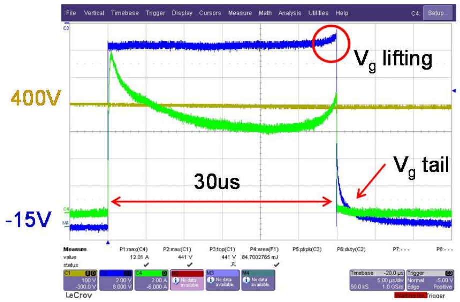

Fig. 8. I_{sat}-T_j model and estimation of failure temperature.

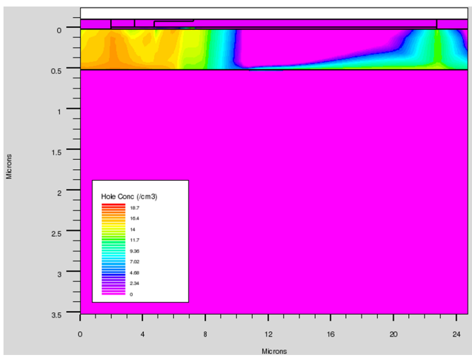

Fig. 9. I_{sat}-T_j model and estimation of failure temperature.

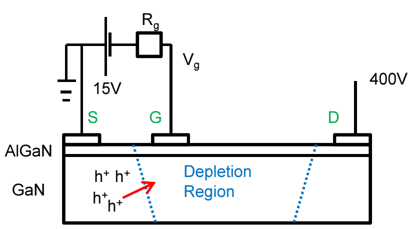

Fig. 10. I_{sat}-T_j model and estimation of failure temperature.

this condition is not thermally related because the extracted temperature at failure was below 150 °C. The device showed 10µs short-circuit capability with drain biased at 250V but the duration reduced to less than 0.5µs at 400V. However, lower on-state gate bias (<0V) can significantly enhance the durability and energy tolerance. At V_d=400V, as V_{GG+} was reduced from 0 to -1.5V, the short-circuit performance could be improved from <0.5µs to 30µs in durability and from 5mJ to 85mJ in energy tolerance. Based on the observed gate voltage tail and high density of holes shown in simulation, holes generated from impact ionization during the short-circuit operation could have caused the premature breakdown near the gate. Due to lack of direct observation of holes in this work, more study is still needed to further understand the failure mechanism of HV GaN HEMTs under short-circuit operation.

References

[1] G. Wang, X. Huang, J. Wang, T. Zhao, S. Bhattacharya, and A. Huang, "Comparisons of 6.5kV 25A Si IGBT and 10-kV SiC MOSFET in Solid-State Transformer application," in *Energy Conversion Congress and Exposition (ECCE), 2010 IEEE*, Sept 2010, pp. 100–104.

[2] X. Huang, Z. Liu, Q. Li, and F. Lee, "Evaluation and Application of 600 V GaN HEMT in Cascode Structure," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2453–2461, May 2014.

[3] C. Li, D. Jiao, M. Scott, C. Yao, L. Fu, X. Lu, T. Chen, J. Li, and J. Wang, "A 2 kW Gallium Nitride based switched capacitor three-port inverter," in *Wide Bandgap Power Devices and Applications (WiPDA), 2013 IEEE Workshop on*, Oct 2013, pp. 119–124.

[4] C. Pham, R. Teodorescu, T. Kerekes, and L. Mathe, "High efficiency battery converter with sic devices for residential pv systems," in *Power Electronics and Applications (EPE), 2013 15th European Conference on*, Sept 2013, pp. 1–10.

[5] A. Huang and J. Baliga, "FREEDM system: Role of power electronics and power semiconductors in developing an energy internet," in *Power Semiconductor Devices IC's, 2009. ISPSD 2009. 21st International Symposium on*, Jun. 2009, pp. 9 –12.

[6] X. Huang, G. Wang, L. Jiang, and A. Huang, "Ruggedness analysis of 600V 4H-SiC JBS diodes under repetitive avalanche conditions," in *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, Feb 2012, pp. 1688–1691.

[7] X. Huang, G. Wang, M.-C. Lee, and A. Huang, "Reliability of 4H-SiC SBD/JBS diodes under repetitive surge current stress," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, Sept 2012, pp. 2245–2248.

[8] X. Huang, G. Wang, Y. Li, A. Q. Huang, and B. Baliga, "Short-circuit capability of 1200V SiC MOSFET and JFET for fault protection," in *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*, March 2013, pp. 197–200.

[9] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 1st ed. Springer, Sep. 2008.

[10] H. Hagino, J. Yamashita, A. Uenishi, and H. Haruguchi, "An experimental and numerical study on the forward biased SOA of IGBTs," *Electron Devices, IEEE Transactions on*, vol. 43, no. 3, pp. 490–500, Mar 1996.

[11] F. Hille, F. Umbach, T. Raker, and R. Roth, "Failure mechanism and improvement potential of IGBT's short circuit operation," in *Power Semiconductor Devices IC's (ISPSD), 2010 22nd International Symposium on*, June 2010, pp. 33–36.

[12] C. Abbate, F. Iannuzzo, and G. Busatto, "Thermal instability during short circuit of normally-off AlGaN/GaN HFETs," *Microelectronics Reliability*, vol. 53, no. 911, pp. 1481 – 1485, 2013, european Symposium on Reliability of Electron Devices, Failure Physics and Analysis.

[13] R. Mitova, R. Ghosh, U. Mhaskar, D. Klikic, M.-X. Wang, and A. Dentella, "Investigations of 600-V GaN HEMT and GaN Diode for Power Converter Applications," *Power Electronics, IEEE Transactions on*, vol. 29, no. 5, pp. 2441–2452, May 2014.

[14] S. Lefebvre, Z. Khatir, and F. Saint-Eve, "Experimental behavior of single-chip IGBT and COOLMOS devices under repetitive short-circuit conditions," *Electron Devices, IEEE Transactions on*, vol. 52, no. 2, pp. 276–283, Feb 2005.

[15] Z. Xu, F. Wang, and P. Ning, "Junction temperature measurement of IGBTs using short circuit current," in *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*. IEEE, 2012, pp. 91–96.

[16] B. Zhang, Z. Xu, and A. Huang, "Analysis of the forward biased safe operating area of the super junction MOSFET," in *Power Semiconductor Devices and ICs, 2000. Proceedings. The 12th International Symposium on*, 2000, pp. 61–64.

[17] A. M. Ozbek, "Measurement of Impact Ionization Coefficients in Gallium Nitride," Ph.D. dissertation, North Carolina State University, 2011.

[18] S. Bahl, M. Van Hove, X. Kang, D. Marcon, M. Zahid, and S. Decoutere, "New source-side breakdown mechanism in AlGaN/GaN insulated-gate HEMTs," in *Power Semiconductor Devices and ICs (ISPSD), 2013 25th International Symposium on*, May 2013, pp. 419–422.

[19] T. Kachi, D. Kikuta, and T. Uesugi, "GaN power device and reliability for automotive applications," in *Reliability Physics Symposium (IRPS), 2012 IEEE International*. IEEE, 2012, pp. 3D–1.