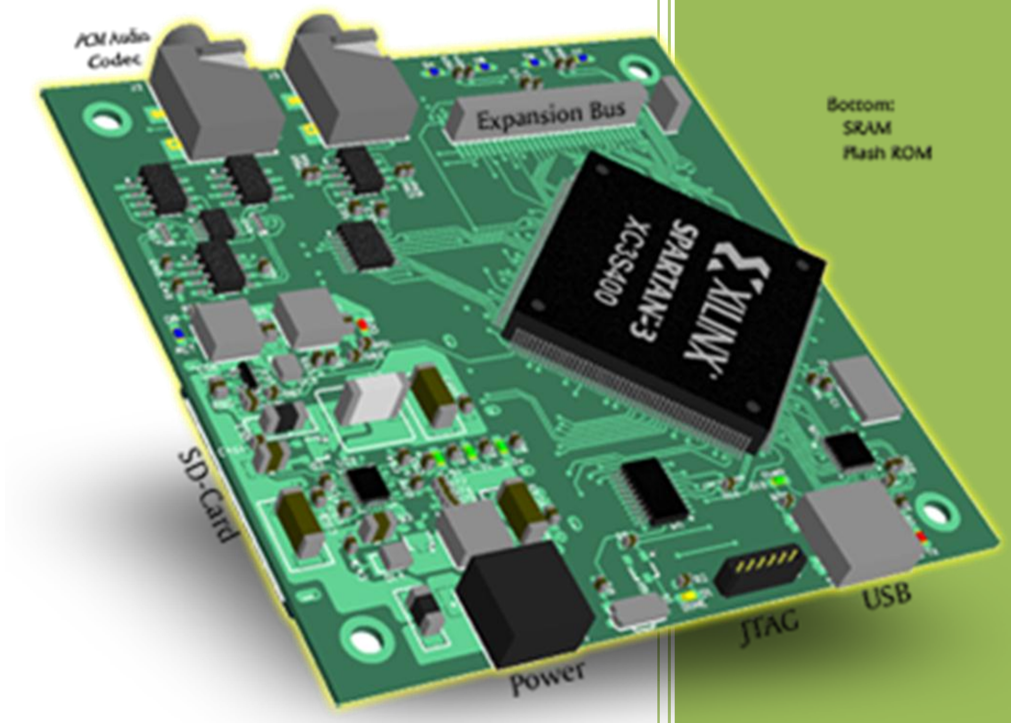
EHD FPGA Project

Digital Alarm Clock



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1. General Description

The aim this project is to implement the functionality of a digital alarm clock on a FPGA. As soon as the FPGA is switched on, the clock starts. The alarm can be set using the dip-switches provided on the FPGA board. This is indicated through the LEDs of the corresponding dip switch. The counter keeps rolling and as soon as the alarm goes off, a buzzer like sound is magnified via a speaker.

2. System Requirements

2.1 General Requirements

The Digital Alarm Clock system has the following general requirements:

- It should use low power
- The cost of production should be low
- The software architecture must be modular

2.2 Functional Requirements

The Digital Alarm Clock system should have following Functional Requirements:

- The clock timing should be accurate i.e. no glitches should be present.
- The design should use power judiciously.
- The speaker should play the sound clearly and should be synchronized.

2.3 Memory Requirements

No permanent storage is required. All the data is stored on the programming stack

3. Overview of the FPGA

3.1 Introduction

The Spartan™-3 family of Field-Programmable Gate Arrays is specifically designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The Spartan-3 family builds on the success of the earlier. Spartan-IIE family by increasing the amount of logic resources, the capacity of internal RAM, the total number of I/Os, and the overall level of performance as well as by improving clock management functions. Because of their exceptionally low cost, Spartan-3 FPGAs are ideally suited to a wide range of consumer electronics applications; including broadband access, home networking, display/projection and digital television equipment.

The Spartan-3 family is a superior alternative to mask programmed ASICs. FPGAs avoid the high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs.

3.2 Features

•Low-cost, high-performance logic solution for high-volume, consumer-oriented applications

-Densities up to 74,880 logic cells

•SelectIO™ signaling

-Up to 784 I/O pins

-622 Mb/s data transfer rate per I/O

-18 single-ended signal standards

-8 differential I/O standards including LVDS, RSD

-Termination by Digitally Controlled Impedance

-Signal swing ranging from 1.14V to 3.45V

-Double Data Rate (DDR) support

-DDR, DDR2 SDRAM support up to 333 Mbps

•Logic resources

-Abundant logic cells with shift register capability

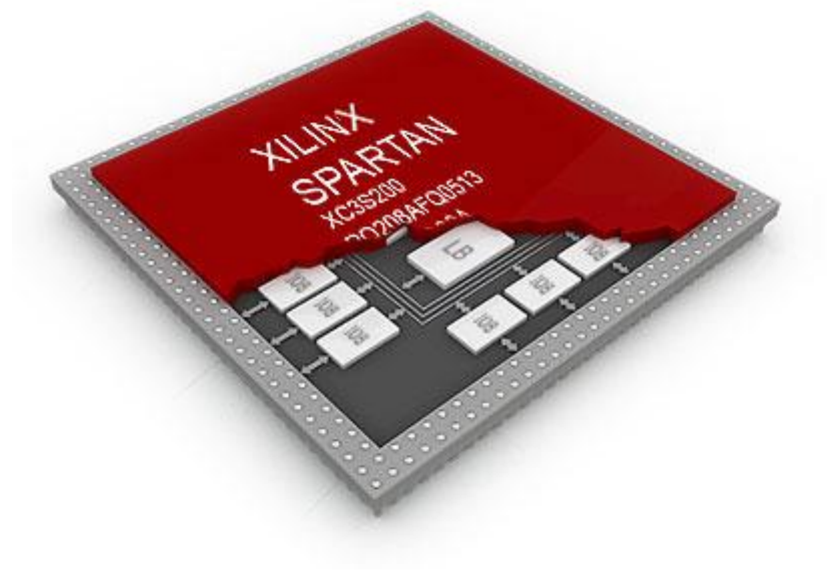
-Wide, fast multiplexers

-Fast look-ahead carry logic

-Dedicated 18 x 18 multipliers

-JTAG logic compatible with IEEE 1149.1/1532

- SelectRAM™ hierarchical memory
  - Up to 1,872 Kbits of total block RAM
  - Up to 520 Kbits of total distributed RAM
- Digital Clock Manager (up to four DCMs)
  - Clock skew elimination
  - Frequency synthesis
  - High resolution phase shifting
- Eight global clock lines and abundant routing
- Fully supported by Xilinx ISE development system
  - Synthesis, mapping, placement and routing
- MicroBlaze™ processor, PCI, and other cores
- Pb-free packaging options
- Low-power Spartan-3L Family and Automotive Spartan-3 XA Family variants



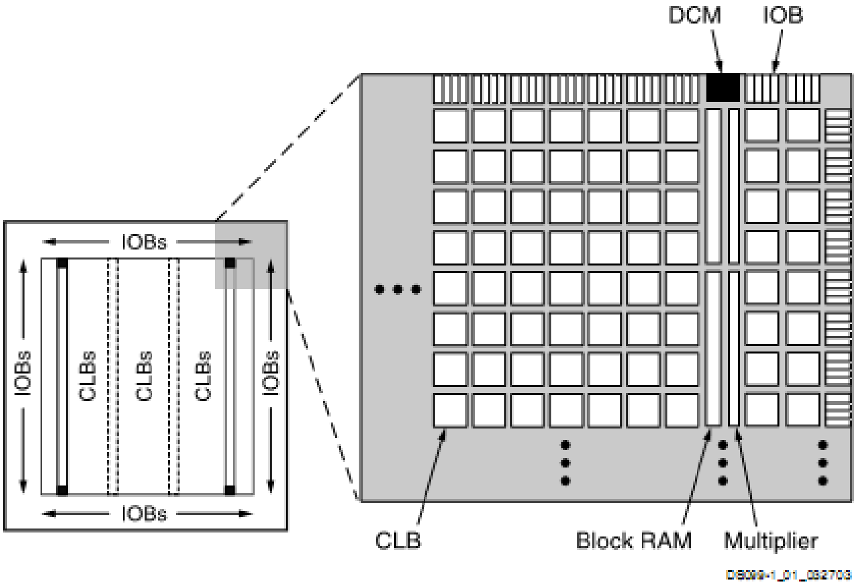
4. Architectural Overview of the FPGA

4.1 Architectural Overview

The Spartan-3 family architecture consists of five fundamental programmable functional elements:

1. **Configurable Logic Blocks (CLBs)** contain RAM-based Look-Up Tables (LUTs) to implement logic and storage elements that can be used as flip-flops or latches. CLBs can be programmed to perform a wide variety of logical functions as well as to store data.
2. **Input-Output Blocks (IOBs)** control the flow of data between the I/O pins and the internal logic of the device. Each IOB supports bidirectional data flow plus 3-state operation. Twenty-four different signal standards, including seven high-performance differential standards, are available as shown in Table2. Double Data-Rate (DDR) registers are included. The Digitally Controlled Impedance (DCI) feature provides automatic on-chip terminations, simplifying board designs.
3. **Block RAM** provides data storage in the form of 18-Kbit dual-port blocks.
4. **Multiplier blocks** accept two 18-bit binary numbers as inputs and calculate the product.
5. **Digital Clock Manager (DCM)** blocks provide self-calibrating, fully digital solutions for distributing, delaying, multiplying, dividing, and phase shifting clock signals.

These elements are organized as shown in Figure below. A ring of IOBs surrounds a regular array of CLBs.

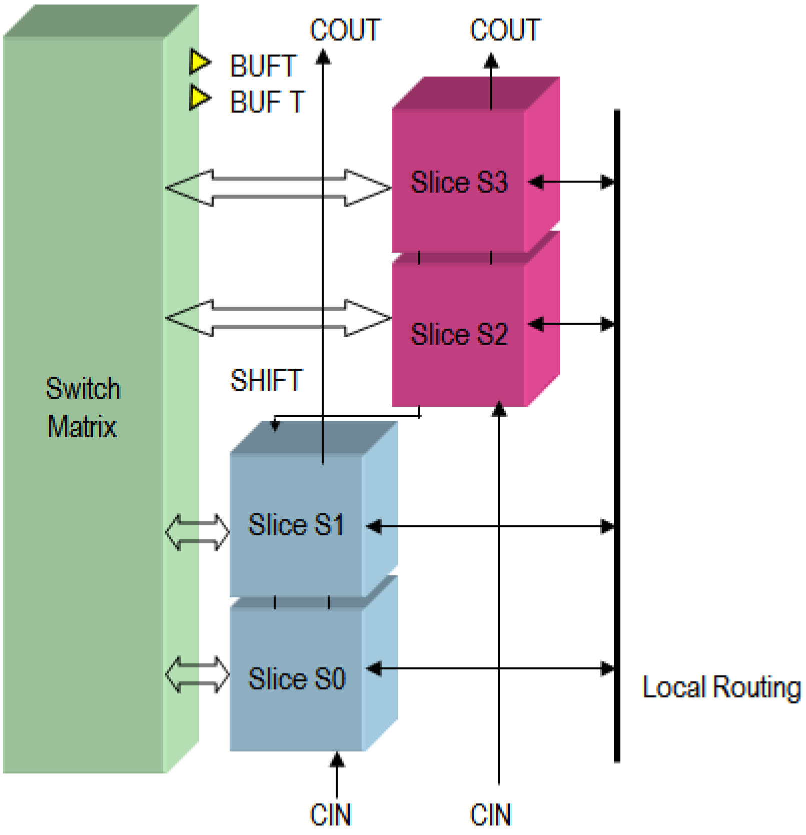


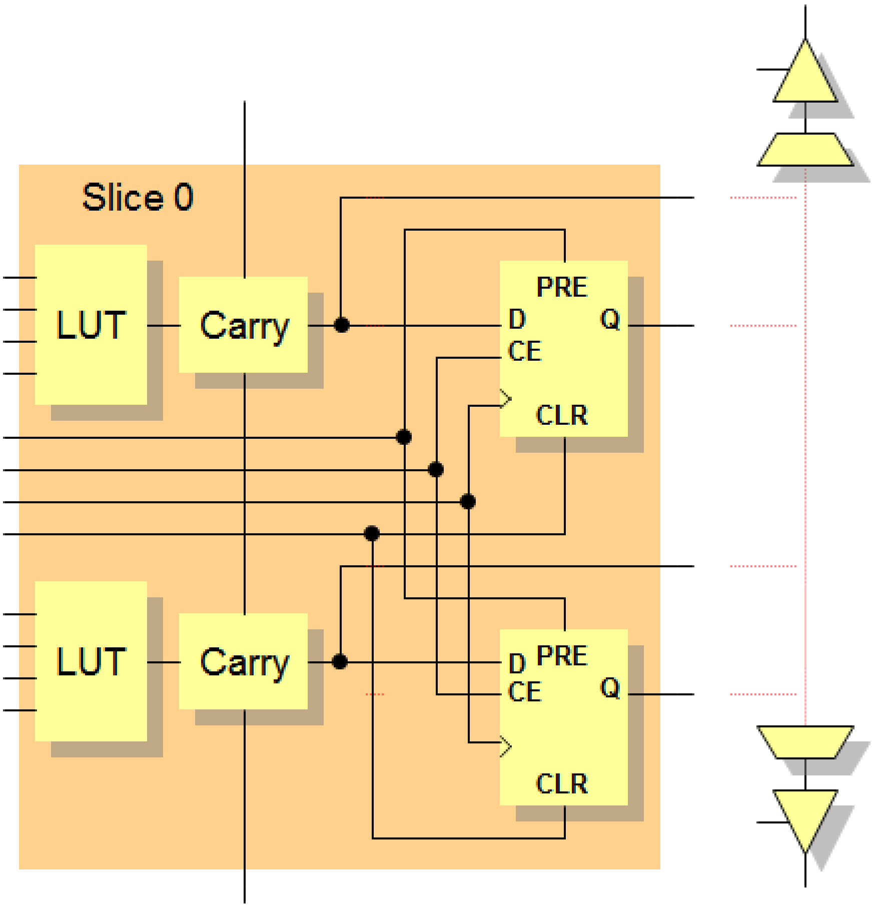
Spartan-3 Family Architecture

4.2 Configurable Logic Blocks (CLBs)

The Configurable Logic Blocks (CLBs) constitute the main logic resource for implementing synchronous as well as combinatorial circuits. Each CLB comprises four interconnected slices. These slices are grouped in pairs. Each pair is organized as a column with an independent carry chain.

- Local routing provides feedback between slices in the same CLB, and it provides routing to neighboring CLBs
- A switch matrix provides access to general routing resources
- Each slice has four outputs
  - Two registered outputs, two non-registered outputs
  - Two BUFTs associated with each CLB, accessible by all 16 CLB outputs





Simplified Slice Structure

4.2.1 Look Up Tables

- Combinatorial logic is stored in Look-Up Tables (LUTs)
  - Also called Function Generators (FGs)
  - Capacity is limited by the number of inputs, not by the complexity
- Delay through the LUT is constant

The RAM-based function generator — also known as a Look-Up Table or LUT — is the main resource for implementing logic functions. Furthermore, the LUTs in each left-hand slice pair can be configured as Distributed RAM or a 16-bit shift register.
The storage element, which is programmable as either a D-type flip-flop or a level-sensitive latch, provides a means for synchronizing data to a clock signal, among other uses.
The storage elements in the upper and lower portions of the slice are called FFY and FFX, respectively. Wide-function multiplexers effectively combine LUTs in order to permit more complex logic operations.

4.3 Input-output Blocks (IOB)

The Input-Output Block (IOB) provides a programmable, bidirectional interface between an I/O pin and the FPGA's internal logic. There are three main signal paths within the IOB: the output path, input path, and 3-state path. Each path has its own pair of storage elements that can act as either registers or latches.

The three main signal paths are as follows:

•The input path carries data from the pad, which is bonded to a package pin, through an optional programmable delay element directly to the I line. There are alternate routes through a pair of storage elements to the IQ1 and IQ2 lines. The IOB outputs I, IQ1, and IQ2 all lead to the FPGA's internal logic. The delay element can be set to ensure a hold time of zero.

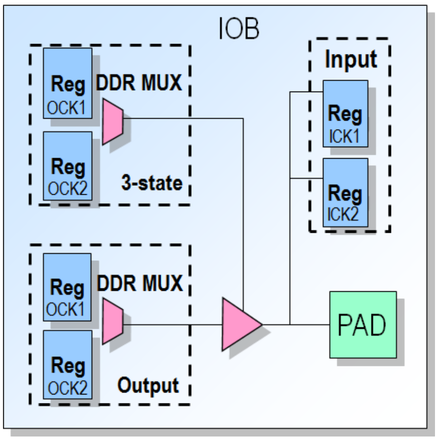
•The output path, starting with the O1 and O2 lines, carries data from the FPGA's internal logic through a multiplexer and then a three-state driver to the IOB pad. In addition to this direct path, the multiplexer provides the option to insert a pair of storage elements.

•The 3-state path determines when the output driver is high impedance. The T1 and T2 lines carry data from the FPGA's internal logic through a multiplexer to the output driver. In addition to this direct path, the multiplexer provides the option to insert a pair of

storage elements. When the T1 or T2 lines are asserted High, the output driver is high-impedance (floating, Hi-Z). The output driver is active-Low enabled.

All signal paths entering the IOB, including those associated with the storage elements, have an inverter option. Any inverter placed on these paths is automatically absorbed into the IOB.

There are three pairs of storage elements in each IOB, one pair for each of the three paths. It is possible to configure each of these storage elements as an edge-triggered D-type flip-flop (FD) or a level-sensitive latch (LD). The storage-element-pair on either the Output path or the Three-State path can be used together with a special multiplexer to produce Double-Data-Rate (DDR) transmission. This is accomplished by taking data synchronized to the clock signal's rising edge and converting them to bits synchronized on both the rising and the falling edge.

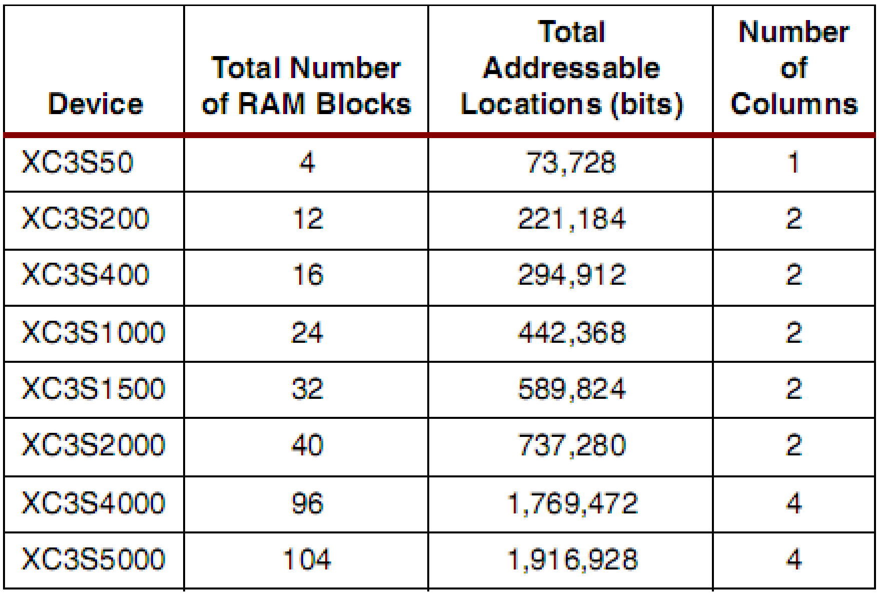


4.4 Block RAM

All Spartan-3 devices support block RAM, which is organized as configurable, synchronous 18Kbit blocks. Block RAM stores relatively large amounts of data more efficiently than the distributed RAM feature described earlier. (The latter is better suited for buffering small amounts of data any-where along signal paths) The aspect ratio — i.e., width vs. depth — of each block RAM is configurable. Furthermore, multiple blocks can be cascaded to create still wider and/or deeper memories.

4.4.1 Arrangement of RAM Blocks on die

The XC3S50 has one column of block RAM. The Spartan-3 devices ranging from the XC3S200 to XC3S2000 have two columns of block RAM. The XC3S4000 and XC3S5000 have four columns. The position of the columns on the die is shown in the following figure. For a given device, the total available RAM blocks are distributed equally among the columns. The following table shows the number of RAM blocks, the data storage capacity, and the number of columns for each device.



Device	Total Number of RAM Blocks	Total Addressable Locations (bits)	Number of Columns
XC3S50	4	73,728	1
XC3S200	12	221,184	2
XC3S400	16	294,912	2
XC3S1000	24	442,368	2
XC3S1500	32	589,824	2
XC3S2000	40	737,280	2
XC3S4000	96	1,769,472	4
XC3S5000	104	1,916,928	4

4.4.2 Internal structure of the Block RAM

The block RAM has a dual port structure. The two identical data ports called A and B permit independent access to the common RAM block, which has a maximum capacity of 18,432 bits — or 16,384 bits when no parity lines are used.

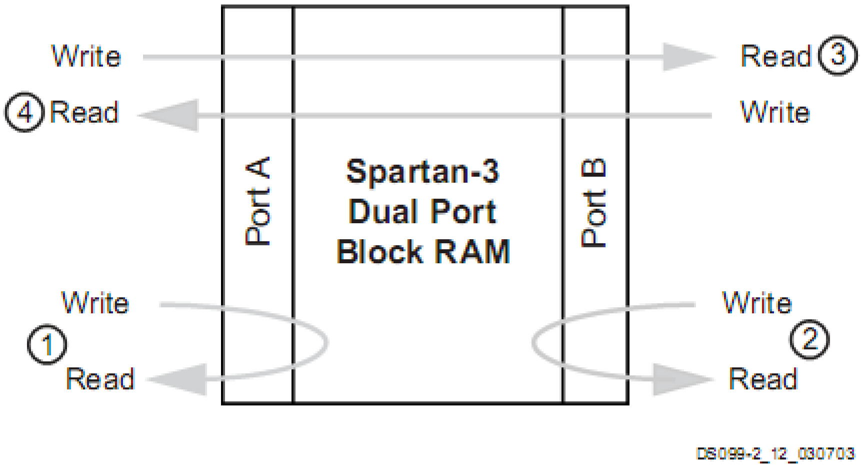
Each port has its own dedicated set of data, control and clock lines for synchronous read and write operations There are four basic data paths, as shown in the figure:

(1) Write to and read from Port A

(2) Write to and read from Port B

(3) Data transfer from Port A to Port B

(4) Data transfer from Port B to Port A.



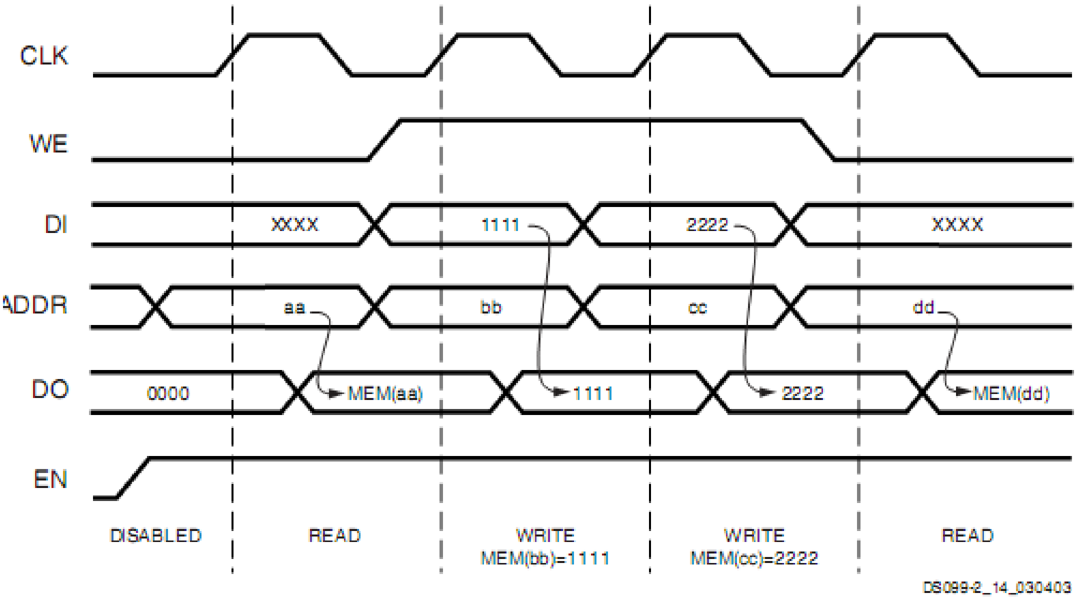
4.4.3 Block RAM Data Operations

Writing data to and accessing data from the block RAM are synchronous operations that take place independently on each of the two ports. The waveforms for the write operation are shown in the following three figures. When the WE and EN signals enable the active edge of CLK, data at the DI input bus is written to the block RAM location addressed by the ADDR lines. There are a number of different conditions under which data can be accessed at the DO outputs. Basic data access always occurs when the WE input is inactive. Under this condition, data stored in the memory location addressed by the ADDR lines passes through a transparent output latch to the DO outputs. The timing for basic data access is shown in the portions of the three figures during which WE is Low.

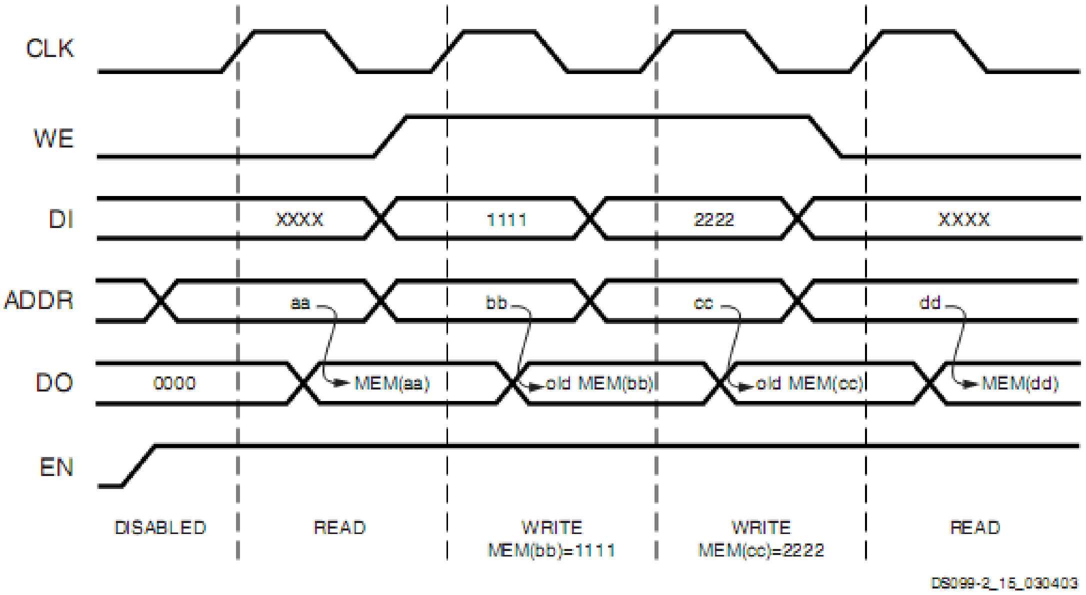
Data can also be accessed on the DO outputs when asserting the WE input. This is accomplished using two different attributes:

(i) Choosing the WRITE_FIRST attribute,

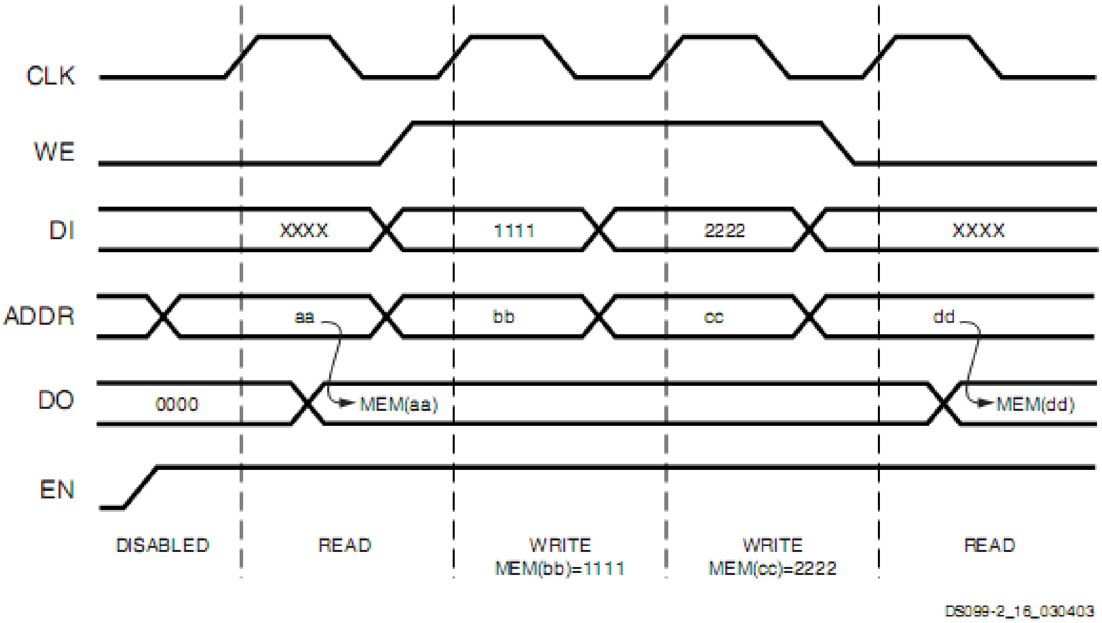
Data is written to the addressed memory location on an enabled active CLK edge and is also passed to the DO outputs. WRITE_FIRST timing is shown in the portion of the following figure, during which WE is high.



(ii)Choosing the READ_FIRST attribute, data already stored in the addressed location pass to the DO outputs before that location is overwritten with new data from the DI inputs on an enabled active CLK edge. READ_FIRST timing is shown in the portion of the following figure, during which WE is high.



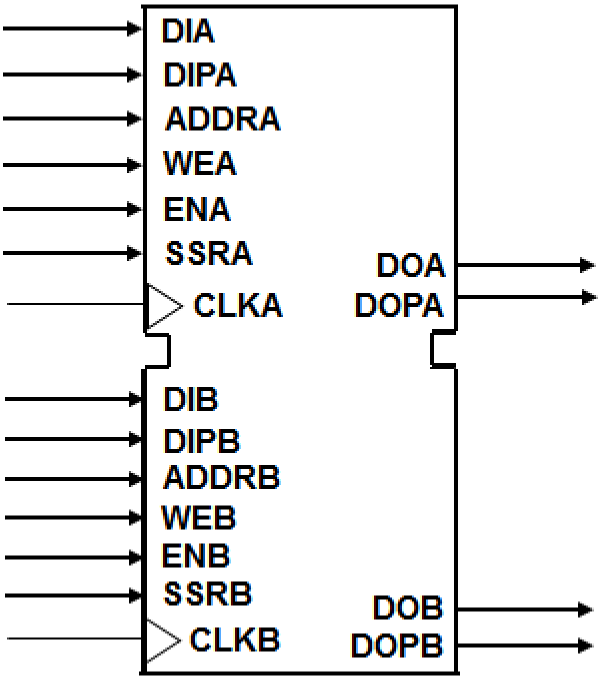
(iii)Choosing a third attribute called NO_CHANGE puts the DO outputs in a latched state when asserting WE. Under this condition, the DO outputs will retain the data driven just before WE was asserted. NO_CHANGE timing is shown in the portion of the following figure, during which WE is high.



4.4.4 Block SelectRAM Resources

- Up to 3.5 Mb of RAM in 18-kb blocks
  - Synchronous read and write
- True dual-port memory
  - Each port has synchronous read and write capability
  - Different clocks for each port
- Supports initial values
- Synchronous reset on output latches
- Supports parity bits
  - One parity bit per eight data bits

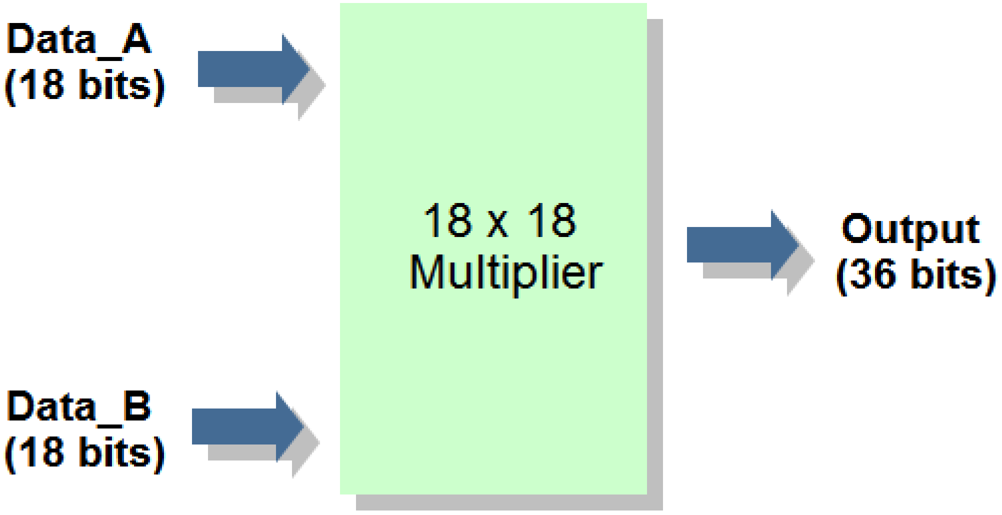
18-kb block SelectRAM memory



4.5 Multiplier Block

All Spartan-3 devices provide embedded multipliers that accept two 18-bit words as inputs to produce a 36-bit product. The input buses to the multiplier accept data in two's-complement form (either 18-bit signed or 17-bit unsigned). One such multiplier is matched to each block RAM on the die. The close physical proximity of the two ensures efficient data handling. Cascading multipliers permits multiplicands more than three in number as well as wider than 18-bits.

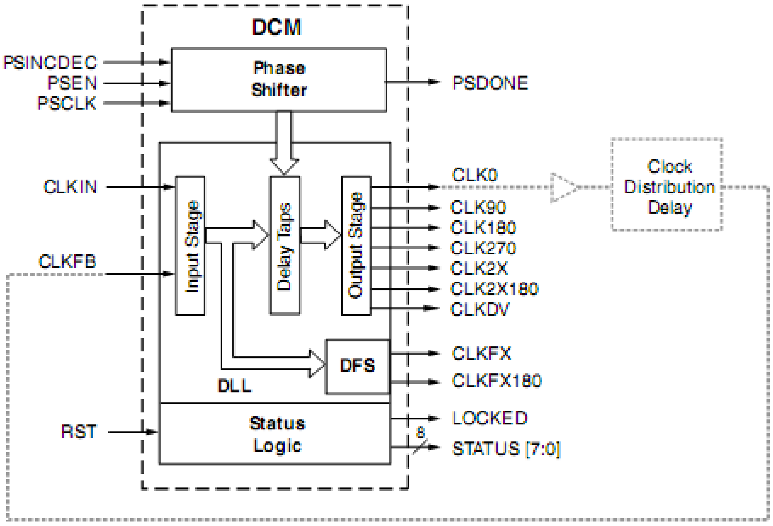
The multiplier is placed in a design using one of two primitives: an asynchronous version called MULT18X18 and a version with a register called MULT18X18S. The signals for these primitives are defined in Table11. The CORE Generator system produces multipliers based on these primitives that can be configured to suit a wide range of requirements.



4.6 Digital Clock Manager

Spartan-3 devices provide flexible, complete control over clock frequency, phase shift and skew through the use of the DCM feature. To accomplish this, the DCM employs a Delay-Locked Loop (DLL), a fully digital control system that uses feedback to maintain clock signal characteristics with a high degree of precision despite normal variations in operating temperature and voltage. This section provides a fundamental description of the DCM. Using Digital Clock Managers (DCMs) in Spartan-3 FPGAs. Each member of the Spartan-3 family has four DCMs, except the smallest, the XC3S50, which has two DCMs. The DCMs are located at the ends of the outermost Block RAM column(s). The Digital Clock Manager is placed in a design as the “DCM” primitive. The DCM supports three major functions:

- Clock-skew Elimination: Clock skew describes the extent to which clock signals may, under normal circumstances, deviate from zero-phase alignment. It occurs when slight differences in path delays cause the clock signal to arrive at different points on the die at different times. This clock skew can increase set-up and hold time requirements as well as clock-to-out time, which may be undesirable in applications operating at a high frequency, when timing is critical. The DCM eliminates clock skew by aligning the output clock signal it generates with another version of the clock signal that is fed back. As a result, the two clock signals establish a zero-phase relationship. This effectively cancels out clock distribution delays that may lie in the signal path leading from the clock output of the DCM to its feedback input.
- Frequency Synthesis: Provided with an input clock signal, the DCM can generate a wide range of different output clock frequencies. This is accomplished by either multiplying and/or dividing the frequency of the input clock signal by any of several different factors.
- Phase Shifting: The DCM provides the ability to shift the phase of all its output clock signals with respect to its input clock signal.



DCM Functional Blocks and Associated Signals

5. Design Summary

Summary

ALARM Project Status			
Project File:	alarm.ise	**Current State:**	Placed and Routed
Module Name:	alarm	• **Errors:**	No Errors
Target Device:	xc3s400-4pq208	• **Warnings:**	6 Warnings
Product Version:	ISE 8.2i	• **Updated:**	Mon 15. Nov 16:31:44 2010

ALARM Partition Summary			
Partition Name	**Synthesis Status**	**Placement Status**	**Routing Status**
/alarm	Implemented		

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	59	7,168	1%	
Number of 4 input LUTs	125	7,168	1%	
Logic Distribution				
Number of occupied Slices	81	3,584	2%	
Number of Slices containing only related logic	81	81	100%	
Number of Slices containing unrelated logic	0	81	0%	
Total Number 4 input LUTs	147	7,168	2%	
Number used as logic	125			
Number used as a route-thru	22			
Number of bonded IOBs	29	141	20%	

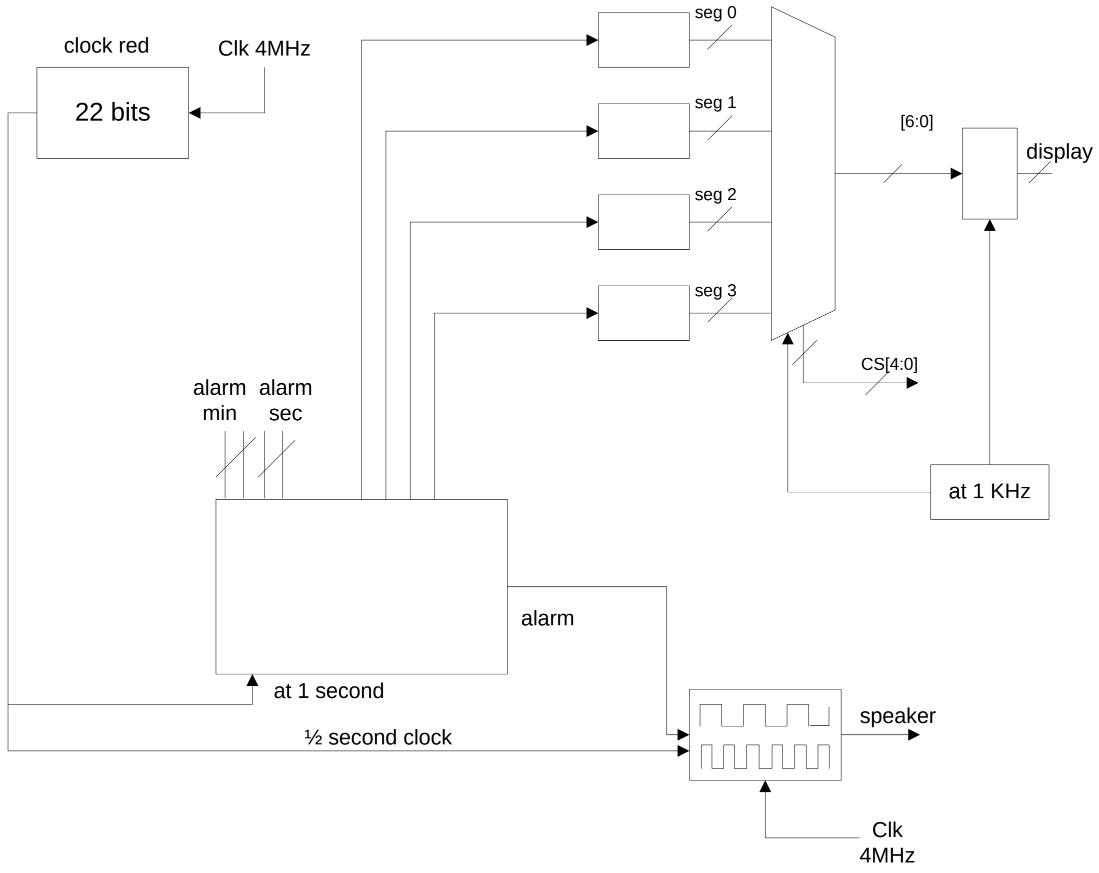
IOB Flip Flops	19		
Number of GCLKs	2	8	25%
Total equivalent gate count for design	1,605		
Additional JTAG gate count for IOBs	1,392		

Performance Summary			
Final Timing Score:	0	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

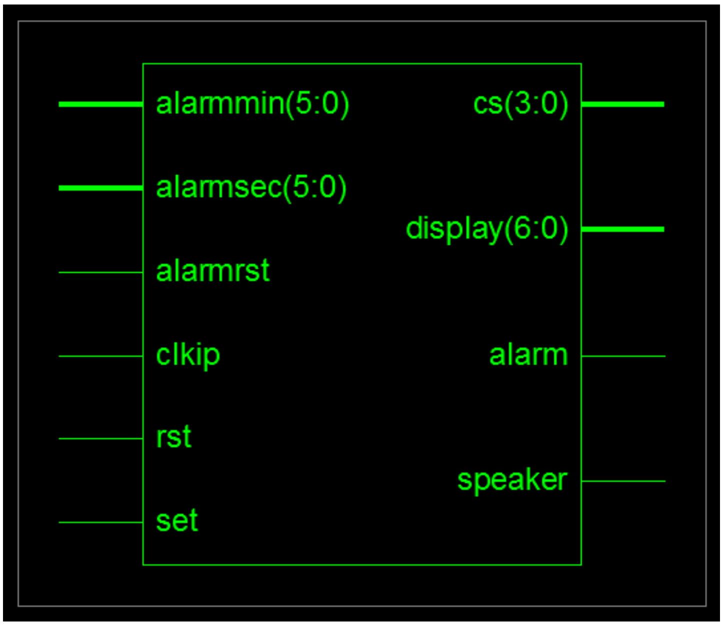
Detailed Reports					
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Mon 15. Nov 16:26:50 2010	0	4 Warnings	3 Infos
Translation Report	Current	Mon 15. Nov 16:28:04 2010	0	0	0
Map Report	Current	Mon 15. Nov 16:28:11 2010	0	0	3 Infos
Place and Route Report	Current	Mon 15. Nov 16:28:23 2010	0	2 Warnings	2 Infos
Static Timing Report	Current	Mon 15. Nov 16:28:27 2010	0	0	2 Infos
Bitgen Report					

Secondary Reports		
Report Name	**Status**	**Generated**
Xplorer Report		

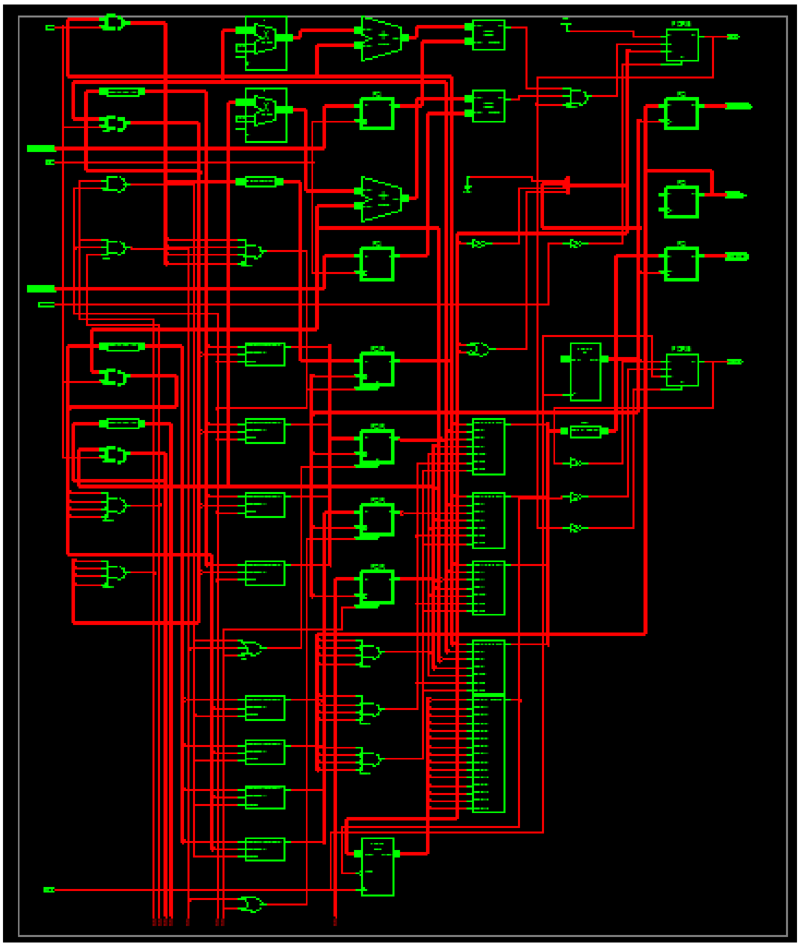
5.1 Block Diagram



5.2 RTL Schematic

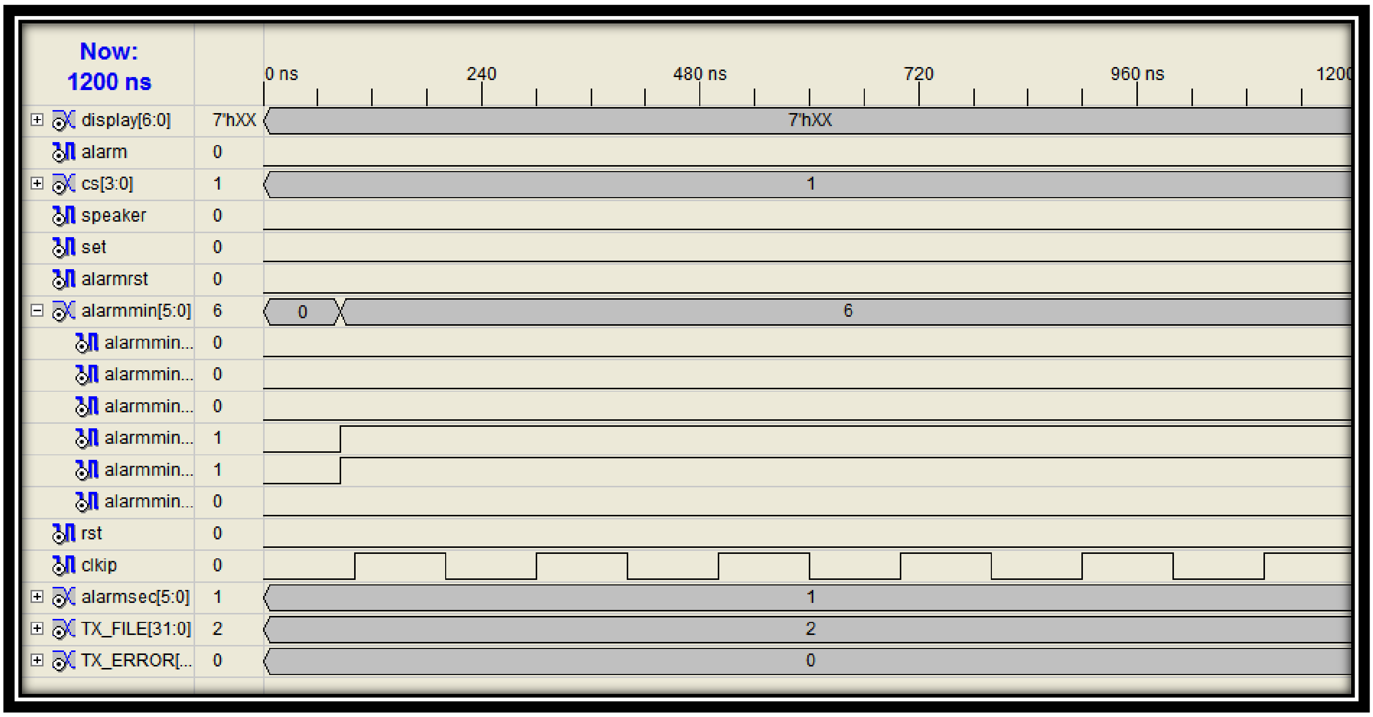


Level 1

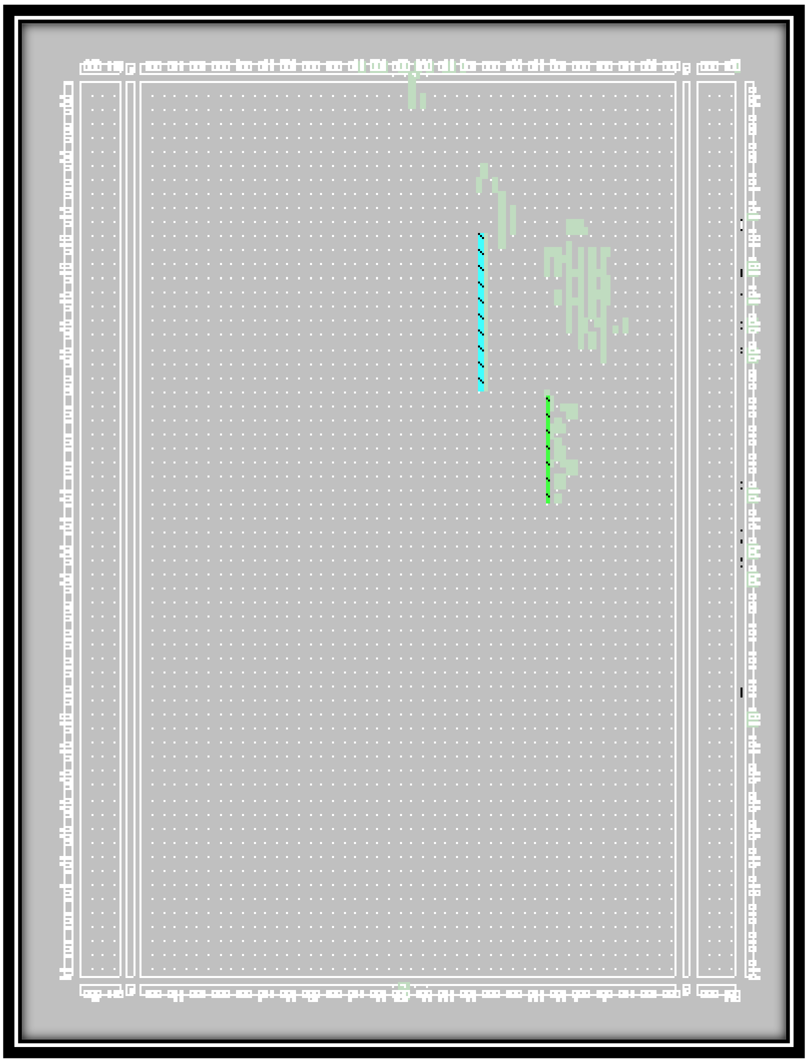


Level 2

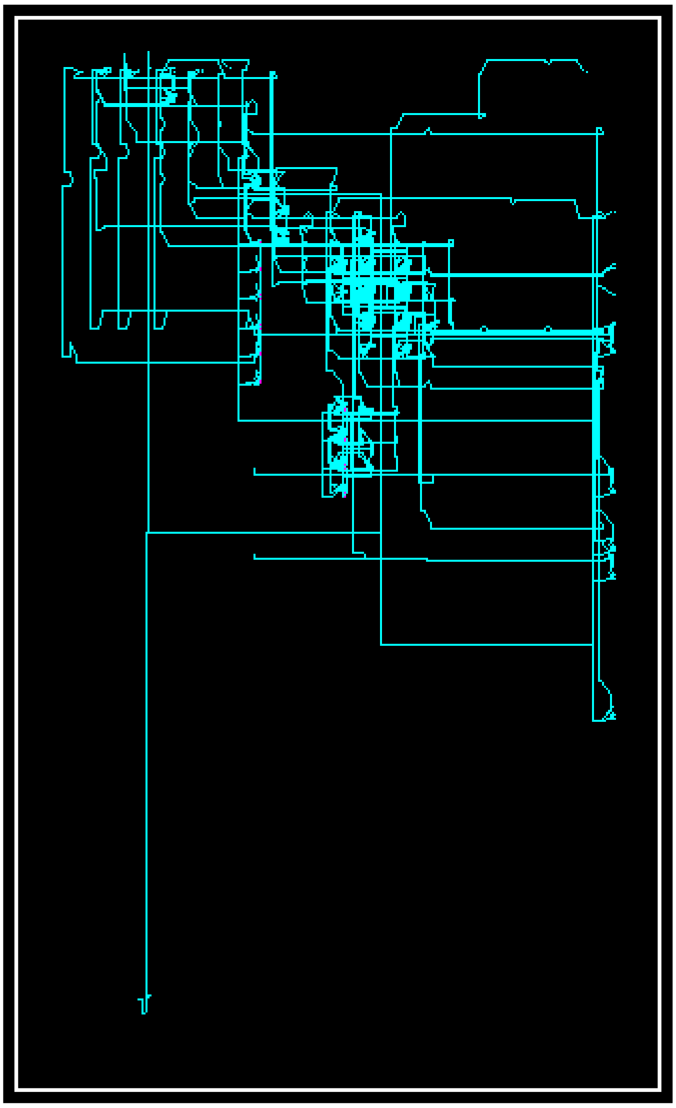
5.3 Testbench Waveform



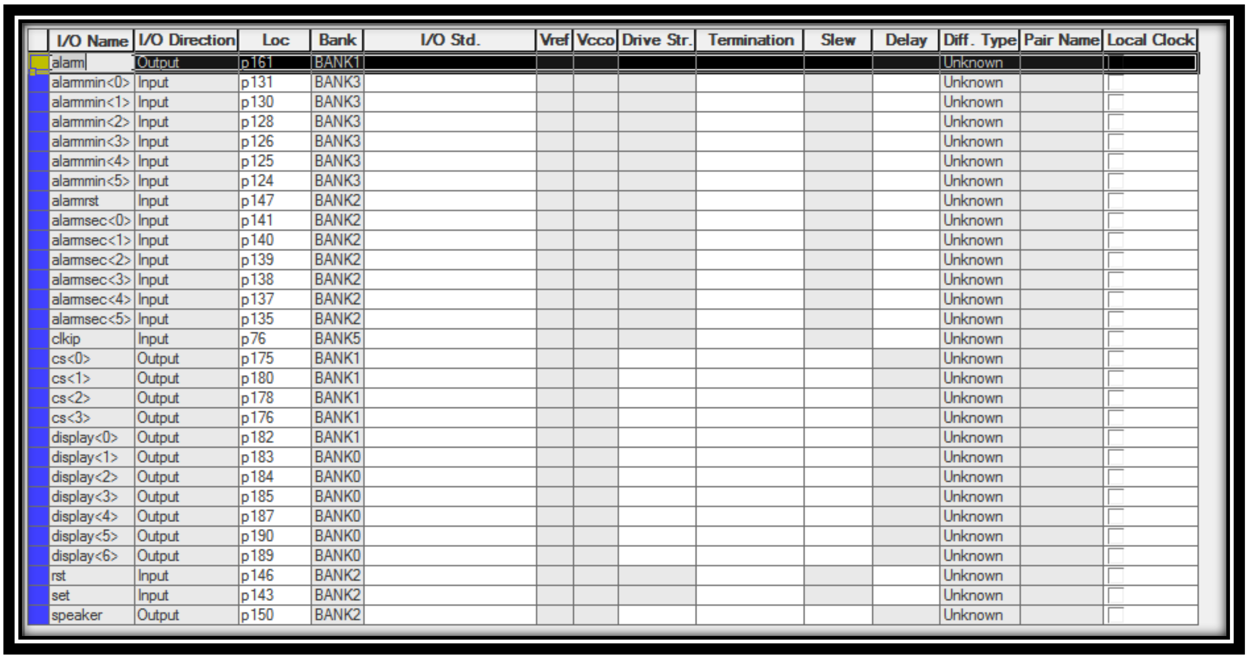
5.4 Floorplan Design



5.5 Clock Route



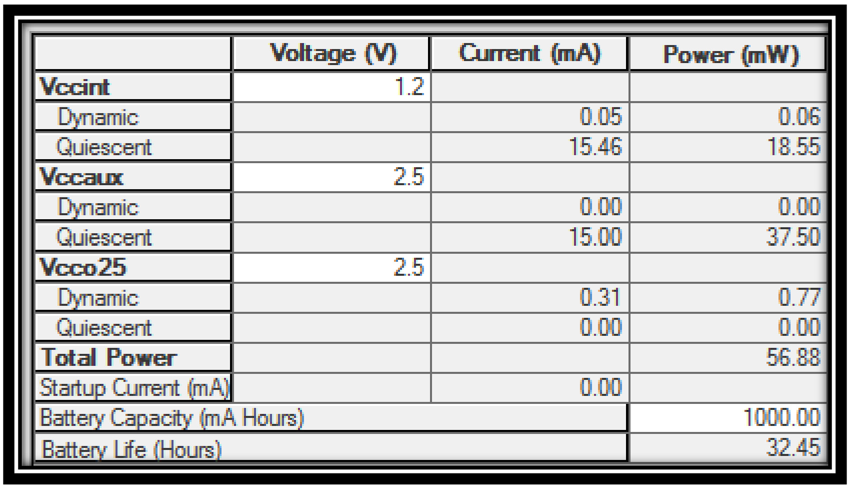
5.6 Pin Configuration



	I/O Name	I/O Direction	Loc	Bank	I/O Std.	Vref	Vcco	Drive Str.	Termination	Slew	Delay	Diff. Type	Pair Name	Local Clock
🟨	alarm	Output	p161	BANK1								Unknown		□
🟦	alammin<0>	Input	p131	BANK3								Unknown		□
🟦	alammin<1>	Input	p130	BANK3								Unknown		□
🟦	alammin<2>	Input	p128	BANK3								Unknown		□
🟦	alammin<3>	Input	p126	BANK3								Unknown		□
🟦	alammin<4>	Input	p125	BANK3								Unknown		□
🟦	alammin<5>	Input	p124	BANK3								Unknown		□
🟦	alamrst	Input	p147	BANK2								Unknown		□
🟦	alamsec<0>	Input	p141	BANK2								Unknown		□
🟦	alamsec<1>	Input	p140	BANK2								Unknown		□
🟦	alamsec<2>	Input	p139	BANK2								Unknown		□
🟦	alamsec<3>	Input	p138	BANK2								Unknown		□
🟦	alamsec<4>	Input	p137	BANK2								Unknown		□
🟦	alamsec<5>	Input	p135	BANK2								Unknown		□
🟦	clkip	Input	p76	BANK5								Unknown		□
🟦	cs<0>	Output	p175	BANK1								Unknown		□
🟦	cs<1>	Output	p180	BANK1								Unknown		□
🟦	cs<2>	Output	p178	BANK1								Unknown		□
🟦	cs<3>	Output	p176	BANK1								Unknown		□
🟦	display<0>	Output	p182	BANK1								Unknown		□
🟦	display<1>	Output	p183	BANK0								Unknown		□
🟦	display<2>	Output	p184	BANK0								Unknown		□
🟦	display<3>	Output	p185	BANK0								Unknown		□
🟦	display<4>	Output	p187	BANK0								Unknown		□
🟦	display<5>	Output	p190	BANK0								Unknown		□
🟦	display<6>	Output	p189	BANK0								Unknown		□
🟦	rst	Input	p146	BANK2								Unknown		□
🟦	set	Input	p143	BANK2								Unknown		□
🟦	speaker	Output	p150	BANK2								Unknown		□

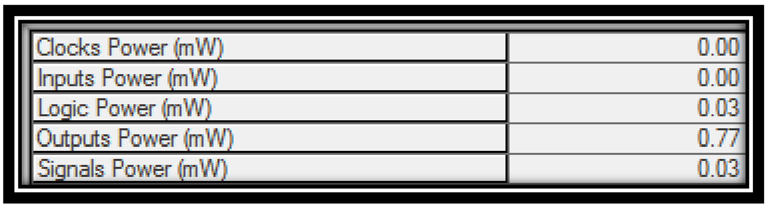
5.7 Power Analysis

5.7.1 Summary



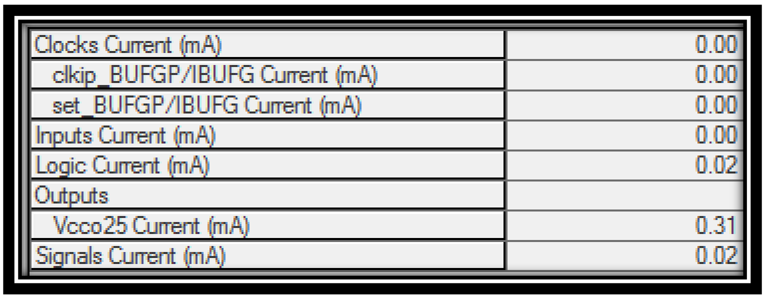
	Voltage (V)	Current (mA)	Power (mW)
Vccint	1.2		
Dynamic		0.05	0.06
Quiescent		15.46	18.55
Vccaux	2.5		
Dynamic		0.00	0.00
Quiescent		15.00	37.50
Vcco25	2.5		
Dynamic		0.31	0.77
Quiescent		0.00	0.00
Total Power			56.88
Startup Current (mA)		0.00	
Battery Capacity (mA Hours)			1000.00
Battery Life (Hours)			32.45

5.7.2 Power Subtotals



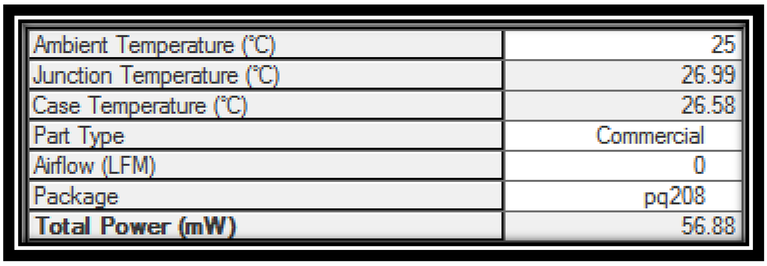
Clocks Power (mW)	0.00
Inputs Power (mW)	0.00
Logic Power (mW)	0.03
Outputs Power (mW)	0.77
Signals Power (mW)	0.03

5.7.3 Current Subtotals



Clocks Current (mA)	0.00
clkip_BUFGP/IBUFG Current (mA)	0.00
set_BUFGP/IBUFG Current (mA)	0.00
Inputs Current (mA)	0.00
Logic Current (mA)	0.02
Outputs	
Vcco25 Current (mA)	0.31
Signals Current (mA)	0.02

5.7.4 Thermal



Ambient Temperature (°C)	25
Junction Temperature (°C)	26.99
Case Temperature (°C)	26.58
Part Type	Commercial
Airflow (LFM)	0
Package	pq208
Total Power (mW)	56.88

5.7.5 Power Report

Release 8.2i - XPower SoftwareVersion:I.31 Copyright (c) 1995-2006 Xilinx, Inc. All rights reserved.
Copyright (c) 1995-2006 Xilinx, Inc. All rights reserved.

Design:	C:\Users\Yash\Desktop\alarm_clock\alarm.ncd
Preferences:	alarm.pcf
VCD File:	C:\Users\Yash\Desktop\alarm_clock\xpower3.vcd
Part:	3s400pq208-4
Data version:	ADVANCED,v1.0,11-03-03

XPower and Datasheet may have some Quiescent Current differences. This is due to the fact that the quiescent numbers in XPower are based on measurements of real designs with active functional elements reflecting real world design scenarios.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		57
Vccint 1.20V:	16	19
Vccaux 2.50V:	15	38
Vcco25 2.50V:	0	1
Clocks:	0	0
Inputs:	0	0
Logic:	0	0
Outputs:		
Vcco25	0	1
Signals:	0	0

Quiescent Vccint 1.20V:	15	19
Quiescent Vccaux 2.50V:	15	38

Thermal summary:	
Estimated junction temperature:	27C
Ambient temp:	25C
Case temp:	27C
Theta J-A range:	35 - 35C/W

Decoupling Network Summary:	Cap Range (uF)	#
Capacitor Recommendations:		
Total for Vccint		4
	470.0-1000.0	1
	0.0100-0.0470	1
	0.0010-0.0047	2
Total for Vccaux		8
	470.0-1000.0	1
	0.0470-0.2200	1
	0.0100-0.0470	2
	0.0010-0.0047	4
Total for Vcco25		8
	470.0-1000.0	1
	0.0470-0.2200	1
	0.0100-0.0470	2
	0.0010-0.0047	4

Analysis completed: Mon Nov 15 21:02:10 2010

For a General Battery with a capacity of 1000mA Hours, the battery would last for about 32.45 hours.

6. Working

Generating different frequencies' clock:

FPGA provides 4 MHz clock by default. to achieve 1 Hz clock we are taking 22 bit register which can go upto 4194304 value which is approximately 4000000. The 22nd bit of this register toggles its value at every .5 second and has frequency of 1HZ.

For getting 1 KHz frequency we take the 12th bit of the register which toggles after every .5 ms.

Working of digital clock:

- We are taking four variable seg3 to seg-0 (from MSB to LSB).
- At every one second we just increment the value of seg-0. When seg-0 reach at 9 it makes seg-1 to increment by 1 and reset its own value to 0.
- When seg-0 reaches at 9 and seg-1 reaches at 5 we make seg-2 incremented by 1 and reset both seg-0 1nd seg-1 to 0. (This is because every minute have 60 seconds.)
- When seg-2 reaches at 9 and also sed-1 and seg-0 at 5 and 9 respectively then seg-3 get incremented by 1.
- After every 60 minutes clock starts counting again from 0 second.
- There is a set alarm button given to make clock start from the beginning at any point of time.

Seven segment display algorithm:

We are assigning the variables seg-3 - seg-0 to four seven-segment LEDs and then at 1 KHz frequency we show LEDs one by one
in order to make it look continuous.

Alarm:

Total 12 input ports have been used in this to set alarm. Six ports to set seconds and other six to set minutes. After setting values on this input port by pressing set key we are fixing the alarm value in order to make it activated. Now at every second the logic will check whether the set value matches with the current time of the digital clock. When match happens an LED will become on and the speaker starts generating volume of two different frequencies.

Speaker:

When the alarm match take place, a variable starts toggling at the desired frequency rate for 0.5 second and for other 0.5 second that same variable changes its toggling frequency to some other value. By this we get two different values of frequency and it sounds like a beep or siren. It goes on until we press resetalarm button.

7. Appendix

7.1 Verilog Code

```
`timescale 1ns / 1ps
////////////////////////////////////////////////////////////////////////////////
// Company: 
// Engineer: 
// 
// Create Date:    16:55:38 11/15/2010 
// Design Name: 
// Module Name:    alarm 
// Project Name: 
// Target Devices: 
// Tool versions: 
// Description: 
//
// Dependencies: 
//
// Revision: 
// Revision 0.01 - File Created
// Additional Comments: 
//
////////////////////////////////////////////////////////////////////////////////
module alarm(input clkip ,input [5:0] alarmsec ,input [5:0] alarmmin ,input set ,input
rst ,input alarmrst ,output  reg [6:0]display,output reg [3:0]cs=4'b0001 ,output reg
alarm = 0 ,output reg speaker = 0);

reg [21:0] clkreg = 0;
wire clkone = clkreg[21];
wire clk1kay =  clkreg[11];

reg [5:0]min,sec;
reg [5:0]amin,asec;
wire [3:0]predisplay;
parameter clkdivider = 4000000/440/2;

reg [3:0] seg1 = 0,seg2=0 ,seg3=0,seg0 = 0;
```

```
assign predisplay = (~cs[3]&&~cs[2]&&~cs[1]&&cs[0])?
seg0:(~cs[3]&&~cs[2]&&cs[1]&&~cs[0])?seg1:(~cs[3]&&cs[2]&&~cs[1]&&~cs[0])?se
g2:seg3;

reg [14:0] counter;
always @(posedge clkip) if(counter==0) counter <= (clkreg[21] ? clkdivider-1 :
clkdivider/2-1); else counter <= counter-1;

always @(posedge clkip)
begin
 if(alarm == 0)
 speaker <=0 ;
 else if(counter==0) speaker <= ~speaker;
end



always@(posedge set)
begin
amin = alarmmin;
asec = alarmsec;
end

always @ (posedge clkip)
begin
clkreg = clkreg + 1'b1;
end





//every one second
always @ (posedge clkone )
begin
        min = seg3*4'b1010 + seg2;
        sec = seg1*4'b1010 + seg0 + 1;

        if(alarm == 0 && min == amin && sec == asec)
        begin
        alarm = 1;

        end
        if(rst == 0)begin seg0 = 0; seg1 = 0; seg2 = 0;seg3 = 0;end

        if(alarmrst == 0) begin alarm = 0; end


        if(seg3 == 5 && seg2 == 9 && seg0 == 9 && seg1 == 5)
        begin
                seg3 = 0;
                seg2 = 0;
                seg1 = 0;
                seg0 = 0;
        end


        else if(seg2 == 9&&seg0 == 9 && seg1 == 5)
        begin
                seg3 = seg3 + 1;
                seg2 = 0;
                seg1 = 0;
                seg0 = 0;
        end

        else if(seg0 == 9 && seg1 == 5)
        begin
                seg2 = seg2 + 1;
                seg1 = 0;
                seg0 = 0;
        end

        else if(seg0 == 9)
        begin
                seg1 = seg1+1;
                seg0 = 0;
        end

        else seg0  = seg0+1;

end

// for the seven segment display
```

```
always @ (posedge clk1kay)
begin
                cs = {cs[2],cs[1],cs[0],cs[3]};
        case(predisplay)

                4'b0000: display = 7'b1111110;
                4'b0001: display = 7'b0110000;
                4'b0010: display = 7'b1101101;
                4'b0011: display = 7'b1111001;
                4'b0100: display = 7'b0110011;
                4'b0101: display = 7'b1011011;
                4'b0110: display = 7'b1011111;
                4'b0111: display = 7'b1110000;
                4'b1000: display = 7'b1111111;
                4'b1001: display = 7'b1110011;
                default: display = 7'b0000000;
        endcase
end
endmodule
```

7.2 Synthesis Report

```

=========================================================================
*                      Synthesis Options Summary                      *
=========================================================================
---- Source Parameters
Input File Name                    : "alarm.prj"
Input Format                       : mixed
Ignore Synthesis Constraint File   : NO

---- Target Parameters
Output File Name                   : "alarm"
Output Format                      : NGC
Target Device                      : xc3s400-4-pq208

---- Source Options
Top Module Name                    : alarm
Automatic FSM Extraction           : YES
FSM Encoding Algorithm             : Auto
FSM Style                          : lut
RAM Extraction                     : Yes
RAM Style                          : Auto
ROM Extraction                     : Yes
Mux Style                          : Auto
Decoder Extraction                 : YES
Priority Encoder Extraction        : YES
Shift Register Extraction          : YES
Logical Shifter Extraction         : YES
XOR Collapsing                     : YES
ROM Style                          : Auto
Mux Extraction                     : YES
Resource Sharing                   : YES
Multiplier Style                   : auto
Automatic Register Balancing       : No

---- Target Options
Add IO Buffers                     : YES
Global Maximum Fanout              : 500
Add Generic Clock Buffer(BUFG)     : 8
Register Duplication               : YES
Slice Packing                      : YES
Pack IO Registers into IOBs        : auto
Equivalent register Removal        : YES

---- General Options
Optimization Goal                  : Speed
Optimization Effort                : 1
```

```
Keep Hierarchy                     : NO
RTL Output                         : Yes
Global Optimization                : AllClockNets
Write Timing Constraints           : NO
Hierarchy Separator                : /
Bus Delimiter                      : <>
Case Specifier                     : maintain
Slice Utilization Ratio            : 100
Slice Utilization Ratio Delta      : 5

---- Other Options
lso                                : alarm.lso
Read Cores                         : YES
cross_clock_analysis               : NO
verilog2001                        : YES
safe_implementation                : No
Optimize Instantiated Primitives   : NO
use_clock_enable                   : Yes
use_sync_set                       : Yes
use_sync_reset                     : Yes

================================================================================


================================================================================
*                          HDL Compilation                          *
================================================================================
Compiling verilog file "../../alarm_clock/alarm.v" in library work
Module <alarm> compiled
No errors in compilation
Analysis of file <"alarm.prj"> succeeded.


================================================================================
*                     Design Hierarchy Analysis                     *
================================================================================
Analyzing hierarchy for module <alarm> in library <work> with parameters.
	clkdivider = "00000000000000000001000111000001"

Building hierarchy successfully finished.

================================================================================
*                            HDL Analysis                           *
================================================================================
Design Repository: return true for module <alarm>
Analyzing top module <alarm>.
	clkdivider = 32'sb00000000000000000001000111000001
Module <alarm> is correct for synthesis.
 
```

```

=========================================================================
*                          HDL Synthesis                              *
=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <alarm>.
    Related source file is "../../alarm_clock/alarm.v".
WARNING:Xst:646 - Signal <min> is assigned but never used.
WARNING:Xst:646 - Signal <sec> is assigned but never used.
WARNING:Xst:643 - "../../alarm_clock/alarm.v" line 84: The result of a 4x4-bit multiplication is partially used. Only the 6 least significant bits are used. If you are doing this on purpose, you may safely ignore this warning. Otherwise, make sure you are not losing information, leading to unexpected circuit behavior.
WARNING:Xst:643 - "../../alarm_clock/alarm.v" line 85: The result of a 4x4-bit multiplication is partially used. Only the 6 least significant bits are used. If you are doing this on purpose, you may safely ignore this warning. Otherwise, make sure you are not losing information, leading to unexpected circuit behavior.
    Found 16x7-bit ROM for signal <$mux0004> created at line 136.
    Found 4-bit register for signal <cs>.
    Found 1-bit register for signal <speaker>.
    Found 1-bit register for signal <alarm>.
    Found 7-bit register for signal <display>.
    Found 4-bit adder for signal <$add0000> created at line 128.
    Found 4-bit adder for signal <$addsub0000> created at line 124.
    Found 4-bit adder for signal <$addsub0001> created at line 117.
    Found 4-bit adder for signal <$addsub0002> created at line 109.
    Found 6-bit comparator equal for signal <$cmp_eq0001> created at line 87.
    Found 6-bit comparator equal for signal <$cmp_eq0002> created at line 87.
    Found 4x4-bit multiplier for signal <$mult0004> created at line 84.
    Found 4x4-bit multiplier for signal <$mult0005> created at line 85.
    Found 6-bit adder for signal <$old_min_1>.
    Found 6-bit adder for signal <$old_sec_2>.
    Found 6-bit register for signal <amin>.
    Found 6-bit register for signal <asec>.
    Found 22-bit up counter for signal <clkreg>.
    Found 15-bit down counter for signal <counter>.
    Found 4-bit register for signal <seg0>.
    Found 4-bit register for signal <seg1>.
    Found 4-bit register for signal <seg2>.
    Found 4-bit register for signal <seg3>.
    Summary:
        inferred   1 ROM(s).
        inferred   2 Counter(s).
        inferred  41 D-type flip-flop(s).
        inferred   6 Adder/Subtractor(s).
        inferred   2 Multiplier(s).
        inferred   2 Comparator(s).
Unit <alarm> synthesized.

```

```

=========================================================================
HDL Synthesis Report

Macro Statistics
# ROMs                                                 : 1
 16x7-bit ROM                                          : 1
# Multipliers                                          : 2
 4x4-bit multiplier                                    : 2
# Adders/Subtractors                                   : 6
 4-bit adder                                           : 4
 6-bit adder                                           : 2
# Counters                                             : 2
 15-bit down counter                                   : 1
 22-bit up counter                                     : 1
# Registers                                            : 10
 1-bit register                                        : 2
 4-bit register                                        : 5
 6-bit register                                        : 2
 7-bit register                                        : 1
# Comparators                                          : 2
 6-bit comparator equal                                : 2

=========================================================================

=========================================================================
*                       Advanced HDL Synthesis                          *
=========================================================================

Loading device for application Rf_Device from file '3s400.nph' in environment H:\Xilinx.
INFO:Xst:1647 - Data output of ROM <Mrom__mux0004> is tied to register <display>.
INFO:Xst:2506 - In order to maximize performance and save block RAM resources, this small ROM will be implemented on LUT. If you want to force its implementation on block, use option/constraint rom_style.

```

```
===============================================================================
Advanced HDL Synthesis Report

Macro Statistics
# ROMs                                 : 1
 16x7-bit ROM                          : 1
# Multipliers                          : 2
 4x4-bit multiplier                    : 2
# Adders/Subtractors                   : 6
 4-bit adder                           : 4
 6-bit adder                           : 2
# Counters                             : 2
 15-bit down counter                   : 1
 22-bit up counter                     : 1
# Registers                            : 41
 Flip-Flops                            : 41
# Comparators                          : 2
 6-bit comparator equal                : 2

===============================================================================

===============================================================================
*                          Low Level Synthesis                          *
===============================================================================

Optimizing unit <alarm> ...

Mapping all equations...
Building and optimizing final netlist ...
Found area constraint ratio of 100 (+ 5) on block alarm, actual ratio is 2.

Final Macro Processing ...

===============================================================================
Final Register Report

Macro Statistics
# Registers                            : 78
 Flip-Flops                            : 78

===============================================================================

===============================================================================
*                    Partition Report                    *
=========================================================================

Partition Implementation Status
-------------------------------

  Preserved Partitions:


  Implemented Partitions:

    Partition "/alarm":
There was no implementation for this Partition.

-------------------------------


Partition NGC Files
-------------------------------

    Partition "/alarm":
      NGC File: alarm.ngc

-------------------------------

=========================================================================
*                     Final Report                     *
=========================================================================
Final Results
RTL Top Level Output File Name     : alarm.ngr
Top Level Output File Name         : alarm
Output Format                      : NGC
Optimization Goal                  : Speed
Keep Hierarchy                     : NO

Design Statistics
# IOs                              : 29

Cell Usage :
# BELS                             : 227
#      GND                         : 1
#      INV                         : 18
#      LUT1                        : 22
#      LUT2                        : 17
#      LUT2_D                      : 1
#      LUT3                        : 22
#      LUT3_D                      : 3
#      LUT3_L                      : 2
#      LUT4                        : 49
#      LUT4_D                      : 8
#      LUT4_L                      : 8
#      MUXCY                       : 35
#      MUXF5                       : 4
#      VCC                         : 1
#      XORCY                       : 36
# FlipFlops/Latches                : 78
#      FD                          : 57
#      FDR                         : 17
#      FDRE                        : 2
#      FDS                         : 2
# Clock Buffers                    : 2
#      BUFGP                       : 2
# IO Buffers                       : 27
#      IBUF                        : 14
#      OBUF                        : 13
=========================================================================

Device utilization summary:
---------------------------

Selected Device : 3s400pq208-4

 Number of Slices:                      78  out of   3584     2%
 Number of Slice Flip Flops:            66  out of   7168     0%
 Number of 4 input LUTs:               150  out of   7168     2%
 Number of IOs:                         29
 Number of bonded IOBs:                 29  out of    141    20%
    IOB Flip Flops:                     12
 Number of GCLKs:                        2  out of      8    25%


=========================================================================
TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.
      FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT
      GENERATED AFTER PLACE-and-ROUTE.

Clock Information:
------------------
-----------------------------------+------------------------+-------+
Clock Signal                       | Clock buffer(FF name)  | Load  |
-----------------------------------+------------------------+-------+
set                                | BUFGP                  | 12    |
clkreg_21                          | NONE(seg1_2)           | 17    |
clkreg_11                          | NONE(cs_1)             | 11    |
clkip                              | BUFGP                  | 38    |
-----------------------------------+------------------------+-------+
INFO:Xst:2169 - HDL ADVISOR - Some clock signals were not automatically buffered by XST with BUFG/BUFR resources. Please use the buffer_type constraint in order to insert these buffers to the clock signals to help prevent skew problems.

Asynchronous Control Signals Information:
----------------------------------------
No asynchronous control signals found in this design

Timing Summary:
---------------
Speed Grade: -4

   Minimum period: 8.938ns (Maximum Frequency: 111.882MHz)
   Minimum input arrival time before clock: 8.421ns
   Maximum output required time after clock: 7.367ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)

=========================================================================
Timing constraint: Default period analysis for Clock 'clkreg_21'
  Clock period: 8.938ns (frequency: 111.882MHz)
  Total number of paths / destination ports: 407 / 33
-------------------------------------------------------------------------
Delay:               8.938ns (Levels of Logic = 5)
  Source:            seg1_0 (FF)
  Destination:       alarm (FF)
  Source Clock:      clkreg_21 rising
  Destination Clock: clkreg_21 rising

  Data Path: seg1_0 to alarm
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDR:C->Q             16   0.720   1.432  seg1_0 (seg1_0)
     LUT3:I1->O            1   0.551   0.000  Madd__old_sec_2_cy<2>11_SW1_F (N384)
     MUXF5:I0->O           1   0.360   0.996  Madd__old_sec_2_cy<2>11_SW1 (N377)
     LUT3_D:I1->O          1   0.551   0.827  Madd__old_sec_2_cy<3>11 (Madd__old_sec_2_cy<3>)
     LUT4:I3->O            1   0.551   0.996  _and000017 (_and0000_map51)
     LUT4:I1->O            1   0.551   0.801  _and0000234 (_and0000)
     FDRE:CE                   0.602          alarm
    ----------------------------------------
    Total                      8.938ns (3.886ns logic, 5.052ns route)
                                       (43.5% logic, 56.5% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'clkreg_11'
```

```
  Clock period: 7.813ns (frequency: 127.992MHz)
  Total number of paths / destination ports: 452 / 12
-------------------------------------------------------------------------
Delay:               7.813ns (Levels of Logic = 4)
  Source:            cs_2 (FF)
  Destination:       display_0 (FF)
  Source Clock:      clkreg_11 rising
  Destination Clock: clkreg_11 rising

  Data Path: cs_2 to display_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               6   0.720   1.342  cs_2 (cs_2)
     LUT4:I0->O            4   0.551   0.943  predisplay<3>31 (N211)
     LUT4:I3->O            1   0.551   0.996  predisplay<2>9 (predisplay<2>_map19)
     LUT2:I1->O            7   0.551   1.405  predisplay<2>10 (predisplay<2>)
     LUT4:I0->O            1   0.551   0.000  Mrom__mux00046 (N7)
     FD:D                      0.203          display_5
    ----------------------------------------
    Total                      7.813ns (3.127ns logic, 4.686ns route)
                                       (40.0% logic, 60.0% route)

=========================================================================
Timing constraint: Default period analysis for Clock 'clkip'
  Clock period: 6.473ns (frequency: 154.488MHz)
  Total number of paths / destination ports: 622 / 41
-------------------------------------------------------------------------
Delay:               6.473ns (Levels of Logic = 17)
  Source:            counter_0 (FF)
  Destination:       counter_14 (FF)
  Source Clock:      clkip rising
  Destination Clock: clkip rising

  Data Path: counter_0 to counter_14
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FD:C->Q               2   0.720   1.216  counter_0 (counter_0)
     LUT1:I0->O            1   0.551   0.000  counter_0_rt (counter_0_rt)
     MUXCY:S->O            1   0.500   0.000  Mcount_counter_cy<0> (Mcount_counter_cy<0>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<1> (Mcount_counter_cy<1>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<2> (Mcount_counter_cy<2>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<3> (Mcount_counter_cy<3>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<4> (Mcount_counter_cy<4>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<5> (Mcount_counter_cy<5>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<6> (Mcount_counter_cy<6>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<7> (Mcount_counter_cy<7>)
     MUXCY:CI->O           1   0.064   0.000  Mcount_counter_cy<8> (Mcount_counter_cy<8>)
     MUXCY:CI->O         1   0.064   0.000  Mcount_counter_cy<9> (Mcount_counter_cy<9>)
     MUXCY:CI->O         1   0.064   0.000  Mcount_counter_cy<10> (Mcount_counter_cy<10>)
     MUXCY:CI->O         1   0.064   0.000  Mcount_counter_cy<11> (Mcount_counter_cy<11>)
     MUXCY:CI->O         1   0.064   0.000  Mcount_counter_cy<12> (Mcount_counter_cy<12>)
     MUXCY:CI->O         0   0.064   0.000  Mcount_counter_cy<13> (Mcount_counter_cy<13>)
     XORCY:CI->O         1   0.904   0.996  Mcount_counter_xor<14> (Result<14>1)
     LUT2:I1->O          1   0.551   0.000  counter_Eqn_141 (counter_Eqn_14)
     FD:D                    0.203          counter_14
    ----------------------------------------
    Total                    6.473ns (4.261ns logic, 2.212ns route)
                                       (65.8% logic, 34.2% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'set'
  Total number of paths / destination ports: 12 / 12
-------------------------------------------------------------------------
Offset:              1.825ns (Levels of Logic = 1)
  Source:            alarmmin<0> (PAD)
  Destination:       amin_0 (FF)
  Destination Clock: set rising

  Data Path: alarmmin<0> to amin_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O           1   0.821   0.801  alarmmin_0_IBUF (alarmmin_0_IBUF)
     FD:D                    0.203          amin_0
    ----------------------------------------
    Total                    1.825ns (1.024ns logic, 0.801ns route)
                                       (56.1% logic, 43.9% route)

=========================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clkreg_21'
  Total number of paths / destination ports: 110 / 33
-------------------------------------------------------------------------
Offset:              8.421ns (Levels of Logic = 4)
  Source:            rst (PAD)
  Destination:       seg3_0 (FF)
  Destination Clock: clkreg_21 rising

  Data Path: rst to seg3_0
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O          30   0.821   2.181  rst_IBUF (rst_IBUF)
     LUT3:I0->O          1   0.551   0.827  _and000111_SW0_SW1 (N380)
     LUT4_D:I3->O        1   0.551   0.996  _and000111_SW0 (N363)
     LUT4:I1->O          4   0.551   0.917  _and0001 (_and0001)
     FDR:R                   1.026          seg3_2
  ---------------------------------------
  Total                     8.421ns (3.500ns logic, 4.921ns route)
                                  (41.6% logic, 58.4% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clkip'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              7.241ns (Levels of Logic = 1)
  Source:            speaker (FF)
  Destination:       speaker (PAD)
  Source Clock:      clkip rising

  Data Path: speaker to speaker
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             2   0.720   0.877  speaker (speaker_OBUF)
     OBUF:I->O                 5.644          speaker_OBUF (speaker)
    ----------------------------------------
    Total                     7.241ns (6.364ns logic, 0.877ns route)
                                  (87.9% logic, 12.1% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clkreg_21'
  Total number of paths / destination ports: 1 / 1
-------------------------------------------------------------------------
Offset:              7.271ns (Levels of Logic = 1)
  Source:            alarm (FF)
  Destination:       alarm (PAD)
  Source Clock:      clkreg_21 rising

  Data Path: alarm to alarm
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     FDRE:C->Q             3   0.720   0.907  alarm (alarm_OBUF)
     OBUF:I->O                 5.644          alarm_OBUF (alarm)
    ----------------------------------------
    Total                     7.271ns (6.364ns logic, 0.907ns route)
                                  (87.5% logic, 12.5% route)

=========================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clkreg_11'
  Total number of paths / destination ports: 11 / 11
-------------------------------------------------------------------------
Offset:              7.367ns (Levels of Logic = 1)
  Source:            cs_3 (FF)
  Destination:       cs<3> (PAD)
```

```
 Source Clock:      clkreg_11 rising

 Data Path: cs_3 to cs<3>
                          Gate     Net
   Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
   ----------------------------------------  ------------
    FD:C->Q               6   0.720   1.003  cs_3 (cs_3)
    OBUF:I->O                 5.644          cs_3_OBUF (cs<3>)
   ----------------------------------------
   Total                      7.367ns (6.364ns logic, 1.003ns route)
                                       (86.4% logic, 13.6% route)

=========================================================================
CPU : 13.66 / 14.15 s | Elapsed : 14.00 / 14.00 s

-->

Total memory usage is 186816 kilobytes

Number of errors   :    0 (   0 filtered)
Number of warnings :    4 (   0 filtered)
Number of infos    :    3 (   0 filtered)
```

7.3 Post Synthesis Report

```
Release 8.2i - netgen I.31
Copyright (c) 1995-2006 Xilinx, Inc.  All rights reserved.

Command Line: netgen -intstyle ise -insert_glbl true -w -dir netgen/synthesis
-ofmt verilog -sim alarm.ngc _synthesis.v

Reading design 'alarm.ngc' ...
Flattening design ...
Processing design ...
  Preping design's networks ...
  Preping design's macros ...
Writing Verilog netlist file 'H:\Treasure\Interns &
Projects\EHD\FPGA\code\alarm2\alarm\netgen\synthesis\_synthesis.v' ...
INFO:NetListWriters:633 - The generated Verilog netlist contains Xilinx UNISIM
   simulation primitives and has to be used with UNISIM simulation library for
   correct compilation and simulation.
Number of warnings: 0
Number of info messages: 1
Total memory usage is 94780 kilobytes
```

7.4 Map Report

```
Release 8.2i Map I.31
Xilinx Mapping Report File for Design 'alarm'

Design Information
------------------
Command Line   : H:\Xilinx\bin\nt\map.exe -ise H:/Treasure/Interns &
Projects/EHD/FPGA/code/alarm_new/alarm_new.ise -intstyle ise -p xc3s400-pq208-
4
-cm area -pr b -k 4 -c 100 -o alarm_map.ncd alarm.ngd alarm.pcf
Target Device  : xc3s400
Target Package : pq208
Target Speed   : -4
Mapper Version : spartan3 -- $Revision: 1.34.32.1 $
Mapped Date    : Mon Nov 15 17:03:17 2010

Design Summary
--------------
Number of errors:      0
Number of warnings:    0
Logic Utilization:
  Number of Slice Flip Flops:          59 out of   7,168    1%
  Number of 4 input LUTs:             119 out of   7,168    1%
Logic Distribution:
  Number of occupied Slices:                       78 out of   3,584    2%
  Number of Slices containing only related logic:      78 out of      78  100%
   Number of Slices containing unrelated logic:         0 out of      78    0%
  *See NOTES below for an explanation of the effects of unrelated logic
Total Number 4 input LUTs:            141 out of   7,168    1%
  Number used as logic:              119
  Number used as a route-thru:         22
  Number of bonded IOBs:               29 out of     141   20%
  IOB Flip Flops:                  19
  Number of GCLKs:                     2 out of       8   25%
```

7.5 Floor and Route report

```
Release 8.2i par I.31
Copyright (c) 1995-2006 Xilinx, Inc.  All rights reserved.

YASH-PC::  Mon Nov 15 17:03:22 2010

par -w -intstyle ise -ol std -t 1 alarm_map.ncd alarm.ncd alarm.pcf


Constraints file: alarm.pcf.
Loading device for application Rf_Device from file '3s400.nph' in environment H:\Xilinx.
   "alarm" is an NCD, version 3.1, device xc3s400, package pq208, speed -4

Initializing temperature to 85.000 Celsius. (default - Range: 0.000 to 85.000 Celsius)
Initializing voltage to 1.140 Volts. (default - Range: 1.140 to 1.260 Volts)

INFO:Par:282 - No user timing constraints were detected or you have set the option to
ignore timing constraints ("par
   -x"). Place and Route will run in "Performance Evaluation Mode" to automatically
improve the performance of all
   internal clocks in this design. The PAR timing summary will list the performance
achieved for each clock. Note: For
   the fastest runtime, set the effort level to "std".  For best performance, set the effort
level to "high". For a
   balance between the fastest runtime and best performance, set the effort level to
"med".

Device speed data version:  "PRODUCTION 1.38 2006-05-03".


Device Utilization Summary:

   Number of BUFGMUXs                 2 out of 8      25%
   Number of External IOBs           29 out of 141    20%
      Number of LOCed IOBs            0 out of 29      0%

   Number of Slices                  78 out of 3584    2%
      Number of SLICEMs               0 out of 1792    0%
```

7.6 Static Timing report

```
--------------------------------------------------------------------------------
Release 8.2i Trace
Copyright (c) 1995-2006 Xilinx, Inc.  All rights reserved.

H:\Xilinx\bin\nt\trce.exe -ise
H:/Treasure/Interns & Projects/EHD/FPGA/code/alarm_new/alarm_new.ise -
intstyle
ise -e 3 -l 3 -s 4 -xml alarm alarm.ncd -o alarm.twr alarm.pcf -ucf alarm.ucf

Design file:              alarm.ncd
Physical constraint file: alarm.pcf
Device,speed:             xc3s400,-4 (PRODUCTION 1.38 2006-05-03)
Report level:             error report

Environment Variable      Effect 
--------------------      ------ 
NONE                      No environment variables were set
--------------------------------------------------------------------------------

INFO:Timing:2698 - No timing constraints found, doing default enumeration.
INFO:Timing:2752 - To get complete path coverage, use the unconstrained paths 
   option. All paths that are not constrained will be reported in the 
   unconstrained paths section(s) of the report.



Data Sheet report:
-----------------
All values displayed in nanoseconds (ns)

Setup/Hold to clock set
------------+------------+------------+------------------+--------+
            | Setup to   |  Hold to   |                  | Clock  |
Source      | clk (edge) | clk (edge) |Internal Clock(s) | Phase  |
------------+------------+------------+------------------+--------+
alarmmin<0> |    2.852(R)|   -0.323(R)|set_BUFGP         |   0.000|
alarmmin<1> |    2.868(R)|   -0.342(R)|set_BUFGP         |   0.000|
alarmmin<2> |    2.852(R)|   -0.323(R)|set_BUFGP         |   0.000|
alarmmin<3> |    2.868(R)|   -0.342(R)|set_BUFGP         |   0.000|
alarmmin<4> |    2.868(R)|   -0.342(R)|set_BUFGP         |   0.000|
alarmmin<5> |    2.868(R)|   -0.342(R)|set_BUFGP        |   0.000|
alarmsec<0> |    2.852(R)|   -0.323(R)|set_BUFGP        |   0.000|
alarmsec<1> |    2.852(R)|   -0.323(R)|set_BUFGP        |   0.000|
alarmsec<2> |    2.868(R)|   -0.342(R)|set_BUFGP        |   0.000|
alarmsec<3> |    2.868(R)|   -0.342(R)|set_BUFGP        |   0.000|
alarmsec<4> |    2.852(R)|   -0.323(R)|set_BUFGP        |   0.000|
alarmsec<5> |    2.868(R)|   -0.342(R)|set_BUFGP        |   0.000|
------------+------------+------------+------------------+--------+

Clock clkip to Pad
------------+------------+------------------+--------+
            | clk (edge) |                  | Clock  |
Destination |   to PAD   |Internal Clock(s) | Phase  |
------------+------------+------------------+--------+
speaker     |    8.426(R)|clkip_BUFGP       |   0.000|
------------+------------+------------------+--------+

Clock to Setup on destination clock clkip
---------------+---------+---------+---------+---------+
               | Src:Rise| Src:Fall| Src:Rise| Src:Fall|
Source Clock   |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|
---------------+---------+---------+---------+---------+
clkip          |    5.610|         |         |         |
---------------+---------+---------+---------+---------+


Analysis completed Mon Nov 15 17:03:34 2010
--------------------------------------------------------------------------------

Trace Settings:
-------------------------
Trace Settings
```

Peak Memory Usage: 146 MB