Assignment-7 (Report)

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Below we have mentioned the following modules that will be executed in a sequential manner:

1> Main_Controller_test_bench.v

➔ Here, our main top module named “Main_Controller.v” will be called and executed with respect to the given initial parameters like: clk, reset.

2> Main_Controller.v

➔ Here, we did the whole computation related work like fetching, decoding.

Then, we use some modules like ALU, Branch, Store_Load modules and stored the result (if the instruction was arithmetic) or stored the data in registers (if the instruction was load word) or stored the incremented (new PC) in Next_PC (if the instruction is Branching).

Finally, we check the Mode (type of instruction) and accordingly performed the corresponding computation.

3> Fetch.v

➔ Here, we used one bin file for instruction and fetch the required instruction using the provided or updated PC.

4> Decode.v

➔ Here, we used the fetched instruction to decode the instruction and updated the opcode value of ALU, Branch, Data as per the instruction using its opcode and func value.

5> ALU.v

➔ Here, we did all the ALU computation like add, sub etc using Opcode_ALU value. And store the result.

6> Branch.v

➔ Here, we did all the Branching operations like bne, beq etc using the opcode_Branch value and stores the Next_PC value.

7> Store_Load.v

➔ Here, we did all the load and store operations (Data memory related operations) using the opcode_Data value and stores the value in Data_Memory and used the same Data_Memory for loading the value into register.

Finally, after all these operations, we update PC value as per the mode (R-type, I-type, jr, Store, Load). After every negedge, above steps would be executed and whole process would end after #10000.