

# CppMem: Atomics with Sequential Consistency

This lesson gives an overview of atomics with sequential consistency used in the context of CppMem.

## WE'LL COVER THE FOLLOWING

- CppMem
  - Execution for (y = 0, x = 0)
  - Executions for (y = 0, x = 2000)
  - Execution for (y = 11, x = 2000)
- Sequence of Instructions
- Cases:

If you don't specify the memory model, [sequential consistency](#) will be applied. Sequential consistency guarantees two properties: each thread executes its instructions in source code order, and all threads follow the same global order. Here is the optimized version of the program using atomics.

```
// ongoingOptimisationSequentialConsistency.cpp
```

```
#include <atomic>
#include <iostream>
#include <thread>

std::atomic<int> x{0};
std::atomic<int> y{0};

void writing(){
    x.store(2000);
    y.store(11);
}

void reading(){
    std::cout << y.load() << " ";
    std::cout << x.load() << std::endl;
}
```

```
int main(){
    std::thread thread1(writing);
    std::thread thread2(reading);
    thread1.join();
    thread2.join();
}
```



```
thread1.join();
thread2.join();
};
```



Let's analyze the program. The program is data race free because `x` and `y` are atomics. Therefore, only one question is left to answer: What values are possible for `x` and `y`? The question is easy to answer. Thanks to the sequential consistency, all threads have to follow the same global order.

It holds true:

- `x.store(2000);` **happens-before** `y.store(11);`
- `std::cout << y.load() << " ";` **happens-before** `std::cout << x.load() << std::endl;`

Hence the value of `x.load()` cannot be `0` if `y.load()` has the value `11`, because `x.store(2000)` happens before `y.store(11)`.

All other values for `x` and `y` are possible. Here are three possible interleavings resulting in the three different values for `x` and `y`.

1. `thread1` will be completely executed before `thread2`.
2. `thread2` will be completely executed before `thread1`.
3. `thread1` will execute its first instruction `x.store(2000)` before `thread2` will be completely executed.

Here are all the values for `x` and `y`.

y	x	Values possible?
0	0	Yes
11	0	
0	2000	Yes

Let me verify my reasoning with CppMem.

## CppMem #

Here is the corresponding program in CppMem.

```
int main(){
  atomic_int x = 0;
  atomic_int y = 0;
  {{{ {
    x.store(2000);
    y.store(11);
  }
  ||| {
    y.load();
    x.load();
  }
  }}}
}
```

First, a little bit of syntax. CppMem uses the `typedef atomic_int` for `std::atomic<int>` in lines 2 and 3. When I execute the program, I'm overwhelmed by the number of execution candidates.

**CppMem: Interactive C/C++ memory model** 2 **Execution candidate no. 24 of 384**

Model: ☒ standard ☒ preferred ☐ release\_acquire ☐ tot ☐ relaxed\_only

Program: examples/LB\_load\_buffering LB+acq rel+acq rel.c v

**Model Predicates**

- ☒ consistent\_race\_free\_execution = true
- ☒ consistent\_execution = true
- ☒ assumptions = true
- ☒ well\_formed\_threads = true
- ☒ well\_formed\_rf = true
- ☒ locks\_only\_consistent\_locks = true
- ☒ locks\_only\_consistent\_lo = true
- ☒ consistent\_mo = true
- ☒ sc\_accesses\_consistent\_sc = true
- ☒ sc\_fenced\_sc\_fences\_heeded = true
- ☒ consistent\_hb = true
- ☒ consistent\_rf = true
- ☒ det\_read = true
- ☒ consistent\_non\_atomic\_rf = true
- ☒ consistent\_atomic\_rf = true
- ☒ coherent\_memory\_use = true
- ☒ rmw\_atomicity = true
- ☒ sc\_accesses\_sc\_reads\_restricted = true
- ☒ unsequenced\_races are absent
- ☒ data\_races are absent
- ☒ indeterminate\_reads are absent
- ☒ locks\_only\_bad\_mutexes are absent

**Computed executions**

**Display Relations**

☒ sb ☐ asw ☐ dd ☐ cd

☒ rf ☐ mo ☒ sc ☒ lo

☐ hb ☐ vse ☐ lthb ☐ sw ☐ rs ☐ hrs ☒ dob ☐ cad

☒ unsequenced\_races ☒ data\_races

**Display Layout**

☐ dot ☐ neato par ☒ neato par Init ☐ neato downwards

**Execution Diagram:**

```

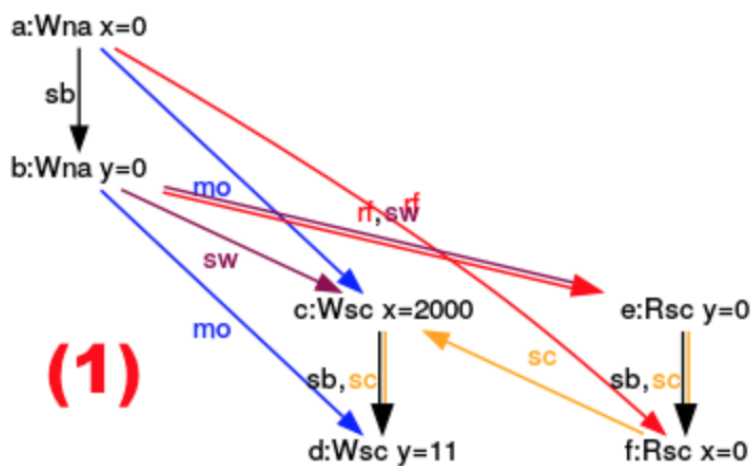
graph TD
    a["a:Wna x=0"] -- sb --> b["b:Wna y=0"]
    a -- "r1,6W" --> c["c:Wsc x=2000"]
    a -- "r1,6W" --> e["e:Rsc y=0"]
    b -- "mo" --> c
    b -- "sw" --> c
    b -- "mo" --> d["d:Wsc y=11"]
    c -- "sb,sc" --> d
    c -- "sc" --> f["f:Rsc x=0"]
    e -- "sb,sc" --> f
  
```

**1** reset help 384 executions; 6 consistent, all race free

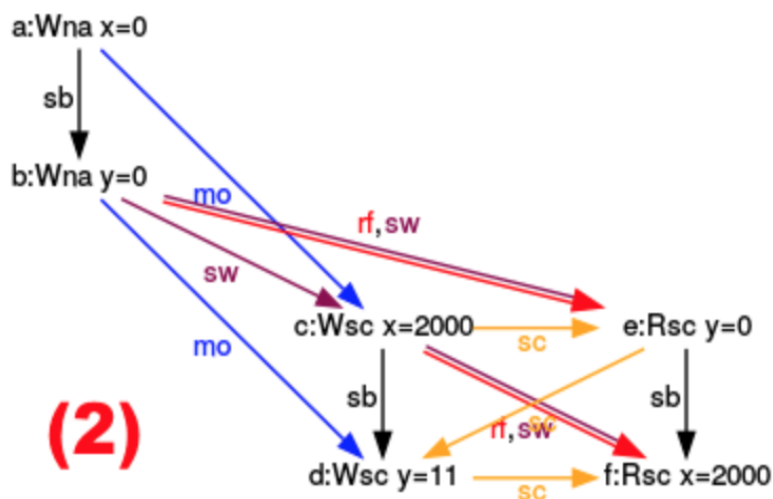
There are 384 **(1)** possible execution candidates, but only 6 of them are consistent; no candidate has a *data race*. I'm only interested in the 6 consistent executions and ignore the other 378 non-consistent executions. Non-consistent means, for example, that they will not respect the *modification order*. I use the interface **(2)** to get the six annotated graphs.

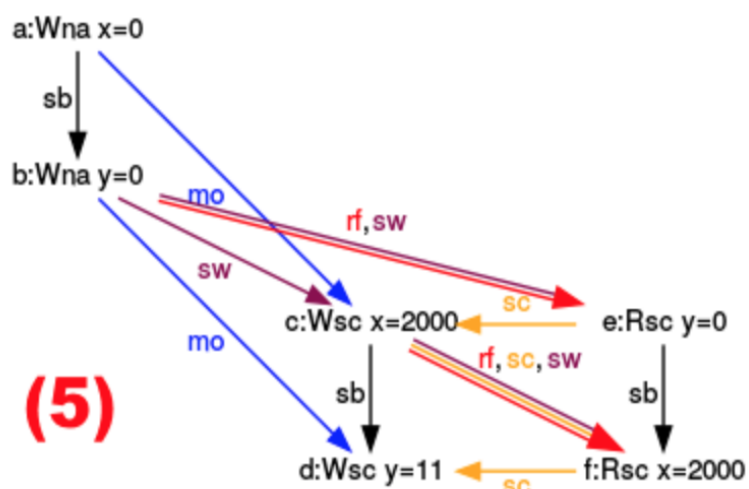
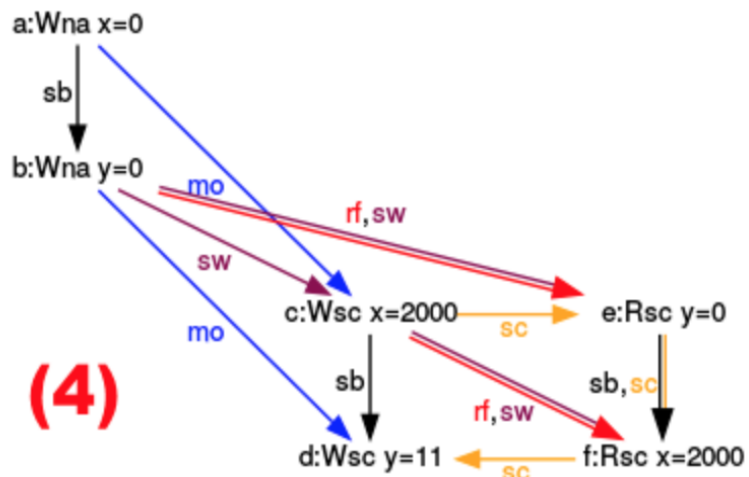
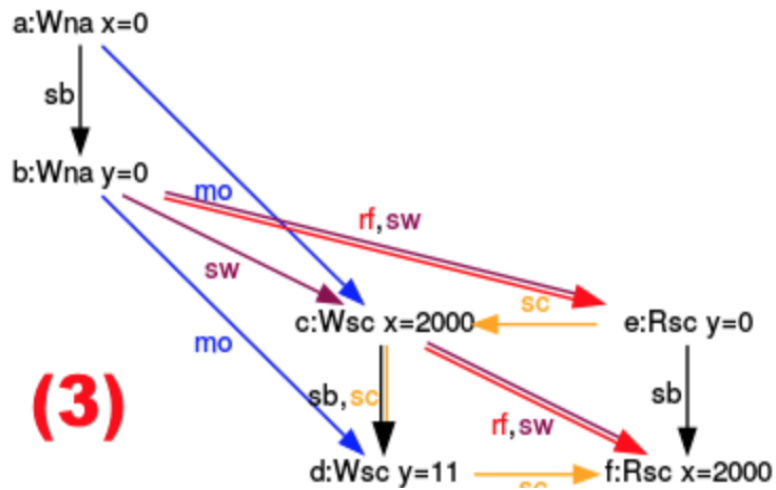
We already know that all values for  $x$  and  $y$  are possible except for  $y = 11$  and  $x = 0$ . This is because of the sequential consistency. Now I'm curious, which interleaving of threads will produce which values for  $x$  and  $y$ ?

Execution for ( $y = 0, x = 0$ ) #

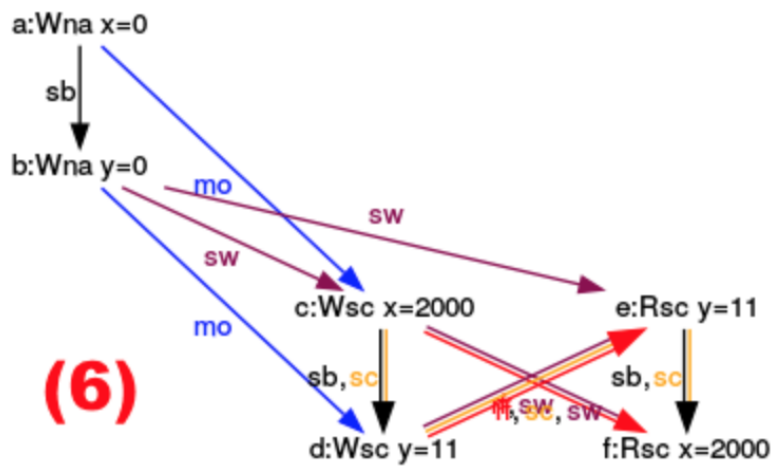


Executions for ( $y = 0, x = 2000$ ) #





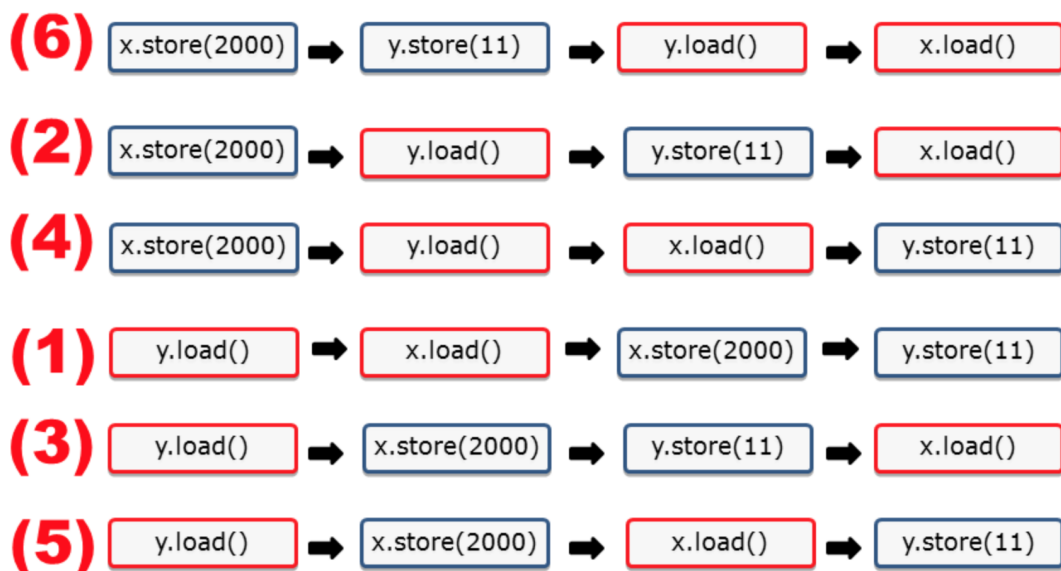
Execution for (y = 11, x = 2000) #



I'm not done with my analysis. I'm interested in which sequence of instructions corresponds to which of the six graphs.

## Sequence of Instructions #

I have assigned each graph to its corresponding sequence of instructions.



time

Cases: #

Let me start with the simpler cases.

- **(1):** It's quite simple to assign the graph (1) to the sequence (1). In the sequence (1) `x` and `y` have the values 0 because `y.load()` and `x.load()` are executed before the operations `x.store(2000)` and `y.store(11)`.
- **(6):** The reasoning for the execution (6) is similar. `y` has the value 11 and `x` the value 2000 because all load operations happen after all store operations.
- **(2), (3), (4), (5):** Now to the more interesting cases in which `y` has the value 0 and `x` has the value 2000. The yellow arrows (sc) in the graph are the key to my reasoning because they stand for the sequence of instructions. For example, let's look at execution (2).
  - **(2):** Here is the sequence of the yellow arrows (sc) in the graph (2):  
write `x = 2000` => read `y = 0` => write `y = 11` => read `x = 2000`.  
This sequence corresponds to the sequence of instructions of the second interleaving of threads (2).

Let's break the sequential consistency with the acquire-release semantic in the next lesson.