

Experimental investigation of Phase Change Materials for thermal management of handheld devices

Yash Ganatra^a, Javieradrian Ruiz^b, John A. Howarter^{c,d}, Amy Marconnet^{a,*}

^a School of Mechanical Engineering, Purdue University, 585 Purdue Mall, West Lafayette, IN, 47907, United States

^b School of Chemical Engineering, Purdue University, Forney Hall of Chemical Engineering, 480 Stadium Mall Drive, West Lafayette, IN, 47907, United States

^c School of Materials Engineering, Purdue University, Neil Armstrong Hall of Engineering, 701 West Stadium Avenue, West Lafayette, IN, 47907, United States

^d Division of Environmental & Ecological Engineering, Purdue University, Potter Engineering Center, 500 Central Drive, West Lafayette, IN 47907, United States

ARTICLE INFO

Keywords:

Electronics thermal management
Phase change material
Thermal energy storage

ABSTRACT

The trend of enhanced functionality and reducing size of mobile devices has led to a rapid increase in power density and a potential thermal bottleneck since thermal limits of components remain unchanged. Active cooling mechanisms are not feasible due to size, weight, and cost constraints. This work explores the feasibility of a passive cooling system based on Phase Change Materials (PCMs) for thermal management of mobile devices. The PCMs stabilize device temperatures due to the latent heat of phase change, thus increasing the operating time of the device before threshold temperatures are exceeded. The primary contribution of this work is the experimental evaluation of key parameters which influence the design of a PCM based thermal management system. *In situ* measurements with PCMs as a passive thermal management solution demonstrate that a significant extension in the time that the processor can run at full power before the processing power would need to be throttled to prevent damage.

1. Introduction

The development and rapid progress in computing over the last century ushered in an era of unprecedented scientific and technological advancements. The pervasive use of computers and other electronic devices is due, in part, to cost reduction and mobility brought about by the miniaturization of the circuit components, in accordance with the Moore's Law. To highlight the manifold growth in processing performance in the last 20 years, the peak performance (measured in floating point operations per second) of a Samsung Galaxy S6 smartphone (launched in 2015) is 5 times greater than a Sony Playstation 2 (launched in 2000), and the power density has in turn increased due to an increase in power dissipation coupled with a reduction in form factor. This results in an increase in processor temperatures which poses serious reliability concerns. Thermal issues have been long standing, and a 1989 survey by US Air Force [1] demonstrated that more than half the failures in electronic components were due to thermal issues. The thermal limits, which include the processor, Random access memory (RAM), Multi-Media card, and the surface (or skin) temperature of the device, remain unchanged. The maximum operating temperatures of electronic components range from 70 °C to 120 °C. The surface temperature of handheld consumer electronics is limited to 40 °C due to

ergonomic constraints [2].

Thermal Energy Storage (TES) systems for passive thermal management are promising due to their ability to absorb heat (during solid to liquid or liquid to vapor phase transitions), which dampens temperature fluctuations in response to power variations, thus reducing the susceptibility to thermal fatigue. Consequently, surface temperatures are maintained within ergonomic requirements. Phase change materials (PCMs) represent a type of TES system which exploits the latent heat of melting during the solid to liquid transition to dampen the temperature spikes, thus increasing the operating time of the device before the threshold safe operating temperatures are reached.

Over the past several decades, many different combinations of PCMs properties and configurations have been evaluated. For example, Amon et al. [3] experimentally studied the influence of adding foams or nanofibers to enhance the thermal conductivity of paraffin wax and found that the graphite nanofiber - PCM composite showed the greatest delay in the time to melt. However, at higher heat fluxes, the temperatures at the baseplate were as high as for pure paraffin wax. The graphite foam (with higher thermal conductivity) had the lowest baseplate temperatures at these heat fluxes. This study clearly indicated the importance of thermal conductivity in design of PCM infiltrated heat sinks.

* Corresponding author.

E-mail address: marconnet@purdue.edu (A. Marconnet).

Acronyms

DSC	Differential Scanning Calorimetry
GPU	Graphics Processing Unit
I/O	Input/Output
IR	Infrared

PCB	Printed Circuit Board.
PCM	Phase Change Material
RAM	Random access memory
SBC	Single Board Computer
TES	Thermal Energy Storage
TIM	Thermal Interface Material

Many applications in mobile devices require short bursts of high computational demand interspersed with periods of lower demand, therefore it is often effective to design for responsiveness rather than sustained performance. To ensure that the temperatures remain within prescribed limits, Shao et al. [4] integrated the PCM on the chip. Specifically, the PCM was filled in cavities etched on the opposite side of a heater (which mimicked a processor on a silicon chip). This package was exposed to ambient air and mounted in a smartphone. There was a drop in peak temperatures due to the PCM. Also, the melting process was completed within a second and the solidification process completed within few seconds when the package was placed in the smartphone due to high thermal conductivity of integrated heat spreaders.

Much past work has demonstrated that PCMs can be effective in reducing the operating temperature in consumer electronic devices through investigation of different power profiles, boundary conditions, device geometries, and PCMs [4–8]. To integrate PCMs in consumer electronics (especially in mobile devices), it is imperative to develop a set of design guidelines. These guidelines require understanding the influence of not only the material properties of the PCM, but also the interplay of material properties and geometry of the structure containing the PCM for real-time power profiles.

This work experimentally studies the feasibility of using a PCM in consumer electronic devices by placing the PCM filled in an enclosure (open from the top to allow for infrared thermal imaging) used as a passive heat sink for a smartphone processor. Different enclosure sizes and PCMs are used to identify key parameters that influence the effective integration of the PCM. Ultimately, the results are analyzed to provide design guidelines for integrating PCMs into thermal management systems.

2. Methodology

2.1. Selected phase change materials

This work investigates the effect of PCMs with transition temperatures between 42 °C and 62 °C. This transition temperature range is selected because it is below the maximum operating temperature limits of the processor. Specifically, three commercially-available wax-based PCMs are obtained: pure paraffin wax from Sigma-Aldrich®, PureTemp® PCM from Entropy Solutions, and AllCell PCC® from AllCell Technologies. The latent heat is measured using Differential Scanning Calorimetry (DSC) 2000 (TA Instruments, New Castle, DE, USA) with a

liquid nitrogen cooling system. The temperature range used for the DSC is from 0 °C to 100 °C, with heating and cooling rate of 5 °C min⁻¹. Table 1 shows selected material properties for the tested phase change materials.

2.2. In situ thermal measurements

Here, we measure the impact of PCM-based thermal management solution on the thermal performance of an android processor. Specifically, the setup consists of an enclosure filled with PCM, which acts as a heat sink, placed directly on the smartphone processor. To allow access to the processor for integration of this heat sink, we use a Single Board Computer (SBC) (see Fig. 1), which is a development board containing the essential components in a smartphone - the processor, Graphics Processing Unit (GPU), memory, and Input/Output (I/O) laid out on a single Printed Circuit Board (PCB), instead of a true smartphone.

The SBC runs Android based benchmarking applications, which are configured to stress the processor, thus representing worst case realtime usage scenario for a mobile device. Furthermore, since the components are laid out laterally, this geometry enables non-contact surface thermal measurements using Infrared (IR) imaging. The SBC (model IFC 6410, Inforce Computing Inc. Fremont, CA) runs an Android 4.0 operating system and has a Qualcomm Snapdragon APQ 8064 processor. The SBC is connected to I/O using USB ports, to a display via micro-HDMI port, and to a computer for data acquisition via micro-USB port. Processor temperatures and clock frequencies are monitored using a custom script and sampled at 60 Hz. The resolution of the temperature sensors is 1 °C. One temperature sensor is active before core 0 reaches 70 °C, then multiple sensors on the die are monitored. Here, we use 70 °C as a “cutoff” temperature in our thermal comparisons. In addition to the die temperatures, the top surface temperature is measured with an infrared microscope (Quantum Focus Instruments Corporation).

PCMs are contained in enclosures of size 10 mm × 10 mm × 3 mm, 10 mm × 10 mm × 5 mm, and 15 mm × 15 mm × 5 mm fabricated from 0.3 mm thick copper sheets. The enclosures are handmade from metal sheets and the edges are sealed to prevent leakage (The Gorilla Glue Company, Cincinnati, OH). Target dimensions for the enclosure are presented as X × Y × Z, but given the manual nature of the fabrication the dimensions are accurate to within 0.5 mm. Since the enclosures are slightly flexible, the 10 mm × 10 mm × 3 mm and 10 mm × 10 mm × 5 mm volumes reported are approximate, which is

Table 1

Material properties of PCMs used for *in situ* tests. (s) and (l) denote the solid and liquid state properties where available. All other properties, unless indicated are for solid phase. Thermal conductivity k , specific heat C_p , and density ρ are from Sigma Aldrich® [9,10], PureTemp® [11] and AllCell PCC® [12]. The transition temperature T_m , transition temperature range ΔT_m , and latent heats ΔH are measured using DSC.

PCM	T_m (datasheet) (°C)	T_m (DSC heating) (°C)	T_m (DSC cooling) (°C)	ΔT_m (DSC heating) (°C)	ΔT_m (DSC cooling) (°C)	ΔH (datasheet) (J/kg)	ΔH (DSC major transition) (J/kg)	k (W/(mK))	C_p (J/(kg K))	ρ (kg/m ³)
Paraffin Wax	58	60.36	54.04	18	9	NA	194.2×10^3	0.21 (s) 0.12 (l)	2890	900(s) 750 (l)
PureTemp®	42	41.3	37.3	12	4.25	218×10^3	310.5×10^3	0.25 (s) 0.15 (l)	1850 (s) 1910 (l)	940(s) 850 (l)
AllCell PCC®	55	53.6	49.8	13	6	165×10^3	222.3×10^3	10 (in-plane) 6 (cross-plane)	1960 (s) 2200 (l)	875

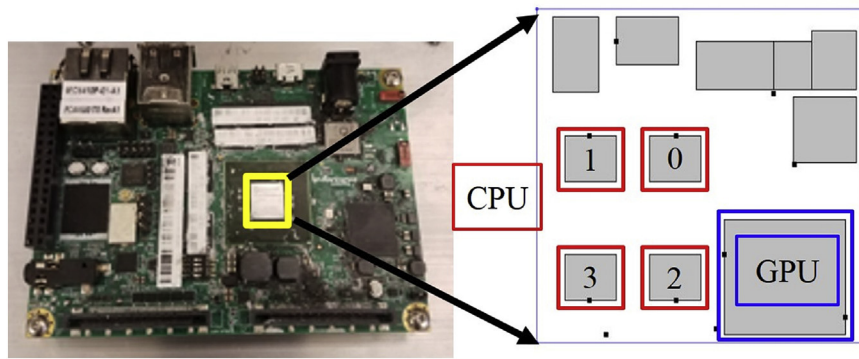


Fig. 1. Experimental setup of the Single Board Computer (SBC). An expanded schematic of the processor is shown on the right highlighting key components including the 4 cores of the CPU and the GPU. Core temperatures of the die (at locations indicated by the black dots in the exploded view) are recorded during operation. The SBC is connected to a display via a micro HDMI port and to a computer via USB ports.

why the weights are also presented (see Table 2). To ensure that the PCM does not overflow, it was heated on a hotplate at 90 °C until it is fully melted. If the PCM overflows, the volume of the PCM is reduced and the process repeated till no PCM leaks out of the container. The PCM was cooled down under natural convection while the hotplate remains at 30 °C. The mass of the PCM was recorded prior to the melting cycling and thus slightly overestimates the final mass. As an example, for the paraffin wax, ≈ 0.1 g of wax was removed from the largest container to prevent over filling during the cyclic melting. The AllCell PCC[®], being a shape stable material does not melt, so it is cut into small pieces and filled into the enclosure.

To evaluate the influence of the PCMs, two baseline experiments are required: (1) the bare die with no added thermal solutions and (2) the bare die with each empty enclosure. After measuring the thermal performance of the bare die, each enclosure to the die is attached with OMEGATHERM[®] 201 Thermal Interface Material (TIM) [13] and the thermal performance is measured. After the baseline measurements, the enclosures are filled with PCM, attached to the processor with OMEGATHERM[®] 201 TIM, and evaluated. The masses of all PCMs used for each enclosure size are listed in Table 2. The mass is measured using a weighing balance (model Entris, Sartorius Corporation, Bohemia, NY) with an uncertainty of 0.001 g.

During the thermal testing, IR thermal imaging measures the temperature of the topmost surface over an area of about 121 mm² with 11 μ m resolution. Here, with the real android device as the heat source during the *in situ* testing, it is not possible to achieve a truly uniform temperature above room temperature for *in situ* calibration of emissivity. Specifically, the emissivity of the wax was calibrated using a uniform heating thermal stage *ex situ*, and a uniform emissivity was applied to the whole image domain for the *in situ* testing. Thus, that value is only appropriate for the region with wax. For the “die only” and the copper enclosure for the “die and unfilled enclosure”, the low emissivity of the top surfaces imaged would provide challenges for accurate thermal data, and a graphite spray (B’Laster Corporation, Cleveland, Ohio) is used to improve the measurements. To prevent contamination of PCM, graphite coating is not applied for the measurements with the wax samples. The graphite spray has been calibrated *ex situ* as well, consistently showing emissivity of ≈ 0.90 , regardless of the underlying substrate. The reference thermal image is taken in the unpowered state (i.e., without any connections to power supply, display and computer) and a constant emissivity of 0.9 is applied to the whole image. For both materials, the high emissivity ensures that even with $\pm 10\%$ uncertainty in the emissivity of the surface, results in $\pm 6\%$ uncertainty in the measured temperature rise at 85 °C. Thermal movies are recorded throughout the duration of the benchmark with a frame delay of 1 s for approximately twice as long as the benchmark to capture the entire heating and cool down process. The movies are sufficiently long that the temperature at the end is almost equal to the initial temperature ($\approx 30^\circ\text{C}$). The temperature logging script starts at about the same time as the movie. There is an

approximately 10 s delay in starting the benchmark test.

2.2.1. Thermal performance evaluation

In this work, the LINPACK Benchmark [14] is used to evaluate the performance with and without the PCM thermal solutions. The LINPACK Benchmark stresses the system by solving a dense system of linear equations of the form $Ax = b$. Square matrices from size 250 to 1000 are solved for two different step sizes – 25 and 15 using the LINPACK benchmark, which translates to two use cases referred as LINPACK 1 and 2, respectively. LINPACK 1 and 2 consume average power of 1.5 W and 2 W, as measured using Qualcomm App Tuneup Kit application. The results of the benchmark represent the systems performance for floating point operations only and not the overall performance. In addition to the temperatures monitored during the benchmarking app, the runtime of the benchmark, as impacted by the varying clock frequencies of the cores, is an indication of the effectiveness of the thermal solution.

3. Results and discussion

3.1. Latent heat & transition temperatures

In the DSC tests, the sample is first heated to 100 °C, and then cooled down. The transition temperature and latent heat are measured in both the heating and cooling portion of the cycle (see Fig. 2(a)). Undercooling is indicated by the difference between the transition temperatures during heating and cooling cycles. Solidification is initiated from nucleation sites, which include container walls, impurities, or voids in the sample. In the absence of these nuclei, the liquid phase can be maintained throughout despite temperature below the transition temperature. Since the commercial PCMs are comprised of multiple constituents (base material + fillers), which serve as nucleation sites, they solidify with a relatively low degree of undercooling (less than 5 °C). Multiple transitions can be represented by multiple peaks on the heating and cooling curves. The AllCell PCC[®] exhibits multiple transition implying that a mixture of PCMs are present. For paraffins, the melting point is directly proportional to the chain length of the hydrocarbon. A mixture of waxes would exhibit multiple peaks because of different transition temperatures of individual components.

Table 2

Mass of PCMs (in g) and the enclosures for the *in situ* tests.

PCM		Enclosure Dimensions (mm)		
Type	Supplier	10 × 10 × 3	10 × 10 × 5	15 × 15 × 5
Paraffin Wax	Sigma- Aldrich	0.274	0.447	0.963
PureTemp [®]	Entropy Solutions	0.27	0.3	0.72
AllCell PCC [®]	AllCell Technologies	0.191	0.443	0.859
Copper Enclosure	McMaster Carr	1.136	1.711	2.878

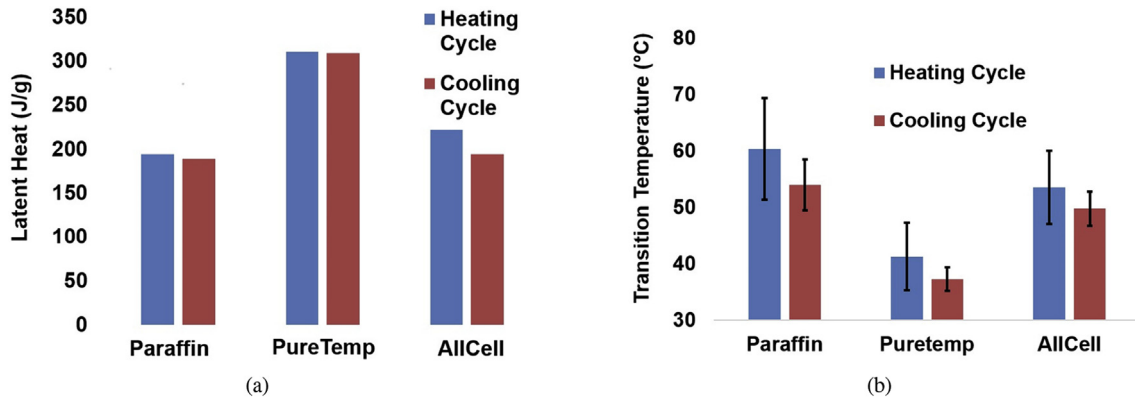


Fig. 2. Characterization of thermophysical properties of the commercial PCMs. (a) Latent Heat during heating and cooling cycles. The PureTemp[®] has the highest latent heat while the paraffin wax has the lowest latent heat. (b) Transition temperatures during heating and cooling cycles. The error bars represent the transition temperature ranges for the heating and cooling cycles. The difference in the transition temperatures between the two cycles is within 5 °C, indicating that undercooling effects may be insignificant.

3.2. In situ thermal testing

To evaluate the optimum configuration of the thermal solution, we vary the enclosure size and the choice of PCM. The time taken to reach the cutoff temperature is a metric used to characterize the performance of PCMs, since the primary goal of a latent heat based TES system is to increase the time the processor can operate a high power before it would need to be throttled to prevent overheating. Here, this time (referred as the “cutoff time”) is chosen as 70 °C (see Section 2). Fig. 3 shows the internal core temperature measurements for the bare die, the die with an unfilled enclosure, and the die with an enclosure filled with PureTemp[®] PCM for LINPACK 1 benchmark.

Attaching the unfilled enclosure increases the cutoff time due to improved heat spreading, increased surface area available for convection, and the added thermal mass of the system with the enclosure. Filling the enclosure with the PCM delays this cutoff time by ~ 40 s for the LINPACK 1 and ~ 33 s for the LINPACK 2 benchmark (for the 10 mm × 10 mm × 3 mm enclosure) relative to the unfilled enclosure, due to the latent heat of PCM, which absorbs energy during the phase change process. Note that a plateau in the melting range is not obvious

in the data in this plot because temperature presented is the core (processor) temperature, which is physically separated from the PCM by many layers. However, the shift in the curves with the PCM indicates the effect of melting. At the end of the experiment, the PCM is fully solidified.

In addition to the choice of PCM, the enclosure dimensions impact the performance of the thermal storage solution. Here, in addition to the 10 mm × 10 mm × 3 mm case shown above, enclosures with (1) an equal base area, but thicker film of PCM (10 mm × 10 mm × 5 mm) and (2) a larger base and height (15 mm × 15 mm × 5 mm) are evaluated. The cutoff times and maximum temperatures are shown in Fig. 4 for each enclosure size with 3 commercial PCMs for both the LINPACK 1 and LINPACK 2 benchmarks. The error bars for the cutoff time indicate a 15% error representative of the variation observed when repeating the tests 3 times. For unfilled enclosures, the time taken to reach the cutoff temperature increases with increased enclosure height (from 3 mm to 5 mm) because of the increased area for convection and the added thermal mass of the enclosure.

The cutoff time is increased for the enclosure filled with PCM compared to the unfilled enclosure for all benchmarks and enclosure

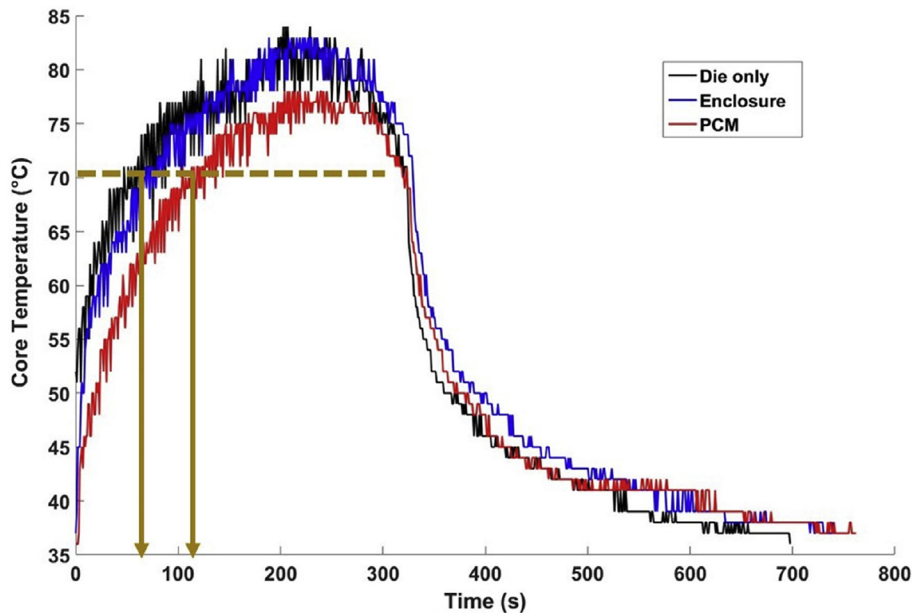


Fig. 3. Transient thermal response of a processor core during the LINPACK 1 benchmark for 10 mm × 10 mm × 3 mm copper enclosure filled with PureTemp[®]. The addition of the PCM delays the cutoff time by ~ 40s relative to the unfilled enclosure, and reduces the maximum temperature during the benchmarking tests. The temperature fluctuations observed during the benchmarking application execution (0 ~ 350 s) are due to rapid variations in the clock frequency. After the benchmark is complete, the plateaus in temperature during the decay are due to roundoff error since the temperature resolution of the sensor is 1 °C.

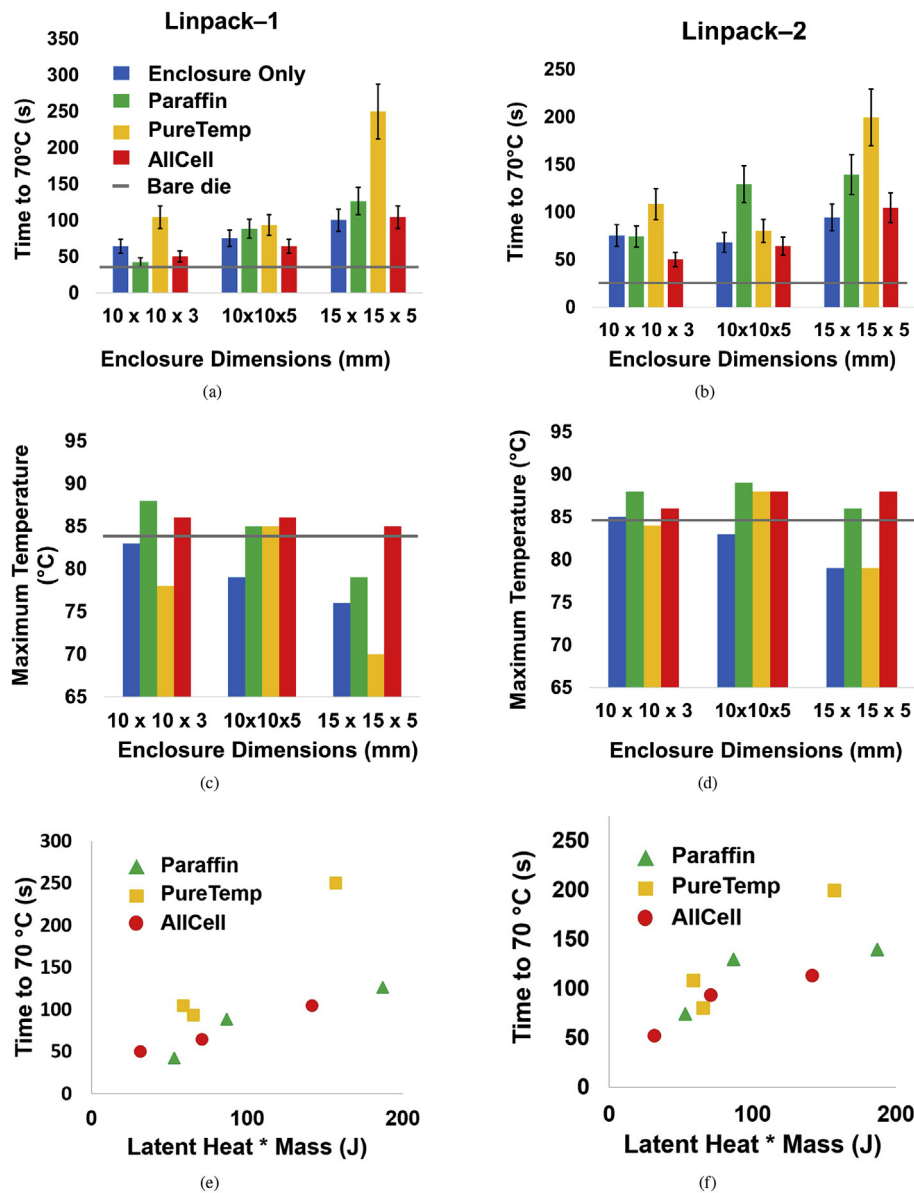


Fig. 4. Effect of enclosure size and PCM on ((a)–(b)) the time taken to reach the cutoff temperature of 70 °C and ((c)–(d)) the maximum core temperature while running the LINPACK benchmarks. The PureTemp® stores more energy for a given volume since it has the highest volumetric latent heat. The trend in maximum temperature is less clear due to the competing effects of increased surface area (heat spreading with increasing surface area) and increasing thermal resistances to the environment with increasing thickness. (e)–(f) Cutoff time as a function of the maximum possible energy storage in the PCM (mass of PCM × latent heat). The delay time increases approximately linearly with energy storage capacity, as expected from an energy balance of the PCM. The PureTemp® increases the cutoff time most effectively due to enhanced heat spreading capabilities.

sizes because of heat absorption in the transition temperature range due to latent heat of phase change. For the lower power LINPACK 1 benchmark, the PureTemp® outperforms the other PCMs due to a combination of the highest volumetric energy storage capability and lowest transition temperature. The transition temperature of 42 °C makes effective use of the energy storage due to latent heat. For paraffin wax, the transition temperature is ~ 58 °C. Thus, initially the mass of PCM is storing energy by sensible heating, which is not as effective as the latent heat. Further, the low thermal conductivity of paraffin wax impedes heat transfer thereby increasing the processor temperature and limiting the effect of the PCM on the cutoff time. The AllCell PCC® is a form stable PCM meaning that it does not fully liquify when heated. Instead, the active PCM is encapsulated inside a high thermal conductivity structure. For most enclosure sizes, the thermal performance of AllCell PCC® is comparable to the unfilled enclosure baseline measurement, perhaps as a consequence of poor contact between the AllCell PCC® and our enclosure. Hence in some cases (see Fig. 4(a)), the

enclosure exhibits lower cutoff time than the AllCell PCC® and PureTemp® since it dissipates heat quickly due to improved heat spreading.

As the enclosure size increases, improved heat spreading within the enclosure and the added material increases the cutoff time. For a larger base area (height unchanged), the cutoff time increases by as much as 2.6 times for the LINPACK 1 benchmark and 2.5 times for the LINPACK 2 benchmark. Because the PCMs have different volumetric energy storage capabilities and transition temperatures, the relationship between the performance, enclosure size, and PCM is complex. For a clearer comparison, we evaluate the maximum energy storage capability of the material in the enclosure, which is the latent heat of phase change times the mass of the PCM. From a simple energy balance, we expect approximately a linear increase in the cutoff time with increasing energy storage capability. As illustrated in Fig. 4(e–f), for each material, the delay time increases approximately linearly with energy storage capability. Deviations from the linear trend indicate the interplay between thermal transport and thermal storage mechanisms. The PureTemp®

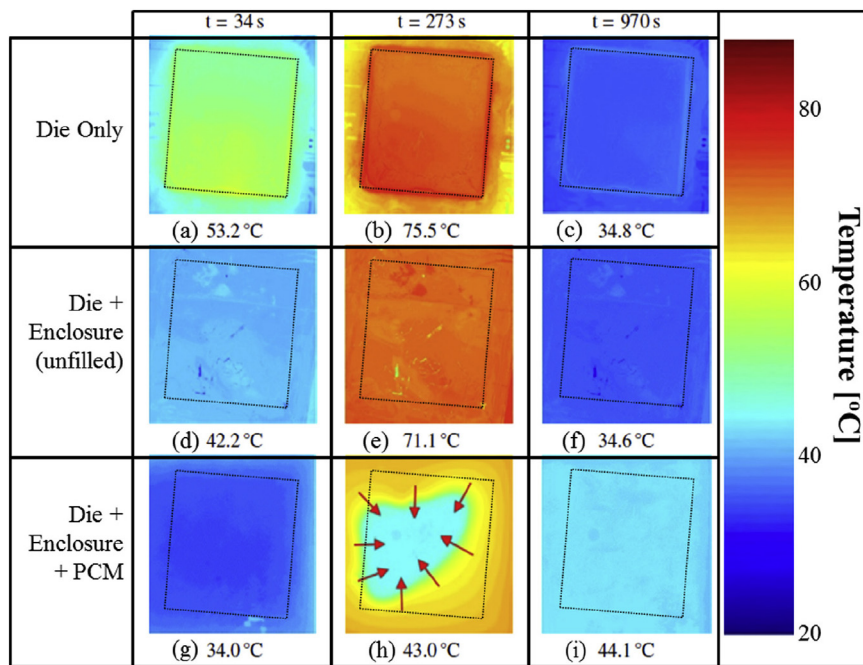


Fig. 5. 2D surface temperature maps (in °C) for the die, enclosure (unfilled) attached to die, and enclosure filled with PureTemp® for three times - before phase change, during phase change, and after complete re-solidification - recorded during the LINPACK 2 benchmark. The maximum temperature gradients for the die at 273 s, along the horizontal and vertical centerline are 0.5 °C and 8 °C, respectively. Hot spots are observed in bottom left corner due to the proximity to the heat generating components. The temperatures below each image represent the maximum temperature in the observed surface. Note that the melt front propagates inwards from the enclosure walls (shown by red arrows) and from the bottom of the enclosure to the top. For the enclosure filled with PCM at 273 s, the maximum temperature denotes the maximum temperature of the solid phase in the observed region, as the emissivity was not calibrated in the molten phase. The dotted black line in each panel indicates the outline of the die. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

exhibits the greatest delay in reaching 70 °C.

In many cases, the addition of PCM decreases the maximum temperature observed in the die. However, increasing thickness of the PCM does not consistently improve this metric (see Fig. 4(c–d)). Although the available surface area of the enclosure increases as the enclosure height increases, the increased thickness of the PCM results in an increase in the thermal resistance between the die and ambient in the vertical direction, resulting in an inferior heat dissipation through the PCM. Hence, the maximum core temperatures are often higher than the shorter enclosure, which also shortens the cutoff time. Fig. 5 shows 2D temperature maps (obtained from IR imaging) of the baseline cases and the enclosure (15 mm × 15 mm × 5 mm) filled with a PCM (PureTemp®) during the LINPACK 2 benchmark for three illustrative times. For the die only case, a maximum temperature difference of 0.5 °C and 8 °C is observed along the horizontal and vertical centerlines, respectively. The spatial temperature gradients are likely due to the location of the main heat generating components - CPU cores and GPU. For the die + enclosure (unfilled) case, the temperatures are vary uniform due to the heat spreading of the copper enclosure. At short times (illustrated at $t = 34$ s), the surface of the PCM is considerably cooler than the surface of the die at the same time during the benchmark. In part, this is due to the required time for heat to penetrate from the die through the PCM to the top surface. Later during the benchmark (illustrated at $t = 273$ s), the melt front is clearly observed in the infrared image. Note that the melt front propagates from the bottom surface upwards and from the outer edges inwards simultaneously. This is due to the high thermal conductivity of the enclosure walls. Thus, there is a cold mass of solid PCM observable in the center of the imaging plane. After the benchmarking ends (illustrated at $t = 970$ s), the PCM cools slightly slower than the baseline cases as the PCM must re-solidify during the cooling phase. However, from the die temperature measurements (see Fig. 3), this does not significantly delay the cooling of the die core temperature, which indicates that there are alternate pathways for heat dissipation during this phase, such as through the PCB underneath the processor.

4. Conclusions

This work experimentally evaluated passive thermal management of an android processor using 3 commercial PCMs and various packaging

sizes. The PCMs are effective at increasing the time for the processor to reach a selected cutoff temperature, however, there is a complex interaction between material properties when optimizing the thermal solution geometry. Thermal conductivity and latent heat need to be optimized according to packaging constraints (enclosure sizes and weight of PCMs). Thermal design using heat spreaders and thermal interface materials is often based on the peak load and, thus, thermal resistances are minimized. PCMs exploit the thermal capacitance through their latent heat, hence the thermal design is based on average loads. PCMs are also compatible with “soft” thermal management strategies [15,16] used in consumer electronics which limit the clock frequencies if a temperature threshold is reached. PCM are more suited to longer benchmark runtimes if a strategy that estimates the unmelted PCM mass is used. Future directions should focus on integrating PCMs in high thermal conductivity leak proof packages and *in situ* tests for high power use cases.

Acknowledgements

The contribution of Alex Bruce, Prahlad Kulkarni, and Collier Miers for materials characterization and *in situ* tests is gratefully acknowledged. The authors are grateful to Nader Nikfar and Damion Gastelum of Qualcomm Technologies for providing insights on setting up the experiment. This study was funded by members of the Cooling Technologies Research Center, an NSF Industry/University Cooperative Research Center at Purdue University.

Appendix A. Supplementary data

Supplementary data related to this article can be found at <http://dx.doi.org/10.1016/j.ijthermalsci.2018.03.012>.

References

- [1] L. Yeh, Review of heat transfer technologies in electronic equipment, *J Electron Packag* (1995) 333–339.
- [2] A. Tilley, H. Associates, The measure of man and woman: human factors in design, Wiley, New York, 2002.
- [3] K. Chintakrinda, R. Weinstein, A. Fleischer, A direct comparison of three different material enhancement methods on the transient thermal response of paraffin phase change material exposed to high heat fluxes, *Int J Therm Sci* 50 (2011) 1639–1647.
- [4] L. Shao, A. Raghavan, L. Emurian, M. Papaefthymiou, T. Wenisch, M. Martin, et al,

- On-chip phase change heat sinks designed for computational sprinting, IEEE, pp. 29–34.
- [5] M. Hodes, R. Weinstein, S. Pence, J. Piccini, L. Manzione, C. Chen, Transient thermal management of a handset using phase change material (PCM), *J Electron Packag* 124 (2002) 419–426.
 - [6] N. Leoni, C.H. Amon, Transient thermal design of wearable computers with embedded electronics using phase change materials, *Proceedings of the 32nd ASME national heat transfer conference* vol. 343, (1997), pp. 49–56.
 - [7] C. Bauer, R. Wirtz, Thermal characteristics of a compact, passive thermal energy storage device, *Proceedings of the ASME international mechanical engineering conference and exposition (IMECE)* vol. 366, (2000), pp. 283–290.
 - [8] S. Gurrum, Y. Joshi, J. Kim, Thermal management of high temperature pulsed electronics using metallic phase change materials, *Numer Heat Tran Part A: Applications* 42 (2002) 777–790.
 - [9] Sigma Aldrich phase change material datasheet, <https://www.sigmaaldrich.com/catalog/product/aldrich/327212?lang=en®ion=US>, Accessed: 2017-03-22.
 - [10] R. Kandasamy, X. Wang, A.S. Mujumdar, Application of phase change materials in thermal management of electronics, *Appl Therm Eng* 27 (2007) 2822–2832.
 - [11] PureTemp-42 phase change material datasheet, <http://www.puretemp.com/images/pdfs/PureTemp%2042%20Technical%20Data%20Sheet.pdf>, Accessed: 2017-03-29.
 - [12] AllCell technologies phase change material datasheet, https://www.allcelltech.com/images/datasheets/pcc/AllCell_PCC.pdf, Accessed: 2017-03-29.
 - [13] Omegatherm 201 thermal interface material datasheet, <http://www.omega.com/temperature/pdf/OT-201.pdf>, Accessed: 2016-07-25.
 - [14] J. Dongarra, Performance of various computers using standard linear equations software (Linpack Benchmark Report), University of Tennessee Computer Science Technical Report, Technical Report, 2005 CS-89–85.
 - [15] C. De Vivero, F. Kaplan, A. Coskun, Experimental validation of a detailed phase change model on a hardware testbed, in: *ASME 2015 international technical conference and exhibition on packaging and integration of electronic and photonic microsystems collocated with the ASME 2015 13th international conference on nanochannels, microchannels, and minichannels*, American society of mechanical engineers, pp. V001T09A086–V001T09A086.
 - [16] Tilli, A. and Bartolini, A. and Cacciari M. and Benini L., Don't burn your mobile!: safe computational re-sprinting via model predictive control, in: *Proceedings of the eighth IEEE/ACM/IFIP international conference on hardware/software Co-design and system synthesis*, ACM, pp. 373–382.