

# BASIC ELECTRONIC CIRCUITS

Amplifiers, and Op-Amps

# Amplifiers

- **Signal Amplification:**
  - Increase the amplitude of the signal without changing the other parameters.
- Why the signal amplification is needed?
  - The weak signal are too small for reliable processing
- **Linearity:** it is essential to make sure that the information contained in the signal is not changed and no new information is introduced. Then the output signal will be exact replica of that at the input.
- Any changes in waveform is considered to be distortion and is obviously undesirable.
- Ex: Voltage amplifier, Power Amplifier.

# Amplifier parameters

- Gain
- Frequency response
- Bandwidth
- Input impedance
- Output impedance

# Gain

- Measure of the amplification of an amplifier
- Ratio of the output signal amplitude to input signal amplitude
- Symbol -  $A$
- Voltage gain ( $A_V$ ), Current gain ( $A_i$ ), power gain ( $A_P$ )

$$A_V = \frac{V_{out}}{V_{in}}$$

$$A_I = \frac{I_{out}}{I_{in}}$$

$$A_P = \frac{P_{out}}{P_{in}}$$

Voltage Gain in dB=  $20 \log |A_V|$

Current Gain in dB=  $20 \log |A_i|$

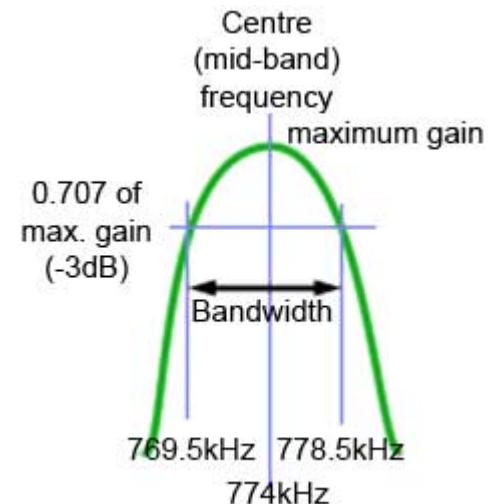
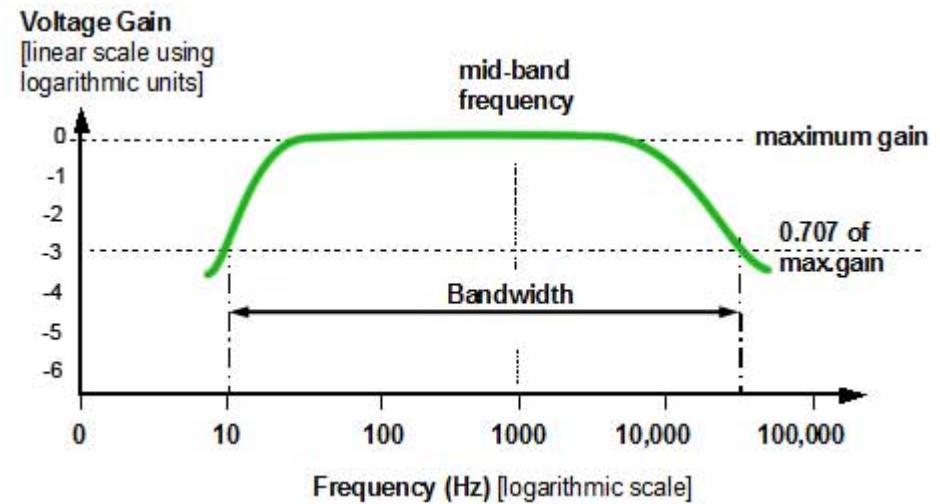
Power Gain in dB=  $10 \log A_P$

# Input and output Impedance

- Input impedance: impedance experienced as the amount of current able flow into the input terminals
- Depends upon, frequency of the signal, gain of the amplifier, and load connected at the output terminals.
- Output impedance: responsible for the fall in signal voltage at the output terminals, when current is drawn from the output terminals.

# Frequency Response and Bandwidth

- Do not have same gain at all frequencies
- Ex: Audio amplifier can amplify only audio frequencies (<20 kHz).
- Band of frequencies over which the amplifier has a useful gain.

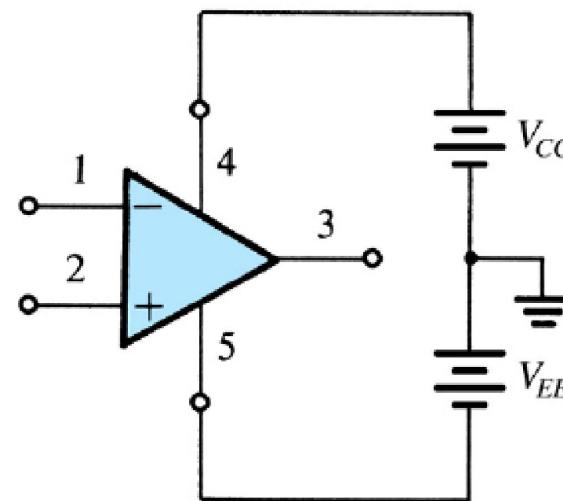
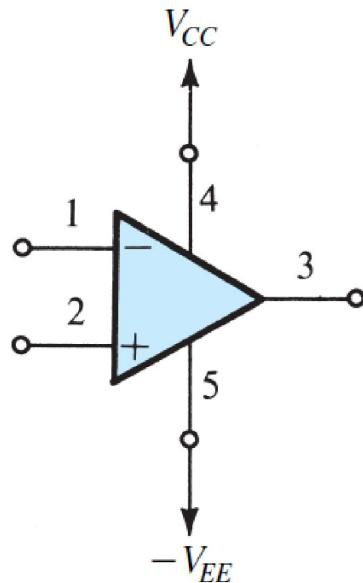
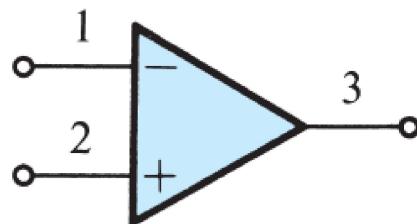


# Operational Amplifiers

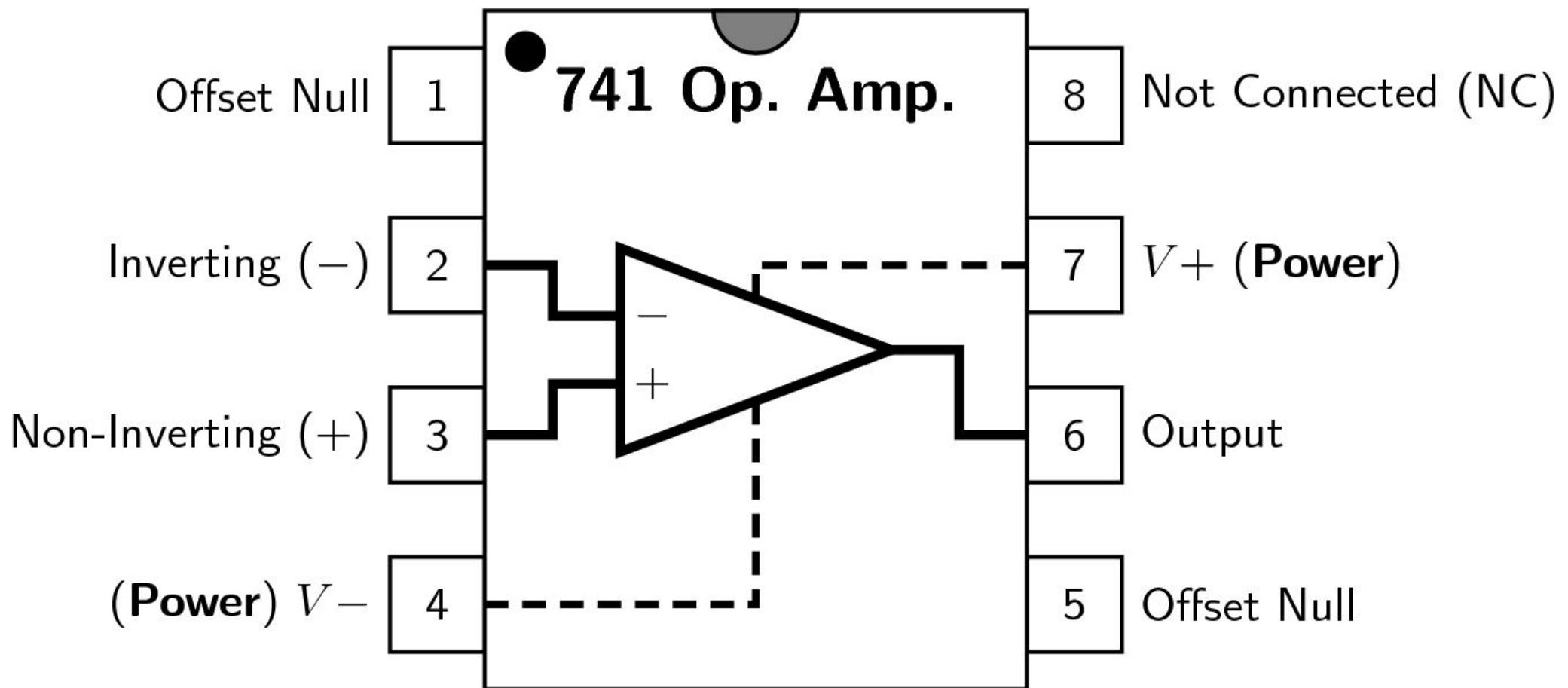
- Widely used in almost all modern communication, instrumentation, and computation systems because they are "Versatile".
- OP-amps are used to overcome the shortcomings of basic amplifier like low i/p impedance, moderate gain, and limited bandwidth.
- The op-amp is made up of a large number of transistors and resistors etc., here we consider it as a circuit building block, study its terminal characteristics and its applications.

# The Ideal Op-Amp: terminals

- 3 terminals: Two input and one output.
- No terminal of the op-amp package is physically connected to ground.

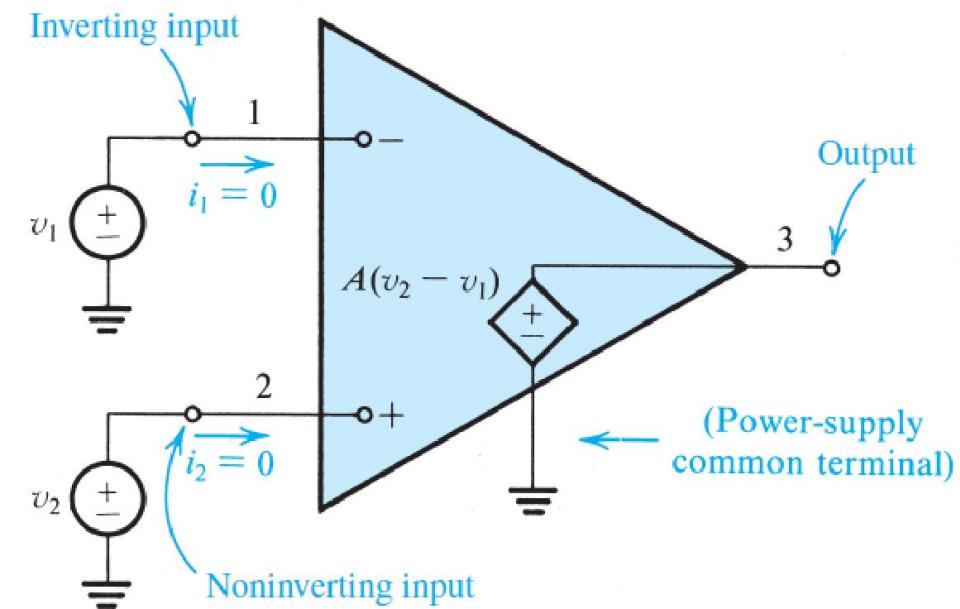


# Pin configuration



# Function and characteristics

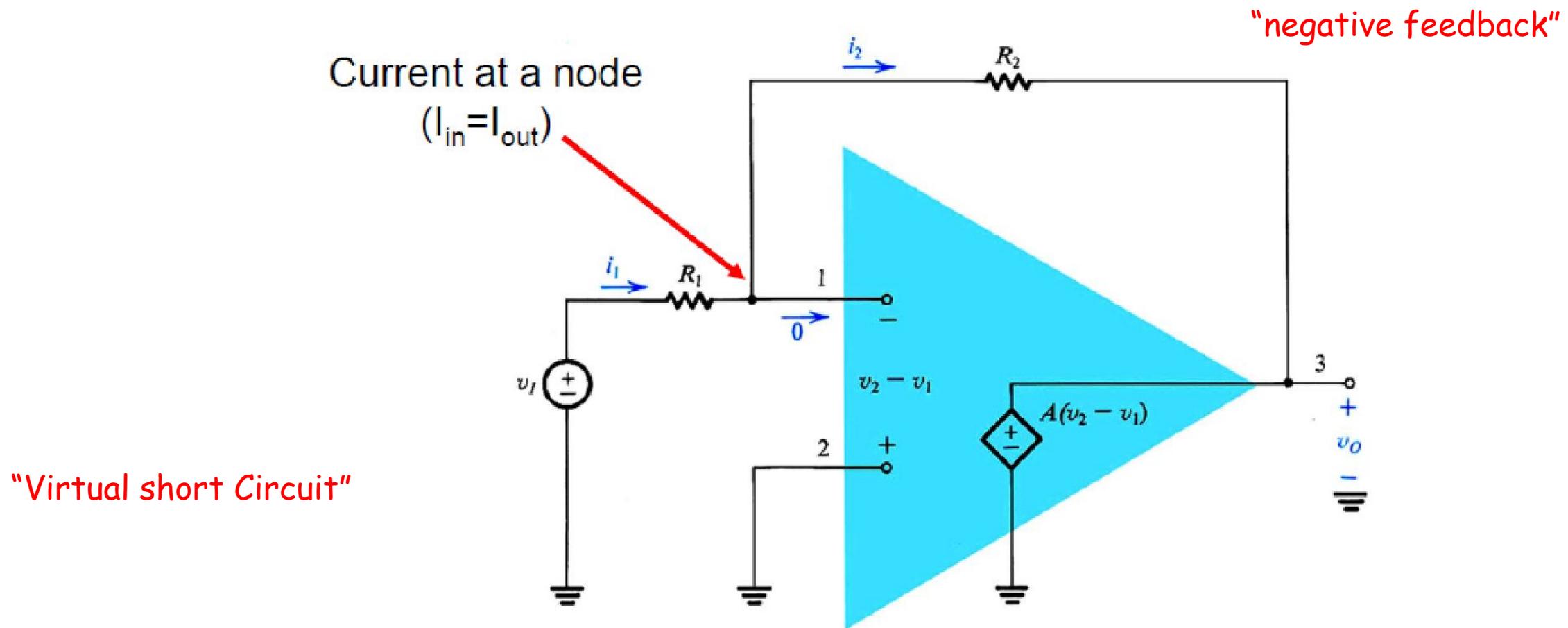
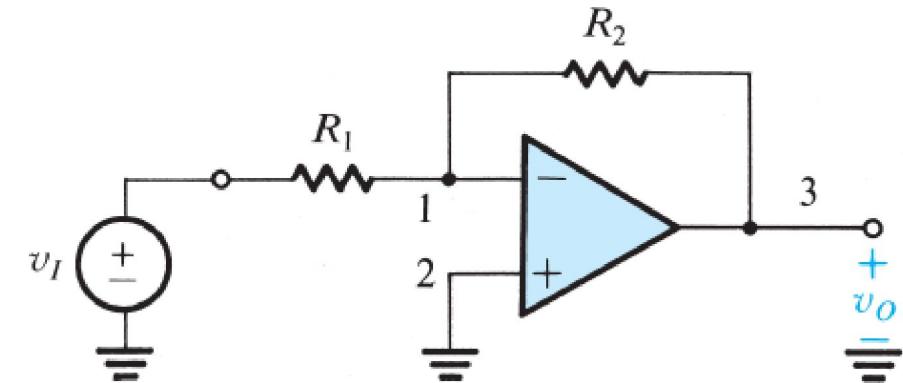
- Basic function is to sense the difference between the voltage signals applied at its input terminals.
  - Infinite input impedance
  - Zero output impedance
  - Zero common mode gain
  - Infinite open-loop gain  $A$
  - Infinite bandwidth

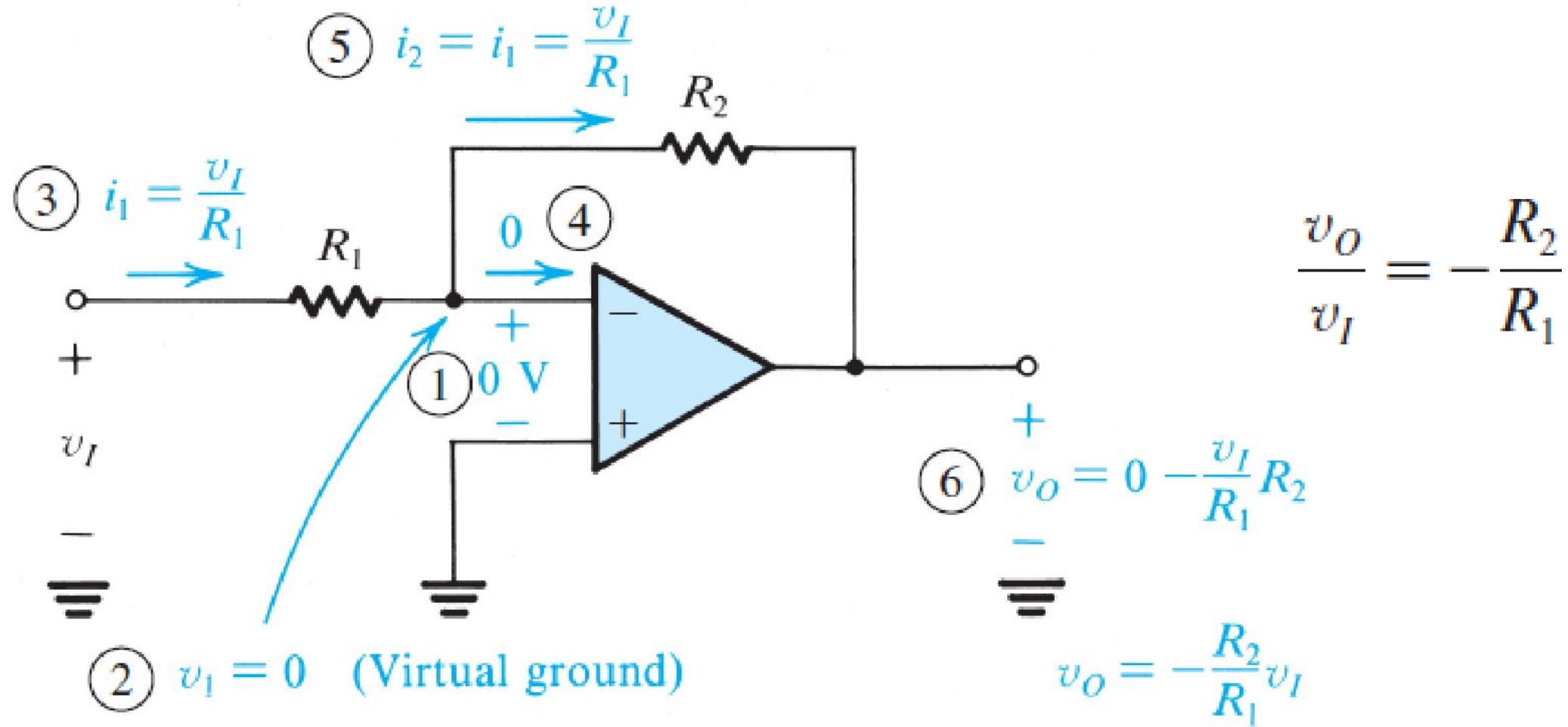


Equivalent Circuit (VCVS) model of the ideal OP-AMP

Differential input, single-ended output amplifier

# Inverting Configuration



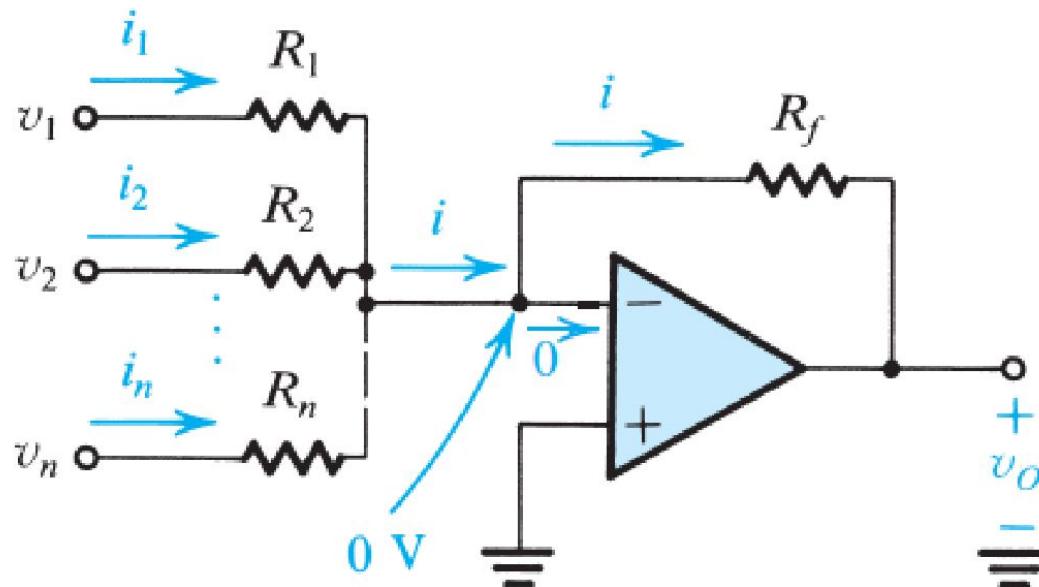


Closed loop gain is independent of open-loop gain, entirely depends on the passive elements.

# Application: The weighted Summer

$$i = i_1 + i_2 + \cdots + i_n$$

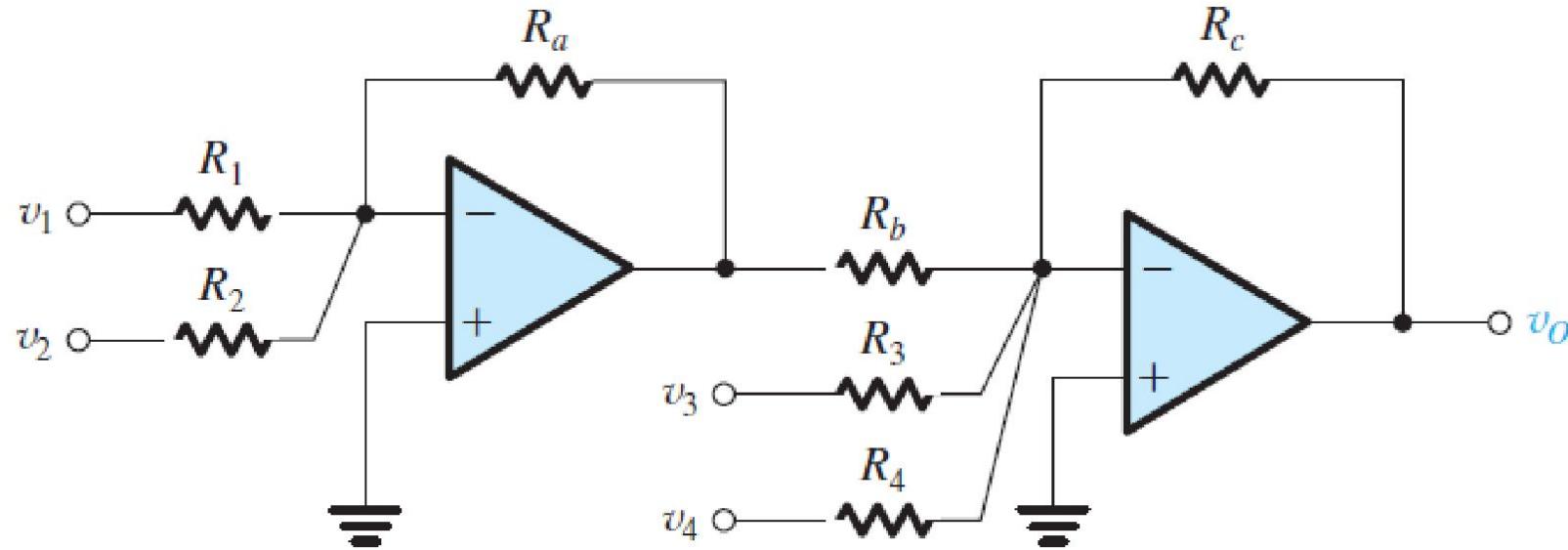
$$v_O = 0 - iR_f = -iR_f$$



$$v_O = - \left( \frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \cdots + \frac{R_f}{R_n} v_n \right)$$



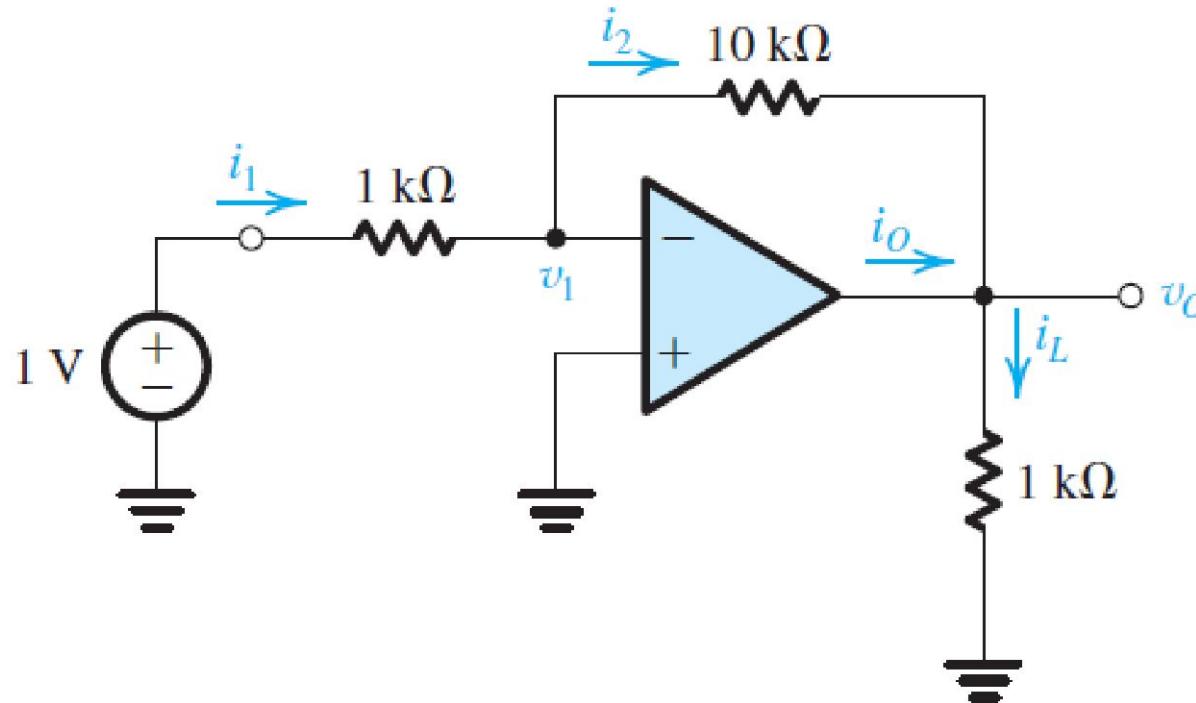
# Summing signals with opposite sign



$$v_O = v_1 \left( \frac{R_a}{R_1} \right) \left( \frac{R_c}{R_b} \right) + v_2 \left( \frac{R_a}{R_2} \right) \left( \frac{R_c}{R_b} \right) - v_3 \left( \frac{R_c}{R_3} \right) - v_4 \left( \frac{R_c}{R_4} \right)$$



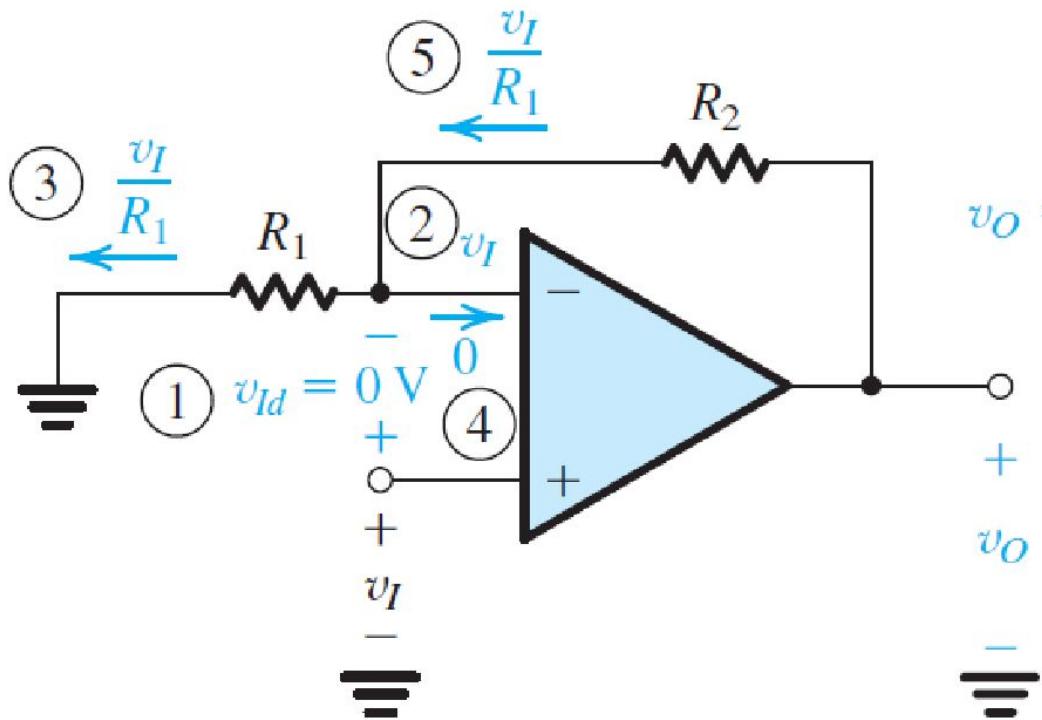
Determine the values of  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_o$ ,  $i_L$ , and  $i_o$ . Also determine the values of  $V_o/V_I$ ,  $I_L/i_1$  and power gain  $P_L/P_i$



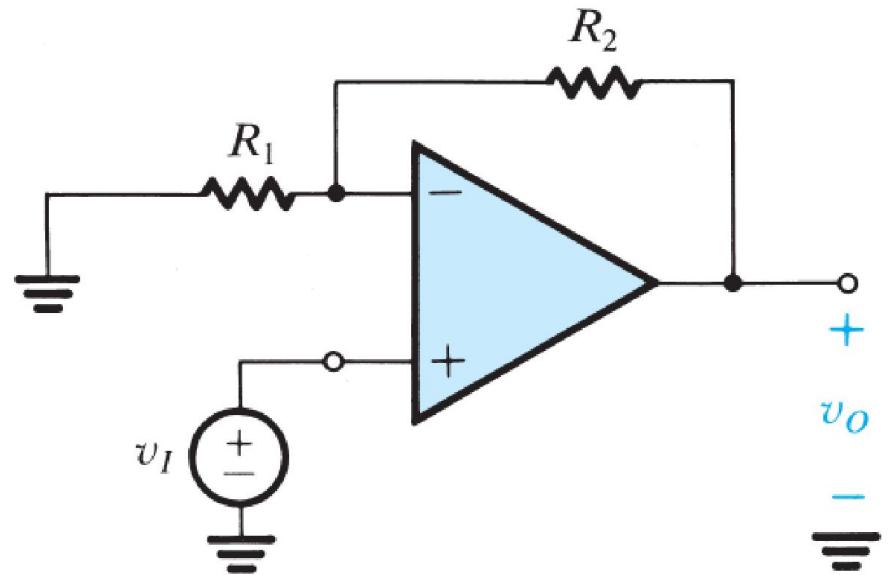
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# Noninverting Configuration

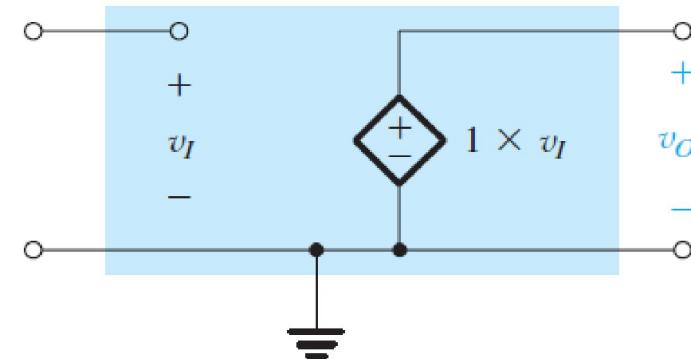
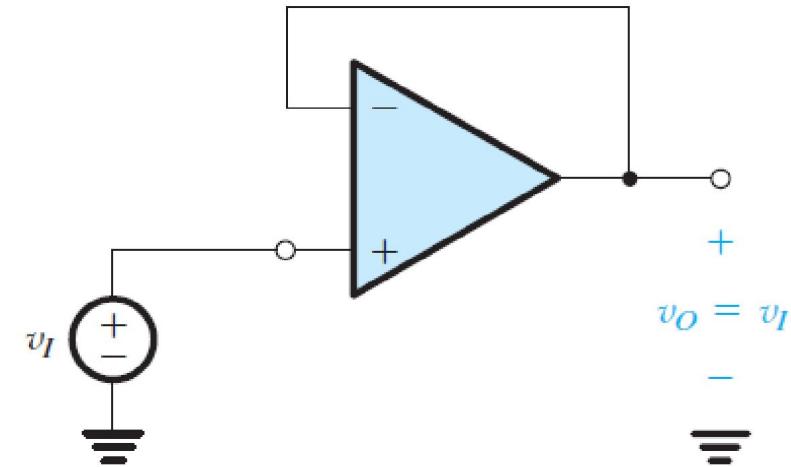


$$v_O = v_I + \frac{v_I}{R_1} R_2 = v_I \left(1 + \frac{R_2}{R_1}\right) \quad (6)$$

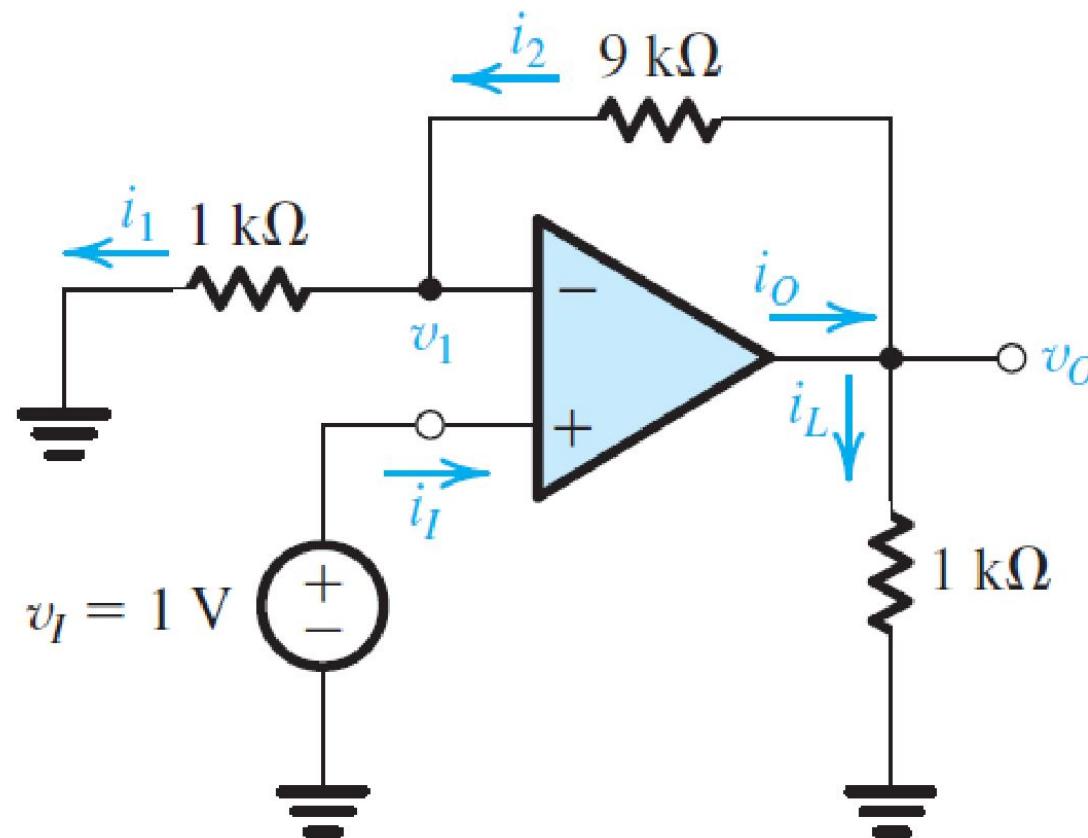


# Application: Voltage follower

- High input impedance is a desirable feature of non inverting configuration.
- Unity-gain amplifier or Voltage follower.
- Used as an impedance transformer.

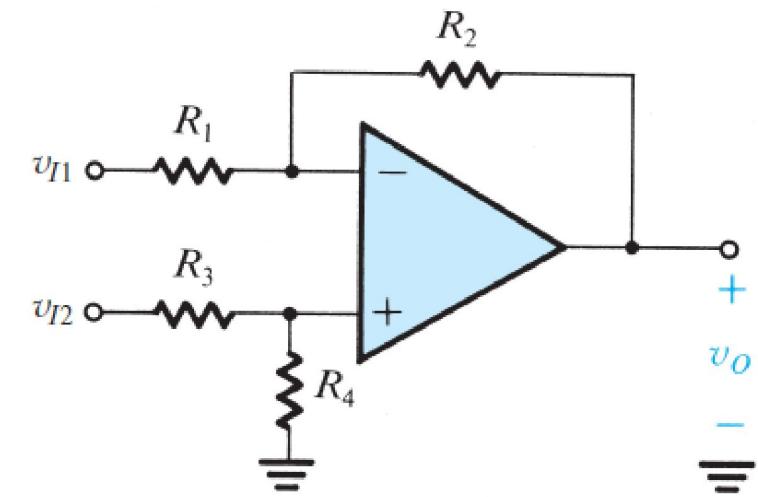


Determine the values of  $i_I$ ,  $v_1$ ,  $i_1$ ,  $i_2$ ,  $v_o$ ,  $i_L$ , and  $i_o$ . Also determine the values of  $V_o/V_I$ ,  $I_L/i_I$  and power gain  $P_L/P_I$



# Difference Amplifier

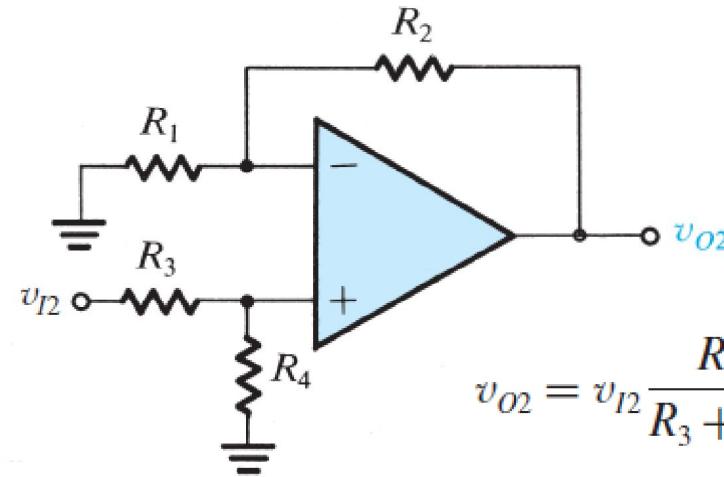
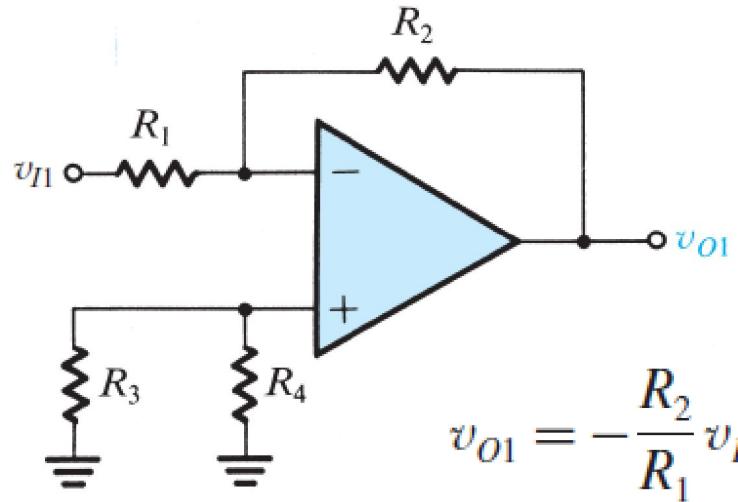
- Combination of inverting and noninverting configurations.
- Common mode signals need to be rejected, hence the magnitude of the inverting and noninverting must be same.
- Hence attenuate the gain of the +ve path from  $(1+R_2/R_1)$  to  $R_2/R_1$ .



$$\frac{R_4}{R_4 + R_3} \left( 1 + \frac{R_2}{R_1} \right) = \frac{R_2}{R_1}$$

$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

- By Superposition:



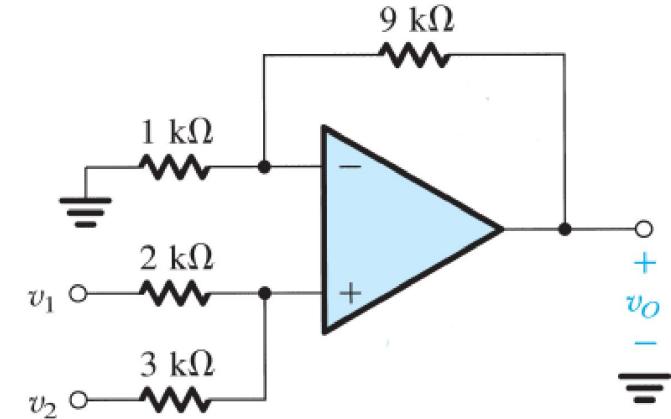
$$\frac{R_4}{R_3} = \frac{R_2}{R_1}$$

$$v_o = \frac{R_2}{R_1} (v_{I2} - v_{I1}) = \frac{R_2}{R_1} v_{Id}$$

$$A_d = \frac{R_2}{R_1}$$

$$R_3 = R_1 \quad \text{and} \quad R_4 = R_2$$

- Use superposition to determine  $V_o$



$$v_O = 6v_1 + 4v_2$$

- If the 1K resistor is disconnected from the ground and connected to  $V_3$ , determine  $V_o$ .

$$v_O = 6v_1 + 4v_2 - 9v_3$$

- Design a non inverting amplifier with a gain of 2. At the maximum output voltage of 10 V the current in the voltage divider is to be 10  $\mu A$ .

$$v_0 = 10 V$$

$$\frac{v_0 - v_1}{R_s} = 10 \mu A$$

$$G = 2 = 1 + R_2/R_1$$

$$\frac{v_1}{R_s} = 10 \mu A$$

$$R_1 = 0.5 M\Omega$$

$$R_1 = R_2$$

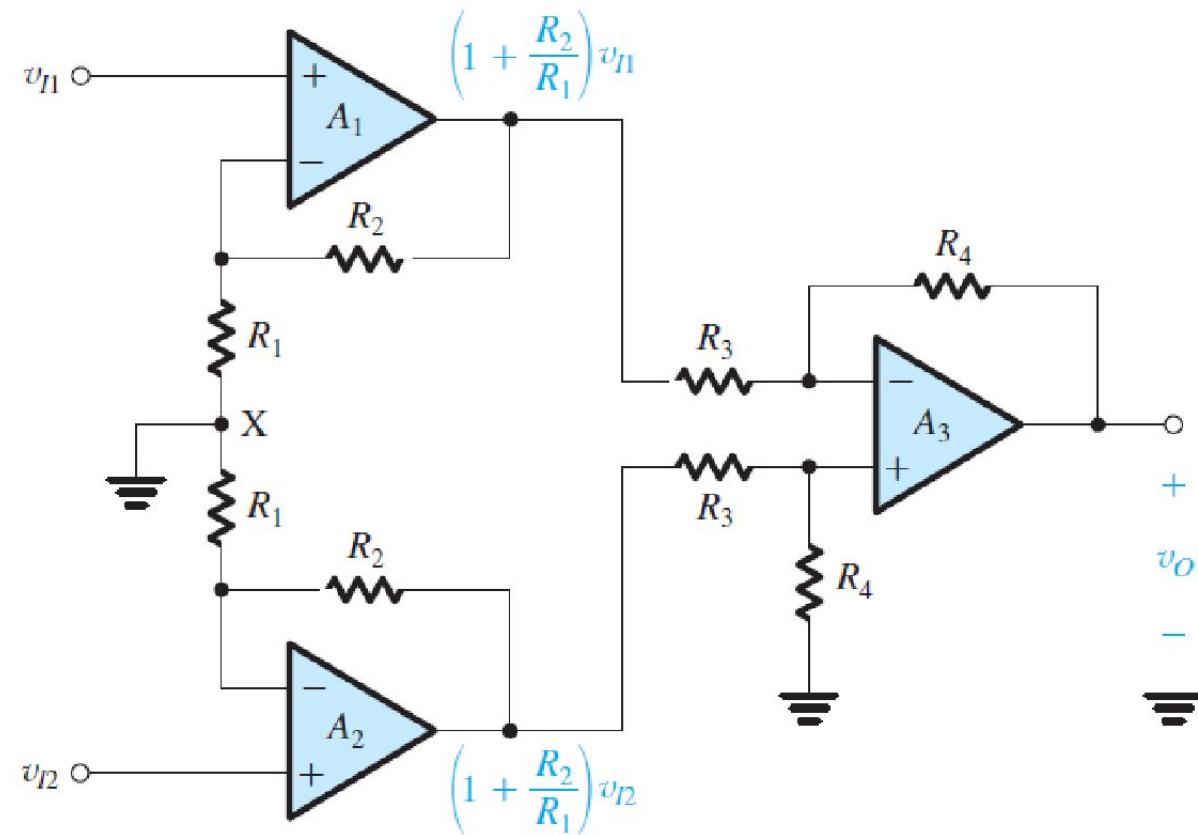
$$v_o = 2v_1$$

$$v_1 = 5 V$$

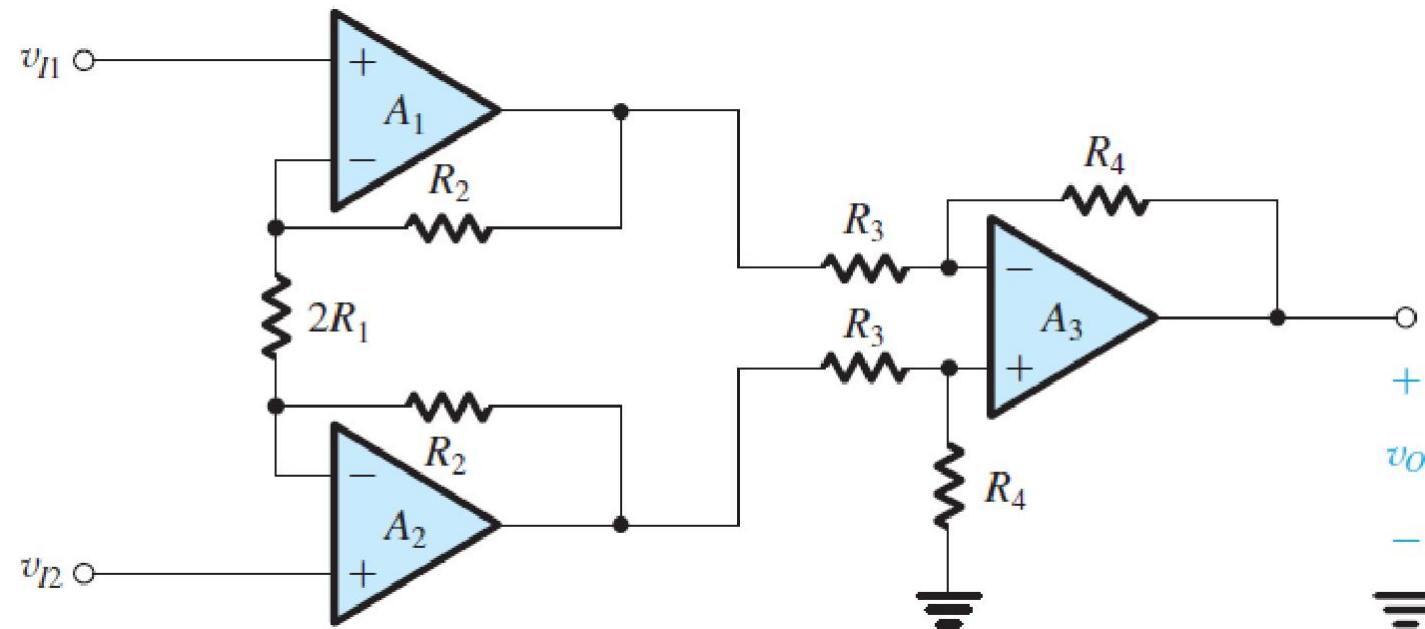
# Instrumentation Amplifier

- To address the low input resistance of the difference amplifier.

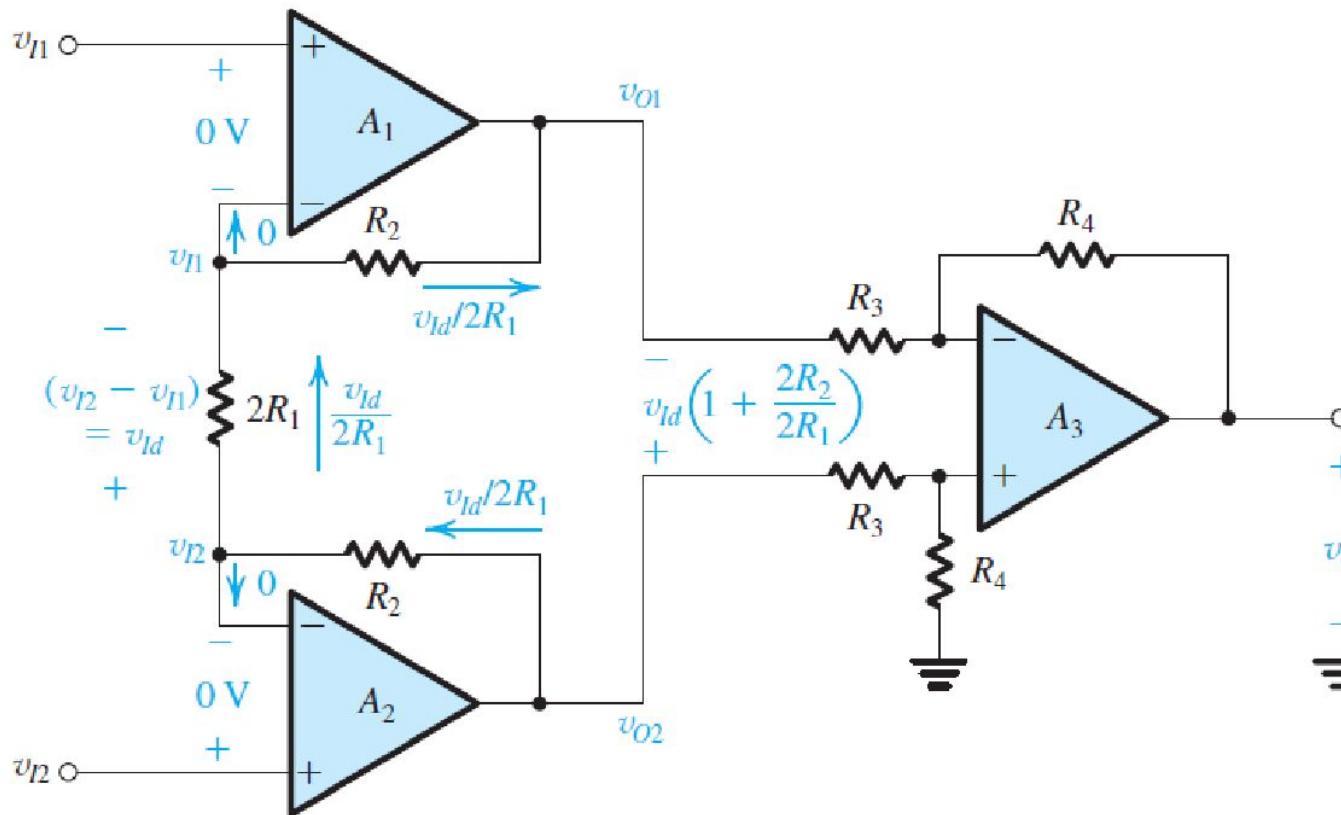
$$v_O = \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) v_{Id}$$



# Instrumentation Amplifier



# Instrumentation Amplifier



$$v_{O2} - v_{O1} = \left(1 + \frac{2R_2}{2R_1}\right)v_{Id}$$

$$A_d \equiv \frac{v_o}{v_{Id}} = \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right)$$

$$v_O = \frac{R_4}{R_3} \left( 1 + \frac{R_2}{R_1} \right) v_{ld}$$

$$A_d = \frac{R_4}{R_3} \left( 1 + \frac{R_2 + R'_2}{2R_1} \right)$$

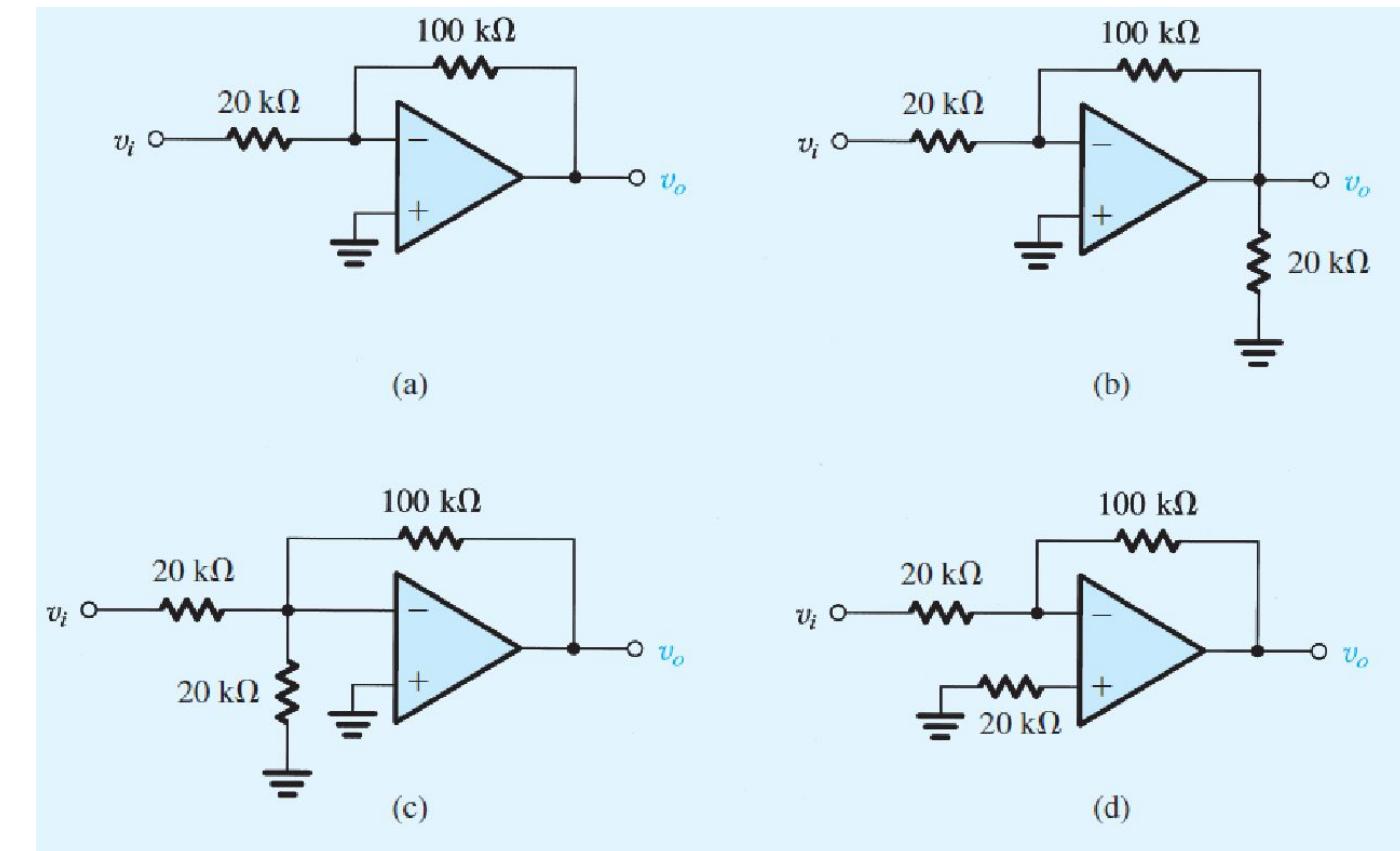


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# BEC Tutorial

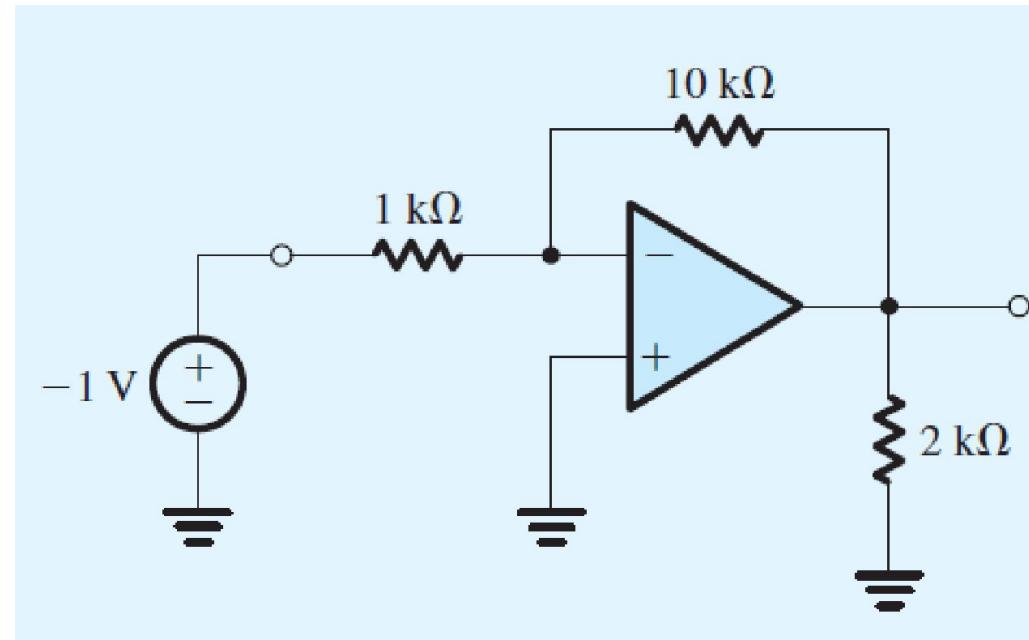
# Op-Amp

- Find  $v_o/v_i$  for each case, also find current through each resistor if  $v_i = 12 \text{ V}$ .



# Op-amp

- For the circuit given here, assuming an ideal op amp, find the currents through all branches and the voltages at all nodes.

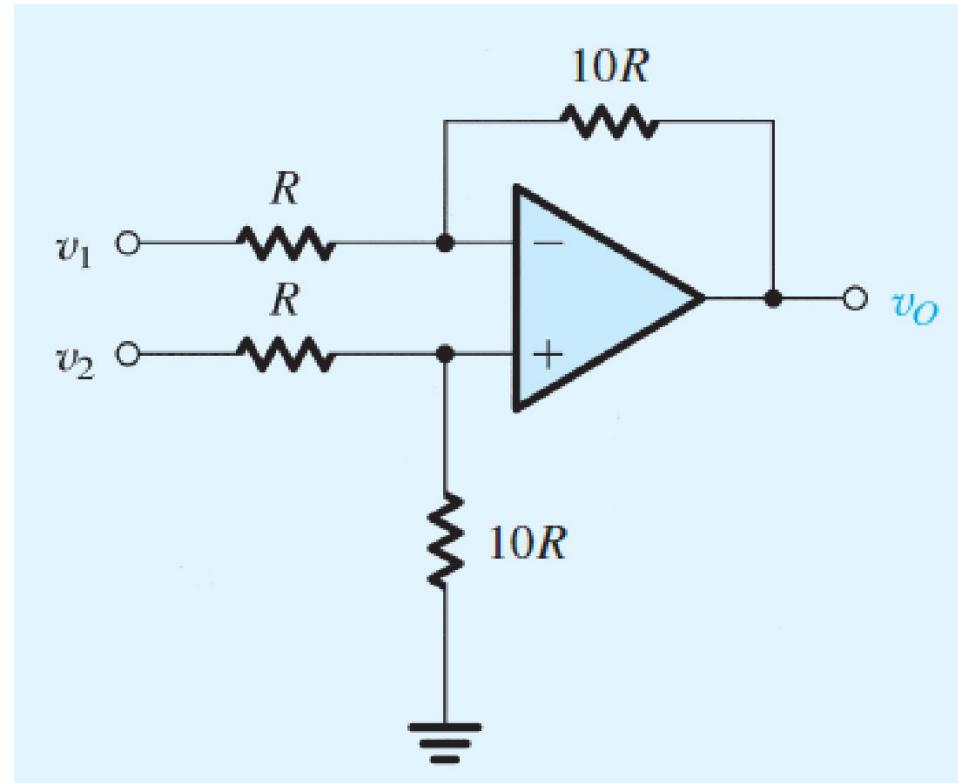


# Op-amp

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- design an op-amp circuit with inputs  $v_1$ ,  $v_2$ , and  $v_3$ , whose output is  $v_O = -(2v_1 + 4v_2 + 8v_3)$  using small resistors but no smaller than 1 k.
- Design a circuit based on the topology of the noninverting amplifier to obtain a gain of +1.5 V/V, using only 10-k resistors.

- For the circuit, use superposition to find  $v_O$  in terms of the input voltages  $v_1$  and  $v_2$ . Assume an ideal op amp. For
- $V_1 = 10\sin(2\pi \times 60t) - 0.1 \sin(2\pi \times 1000t)$ , volts
- $V_2 = 10\sin(2\pi \times 60t) + 0.1 \sin(2\pi \times 1000t)$ , volts
- find  $v_O$ .



# BASIC ELECTRONIC CIRCUITS

OP-AMP Applications: Active  
filters

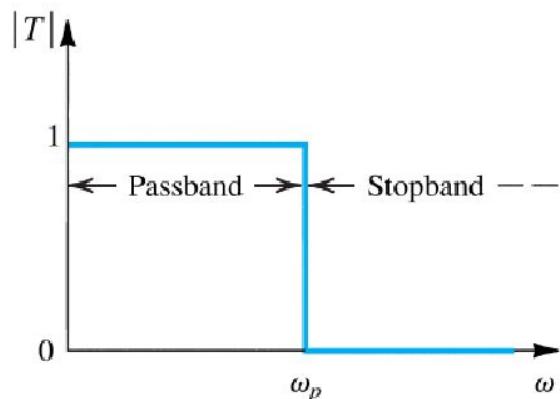
# contents

- Filter basics
- Brick wall responses
- Passive Vs Active filters
- RC passive filters
- Active filters

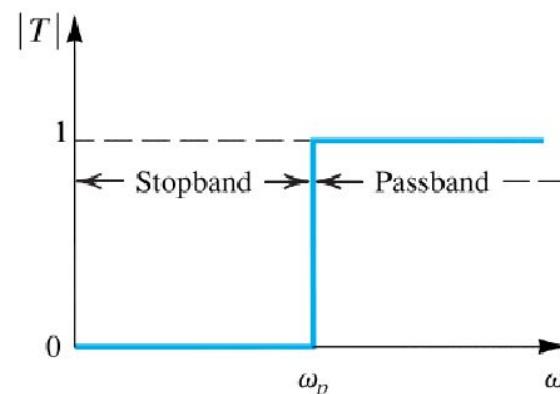
# Filters

- Pass band: A frequency band over which the magnitude of transmission is unity
- Stop band: A frequency band over which the magnitude of the transmission is zero.
- Major filter types are: Low pass, High pass, Band pass and Band reject

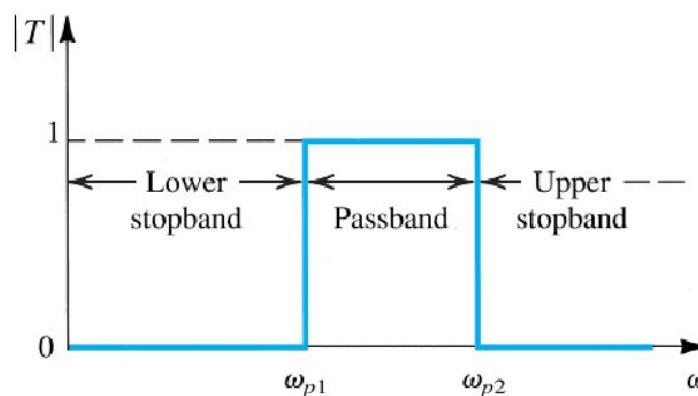
# Brick-wall responses of the filter types



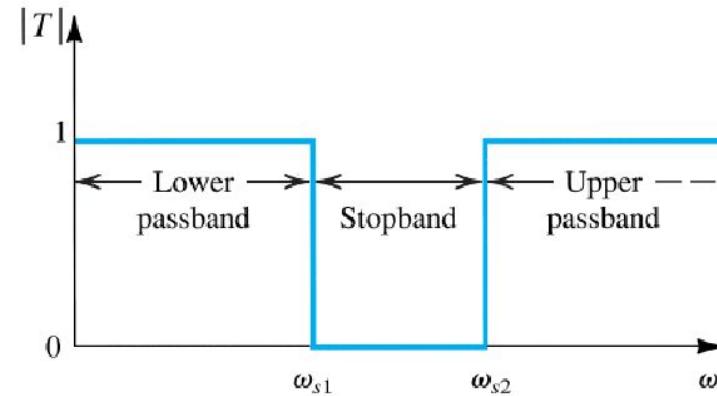
(a) Low-pass (LP)



(b) High-pass (HP)



(c) Bandpass (BP)



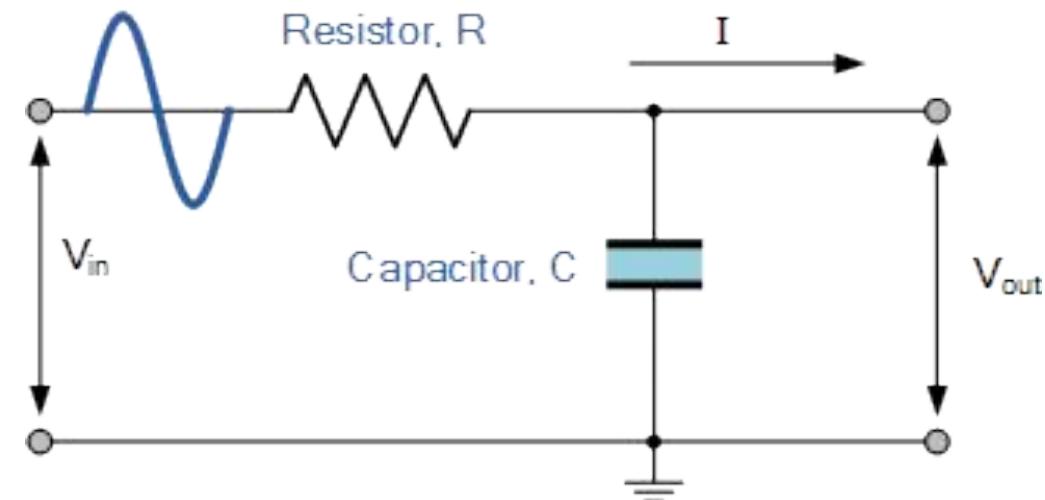
(d) Bandstop (BS)

# Passive Vs Active filters

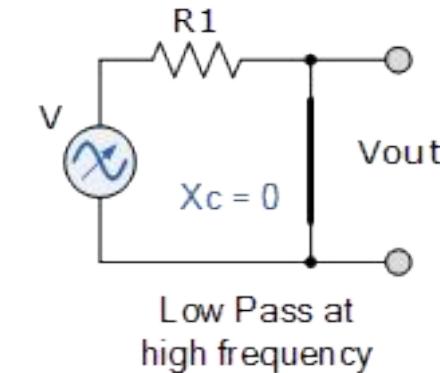
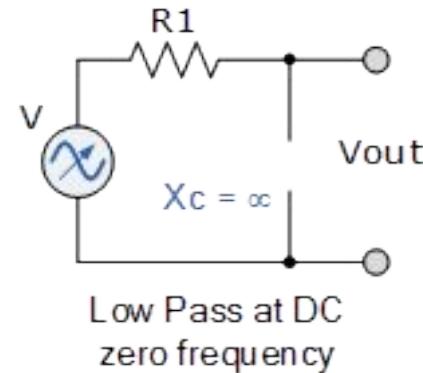
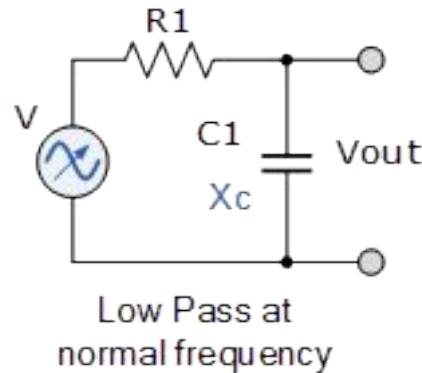
- **Passive filters** are made up of passive components such as resistors, capacitors and inductors and have no amplifying elements (transistors, op-amps, etc) so have no signal gain, therefore their output level is always less than the input.
- **Active filters** contain amplifying devices to increase signal strength while passive do not contain amplifying devices to strengthen the signal

# RC Low Pass Filter: Passive

- A Low Pass Filter is a circuit that can be designed to modify, reshape or reject all unwanted high frequencies of an electrical signal and accept or pass only those signals wanted by the circuits designer.



$$V_{out} = V_{in} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = V_{in} \frac{X_C}{Z}$$

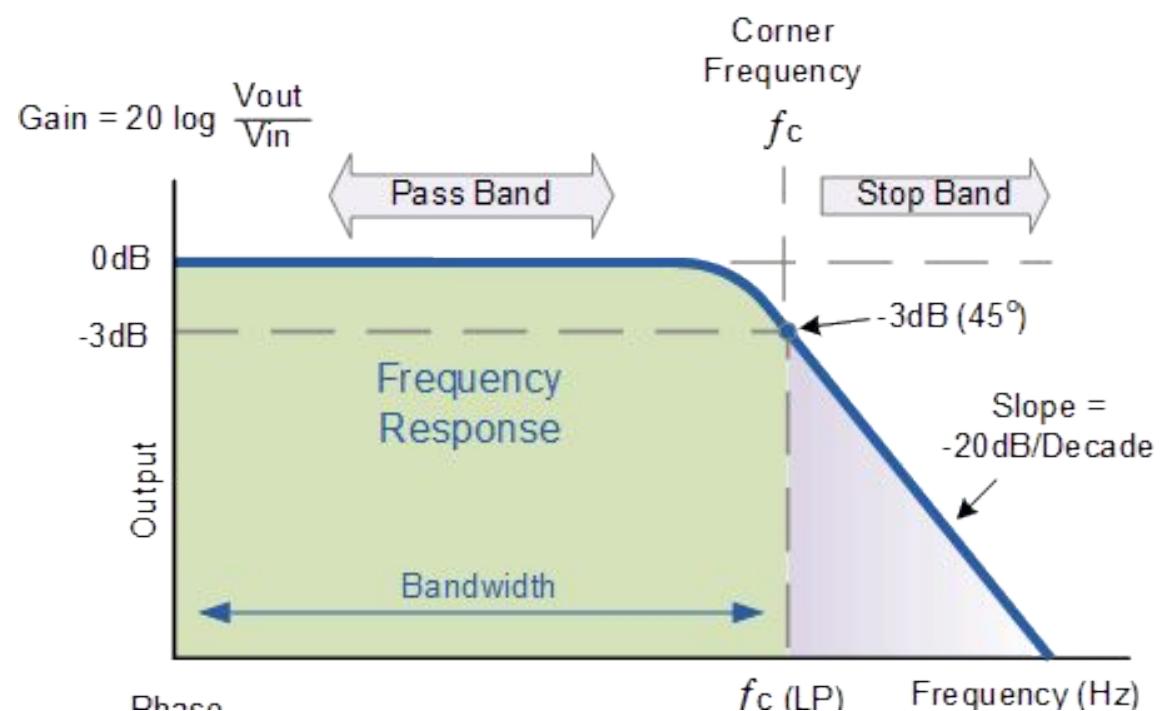


- $X_C$  - capacitive reactance, varies with applied frequency
- $X_C = 1/2\pi f C$
- Ex: A Low Pass Filter circuit consisting of a resistor of  $4.7k\Omega$  in series with a capacitor of  $47nF$  is connected across a  $10V$  sinusoidal supply. Calculate the output voltage ( $V_{OUT}$ ) at a frequency of  $100Hz$  and again at frequency of  $10kHz$ .

# Frequency Response:

- This "Cut-off", "Corner" or "Breakpoint" frequency is defined as being the frequency point where the capacitive reactance and resistance are equal,  $R = X_C$ .

$$f_C = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 4700 \times 47 \times 10^{-9}} = 720\text{Hz}$$



# Low Pass Active Filter

- Non inverting configuration

- Pass band gain 'G'

$$G = \left( 1 + \frac{R_2}{R_1} \right)$$

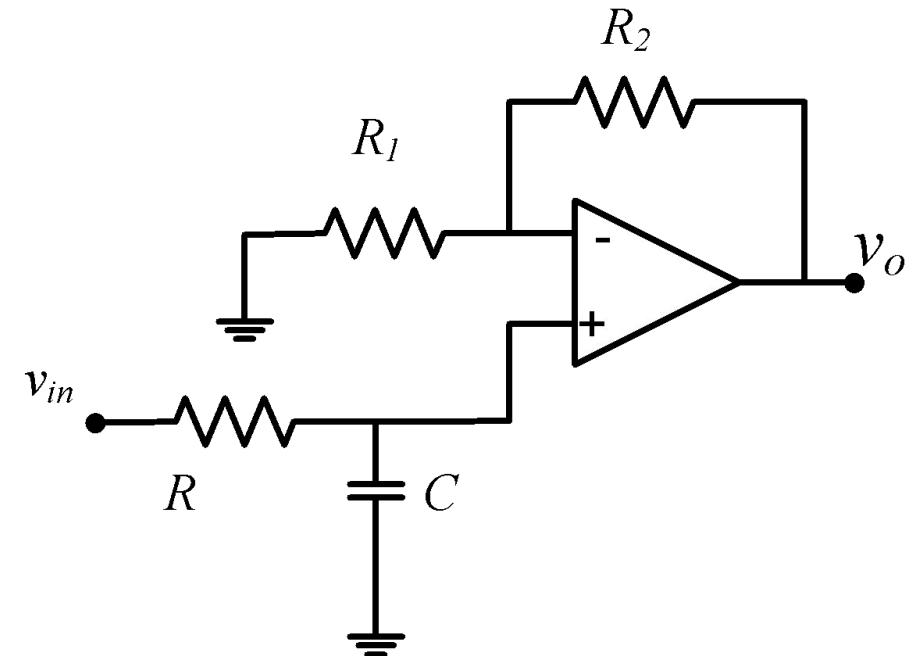
- At low freq.  $f < f_c$ :  $v_o \cong G v_{in}$

- At the cut-off freq.  $f = f_c$ :  $v_o \cong \frac{G}{\sqrt{2}} v_{in}$

- At high freq.  $f > f_c$ :

$$v_o < G v_{in}$$

$$f_c = \frac{1}{2\pi R C}$$

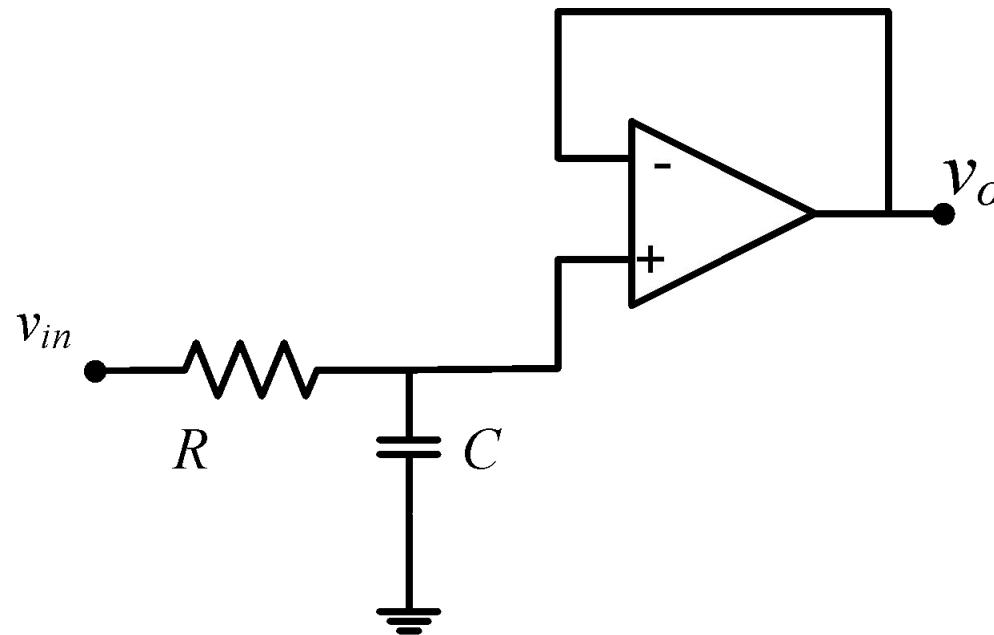


$$v_o = \frac{\left( 1 + \frac{R_2}{R_1} \right)}{\sqrt{1 + \left( \frac{f}{f_c} \right)^2}} v_{in}$$

$$\text{DC Gain} = \left( 1 + \frac{R_2}{R_1} \right)$$

# Low Pass Active Filter:

- Unit gain (Voltage follower)

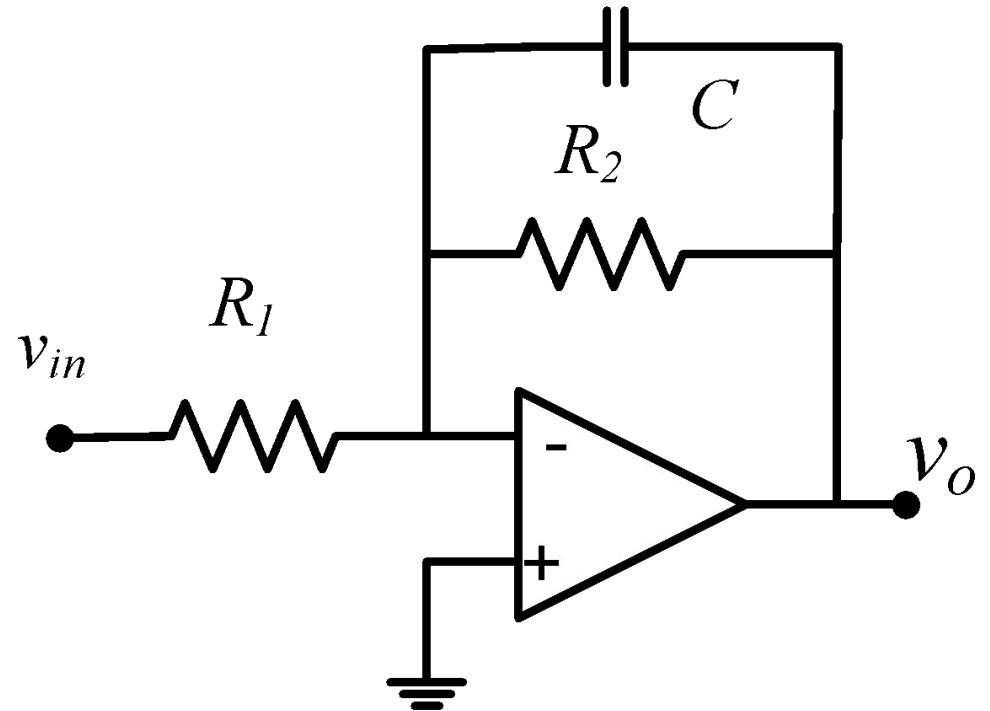


# Example:

- Design a non-inverting active low pass filter circuit that has a gain of ten at low frequencies, a high frequency cut-off or corner frequency of 159Hz and an input impedance of  $10\text{K}\Omega$ . Assume that the resistance in feed-in path is  $1\text{ K}\Omega$ . Determine the voltage gain at 100 Hz, 10kHz.
- Ans:  $R_2 = 9\text{K}\Omega$ ;  $C = 100 \text{ nF}$

# Low Pass Active Filter: Inverting configuration

- DC gain =  $-R_2/R_1$
- Integrator (in time domain)

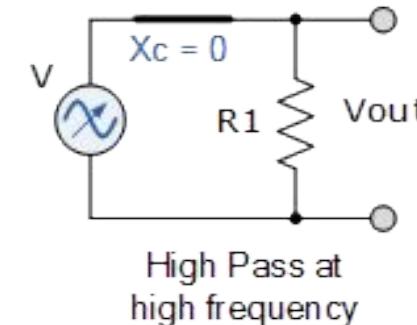
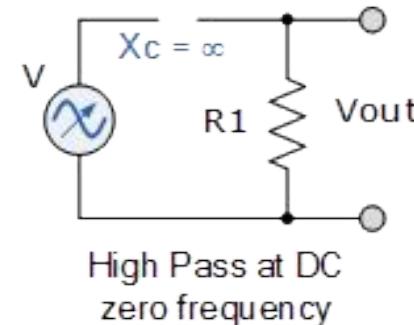
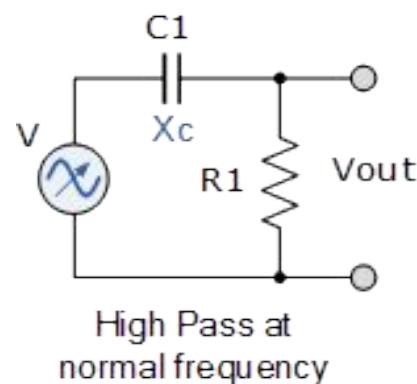
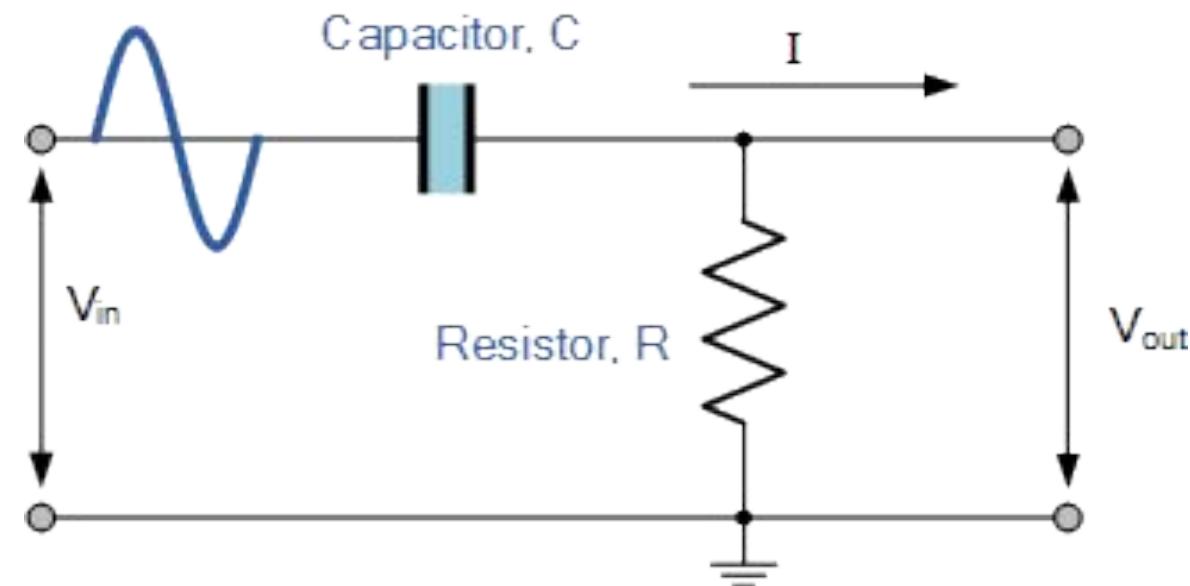


# BASIC ELECTRONIC CIRCUITS

OP-AMP Applications: Active  
filters

# High pass filter

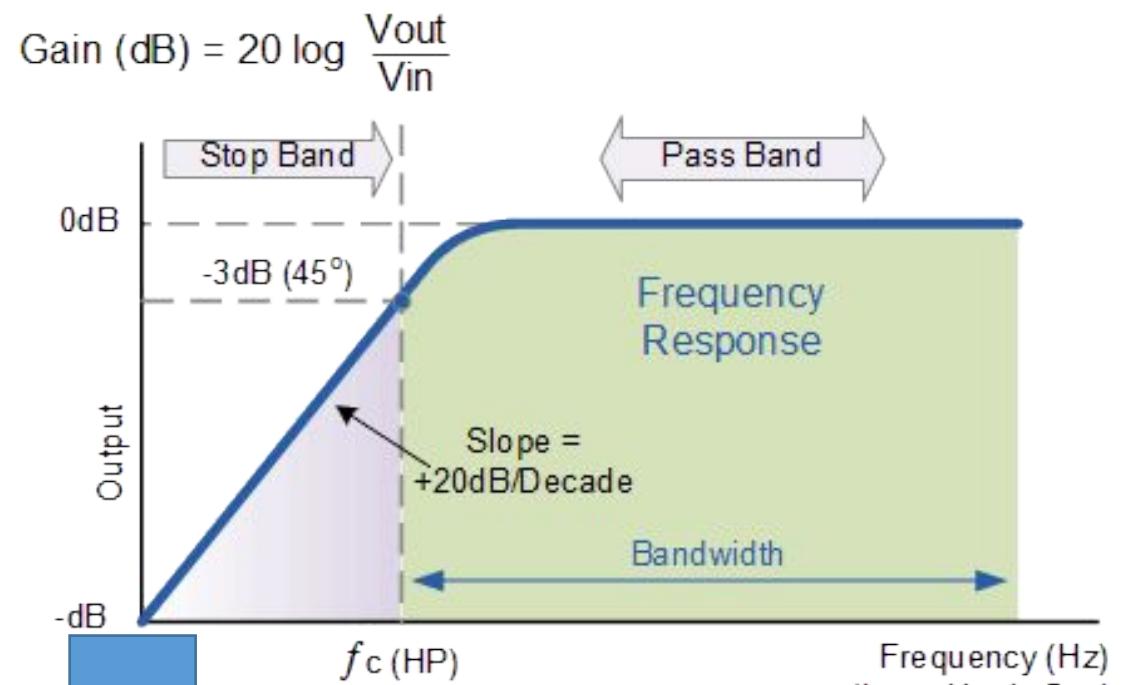
- A High Pass Filter response is the exact opposite to the low pass filter circuit as the two components have been interchanged with the filters output signal now being taken across the resistor.



# Frequency Response:

$$f_c = \frac{1}{2\pi RC}$$

- Calculate the cut-off or "breakpoint" frequency ( $f_c$ ) for a simple passive high pass filter consisting of an 82pF capacitor connected in series with a 240k $\Omega$  resistor.



$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R}{\sqrt{R^2 + X_c^2}} = \frac{R}{Z}$$

at low  $f$ :  $X_c \rightarrow \infty$ ,  $V_{out} = 0$   
at high  $f$ :  $X_c \rightarrow 0$ ,  $V_{out} = V_{in}$

# Active High Pass Filter

- Noninverting configuration

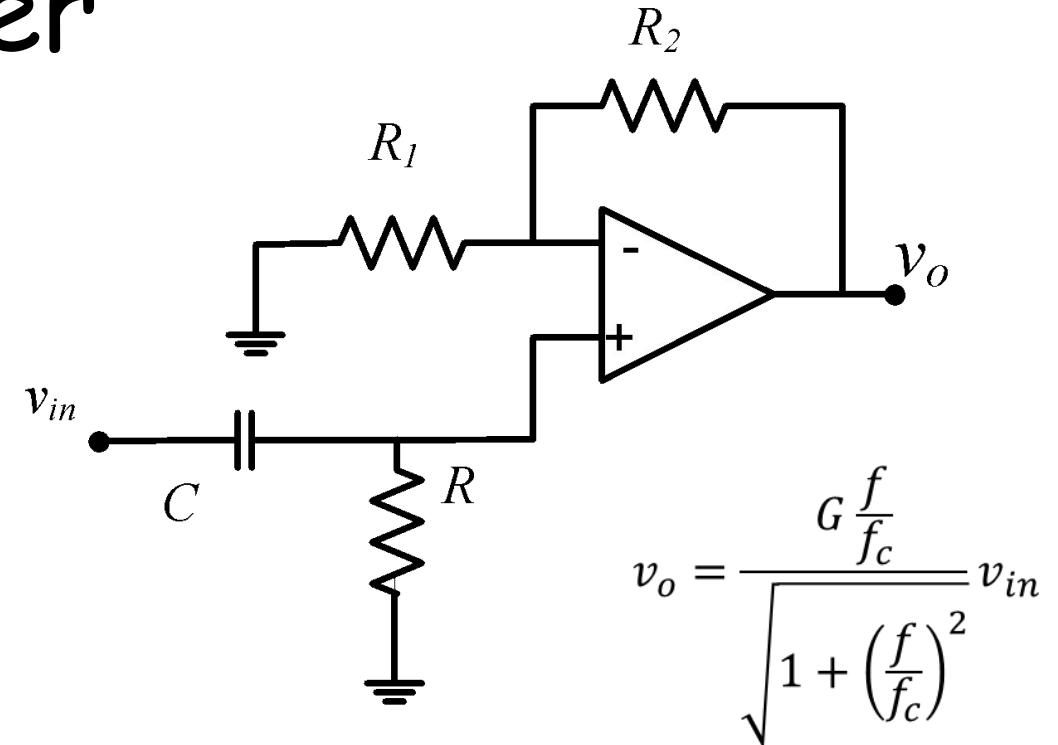
- Pass band gain

$$G = \left( 1 + \frac{R_2}{R_1} \right)$$

- At low freq.  $f < f_c$ :  $v_o < Gv_{in}$

- At the cut-off freq.  $f = f_c$ :  $v_o \cong \frac{G}{\sqrt{2}} v_{in}$

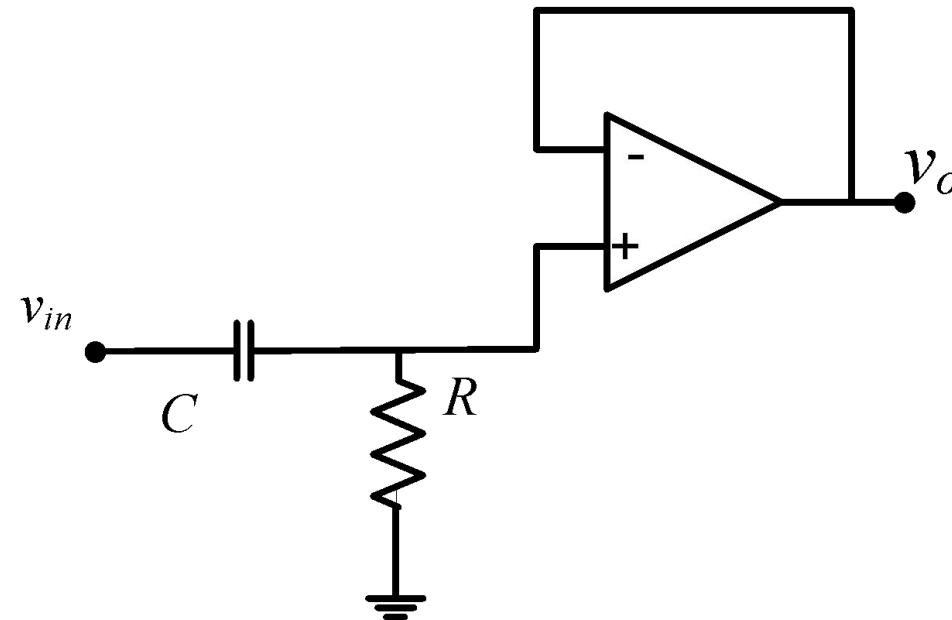
- At high freq.  $f > f_c$ :  $v_o \cong Gv_{in}$



$$f_c = \frac{1}{2\pi RC}$$

# High Pass Active Filter

- Unit gain

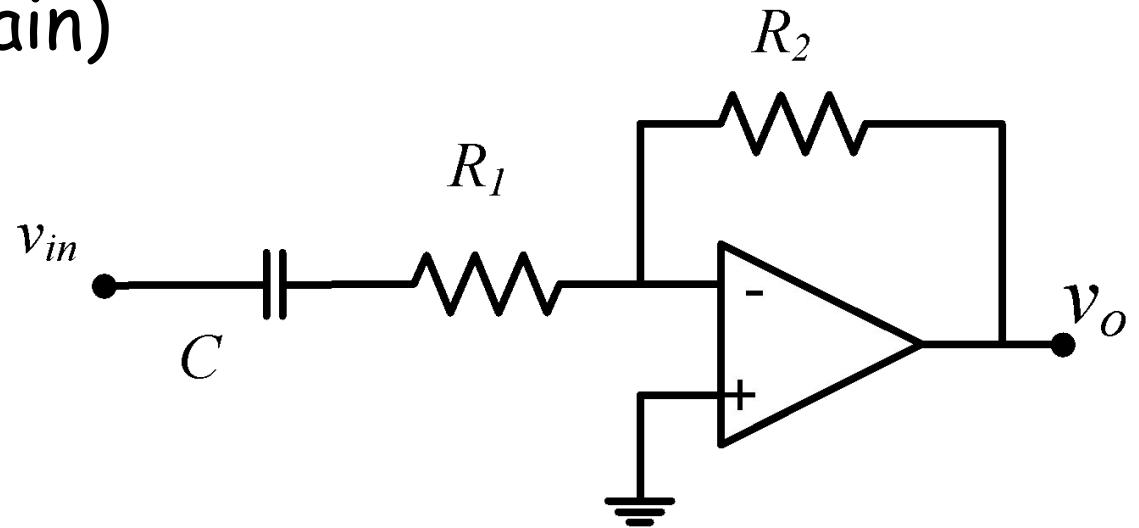


# Example:

- A first order active high pass filter has a pass band gain of two and a cut-off corner frequency of 1kHz. If the input capacitor has a value of  $10\text{nF}$ , calculate the value of the cut-off frequency determining resistor and if the feed in resistor is  $10 \text{ k}\Omega$  determine feedback resistance.
- Also determine the gain at 10 Hz, 100 Hz, 1KHz and 10 kHz.

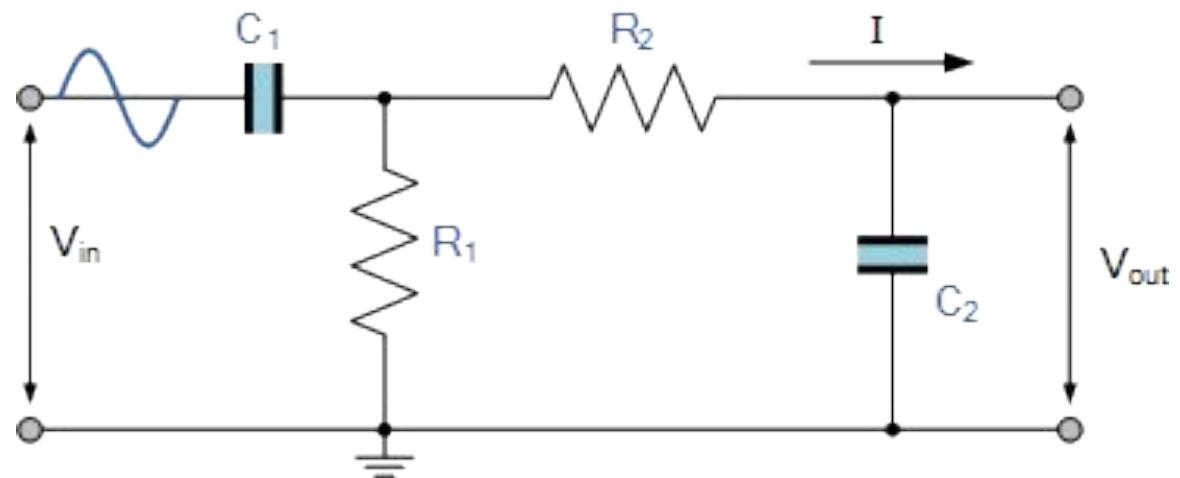
# High Pass Active Filter

- Inverting configuration
- Differentiator (time domain)



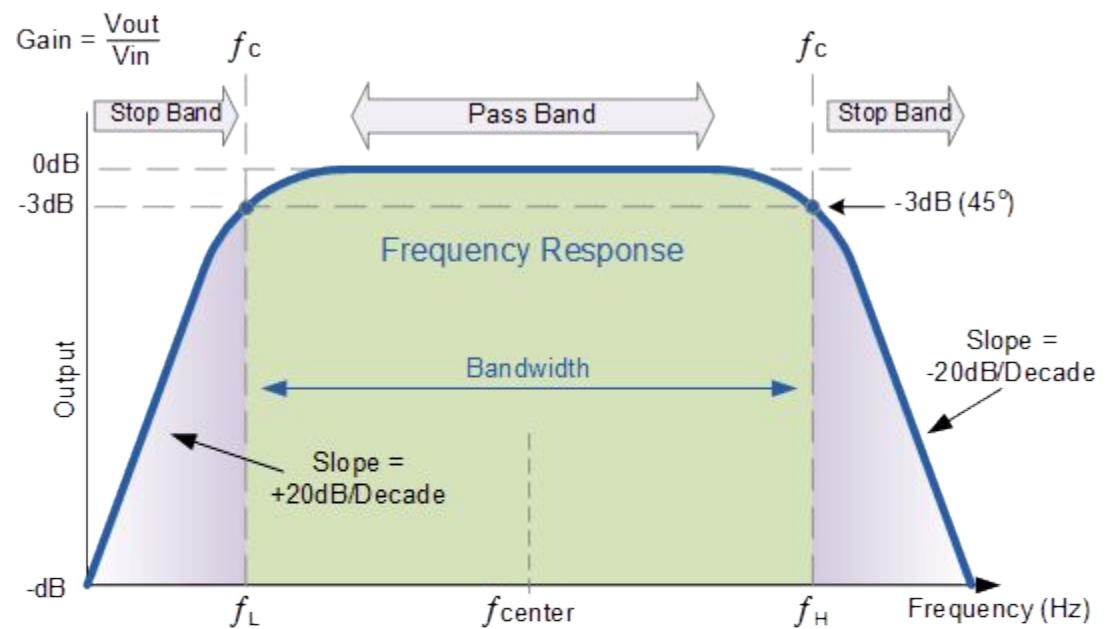
# Band pass filter

- Passive Band Pass Filters can be made by connecting together a low pass filter with a high pass filter



# Frequency Response:

- $f_L$  – cut off frequency of the high pass stage
- $f_H$  – cutoff frequency of the low pass stage
- Bandwidth =  $f_H - f_L$ .



$$fr = \sqrt{f_L \times f_H}$$

# BASIC ELECTRONIC CIRCUITS

OP-AMP Applications: Active  
filters

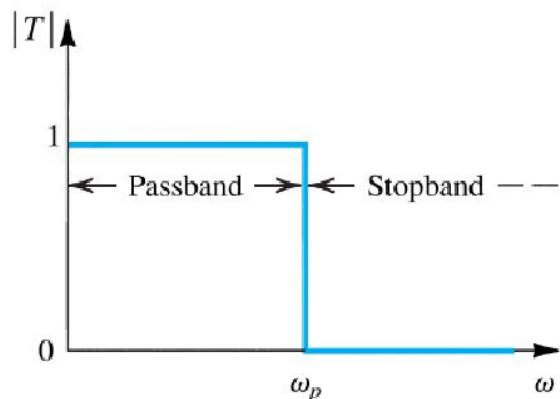
# contents

- Filter basics
- Brick wall responses
- Passive Vs Active filters
- RC passive filters
- Active filters

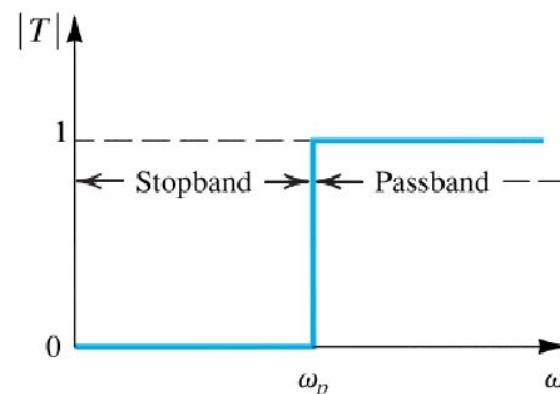
# Filters

- Pass band: A frequency band over which the magnitude of transmission is unity
- Stop band: A frequency band over which the magnitude of the transmission is zero.
- Major filter types are: Low pass, High pass, Band pass and Band reject

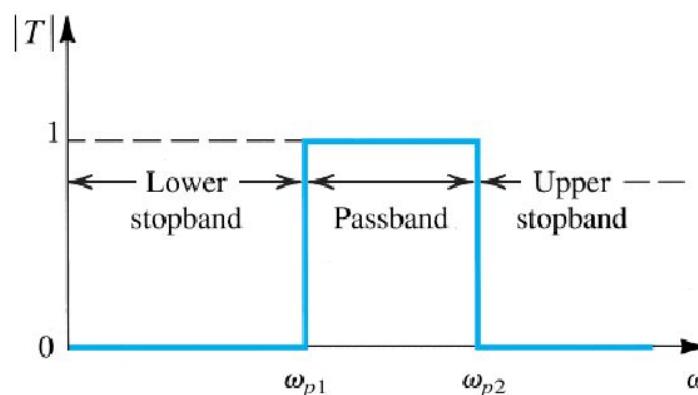
# Brick-wall responses of the filter types



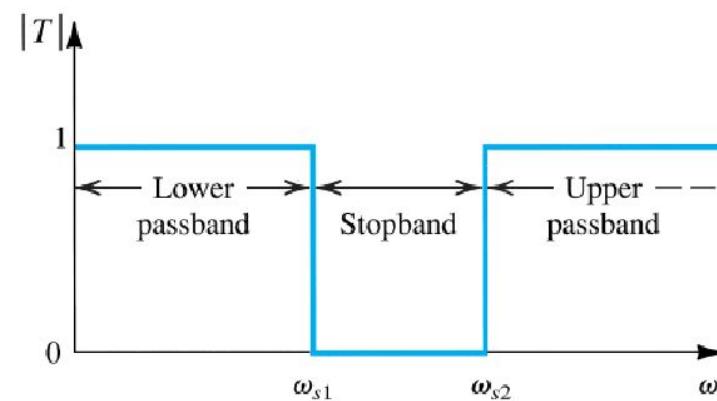
(a) Low-pass (LP)



(b) High-pass (HP)



(c) Bandpass (BP)



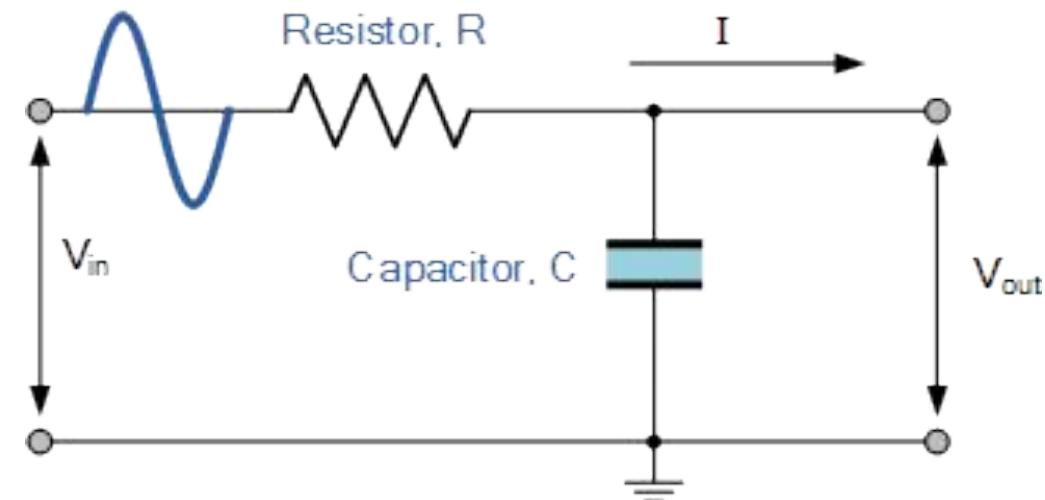
(d) Bandstop (BS)

# Passive Vs Active filters

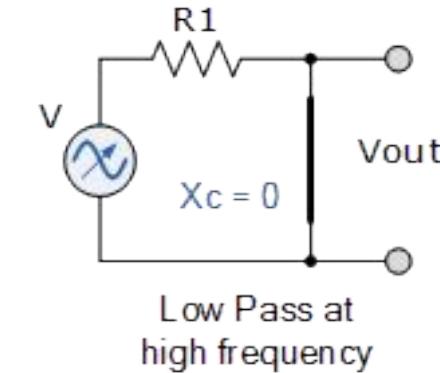
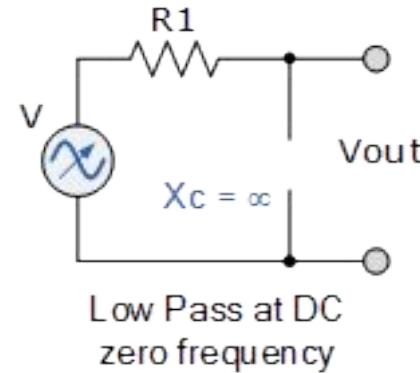
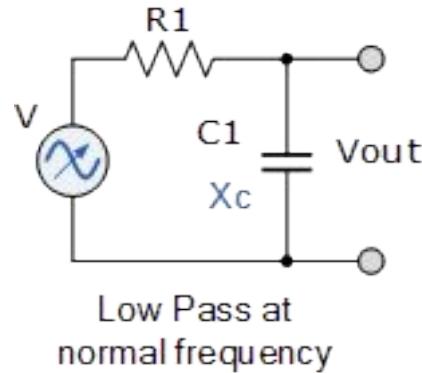
- **Passive filters** are made up of passive components such as resistors, capacitors and inductors and have no amplifying elements (transistors, op-amps, etc) so have no signal gain, therefore their output level is always less than the input.
- **Active filters** contain amplifying devices to increase signal strength while passive do not contain amplifying devices to strengthen the signal

# RC Low Pass Filter: Passive

- A Low Pass Filter is a circuit that can be designed to modify, reshape or reject all unwanted high frequencies of an electrical signal and accept or pass only those signals wanted by the circuits designer.



$$V_{out} = V_{in} \times \frac{X_C}{\sqrt{R^2 + X_C^2}} = V_{in} \frac{X_C}{Z}$$

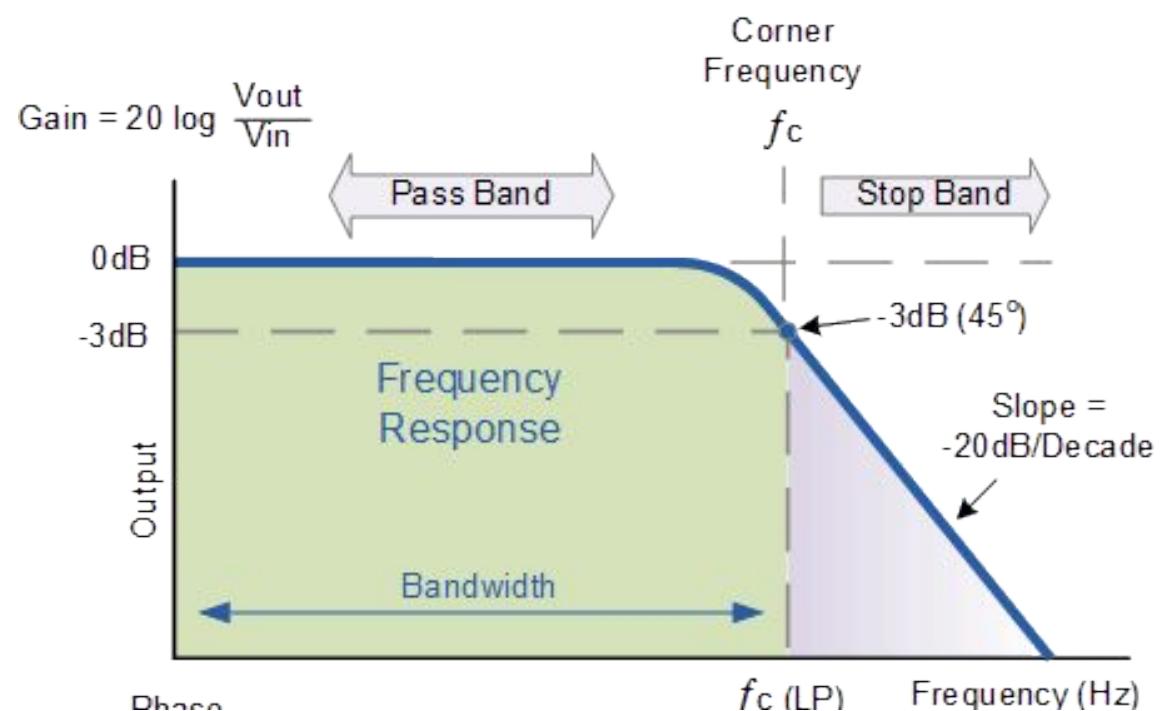


- $X_C$  - capacitive reactance, varies with applied frequency
- $X_C = 1/2\pi f C$
- Ex: A Low Pass Filter circuit consisting of a resistor of  $4.7k\Omega$  in series with a capacitor of  $47nF$  is connected across a  $10V$  sinusoidal supply. Calculate the output voltage ( $V_{OUT}$ ) at a frequency of  $100Hz$  and again at frequency of  $10kHz$ .

# Frequency Response:

- This "Cut-off", "Corner" or "Breakpoint" frequency is defined as being the frequency point where the capacitive reactance and resistance are equal,  $R = X_C$ .

$$f_C = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 4700 \times 47 \times 10^{-9}} = 720\text{Hz}$$



# Low Pass Active Filter

- Non inverting configuration

- Pass band gain 'G'

$$G = \left( 1 + \frac{R_2}{R_1} \right)$$

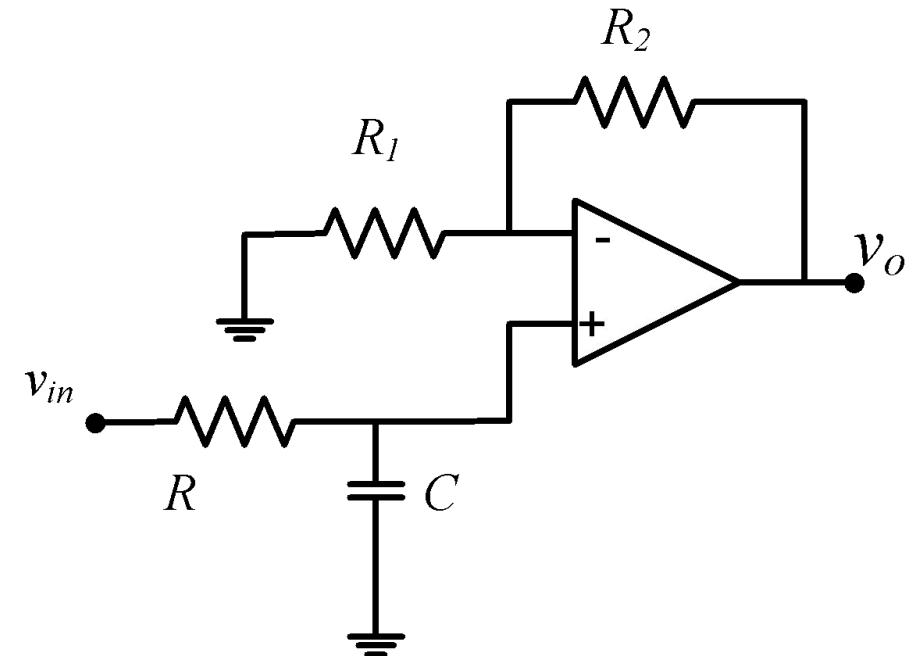
- At low freq.  $f < f_c$ :  $v_o \cong G v_{in}$

- At the cut-off freq.  $f = f_c$ :  $v_o \cong \frac{G}{\sqrt{2}} v_{in}$

- At high freq.  $f > f_c$ :

$$v_o < G v_{in}$$

$$f_c = \frac{1}{2\pi R C}$$

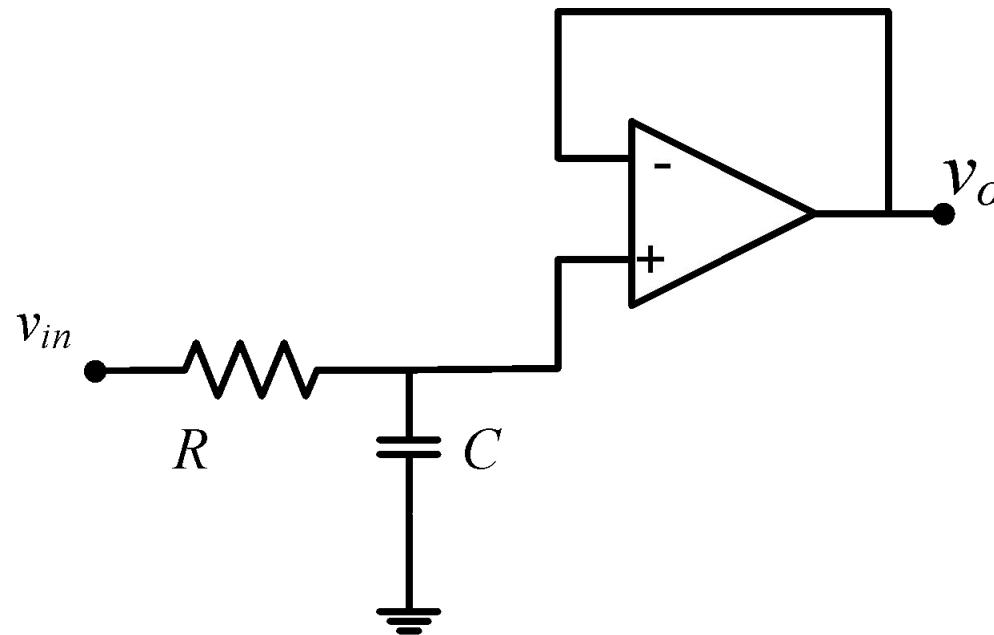


$$v_o = \frac{\left( 1 + \frac{R_2}{R_1} \right)}{\sqrt{1 + \left( \frac{f}{f_c} \right)^2}} v_{in}$$

$$\text{DC Gain} = \left( 1 + \frac{R_2}{R_1} \right)$$

# Low Pass Active Filter:

- Unit gain (Voltage follower)

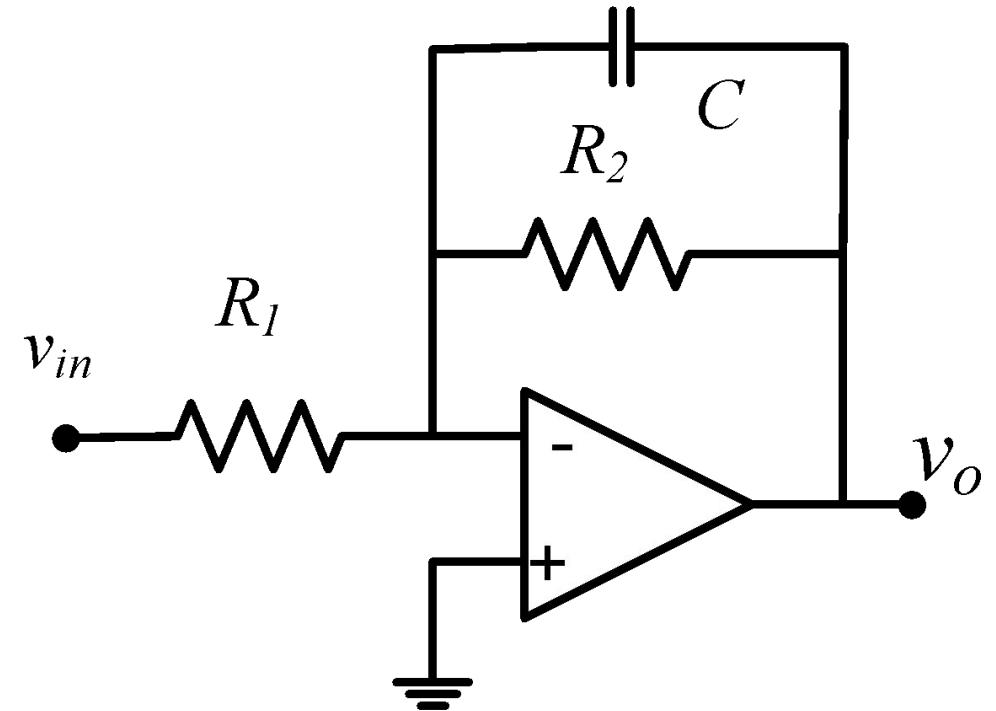


# Example:

- Design a non-inverting active low pass filter circuit that has a gain of ten at low frequencies, a high frequency cut-off or corner frequency of 159Hz and an input impedance of  $10\text{K}\Omega$ . Assume that the resistance in feed-in path is  $1\text{ K}\Omega$ . Determine the voltage gain at 100 Hz, 10kHz.
- Ans:  $R_2 = 9\text{K}\Omega$ ;  $C = 100 \text{ nF}$

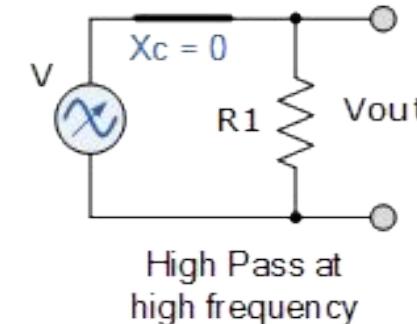
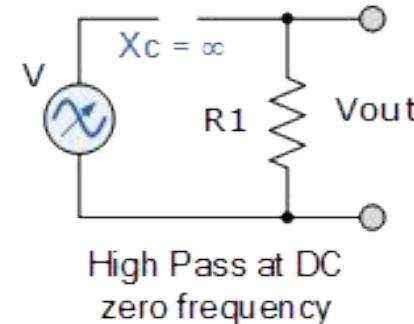
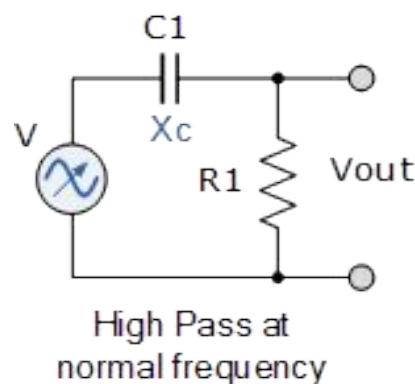
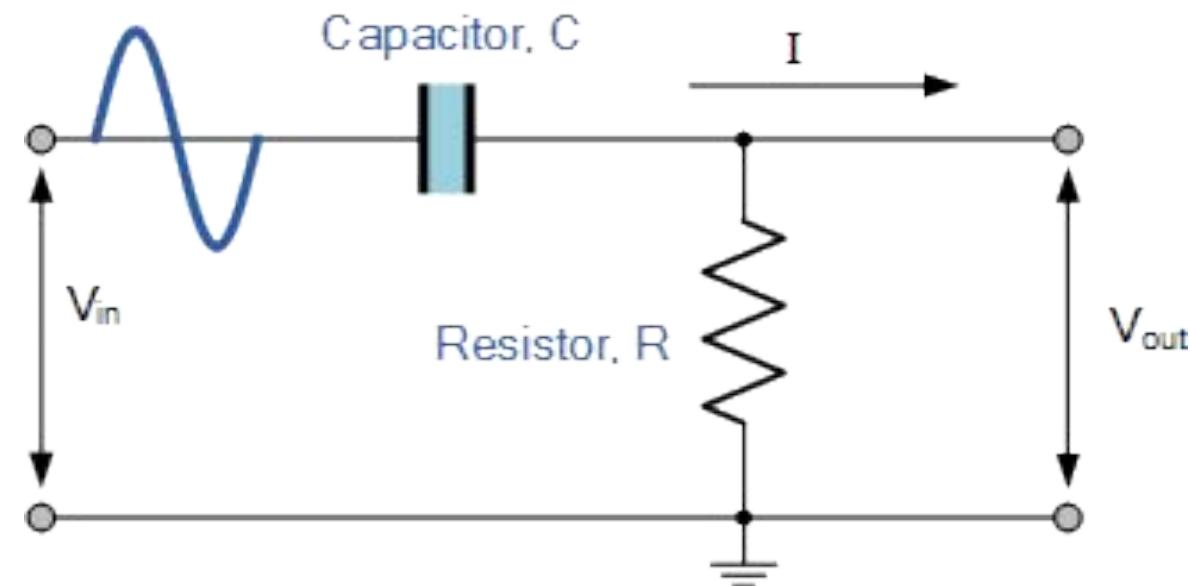
# Low Pass Active Filter: Inverting configuration

- DC gain =  $-R_2/R_1$
- Integrator (in time domain)



# High pass filter

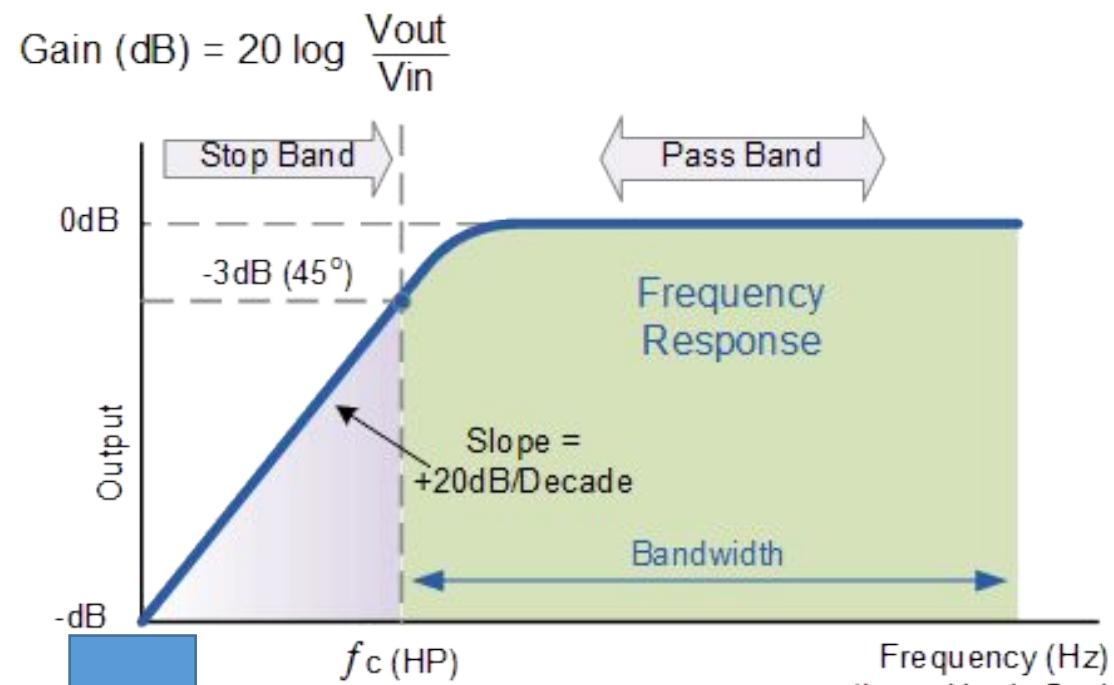
- A High Pass Filter response is the exact opposite to the low pass filter circuit as the two components have been interchanged with the filters output signal now being taken across the resistor.



# Frequency Response:

$$f_c = \frac{1}{2\pi RC}$$

- Calculate the cut-off or "breakpoint" frequency ( $f_c$ ) for a simple passive high pass filter consisting of an 82pF capacitor connected in series with a 240k $\Omega$  resistor.



$$A_V = \frac{V_{OUT}}{V_{IN}} = \frac{R}{\sqrt{R^2 + X_c^2}} = \frac{R}{Z}$$

at low  $f$ :  $X_c \rightarrow \infty$ ,  $V_{out} = 0$   
at high  $f$ :  $X_c \rightarrow 0$ ,  $V_{out} = V_{in}$

# Active High Pass Filter

- Noninverting configuration

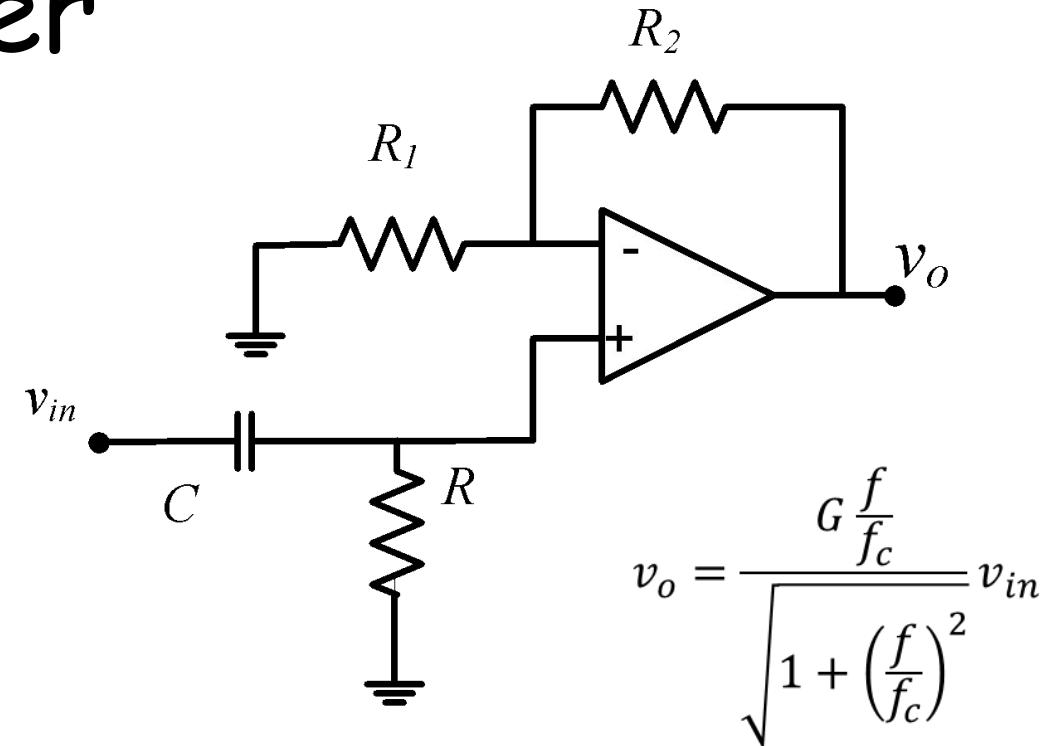
- Pass band gain

$$G = \left( 1 + \frac{R_2}{R_1} \right)$$

- At low freq.  $f < f_c$ :  $v_o < Gv_{in}$

- At the cut-off freq.  $f = f_c$ :  $v_o \approx \frac{G}{\sqrt{2}} v_{in}$

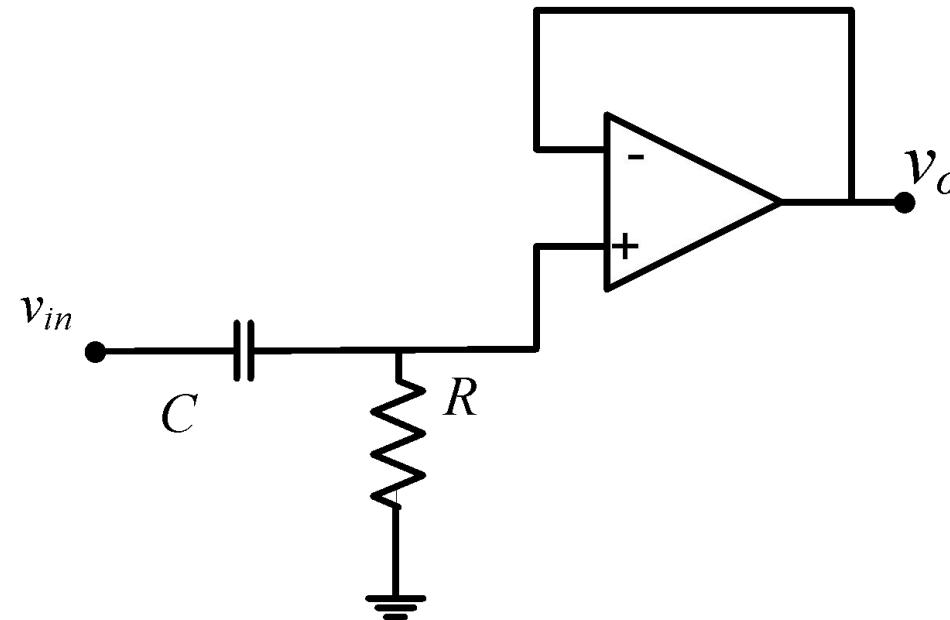
- At high freq.  $f > f_c$ :  $v_o \approx Gv_{in}$



$$f_c = \frac{1}{2\pi RC}$$

# High Pass Active Filter

- Unit gain

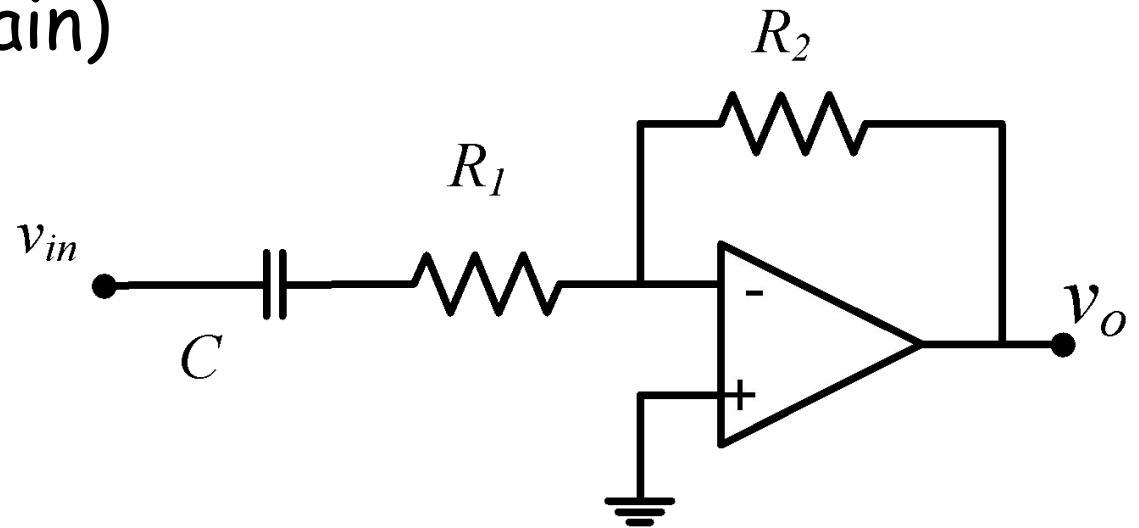


# Example:

- A first order active high pass filter has a pass band gain of two and a cut-off corner frequency of 1kHz. If the input capacitor has a value of  $10\text{nF}$ , calculate the value of the cut-off frequency determining resistor and if the feed in resistor is  $10 \text{ k}\Omega$  determine feedback resistance.
- Also determine the gain at 10 Hz, 100 Hz, 1KHz and 10 kHz.

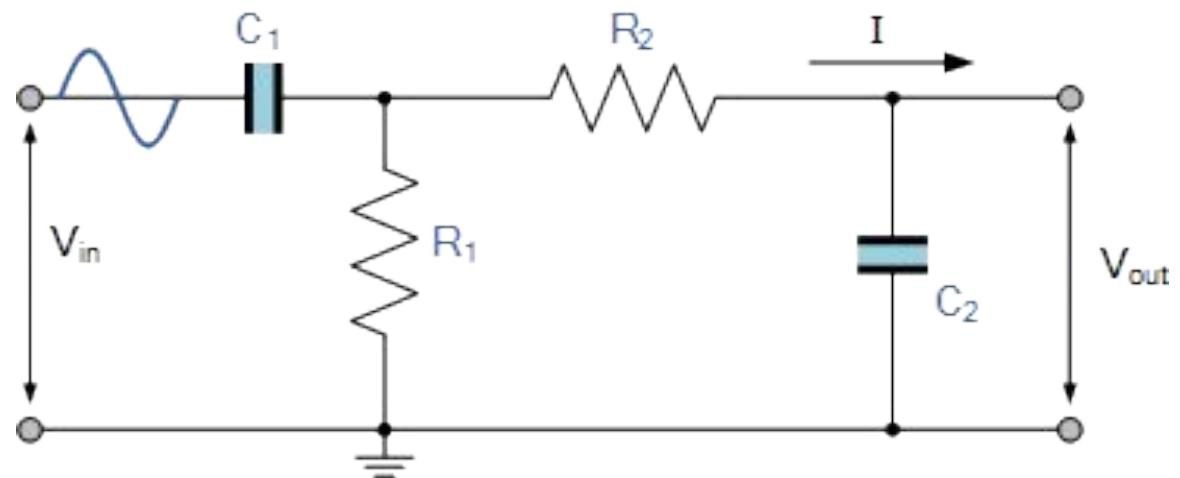
# High Pass Active Filter

- Inverting configuration
- Differentiator (time domain)



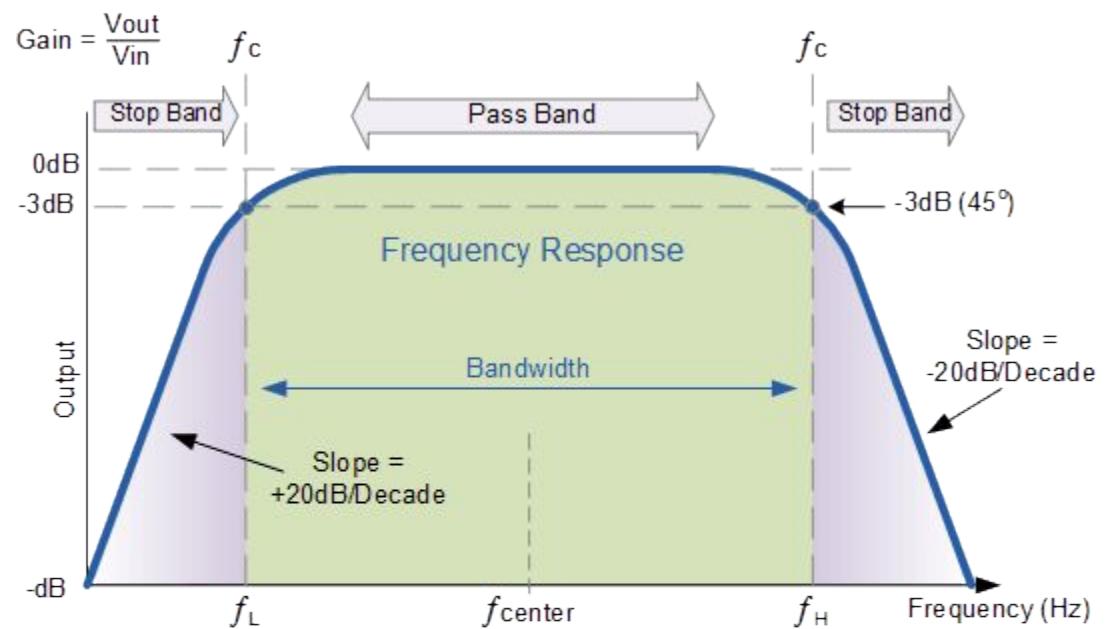
# Band pass filter

- Passive Band Pass Filters can be made by connecting together a low pass filter with a high pass filter



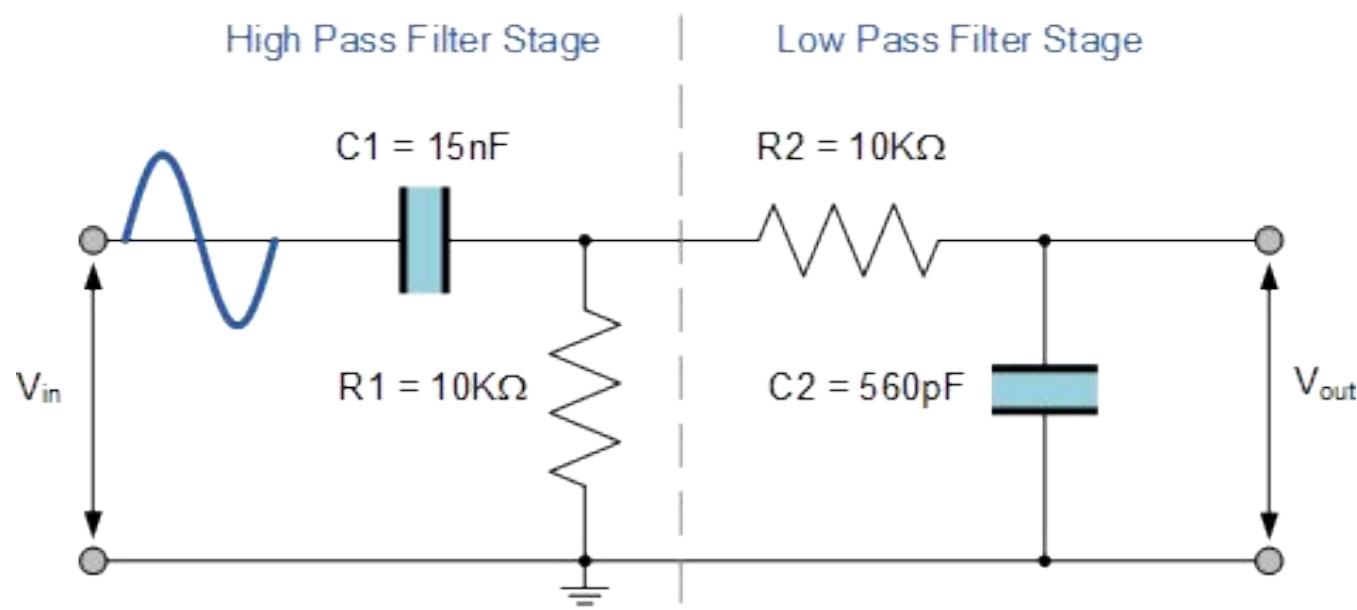
# Frequency Response:

- $f_L$  – cut off frequency of the high pass stage
- $f_H$  – cutoff frequency of the low pass stage
- Bandwidth =  $f_H - f_L$ .



$$fr = \sqrt{f_L \times f_H}$$

- Ex: A second-order band pass filter is to be constructed using RC components that will only allow a range of frequencies to pass above 1kHz (1,000Hz) and below 30kHz (30,000Hz). Assuming that both the resistors have values of  $10\text{k}\Omega$ , calculate the values of the two capacitors required.



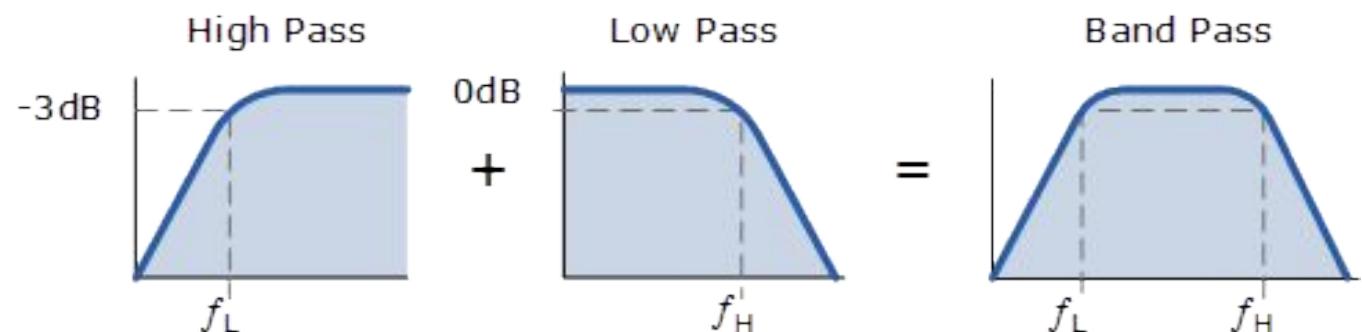
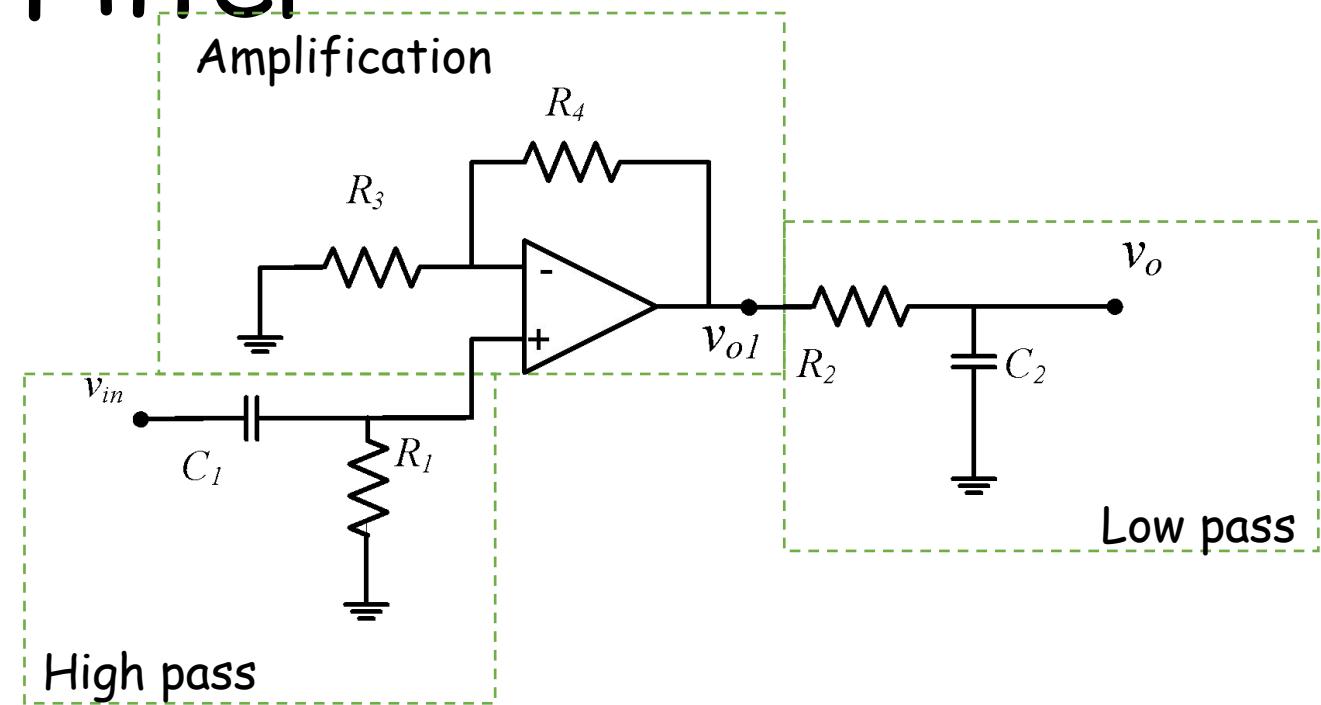
# Band pass Active Filter

- Non inverting configuration

$$v_o = \frac{\left(1 + \frac{R_4}{R_3}\right)}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \frac{f}{f_L} \frac{1}{\sqrt{1 + \left(\frac{f}{f_L}\right)^2}} v_{in}$$

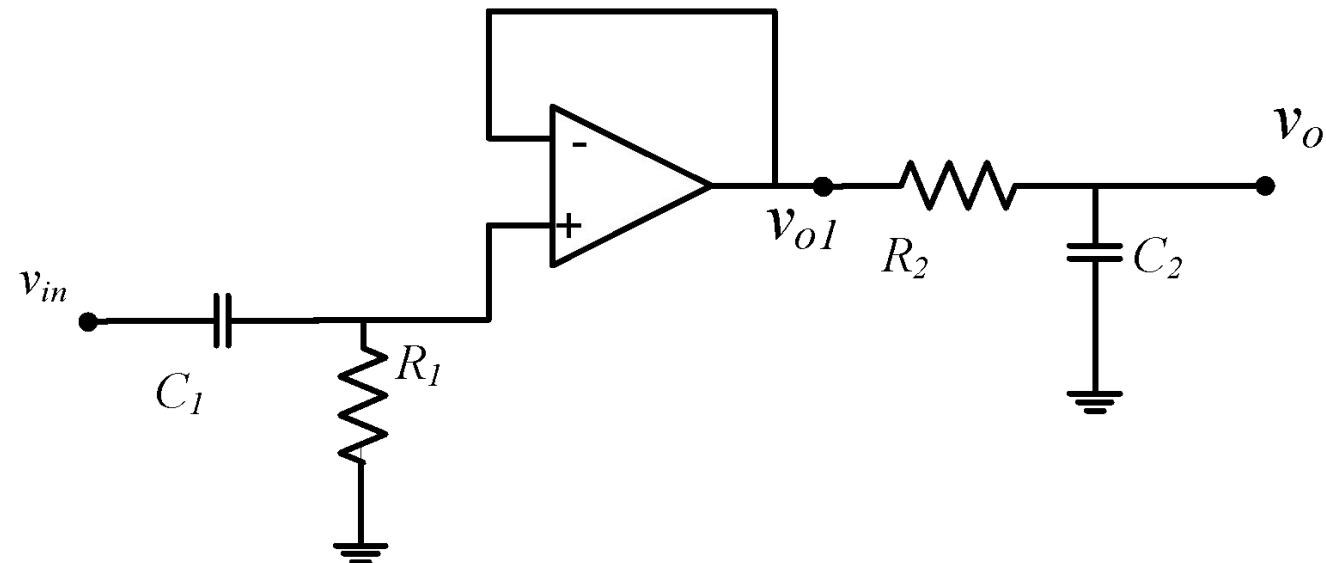
$$f_L = \frac{1}{2\pi R_1 C_1} \quad f_H = \frac{1}{2\pi R_2 C_2}$$

$$f_r = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$



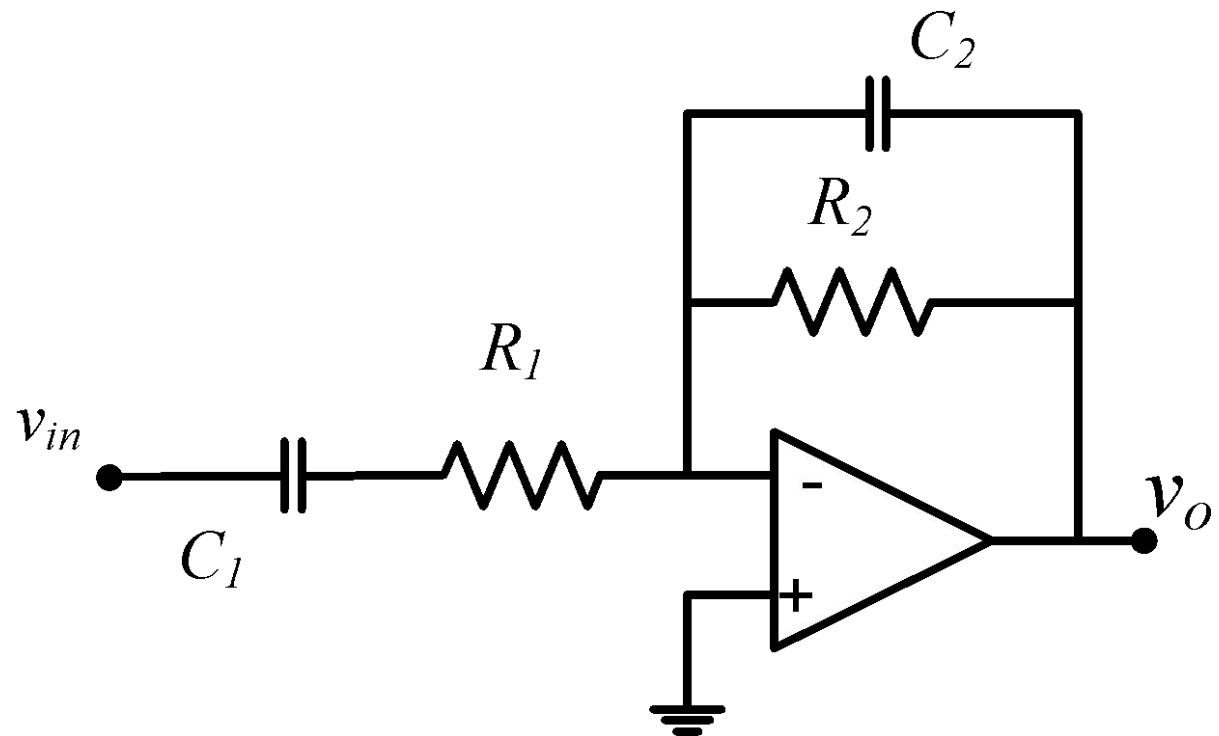
# Band pass active filter

- Unit Gain (Voltage follower)



# Band Pass Active Filter

- Inverting Configuration



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# Op-Amp as Integrator and Differentiator

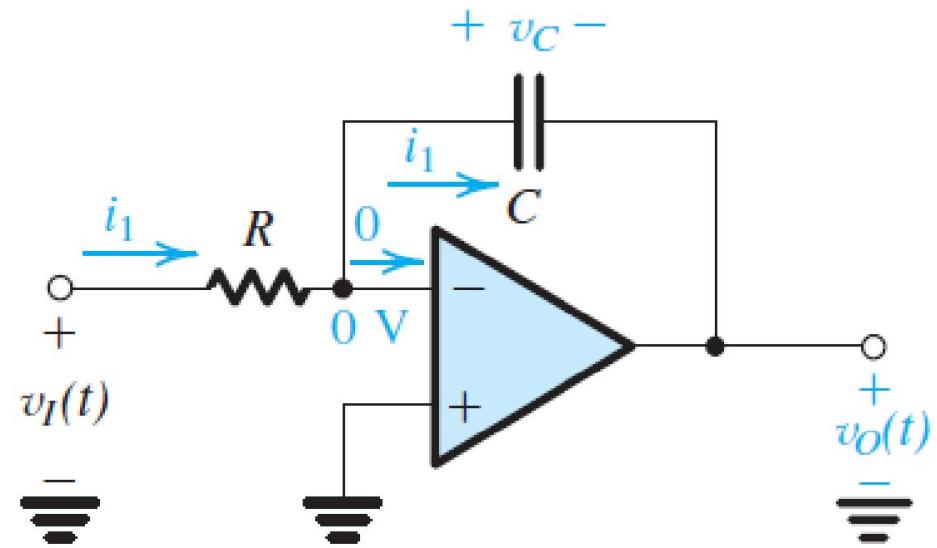




# The Inverting Integrator

$$v_C(t) = V_C + \frac{1}{C} \int_0^t i_1(t) dt$$

$$v_O(t) = -\frac{1}{CR} \int_0^t v_I(t) dt - V_C$$



$$\frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{1}{j\omega CR}$$

$$\left| \frac{V_o}{V_i} \right| = \frac{1}{\omega CR}$$

# Example:

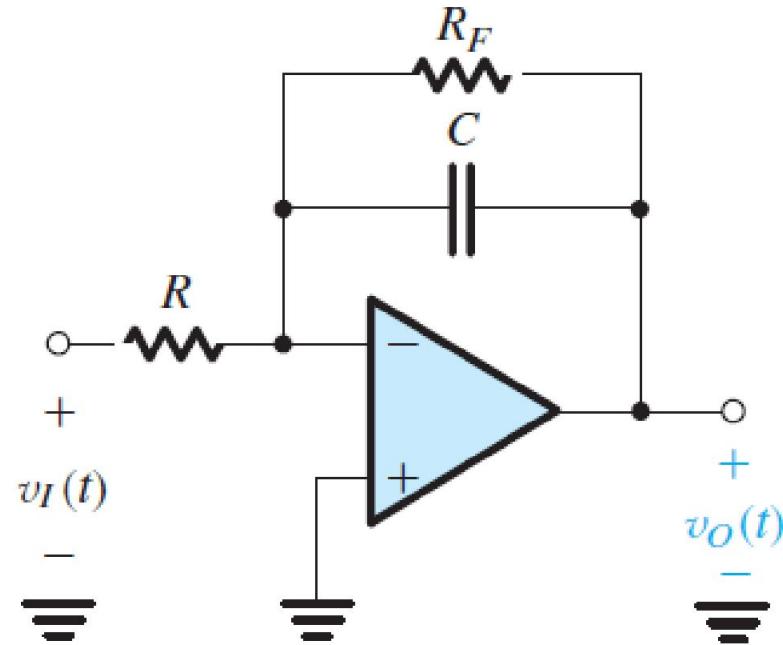
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- Use an ideal op-amp to design an inverting integrator with an input resistance of  $10\text{ k}\Omega$  and an integration time constant of  $10^{-3}\text{ s}$ . What is the gain magnitude and phase angle of this circuit at  $10\text{ rad/s}$  and at  $1\text{ rad/s}$ ? What is the frequency at which the gain magnitude is unity?

# Circuit with finite gain at DC

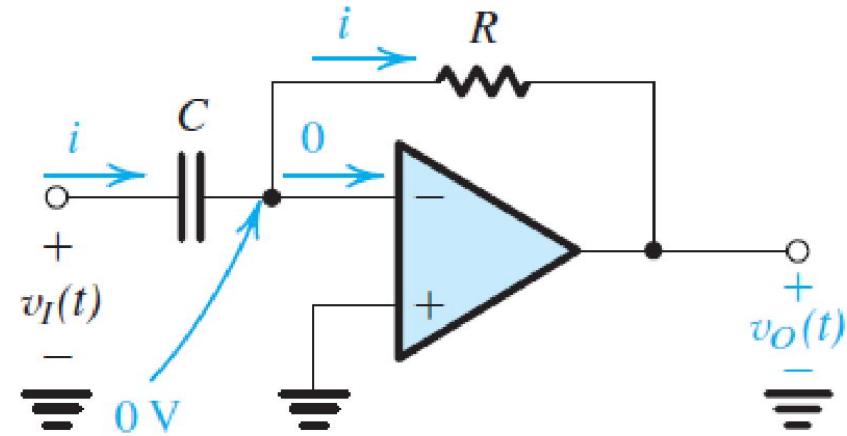
$$V_o = -\frac{1}{j\omega RC + R/R_F} V_i$$

$$\left| \frac{V_o}{V_i} \right| = \frac{R_F/R}{\sqrt{1 + (\omega R_F C)^2}}$$



# Differentiator Circuit

$$V_o = -j\omega RC_F V_i$$



# Example:

---

- Design a differentiator to have a time constant of  $10^{-2}$  s and an input capacitance of  $0.01 \mu\text{F}$ . What is the gain magnitude and phase of this circuit at  $10 \text{ rad/s}$ , and at  $10^3 \text{ rad/s}$ ? In order to limit the high-frequency gain of the differentiator circuit to 100, a resistor is added in series with the capacitor. Find the required resistor value.



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# OP-AMP based Waveform Generators

# Content

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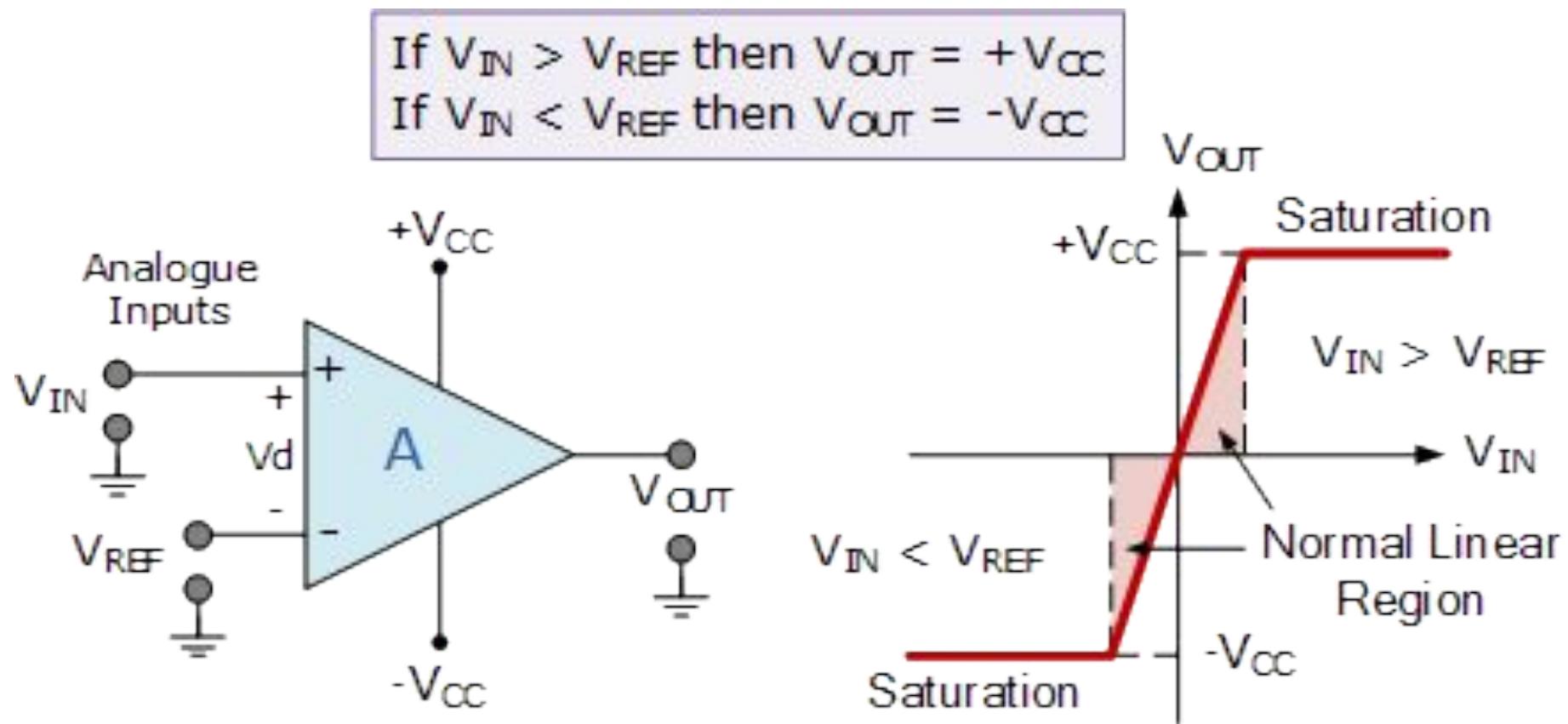
- Comparator: inverting and non-inverting comparators
  - Applications: zero crossing detector, window detector
  - Sine wave generator
  - Schmitt trigger
  - square wave generator (Astable multivibrator)
  - Monostable Multivibrator
  - 555 timers: functional diagram and Monostable operation
-

# Comparator

---

- The op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.
- *Voltage comparators* use either positive feedback or no feedback at all (open-loop mode) to switch its output between two saturated states.
- The open-loop op-amp comparator is an analogue circuit that operates in its non-linear region as changes in the two analogue inputs,  $V_+$  and  $V_-$  causes it to behave like a digital *bistable* device.

# OP-AMP Comparator Circuit



# Operation

---

- lets first assume that  $V_{IN}$  is less than the DC voltage level at  $V_{REF}$ , ( $V_{IN} < V_{REF}$ ):
  - As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output will be LOW and at the negative supply voltage  $-V_{cc}$  resulting in a negative saturation of the output.
- If we now increase the input voltage,  $V_{IN}$ :
  - so that its value is greater than the reference voltage  $V_{REF}$  on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage,  $+V_{cc}$  resulting in a positive saturation of the output.

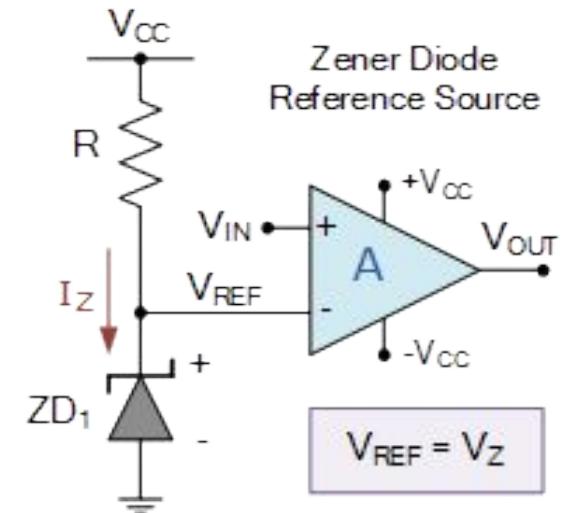
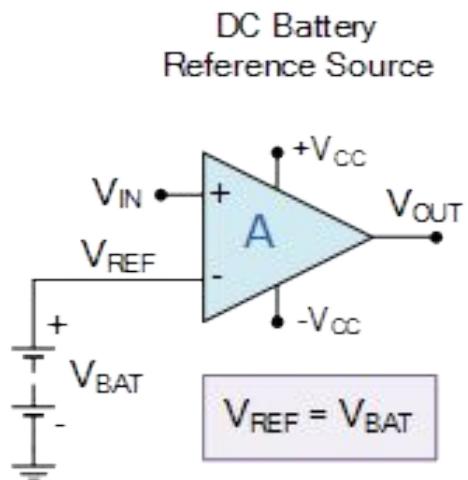
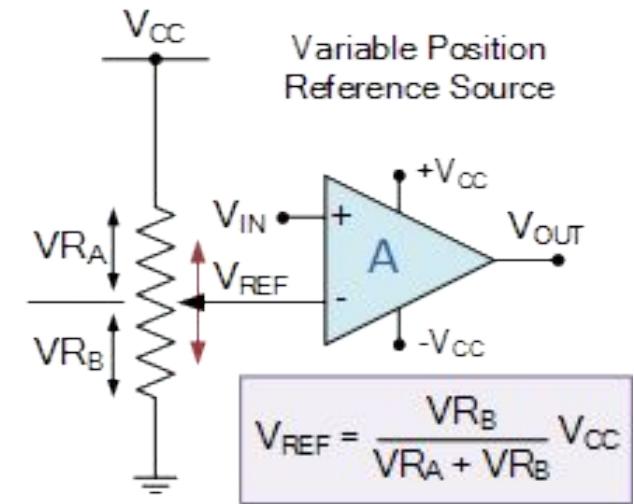
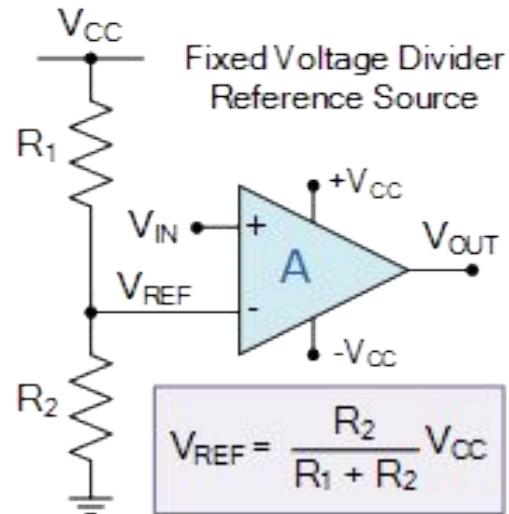
# Summary

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- The op-amp voltage comparator is a device whose output is dependent on the value of the input voltage,  $V_{IN}$  with respect to some DC voltage level as the output is **HIGH** when the voltage on the non-inverting input is greater than the voltage on the inverting input, and **LOW** when the non-inverting input is less than the inverting input voltage.
- This condition is true regardless of whether the input signal is connected to the inverting or the non-inverting input of the comparator.

# Comparator reference voltages

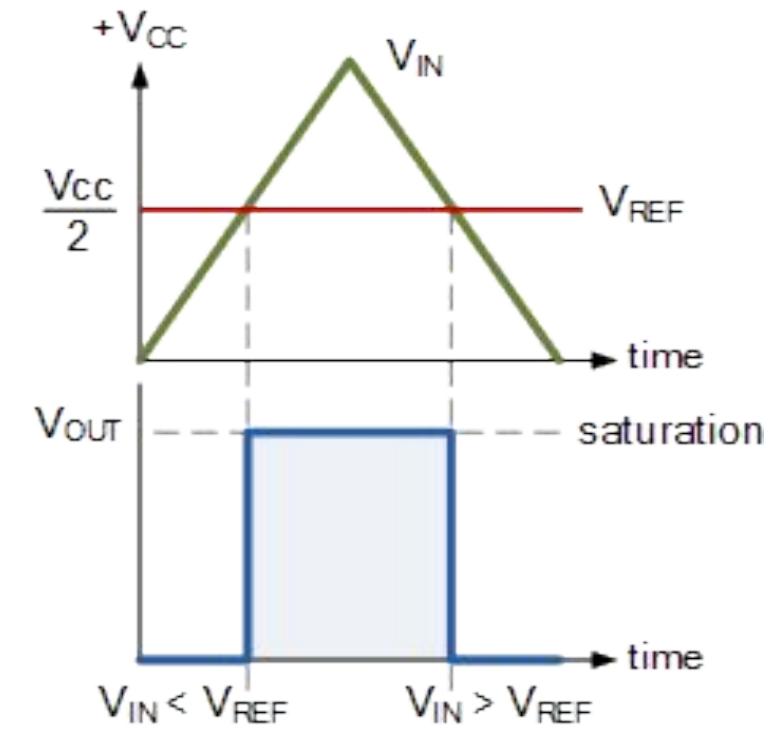
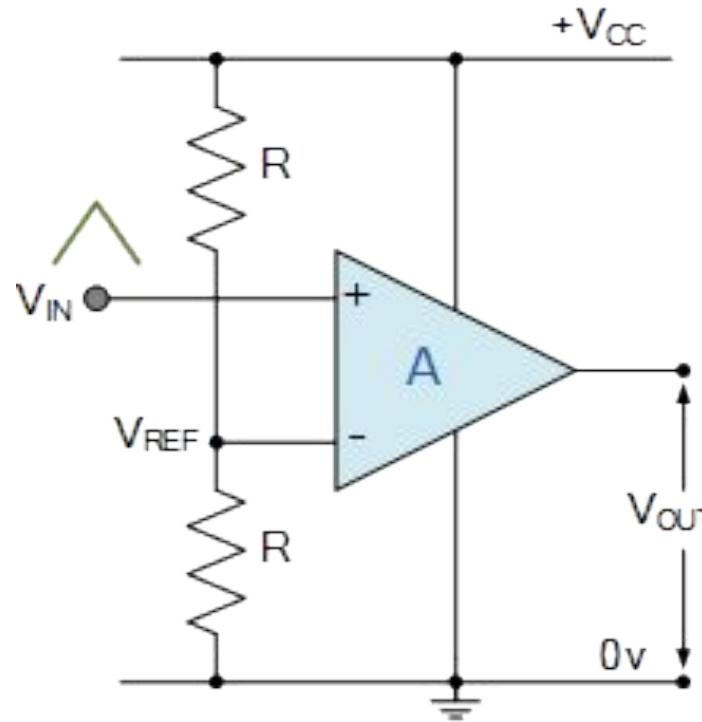
A resistive voltage divider is used to set the input reference voltage of a comparator, but a battery source, zener diode or potentiometer for a variable reference voltage can all be used as shown.



# Non-Inverting Comparator

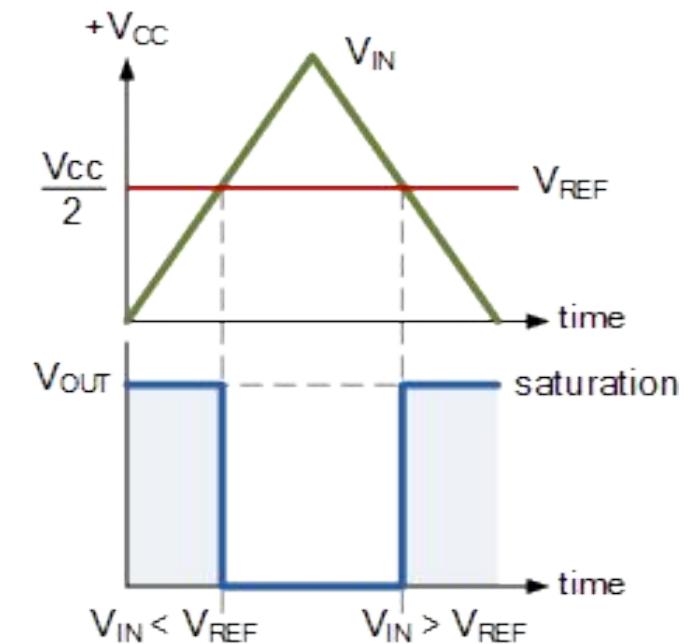
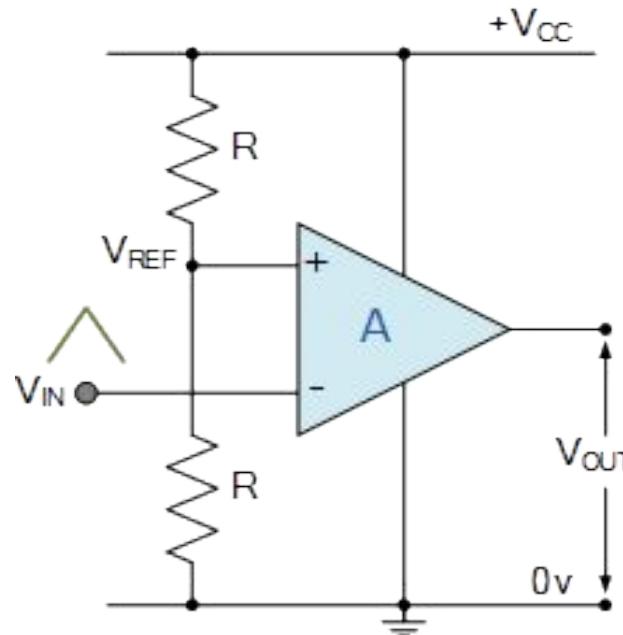
When  $V_{IN}$  is greater than  $V_{REF}$ , the op-amp comparators output will saturate towards the positive supply rail,  $V_{CC}$ .

When  $V_{IN}$  is less than  $V_{REF}$  the op-amp comparators output will change state and saturate at the negative supply rail, 0v as shown.

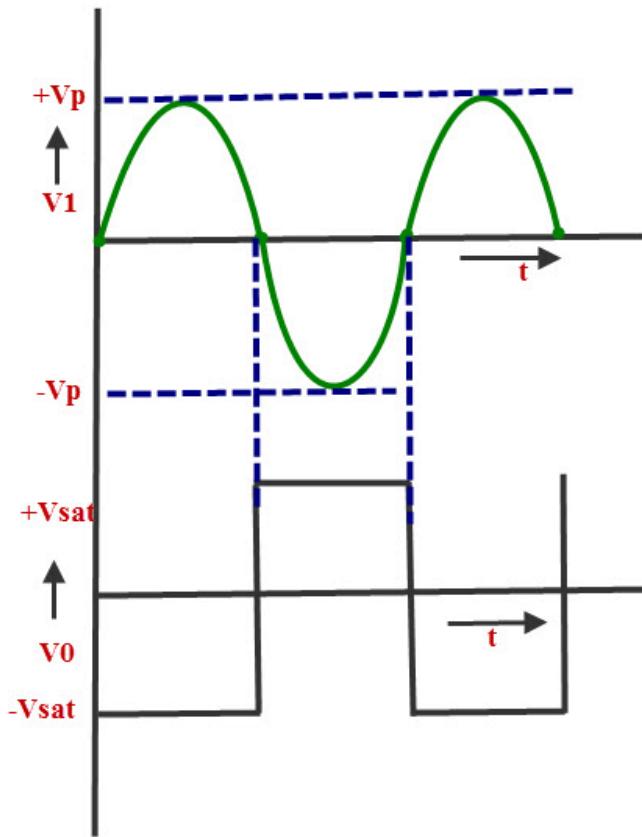


# Inverting Comparator

In the inverting configuration, the reference voltage is connected to the non-inverting input of the operational amplifier while the input signal is connected to the inverting input. Then when  $V_{IN}$  is less than  $V_{REF}$  the op-amp comparators output will saturate towards the positive supply rail,  $V_{cc}$ .



# Application: Zero Crossing Detector

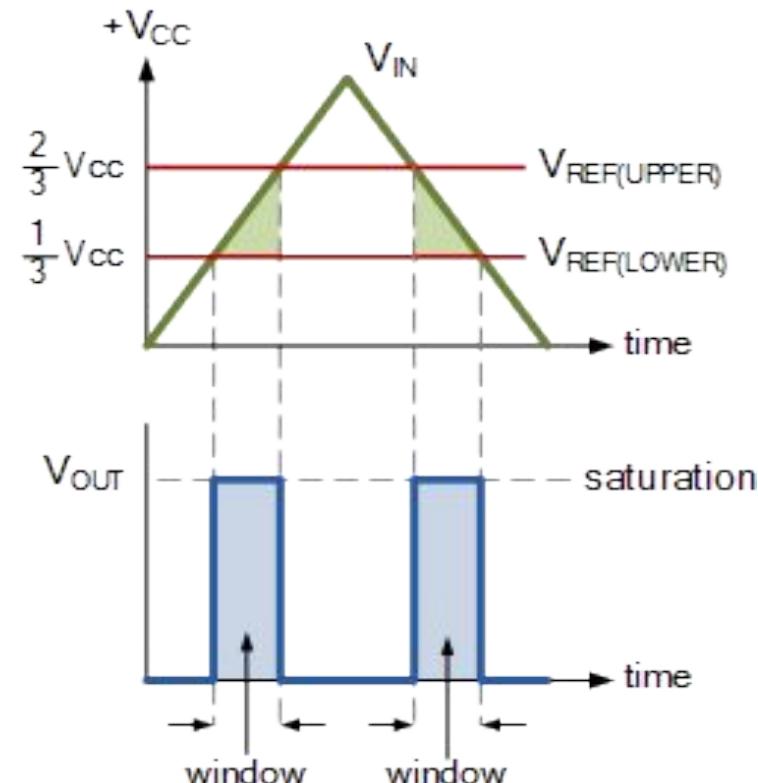
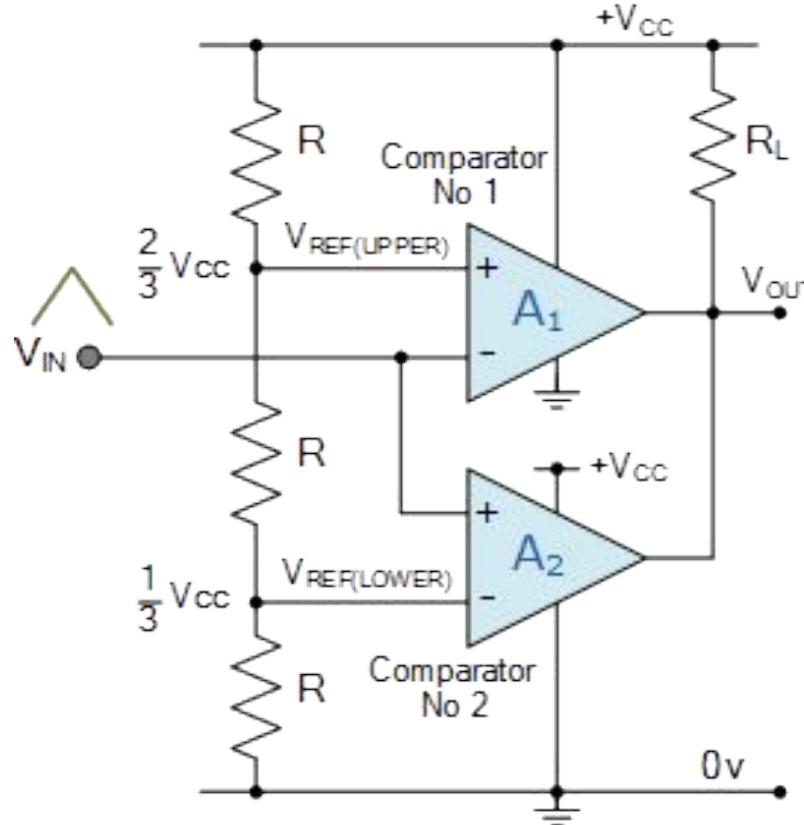


# Applications: Window Comparator

- is basically the combination of inverting and the non-inverting comparators into a single comparator stage.
- The window comparator detects input voltage levels that are within a **specific band or window of voltages**, (instead of indicating whether a voltage is greater or less than some preset or fixed voltage reference point).
- i.e. instead of having just one reference voltage value, a **window comparator will have two reference voltages** implemented by a pair of voltage comparators.
- One which triggers an op-amp comparator on detection of some upper voltage threshold,  $V_{REF(UPPER)}$  and one which triggers an op-amp comparator on detection of a lower voltage threshold level,  $V_{REF(LOWER)}$ . Then the voltage levels between these two upper and lower reference voltages is called the “window”.

# Window Comparator Circuit

- Using a voltage divider network, if we now use three equal value resistors so that  $R_1 = R_2 = R_3 = R$  we can create a very simple window comparator circuit as shown. Also as the resistive values are all equal, the voltage drops across each resistor will also be equal at one-third the supply voltage,  $1/3V_{cc}$ . Then in this simple example, we can set the upper reference voltage to  $2/3V_{cc}$  and the lower reference voltage to  $1/3V_{cc}$ .



# Operation

---

- When  $V_{IN}$  is below the lower voltage level,  $V_{REF(LOWER)}$  which equates to  $1/3V_{cc}$ , the output will be LOW. When  $V_{IN}$  exceeds this ( $1/3V_{cc}$ ) lower voltage level, the first op-amp comparator detects this and switches the output HIGH to  $V_{cc}$ .
- As  $V_{IN}$  continues to increase it passes the upper voltage level,  $V_{REF(UPPER)}$  at  $2/3V_{cc}$  and the second op-amp comparator detects this and switches the output back LOW. Then the difference between  $V_{REF(UPPER)}$  and  $V_{REF(LOWER)}$  (which is  $2/3V_{cc} - 1/3V_{cc}$  in this example) creates the switching window for the positive going signal.

# Operation

---

- Lets now assume that  $V_{IN}$  is at its maximum value and equal to  $V_{cc}$ . As  $V_{IN}$  decreases it passes the upper voltage level  $V_{REF(UPPER)}$  of the second op-amp comparator which switches the output HIGH. As  $V_{IN}$  continues to decrease it passes the lower voltage level,  $V_{REF(LOWER)}$  of the first op-amp comparator once again switching the output LOW.
- Then the difference between  $V_{REF(UPPER)}$  and  $V_{REF(LOWER)}$  creates the window for the negative going signal. So we can see that as  $V_{IN}$  passes above or passes below the upper and lower reference levels set by the two op-amp comparators, the output signal  $V_{OUT}$  will be HIGH or LOW.



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# BEC Tutorial 6





# Op-Amp integrator

---

- For the component values  $R_1 = 10 \text{ K}\Omega$ ,  $R_f = 100 \text{ K}\Omega$ ,  $C_f = 10 \text{ nF}$ , determine the frequency of integration, study the response for
  - sine wave 1 V peak with 5 KHz
  - square wave 1 V peak, 5 KHz
  - Step 1V for  $0 < t < 0.3 \text{ msec.}$



# Integrator

---

- Find  $R_1$  and  $R_F$  in the integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when  $w = 10,000$  rad/sec. use the capacitance as 0.01  $\mu F$ , and 1 nF.

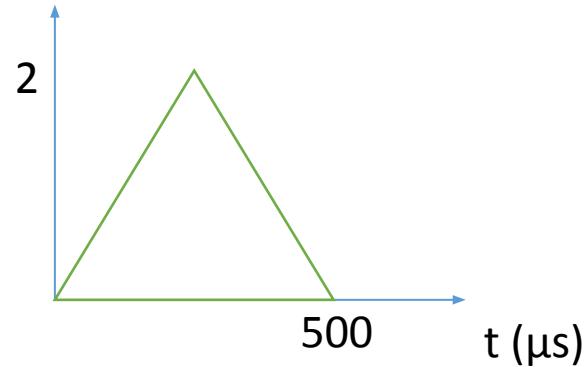
# Differentiator

---

- Design an op-amp differentiator that will differentiate an input signal with  $f_{\max} = 100 \text{ Hz}$ .
- Draw output wave form for a sine wave of 1 V peak at 100 Hz applied to differentiator.
- Repeat for square wave.

# Differentiator

- Input of the Differentiator is given as, find output if  $R_F = 2 \text{ k}\Omega$ , and  $C_1 = 0.1 \mu\text{F}$ .





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# OP-AMP based Waveform Generators

# Content

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- Comparator: inverting and non-inverting comparators
  - Applications: zero crossing detector, window detector
  - Sine wave generator
  - Schmitt trigger
  - square wave generator (Astable multivibrator)
  - Monostable Multivibrator
  - 555 timers: functional diagram and Monostable operation
-

# Waveform Generators

---

- In the design of electronic systems, the need for signals having standard waveforms - sinusoidal, square, triangular, or pulse.
- Systems like computer and control systems require standard signals i.e. clock pulses are needed for timing.
- Communication systems where signals of a variety of waveforms are utilized as information carriers.
- Test and measurement systems where signals, a variety of waveforms, are employed for testing and characterizing electronic devices and circuits.

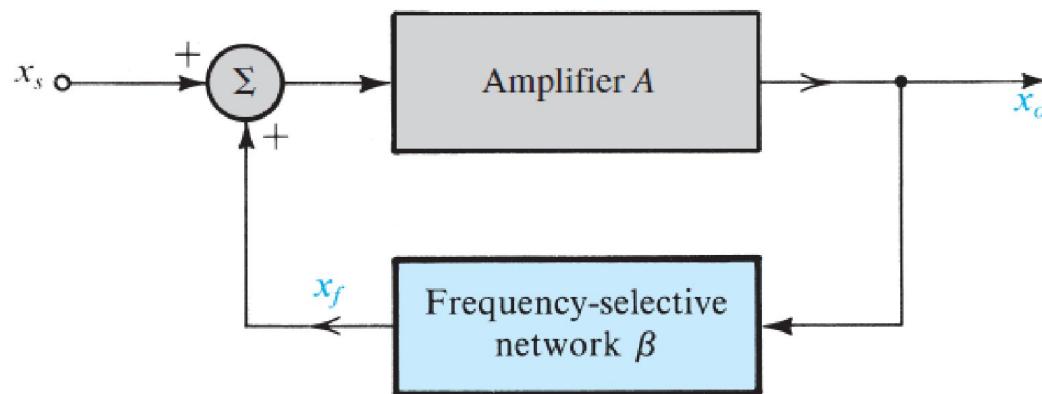
# Waveform Generators

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- Sinusoidal Waveform
  - for the generation of sinusoids a **positive-feedback loop** consisting of an amplifier and an RC **frequency-selective network**.
- Generating square, triangular, pulse (etc.) waveforms
  - employ circuit building blocks known as **multivibrators**.
  - They are three types : the **bistable**, the **astable**, and the **monostable**.

# Basic Principles of Sinusoidal Oscillators

- The basic structure of a sinusoidal oscillator consists of an amplifier and a frequency-selective network connected in a **positive-feedback loop**



$$x_o = A(x_s + x_f) \quad x_f = \beta x_o$$

$$x_o = A(x_s + \beta x_o) \quad x_o(1 - A\beta) = Ax_s$$

$$\frac{x_o}{x_s} = \frac{A}{(1 - A\beta)} = A_f$$

$$A_f(s) = \frac{A(s)}{1 - A(s)\beta(s)}$$

$$L(s) \equiv A(s)\beta(s)$$

# Condition for Oscillation

---

- The characteristic equation is

$$1 - L(s) = 0$$

- If at a specific frequency  $f_0$  the loop gain  $L = A\beta$  is equal to unity, it follows from that  $A_f$  will be infinite.
- That is, at this frequency the circuit will have a finite output for zero input signal. Such a circuit is called as “Oscillator”.
- Thus the condition for the feedback loop to provide sinusoidal oscillations of frequency  $\omega_0$  is

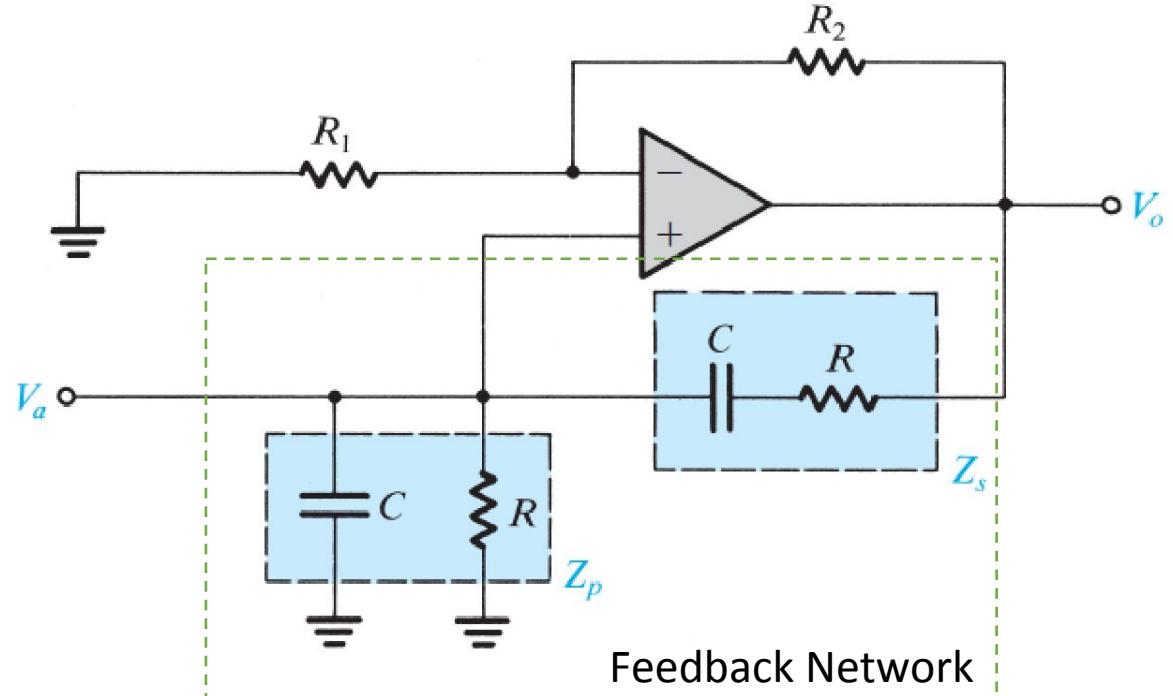
$$L(j\omega_0) \equiv A(j\omega_0)\beta(j\omega_0) = 1$$

---

# Wien-Bridge Oscillator

- The circuit consists of an op amp connected in the noninverting configuration, with a closed-loop gain of  $A = 1+R_2/R_1$ .
- In the feedback path, RC network is connected
- Feedback factor  $\beta$  is given by,

$$\beta = \frac{V_a}{V_o} = \frac{Z_p}{Z_p + Z_p}$$



# Analysis

---

- Impedance of the RC parallel combination

$$Z_p = \frac{1}{Y_p} = \frac{1}{\frac{1}{R} + j\omega C} = \frac{R}{1 + j\omega RC}$$

- Impedance of the RC series combination

$$Z_s = \frac{1}{j\omega C} + R = \frac{1 + j\omega RC}{j\omega C}$$

- Hence the feedback factor is

$$\beta = \frac{Z_p}{Z_p + Z_s} = \frac{j\omega RC}{1 - (\omega RC)^2 + j3\omega RC}$$

$$Z_p + Z_s = \frac{1 - (\omega RC)^2 + j3\omega RC}{j\omega C(1 + j\omega RC)}$$

# Analysis

---

- For the circuit to have oscillations,

$$A\beta = 1$$

- Since A is a real quantity,  $\beta$  must also be a real quantity, hence

$$1 - (\omega RC)^2 = 0$$

- Thus the frequency of oscillation is,  $f = \frac{1}{2\pi RC}$

- Then  $\beta = 1/3$ , leading to  $A = 3$ , (since  $A = 1+R_2/R_1$ ),  $R_2 = 2R_1$ .

# Example:

---

- Determine the maximum and minimum frequency of oscillations of a **Wien Bridge Oscillator** circuit having a resistor of  $10\text{k}\Omega$  and a variable capacitor of  $1\text{nF}$  to  $1000\text{nF}$ .



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# OP-AMP based Waveform Generators

# Content

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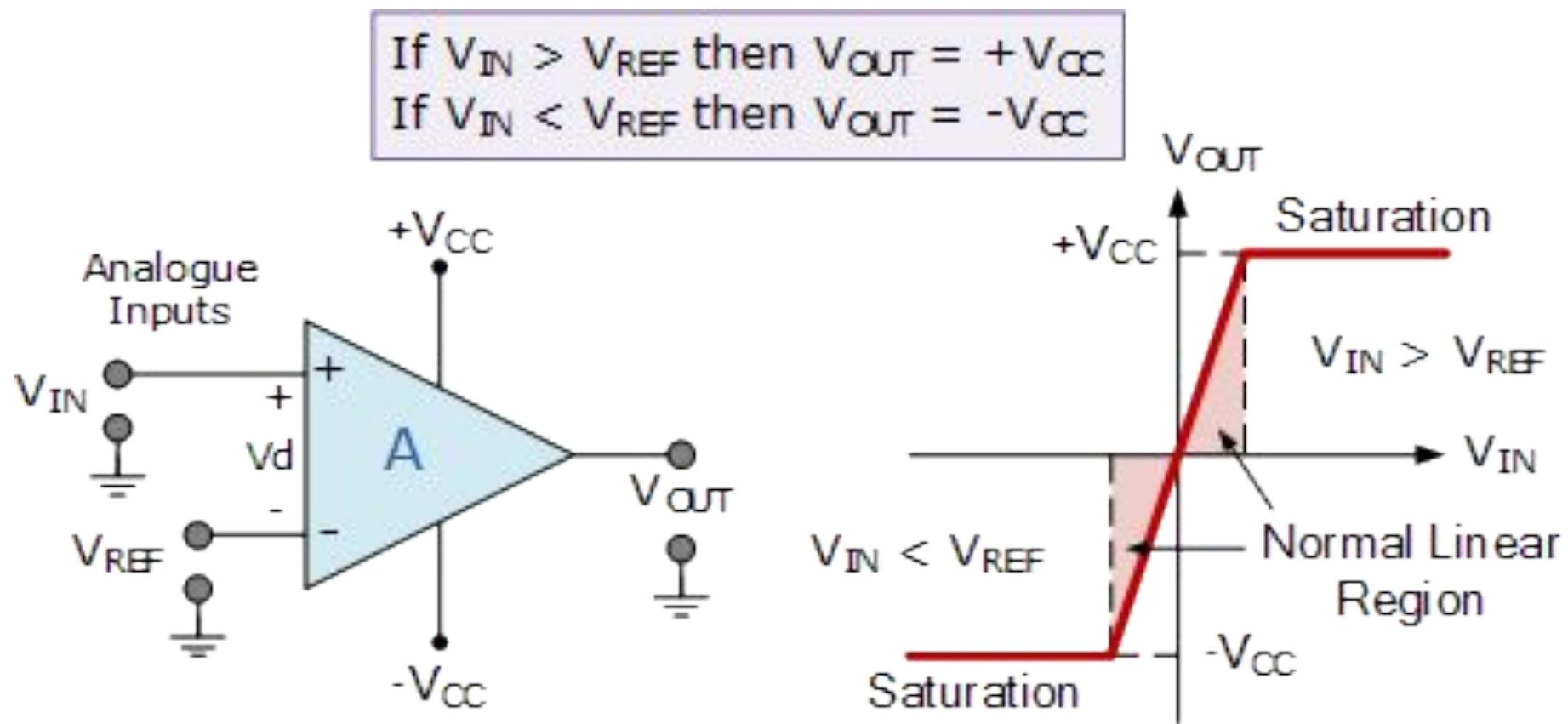
- Comparator: inverting and non-inverting comparators
  - Applications: zero crossing detector, window detector
  - Sine wave generator
  - Schmitt trigger
  - square wave generator (Astable multivibrator)
  - Monostable Multivibrator
  - 555 timers: functional diagram and Monostable operation
-

# Comparator

---

- The op-amp voltage comparator compares the magnitudes of two voltage inputs and determines which is the largest of the two.
- *Voltage comparators* use either positive feedback or no feedback at all (open-loop mode) to switch its output between two saturated states.
- The open-loop op-amp comparator is an analogue circuit that operates in its non-linear region as changes in the two analogue inputs,  $V_+$  and  $V_-$  causes it to behave like a digital *bistable* device.

# OP-AMP Comparator Circuit



# Operation

---

- lets first assume that  $V_{IN}$  is less than the DC voltage level at  $V_{REF}$ , ( $V_{IN} < V_{REF}$ ):
  - As the non-inverting (positive) input of the comparator is less than the inverting (negative) input, the output will be LOW and at the negative supply voltage  $-V_{cc}$  resulting in a negative saturation of the output.
- If we now increase the input voltage,  $V_{IN}$ :
  - so that its value is greater than the reference voltage  $V_{REF}$  on the inverting input, the output voltage rapidly switches HIGH towards the positive supply voltage,  $+V_{cc}$  resulting in a positive saturation of the output.

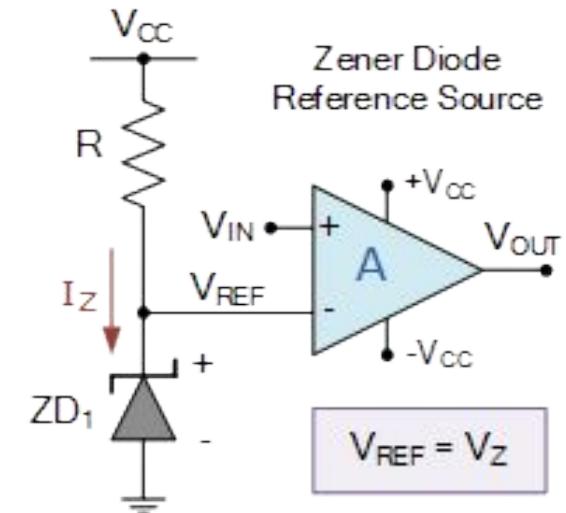
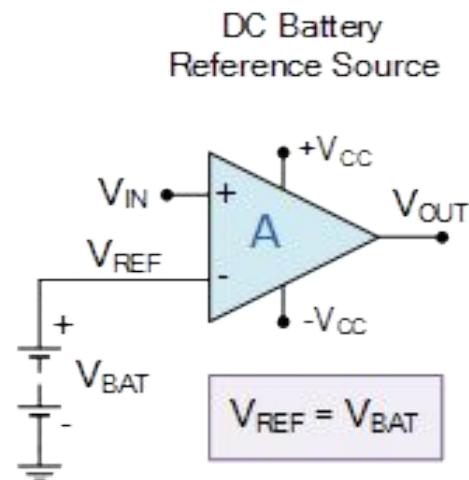
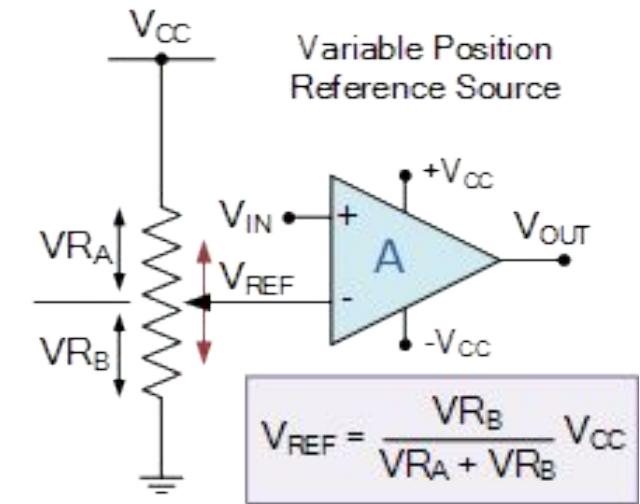
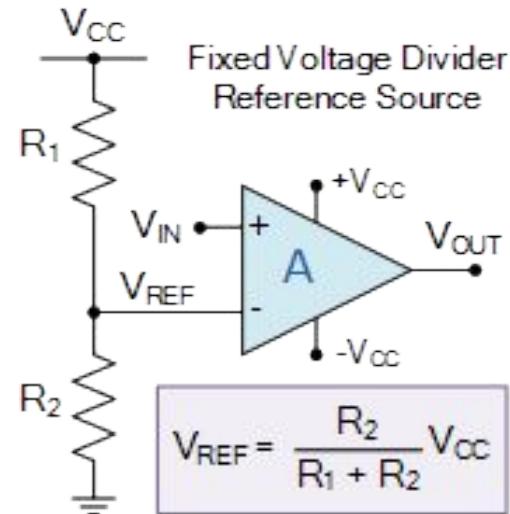
# Summary

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- The op-amp voltage comparator is a device whose output is dependent on the value of the input voltage,  $V_{IN}$  with respect to some DC voltage level as the output is **HIGH** when the voltage on the non-inverting input is greater than the voltage on the inverting input, and **LOW** when the non-inverting input is less than the inverting input voltage.
- This condition is true regardless of whether the input signal is connected to the inverting or the non-inverting input of the comparator.

# Comparator reference voltages

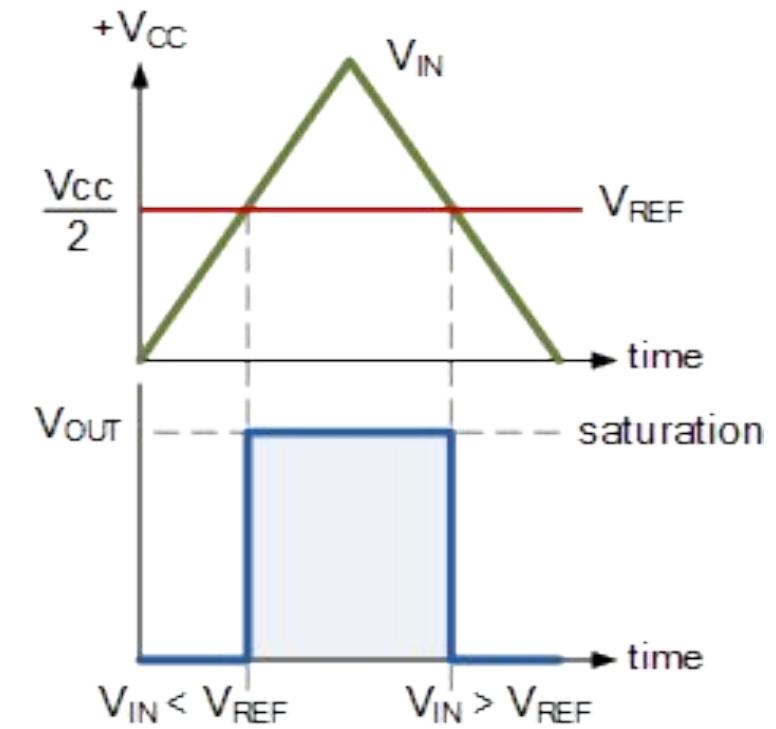
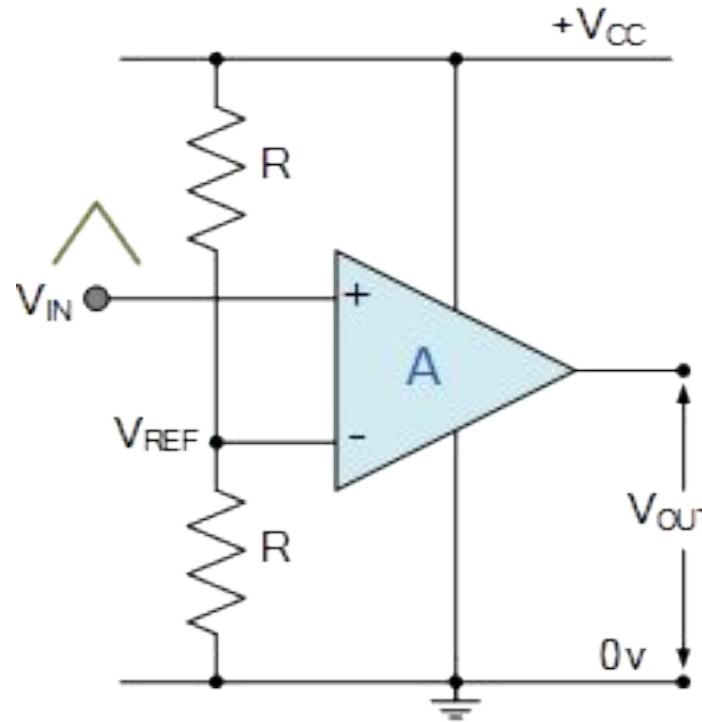
A resistive voltage divider is used to set the input reference voltage of a comparator, but a battery source, zener diode or potentiometer for a variable reference voltage can all be used as shown.



# Non-Inverting Comparator

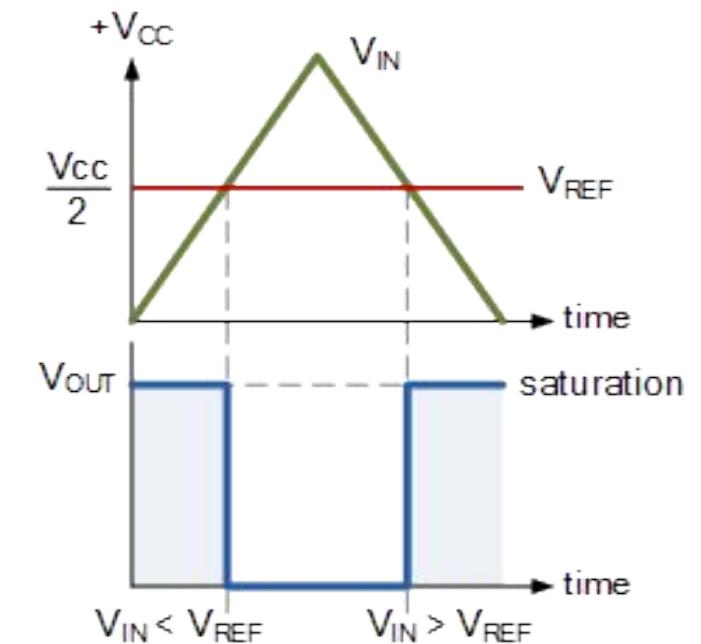
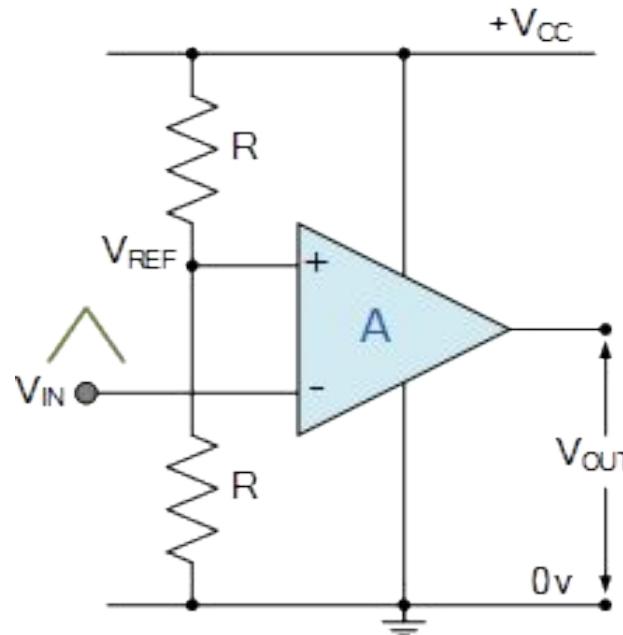
When  $V_{IN}$  is greater than  $V_{REF}$ , the op-amp comparators output will saturate towards the positive supply rail,  $V_{CC}$ .

When  $V_{IN}$  is less than  $V_{REF}$  the op-amp comparators output will change state and saturate at the negative supply rail, 0v as shown.

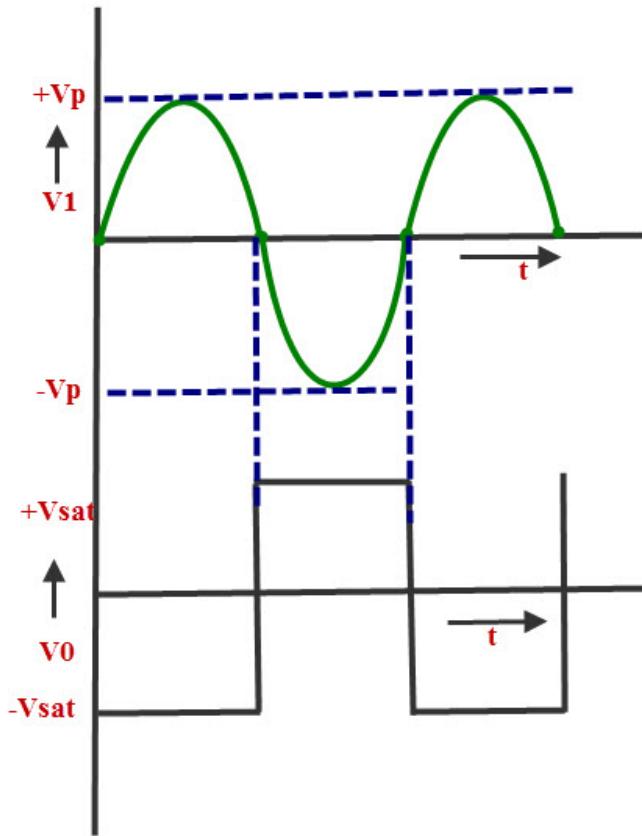


# Inverting Comparator

In the inverting configuration, the reference voltage is connected to the non-inverting input of the operational amplifier while the input signal is connected to the inverting input. Then when  $V_{IN}$  is less than  $V_{REF}$  the op-amp comparators output will saturate towards the positive supply rail,  $V_{cc}$ .



# Application: Zero Crossing Detector

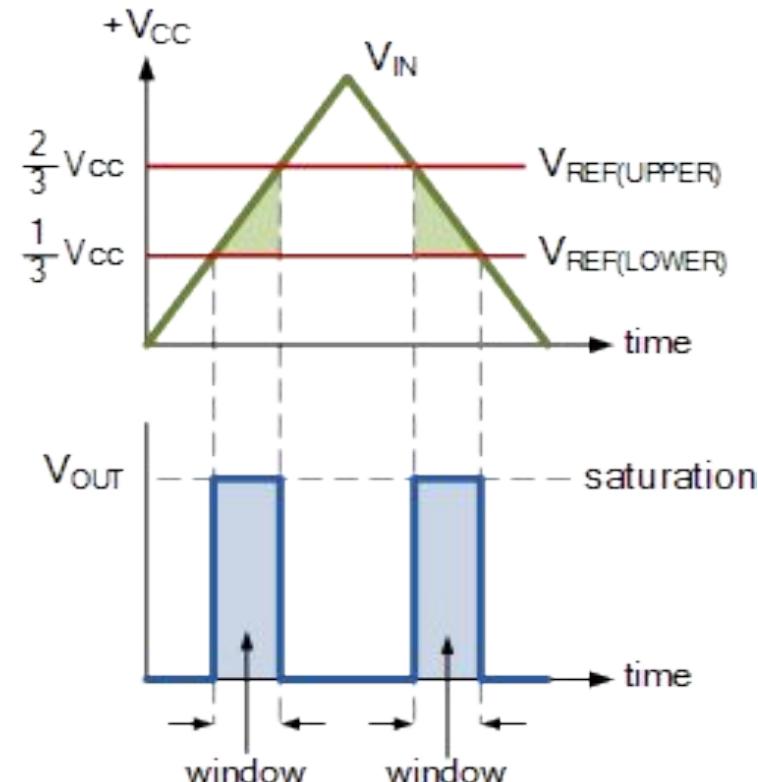
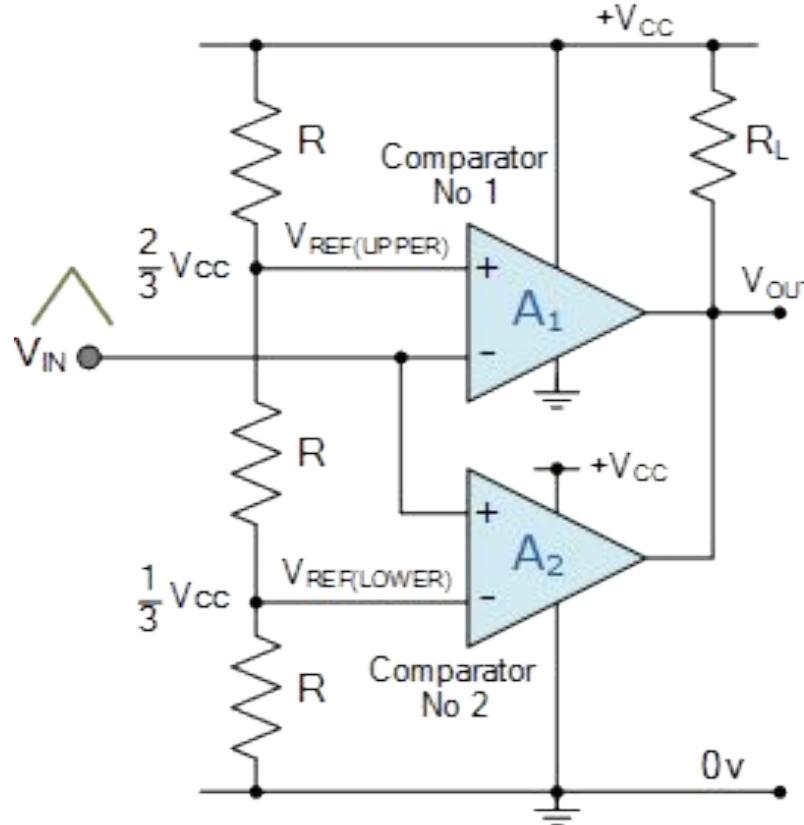


# Applications: Window Comparator

- is basically the combination of inverting and the non-inverting comparators into a single comparator stage.
- The window comparator detects input voltage levels that are within a **specific band or window of voltages**, (instead of indicating whether a voltage is greater or less than some preset or fixed voltage reference point).
- i.e. instead of having just one reference voltage value, a **window comparator will have two reference voltages** implemented by a pair of voltage comparators.
- One which triggers an op-amp comparator on detection of some upper voltage threshold,  $V_{REF(UPPER)}$  and one which triggers an op-amp comparator on detection of a lower voltage threshold level,  $V_{REF(LOWER)}$ . Then the voltage levels between these two upper and lower reference voltages is called the “window”.

# Window Comparator Circuit

- Using a voltage divider network, if we now use three equal value resistors so that  $R_1 = R_2 = R_3 = R$  we can create a very simple window comparator circuit as shown. Also as the resistive values are all equal, the voltage drops across each resistor will also be equal at one-third the supply voltage,  $1/3V_{cc}$ . Then in this simple example, we can set the upper reference voltage to  $2/3V_{cc}$  and the lower reference voltage to  $1/3V_{cc}$ .



# Operation

---

- When  $V_{IN}$  is below the lower voltage level,  $V_{REF(LOWER)}$  which equates to  $1/3V_{cc}$ , the output will be LOW. When  $V_{IN}$  exceeds this ( $1/3V_{cc}$ ) lower voltage level, the first op-amp comparator detects this and switches the output HIGH to  $V_{cc}$ .
- As  $V_{IN}$  continues to increase it passes the upper voltage level,  $V_{REF(UPPER)}$  at  $2/3V_{cc}$  and the second op-amp comparator detects this and switches the output back LOW. Then the difference between  $V_{REF(UPPER)}$  and  $V_{REF(LOWER)}$  (which is  $2/3V_{cc} - 1/3V_{cc}$  in this example) creates the switching window for the positive going signal.

# Operation

---

- Lets now assume that  $V_{IN}$  is at its maximum value and equal to  $V_{cc}$ . As  $V_{IN}$  decreases it passes the upper voltage level  $V_{REF(UPPER)}$  of the second op-amp comparator which switches the output HIGH. As  $V_{IN}$  continues to decrease it passes the lower voltage level,  $V_{REF(LOWER)}$  of the first op-amp comparator once again switching the output LOW.
- Then the difference between  $V_{REF(UPPER)}$  and  $V_{REF(LOWER)}$  creates the window for the negative going signal. So we can see that as  $V_{IN}$  passes above or passes below the upper and lower reference levels set by the two op-amp comparators, the output signal  $V_{OUT}$  will be HIGH or LOW.

# Waveform Generators

---

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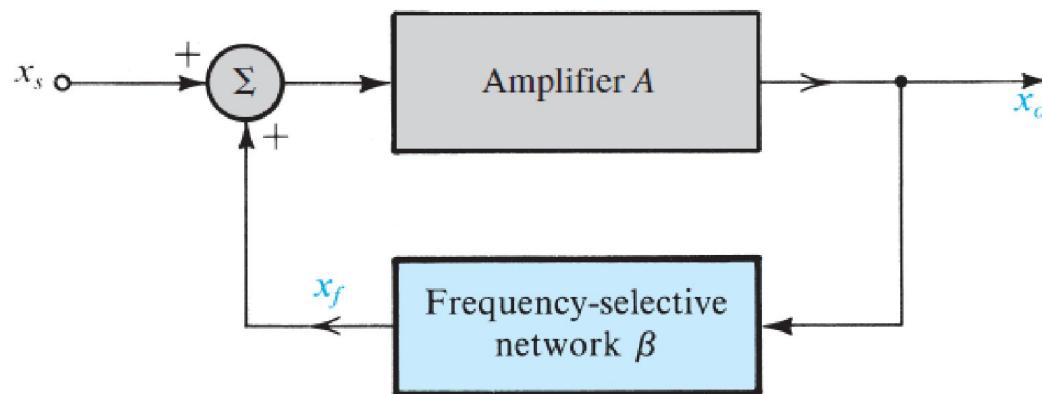
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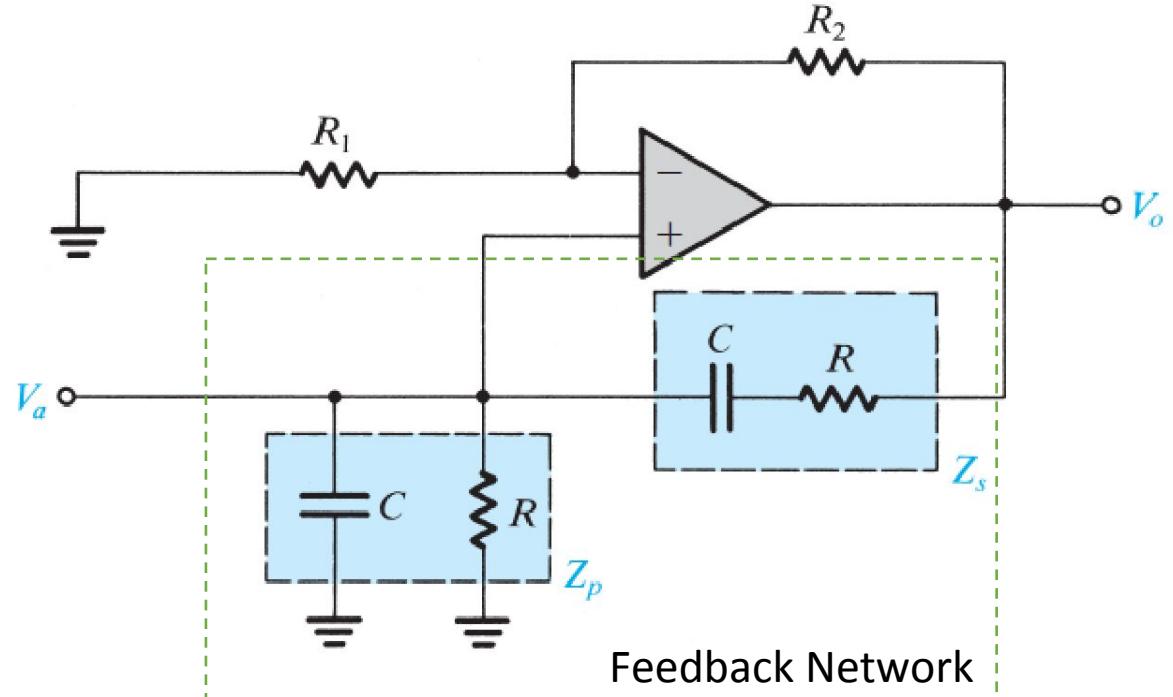
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---

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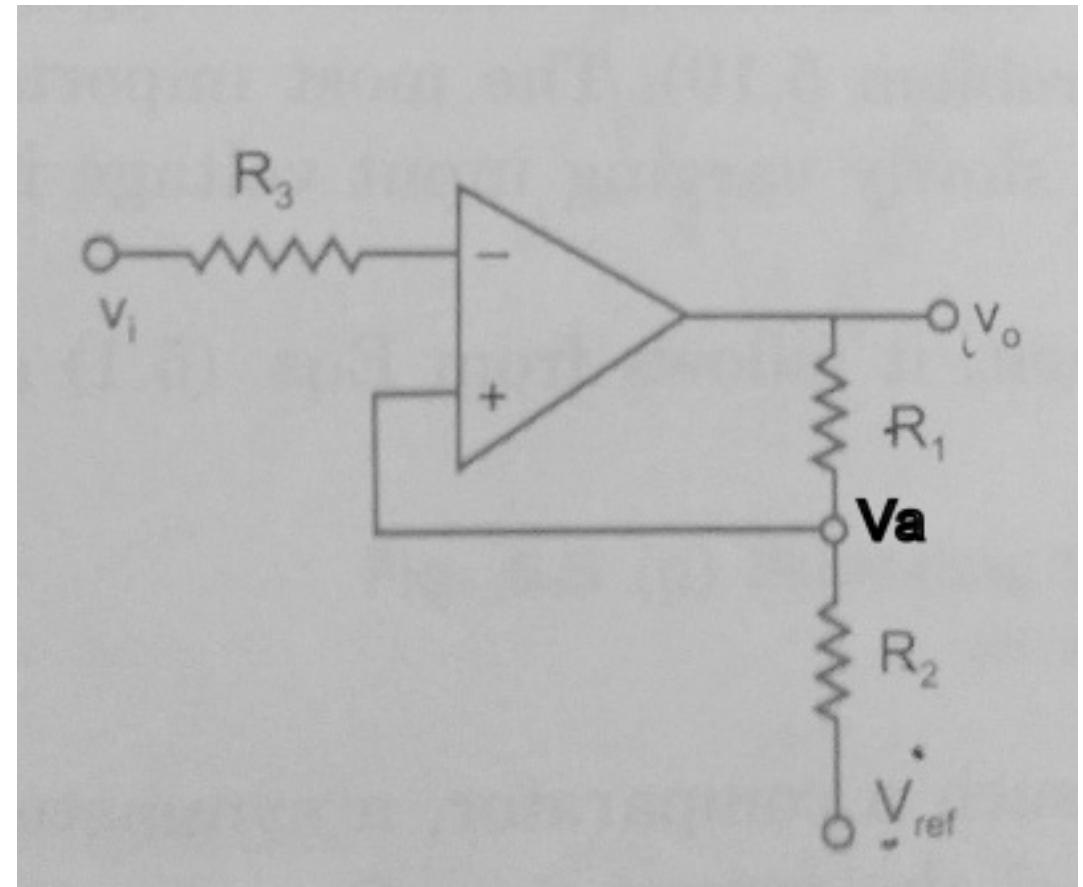
# Example:

---

- Determine the maximum and minimum frequency of oscillations of a **Wien Bridge Oscillator** circuit having a resistor of  $10\text{k}\Omega$  and a variable capacitor of  $1\text{nF}$  to  $1000\text{nF}$ .

# Regenerative Comparator

- $V_i$  applied at (-) input terminal and feedback voltage to the (+) input terminal.
- $V_i$  triggers the output  $V_o$  every time it exceeds the certain voltage level.
- The voltage levels are called upper (lower) threshold voltage  $V_{UT}$  ( $V_{LT}$ ).
- $V_{UT} - V_{LT}$  is referred as hysteresis width



# Computing Upper Threshold voltages ( $V_{UT}$ )

---

- Let  $V_o = +V_{sat}$ : to determine ' $V_a$ ' i.e.  $V_{UT}$ , use superposition
- Case 1: Assuming  $V_{ref} = 0$ , voltage across " $R_2$ " will be  $V_a$ ,

$$V_a = V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

- Case 2: By considering  $V_o = 0$ , then voltage across  $R_1$  will be  $V_a$

$$V_a = \frac{R_1}{R_1 + R_2} V_{ref}$$

- By combining the above two cases,

$$V_{UT} = \frac{R_1}{R_1 + R_2} V_{ref} + \frac{R_2}{R_1 + R_2} V_{sat}$$

---

# Computing Lower Threshold voltage ( $V_{LT}$ )

---

- Let  $V_o = -V_{sat}$ : to determine ' $V_a$ ' i.e.  $V_{LT}$ , again use superposition
- Case 1: Assuming  $V_{ref} = 0$ , voltage across " $R_2$ " will be,

$$V_a = -\frac{R_2}{R_1 + R_2} V_{sat}$$

- Case 2: By considering  $V_o = 0$ , then voltage across  $R_1$  will be,

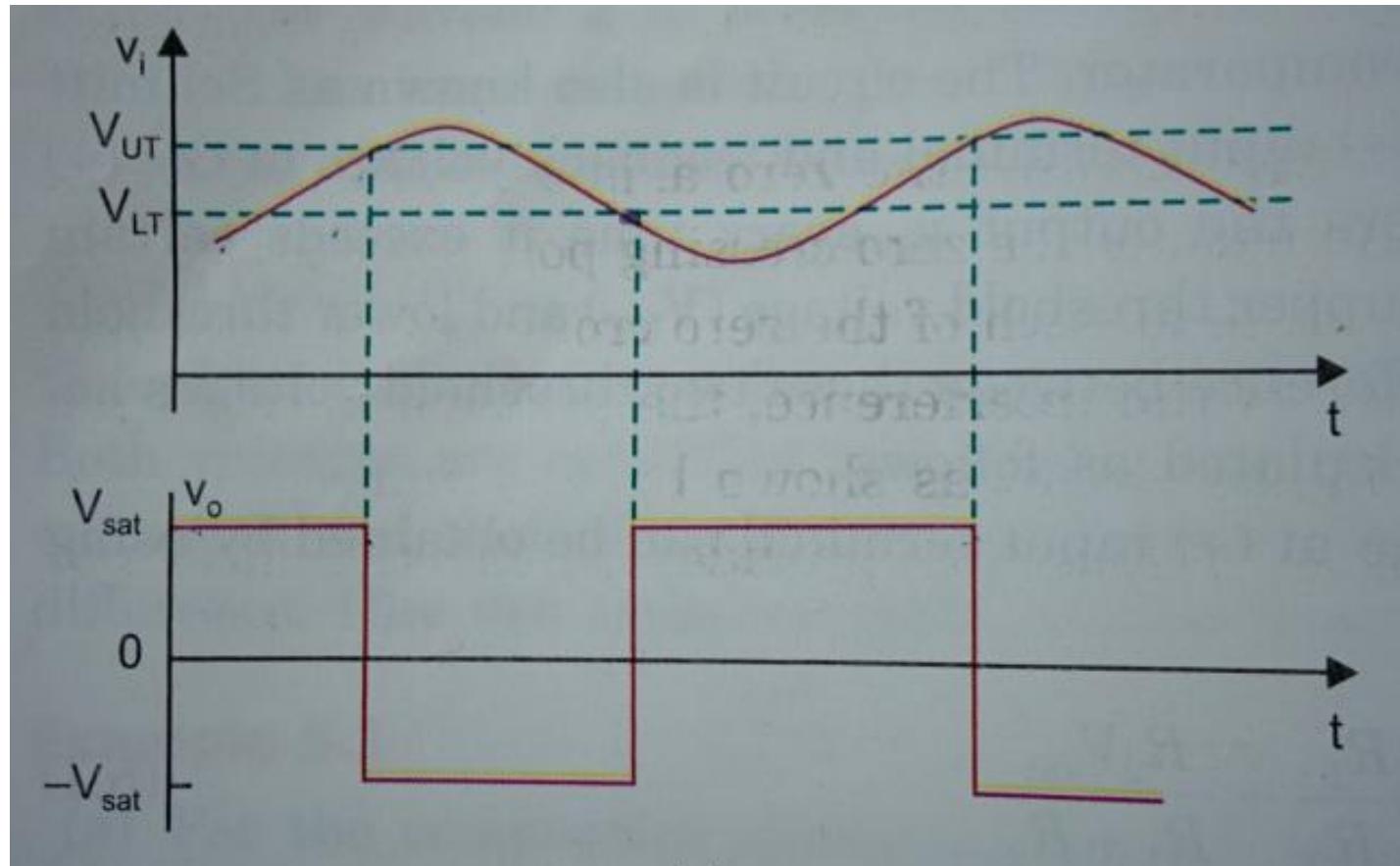
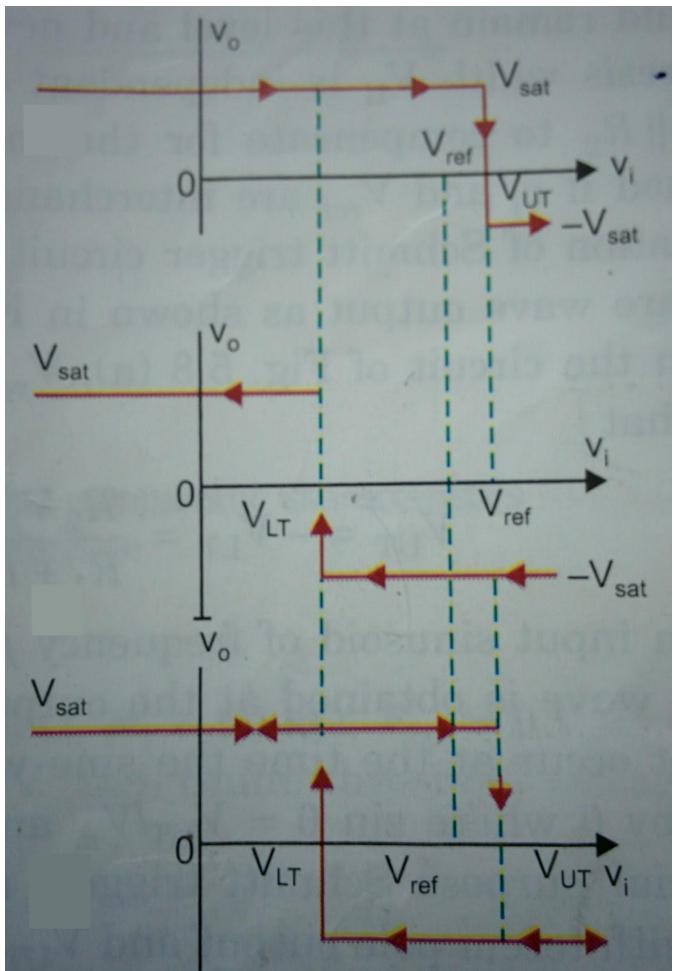
$$V_a = \frac{R_1}{R_1 + R_2} V_{ref}$$

- By combining the above two cases,

$$V_{LT} = \frac{R_1}{R_1 + R_2} V_{ref} - \frac{R_2}{R_1 + R_2} V_{sat}$$

---

# Square wave



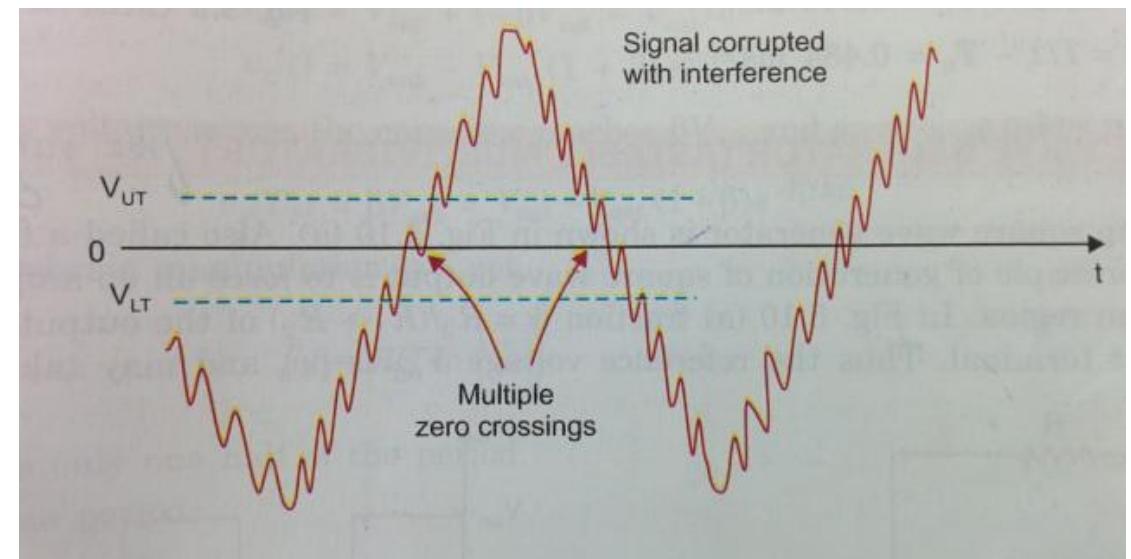
- Hysteresis width is

$$V_H = \frac{2R_2}{R_1 + R_2} V_{sat}$$

- Further, if the ref voltage is zero, then symmetric square wave can be obtained.

- Application:

- slow varying input can be converted in square wave output.
- Superior to simple zero crossing detector circuit.



# Example:

---

- In the given circuit of Schmitt trigger,  $R_2 = 100 \Omega$ ,  $R_1 = 50 K\Omega$ ,  $V_{ref} = 0 V$ ,  $V_i = 1 V_{pp}$  sine wave and saturation voltage  $= +/- 14 V$ . Determine the threshold voltages  $V_{UT}$ ,  $V_{LT}$  and  $V_H$ .

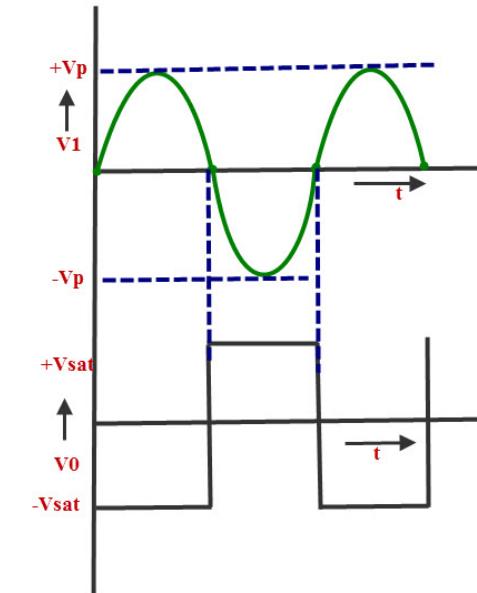
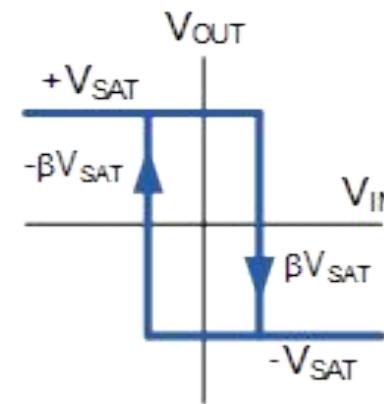
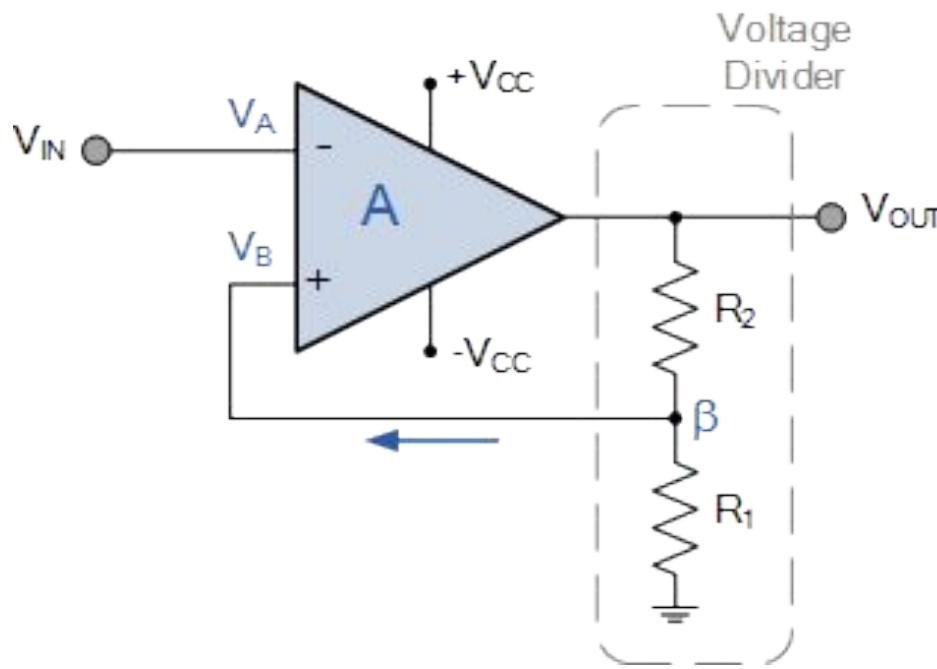
$$V_{UT} = + \frac{R_2}{R_1 + R_2} V_{sat} = 28mV$$

$$V_H = \frac{2R_2}{R_1 + R_2} V_{sat} = 56mV$$

$$V_{LT} = - \frac{R_2}{R_1 + R_2} V_{sat} = -28mV$$

# Generation of a Square wave using Astable Multivibrator

- by connecting the bistable multivibrator with an RC circuit in a feedback loop



# Square wave Generator

The Square Wave Generator Using Op amp means the astable multivibrator circuit using op-amp, which generates the square wave of required frequency.

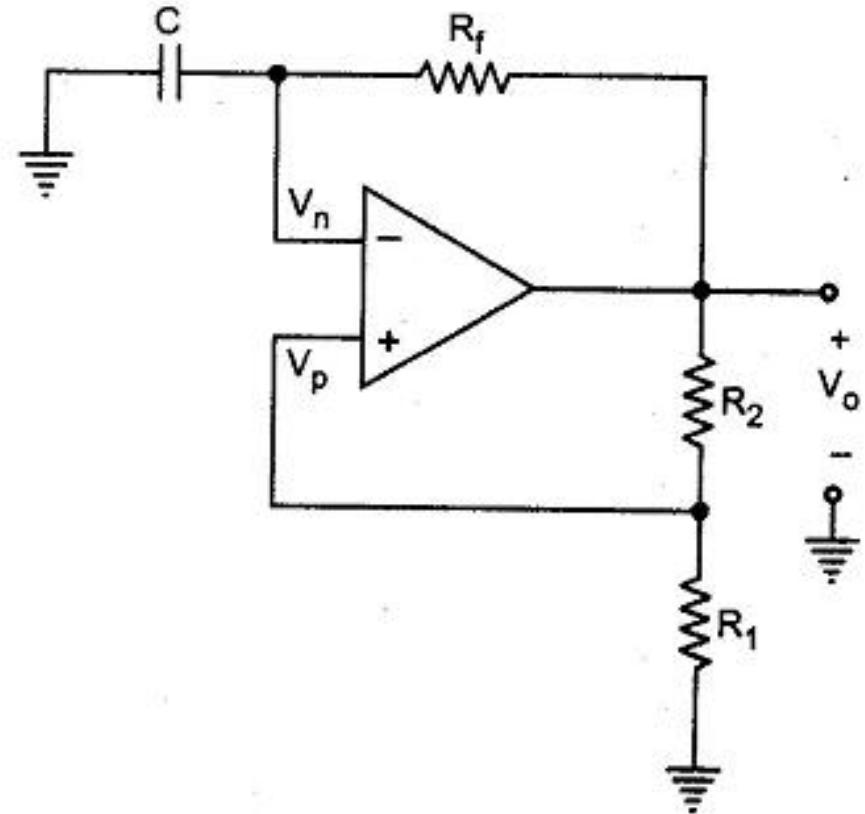
It looks like a comparator with hysteresis (schmitt trigger), except that the input voltage is replaced by a capacitor. The circuit has a time dependent elements such as resistance and capacitor to set the frequency of oscillation.

When  $V_o$  is at  $+V_{sat}$ , the feedback voltage is called the upper threshold voltage  $V_{UT}$  and is given as

$$V_{UT} = \frac{R_1 + V_{sat}}{R_1 + R_2}$$

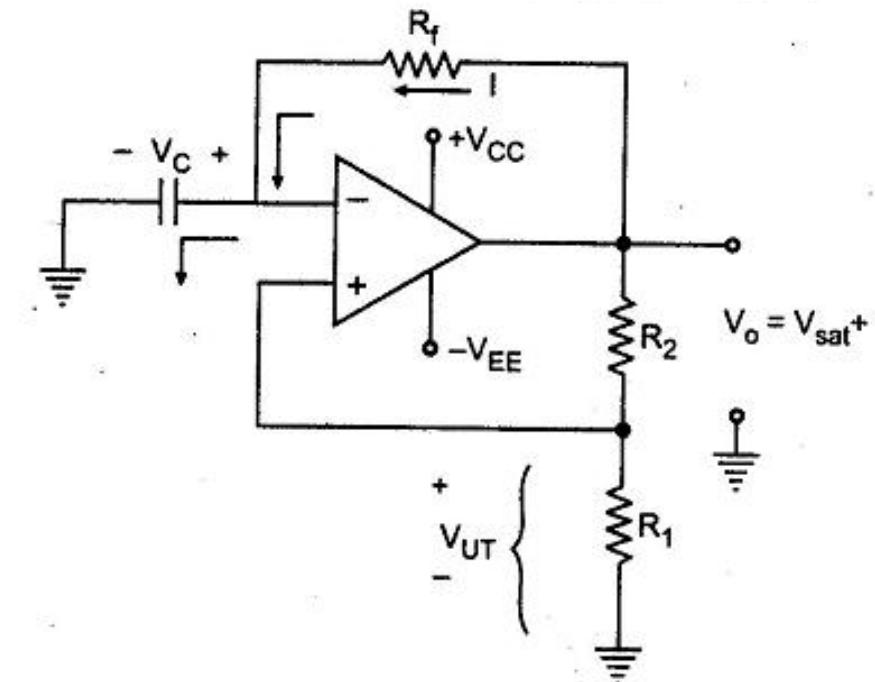
When  $V_o$  is at  $-V_{sat}$ , the feedback voltage is called the lower-threshold voltage  $V_{LT}$  and is given as

$$V_{LT} = \frac{R_1 - V_{sat}}{R_1 + R_2}$$



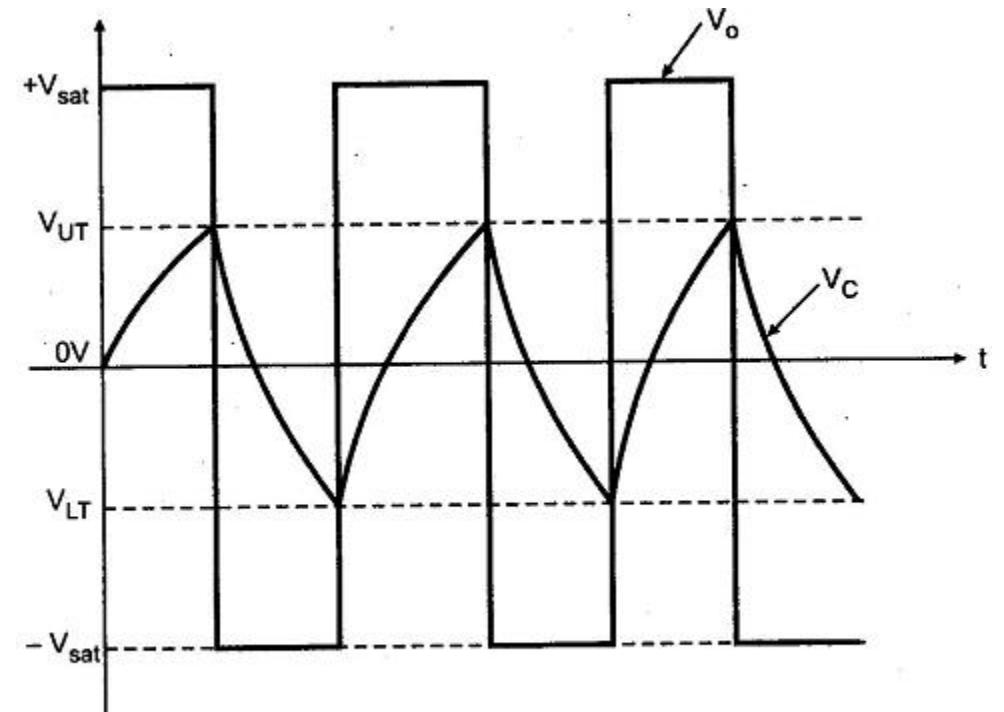
# Operation:

- When power is turn ON:  $V_{out}$  automatically swings either to  $+V_{sat}$  or to  $-V_{sat}$  since these are the only stable states allowed by the schmitt trigger.
- Assume it swings to  $+V_{sat}$ : With  $V_o = +V_{sat}$  and  $V_c = V_{sat}$  and capacitor starts charging towards  $+V_{sat}$  through the feedback path provided by the resistor  $R_f$  to the inverting ( $-$ ) input.
- As long as the capacitor voltage  $V_c$  is less than  $V_{sat}$ , the output voltage remains at  $+V_{sat}$ .
- As soon as  $V_c$  charges to a value slightly greater than  $V_{sat}$ , the ( $-$ ) input goes positive with respect to the ( $+$ ) input. This switches the output voltage from  $+V_{sat}$  to  $-V_{sat}$  and we have  $V_c = V_{sat}$  which is negative with respect to ground. As  $V_o$  switches to  $-V_{sat}$ , capacitor starts discharging via  $R_f$ .
- The current  $I$  – discharges capacitor to 0 V and recharges capacitor to  $V_{sat}$ . When  $V_c$  becomes slightly more negative than the feedback voltage  $V_{sat}$ , output voltage  $V_o$  switches back to  $+V_{sat}$



# Waveform

- As a result, the condition is reestablished except that capacitor now has a initial charge equal to  $V_{LT}$ .
- The capacitor will discharge from  $V_{LT}$  to OV and then recharge to  $V_{UT}$ , and the process is repeating.
- Once the, initial cycle is completed, the waveforms become periodic.



# Frequency of Oscillations

---

- The frequency of oscillation is determined by the time it takes the capacitor to charge from  $V_{LT}$  to  $V_{UT}$  and vice versa. The voltage across the capacitor as a function of time is given as

$$V_C(t) = V_{max} + (V_{initial} - V_{max}) e^{(-t/T)}$$

- where  $V_c(t)$  is the instantaneous voltage across the capacitor.
- $V_{initial}$  is the initial voltage
- $V_{max}$  is the voltage toward which the capacitor is charging.

- Let us consider the charging of capacitor from  $V_{LT}$  to  $V_{UT}$ , where  $V_{LT}$  is the initial voltage,  $V_{UT}$  is the instantaneous voltage and  $+V_{sat}$  is the maximum voltage. At  $t = T_1$ , voltage across capacitor reaches  $V_{UT}$  and therefore equation becomes

$$V_{UT} = +V_{sat} + (V_{LT} - +V_{sat}) e^{(-T_1/R_f C)}$$

$$\therefore -(V_{LT} - +V_{sat}) e^{(-T_1/R_f C)} = +V_{sat} - V_{UT}$$

$$\therefore e^{(-T_1/R_f C)} = \frac{(+V_{sat} - V_{UT})}{(+V_{sat} - V_{LT})}$$

$$\frac{-T_1}{R_f C} = \ln \left( \frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}} \right)$$

$$T_1 = -R_f C \ln \left( \frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}} \right)$$

$$= R_f C \ln \left( \frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}} \right)$$

- The time taken by capacitor to charge from  $V_{UT}$  to  $V_{LT}$  is same as time required for charging capacitor from  $V_{LT}$  to  $V_{UT}$ . Therefore, total time required for one oscillation is given as

$$T = 2T_1$$

$$= 2R_f C \ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)$$

$$T = 2R_f C \ln\left(\frac{1 + \beta}{1 - \beta}\right)$$

$$V_{LT} = -\beta V_{sat}$$

$$\beta = \frac{R_1}{R_1 + R_2}$$

$$V_{UT} = +\beta V_{sat}$$

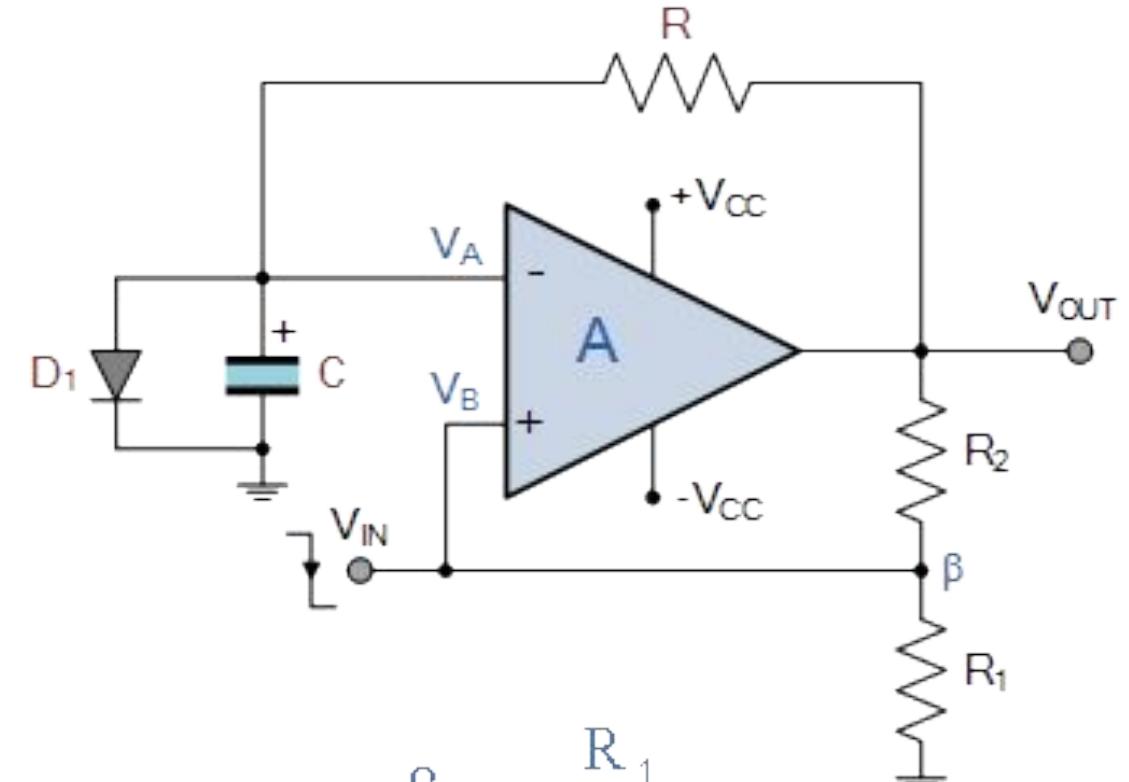
- The frequency of oscillation can be determined as  $f_o = 1/T$ , where  $T$  represents the time required for one oscillation.
- Substituting the value of  $T$  we get,

$$f_o = \frac{1}{2R_f C \ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)}$$

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# Monostable Multivibrator

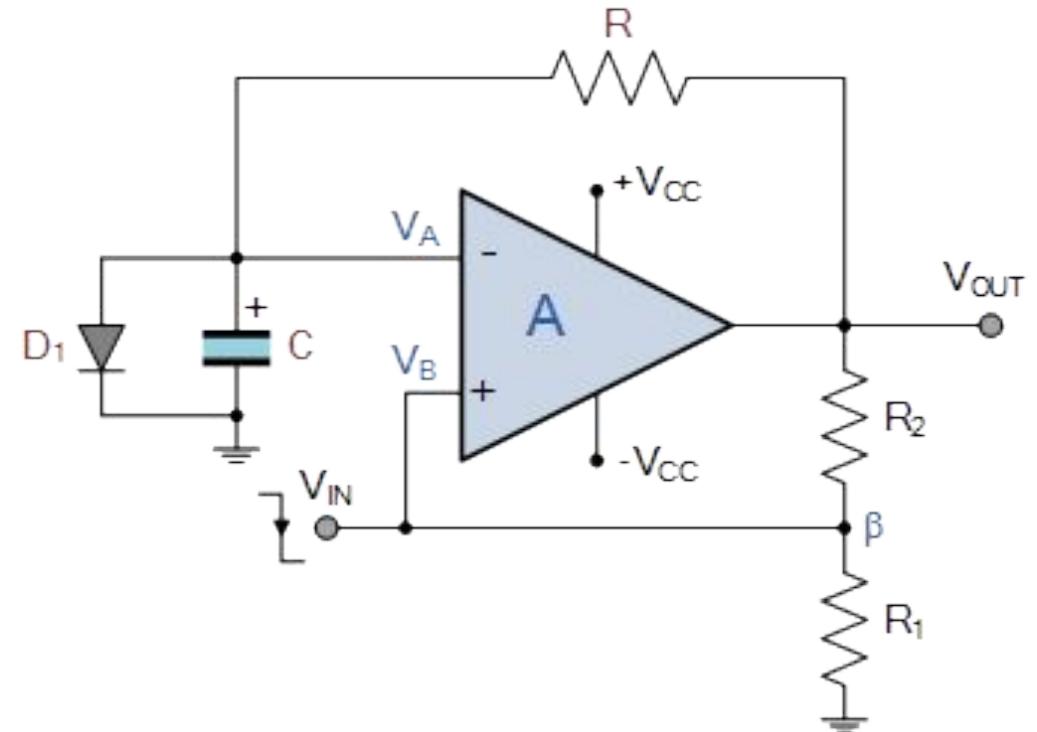
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- The inverting input is held at 0.7 volts, the forward volt drop of diode,  $D_1$  and clamped to 0v (ground) by the diode, preventing it from going any more positive. Thus the potential at  $V_A$  is much less than that at  $V_B$  and the output remains stable at  $+V_{CC}$ .
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$$\beta = \frac{R_1}{R_1 + R_2}$$

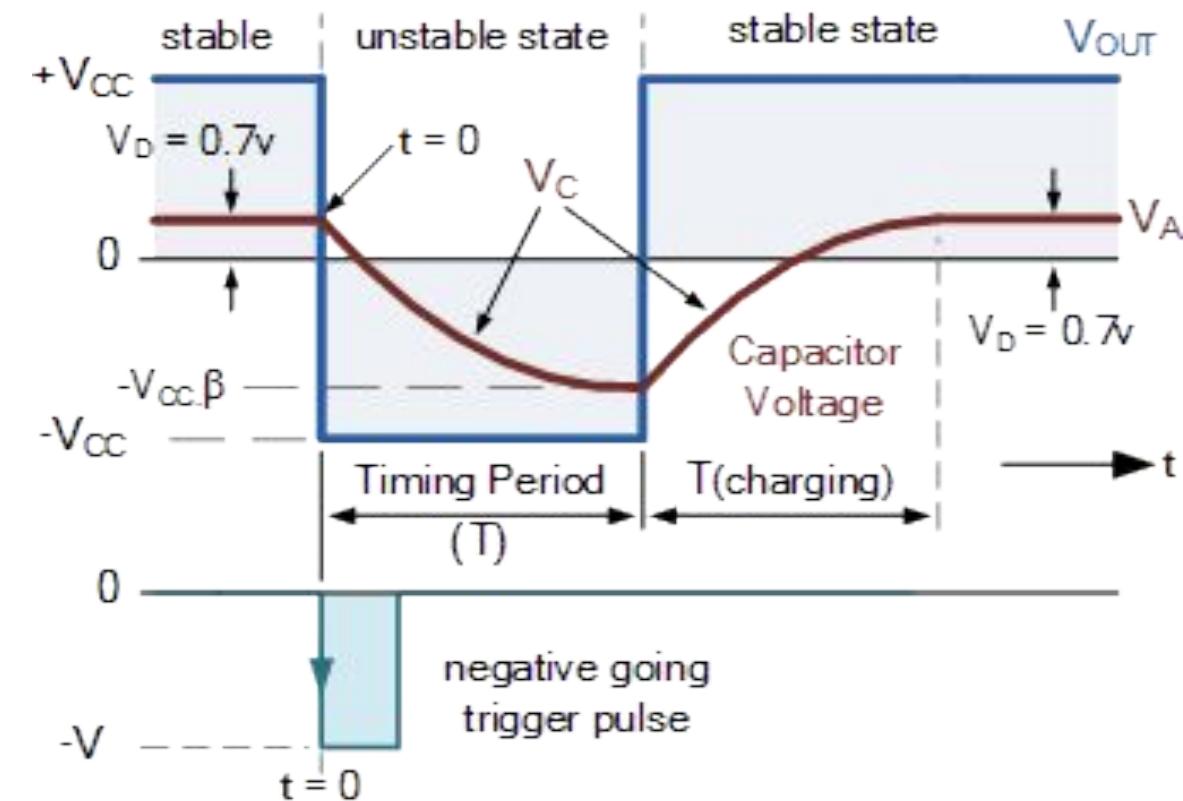
# Monostable Multivibrator

- If we were to apply a negative pulse to the non-inverting input, the 0.7v voltage at  $V_A$  now becomes greater than the voltage at  $V_B$  since  $V_B$  is now negative. Thus the output of the Schmitt configured op-amp switches state and saturates towards the negative supply rail,  $-V_{cc}$ . The result is that the potential at  $V_B$  is now equal to  $-V_{cc} \cdot \beta$ .
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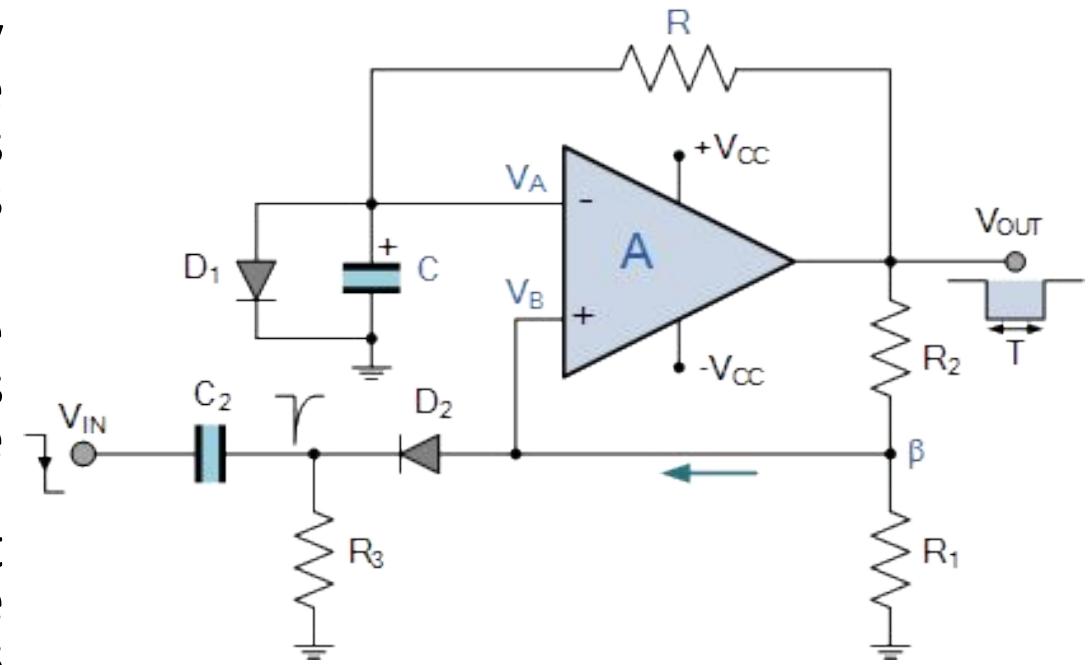
# Waveform

- Note that once the timing period is complete and the op-amps output changes back to its stable state and saturates towards the positive supply rail, the capacitor tries to charge up in reverse to  $+V_{CC}$  but can only charge to a maximum value of  $0.7v$  given by the diodes forward voltage drop. We can show this effect graphically as:
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- For the circuit,  $V_f = -V_{sat}$ , and  $V_i = V_D$ ;  $v_c = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$
- At  $t = T$   $v_c = -\beta V_{sat}$  then  $-\beta V_{sat} = -V_{sat} + (V_D + V_{sat}) e^{-T/RC}$
- Pulse width  $T$  
$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1 - \beta}$$
- If,  $V_{sat} \gg V_D$   $R_1 = R_2$  so that  $\beta = 0.5$ ,  $T = 0.69RC$

# 555 Timer

---

- IC's especially are designed to accurately produce the required output waveform with the addition of just a few extra timing components.
- One such device is the **555 Timer Oscillator** which is more commonly called the "**555 Timer**"
- The basic **555 timer** gets its name from the fact that there are three internally connected  $5k\Omega$  resistors which it uses to generate the two comparators reference voltages.
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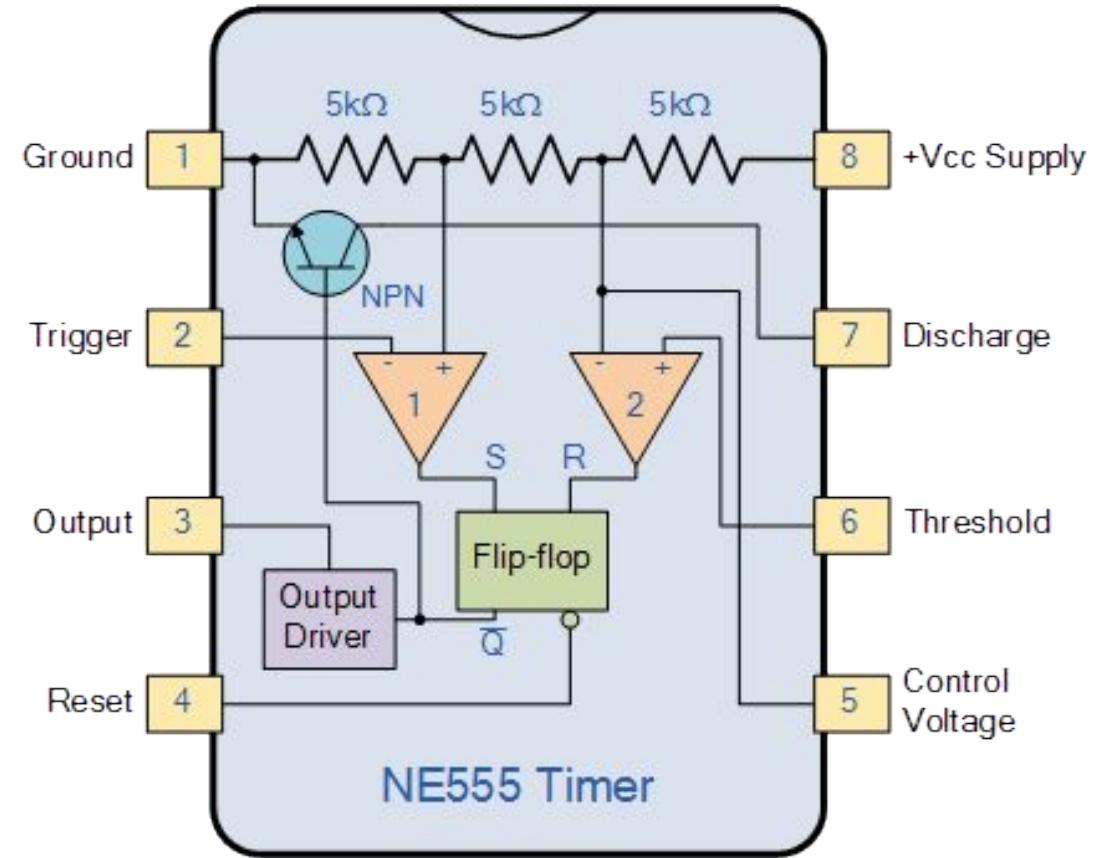
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- To produce a variety of applications such as one-shot or delay timers, pulse generation, LED and lamp flashers, alarms and tone generation, logic clocks, frequency division, power supplies and converters etc.
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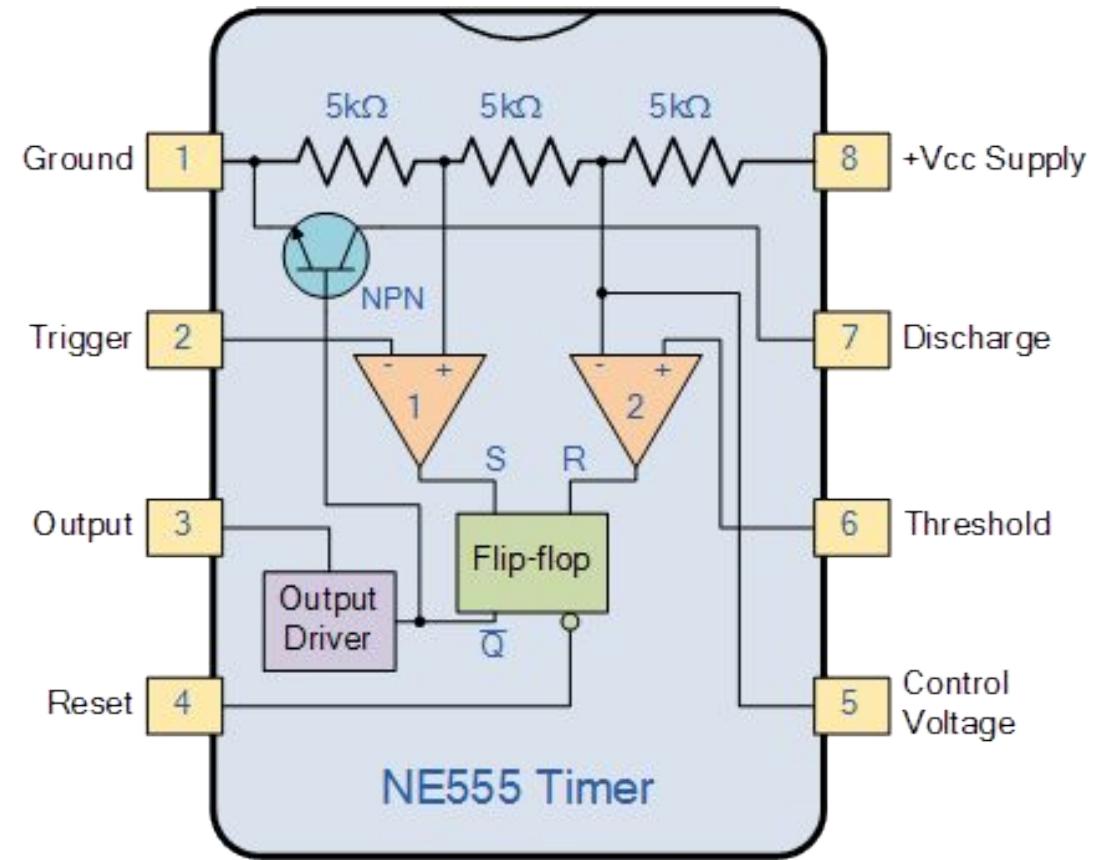
# 555 Timer Block Diagram

- Pin 1. – **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.
- Pin 2. – **Trigger**, The negative input to comparator No 1. A negative pulse on this pin “sets” the internal Flip-flop when the voltage drops below  $1/3V_{cc}$  causing the output to switch from a “LOW” to a “HIGH” state.
- Pin 3. – **Output**, The output pin is capable of sourcing or sinking up to 200mA of current at an output voltage so small speakers, LEDs or motors can be connected directly to the output.
- Pin 4. – **Reset**, This pin is used to “reset” the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic “1” level when not used to prevent any unwanted resetting of the output.



# 555 Timer Block Diagram

- Pin 5. – **Control Voltage**, This pin controls the timing of the 555 by overriding the  $2/3V_{cc}$  level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a  $10nF$  capacitor to eliminate any noise.
- Pin 6. – **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds  $2/3V_{cc}$  causing the output to switch from “HIGH” to “LOW” state. This pin connects directly to the RC timing circuit.
- Pin 7. – **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to “discharge” the timing capacitor to ground when the output at pin 3 switches “LOW”.
- Pin 8. – **Supply +V<sub>cc</sub>**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

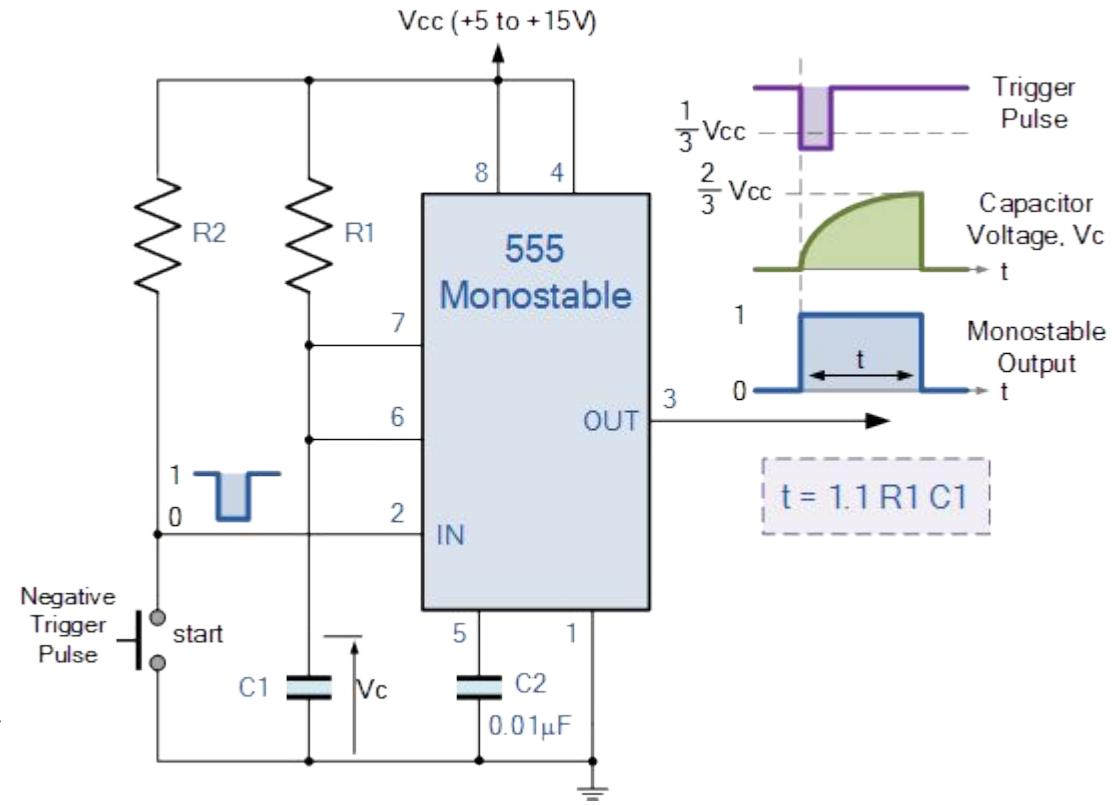


# 555 Timer Basic Operation

- The **555 Timers** name comes from the fact that there are three  $5\text{k}\Omega$  resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1.
- The voltage across this series resistive network holds the inverting input of comparator two at  $2/3V_{cc}$  and the non-inverting input to comparator one at  $1/3V_{cc}$ .
- The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network.
- The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a “HIGH” or “LOW” level output at Q based on the states of its inputs.
- The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a “HIGH” or “LOW” voltage level at the output pin.

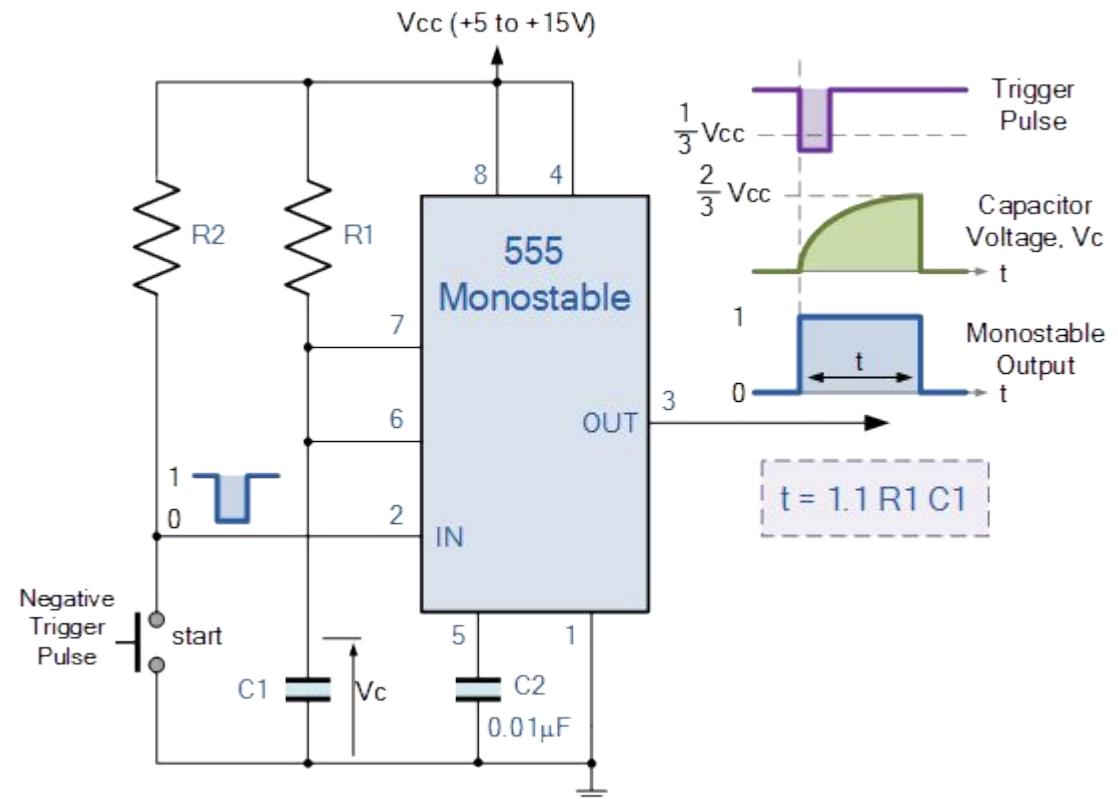
# Monostable multivibrator using 555 timer

- This is the basic mode of operation of the IC 555. It requires only two extra components to make it work as a monostable multivibrator: a resistor and a capacitor.
- When a negative ( 0V ) pulse is applied to the trigger input (pin 2) of the Monostable configured 555 Timer oscillator, the internal comparator, (comparator No1) detects this input and “sets” the state of the flip-flop, changing the output from a “LOW” state to a “HIGH” state.
- This action in turn turns “OFF” the discharge transistor connected to pin 7, thereby removing the short circuit across the external timing capacitor, C1.



# Monostable Operation

- This action allows the timing capacitor to start to charge up through resistor, R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of  $2/3V_{cc}$  set up by the internal voltage divider network.
- At this point the comparators output goes “HIGH” and “resets” the flip-flop back to its original state which in turn turns “ON” the transistor and discharges the capacitor to ground through pin 7.
- This causes the output to change its state back to the original stable “LOW” value awaiting another trigger pulse to start the timing process over again.
- Then as before, the Monostable Multivibrator has only “ONE” stable state.



# Time period

---

- The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully.
- Once triggered, the 555 Monostable will remain in this “HIGH” unstable output state until the time period set up by the  $R_1 \times C_1$  network has elapsed.
- The amount of time that the output voltage remains “HIGH” or at a logic “1” level, is given by the following time constant equation.

$$\tau = 1.1 R_1 C_1$$

# Pulse Width Calculation

---

- The voltage across the capacitor is,

$$v_c = V_f + (V_i - V_f) e^{-t/R_1 C_1}$$

- $V_f = +V_{CC}$ ,  $V_i = 0$  V, and the capacitor is charging to  $V_c = 2/3(V_{CC})$ :

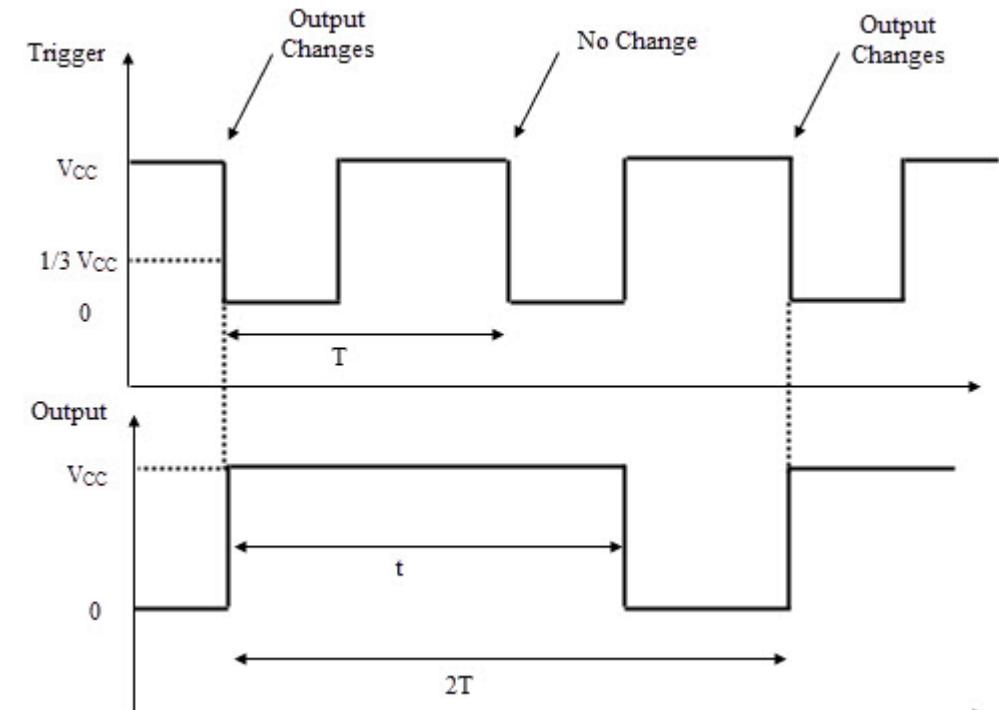
$$\frac{2}{3}V_{CC} = V_{CC} - V_{CC} e^{-t/R_1 C_1}$$

$$\frac{2}{3} = 1 - e^{-t/R_1 C_1} \quad e^{-t/R_1 C_1} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$-t / R_1 C_1 = \ln\left(\frac{1}{3}\right) = -1.098 \quad t = 1.1R_1 C_1$$

# Frequency Divider: Application of Monostable Multivibrator

- When the IC 555 is used as a monostable multivibrator, a positive going rectangular pulse is available at the output when a negative going pulse of short duration is applied at the trigger input.
- By adjusting the time interval  $t$  of the charging or timing circuit the device can be made to work as a Frequency Divider circuit.
- If the timing interval  $t$  is made slightly larger than the time period of the input pulse (trigger pulse), the device can act as a Divide – by – two circuit.
- The timing interval can be controlled by appropriately choosing the values of the resistor  $R$  and the capacitor  $C$  in the timing circuit. The waveforms of the input and output signals corresponding to the divide-by-two circuit are shown here.
- The circuit will trigger for the first negative pulse of the trigger input. As a result, the output will go to high state. The output will remain high for the time interval  $t$ .
- During this interval, even if a second negative going trigger pulse is applied, the output will not be affected and continues to remain high as the timing interval is greater than the time period of the trigger pulse. On the third negative going trigger pulse, the circuit is retriggered.



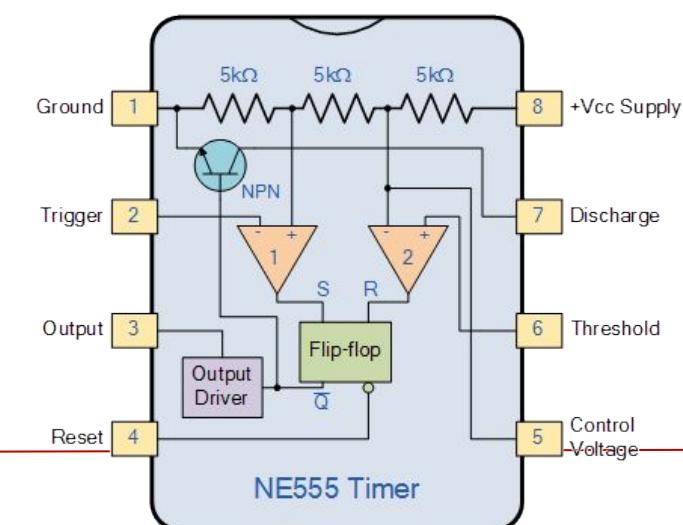
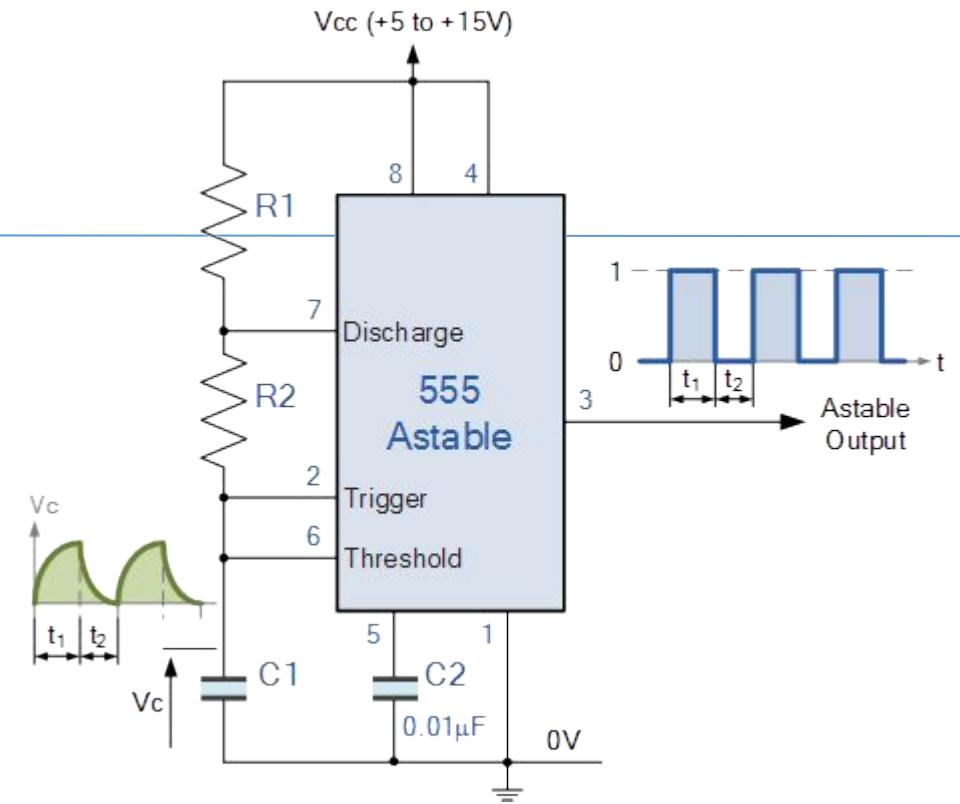
# 555 Timer: Astable Multivibrator

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- The **555 Timer IC** can be connected in its Monostable mode thereby producing a precision timer of a fixed time duration
- the 555 timer IC in an Astable mode to produce a very stable **555 Oscillator** circuit for generating highly accurate free running waveforms whose output frequency can be adjusted by means of an externally connected RC tank circuit consisting of just two resistors and a capacitor.
- It has no stable states as it continuously switches from one state to the other

# Operation

- In the **555 Oscillator** circuit, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator.
- During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the *discharge* terminal, pin 7.
- Then the capacitor charges up to  $2/3V_{cc}$  (the upper comparator limit) which is determined by the  $(R_1+R_2)$  combination and discharges itself down to  $1/3V_{cc}$  (the lower comparator limit) determined by the R2.
- This results in an output waveform whose output “ON” and “OFF” time periods are determined by the capacitor and resistors combinations.



# Time period

- Charging time ( $t_1$ ) and discharge time ( $t_2$ ):

$$t_1 = 0.693(R_1 + R_2) \cdot C$$

and

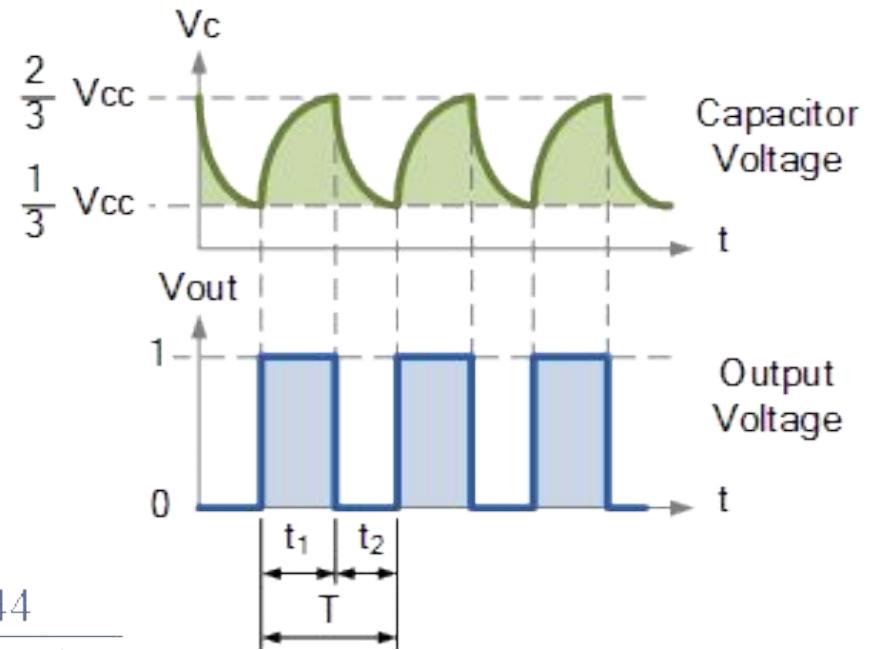
$$t_2 = 0.693 \times R_2 \times C$$

- Total time period and frequency:

$$T = t_1 + t_2 = 0.693(R_1 + 2R_2) \cdot C \quad f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) \cdot C}$$

- Duty cycle:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$



# Example:

- An **Astable 555 Oscillator** is constructed using the following components,  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 2\text{k}\Omega$  and capacitor  $C = 10\text{uF}$ . Calculate the output frequency from the 555 oscillator and the duty cycle of the output waveform.

$t_1$  – capacitor charge “ON” time is calculated as:

$$\begin{aligned}t_1 &= 0.693(R_1 + R_2).C \\&= 0.693(1000 + 2000) \times 10 \times 10^{-6} \\&= 0.021\text{s} = 21\text{ms}\end{aligned}$$

$t_2$  – capacitor discharge “OFF” time is calculated as:

$$\begin{aligned}t_2 &= 0.693 R_2.C \\&= 0.693 \times 2000 \times 10 \times 10^{-6} \\&= 0.014\text{s} = 14\text{ms}\end{aligned}$$

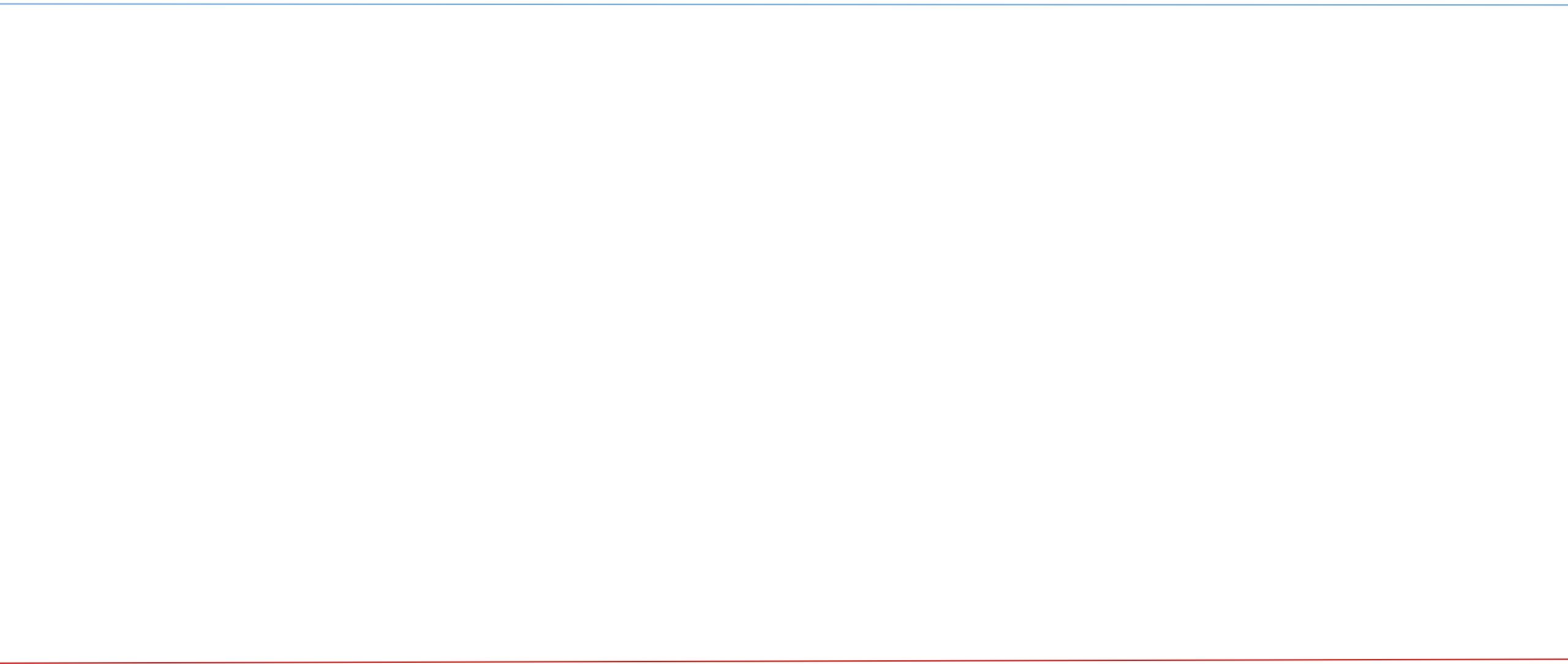
$$T = t_1 + t_2 = 21\text{ms} + 14\text{ms} = 35\text{ms}$$

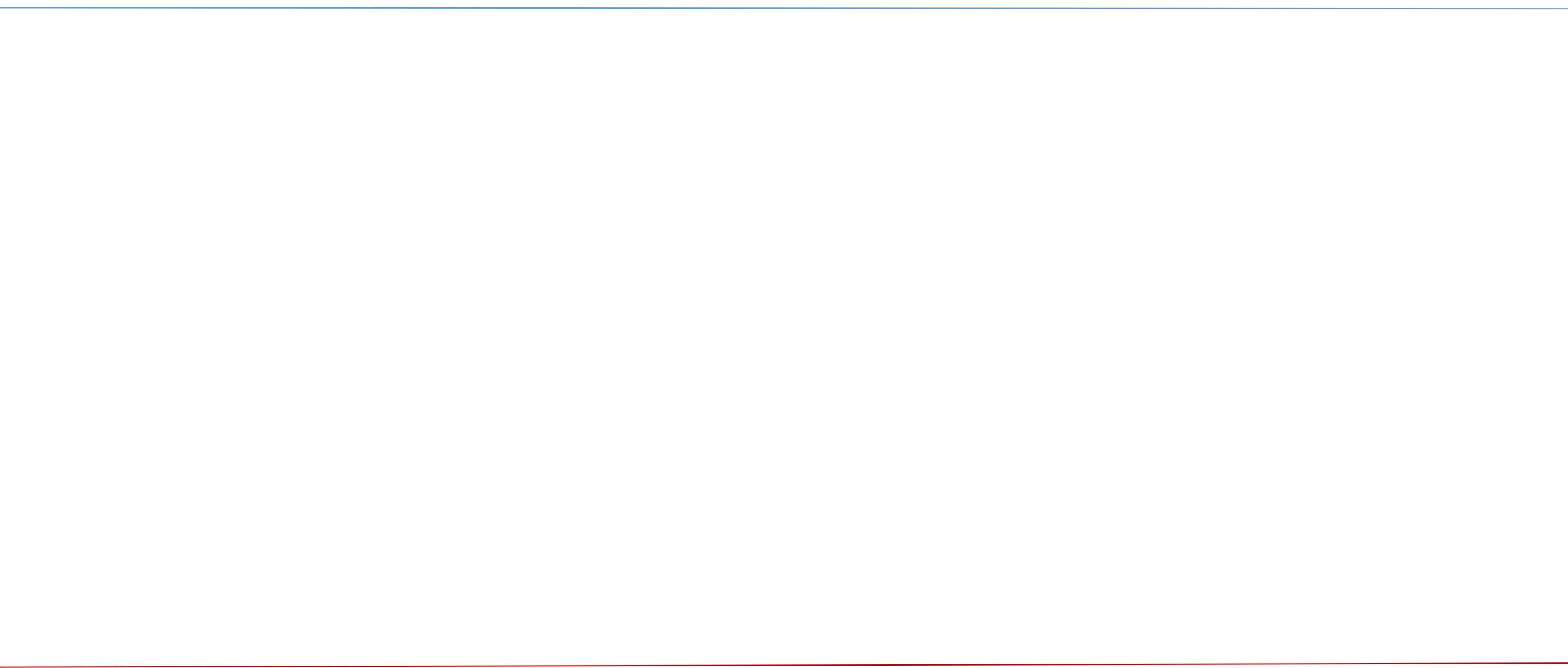
$$f = \frac{1}{T} = \frac{1}{35\text{ms}} = 28.6\text{Hz}$$

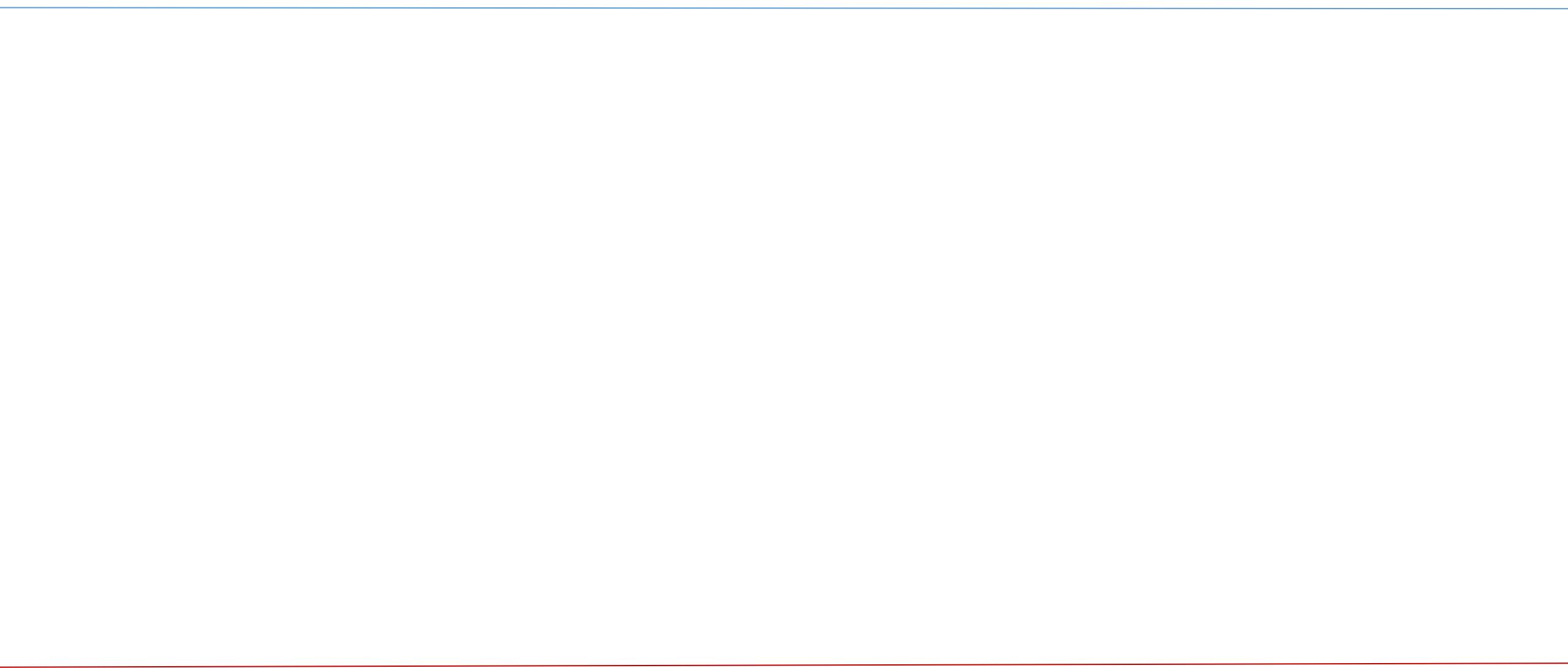
Giving a duty cycle value of:

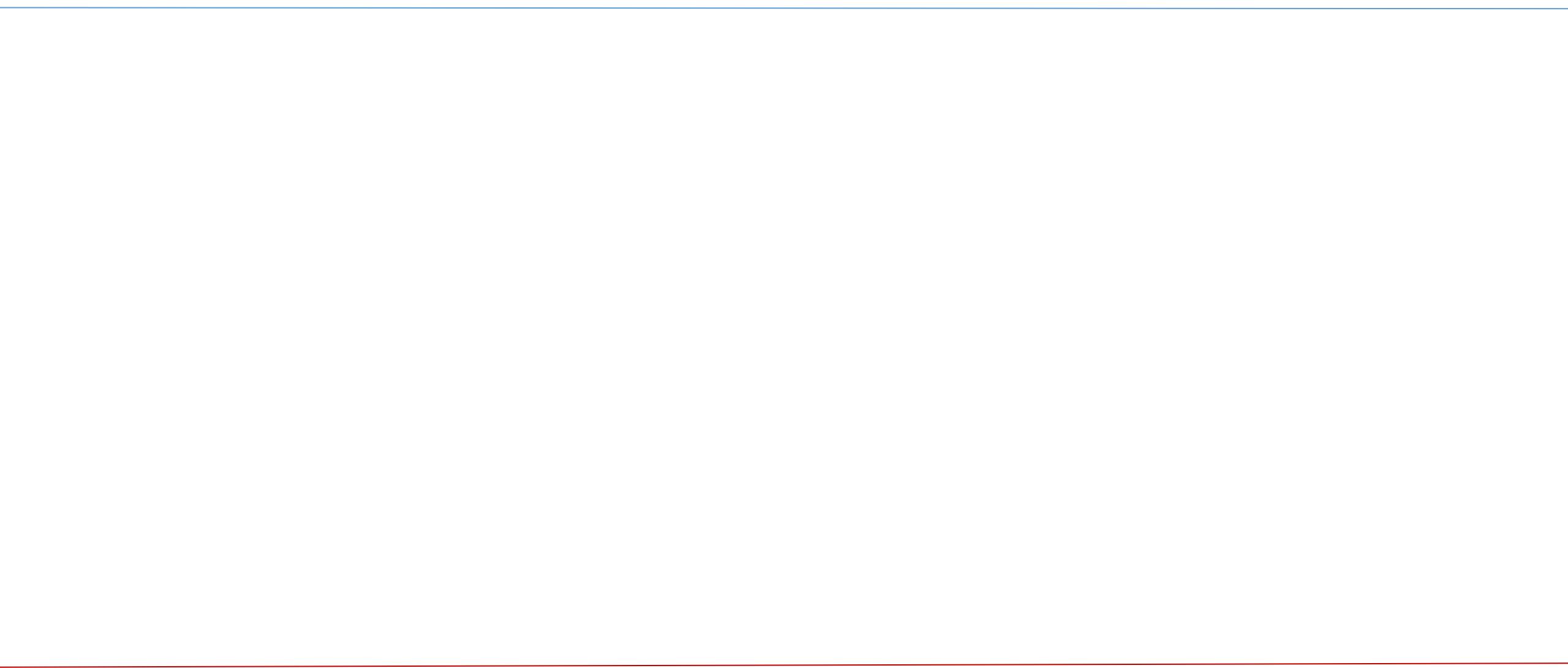
$$\text{Duty Cycle} = \frac{R_1 + R_2}{(R_1 + 2R_2)} = \frac{1000 + 2000}{(1000 + 2 \times 2000)} = 0.6 \text{ or } 60\%$$

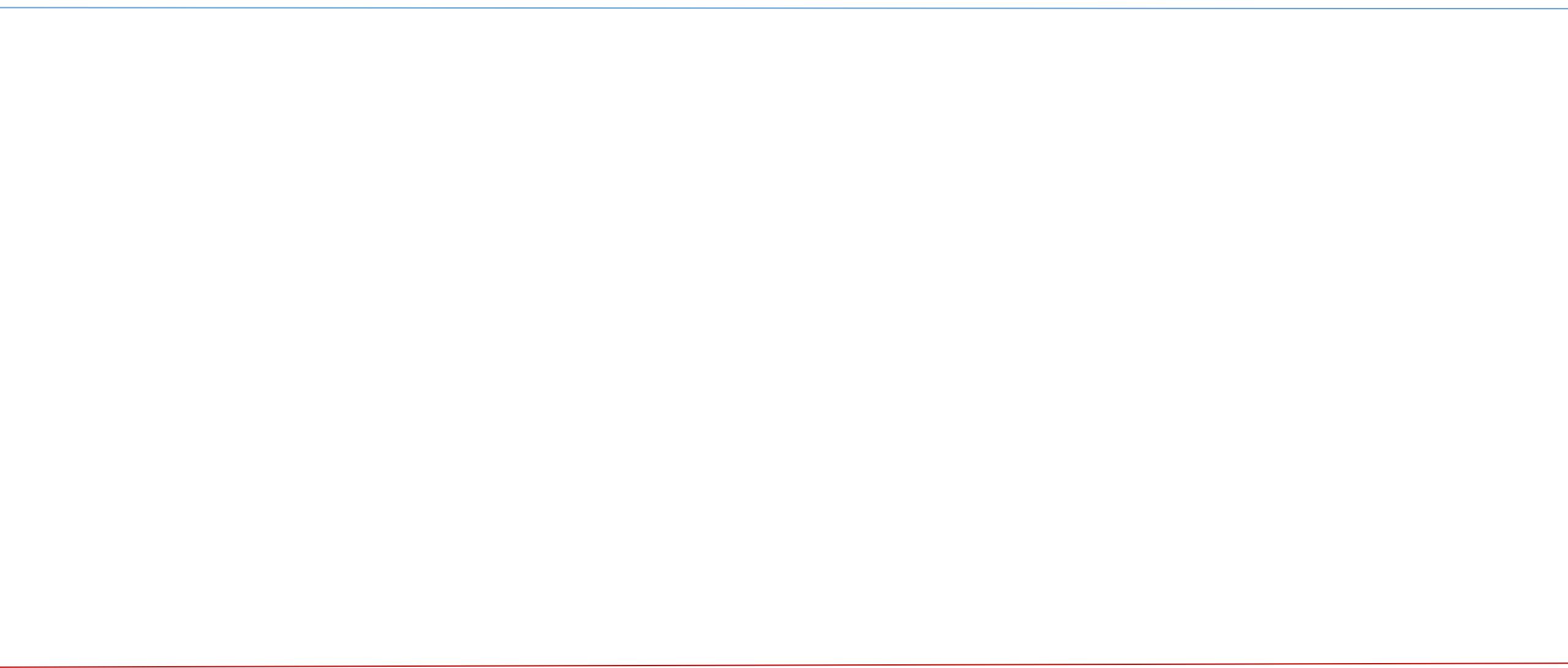
As the timing capacitor, C charges through resistors R1 and R2 but only discharges through resistor R2 the output duty cycle can be varied between 50 and 100% by changing the value of resistor R2. By decreasing the value of R2 the duty cycle increases towards 100% and by increasing R2 the duty cycle reduces towards 50%.













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# OP-AMP based Waveform Generators

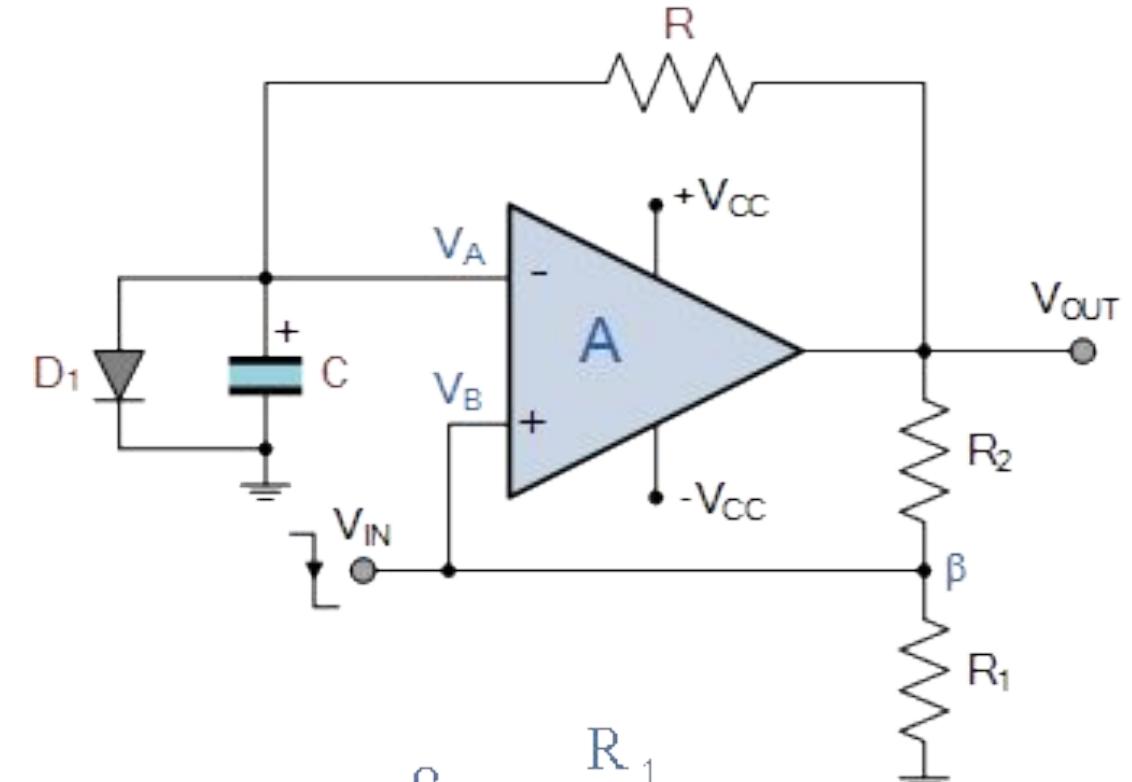
# Content

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- Comparator: inverting and non-inverting comparators
  - Applications: zero crossing detector, window detector
  - Sine wave generator
  - Schmitt trigger
  - square wave generator (Astable multivibrator)
  - Monostable Multivibrator
  - 555 timers: functional diagram and Monostable operation
-

# Monostable Multivibrator

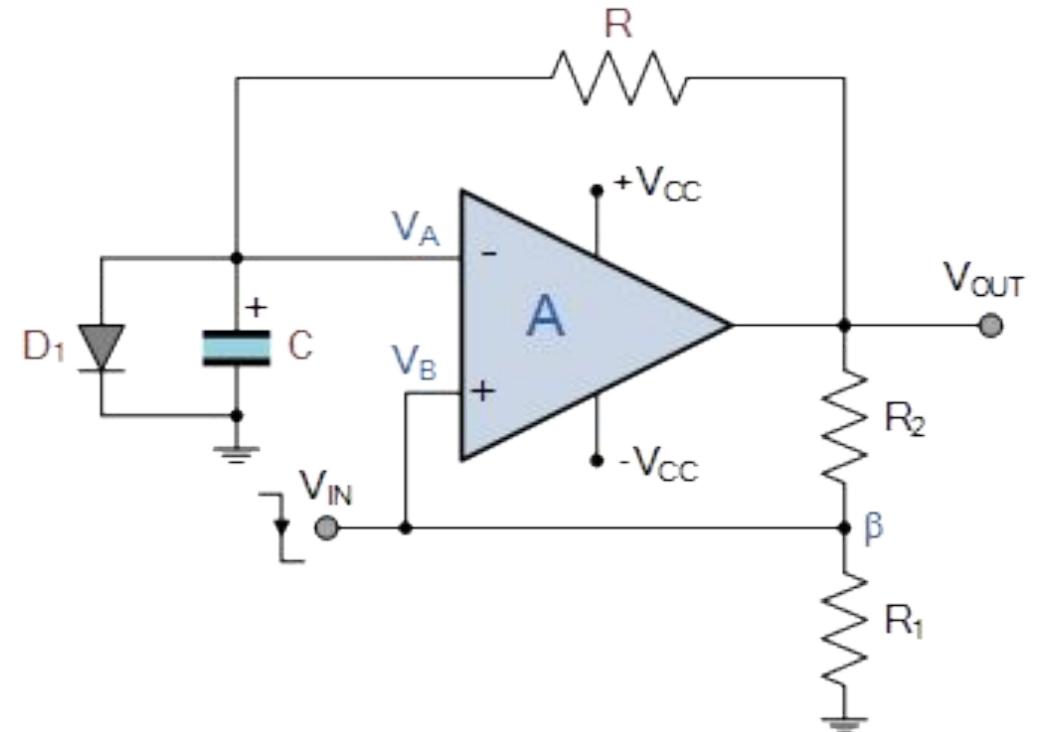
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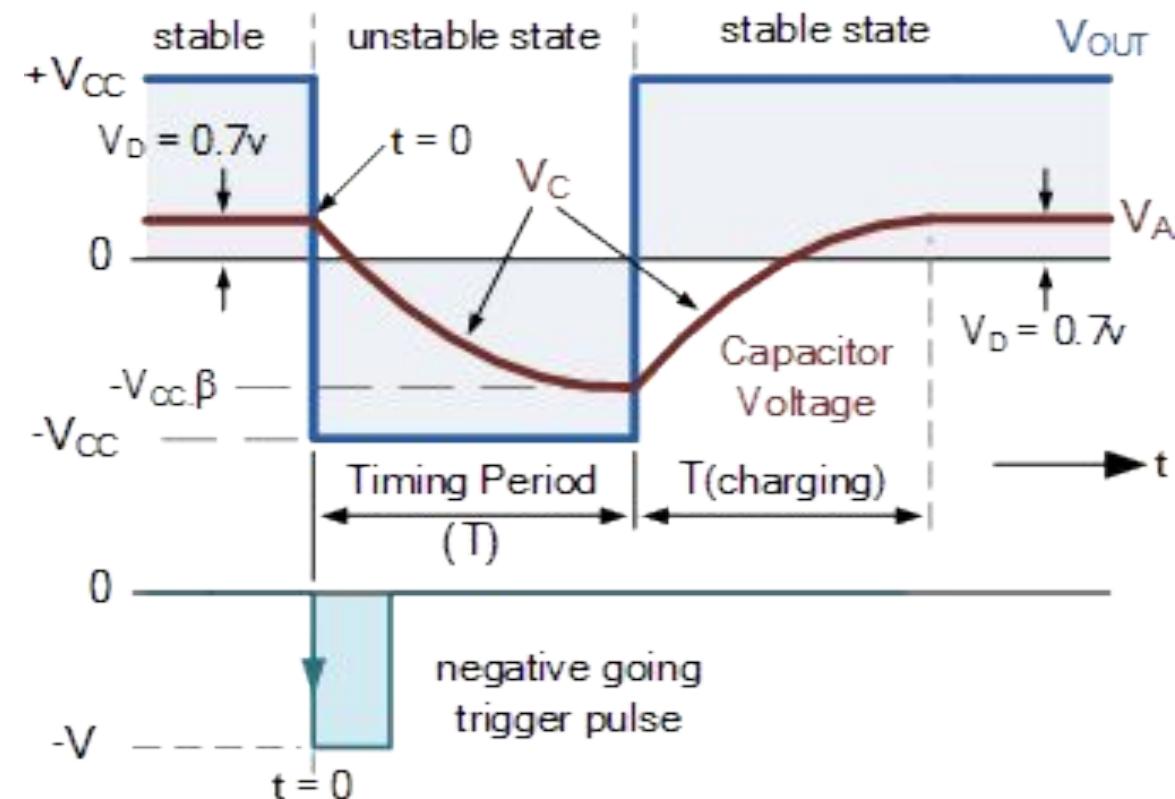
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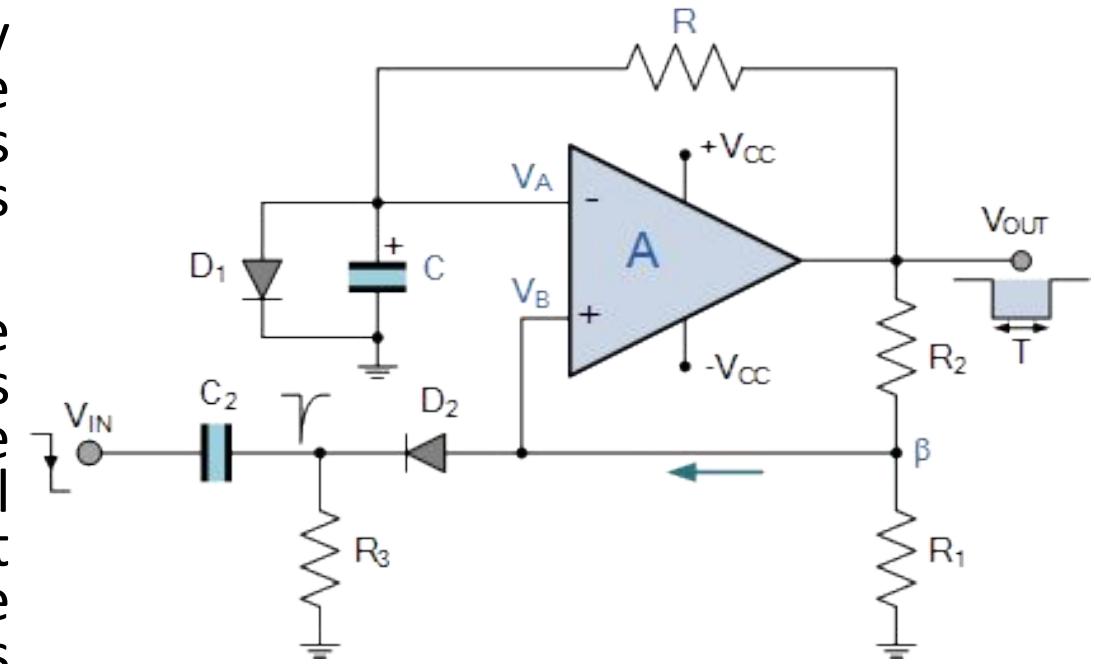
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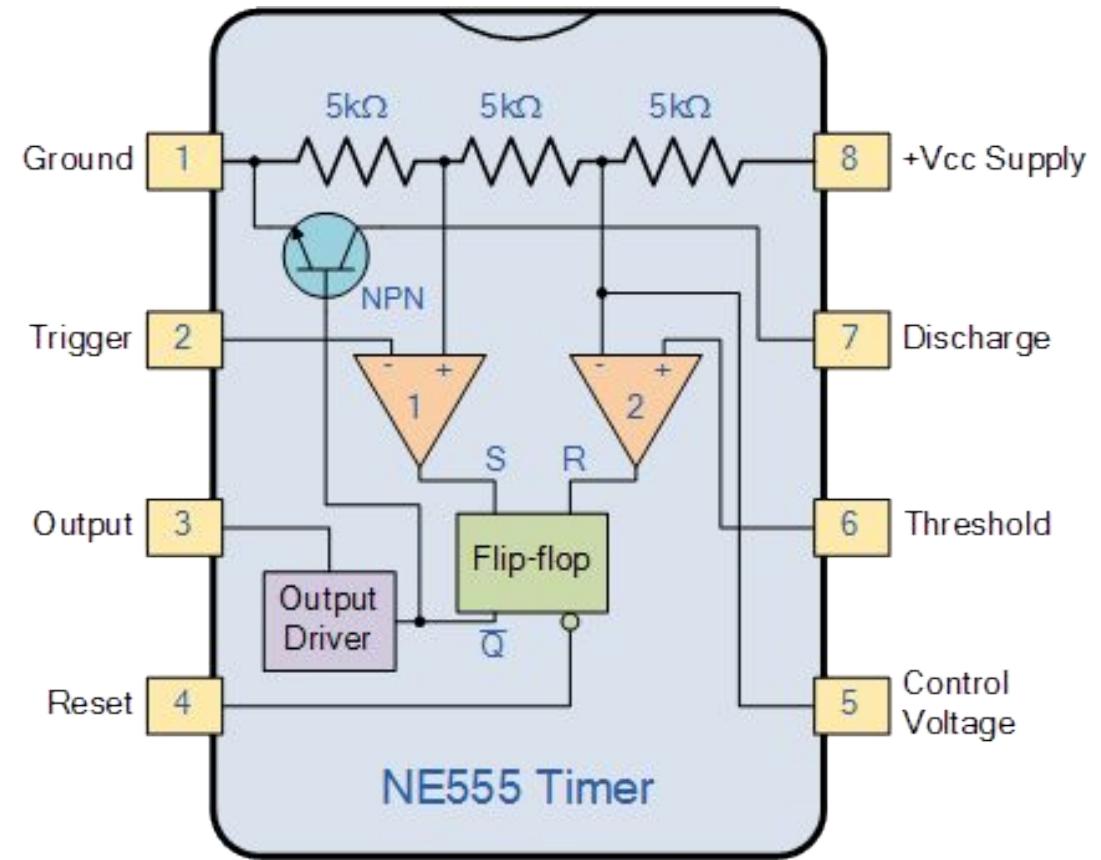
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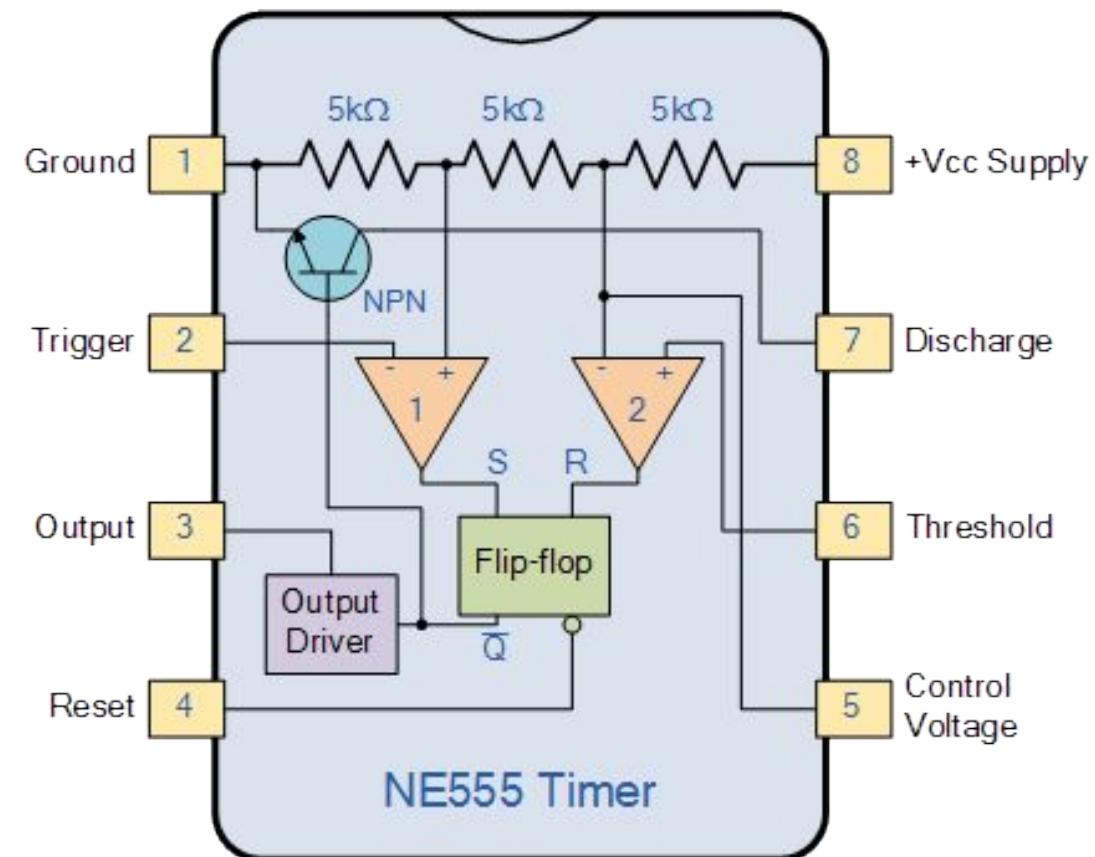
# 555 Timer Block Diagram

- Pin 1. – **Ground**, The ground pin connects the 555 timer to the negative (0v) supply rail.
- Pin 2. – **Trigger**, The negative input to comparator No 1. A negative pulse on this pin “sets” the internal Flip-flop when the voltage drops below  $1/3V_{cc}$  causing the output to switch from a “LOW” to a “HIGH” state.
- Pin 3. – **Output**, The output pin is capable of sourcing or sinking up to 200mA of current at an output voltage so small speakers, LEDs or motors can be connected directly to the output.
- Pin 4. – **Reset**, This pin is used to “reset” the internal Flip-flop controlling the state of the output, pin 3. This is an active-low input and is generally connected to a logic “1” level when not used to prevent any unwanted resetting of the output.



# 555 Timer Block Diagram

- Pin 5. – **Control Voltage**, This pin controls the timing of the 555 by overriding the  $2/3V_{cc}$  level of the voltage divider network. By applying a voltage to this pin the width of the output signal can be varied independently of the RC timing network. When not used it is connected to ground via a  $10nF$  capacitor to eliminate any noise.
  - Pin 6. – **Threshold**, The positive input to comparator No 2. This pin is used to reset the Flip-flop when the voltage applied to it exceeds  $2/3V_{cc}$  causing the output to switch from “HIGH” to “LOW” state. This pin connects directly to the RC timing circuit.
  - Pin 7. – **Discharge**, The discharge pin is connected directly to the Collector of an internal NPN transistor which is used to “discharge” the timing capacitor to ground when the output at pin 3 switches “LOW”.
  - Pin 8. – **Supply +V<sub>cc</sub>**, This is the power supply pin and for general purpose TTL 555 timers is between 4.5V and 15V.

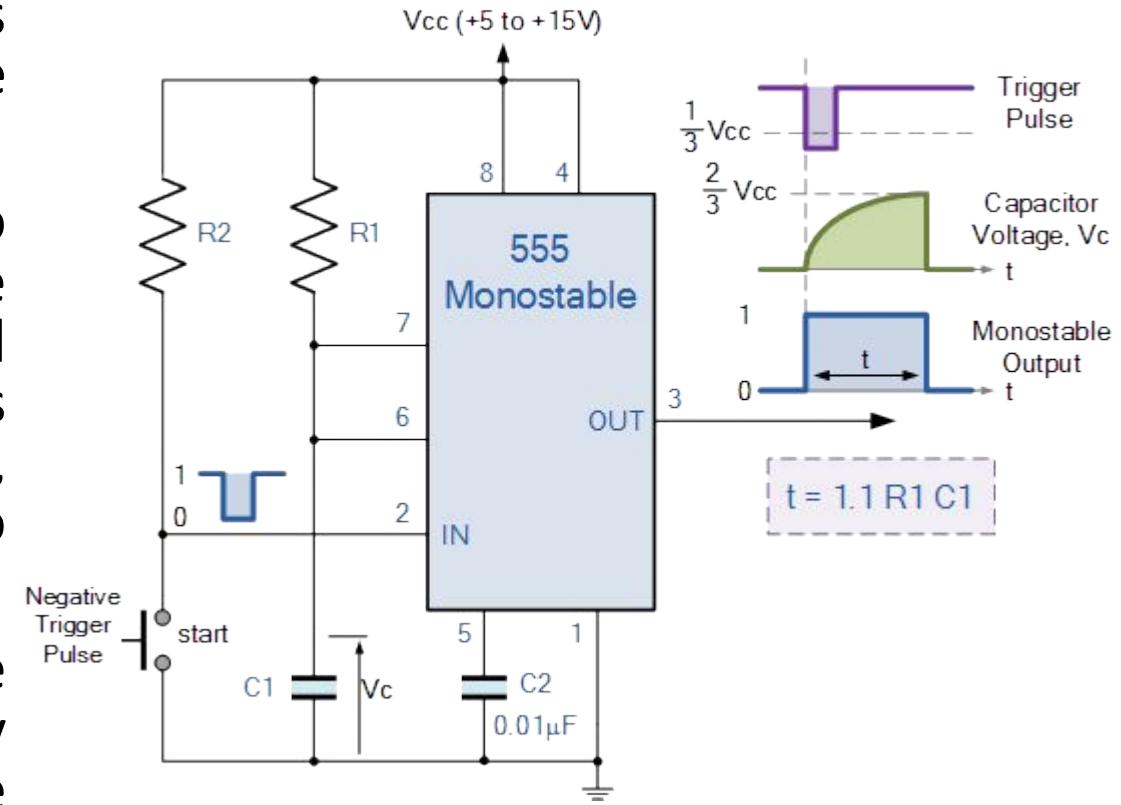


# 555 Timer Basic Operation

- The **555 Timers** name comes from the fact that there are three  $5\text{k}\Omega$  resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1.
- The voltage across this series resistive network holds the inverting input of comparator two at  $2/3V_{cc}$  and the non-inverting input to comparator one at  $1/3V_{cc}$ .
- The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network.
- The outputs from both comparators are connected to the two inputs of the flip-flop which in turn produces either a “HIGH” or “LOW” level output at Q based on the states of its inputs.
- The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a “HIGH” or “LOW” voltage level at the output pin.

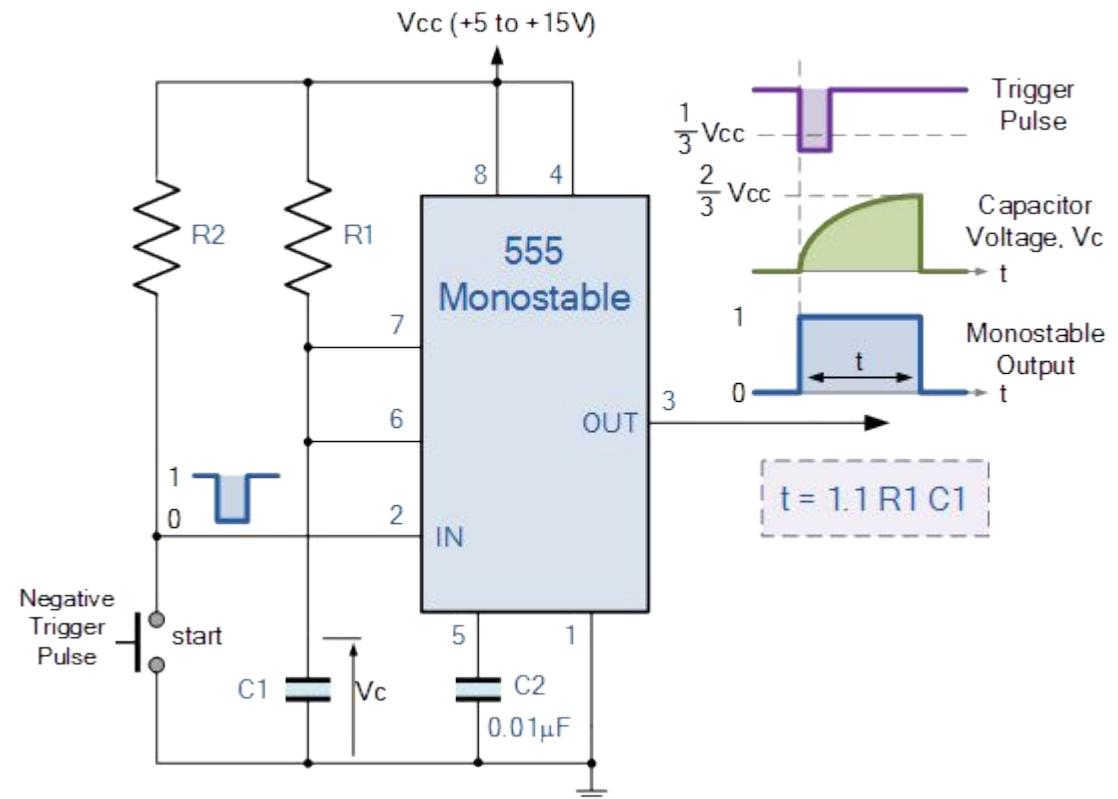
# Monostable multivibrator using 555 timer

- This is the basic mode of operation of the IC 555. It requires only two extra components to make it work as a monostable multivibrator: a resistor and a capacitor.
- When a negative ( 0V ) pulse is applied to the trigger input (pin 2) of the Monostable configured 555 Timer oscillator, the internal comparator, (comparator No1) detects this input and “sets” the state of the flip-flop, changing the output from a “LOW” state to a “HIGH” state.
- This action in turn turns “OFF” the discharge transistor connected to pin 7, thereby removing the short circuit across the external timing capacitor, C1.



# Monostable Operation

- This action allows the timing capacitor to start to charge up through resistor, R1 until the voltage across the capacitor reaches the threshold (pin 6) voltage of  $2/3V_{cc}$  set up by the internal voltage divider network.
- At this point the comparators output goes “HIGH” and “resets” the flip-flop back to its original state which in turn turns “ON” the transistor and discharges the capacitor to ground through pin 7.
- This causes the output to change its state back to the original stable “LOW” value awaiting another trigger pulse to start the timing process over again.
- Then as before, the Monostable Multivibrator has only “ONE” stable state.



# Time period

---

- The **Monostable 555 Timer** circuit triggers on a negative-going pulse applied to pin 2 and this trigger pulse must be much shorter than the output pulse width allowing time for the timing capacitor to charge and then discharge fully.
- Once triggered, the 555 Monostable will remain in this “HIGH” unstable output state until the time period set up by the  $R_1 \times C_1$  network has elapsed.
- The amount of time that the output voltage remains “HIGH” or at a logic “1” level, is given by the following time constant equation.

$$\tau = 1.1 R_1 C_1$$

# Pulse Width Calculation

---

- The voltage across the capacitor is,

$$v_c = V_f + (V_i - V_f) e^{-t/R_1 C_1}$$

- $V_f = +V_{CC}$ ,  $V_i = 0$  V, and the capacitor is charging to  $V_c = 2/3(V_{CC})$ :

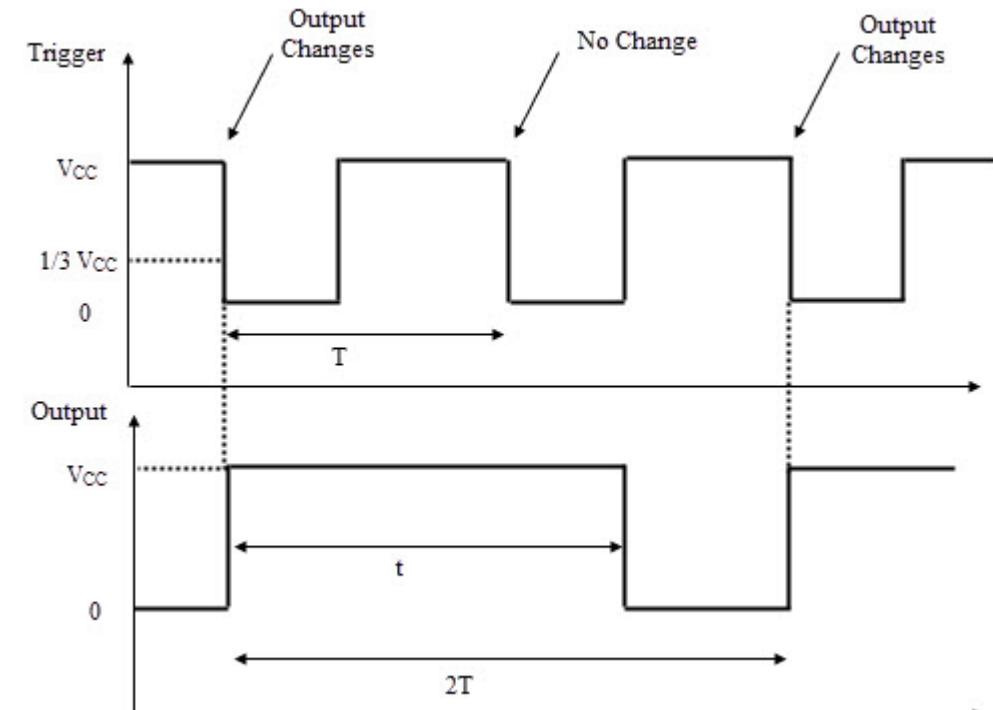
$$\frac{2}{3}V_{CC} = V_{CC} - V_{CC} e^{-t/R_1 C_1}$$

$$\frac{2}{3} = 1 - e^{-t/R_1 C_1} \quad e^{-t/R_1 C_1} = 1 - \frac{2}{3} = \frac{1}{3}$$

$$-t / R_1 C_1 = \ln\left(\frac{1}{3}\right) = -1.098 \quad t = 1.1R_1 C_1$$

# Frequency Divider: Application of Monostable Multivibrator

- When the IC 555 is used as a monostable multivibrator, a positive going rectangular pulse is available at the output when a negative going pulse of short duration is applied at the trigger input.
- By adjusting the time interval  $t$  of the charging or timing circuit the device can be made to work as a Frequency Divider circuit.
- If the timing interval  $t$  is made slightly larger than the time period of the input pulse (trigger pulse), the device can act as a Divide – by – two circuit.
- The timing interval can be controlled by appropriately choosing the values of the resistor  $R$  and the capacitor  $C$  in the timing circuit. The waveforms of the input and output signals corresponding to the divide-by-two circuit are shown here.
- The circuit will trigger for the first negative pulse of the trigger input. As a result, the output will go to high state. The output will remain high for the time interval  $t$ .
- During this interval, even if a second negative going trigger pulse is applied, the output will not be affected and continues to remain high as the timing interval is greater than the time period of the trigger pulse. On the third negative going trigger pulse, the circuit is retriggered.





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# Analog to Digital and Digital to Analog Converters

# Contents

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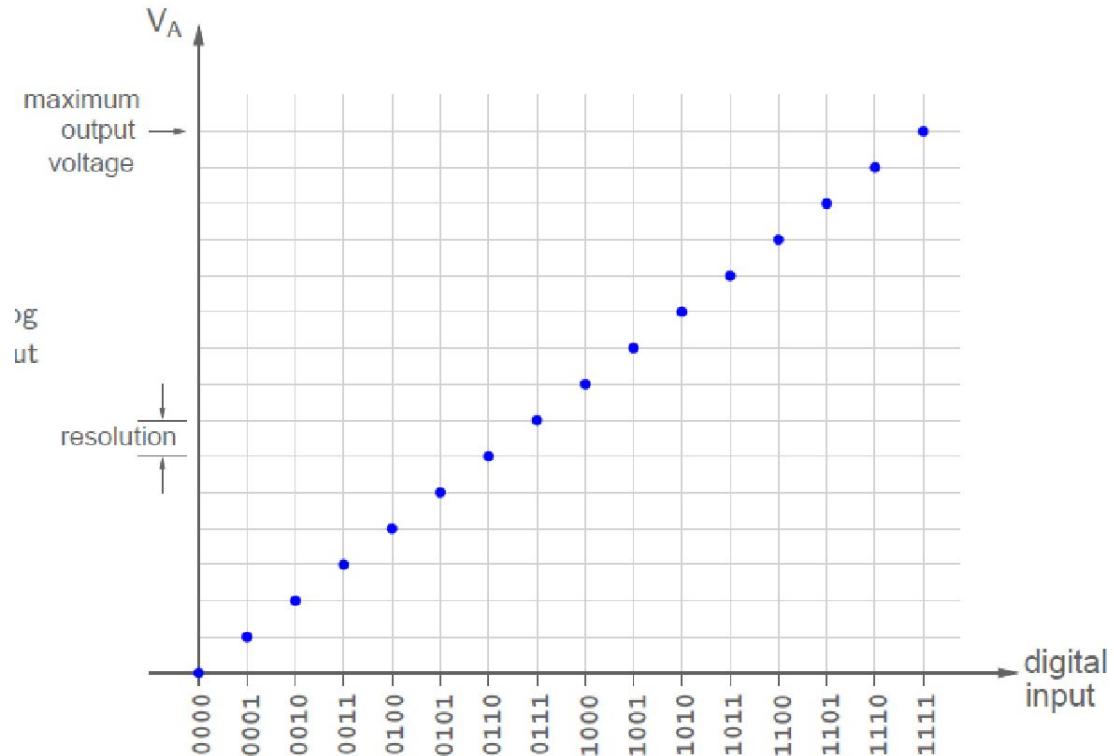
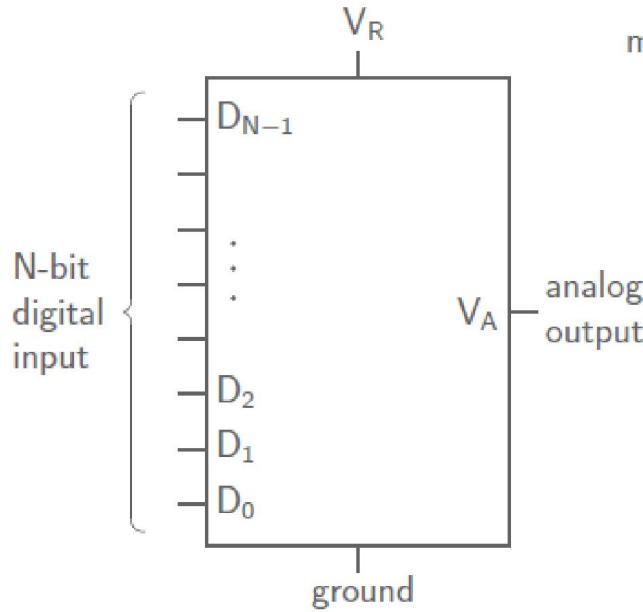
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  - Counting ADC

# Introduction

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- Physical quantities (e.g., Temperature, a voltage or a speech signal) are analog in nature, varying continuously with time.
  - Digital format offers several advantages: digital signal processing, storage, use of computers, robust transmission, etc.
  - An ADC (Analog-to-Digital Converter) is used to convert an analog signal to the digital format.
  - The reverse conversion (from digital to analog) is also required. For example, music stored in a DVD in digital format must be converted to an analog voltage for playing out on a speaker.
  - A DAC (Digital-to-Analog Converter) is used to convert a digital signal to the analog format.
-

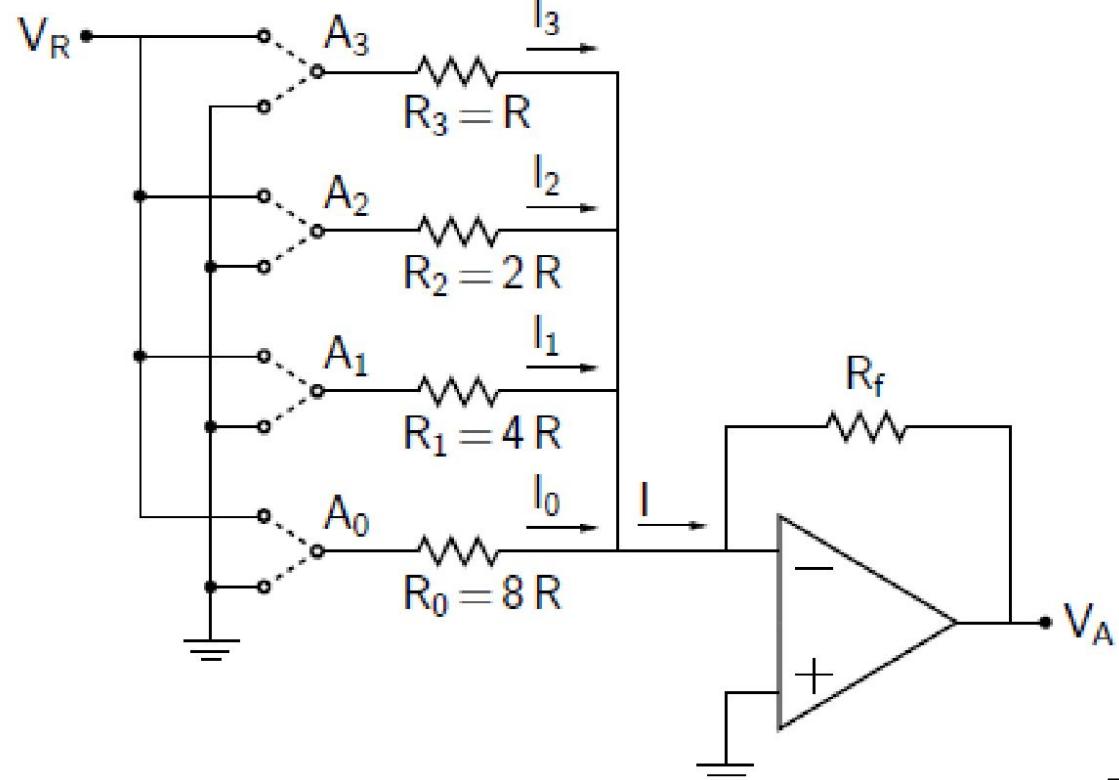
# Digital to Analog Converters



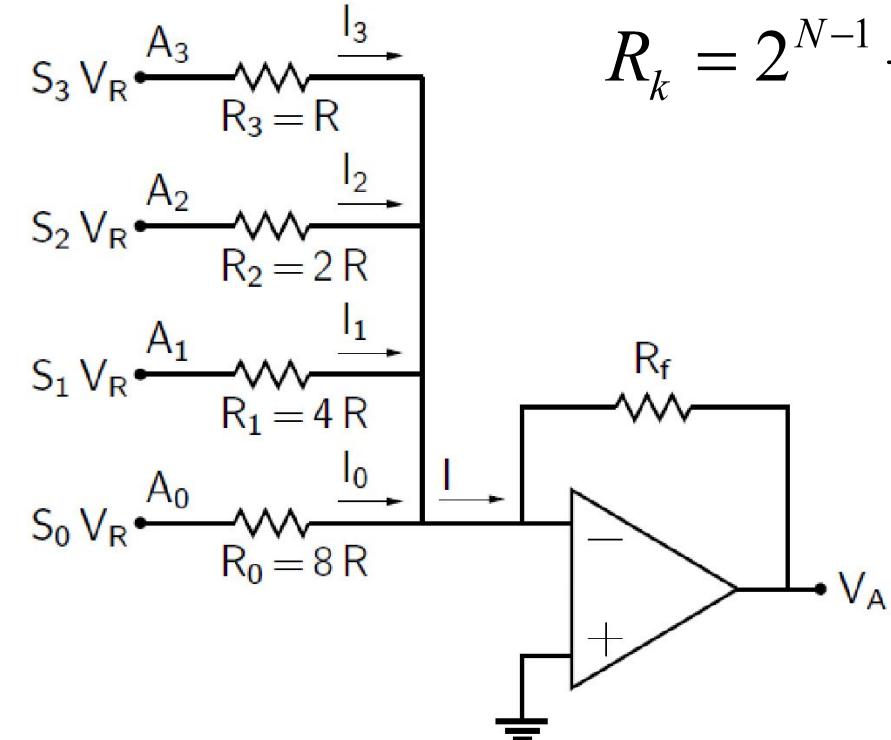
For a 4-bit DAC, with input  $S_3 S_2 S_1 S_0$ , the output voltage is  $V_A = K [(S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0)]$ . In general,  $V_A = K \sum_0^{N-1} S_k 2^k$ .

K is proportional to the reference voltage  $V_R$ . Its value depends on how the DAC is implemented.

# DAC using Binary-weighted resistors



$$I = I_0 + I_1 + I_2 + I_3$$



$$I_0 = \frac{S_0 V_R}{R_0} \quad I_1 = \frac{S_1 V_R}{R_1}$$

$$R_k = 2^{N-1} \frac{R}{2^k}$$

# DAC using Binary-weighted resistors

---

If the input bit  $S_k$  is 1,  $A_k$  gets connected to  $V_R$ ; else, it gets connected to ground.  
 $\rightarrow V(A_k) = S_k \times V_R$ .

Since the inverting terminal of the Op Amp is at virtual ground,

$$I_k = \frac{V(A_k) - 0}{R_k} = \frac{S_k V_R}{R_k}.$$

Using  $R_k = 2^{N-1} R / 2^k$ , we get  $I = \frac{V_R}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$  ( $N = 4$  here).

The output voltage is  $V_o = -R_f I = -V_R \frac{R_f}{2^{N-1} R} \sum_0^{N-1} S_k \times 2^k$ .

- Consider an 8-bit DAC with  $V_R = 5$  V. What is the smallest value of  $R$  which will limit the current drawn from the supply ( $V_R$ ) to 10 mA?

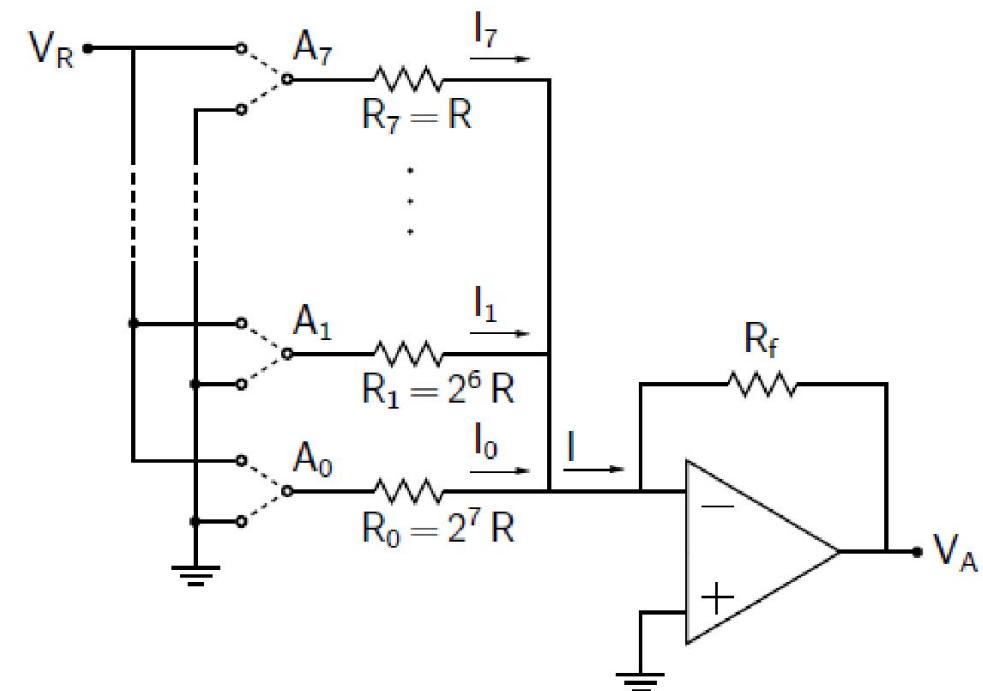
Maximum current is drawn from  $V_R$  when the input is 1111 1111.

→ All nodes  $A_0$  to  $A_7$  get connected to  $V_R$ .

$$\rightarrow 10 \text{ mA} = \frac{V_R}{R} + \frac{V_R}{2R} + \cdots + \frac{V_R}{2^7 R} = \frac{1}{2^7} \frac{V_R}{R} (2^0 + 2^1 + \cdots + 2^7)$$

$$= \frac{1}{2^7} \frac{V_R}{R} (2^8 - 1) = \frac{255}{128} \frac{V_R}{R}$$

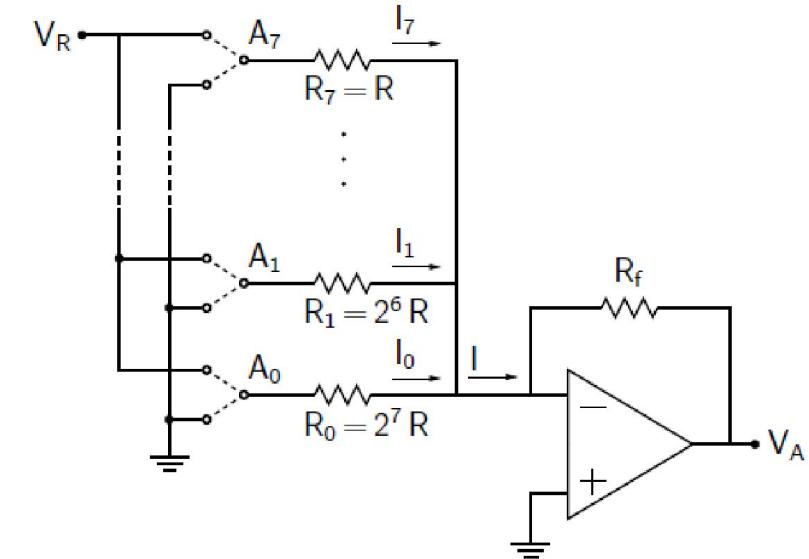
$$\rightarrow R_{\min} = \frac{5 \text{ V}}{10 \text{ mA}} \times \frac{255}{128} = 996 \Omega .$$



- If  $R_f = R$ , what is the resolution (i.e.,  $V_A$  corresponding to the input LSB changing from 0 to 1 with other input bits constant)?

$$V_A = -V_R \frac{R_f}{2^{N-1}R} [S_72^7 + \dots + S_12^1 + S_02^0]$$

$$\rightarrow \Delta V_A = \frac{V_R}{2^{N-1}} \frac{R_f}{R} = \frac{5\text{V}}{2^{8-1}} \times 1 = \frac{5}{128} = 0.0391\text{V.}$$



- What is the maximum output voltage (in magnitude)?

$$V_A = -\frac{V_R}{2^{N-1}} \frac{R_f}{R} [S_72^7 + \dots + S_12^1 + S_02^0].$$

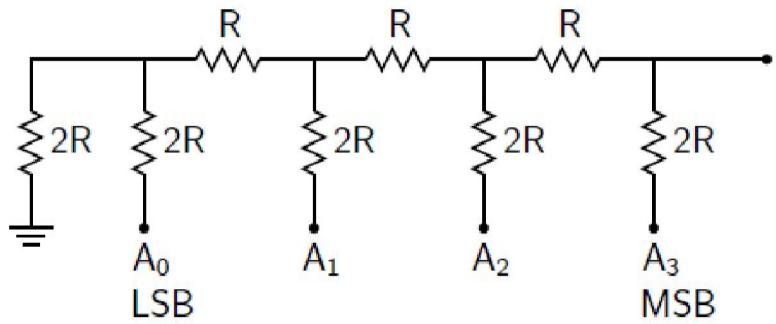
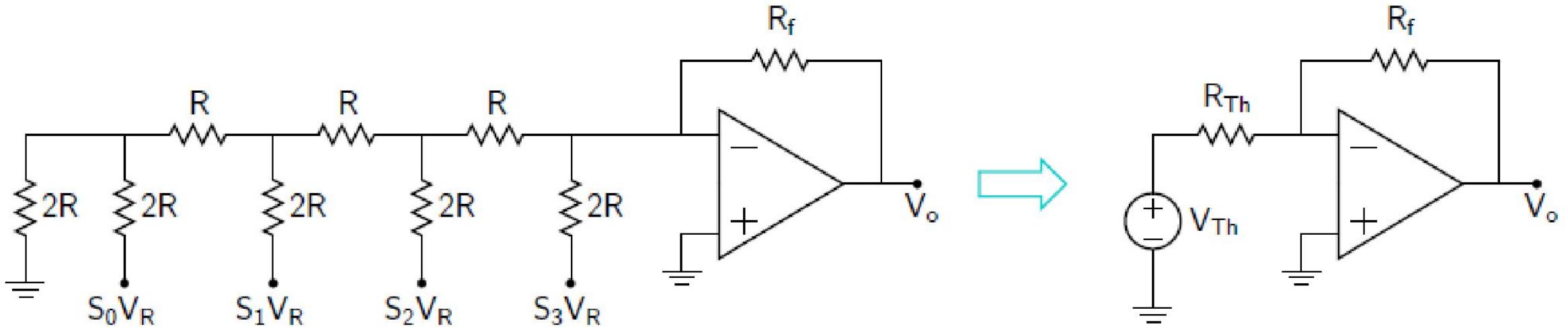
Maximum  $V_A$  (in magnitude) is obtained when the input is 1111 1111.

$$|V_A|_{\max} = \frac{5}{128} \times 1 \times [2^0 + 2^1 + \dots + 2^7] = \frac{5}{128} \times (2^8 - 1) = 5 \times \frac{255}{128} = 9.961\text{V.}$$

- Find the output voltage corresponding to the input 1010 1101.

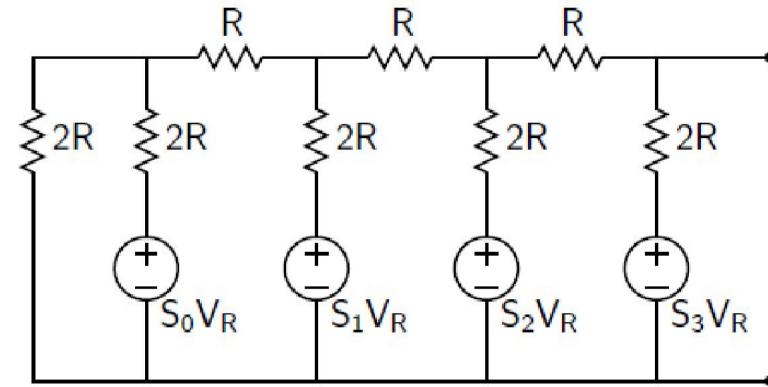
$$\begin{aligned}V_A &= -\frac{V_R}{2^{N-1}} \frac{R_f}{R} [s_7 2^7 + \dots + s_1 2^1 + s_0 2^0] \\&= -\frac{5}{128} \times 1 \times [2^7 + 2^5 + 2^3 + 2^2 + 2^0] = -5 \times \frac{173}{128} = -6.758 \text{ V}.\end{aligned}$$

# DAC with R-2R Ladder



Node  $A_k$  is connected to  $V_R$  if input bit  $S_k$  is 1; else, it is connected to ground.

The original network is equivalent to





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# OP-AMP based Waveform Generators

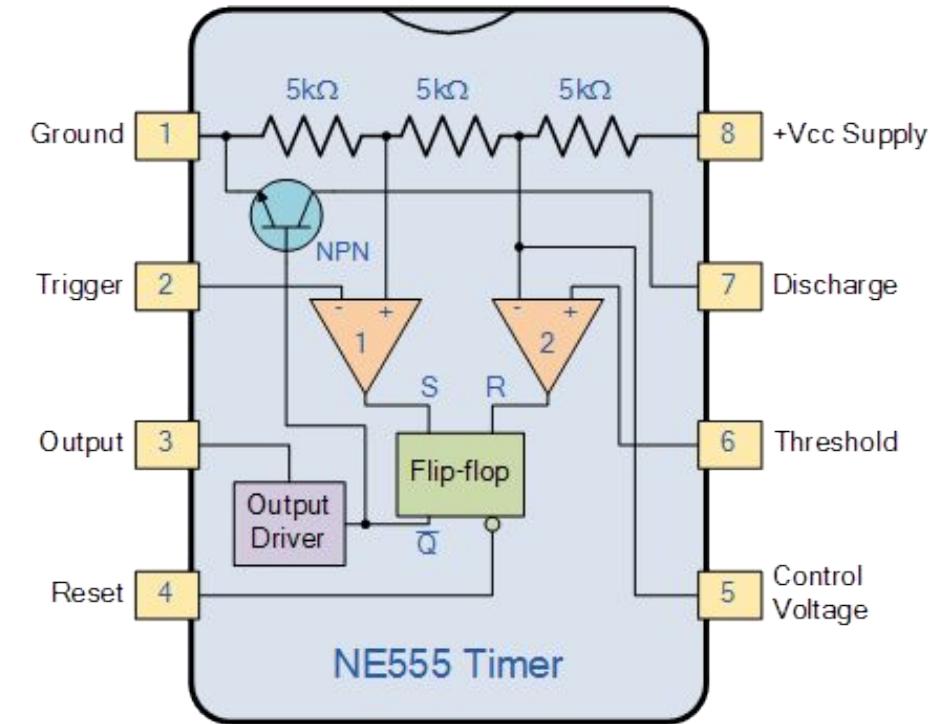
# Content

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- Comparator: inverting and non-inverting comparators
  - Applications: zero crossing detector, window detector
  - Sine wave generator
  - Schmitt trigger
  - square wave generator (Astable multivibrator)
  - Monostable Multivibrator
  - 555 timers: functional diagram and Monostable operation
-

# 555 Timer Basic Operation

- The **555 Timers** name comes from the fact that there are three  $5k\Omega$  resistors connected together internally producing a voltage divider network between the supply voltage at pin 8 and ground at pin 1.
- The voltage across this series resistive network holds the inverting input of comparator 2 at  $2/3V_{cc}$  and the non-inverting input to comparator 1 at  $1/3V_{cc}$ .
- The two comparators produce an output voltage dependent upon the voltage difference at their inputs which is determined by the charging and discharging action of the externally connected RC network.
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- The output from the flip-flop is used to control a high current output switching stage to drive the connected load producing either a “HIGH” or “LOW” voltage level at the output pin.



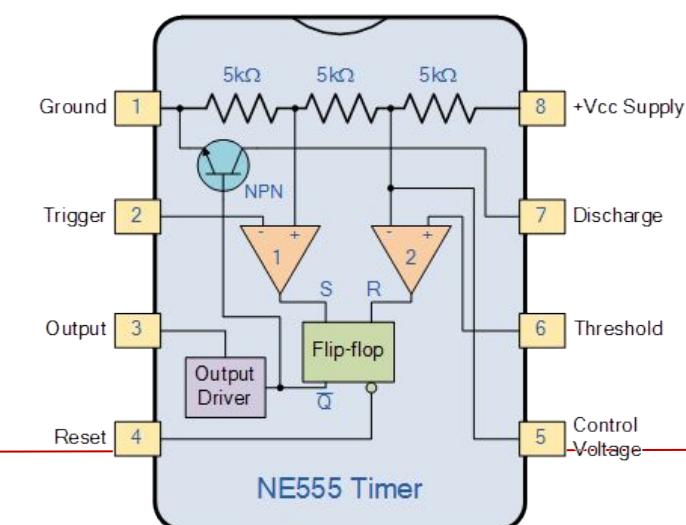
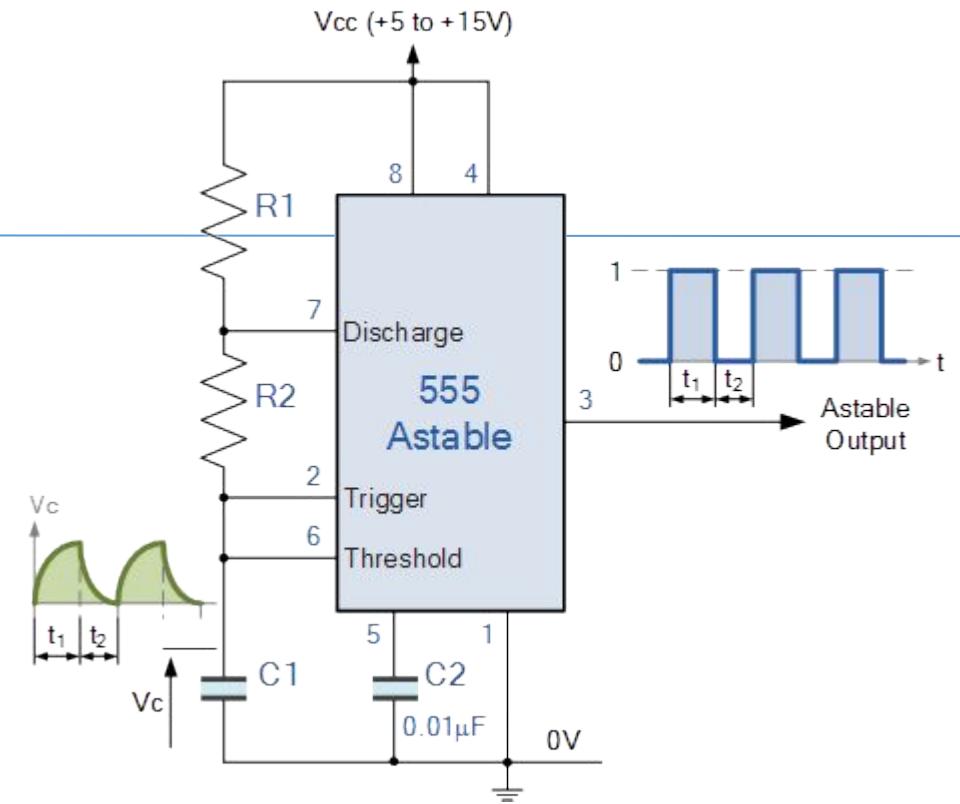
# 555 Timer: Astable Multivibrator

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- The **555 Timer IC** can be connected in its Monostable mode thereby producing a precision timer of a fixed time duration
- the 555 timer IC in an Astable mode to produce a very stable **555 Oscillator** circuit for generating highly accurate free running waveforms whose output frequency can be adjusted by means of an externally connected RC tank circuit consisting of just two resistors and a capacitor.
- It has no stable states as it continuously switches from one state to the other

# Operation

- In the **555 Oscillator** circuit, pin 2 and pin 6 are connected together allowing the circuit to re-trigger itself on each and every cycle allowing it to operate as a free running oscillator.
- During each cycle capacitor, C charges up through both timing resistors, R1 and R2 but discharges itself only through resistor, R2 as the other side of R2 is connected to the *discharge* terminal, pin 7.
- Then the capacitor charges up to  $2/3V_{cc}$  (the upper comparator limit) which is determined by the  $(R_1+R_2)$  combination and discharges itself down to  $1/3V_{cc}$  (the lower comparator limit) determined by the R2.
- This results in an output waveform whose output “ON” and “OFF” time periods are determined by the capacitor and resistors combinations.



# Time period

- Charging time ( $t_1$ ) and discharge time ( $t_2$ ):

$$t_1 = 0.693(R_1 + R_2) \cdot C$$

and

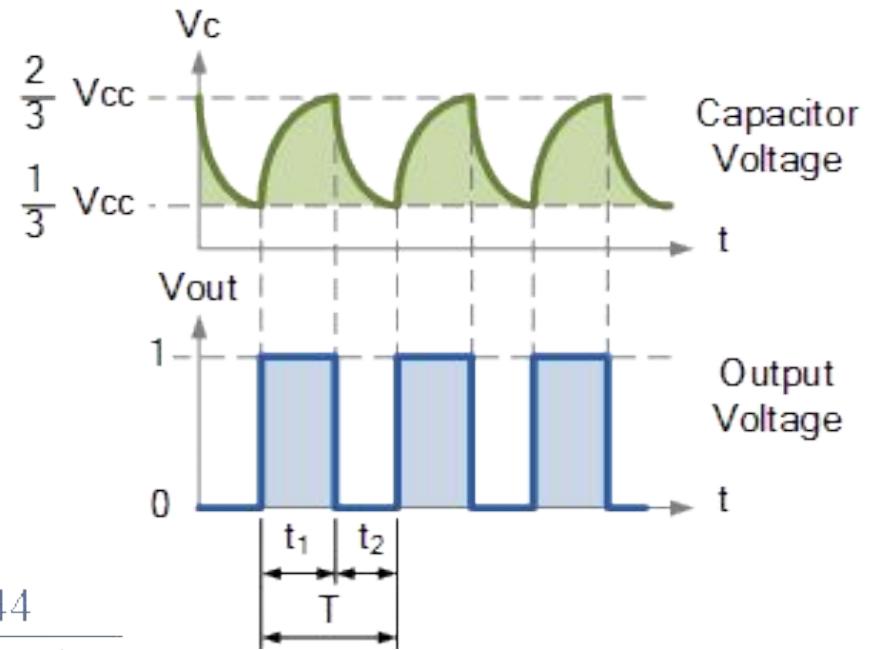
$$t_2 = 0.693 \times R_2 \times C$$

- Total time period and frequency:

$$T = t_1 + t_2 = 0.693(R_1 + 2R_2) \cdot C \quad f = \frac{1}{T} = \frac{1.44}{(R_1 + 2R_2) \cdot C}$$

- Duty cycle:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{OFF} + T_{ON}} = \frac{R_1 + R_2}{(R_1 + 2R_2)} \%$$



# Example:

- An **Astable 555 Oscillator** is constructed using the following components,  $R_1 = 1\text{k}\Omega$ ,  $R_2 = 2\text{k}\Omega$  and capacitor  $C = 10\text{uF}$ . Calculate the output frequency from the 555 oscillator and the duty cycle of the output waveform.

$t_1$  – capacitor charge “ON” time is calculated as:

$$\begin{aligned}t_1 &= 0.693(R_1 + R_2).C \\&= 0.693(1000 + 2000) \times 10 \times 10^{-6} \\&= 0.021\text{s} = 21\text{ms}\end{aligned}$$

$t_2$  – capacitor discharge “OFF” time is calculated as:

$$\begin{aligned}t_2 &= 0.693 R_2.C \\&= 0.693 \times 2000 \times 10 \times 10^{-6} \\&= 0.014\text{s} = 14\text{ms}\end{aligned}$$

$$T = t_1 + t_2 = 21\text{ms} + 14\text{ms} = 35\text{ms}$$

$$f = \frac{1}{T} = \frac{1}{35\text{ms}} = 28.6\text{Hz}$$

Giving a duty cycle value of:

$$\text{Duty Cycle} = \frac{R_1 + R_2}{(R_1 + 2R_2)} = \frac{1000 + 2000}{(1000 + 2 \times 2000)} = 0.6 \text{ or } 60\%$$

As the timing capacitor, C charges through resistors R1 and R2 but only discharges through resistor R2 the output duty cycle can be varied between 50 and 100% by changing the value of resistor R2. By decreasing the value of R2 the duty cycle increases towards 100% and by increasing R2 the duty cycle reduces towards 50%.



# Analog to Digital and Digital to Analog Converters

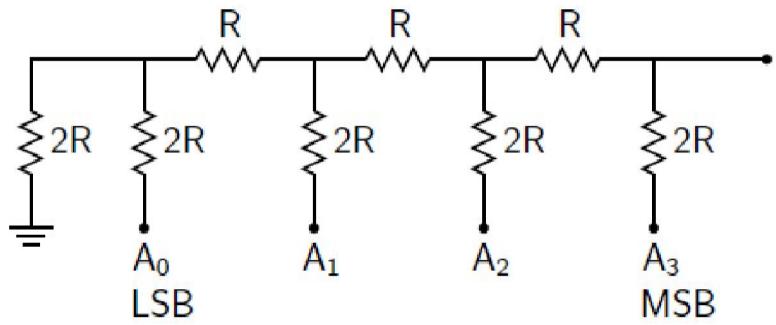
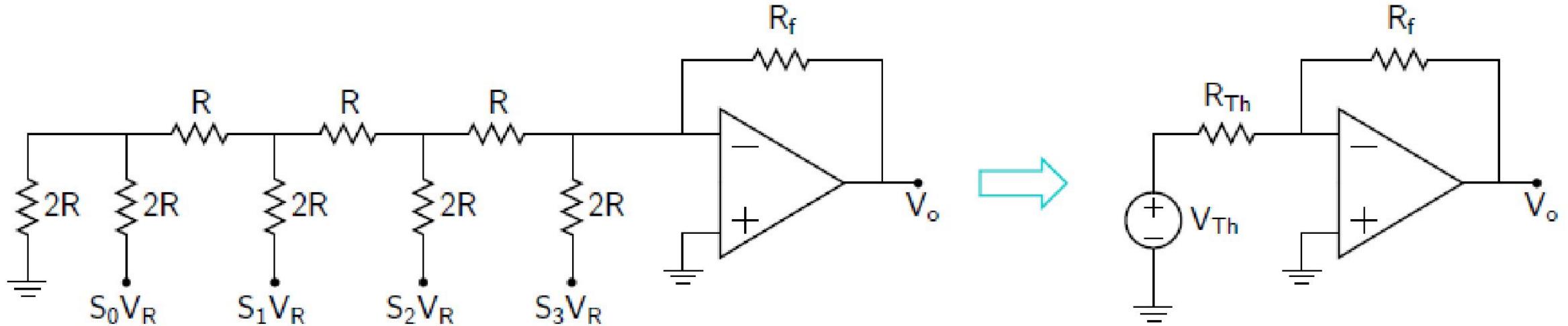
Dr. Kandimalla Divyabramham  
Assistant Professor  
IIIT Sri City

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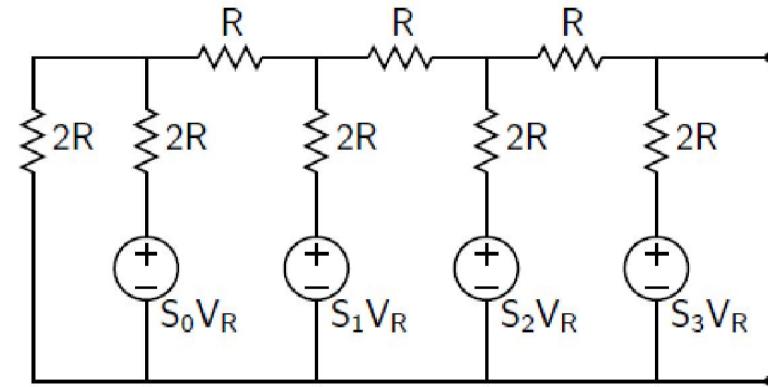
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# DAC with R-2R Ladder



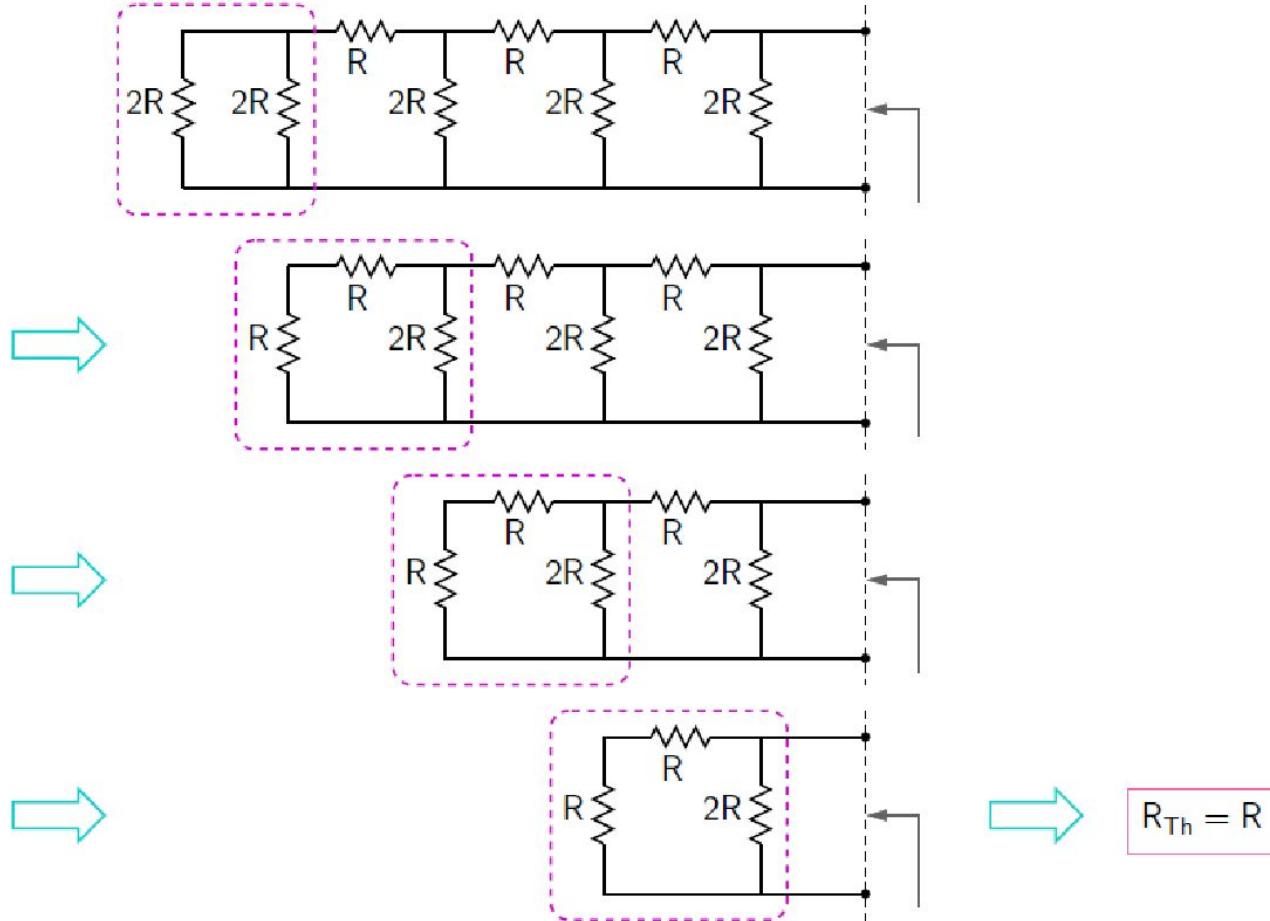
Node  $A_k$  is connected to  $V_R$  if input bit  $S_k$  is 1; else, it is connected to ground.

The original network is equivalent to

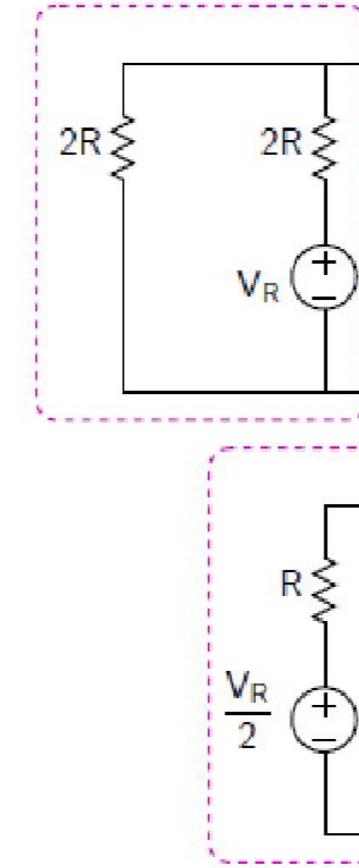
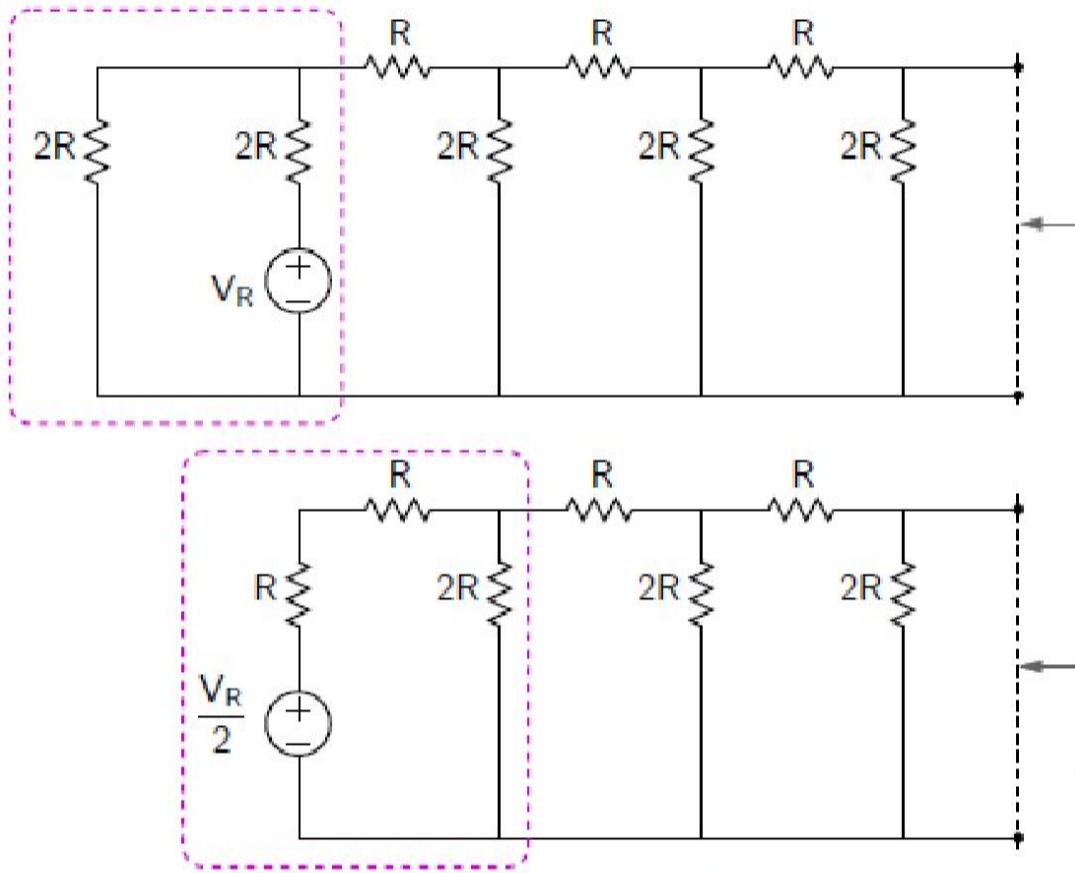




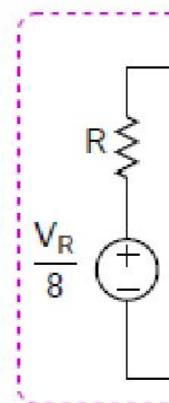
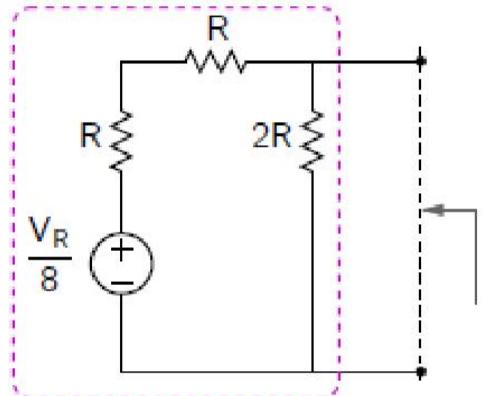
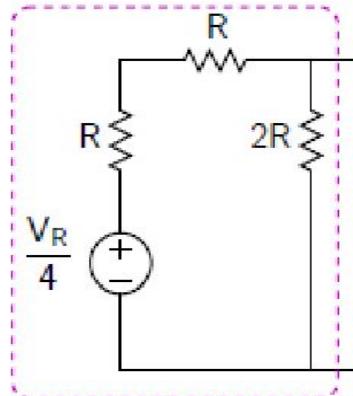
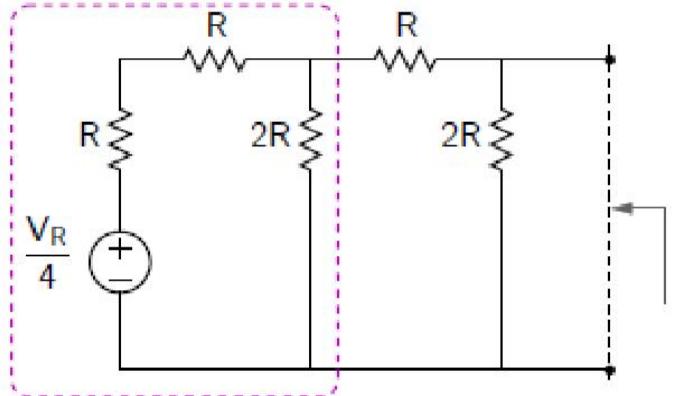
# R-2R Ladder Network: Equivalent resistance



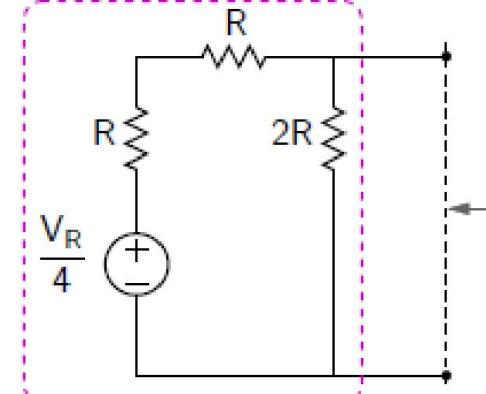
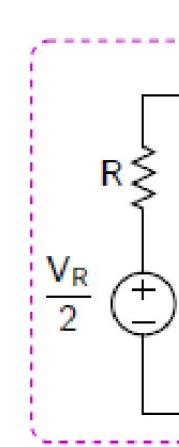
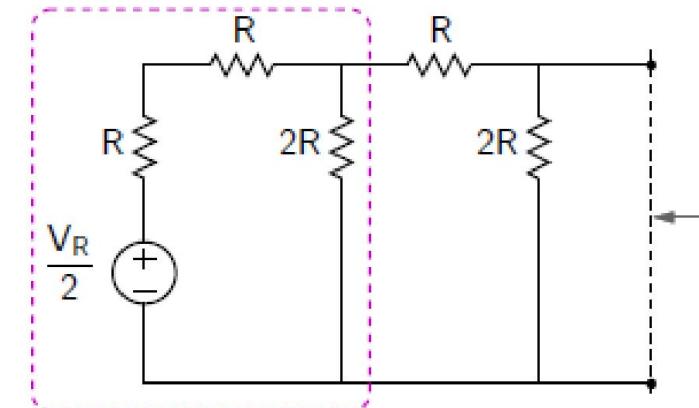
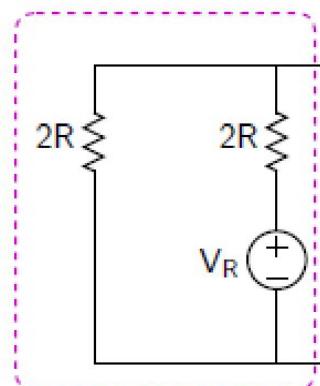
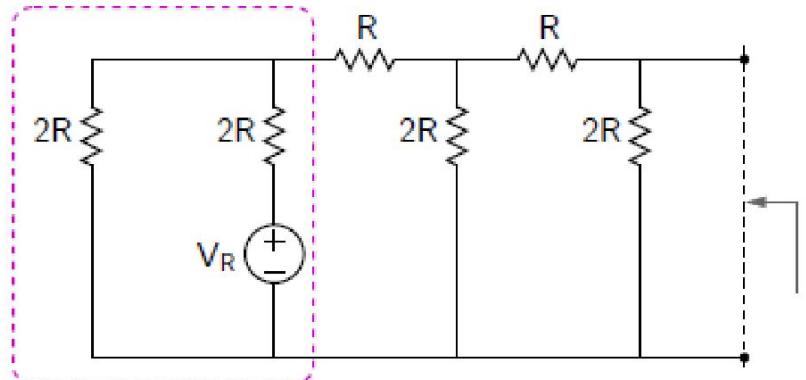
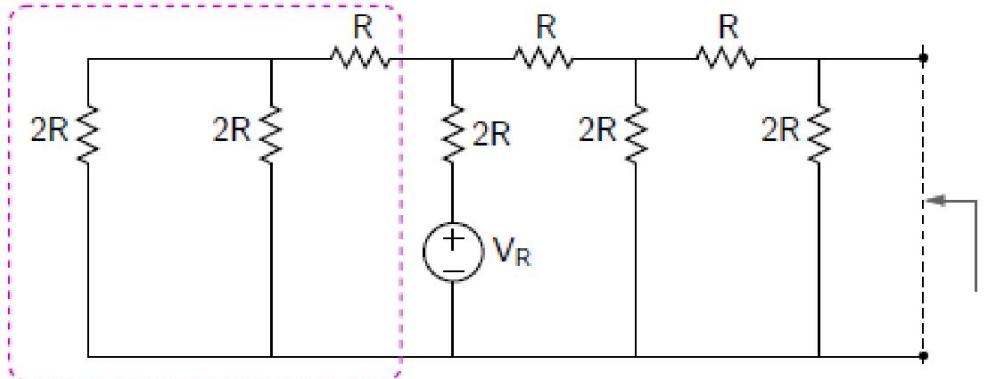
# R-2R ladder network: $V_{Th}$ for $S_0 = 1$



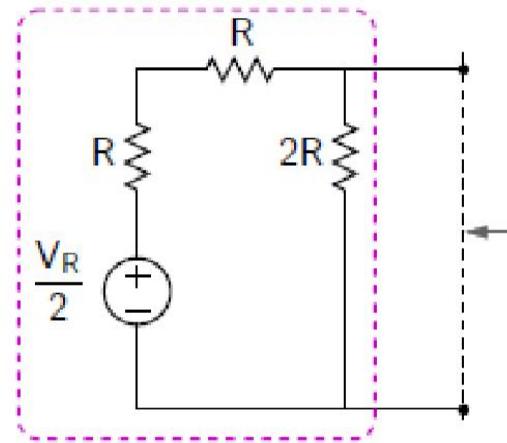
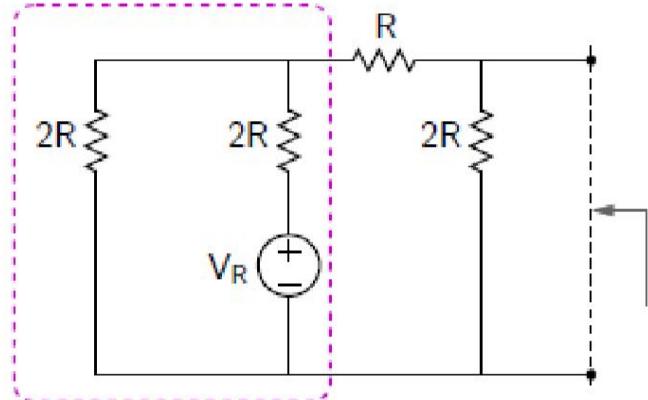
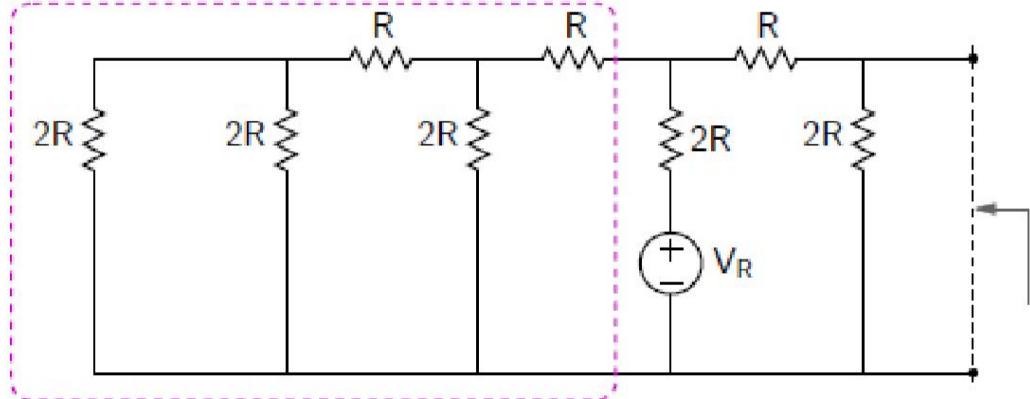
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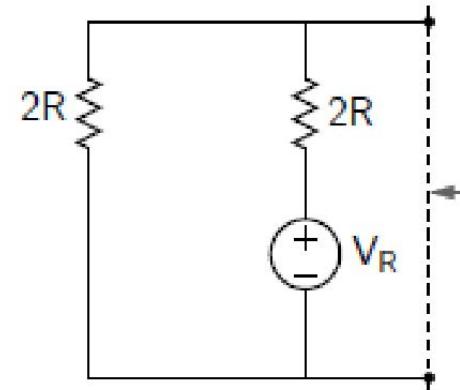
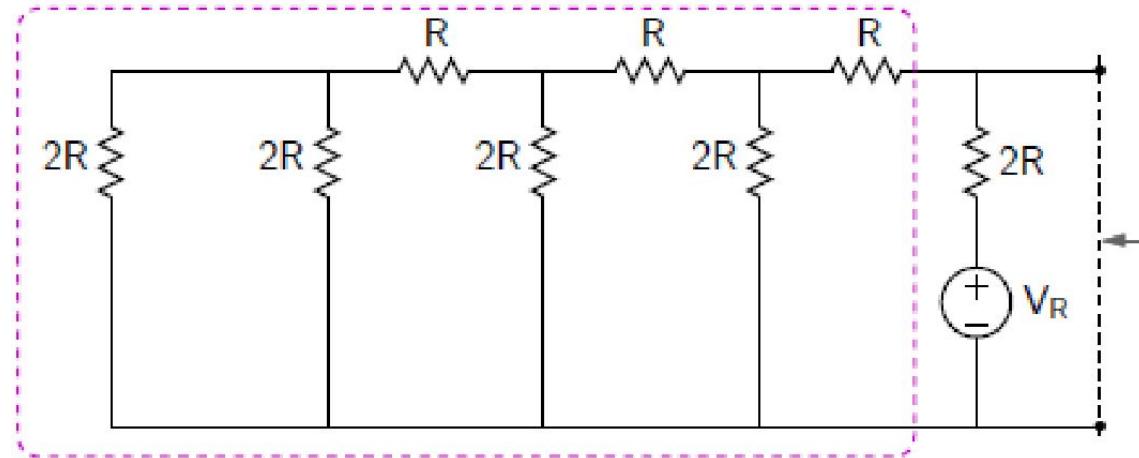
# R-2R ladder network: $V_{Th}$ for $S_1 = 1$

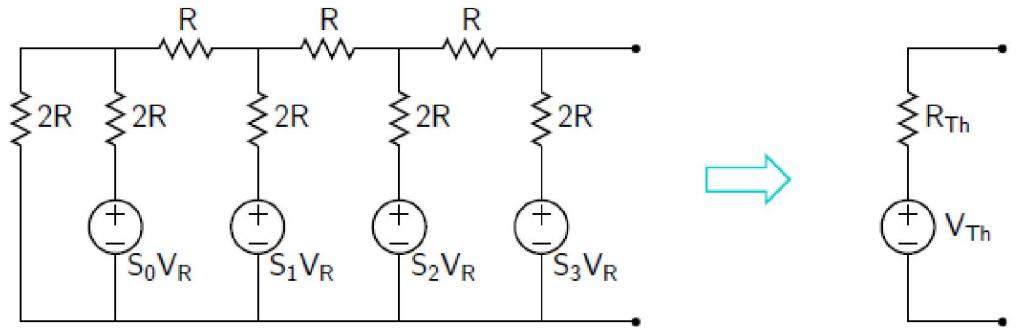


# R-2R ladder network: $V_{Th}$ for $S_2 = 1$



# R-2R ladder network: $V_{Th}$ for $S_3 = 1$

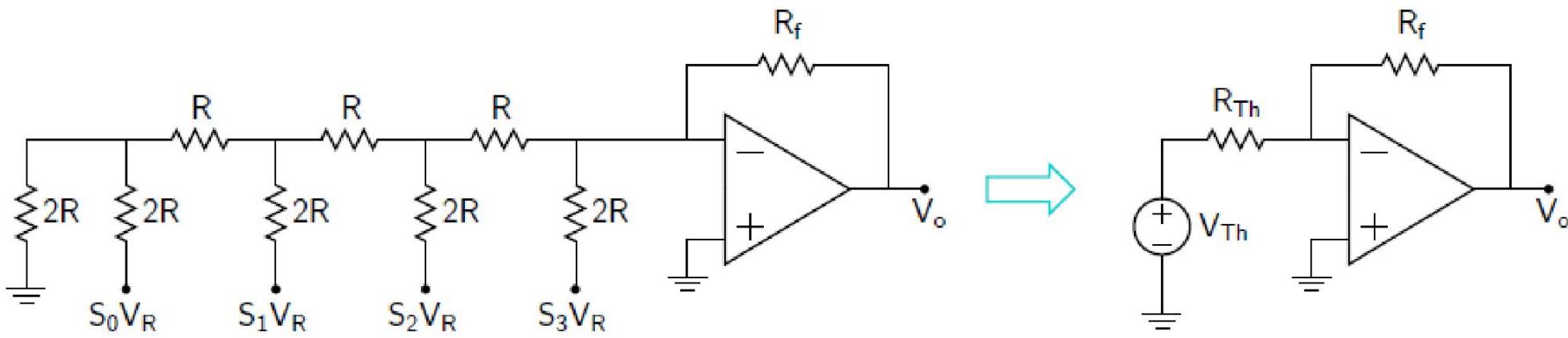




$$R_{Th} = R.$$

$$V_{Th} = V_{Th}^{(S0)} + V_{Th}^{(S1)} + V_{Th}^{(S2)} + V_{Th}^{(S3)} \\ = \frac{V_R}{16} [S_0 2^0 + S_1 2^1 + S_2 2^2 + S_3 2^3].$$

We can use the  $R-2R$  ladder network and an Op Amp



$$V_o = -\frac{R_f}{R_{Th}} V_{Th} = -\frac{R_f}{R_{Th}} \frac{V_R}{16} [S_0 2^0 + S_1 2^1 + S_2 2^2 + S_3 2^3].$$

$$\text{For an } N\text{-bit DAC, } V_o = -\frac{R_f}{R_{Th}} V_{Th} = -\frac{R_f}{R_{Th}} \frac{V_R}{2^N} \sum_0^{N-1} S_k 2^k.$$

6- to 20-bit DACs based on the  $R-2R$  ladder network are commercially available in monolithic form (single chip).

# R-2R Ladder

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- Design a 3 bit R-2R ladder DAC, and determine  $V_o$  for the following input sequences, (a) 010 (b) 011 (c) 100, and (d) 101.

For an N-bit DAC,  $V_o = -\frac{R_f}{R_{Th}} V_{Th} = -\frac{R_f}{R_{Th}} \frac{V_R}{2^N} \sum_0^{N-1} s_k 2^k$ .



# Analog to Digital and Digital to Analog Converters

Dr. Kandimalla Divyabramham  
Assistant Professor  
IIIT Sri City

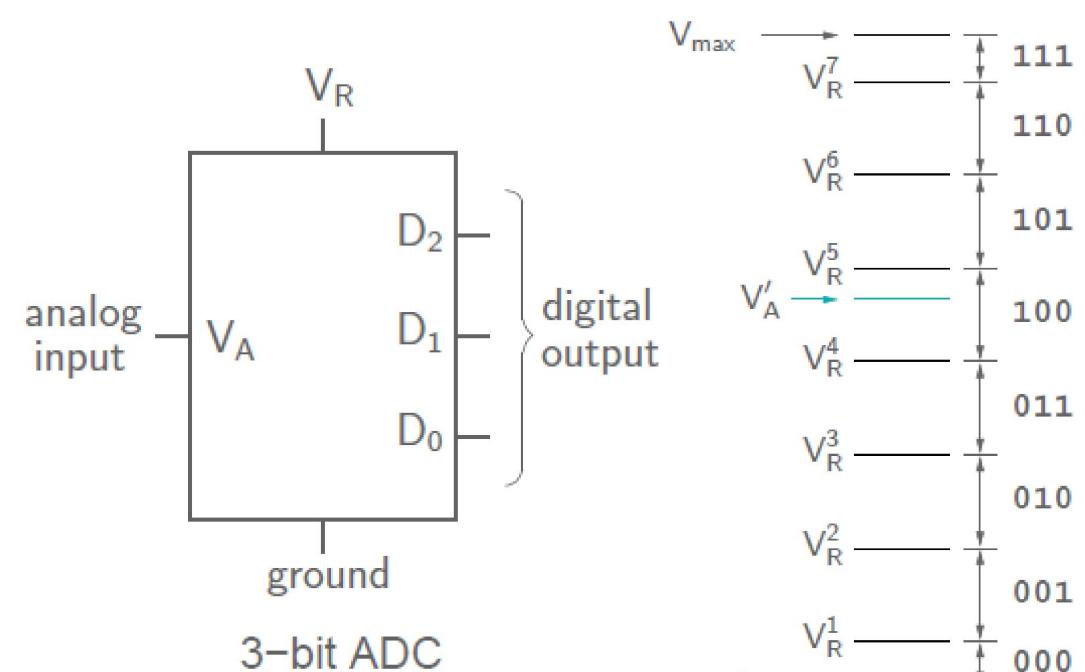
# Contents

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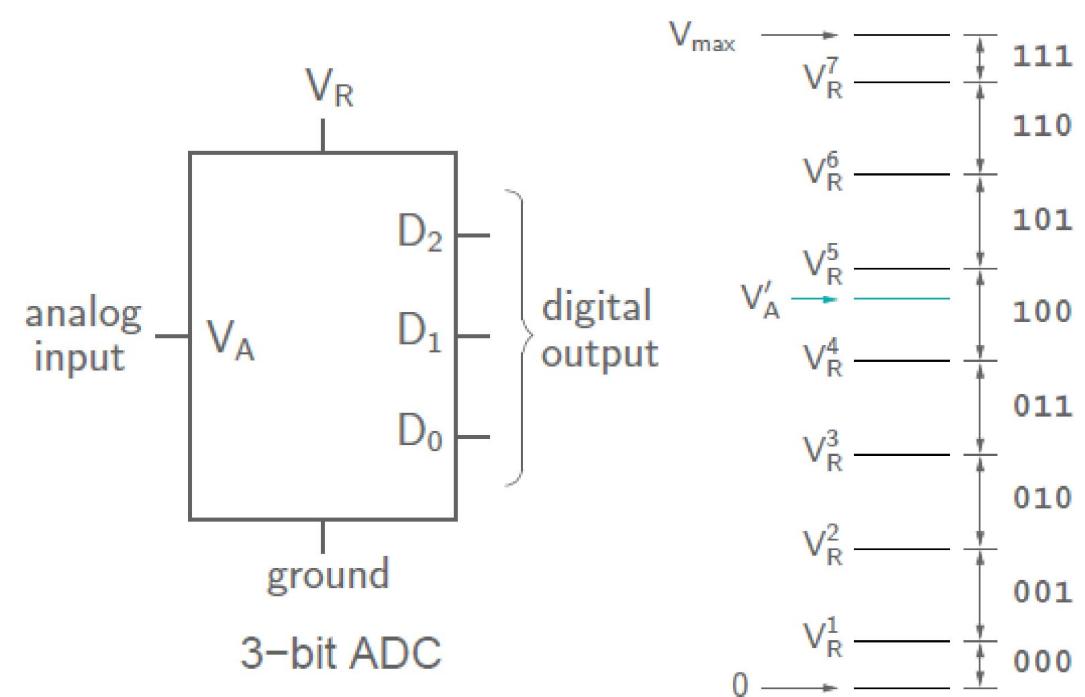
# ADC: Introduction

- If the input  $V_A$  is in the range  $V_R^k < V_A < V_R^{k+1}$ , the output is the binary number corresponding to the integer  $k$ .
- For example, for  $V_A = V'_A$ , the output is 100.
- We may think of each voltage interval (corresponding to 000, 001, etc.) as a “bin”.
- The input voltage  $V'_A$  falls in the 100 bin; therefore, the output of the ADC would be 100.
- Note that, for an  $N$ -bit ADC, there would be  $2^N$  bins.



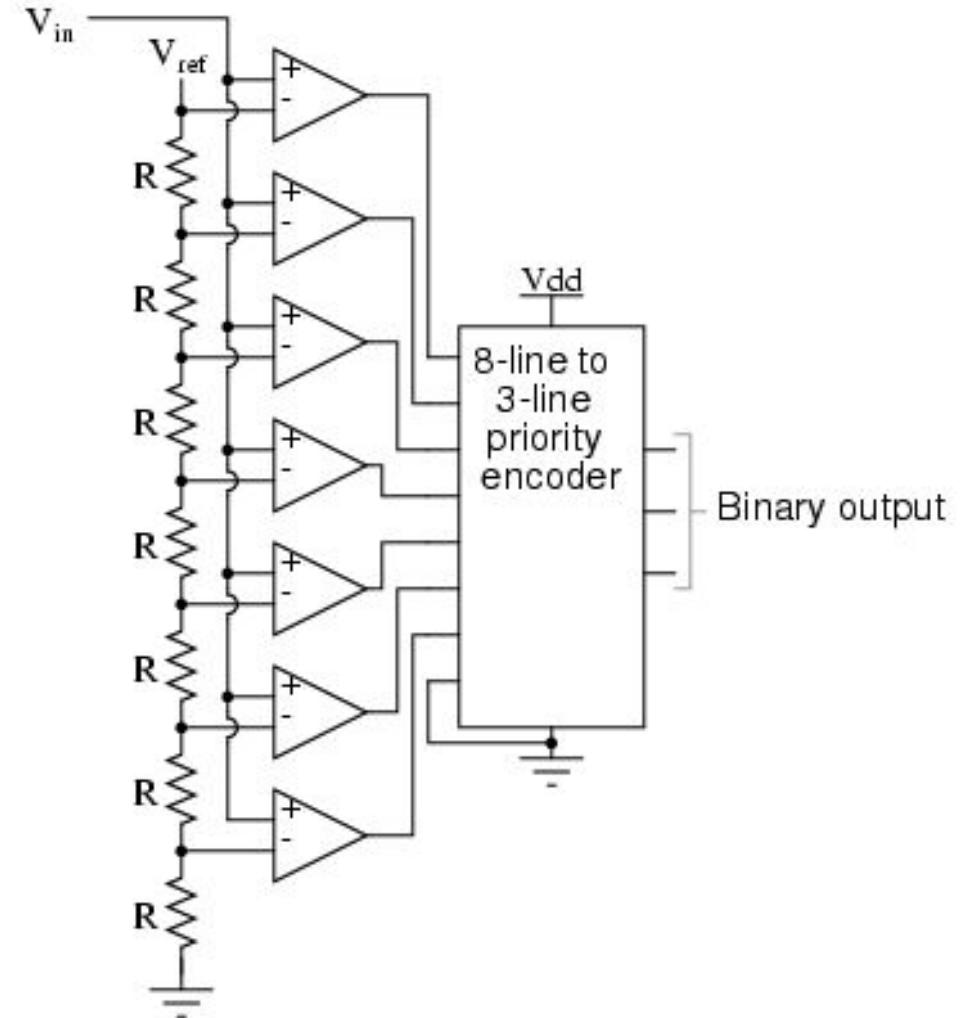
# ADC: Introduction

- The basic idea behind an ADC is simple:
  - Generate reference voltages  $V_R^1, V_R^2, \dots$ , etc.
  - Compare the input  $V_A$  with each of  $V_R^i$  to figure out which bin it belongs to.
  - If  $V_A$  belongs to bin  $k$  (i.e.,  $V_R^k < V_A < V_R^{k+1}$ ), convert  $k$  to the binary format.
- A “parallel” ADC does exactly that.



# The Parallel (Flash) Comparator

- It is formed of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which then produces a binary output
- $V_{ref}$  is a stable reference voltage
- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.



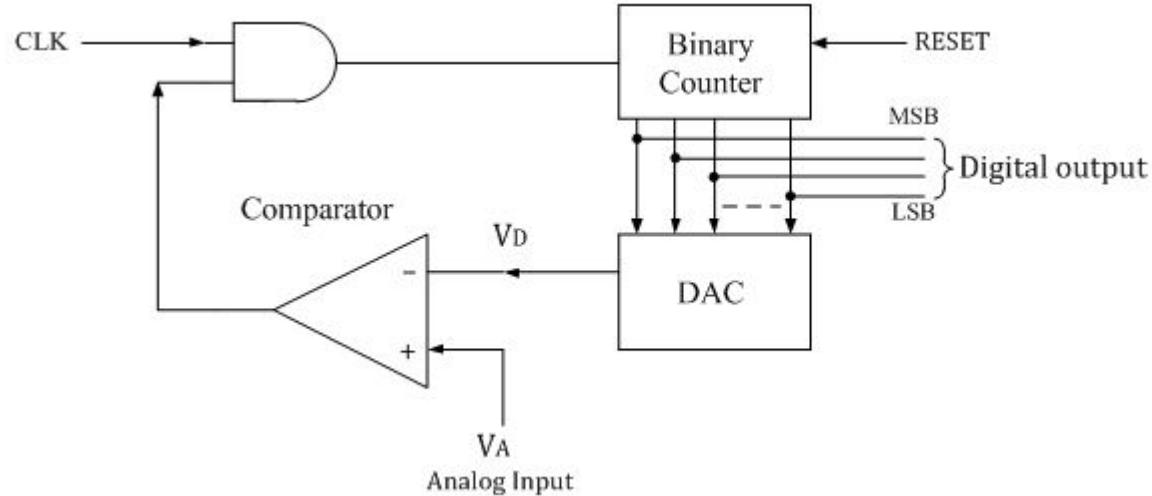
# The Parallel Comparator

---

- It is the fastest and most expensive technique.
- it is the most component-intensive for any given number of output bits. This three-bit flash ADC requires seven comparators.
- A four-bit version would require 15 comparators. With each additional output bit, the number of required comparators doubles.
- N-bit version require  $2^N - 1$  comparators

# Counter Type ADC

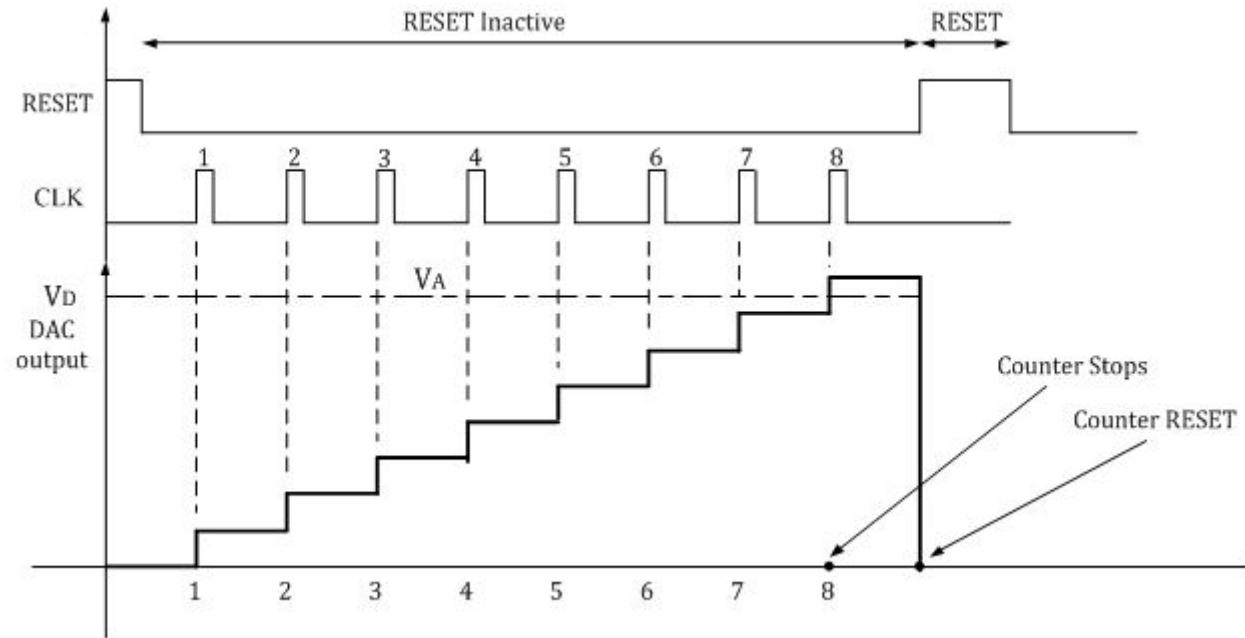
The counter type ADC is constructed using a binary counter, DAC and a comparator. The output voltage of a DAC is  $V_D$  which is equivalent to corresponding digital input to DAC.



The n-bit binary counter is initially set to 0 by using reset command. Therefore the digital output is zero and the equivalent voltage  $V_D$  is also 0V.

When the reset command is removed, the clock pulses are allowed to go through AND gate and are counted by the binary counter.

The D to A converter (DAC) converts the digital output to an analog voltage and applied as the inverting input to the comparator. The output of the comparator enables the AND gate to pass the clock.



**Advantages:**

- 1 Simple construction.
- 2 Easy to design and less expensive.
- 3 Speed can be adjusted by adjusting the clock frequency.

The number of clock pulses increases with time and the analog input voltage  $V_D$  is a rising staircase waveform as shown in figure.

The counting will continue until the DAC output  $V_D$ , equals and just rises more than unknown analog input voltage  $V_A$ . Then the comparator output becomes low and this disables the AND gate from passing the clock.

The counting stops at the instance  $V_A < V_D$ , and at that instant the counter stops its progress and the conversion is said to be complete.

The numbers stored in the n-bit counter is the equivalent n-bit digital data for the given analog input voltage.

# Successive Approximation type ADC

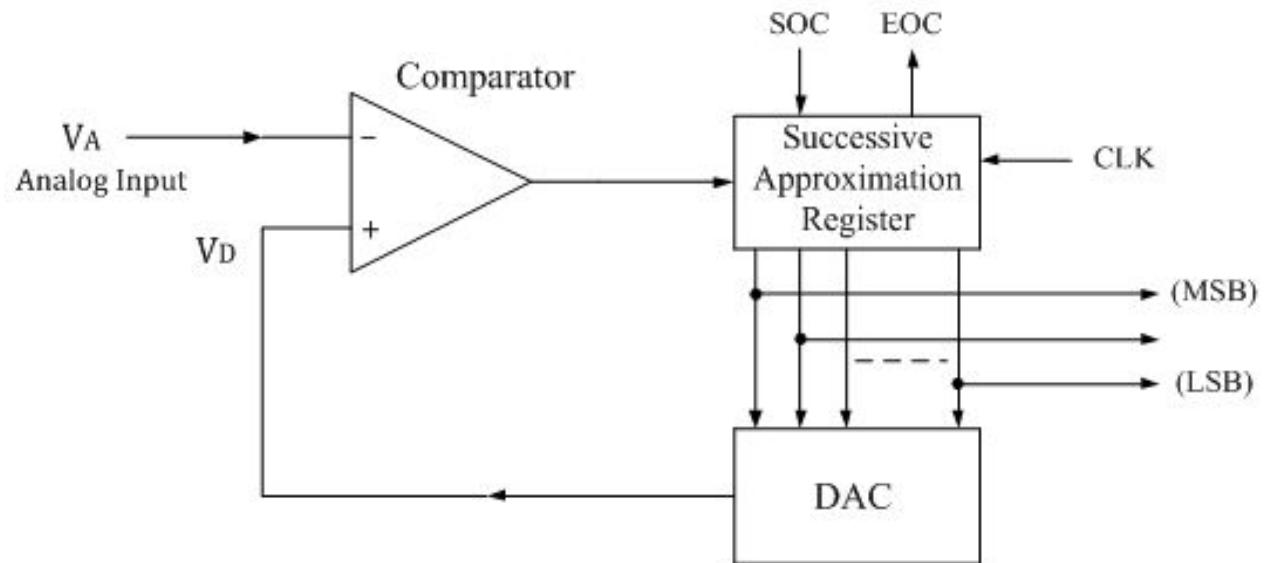
Successive Approximation type ADC is the most widely used and popular ADC method.

The conversion time is maintained constant in successive approximation type ADC, and is proportional to the number of bits in the digital output, unlike the counter type A/D converters.

It consists of a successive approximation register (SAR), DAC and comparator. The output of SAR is given to n-bit DAC.

The equivalent analog output voltage of DAC,  $V_D$  is applied to the non-inverting input of the comparator.

The second input to the comparator is the unknown analog input voltage  $V_A$ . The output of the comparator is used to activate the successive approximation logic of SAR. When the start command is applied, the SAR sets the MSB to logic 1 and other bits are made logic 0, so that the trial code becomes 1000.



The basic principle of this type of A/D converter is that the unknown analog input voltage is approximated against an n-bit digital value by trying one bit at a time, beginning with the MSB.

This type of ADC operates by successively dividing the voltage range by half, as explained in the following steps.

- (1) The MSB is initially set to 1 with the remaining three bits set as 000. The digital equivalent voltage is compared with the unknown analog input voltage.
- (2) If the analog input voltage is higher than the digital equivalent voltage, the MSB is retained as 1 and the second MSB is set to 1. Otherwise, the MSB is set to 0 and the second MSB is set to 1. Comparison is made as given in step (1) to decide whether to retain or reset the second MSB.

The above steps are more accurately illustrated with the help of an example.

Let us assume that the 4-bit ADC is used and the analog input voltage is  $V_A = 11$  V.

when the conversion starts, the MSB bit is set to 1.

Now  $V_A = 11V > V_D = 8V = [1000]_2$

Since the unknown analog input voltage  $V_A$  is higher than the equivalent digital voltage  $V_D$ , as discussed in step (2), the MSB is retained as 1 and the next MSB bit is set to 1 as follows

$V_D = 12V = [1100]_2$

Now  $V_A = 11V < V_D = 12V = [1100]_2$

Here now, the unknown analog input voltage  $V_A$  is lower than the equivalent digital voltage  $V_D$ . As discussed in step (2), the second MSB is set to 0 and next MSB set to 1 as

$V_D = 10V = [1010]_2$

Now again  $V_A = 11V > V_D = 10V = [1010]_2$

Again as discussed in step (2)  $V_A > V_D$ , hence the third MSB is retained to 1 and the last bit is set to 1. The new code word is

$V_D = 11V = [1011]_2$

Now finally  $V_A = V_D$ , and the conversion stops.

# Successive Approximation type ADC

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- **Advantages:**

- Conversion time is very small.

- Conversion time is constant and independent of the amplitude of the analog input signal VA.

- **Disadvantages:**

- Circuit is complex.



**Indian Institute of Information Technology, Sri City, Chittoor**  
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# BEC Tutorial

# DAC

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- In a 8-bit DAC, if 0000 0000 represents 0 V, what is the output voltage produced if the input is 1011 1011? If  $K = 10/2^8$  mV .

For a 4-bit DAC, with input  $S_3 S_2 S_1 S_0$ , the output voltage is  
 $V_A = K [(S_3 \times 2^3) + (S_2 \times 2^2) + (S_1 \times 2^1) + (S_0 \times 2^0)]$ .  
In general,  $V_A = K \sum_0^{N-1} S_k 2^k$ .

# Weighted resistor

---

- Consider an 8-bit DAC with  $V_R = 10 \text{ V}$ . What is the smallest value of  $R$  which will limit the current drawn from the supply ( $V_R$ ) to 2 mA?
- What is the maximum output voltage (in magnitude),  $R_F = R$ ?
- Find the output voltage corresponding to the input 1001 0010

# R-2R Ladder

---

- Design a 4 bit R-2R ladder DAC, and determine  $V_o$  for the following input sequences for  $RF = 2R$  and  $V_{ref} = 10 V$ , (a) 0100 (b) 0110 (c) 1001, and (d) 0101.

For an N-bit DAC,  $V_o = -\frac{R_f}{R_{Th}} V_{Th} = -\frac{R_f}{R_{Th}} \frac{V_R}{2^N} \sum_0^{N-1} s_k 2^k$ .



- An **op-amp multivibrator circuit** is constructed using the following components.  $R_1 = 65\text{k}\Omega$ ,  $R_2 = 35\text{k}\Omega$ ,  $R = 5\text{k}\Omega$  and  $C = 0.001\mu\text{F}$ . Calculate the circuits frequency of oscillation.

- An **op-amp monostable circuit** is constructed using the following components.  $R_1 = 45\text{k}\Omega$ ,  $R_2 = 15\text{k}\Omega$ ,  $R = 15\text{k}\Omega$  and  $C = 10.0\mu\text{F}$ . If the op-amp monostable is supplied from a  $\pm 15\text{V}$  supply and the timing period is initiated with a  $15\text{ms}$  pulse,  $V_D = 0.7 \text{ V}$ .
- Calculate the circuits timing period, capacitor recovery time, total time between trigger pulses.