Combinational Logic

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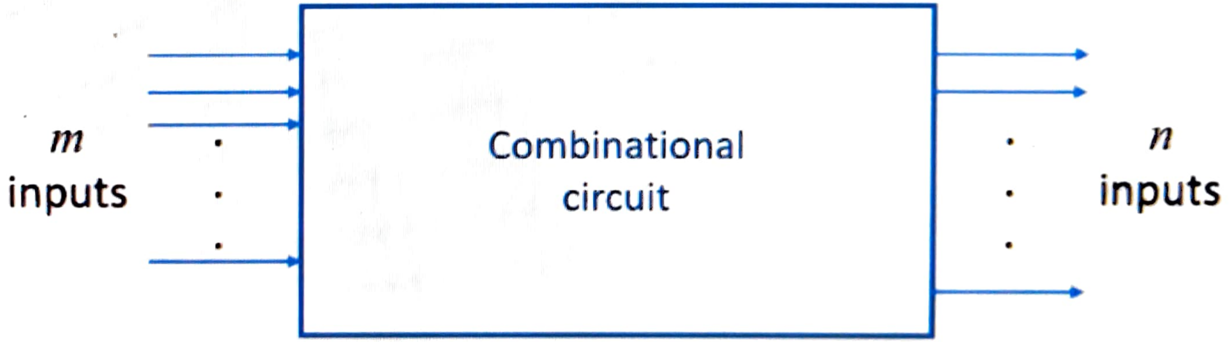
Logic Circuits

- Combinational circuit
  - Logic gate circuit, whose output at a particular time instant is dependent on input combination at that particular time instant
- Sequential circuit
  - Logic gate circuit + Storage element
  - Output depends on the input combination and the state of the memory element

Combinational Circuit

- Logic circuit that consists of interconnection of logic gates
- For m inputs, the possible combinations of binary inputs = 2^m
- For each possible input combination, there is one possible value at the output
- A combinational circuit can be described by truth table



Block diagram of combinational circuit

Combinational Circuits

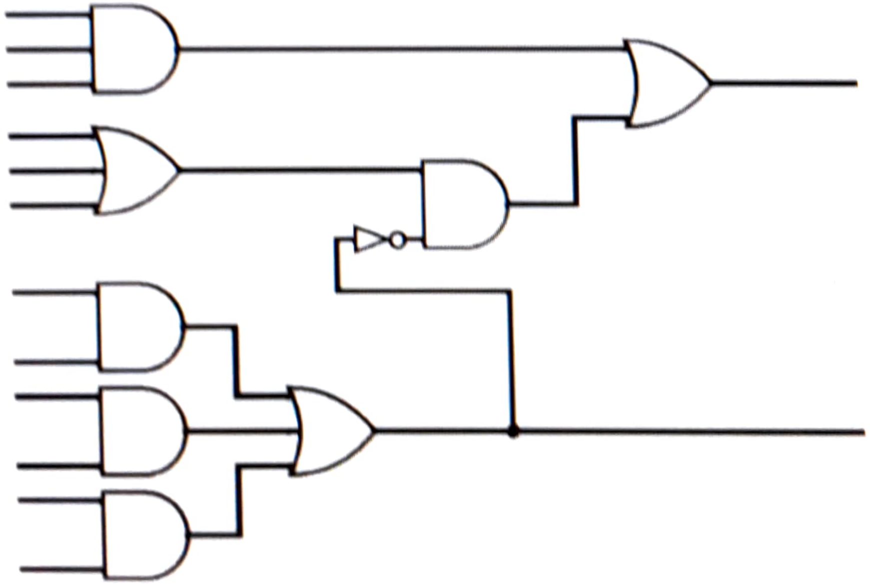
- Binary Adder, Subtractor
- Decimal Adder
- Binary multiplier
- Magnitude comparator
- Decoder
- Encoder
- Multiplexer

Analysis of Combinational Circuit

- Determine the function the circuit implements
- Start with
  - Logic circuit
  - Boolean functions
  - Truth table
  - Explanation of the circuit operation
- Make sure the circuit is not sequential
- Make sure there is no feedback path or memory elements

Procedure to obtain Boolean function from logic circuit

- Label all gate first stage outputs with unique names
- Proceed to the next stage, till you reach final output



Combinational Circuit

$P = ABC$

$Q = A + B + C$

$R = AB$

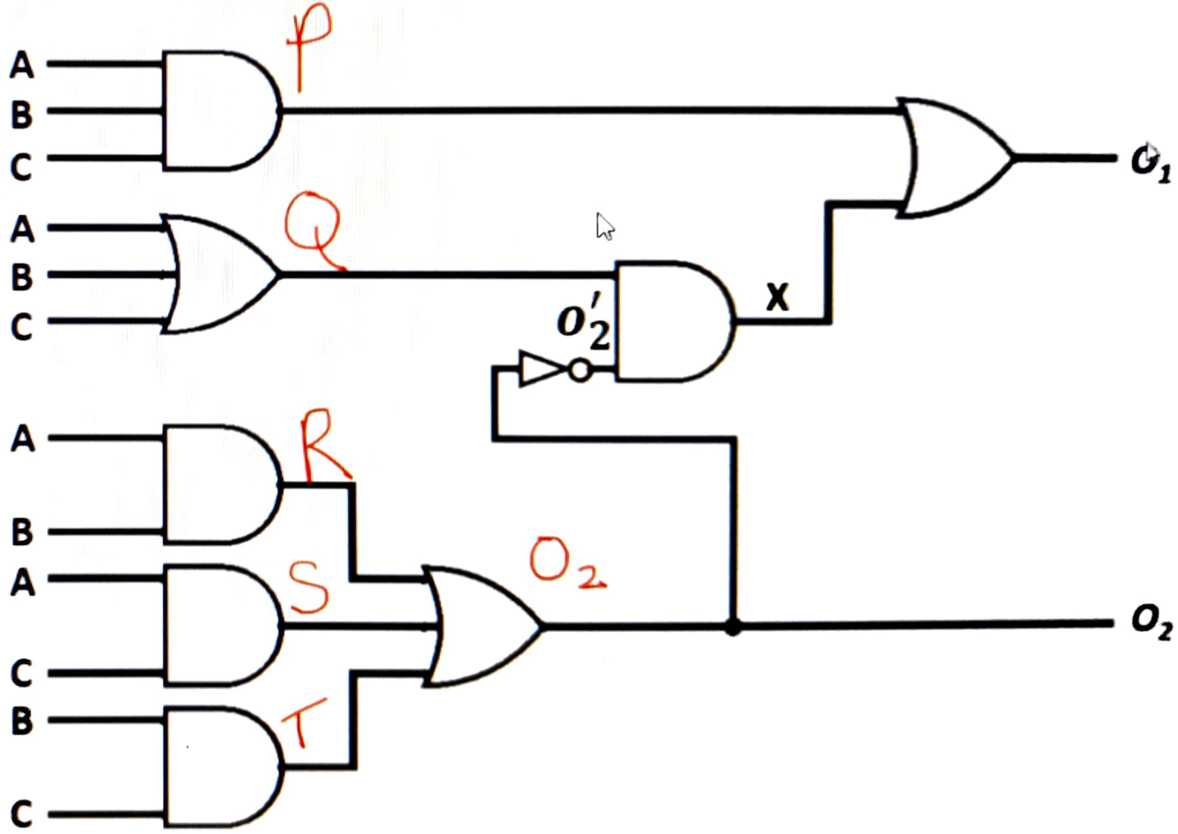
$S = AC$

$T = BC$

$O_2 = R + S + T$

$O_2 = AB + AC + BC$

$O_1 = P + X = (ABC) + (QO_2')$



Code conversion example combinational logic circuit

Decimal	Binary	Excess-3
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010
8	1000	1011
9	1001	1100

Input BCD				Output Excess-3			
A	B	C	D	P	Q	R	S
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

K-maps for the output variables

P

AB \ CD	00	01	11	10
00				
01				
11				
10				

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

Q

AB \ CD	00	01	11	10
00				
01				
11				
10				

R

AB \ CD	00	01	11	10
00				
01				
11				
10				

S

AB \ CD	00	01	11	10
00				
01				
11				
10				

Don’t care conditions

- The six bit combinations not listed beyond 1001 for input are don’t-care combinations
- These values have no meaning in BCD and we assume that they will never occur in actual operation of the circuit
- Therefore we have the liberty to take either 0 or 1
- Don’t care is represented by X
- Idea is to get simple circuit

Binary	Excess-3
0000	0011
0001	0100
0010	0101
0011	0110
0100	0111
0101	1000
0110	1001
0111	1010
1000	1011
1001	1100

Four-variable K-map

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

Simplify the Boolean function given in standard SOP form

F = A′B′C′ + B′CD′ + A′BCD′ + AB′C′

Add missing variables

F = A′B′C′ (D+D′)+(A+A′) B′CD′ + A′BCD′ + AB′C′(D+D′)

AB \ CD	00	01	11	10
00	1	1		1
01				1
11				
10	1	1		1

K-maps for the output variables

P

AB \ CD	00	01	11	10
00				
01		1	1	1
11	X	X	X	X
10	1	1	X	X

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

Q

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	X	X	X	X
10		1	X	X

R

AB \ CD	00	01	11	10
00	1		1	
01	1		1	
11	X	X	X	X
10	1		X	X

S

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1		X	X

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B D + B C + A

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K-maps for the output variables

P = A + BD + BC

AB \ CD	00	01	11	10
00				
01		1	1	1
11	X	X	X	X
10	1	1	X	X

m_0	m_1	m_3	m_2
m_4	m_5	m_7	m_6
m_{12}	m_{13}	m_{15}	m_{14}
m_8	m_9	m_{11}	m_{10}

Q

AB \ CD	00	01	11	10
00		1	1	1
01	1			
11	X	X	X	X
10		1	X	X

R

AB \ CD	00	01	11	10
00	1		1	
01	1		1	
11	X	X	X	X
10	1		X	X

S

AB \ CD	00	01	11	10
00	1			1
01	1			1
11	X	X	X	X
10	1		X	X

Full Adder

Input			Output	
A	B	C	Carry	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Two-bit multiplier

			A_1A_0	$\times\ B_1B_0$
		A_1B_0	A_0B_0	← Partial products
	A_1B_1	A_0B_1		
P_3	P_2	P_1	P_0	

$$P_0 = A_0B_0$$

$$P_1 = A_1B_0 + A_0B_1$$

$$P_2 = A_1B_1$$

$$P_3 = \mathit{Carry\ out\ \ from}\ P_2$$

2 bit × 2bit multiplier

Product

$P_3\ P_2\ P_1\ P_0$

A_1	A_0	B_1	B_0	P_3	P_2	P_1	P_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	0	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1

Magnitude comparator

- Comparison of two numbers to determine whether a number is
  - $>$
  - $<$
  - $=$

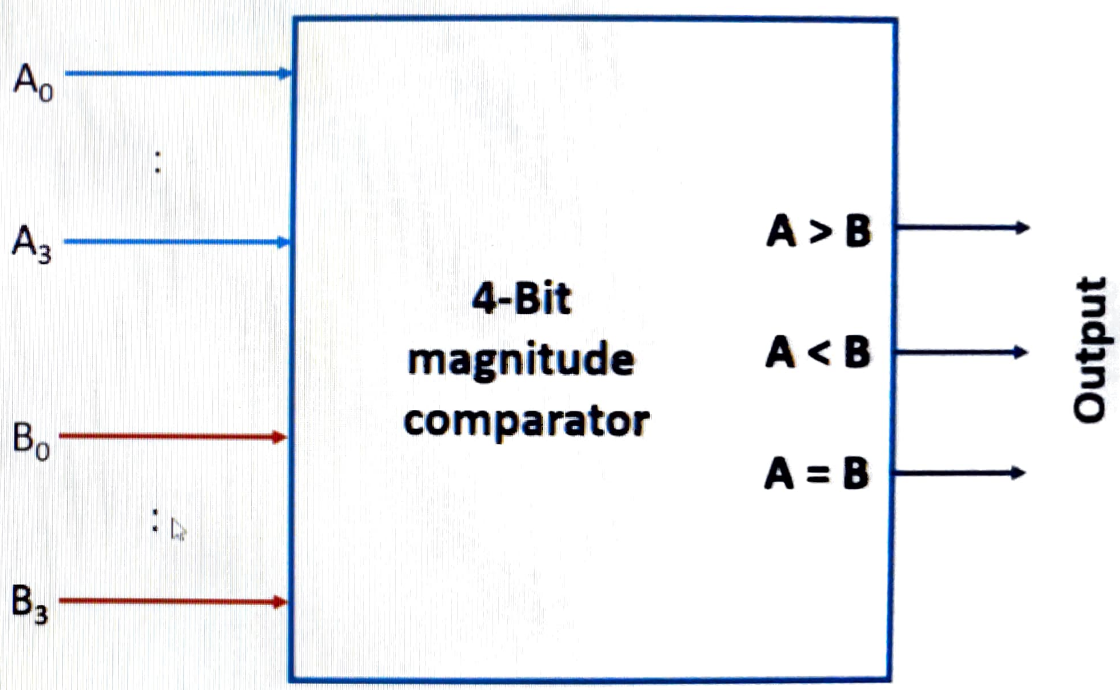
  the other number
- A magnitude comparator is a combinational circuit that compares two numbers A and B and results in a output to indicate

$$A > B$$

$$A < B$$

$$A = B$$

4-Bit Magnitude comparator



4-Bit Magnitude comparator

A3 & B3	A2 & B2	A1 & B1	A0 & B0	A > B	A < B	A = B
A3 > B3				1		0
A3 < B3					1	0
A3 = B3	A2 > B2			1		0
A3 = B3	A2 < B2				1	0
A3 = B3	A2 = B2	A1 > B1		1		0
A3 = B3	A2 = B2	A1 < B1			1	0
A3 = B3	A2 = B2	A1 = B1	A0 > B0	1		0
A3 = B3	A2 = B2	A1 = B1	A0 < B0		1	0
A3 = B3	A2 = B2	A1 = B1	A0 = B0			1

Decoder

- A combinational circuit that converts binary information from *n* input lines to a maximum of 2^n unique output lines

Inputs			Outputs							
x	y	z	D_0	D_0	D_0	D_0	D_0	D_0	D_0	D_0