LOP Submission

END-SEMESTER REPORT

SUCCESSIVE APPROXIMATION REGISTER ADC

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1. ABSTRACT:

This report documents the design, implementation, and evaluation of a successive approximation ADC architecture widely used due to some inherent advantages such as low power, high resolution, and moderate speed among other architectures of ADC. The SAR ADC uses a binary search algorithm to mimic the input analog signal by successively issuing digital outputs. SAR ADC functional blocks are the capacitive DAC for precise voltage level generation, the dynamic comparator for high-speed decision-making, and the final digital SAR logic circuit to manage the binary search algorithm.

However, the capacitive DAC structure employs a charge redistribution technique with binary weighted capacitors and dummy capacitors to generate precise voltage conversion. Therefore, a differential configuration with two such arrays gives better performance due to better linearity as well as reduced noise. Decision tradeoffs which include the actual incorporation of larger unit capacitors to cancel thermal noise as compared to speed limitations are critiqued. Furthermore, the proposed implementation of a common-mode switch with the DAC offers considerably improved connections to the reference voltage during the sampling phase minimizing delay and system stability issues.

The SAR logic block is developed using a synchronous solution with the sequencer register and code register; therefore, they provide efficient digital control. The sequencer register employs one hot encoding to control the binary search iterations based on the control logic even improving on the timing. Another addition to the architecture is a bootstrapped switch design that helps to improve the sampling accurate by guaranteeing that MOSFET switches are properly functional irrespective of the fluctuating input.

Simulation results validate the functionality and performance of the SAR ADC, demonstrating its ability to achieve high-resolution analog-to-digital conversion while maintaining low power consumption and compact design. This report emphasizes the design considerations, architectural optimizations, and trade-offs encountered in the development of the SAR ADC, making it suitable for applications such as sensor interfacing, medical instrumentation, and portable electronic devices.

2. INTRODUCTION:

The Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) has become a popular choice in modern electronic systems, particularly in applications requiring low power consumption, medium resolution, and moderate conversion speed. By employing a binary search algorithm to approximate the input signal iteratively, SAR ADCs achieve high energy efficiency without the need for power-intensive analog components such as operational amplifiers or large arrays of comparators. This architectural simplicity allows the power consumption of SAR ADCs to scale effectively with advancements in technology, making them ideal for systems like computing-in-memory cores used in artificial intelligence, and biomedical signal processing units.

SAR ADCs typically operate by sampling an analog input signal, holding it, and performing successive comparisons to output a digital code representing the input voltage. The process involves three main stages: sample-and-hold, iterative comparisons controlled by SAR logic, and digital code generation. The binary search algorithm ensures that the number of comparisons corresponds to the resolution (N-bit), balancing accuracy and speed. While SAR ADCs generally have lower sample rates compared to pipeline and flash ADCs, their power efficiency and simplicity make them suitable for applications operating at sampling frequencies in the kilohertz to megahertz range.

Two main control schemes are used in SAR ADCs: synchronous and asynchronous architectures. Synchronous SAR ADCs rely on an external clock and require at least N cycles per conversion, while asynchronous SAR ADCs utilize internally generated clock signals, reducing dynamic power consumption and logic complexity. This asynchronous operation also enables faster conversions, as the binary search process is governed by internal circuit conditions rather than clock period constraints.

Furthermore, SAR ADCs can be implemented in single-ended or differential configurations. While the single-ended architecture is straightforward, the differential configuration offers advantages such as better common-mode rejection, reduced harmonic distortion, and an extended input voltage range. These benefits come at the cost of increased layout area due to the duplication of key components.

In this report, the design and operation of a SAR ADC are analyzed, with emphasis on the capacitive DAC structure, comparator design, and SAR logic implementation. Simulation results demonstrate the effectiveness of the proposed enhancements, confirming the suitability of SAR ADCs for low-power, high-precision applications.

3. PROPOSED SAR ADC ARCHITECTURE:

A Synchronous Successive Approximation ADC (SAR ADC) is a widely used analog-to-digital converter that operates by iteratively approximating the input signal using a binary search algorithm. It combines simplicity, speed, and low power consumption, making it ideal for applications like data acquisition systems, signal processing, and portable devices. There are a few Key components to this Architecture.

1. Sample and Hold Circuit – This captures and holds the analog input voltage (VIN) steady during the conversion process. It also ensures that VIN does not change while the ADC is making successive approximations. The realization initially was done with PMOS and NMOS but at last was made using Verilog A code.

```
`include "constants.vams"
`include "disciplines.vams"

module VerilogA_SampleAndHold(clk,vin,vmin,vout);

parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 1p;
parameter real clk_threshold = 0.5;

input clk,vin,vmin;
output vout;

electrical vout,vin,vmin,clk;
real v;

analog begin


        @(cross(V(clk) - clk_threshold, +1))
                v = V(vin);

        V(vout) <+ transition(v,delay,ttime);
end


endmodule
```

2. Comparator – It compares the analog input voltage VIN with a reference voltage Vref. It Outputs a binary decision (either 1 or 0) based on whether Vin is higher or lower than the current approximated voltage.

3. Capacitive Digital-to-Analog Converter – It converts the digital approximation code generated by the SAR logic back into an analog voltage which is then sent to the Comparator as Vref. This Vref is used as the reference for the comparator in the next step of approximation.

4. Output Register – To evaluate the performance of the SAR ADC, an output stage is added to the system to convert the digital output into an equivalent analog signal. The analog output is then compared to the ideal expected output which should be equivalent to the input signal. The output stage consists of 2 blocks, the output register and the output DAC.

The output register's job is to receive the final SAR logic code at the rising edge of the EOC signal and releases it at the falling edge of EOC to DAC which happens at the rising edge of the next external clock cycle.

It is also realized by Veriloga and symbol is created.

```
module
VerilogA_Register_8bit(clk,in0,in1,in2,in3,in4,in5,in6,in7,out0,out1,out2,out3,out4,out5,out6,ou
t7,vdd,vss);

parameter real vtrans=0.5;
parameter real delay = 0;
parameter real ttime = 1p;
parameter real clk_threshold = 0.5;

inout vdd,vss;
input clk,in0,in1,in2,in3,in4,in5,in6,in7;
output out0,out1,out2,out3,out4,out5,out6,out7;

electrical clk,in0,in1,in2,in3,in4,in5,in6,in7,out0,out1,out2,out3,out4,out5,out6,out7,vdd,vss;
real d_0,d_1,d_2,d_3,d_4,d_5,d_6,d_7;

analog begin
        @(cross(V(clk) - clk_threshold, +1))
        begin
                d_7 = V(in7);
                d_6 = V(in6);
                d_5 = V(in5);
                d_4 = V(in4);
                d_3 = V(in3);
                d_2 = V(in2);
                d_1 = V(in1);
                d_0 = V(in0);
        end

        V(out7) <+ transition(d_7,delay,ttime);
        V(out6) <+ transition(d_6,delay,ttime);
        V(out5) <+ transition(d_5,delay,ttime);
        V(out4) <+ transition(d_4,delay,ttime);
        V(out3) <+ transition(d_3,delay,ttime);
        V(out2) <+ transition(d_2,delay,ttime);
        V(out1) <+ transition(d_1,delay,ttime);
```

```
        V(out0) <+ transition(d_0,delay,ttime);
end
endmodule
```

Figure 1 shows the final schematic made using symbol's instance.

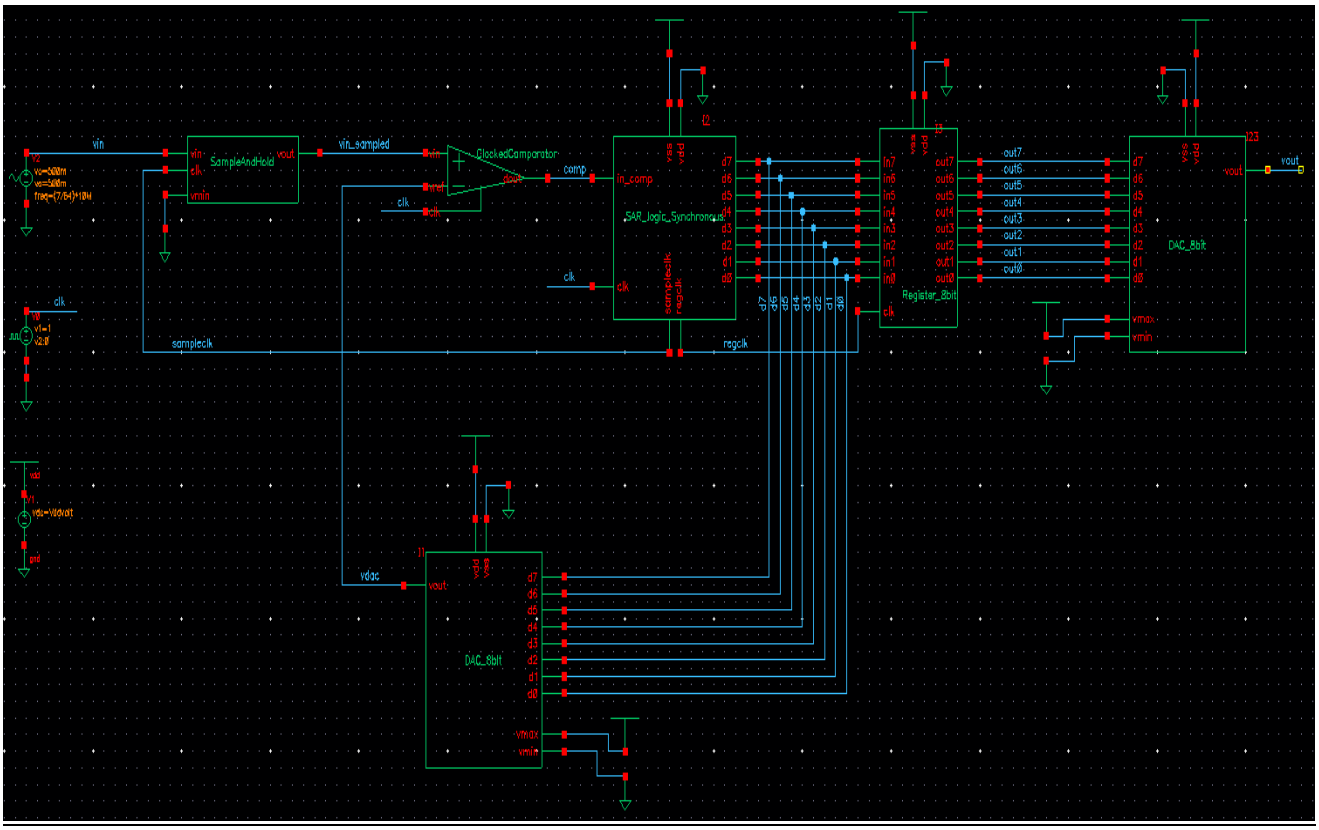

FIGURE: 1

4. WORKING PRINCIPLE:

The SAR ADC used is the Successive Approximation Register which employs the binary search process to analyze an input analog signal and synthesize its digital counterpart with a high speed and resolution. This has made it one of the most common ADC architectures owing to its high sampling rate, Resolution vs Bandwidth tradeoff, and energy efficiency. The operation is successive and every step limits the potential digital value for the given input signal.

The working process commences with the sample and hold circuit used in embracing the analog input voltage VIN and retains it at that value until the conversion is complete. This saves Vin from being altered as the ADC decides its digital counterpart. The SAR ADC type uses a successive approximation register (SAR). This is a control logic mechanism, which directs the conversion on a bit-by-bit basis. The iterative conversion is done in synergy with a digital-to-analog converter (DAC) as well as a comparator.

First, SAR turns on the most significant bit, MSB of the digital output while turning off all the rest of the bits. This digital code is then fed into the DAC where the device comes up with an analog reference voltage particularly for the case of the MSB as shown below. The comparator computes Vref with Vin. Bit stands at 1 if Vin is greater than Vref; it is reset otherwise. This decision defines how close the Vref is to Vin when the MSB of the count is set or cleared. This is done for the next substantial bit, which is 1, and a comparison is made again. The algorithm works on an incremental basis by changing each bit on the SAR code flip flops, starting from the MSB up to the LSB in order to fine tune the digital output code.

The number of iterations required turned out to be equal to the resolution of the ADC implemented. For example, the 8-bit successive approximation register (SAR) ADC needs 8 comparison cycles to produces 8-bit digital output. It has the peculiar feature that each of the steps excludes half the values, in a manner reminiscent of a binary chop. These progressive or step by step refinements make it possible for the final digital output to look considerably like Vin except for any quantization error that may be set by ADC.

Another positive aspect of using SAR ADCs is that, the conversion procedure of this type of ADC is clock controlled; every single operation taking place in distinct clock phase. This makes the architecture predictable, and appropriate for designs that need to work like a clockwork. Further, SAR ADCs are power friendly as only one compare is made in one cycle and also the complexity is much less as compared with pipeline or sigma-delta ADCs.

Due to the high precision and moderate sampling rates, the SAR ADC is used in several real applications like, industrial control systems, medical applications, data acquisition systems, etc., battery-operated systems. This is made even more attractive by its small form factor and low power requirements, making it suitable for systems where space, and/or power usage is a concern.

It effectively quantizes the input signal and decides the digital equivalent employing a sample-and-hold circuit, a DAC, and a comparator at the same time with high accuracy and swift speed.

This architecture has been widely used because it is simple, accurate and efficient in the current ADC designs. Figure 1 and Figure 2 demonstrates the process.

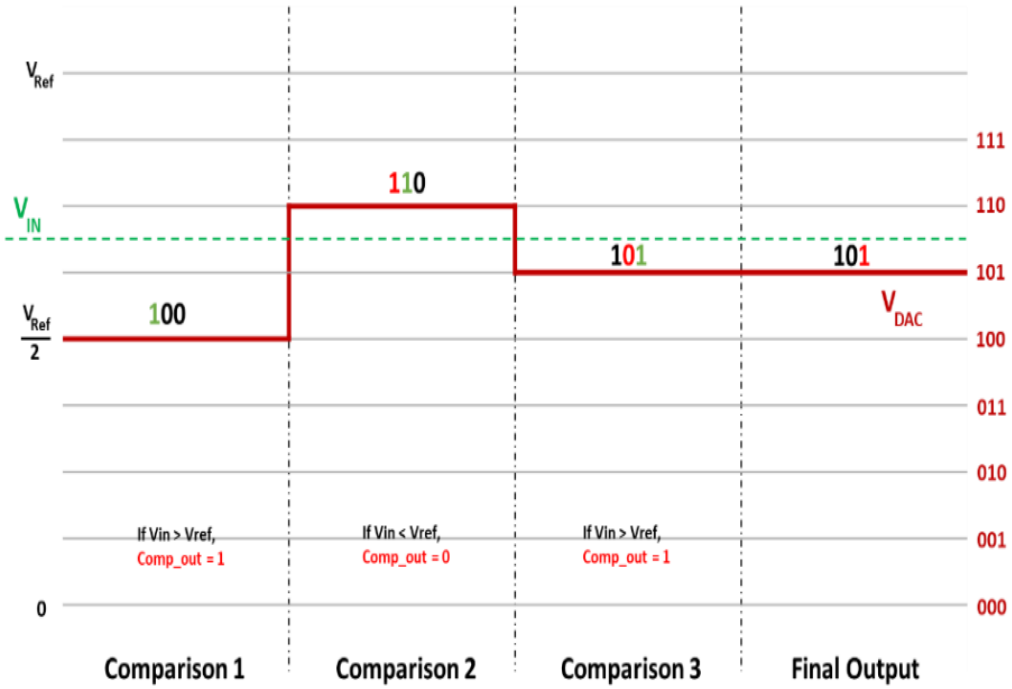

FIGURE: 2

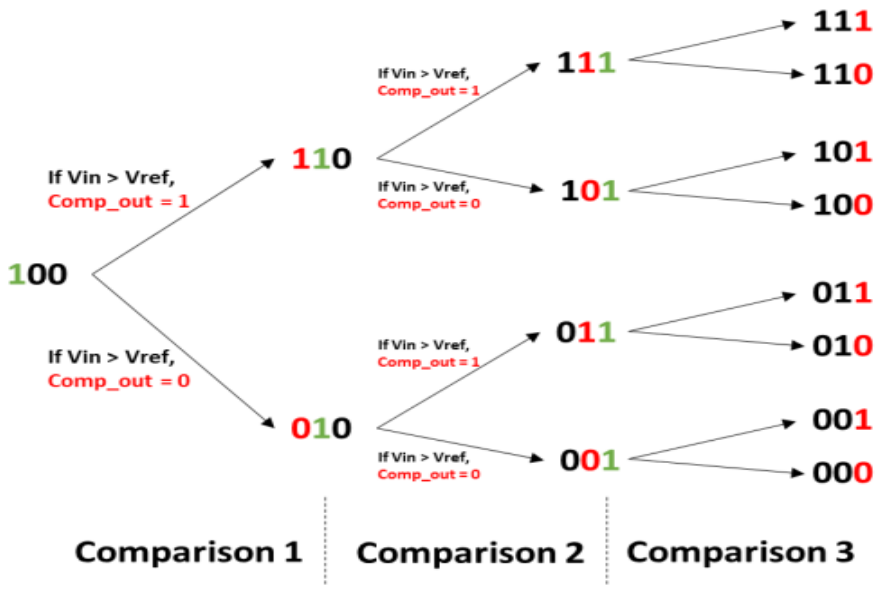

FIGURE: 3 Binary Search Pattern Concept of SAR ADC

5. SIMULATIONS AND RESULTS:

(a) Sample and Hold Circuit

Figure 4 shows the simulation of the Sample and hold circuit where the input is VIN and the output is vin_sampled.

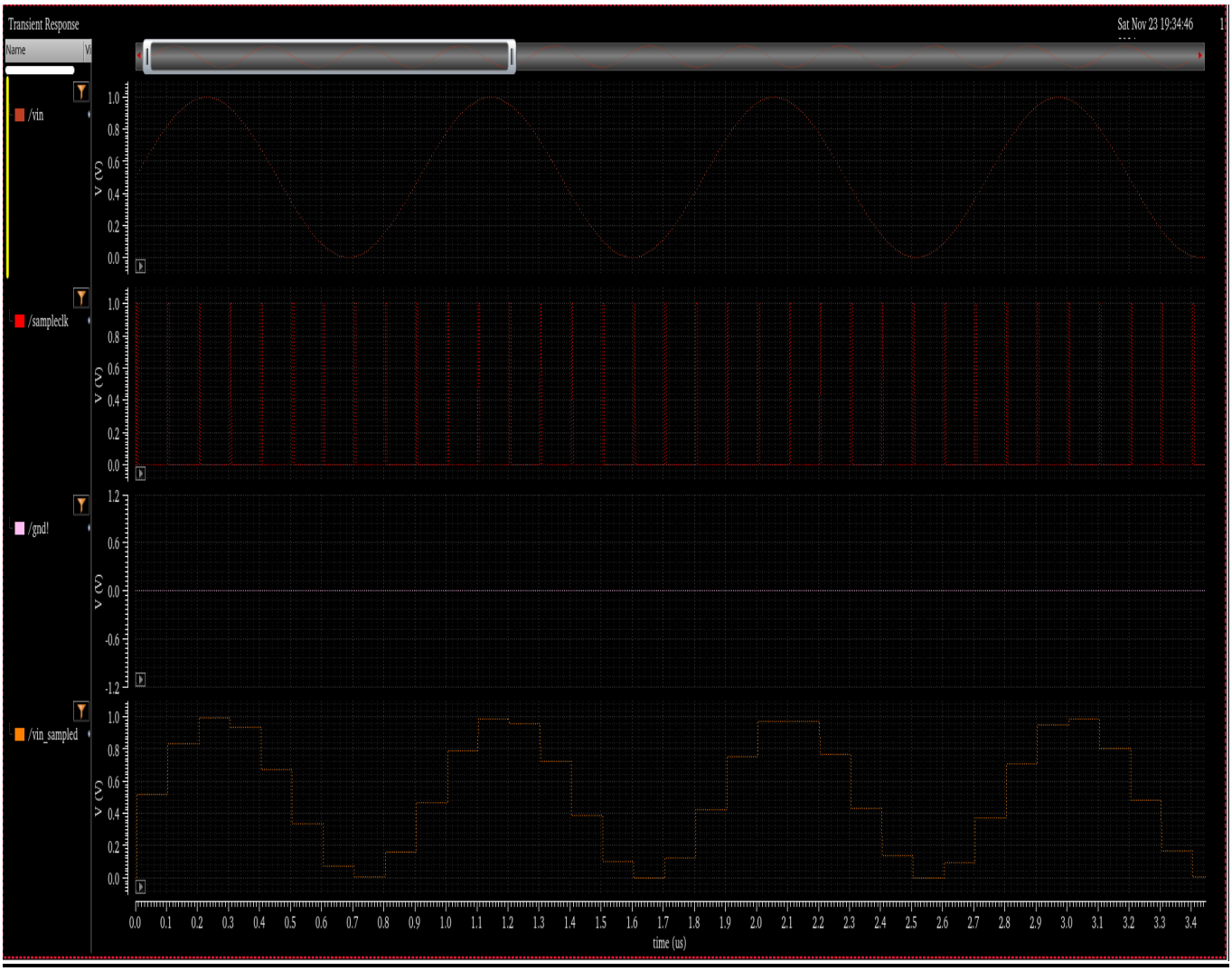

FIGURE: 4

(b) SAR LOGIC

Figure 5 shows the simulation of the SAR logic circuit where the input is from the comparator and the output is 8 bit digital data.

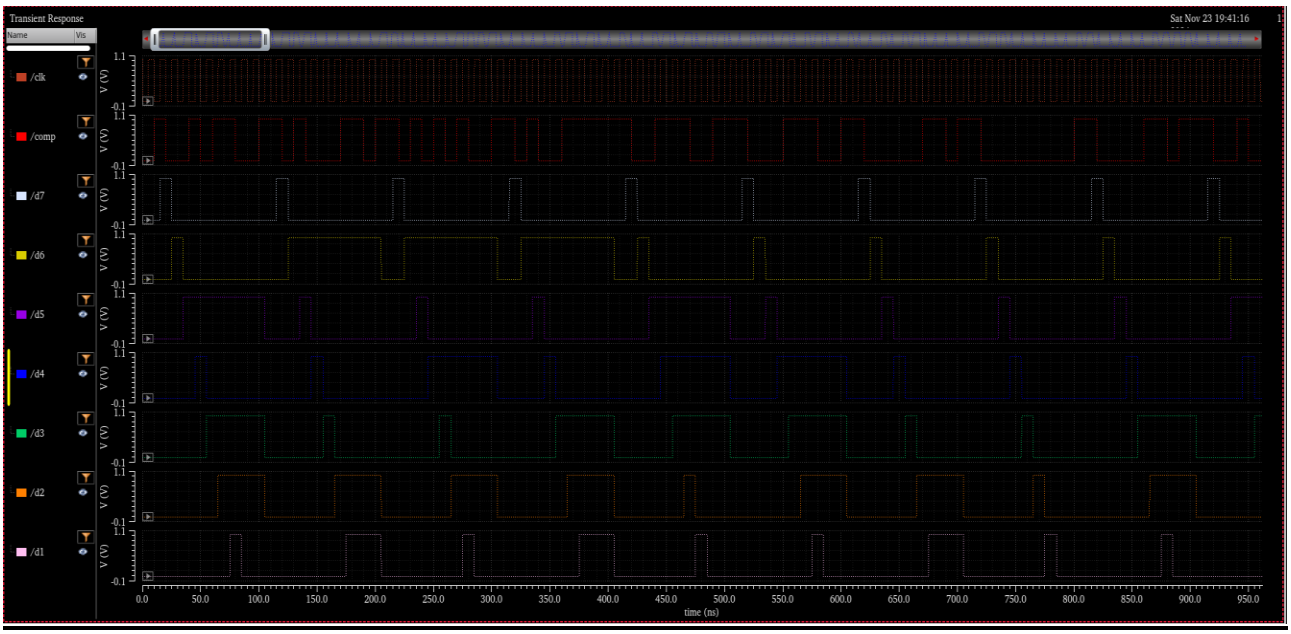

FIGURE: 5

(c) COMPARATOR

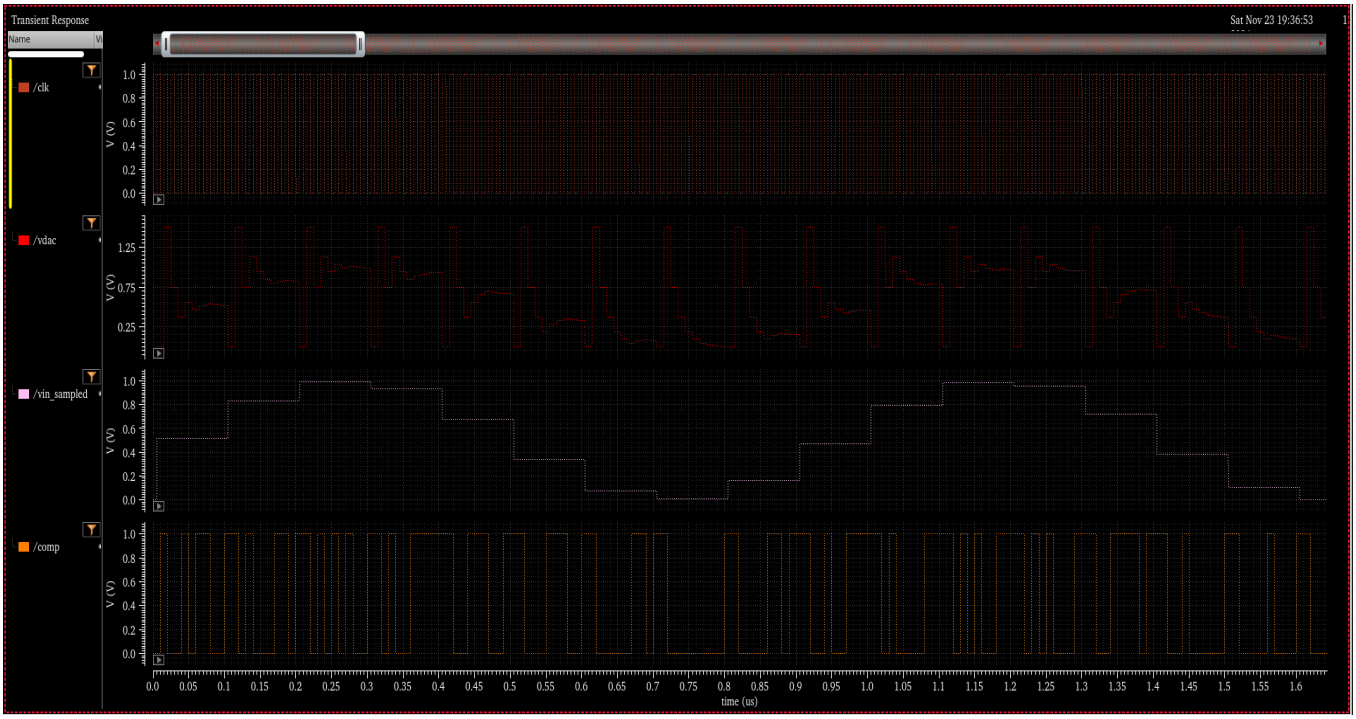

FIGURE: 6

(d) FINAL OUTPUT

Figure 7 shows the simulation of the output pare were the input is 8 bit data from SAR logic and the output is the vout from the last DAC. This step is done for comparison with the input sin wave which is further more explained in figure 8.

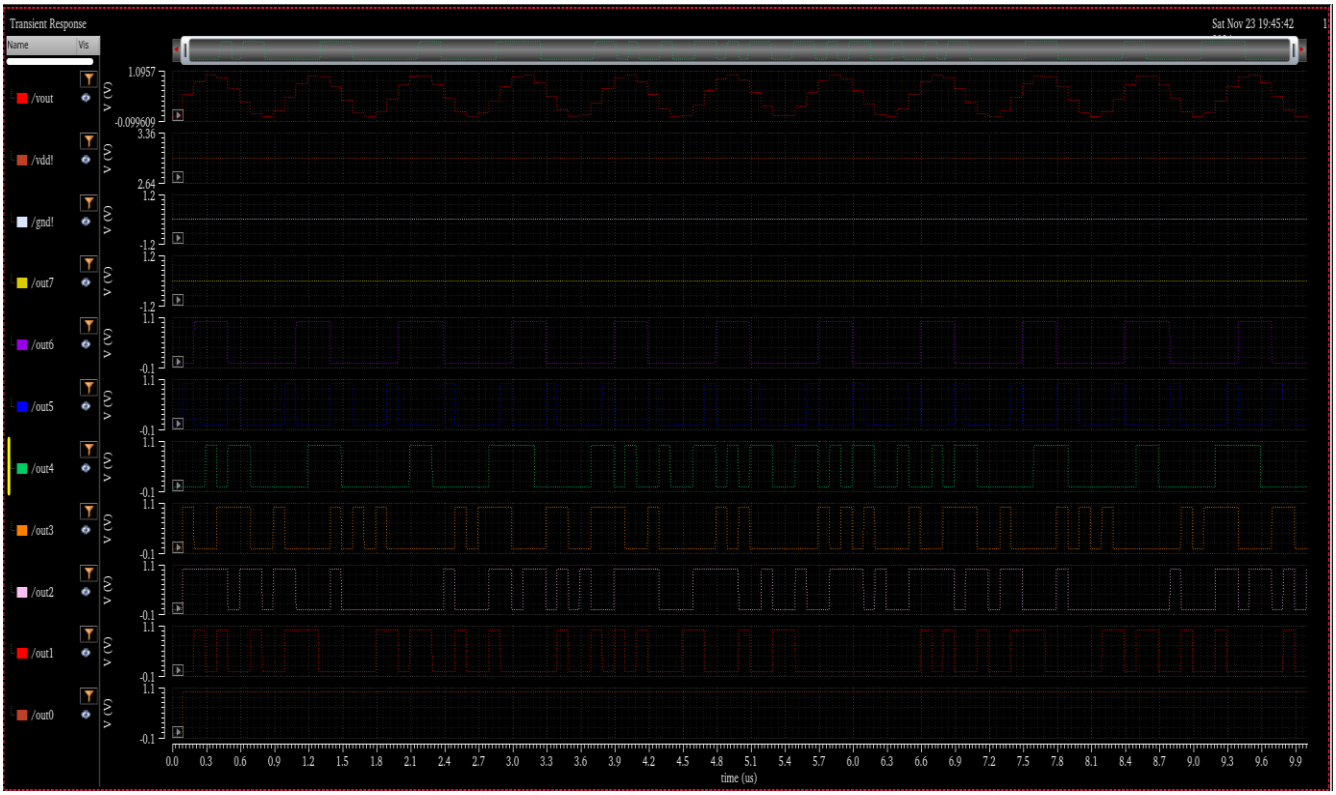

FIGURE: 7

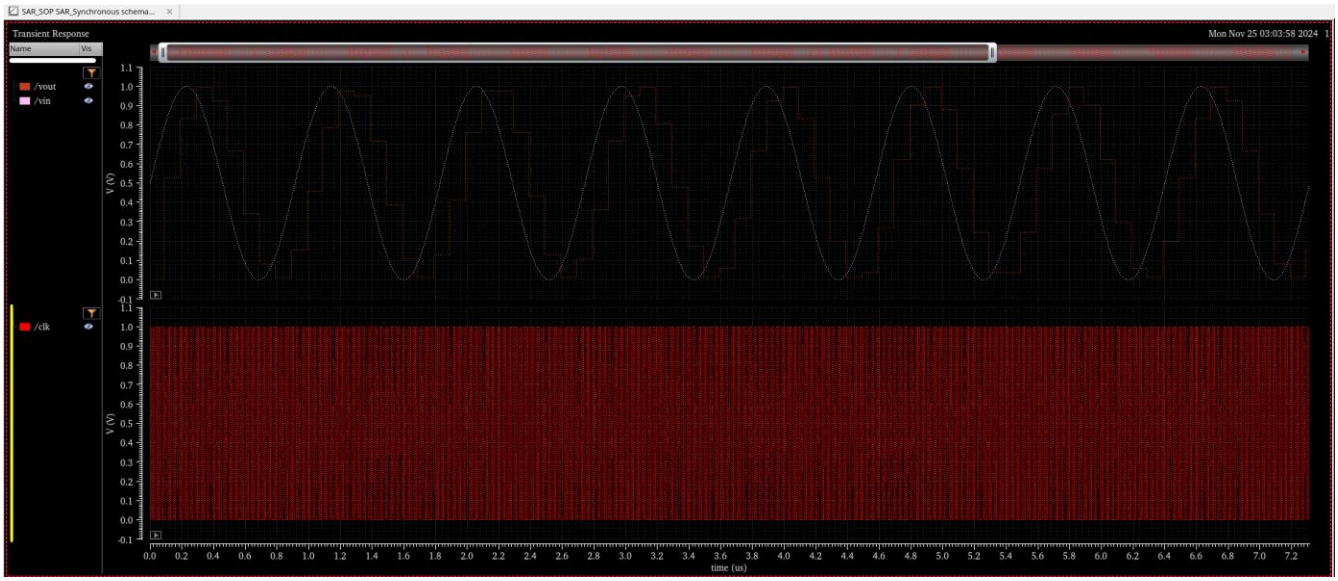

FIGURE: 8

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