Low Power Comparator Design for SAR-ADC

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Abstract: Low power consumption device is always in demand. Systems that are powered by non rechargeable batteries such as medical implant devices require low power design. This system uses Analog to Digital Converter (ADC) as an interface between analog and digital domain. This paper presents a low power comparator used in designing of Successive Approximation Register (SAR) ADC. A simple topology of comparator consist of 8 MOS working in sub-threshold region, is reported in this paper, Which is able to provide low offset voltage, high speed and low power consumption. The comparator is designed with 180nm technology and simulated in cadence EDA tools. This schematic design is efficiently works up to high speed frequency of 29MHz. The design has a low offset voltage of 5mv, low power dissipation about 1.8 µW, gain is 40.5dB and delay is 4ns.

Keywords: CMOS Comparator, Low Offset, Less Power, Low Input Offset, SAR-ADC, Cadence.

I. INTRODUCTION

Comparator acts as the key component in SAR ADC. Its efficiency can affect the SAR ADC characteristics a lot. The Overall power consumption can be minimized by using low power comparator. The comparator is a device that does comparing an analog signal with another analog signal or reference signal and gives output in single bit form. The comparator is widely used in the process of converting analog signal to digital signals. In the analog to digital conversion process, it is necessary to first sample the input. The obtained sampled signal is inserted into comparators as positive input to give digital combination of bits corresponding to the applied analog signal. The symbol of comparator is shown in figure1[1-4].
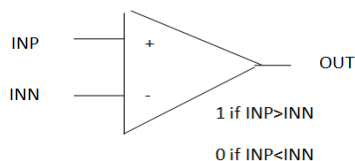

Figure.1. Symbol of Comparator.

II. MATHEMATICAL ANALYSIS

Mathematical analysis is done on the following terms to characterize the proposed circuit.

A. Sampling Frequency

The sampling frequency "fs" is defined as the reciprocal of the time interval T as [19]:

$$f_s = 1/T \tag{1}$$

The sampling frequency has to be equal or greater than twice of the frequency bandwidth of analog signals.

B. Gain

Gain of comparator can be expressed as [14]:

$$Gain = A_v = \lim_{\Delta V \to 0} \frac{V_{OH} - V_{OL}}{\Delta V} \tag{2}$$

Where,

V_{OH} = High output voltage
V_{OL} = Low output voltage
ΔV = Input voltage change.

C. Propagation Delay

It can be defined as the delay between output and input signal and calculated as [18]:

$$t_p = \frac{t_{pLH} + t_{pHL}}{2} \tag{3}$$

Where,

t_p = Propagation delay time
t_{pLH} = Rising propagation delay time
t_{pHL} = Falling propagation delay time.

Inverse of propagation delay time defines the speed of the comparator as [4]:

$$Speed = 1/t_p \tag{4}$$

D. Slew Rate

Slew rate is the rate of change of output with respect to time. It is formulated as [13]:

$$SR = dV_{out}/dt \tag{5}$$

Propagation delay time and Slew rate are interrelated as [18]:

$$t_p = \Delta T = \Delta V/SR = (V_{OH} - V_{OL})/2 \cdot SR \tag{6}$$

C. Power Dissipation

Power dissipation of the comparator is calculated from [17]:

$$P = IV_{dd}^2 \tag{7}$$

Where,

I is the output node current,
V_{dd} is the supply voltage.

III. SCHEMATIC DESIGN OF COMPARATOR

A cmos comparator is implemented using a simple two stage opamp with PMOS input drivers. All the transistors are scaled in least size i.e. W = 240nm and L = 180nm. All the transistors are

forced to work in subthreshold region for reducing power consumption. After the compilation of design, it is observed that results of this design are improved. During this process supply voltage was 1V. The comparator design eliminated the compensation capacitor which will be used for designing a high gain two stage CMOS OPAMP topology and reduced the power consumption & increase speed in the presented design. Compensation capacitor is used in two stage CMOS OPAMP for providing stability in the design, compromise with stability to obtain the high performance as low power consumption with high speed. Present CMOS comparator design is shown in Figure 2.
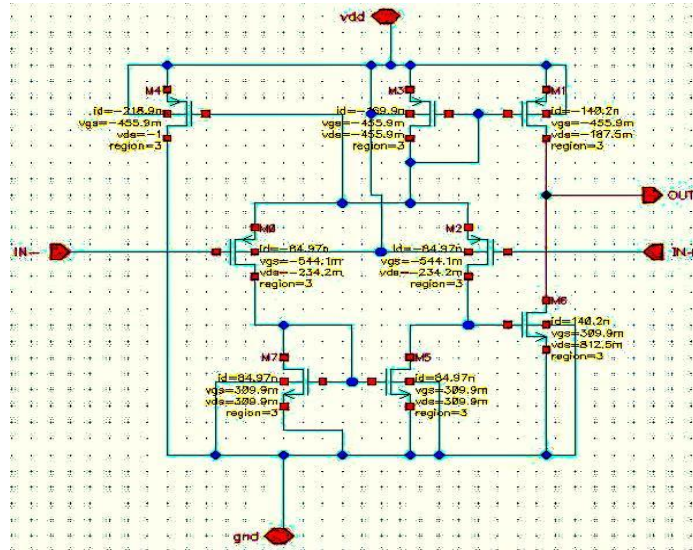

Figure.2. Schematic Design of CMOS Comparator.

III. SIMULATION RESULTS

Simulation of comparator is done by using Cadence EDA Tool. Various analyses are simulated:

A. DC Analysis

For DC analysis, both inputs IN+ and IN- is taken as DC voltage sources. Input offset voltage of the comparator was measured by taking the value of input, IN- at 500 mV and the input, INP swept from 0 to 1V. We can see the input offset voltage is approximately 5 mV for 1V supply as given in Figure.3.
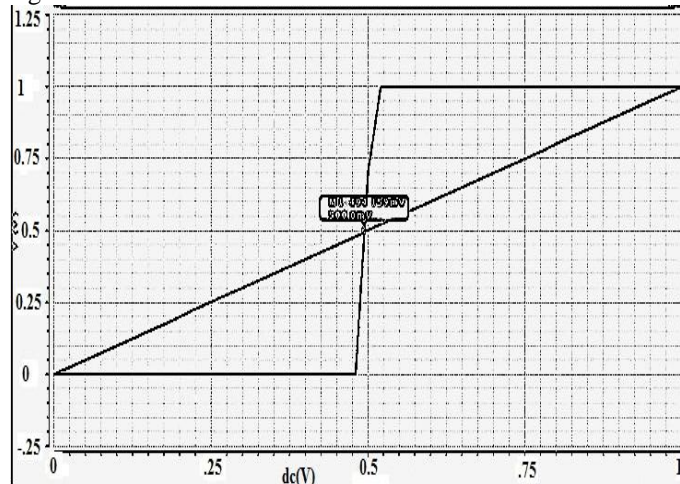

Figure.3. DC Response of Proposed Design.

B. AC Analysis

Authors have done AC analysis of the design and determined gain and bandwidth of the comparator as shown in Figure. 4 and Figure5 respectively. The unity gain bandwidth observed is 245 MHz and overall bandwidth of this design is presented in Figure. 6
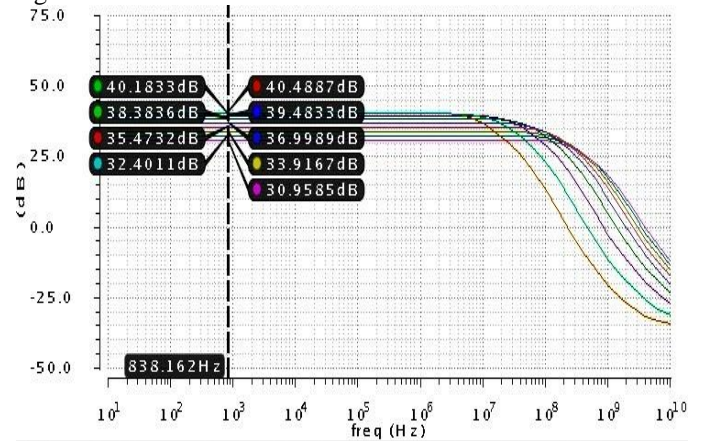

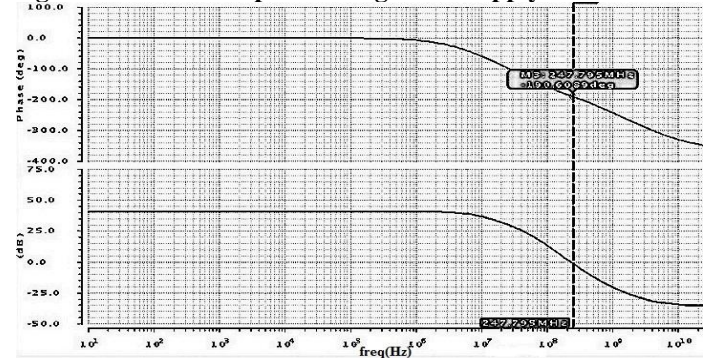**Figure.4. Gain of Proposed Design with supply of 1–1.8 V.**

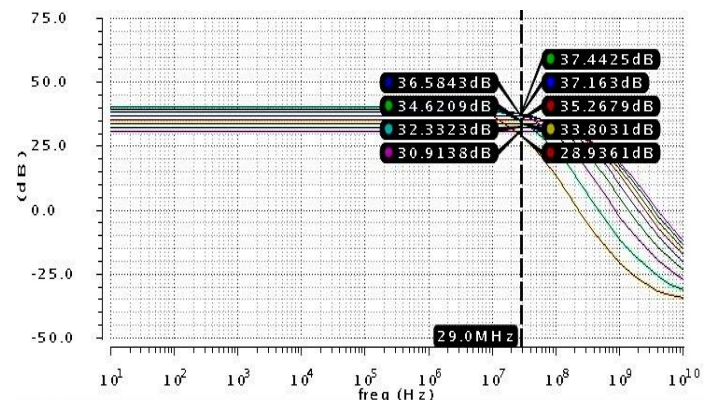**Figure.5. Unity Gain Bandwidth of Proposed Design.**

Figure.6. Bandwidth Graph of Proposed Design.

C. Transient Analysis

Comparator is specifically designed for SAR ADC which is used in biomedical device. Biopotential signals are in the range of 0.1 to 5mV and frequency up to 10KHz. For transient response, IN+ is given sinusoidal voltage of amplitude 200mV and frequency of 100KHz and IN- is given with sinusoidal supply of 100mV amplitude and of same frequency. The transient output of comparator is given in Figure.7.
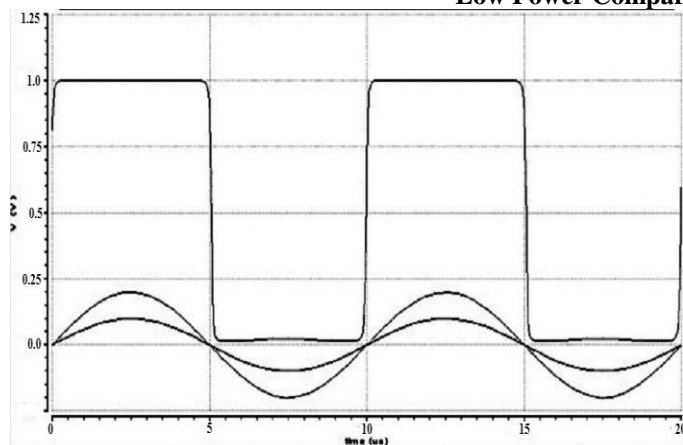
Figure.7. Output Waveform of Proposed Design.

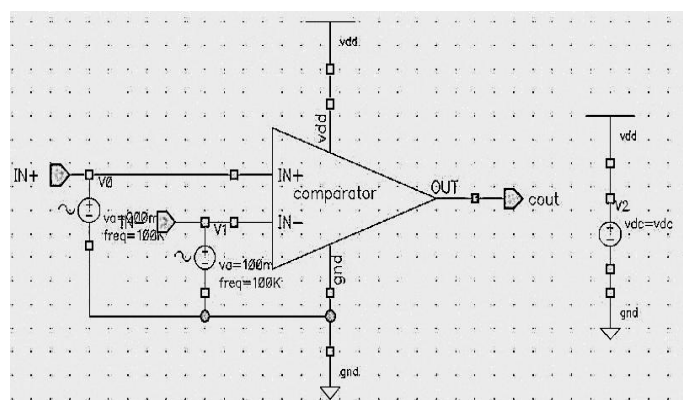Authors have tested the design and set up for testing of comparator is shown in Figure. 8.

Figure.8. Test bench Set up for Proposed Circuit.

D. Power Measurement

Authors have measured DC and transient power that is 0.5 µW and 1.3 µW respectively. Hence total power consumption of comparator is 1.8uW under 1 Volt supply. Maximum transient power consumption of this design is 56uW for 1.8V supply.
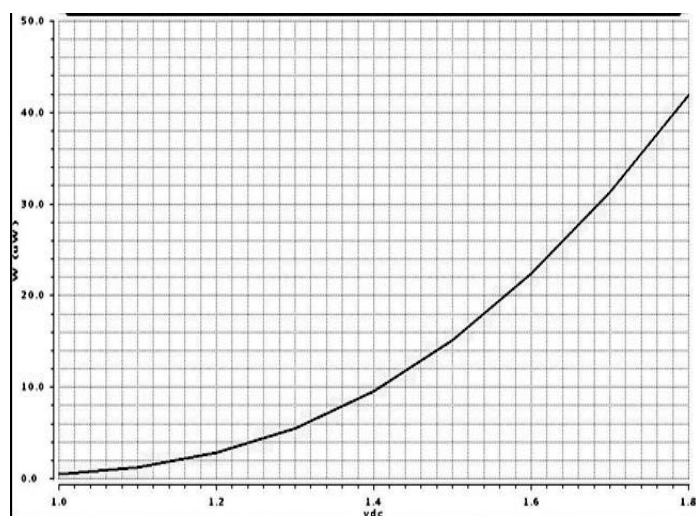

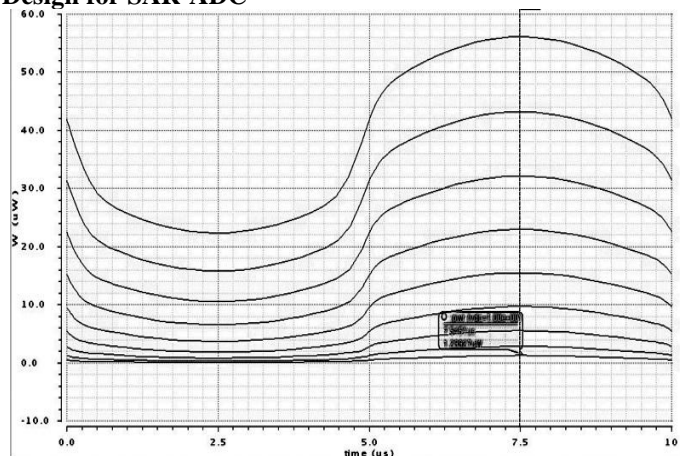**Figure.9. DC Power Graph of Proposed Design.**

Figure.10. AC Power Graph of Proposed Design with Different Supply Voltage.

E. Delay Measurement

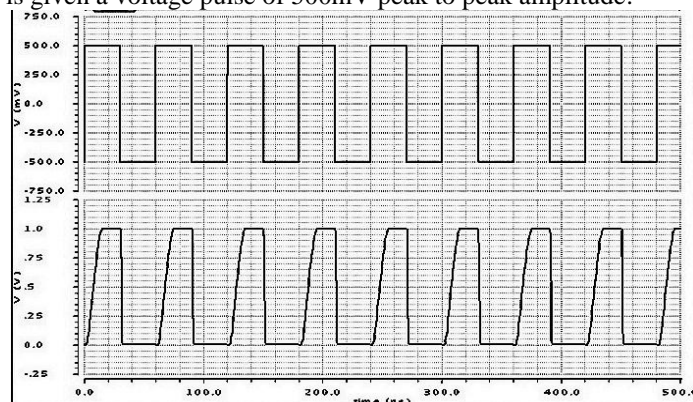For delay measurement, input IN- is grounded and input IN+ is given a voltage pulse of 500mV peak to peak amplitude.

Figure.11. Delay Measurement.

The values obtained from the Cadence calculator for 1V supply are:

t_{pLH} = 6ns

t_{pHL} = 2ns

t_p = 4ns

Slew rate (positive) = 92V/µs

F. Performance Metrics

The comparator is optimized for 1V supply and various value carried out as

Table.1 Analysis of the Proposed Design

Parameters	Value
Power supply	1V
DC Power	0.5uW
Transient power	1.3uW
Propagation delay	4ns
Speed	250MHz
Gain	40.5dB
Input offset voltage	5mV
Bandwidth	29MHz
UGB	245MHz
Sampling frequency	100KHz

IV. LAYOUT OF COMPARATOR

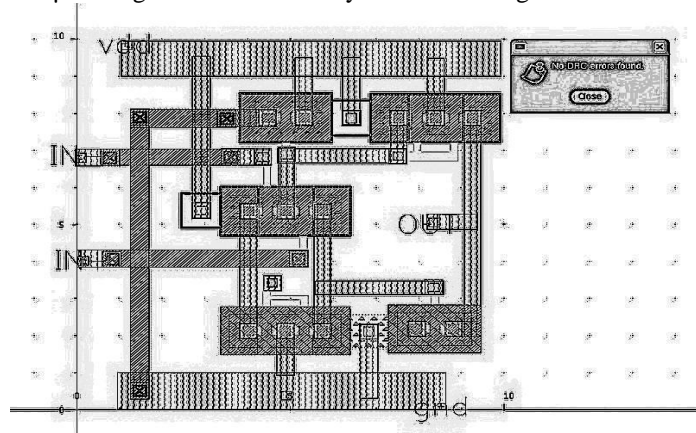Layout design is also done and it is area efficient. Its area is 100 μm². Figure11 shows the layout of this design.

Figure.12. Layout of Proposed Circuit.

IV. COMPARISION WITH PREVIOUS WORKS
Table. 2 Comparision Table

Year Ref.	2011 [3]	2012 [4]	2012 [5]	2013 [6]	2013 [7]	2014 [8]	2015 [9]	This work		
Technology(nm)	180	180	180	180	180	180	180	180		
Supply(V)	1.8	1.8	1.8	1.2	1	1.2	1.8	1	1.2	1.8
Power Consumption(μW)	740	400	265	60	70	1400	52	1.8	8.3	90
Input Offset Voltage(mV)	-	-	-	-	-	7.8	20	5	5.5	7
Propagation Delay(ns)	-	-	-	-	-	0.18	0.21	4	1.2	0.2

V. CONCLUSION

This paper concludes that the presented comparator is better than from previous architecture for voltage supply of 1V. The design consumed least power with sub threshold region. The comparator is best suited for SAR-ADC that contains minimum number of transistors. Low power characteristics is able to provide long time functioning but it can put boundaries on the design performance like expected speed and power. Luckily, the bio signals are low-frequency in nature. The biomedical systems do not demand stern specification.

VI. ACKNOWLEDGMENT

VII. REFERENCES

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