Deductive Fault Simulator

Group 1
Anshul Khandelwal (24EC64R20)
Parvez Rafat (24EC64R28)
Yasho Vardhan Gwaley (24EC64R33)

Indian Institute of Technology Kharagpur

Introduction to Fault Simulation

What is Fault Simulation?

Fault simulation is a process used in VLSI testing to analyze how a digital circuit behaves in the presence of physical defects (faults).

Why is it critical?

- To measure the effectiveness of a set of test vectors.
- This effectiveness is quantified by **Fault Coverage**.
- $\text{Fault Coverage} = \dfrac{\text{Number of Detected Faults}}{\text{Total Number of Faults}} \times 100\%$
- Essential for ensuring the quality and reliability of manufactured chips.

Project Objectives

The primary goal is to develop a robust Deductive Fault Simulator in MATLAB.

1. **Parse Circuit Netlist:** Read and interpret a gate-level Verilog circuit description.
2. **Generate Fault List:** Create a collapsed list of single stuck-at faults to eliminate redundancy.
3. **Process Test Vectors:** Read a set of input test patterns from a file.
4. **Implement Deductive Simulation:**
   - Simulate the fault-free circuit for each test vector.
   - Deduce faulty circuit behavior via fault-list propagation.
5. **Generate Statistics:** Produce a detailed fault coverage report.

Core Concept: The Deductive Method

Unlike serial simulation, which tests one fault at a time, the deductive method is a **one-pass** technique for each vector.

The Fault List (L_x)

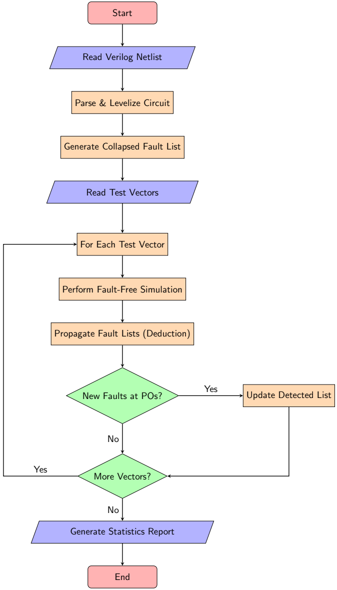
Each signal line x in the circuit has a **fault list** L_x containing all faults that cause x to deviate from its fault-free value.

- These lists are propagated logically rather than through separate simulations.

How it Works:

1. Simulate the good (fault-free) circuit once per vector.
2. For each gate, compute the output fault list (L_{out}) using set operations on input fault lists.
3. A fault is detected if it appears in the fault list of any primary output.

Project Flowchart



Parsing & Levelization

Verilog Parsing & Circuit Levelization

- Read a structural Verilog file (`.v`) and identify primary inputs/outputs, wires, and gates.
- Store circuit data in a `containers.Map` in MATLAB for efficient lookup.
- **Levelization:** Perform a topological sort to ensure a gate is simulated only after its inputs are evaluated.

Fault List Generation

Collapsed Fault List Generation

- Initially generate all single stuck-at-0 and stuck-at-1 faults.
- Apply **Fault Collapsing** to remove equivalent faults (e.g., AND gate input SA0 $\equiv$ output SA0).
- This significantly reduces simulation complexity.

Next Steps to be Implemented

Next To Dos

- Reading Test Vectors
- Deductive Fault Simulation
- Statistics Report Generation