Excellent — this is a very well-structured academic presentation.
Below is a **slide-wise academic narration** tailored for your LaTeX presentation:
Each narration is formal, technically detailed, and flows logically for a **research seminar or defense-style delivery**.

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🎓 **Narration Script: Implementation of a Deductive Fault Simulator for Digital Circuits**

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**Slide 1: Title Page**

**Narration:**

Good morning everyone. Today, I will be presenting my project titled *"Implementation of a Deductive Fault Simulator for Digital Circuits."*
This work focuses on one of the fundamental aspects of VLSI design and testing — fault simulation — which plays a crucial role in ensuring the functional correctness and reliability of integrated circuits.
Through this project, I have developed a MATLAB-based simulator that efficiently predicts circuit behavior in the presence of faults using the deductive fault simulation technique.

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**Slide 2: Introduction to Fault Simulation**

**Narration:**

Fault simulation is a critical process in the domain of digital circuit testing. It allows us to analyze how a circuit behaves when certain components fail or exhibit abnormal behavior — which we represent through *fault models.*
In the context of VLSI design, fault simulation helps us assess the **effectiveness of a given set of test vectors** by measuring how many possible faults those vectors can detect.
This measure is known as **fault coverage**, calculated as the ratio of detected faults to the total number of modeled faults.

Achieving high fault coverage is essential for ensuring that the chips fabricated from a given design are reliable and defect-free.
As illustrated in the figure, modern integrated circuits contain millions of logic gates, making exhaustive physical testing impractical. Hence, efficient fault simulation tools become indispensable for test engineers.

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**Slide 3: Project Objectives**

**Narration:**

The primary objective of this project was to design and implement a robust deductive fault simulator in MATLAB.
The project workflow can be summarized into five major stages:

First, the simulator must be capable of **parsing a Verilog netlist** and interpreting the circuit structure — identifying all gates, nodes, and interconnections.
Second, it must **generate a collapsed fault list**, which minimizes redundancy by eliminating equivalent stuck-at faults.
Third, the simulator should **process a set of test vectors** supplied as input, each representing a unique combination of primary input values.
Fourth, the **deductive simulation** is performed — wherein the fault-free behavior is simulated once, and fault propagation is logically deduced instead of re-simulating for each fault.
Finally, the system should **generate detailed statistical reports**, including fault detection and coverage percentages.

These objectives collectively ensure an efficient and analytically sound simulation framework.

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**Slide 4: Core Concept – The Deductive Method**

**Narration:**

The deductive fault simulation technique differs fundamentally from the traditional serial approach.
In serial simulation, each fault is injected and analyzed individually — a time-consuming process when the fault list is large.
In contrast, the deductive method performs **a single-pass analysis per test vector**, using set operations to infer which faults would alter the output.

Each signal line, denoted as *x*, maintains a **fault list ( L_x )** — representing all faults that could cause the signal to deviate from its correct value.
Instead of repeatedly simulating the entire circuit for each fault, these fault lists are **propagated logically** through the network.

The process begins with a fault-free simulation to determine the reference values. Then, for every gate, the output fault list is computed as a function of its inputs' fault lists.
A fault is deemed detected if it appears in the fault list of any **primary output**.

This single-pass deductive approach achieves **significant computational efficiency** while maintaining analytical accuracy.

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**Slide 5: Step 1 – Parsing and Levelization**

**Narration:**

The first step in the simulator's workflow involves **parsing the Verilog netlist** and performing **circuit levelization**.
The parser reads a gate-level structural Verilog file, identifies all primary inputs, outputs, and intermediate nodes, and stores this data in MATLAB's associative container, containers.Map, which provides efficient key-based access.

Levelization ensures that during simulation, each gate is processed only after all its input values are known.
This is achieved through a **topological sort**, effectively transforming the circuit into a sequence of computation levels.
This ordered structure forms the backbone of deterministic simulation and prevents any dependency conflicts.

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**Slide 6: Step 2 – Fault List Generation**

**Narration:**

The second stage involves generating and optimizing the fault list.
Initially, all possible **single stuck-at faults** — both stuck-at-0 and stuck-at-1 — are enumerated for every signal line.
However, many of these faults are functionally redundant or equivalent.

Through a process known as **fault collapsing**, logically equivalent faults are removed. For instance, in an AND gate, an input stuck-at-0 fault is equivalent to an output stuck-at-0 fault.

By eliminating such redundant faults, the simulator significantly reduces the overall fault space, thereby improving the efficiency of the subsequent deductive simulation process.

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**Slide 7: Step 3 – Simulation Loop**

**Narration:**

The third stage represents the core simulation loop that processes all test vectors.

In the **fault-free simulation phase**, each test vector is applied to the primary inputs, and logic values are propagated through the levelized circuit to establish a correct reference response.

In the **deductive propagation phase**, fault lists are initialized at the primary inputs and propagated through the circuit using logical deduction rules specific to each gate type.
Faults that reach primary outputs are marked as detected. Once a fault is detected, the simulator employs **fault dropping** — removing it from further analysis to save computational effort.

This approach ensures that every test vector contributes incrementally toward complete fault coverage.

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**Slide 8: Project Flowchart**

**Narration:**

This flowchart presents a consolidated view of the entire project workflow.

The process begins with reading the Verilog netlist, followed by parsing and levelizing the circuit.
Once the collapsed fault list is generated, the simulator reads the test vectors and initiates a loop that processes each vector sequentially.

For every vector, the simulator performs a fault-free simulation, propagates fault lists, and checks for new faults at the primary outputs.
When new faults are detected, the detected fault list is updated accordingly.

The loop continues until all test vectors have been processed, after which a comprehensive statistical report is generated.

This structured pipeline ensures deterministic execution, modular design, and efficient fault detection.

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**Slide 9: Implementation Details in MATLAB**

**Narration:**

The entire simulator was implemented in MATLAB using a modular design philosophy to enhance readability and reusability.

The central data structure is MATLAB's **containers.Map**, which acts as a hash map.
Each wire or node name is used as a key, and the corresponding value is a structured object containing attributes such as the node type, logic value, level, and fault list.

The codebase comprises multiple functional modules:

- DeductiveFaultSimulator.m serves as the main controller that orchestrates all subroutines.
- parseVerilog.m handles the parsing and levelization process.
- generateCollapsedFaults.m implements the logic for fault collapsing.
- runSimulation.m executes the deductive simulation loop.
- generateReport.m compiles and formats the output statistics.

This modularity ensures the code can be extended for larger benchmark circuits or alternative fault models with minimal modification.

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**Slide 10: Results and Analysis**

**Narration:**

To validate the simulator's functionality, it was tested using the **ISCAS'85 c17 benchmark circuit**, a standard reference used in fault simulation studies.

The circuit comprises five primary inputs, two primary outputs, six NAND gates, and eleven interconnections.
A total of five test vectors were applied, and the simulator generated a set of 22 collapsed single stuck-at faults.

As shown in the simulation report, all 22 faults were successfully detected, yielding a **fault coverage of 100%**.

This complete coverage demonstrates both the correctness of the deductive propagation algorithm and the adequacy of the test vector set.
The result also highlights the computational efficiency of the deductive method, achieving exhaustive detection in a single pass per test vector.

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**Slide 11: Conclusion**

**Narration:**

In conclusion, this project successfully implemented a **deductive fault simulator** for digital circuits in MATLAB.
The simulator is capable of parsing structural Verilog descriptions, performing fault collapsing, executing deductive fault propagation, and producing detailed fault coverage reports.

The modular and extensible nature of the implementation makes it adaptable for larger benchmark circuits and future enhancements, such as multiple fault simulation and probabilistic fault modeling.

Overall, the developed framework provides a solid foundation for further research in fault diagnosis and design-for-testability (DFT) methodologies in VLSI systems.

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  or
- Keep this as a **separate narration document** (e.g., for a written script or report appendix)?