30/7/21

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· CO (2CSE205)

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Q1 256k words of 32 bits each. (given)

∴ $256k = 2^8 \times 2^{10} = 2^{18}$

$64 = 2^6$

(a) Address bits = 18 bits
Register code = 6 bits
Indirect bit = 1bit
∴ 18 + 6 + 1 = 25bit

⇒ 32 bit each (given)
∴ (32 − 25) bit
= 7bits for op code.

(b)

I	opcode	Register	Address	
1bit	7bits	6bits	18 bits	= 32 bits

(c) There are 32 bits in data memory and 18 bits in address memory.

Q3 (1) After execution of following instruction:-

PUSH	4	TOS ← 4
PUSH	7	TOS ← 7
PUSH	8	TOS ← 8
ADD		TOS ← 7+8 = 15
PUSH	10	TOS ← 10
MUL		TOS ← (7+8) * 10 = 150

Remaining value will be 4.
∴ After execution of instruction value remaining will be, 4.

Q3 (2) Initial value of R = 75 in hexadecimal, in Binary its value is R = 01110101

(a) Add immediate operand C7 to R

```
                1 0     1 1 1
75              0 1 1 1 0 1 0 1
C7              1 1 0 0 0 1 1 1
13C             0 0 1 1 1 1 0 0
```

C = 0 S = 0 Z = 0 V = 1

(b) Add immediate operand 2E to R

```
                1 1 1 1 1
75              0 1 1 1 0 1 0 1
2E              0 0 1 0 1 1 1 0
A3              1 0 1 0 0 0 1 1
```

C = 1 S = 1 Z = 0 V = 0

Q5 Transfer 512 words from magnetic disk starting from address 1320.

Soln (a) CPU initiats DMA by transferring 512 words to the word count register, 1320 to DMA address register. Bits to the control register to specify a write operation. This is how CPU must initialize transfer to DMA controller.

(b) Step 1 :- I/O device sends a DMA request.
Step 2 :- DMA sends BR to CPU.

Step 3 :- CPU responds with a BG (Bus grant).
Step 4 :- Contents of DMA address register are placed in address bus.
Step 5 :- DMA sends acknowledgement to I/O devices and enables the write control line to memory.
Step 6 :- Data word is placed on data bus by I/O device.
Step 7 :- Increment DMA address by 1 and decrement DMA word count register by 1.
Step 8 :- Repeat the above steps for each word transfer.

Q6 (a) No. of block = $\frac{\text{cache size}}{\text{block size}}$

$= \frac{256\ KB}{32\ Bytes} = \frac{2^8 \times 2^{10}}{2^5} = 2^{13}$

No. of sets = $\frac{2^{13}}{4} = \frac{2^{13}}{2^2} = 2^{11}$

Tag + set + byte = 32
Tag = 32 - 11 - 5
Tag = 16

(b) 32 bit address
2 valid bit
1 modified bit
1 replacement bit

Total = 36 bit
Size of cache tag directory = 36 X no. of blocks

$= 36 \times 2^{13}$

$= 294\ k$

∴ Size of cache tag directory $= 294\ k$

Q4 value of address field = 600
Processor register R2 contains number 500
:

⇒ 700 → opcode
701 – 800 → address field of above instruction
:

(a) Direct addressing = 600
(b) Immediate addressing = 701
(c) Relative addressing = 702 + 600 = 1302
(d) Register Indirect = 500
(e) Index with reg. R2 = 500 + 600 = 1100

PC = 700
R2 = 500

Address	Memory	
700	Load to AC	Mode
701	Address = 600	
702	Next Instruction	
1200		

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A2 SC is cleared at 0 at time T_5. If decoder output D_4 is active,
$D_4 T_5 : SC \leftarrow 0$, SC responds to the positive transition of the clock.