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CO [2CSE205]

(1) According to question, the initial values for registers are as follows :-

AR = 10101011
BR = 11110000
CR = 11101010
DR = 11110010

(i) AR ← AR - CR

```
  AR    1 0 1 0 1 0 1 1
- CR    1 1 1 0 1 0 1 0
       ---------------
       0 0 0 0 0 0 0 1
```

1's complement of AR = 01010100
2's complement of AR = 1's complement + 1
= 01010101

```
    1 1 1 0 1 0 1 0
+   0 1 0 1 0 1 0 1
  -----------------
  1 0 0 1 1 1 1 1 1
```

As it was carry 1, the answer is negative,

AR - CR = - 111111

(ii) CR ← AR + CR

```
AR      - 1 1 1 1 1 1
CR        1 1 1 0 1 0
```

CR 11101010
AR 00111111

2's complement of AR = 11000000 + 1
= 11000001

Now,
```
  11101010      CR
+ 11000001      AR's 2's complement
-------------
 |10101011|
```

∴ CR = 10101011

(iii) CR ← CR ^ DR

```
CR   10101011
DR   11110010
-------------
CR   10100010
```

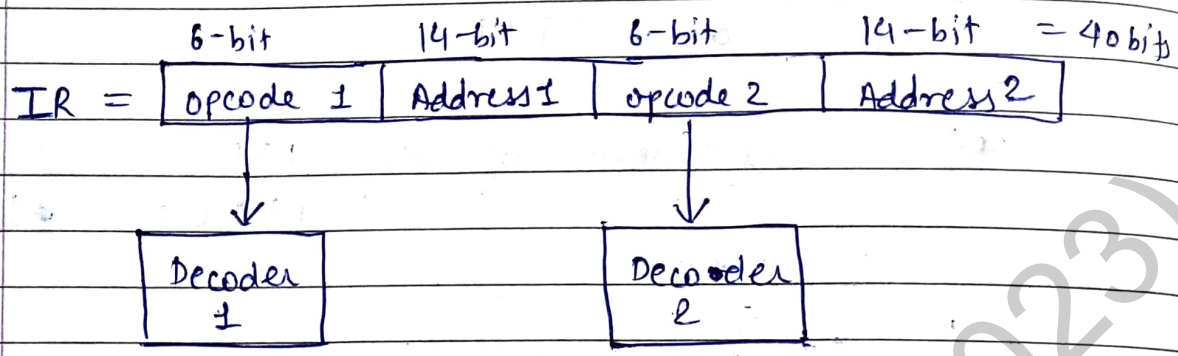
(iv) BR ← BR + 1

```
BR   11110000
   +        1
-------------
BR  |11110001|
```

∴ The final values after performing set of micro-operations are :-

AR → 111111
BR → 11110001
CR → 10100010
DR → 11110010

(2)



(i) 2 instructions are packed in one memory word.

(ii) 8 bits in IR is available in the control unit.

(iii) Step 1 : Read instruction from memory to IR and then increment Program counter (PC).

Step 2 :- Decode opcode 1

Step 3 :- Run Instruction 1 using address 1

Step 4 :- Decode opcode 2

Step 5 :- Run Instruction 2 using address 2

(3) SC is cleared at 0 at time T_5. If decoder output D_4 is active,
$D_4 T_5 : SC \leftarrow 0$, SC responds to the positive transition of the clock.