

CO - Assignment 2



Chapter 7:-

1. What is the difference between a microprocessor and a microprogram? Is it possible to design a microprocessor without a microprogram? Are all microprogrammed computers also microprocessors?

Ans

- Microprocessor is a small sized CPU, i.e computer on a chip.
- Microprogram is a program for a sequence of microoperations.
- The control unit of a microprocessor can be hardwired or microprogrammed, depending on the specific design.
- A microprogrammed computer does not have to be a microprocessor.

2. Explain the diff. b/w hardwired control & microprogrammed control. Is it possible to have a hardwired control associated with a control memory?

Ans

- Hardwired control unit is a sequential circuit that generates control signals while a microprogrammed control unit is a unit with micro-instructions in the control memory to generate control signals.
- Hardwired control does not contain a control memory.

(3)

Define the following :-

- (a) Microoperation.
- (b) microinstruction
- (c) Microprogram
- (d) Microcode

Ans

(a) Microoperation :- Micro operation is an elementary digital computer operation.

(b) Microinstruction :- An instruction that controls data flow and instruction execution sequencing in a processor at a more fundamental level than machine instruction. These are stored in control memory.

(c) Microprogram :- Microprogram is nothing but a sequence of microinstructions.

(d) Microcode :- Microcode is also a sequence of microinstructions same as microprogram.

(5)

The system shown in Fig 7-2 uses a control memory of 1024 words of 32-bits each. The microinstruction has 3 fields as shown in the fig diagram. The microoperations field has 16-bits.

(a) How many bits are there in the branch address field & the select field?

(b) If there are 16 status bits in the system

how many bits of the branch logic are used to select a status bit?

(c) How many bits are left to select an input for the multiplexers?

Ans

$$\text{control memory} = 2^0 \times 32$$

(a) Select = 6

Address = 10

Micro-operations = 16

$$= 6 + 10 + 16 = 32 \text{ bits}$$

(b) 4 bits

(c) 2 bits

(11) Using table 7-1, give 9-bit micro-operation field for the foll. micro-operations :-

(a) $AC \leftarrow AC + 1$, $DR \leftarrow DR + 1$

(b) $PC \leftarrow PC + 1$, $DR \leftarrow M[AR]$

(c) $DR \leftarrow AC$, $AC \leftarrow DR$

Ans

F1

F2

F3

(a)	011	110	000	INCAC	INCDR	NOP
(b)	000	100	101	NOP	READ	INCPL
(c)	100	101	000	DRTAC	ACTDR	NOP

(12)

Using table 7-1, convert following symbolic micro-op. to register transfer statements and to binary.

(a) READ, INCPC

(b) ACTDR, DRTAC

(c) ARTPC, DRTAC, WRITE

BinaryAns

(a) READ	$DR \leftarrow M[AR]$	$F_2 = 100$	001 100 101
DRTAC	$AC \leftarrow DR$	$F_3 = 101$	

(b) ACTDR	$DR \leftarrow AC$	$F_2 = 101$	000 100 101
DRTAC	$AC \leftarrow DR$	$F_1 = 100$	

(c) ARTPC	$PC \leftarrow AR$	$F_3 = 110$	
DRTAC	$AC \leftarrow DR$	$F_1 = 100$	}\ Impossible.
WRITE	$M[AR] \leftarrow DR$	$F_1 = 111$	Both use F1 F1

(14)

The foll. is a symbolic microprogram for an instruction in the computer defined in sec.7-3

ORG 40

NOP S JMP FETCH

NOP Z JMP FETCH

NOP I CALL IN DR

ARTPC U JMP FETCH

(a) Specify the operation performed when the instruction is executed.

(b) Convert the four microinstructions into their equivalent binary form.

Ans

(a) Branch if $S=0$, $Z=0$ (positive & non-zero AC)

(b) 40 : 000 000 000 10 00 1000000
 41 : 000 000 000 11 00 1000000
 42 : 000 000 000 01 01 1000011
 43 : 000 000 110 00 00 1000000

Chapter - 8 :-

- (1) A bus-organized CPU has 16 registers with 32-bits in each, an ALU & a destination decoder.
- (a) How many MUX are there in the bus A & what is the size of each MUX?
 - (b) How many selection inputs are needed for MUX A & MUX B?
 - (c) How many inputs & outputs are there in the decoder?
 - (d) How many inputs & op are there in the ALU for data, including input & o/p carries?
 - (e) Formulate a control word for the system assuming that the ALU has 35 operations.

- Ans
- (a) 32 MUX, each of 16×1
 - (b) 4 input each, to select one of 16 registers.
 - (c) 4-to-16 line decoder
 - (d) $32 + 32 + 1 = 65$ data input lines.
 $32 + 1 = 33$ data output lines.
 - (e)

4	4	4	6	$= 18 \text{ bits}$
SEL A	SEL B	SEL C	OPR	

(7) Convert the foll. arithmetic expressions from infix to reverse Polish notation.

$$(a) A * B + C * D + E * F$$

$$(b) A * B + A * (B * D) + C * E$$

(c) $A + B * [C * D + E * (F + G)]$

$$(d) \frac{A * [B + C * (D+E)]}{F * (G+H)}$$

Ans (a) AB* CD* EF* ++

$$(b) AB^* ABD^* CE^* +^* +$$

(b) $AB^* \quad ABD^* \quad CE^* + + +$

(c) $FG + E^* CD^* + B^* A$

(d) ABCDE * + * + * FGH + * /

(9) Convert the following numerical arithmetic expression into reverse Polish notation & show the stack operations for evaluating the numerical result

$$(3+4)[10(2+6)+8]$$

$$\underline{\text{Ans}} \quad (3+4) \cdot [10(2+6)+8] = 616$$

$$RPN = 34 + 26 + 10 * 8 + *$$

				6		10		8			
	4		2	2	8	8	80	80	88		
3	3	7	7	7	7	7	7	7	7	7	616
3	4	+	2	6	+	10	*	8	+	*	

(18)

An instruction is stored at location 300 with its address field at location 301. The address field has value 400. A processor register RI contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct ; (b) immediate ; (c) relative ; (d) register indirect ; (e) index with RI as the index register.

Solⁿ

- (a) Direct = 400
- (b) Immediate = 301
- (c) Relative = $302 + 400 = 702$
- (d) Reg. indirect = 200
- (e) Indexed = $200 + 400 = 600$

(25)

An 8-bit computer has a register R. Determine the values of status bits C, S, Z & V after each of the following instructions.

The initial value of ~~register~~ register R in each case is hexadecimal 72. The numbers below are also in hexadecimal.

- (a) Add immediate operand C6 to R
- (b) Add immediate operand E1E to R
- (c) Subtract immediate operand 9A from R
- (d) AND immediate operand 8D to R
- (e) Exclusive-OR R with R

Solⁿ

$$\begin{array}{r}
 & 11 \\
 (a) & 72 \quad 01110010 \\
 & C6 \quad 11000110 \\
 \hline
 & 00111000
 \end{array}$$

C=1, S=0, Z=0, V=0

Q1

$$\begin{array}{r}
 (b) \quad 72 \quad 0111\ 0010 \\
 1E \quad 0001\ 1110 \\
 \hline
 90 \quad 1001\ 0000
 \end{array}$$

$$C=0, S=1, Z=0, V=1$$

$$\begin{array}{r}
 (c) \quad 9A = 10011\ 010 \\
 01100110 \quad 2's \text{ complement} \\
 \hline
 72 \quad 01110010 \\
 D8 \quad 10110000
 \end{array}$$

$$C=0, S=1, Z=0, V=1$$

(Borrow = 1)

$$\begin{array}{r}
 (d) \quad 72 = 01110010 \\
 8D \quad 10001100 \\
 \hline
 00 \quad 0000000
 \end{array}$$

$$C=0, S=0, Z=1, V=0$$

$$(e) \quad C=0, S=0, Z=1, V=0$$

(3f) Three computers use register windows with the foll. characteristics. Determine the window size & total no. of registers in each computer.

	Comp. 1	Comp. 2	Comp. 3
Global R	10	8	16
Local R	10	8	16
Common R	6	8	16
No' of windows	8	4	16

Ans

$$\text{Window size} = L + 2C + G$$

$$\text{Computer 1} = 10 + 12 + 10 = 32$$

$$\text{Computer 2} = 8 + 16 + 8 = 32$$

$$\text{Computer 3} = 16 + 32 + 16 = 64$$

$$\text{Register file} = (L+C)W + G$$

$$\hookrightarrow \text{Computer 1} = (10+6)8 + 10 = 138$$

$$\hookrightarrow \text{Computer 2} = (8+8)4 + 8 = 72$$

$$\hookrightarrow \text{Computer 3} = (16+16)16 + 16 = 528$$



Chapter - 9 :-

- (2) Draw a space-time diagram for a six-segment pipeline showing the time it takes to process eight tasks.

Ans

Segment	1	2	3	4	5	6	7	8	9	10	11	12	13
1	T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8					
2		T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8				
3			T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8			
4				T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8		
5					T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8	
6						T_1	T_2	T_3	T_4	T_5	T_6	T_7	T_8

$$(k+n-1)t_p = 6+8-1 = 13 \text{ cycles}$$

- (4) A nonpipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with clock cycle of 10ns. Determine the speed up ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved?

SUP

$$t_n = 50\text{ns}$$

$$K = 6$$

$$t_p = 10\text{ns}$$

$$n = 100$$

$$S = \frac{n t_n}{(K+n-1)t_p} = \frac{100 \times 50}{(6+100-1) \times 10} = \frac{100 \times 50}{105 \times 10} = \frac{5000}{1050} = \frac{500}{105} = \frac{100}{21} = 4.76$$

$$S_{\max} = \frac{t_n}{t_p} = \frac{50}{10} = 5$$

- (5) The pipeline has following propagation times: 40ns for operands to be read from memory to registers R1 & R2, 45ns for signal to propagate through the multiplier, 5ns for transfer into R3 & 15ns to add the two numbers into R5.

(a) what is min. clock cycle time that can be used?

(b) A nonpipeline system can perform the same

operation by removing R₂ & R₄. How long will it take to multiply & add the operands without using the pipeline?

(c) calculate the speedup of the pipeline for 10 tasks & again for 100 tasks.

(d) what is the maximum speedup that can be achieved?

Ans (a) $t_p = 45 + 5 = 50 \text{ ns}$ $k = 3$

(b) $t_n = 40 + 45 + 15 = 100 \text{ ns}$

(c) $S = \frac{n t_n}{P + 2(k+n-1)t_p} = \frac{100 \times 100}{(3+9) 50} = 1.67 \text{ for } n=10$

$\therefore S = \frac{100 \times 100}{(3+9) 50} = 1.96 \text{ for } n=100.$

(d) $S_{\max} = \frac{t_n}{t_p} = \frac{100}{50} = 2$

(7) The time delay of the four segments in the pipeline are as follows:-

$$t_1 = 50 \text{ ns}, t_2 = 30 \text{ ns}, t_3 = 95 \text{ ns}, t_4 = 45 \text{ ns}.$$

The interface registers delay time $t = 5 \text{ ns}$.

(a) How long would it take to add 100 pairs of numbers in the pipeline?

(b) How can we reduce the total time to about one-half of the time calculated in part (a)?

Ans

$$\text{Clock cycle} = 95 + 5 = 100 \text{ ns}$$

$$\text{For } n=100, k=4, t_p = 100 \text{ ns}$$

Time to add 100 numbers

$$\begin{aligned} &= (k+n-1) t_p = (4+99) 100 \\ &= 10300 \text{ ns} = 10.3 \mu\text{s} \end{aligned}$$

(b) Divide segment 3 into two segments of

$$50+5 = 55 \text{ & } 45+5 = 50 \text{ ns.}$$

This makes $t_p = 55 \text{ ns} ; k=5$

$$(k+n-1) t_p = (5+99) 55 = 520 \text{ ns} = 5.2 \mu\text{s}$$

X ————— X —————