VLSI and MEMS TECHNOLOGY

PROJECT REPORT

Topic : The Rise of Semiconductor Industry

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I. Abstract

Look at you, holding that mobile phone device or staring at the screen of a computer or a laptop - not even realizing what that piece of hardware signifies. Who would've thought over 8 decades the room-sized military instruments will shrink into your hands equipping you with all those features without which you can't even think of having a life. Yes exactly, who would've thought - a bunch of nerds who were just there to implement their knowledge for the military to simplify invasion during World War-II, never thought of revolutionizing the consumer electronics industry.

This report is a case study of the events in the field of IC production which restructured the whole Semiconductor Industry. Dive right in and unfold the mystery whether it was ‘Father of Electronics’ or ‘Fathers of Electronics’!

II. Birth of the idea and tyranny of numbers

Mayhem struck the US Military during World War-II. They reached a degree of computational load, where failure losses and downtime exceeded the benefits predicted. The then used Boeing B-29 (1944) carried 300–1000 vacuum tubes and tens of thousands of passive components and ENIAC (1946) used more than 17,000 vacuum tubes. A deadlock in traditional electronics was witnessed with uproar in reduced reliability of devices and lengthened troubleshooting time.

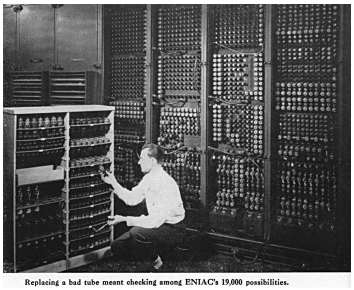

Fig. 1 - Managing Vacuum Tubes in ENIAC.

1947 marked the commencement of the era of 'intelligent machines'. The transistor was invented at Bell Labs in New Jersey in 1947 by John Bardeen, Walter Brattain, and William Shockley. The development of first commercial ICs was observed over two decades and umpteen number of scientists imparted their expertise in designing the fabrication process simplifying the requirements posed by the industry.

In 1949, a German Engineer Werner Jacobi - an employee of Siemens AG - patented an integrated-circuit-like semiconductor amplifying device with five transistors on a common substrate in a 3-stage amplifier arrangement with two transistors working "upside-down" as an impedance converter. However, this prototype was not reported to have commercial usage, yet the market saw its application in hearing aids for a short period.

A couple of years later, a British radio engineer Geoffrey Dummer put forth his vision for the electronic industry. In a public speech in Washington he quoted:
"With the advent of the transistor and the work in semiconductors generally, it seems now to be possible to envisage electronic equipment in a solid block with no connecting wires. The block may consist of layers of insulating, conducting, rectifying and amplifying materials, the electrical functions being connected by cutting out areas of the various layers."

This made him famous as "the prophet of integrated circuits" and in 1956 he produced an IC prototype made from the melt. Though a major leap, yet the ICs were expensive and had lower parameters compared to discrete devices.

In the same year a pioneer named Sidney Darlington, who later earned fame for designing Darlington Pair, filed a patent for a framework with two or three transistors integrated onto a single chip in various configurations. Moreover, Bernard Oliver patented a method of manufacturing three electrically connected planar transistors on one semiconductor crystal.

A year later, in 1953 a method came into being, forming various electronic components – transistors, resistors, lumped and distributed capacitances – on a single chip. Harwick Johnson designed an oscillator with an integrated one-transistor. The method employed a narrow strip of a semiconductor with one end of a bipolar transistor. The strip acted as a series of resistors; the lumped condensers were formed by fusion, while reverse-based p-n junctions acted as distributed capacitors. On the contrary, he did not produce an actual device but just a theoretical explanation for it.

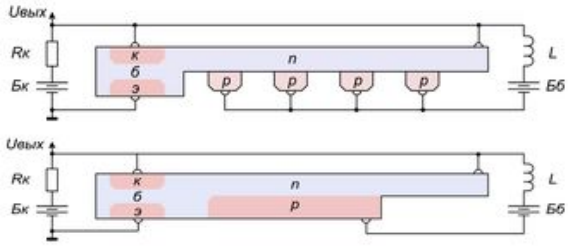

Fig. 2 - Johnson's Integrated Generator.

So the decade from 1947 to 1957 was full of many pioneers experimenting and implementing their prototypes and designs independently in their labs. These early devices featured designs where several transistors could share a common active area, but there were still some drawbacks which hindered the production of more reliable IC chips.

III. Major Breakthrough and Patent war

The second big step in the revolution was, when simultaneously at Fairchild and Texas Instruments Integrated circuit was invented.

At Texas Instruments Jack Kilby patented the Principle of Integration of Hybrid IC. At Fairchild, Jean Hoerni developed the planar transistor and Robert Noyce developed the Integrated Circuit. Also, Kurt Lehovec of Sprague Electric patented the way of Electrical Isolation.

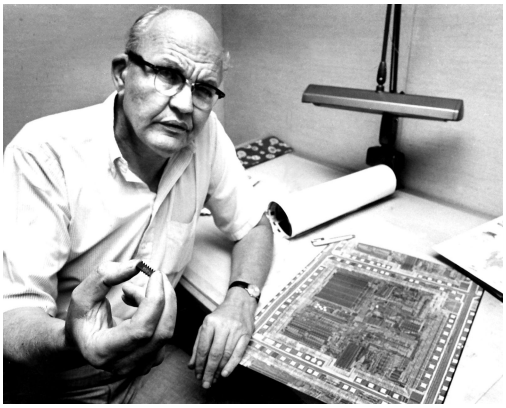

Fig. 3 - Jack Kilby with IC Designs

This clash sparked a patent war among the three. However, the US Court of Appeals ruled in the early 1960s that Noyce was the inventor of the monolithic integrated circuit chip based on adherent oxide and junction insulation technologies.

TI held a hearing with demonstrations of Kilby's inventions, at which Lehovec proved conclusively that Kilby did not mention component isolation. His focus on the Patent for Isolation was finally recognized in April 1966.

By 1965, Fairchild's planar technology became the industry standard which challenged its fierce competitor TI. Kilby 's primary patents had given little profit to Texas Instruments. TI realized that for the whole set of key IC patents, they could not claim priority, and lost interest in the patent war. Texas Instruments and Fairchild agreed in 1966 on mutual recognition of patents and on cross-licensing of key patents; Sprague joined them in 1967.

IV. Silicon ruling over Germanium

Early transistors were made of Germanium. By the mid-1950s it was replaced by Silicon, which could operate at higher temperatures, due to the efforts of Gordon Kidd (TI). Carl Frosch of Bell Labs developed wet silicon oxidation in 1955. By the end of 1958, Frosch and Lincoln Derick showed that layers of Silicon Oxide could protect silicon surfaces during diffusion processes, and could be used to mask diffusion. This revealed the fundamental advantage of SI, i.e., that "wet" silica is a mechanically strong and chemically inert electrical insulator, compared to germanium oxides.

So to conclude the following points demonstrate the preference of Si over Ge for chip manufacturing:

- Reverse current in a Si Diode is in the range of nano-Amperes. The same reverse current is in the micro-Ampere range for a Ge based diode. Diode as a device was invented to allow passage of current only in a single direction (forward bias), Hence, the feature of reverse current rejection is more evident in a Silicon-based diode.
- A Si diode has higher forward voltage potential (0.7V) than germanium (0.3V). The more current conducted, the warmer the device gets. Therefore, we can say that Ge based diodes will get into a thermal runaway as they tend to conduct more current.
- Germanium has a reverse breakdown voltage of 50-70V while Si can withstand up to 100V.
- While high power applications are taken into account, Si-based devices can tolerate high power (more than 50W), while Ge can survive applications under 10W only.

V. Key processes involved in Production

Finally, after most of the prerequisites were met, a certified production process was formulated to convert silicon in the sand to commercially viable ICs and chips. The two backbone processes of fabrication were the advent of Planar Process and Surface Passivation.

- Surface Passivation: It is the process by which a semiconductor surface is rendered inert, and as a result of interaction with air or other materials in contact with the surface or edge of the crystal does not change semiconductor properties, was first developed by Mohammad Atalla at Bell Labs in 1957. Atalla discovered that the formation of a thermally grown SiO_2 layer reduced the concentration of electronic states on the silicon surface, thus preserving the electrical characteristics of p-n junctions and preventing the gaseous ambient environment from deteriorating these electrical characteristics.
- Planar Process: Jean Hoerni was inspired by the introduction of the surface passivation cycle by Mohamed Atalla, and came up with the "planar theory." Taking advantage of the passivating effect of silicon dioxide on the surface of the silicon, Hoerni proposed making transistors that were protected by a silicon dioxide layer. This led to the first successful product implementation of the thermal oxide passivation technique for the Atalla silicon transistor.Armed with the aforementioned knowledge, Hoerni made the prototype of a planar transistor in 1959 and filed a patent application for planar process invention. By the mid-1960s the planar process became the main technology for transistor production and monolithic ICs.

These two processes as a backbone of the **complete process** are described in brief below.

a. Crystal Growth:

In this process, all the silicon melted from sand and other sources is converted into a Single Crystalline structure. The initial form of silicon is polycrystalline melt and after a bunch of processes, it is converted into a single crystal silicon wafer.

The major crystal growth techniques are-

- Bridgman Method: The process involves two related but distinct techniques used mainly to grow single crystal ingots, but which may also be used to solidify polycrystalline ingots. Polycrystal is heated above its melting point and cooled slowly from one end of its container, where there is a seed crystal. A single crystal is grown on the seed of the same crystallographic orientation as the seed material and is progressively formed along the length of the container. The is performed horizontally or vertically and involves a rotating crucible to stir the melt.

- Float Zone Method: In an inert chamber, a float zone of the melt is created in between the polycrystal and the single crystal. The chamber is heated using RF coils on the walls of the chamber. Inert gas with a low-temperature transfer coefficient is used. The ingot produced is less uniform.

- Czochralski method: EGS silicon is melted in a crucible (quartz). Dopants (Boron and Phosphorus) are added to melt. A rod mounted with a seed crystal is dipped into the molten silicon. The rod of the seed crystal is pulled slowly upwards and rotated at the same time. A large, single-crystal, cylindrical ingot can be extracted from the melt by precisely regulating the temperature gradients, pulling rate, and rotation speeds. Argon creates an inert atmosphere.

This is followed by the process of wafer preparation. The ingot is sliced into thin silicon wafers before converting them into ICs. The process of wafer preparation involves grinding, the introduction of flat, slicing, edge contouring, lapping, etching, washing, and polishing. The ingot is sliced very precisely with a thin blade of thickness in micrometers to avoid wastage of the material. The processes following it are just to ensure the purity of the wafer. Wafers have a thickness in Angstroms.

b. Epitaxial Process:

It is a type of crystal growth in which new crystalline layers are formed with a well-defined orientation for the crystalline substrate. The new layers formed are called the epitaxial film or epitaxial layer. It can be done in three ways:

- Vapor Phase Epitaxy: Silicon is deposited by doping with silicon tetrachloride and hydrogen at approximately 1200 to 1250 °C: $SiCl_{4(g)} + 2H_{2(g)} \leftrightarrow Si_{(s)} + 4HCl_{(g)}$

- Liquid Phase Epitaxy: Growth of crystal semiconductor layers on solid substrates from the melt. This occurs at temperatures below the deposited semiconductor's melting point. The semiconductor is dissolved in the melt of another material. Indium phosphide (InP) is the most commonly used substrate.

- Molecular Beam Epitaxy: A source material is heated to produce an evaporated beam of particles. These particles travel through a very high vacuum to the substrate, where they condense. MBE has lower throughput than other forms of epitaxy. Widely used for growing periodic groups III, IV, and V semiconductor crystals.

c. Oxidation:

This is the part of surface passivation devised by Atalla at Bell Labs.Oxidation is performed to ensure that the wafer is insulated from the outside environment by electric means. Silicon reacts to silicon dioxide (SiO2) by containing oxygen. This is conducted at high temperatures (e.g., 1000–1200 ° C) and within ultraclean furnaces in order to speed up this chemical reaction. The inert atmosphere is produced to prevent the introduction of even small amounts of pollutants. The oxygen that is used in the reaction is either introduced as a high purity gas or as steam (wet oxidation). Wet oxidation generally has a faster rate of growth but better electrical characteristics are provided by dry oxidation. The thermally developed oxide layer has excellent properties for electrical insulation. The reactions involved are:

$Si + 2\ H2O \rightarrow SiO2 + 2\ H2(g)$
$Si + O2 \rightarrow SiO2$
The reaction takes place in presence of oxidizing agent HCl.

d. Lithography or PhotoLithography:

Using photolithography, the surface patterns of the different integrated-circuit components can be identified repeatedly. Using a spin-on technique, the wafer surface is coated with a photosensitive layer named photoresist. A photographic plate with drawn

patterns (e.g. a quartz plate with chromium layer for patterning) is then used to expose the photoresist selectively under a deep ultraviolet illumination (UV). The areas exposed will soften (for positive photoresist). Using a chemical manufacturer, the exposed layer may then be removed allowing the mask pattern to replicate on the wafer. This method allows for the precise replication of very fine surface geometries. After the etching step(s), the photoresist is stripped away, leaving behind a permanent pattern of the photomask on the wafer surface.

e. Etching:

Chemical (wet) etching or RIE dry etching is done to permanently imprint the photographic patterns onto the wafer. Different chemical solutions are utilized to remove various layers. Hydrofluoric (HF) acid for example is used to etch SiO2, potassium hydroxide (KOH) for silicon, and aluminum phosphoric acid. In wet etching, the chemical attacks exposed regions in all directions (isotropic etching), which are not protected by the photoresist layer. Therefore the dimensions of the actual pattern will differ slightly from the original pattern in wet etching, small undercuts appear. If the exact dimension is critical, then RIE is used for dry etching. This approach is an exposed surface spatial bombardment, using a corrosive gas (or ions). The etched layer cross-section is typically highly directional (anisotropic etching) and has the same dimensions as the photoresist pattern.

f. Diffusion:

Diffusion Is a process by which atoms move from a region of high concentration to a low concentration area. It is a mechanism by which impurity atoms (dopants) are inserted into silicon to change its resistivity. The rate of diffusion of dopants in silicon is a strong temperature function, therefore it is performed at high temperatures (1000–1200 ° C). The impurities froze in position, when the wafer is cooled to room temperature. Boron(p-type), Phosphorus(n-type), and Arsenic(n-type) are the most common impurities used as dopants. Thin layers of silicon dioxide effectively block those dopants. A p-n junction (diode) is formed by diffusing the boron into an n-type substrate. The diffused layer can also be used as a conducting layer with very low resistivity, if the doping concentration is heavy.

g. Ion Implantation:

The process used for the introduction of impurities into semiconductor crystal is ion implantation. An ion implanter produces the desired dopant ions, accelerates them through an electric field, and allows them to strike the surface of the semiconductor. The ions get trapped in a lattice of quartz. The penetration depth is connected to the ion beam energy which can be regulated by the accelerating-field voltage. The number of ions

being implanted can be controlled by varying the current of the beam (ion flow). Since both voltage and current can be measured and controlled with precision, ion implantation results in impurity profiles that are much more accurate and reproducible than diffusion. In addition, ion implantation may occur at room temperature. Ion implantation is normally used when precise control of the doping profile is essential for the operation of devices.

h. Metallization:

Metallization is carried out to interconnect the different components (transistors, condensers, etc.) to form the desired integrated circuit. It requires the deposition of metal over the entire silicon sheet. It then selectively etches the required interconnection pattern. The layer of metal is typically deposited via a sputtering operation. A pure metal disk (e.g., 99.99 percent aim for aluminum) is put inside a vacuum chamber under an Ar (argon) ion gun. The wafers are placed above the target within the chamber, too. However, the ions are designed to physically attack aim and knock off the metal atoms. Such metal atoms cover all chamber surfaces, including the wafers. The metal film thickness can be controlled by the length of the sputtering time, which is normally within 1 to 2 minutes. The interconnections between metals can then be described using photolithography and etching steps. Packaged ICs are big enough to contain information that distinguishes them. Four specific parts are the name or emblem of the producer, the model number, the batch number and serial number of the component production and a four-digit date code to indicate when the chip was made.

i. Packaging:

A finished silicon wafer has several hundred circuits or chips finished in it. A chip may contain 10 to more than 10 million transistors, each chip being rectangular and on one side being up to tens of millimetres. The circuits will be electrically tested first using an automated probing device. Bad circuits are later marked for labeling. Then, the circuits are separated by dicing, and the successful circuits are placed in packages (headers). Fine gold wires are used to interconnect the packet's pins to the die metallization pattern. Finally, the package is sealed in a vacuum or in an inert atmosphere using plastic or epoxy.

VI. Hurdles in production

While the industry witnessed the uplift in the fabrication process, some hurdles were imposed by the market's requirement for commercial standards. The three fundamental problems were-

a. Integration of all components on a single piece of chip. Reliability was a major issue.

b. Isolation of electrical components on the chip. Unwanted interconnection caused an undesired flow of current. Heating and power loss was observed.
c. Connection of isolated components internally. The only solution is extremely expensive and time-consuming connection using gold wires.

Similar to the scenario where several scientists developed the IC design, it happened that three different companies TI, Sprague Electronics, and Fairchild Semiconductor held the key patents to each of these problems.

a. Integration Solution by Jack Kilby (TI)

On an expedition for 'miniaturization' of ICs, he formulated three existing assets:

- The only thing that a semiconductor company can successfully produce is semiconductors.
- All circuit elements, including resistors and capacitors, can be made of a semiconductor.
- All circuit components can be formed on one semiconductor crystal, adding only the interconnections.

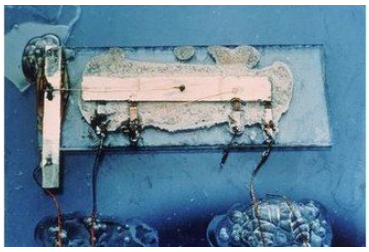

Fig. 4 - Kilby's Hybrid IC.

In 1958 Kilby used these concepts to assemble the prototype of an IC using discrete components on one chip. The regular Texas Instruments chip was 10x10 mm in size for the output of 25 (5x5) mesa transistors. Kilby cut it into 10x1.6 mm strips of five-transistor, but later used no more than two strips. He developed the first IC device that was a single-transistor oscillator with distributed input from RC. The second prototype had a two-transistor trigger in it.But still, this solution did not cater to the problem of isolation and interconnection - the components were separated by cutting grooves on the chip and connected by gold wires - hence the ICs produced were of Hybrid type only, not Monolithic.

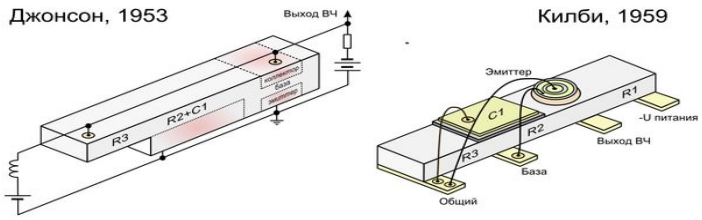

Fig. 5 - Comparison of the oscillators by Johnson (on the left, with an alloyed transistor, length: 10 mm, width: 1.6 mm) and Kilby (on the right, with mesa transistor).

b. Solution for Isolation:
    - By Kurt Lehovec (Sprague) :

Inspired by a seminar at Princeton in late 1958, in which Wallmark presented his vision of the fundamental problems in microelectronics, Lehovec found a simple solution to the problem of isolation that used the p-n junction.He proposed that - *"It is well-known that a p-n junction has a high impedance to electric current, in reverse bias. Therefore, any desired degree of electrical insulation between two components assembled on the same slice can be achieved by having a sufficiently large number of p-n junctions in series between two components."*

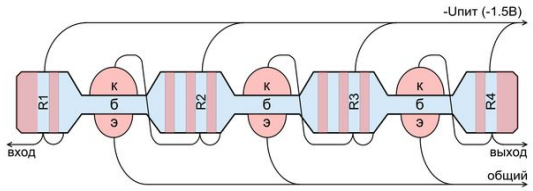

Fig. 6 - Cross-section of a three-stage amplifier (three transistors, four resistors). Blue areas: n-type conductivity, red: p-type, length: 2.2 mm, thickness: 0.1 mm.

The necessary tests were carried out on the transistors available at Sprague. The device designed was a linear structure 2.2×0.5×0.1 mm in size, which was divided into isolated n-type cells by p-n junctions. The type of conductivity was determined by the crystal's pulling speed: an indium-rich p-type layer was formed at a slow rate, while an arsenic-rich n-type layer was created at a high speed.All electrical connections were made by hand, using gold wires.

- By Robert Noyce (Fairchild) :

In 1959 Noyce defined an integrator circuit. The device's transistors, diodes, and resistors are isolated by p-n junctions from each other, in a different way than Lehovec's proposed solution. The manufacturing process began with a highly resistive intrinsic passivated silicon layer chip.

The first step in photolithography was aimed at exposing planned devices and diffusing impurities to create "wells" in the entire chip with low resistance.

Then, conventional planar devices within those wells are formed. Unlike the Lehovec solution, 2-D structures were developed in this approach.

Fig. 7 - Robert Noyce with his design of IC.

In 1976, Noyce claimed that he did not know about the work of Lehovec back in 1959.

c. Connection by Metallization:

This too was deciphered by Noyce in the labs of Fairchild Semiconductor. The method proposed to maintain the oxide layer between the metal layer and the surface, and to deposit the metal layer in such a way that it is securely attached to oxide. Noyce proposed deposition of aluminum by vacuum through a mask and a continuous layer deposition, followed by photolithography and etching off the excess metal.

VII. Hybrid ICs vs Monolithic ICs

By the end of the 1960s, most of the designs of ICs were of Hybrid type - less reliable, merely efficient. The formulation of Monolithic ICs was yet to be invented. But theoretically, the differences between both the concepts can be summarized below.

Table 1 : Comparison of Hybrid and Monolithic ICs

Hybrid Type	Monolithic Type
These are fabricated by interconnecting the chips and components individually via gold wires.	These are fabricated entirely on a single chip and the interconnections between the components are embedded within the substrate.
It has a ceramic substrate carrying one or more silicon chips. Uses mixed technology having GaAs chips along with silicon chips.	It has the full circuit constructed on a single piece of silicon, then enclosed in a package with connecting leads.

Large size and Cheaper	Small size and Expensive
Greater flexibility in circuit design and lower speed of operation.	Smaller flexibility in circuit design and faster speed of operation.
Interconnection established by TEM mode transmission lines.	Components are formed together by diffusion or ion implantation.

TTL Monolithic ICs were invented by James L. Buie in 1961, with sizes and configurations defined by the technological process, and all the diodes and transistors on one IC were of the same type. This became a huge commercial success and dominant IC technology during the 1970s to early 1980s.

MOS Monolithic ICs were designed by Mohamed Atalla and Dawon Kahng at Bell Labs in 1959. The MOSFET made it possible to build high-density ICs.

General Microelectronics introduced the first commercial MOS integrated circuit in 1964 in the form of a 120-transistor shift-register developed by Robert Norman. There has been no looking back since then and MOSFET has become the most critical device component in modern ICs.

VIII. A boom in the Types of Integration

As the production took off, the technology's large scale limited each chip to only a few transistors. As MOS technology saw an uplift, millions and billions of MOS transistors were implanted on a single chip, and good designs required thorough planning, giving rise to the field of Electronic Design Automation. The industry progressed from Small Scale Integration to Very Large Scale Integration.

Table 2 : Levels of Integration

Name	Year	Transistor Count	Logic Gates Number
Small Scale Integration	1964	1 to 10	1 to 12
Medium Scale Integration	1968	10 to 500	13 to 99
Large Scale Integration	1971	500 to 20,000	100 to 9999
Very Large Scale Integration	1980	20,000 to 1,000,000	10 000 to 99 999
Ultra Large Scale Integration	1984	1,000,000 and more	100 000 and more

a. Small Scale Integration (SSI): The initial designs contained a few transistors, up to 10. ICs such as Plessey SL201 and Philips TAA320 had two transistors. The numbers have increased dramatically since then.

b. Medium Scale Integration (MSI): The next generation claimed hundreds of transistors on a single chip, with hundreds of logic gates. The designing process was still done manually. This was possible due to the introduction of MOSFETs. Frank Wanlass demonstrated a 16-bit shift register with 120 MOSFETs and General Microelectronics introduced the first commercial MOS IC with 120 p-channel MOSFETs, in a 20-bit shift register.

c. Large Scale Integration (LSI): Further development led to the immersion of thousands of transistors side-by-side. Integrated circuits such as 1K-bit RAMs, calculator chips, and the first microprocessors, that began to be manufactured in moderate quantities in the early 1970s, had under 4,000 transistors.

d. Very Large Scale Integration (VLSI): The final step in the development process started in the 1980s, continuing to the present. Modern-day transistor count grows to and beyond ten billion transistors per chip. MOSFET design rules were modified to reach this milestone. The more efficient CMOS replaced PMOS and NMOS. The EDA process was adapted by industries, thus eliminating the conventional manual design process. In 1986, the first one-megabit RAM chips were released, containing more than one million transistors.

IX. Moore's Law and Globalization of the Semiconductor Industry

In 1965, Gordon Moore - an Intel R&D Engineer - observed that the number of transistors that can be packed into a given unit of space will double about every two years. This eventually came out to be known as Moore's Law. It modified to doubling transistors within 18 months in recent years. This was the basis of uproar in the levels of integration - from SSI to VLSI.

As time passed, numerous companies emerged out in the electronics domain. It started around 1960, once semiconductor chip fabrication became a viable company. As of 2018, the annual sales of semiconductors in the industry grew to over $481 billion.

The MOSFET is the driving force of the industry, accounting for 99.9% of all transistors. Estimated total of 13 sextillions (1.3×10^{22}) MOSFETs having been manufactured between 1960 and 2018.

Over the years, various companies from the USA, Taiwan, South Korea, and the European Union dominate the market.

Table 3 : Largest Semiconductor Companies

Year	Company
1960 - 1985	Texas Instruments
1985 - 1995	NEC
1995 - 2017	Intel
2017 - present	Samsung Electronics

Table 4 : Semiconductor market Share

Semiconductor Type	Percent Share (In and after 2008)
Silicon MOSFET	>90%
III-V Semiconductors	<7%
Silicon BJT	<3%

X. Future - 22nm and beyond!

How small is possible? This question keeps the engineers and researches on toes all the time. Following upon the legacy of the 'Father's of Electronics', the market waits to get revolutionized once again, to give us a mesmerizing experience with the superpowers of creators unveiling the mysteries of 'Quantum Electronics'.

Ultra Large Scale Integration is the future of fabrication. As the designing process changed from manual methods to EDA, who knows what upcoming technologies like AR/VR will be capable of. Just the thought of a manufacturing process involving gestures, holograms, voice commands sends a chill through the spine, automating the industry completely.

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