# module - 5

① Explain the single bus organization of the data path inside a processor with a diagram.

Ans:- * Processor contain only a single bus for the movement of data, address and instructions

* ALU and all the registers are inter connected via a single common Bus.

* Data & address lines of the External memory-bus is connected to the internal processor-bus via MDR & MAR respectively.

* MDR → memory data register
  MAR → memory Address Register

* MDR has 2 inputs and 2 outputs. Data may be loaded into MDR either from memory-Bus or from processor-bus

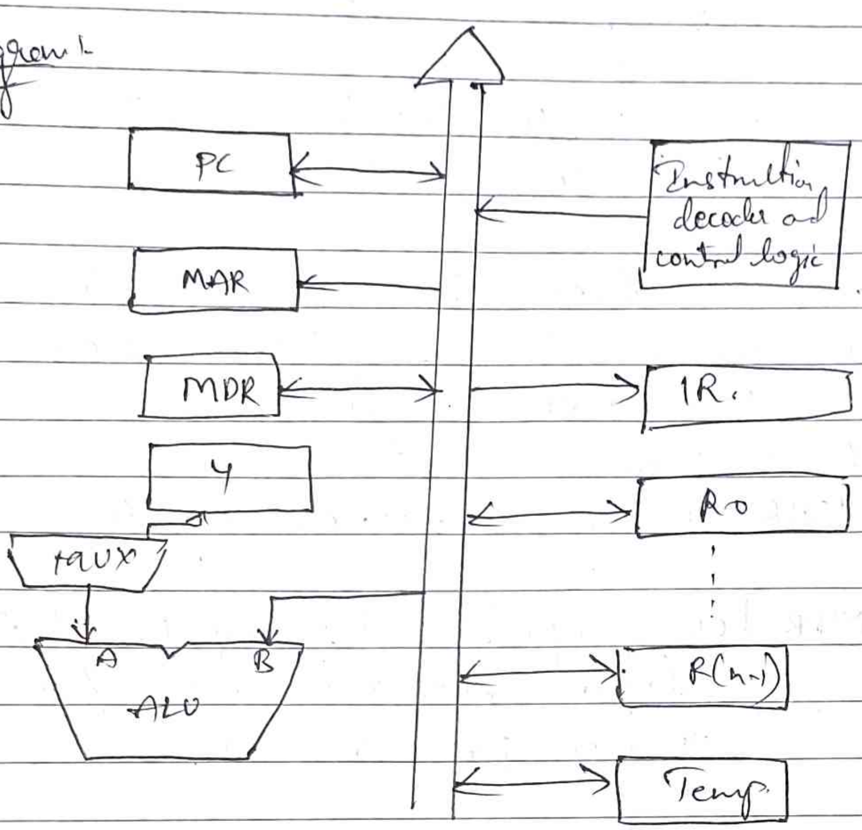
* MAR's input is connected to internal-bus; output is connected to External-bus.

* Instruction Decoder & control Unit is responsible for
- Decoding the instruction and issuing the control-signals to all the units inside the processor
- implementing the actions specified by the instruction

* Processor Registers:- Register R0 through R(n-1) are also called as General purpose Registers.

- Temporary Registers:- there are 3 temporary register in the processor
  - Y, Z and Temp are used for temporary storage during program. Execution.

(f) Diagram:-

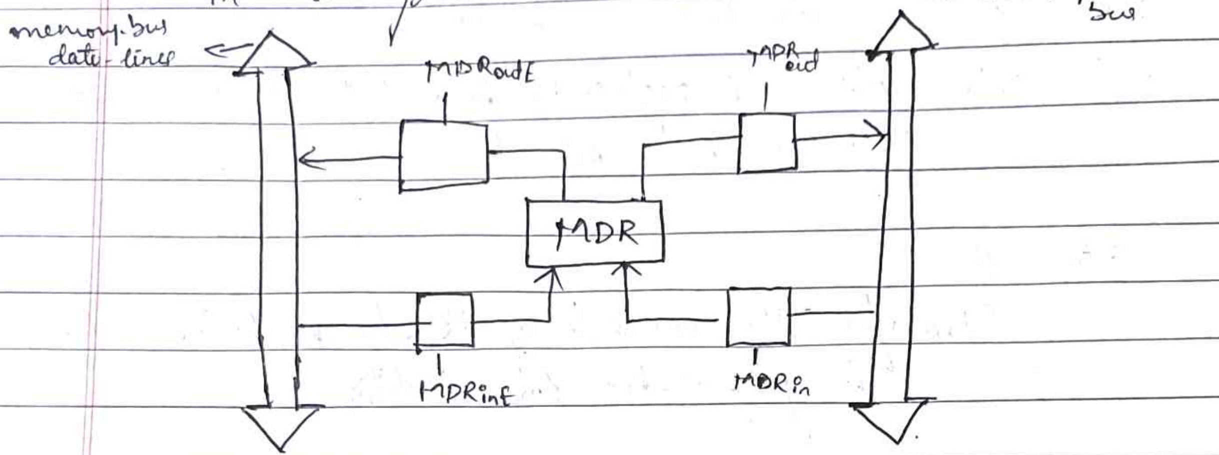


(2) Explain the process of fetching word from memory in processor.

Ans:- To fetch instruction/data from memory, the processor has to specify the address of the memory location where this information is stored and request a Read operation.

- Processor transfer required address to MAR. At the same time, processor issues Read signal on control lines of memory bus.

- when requested-data are received from memory, They are stored in MDR. from MDR, they are transferred to other register in the processor.



(3) Explain the complete set of operations Involved in Executing the instruction Add$(R_3)$R1 along with control Sequence

→ Executing this instruction requires.

- Fetch the instruction.
- Fetch the first operand.
- Perform the addition
- Load the result into R1

Step 1:- - Load the contents of the program counter (PC) into Memory Address Register (MAR).
- Send a Read request to memory.
- Add a constant value (4) to the PC using the ALU and Store the result in RegisterZ.

Step 2:- Transfer the updated value in Register Z to the PC

Step 3: move the fetched instruction from (memory data Register) MDR to Instruction Register (IR).

Step-4 (Execution Phase):

- Decode the instruction in the IR.
- Load the contents of Register R3 into MAR and issue a memory read signal.

Step-5:

Transfer the contents of Register R1 to the Y register in preparation for addition.

Step 6:- when the memory read is complete, the operand from memory is loaded into the MDR.

Step 7:- Add the operand to the value in Y using the ALU and store the result in Z.

transfer the result from Z to register R1.

End signal: Begin a new instruction fetch cycle by returning to step1.

(4) What is pipeline? Explain the performance of pipeline with an Example.

→ Pipelining is a highly Effective method for organizing tasks to run concurrently in a computer system

- It works by breaking down a sequential process into smaller steps, with each step handled by a dedicated part of the system.

- This technique is similar to an assembly line, where different stages work simultaneously to complete tasks faster.

## Pipeline Performance.

- Throughput:-
  - → The number of instructions completed per unit time.
  - → Pipelining increases throughput by overlapping instruction Execution.

- Speedup:-
  - A measure of how much faster a pipelined processor is compared to a non-pipelined processor.

$$\text{Speedup} = \frac{\text{Time without pipelining}}{\text{Time with pipelining}}$$

# module -4

① Explain Direct Memory Access with its registers & controllers.

→ It is the process of transferring the block of data at high speed in between main memory and External device (I/o devices) without continuous intervention of CPU is called as DMA.

→ The DMA operation is performed by one control circuit and is part of the I/O interface.

→ This control circuit is called DMA controller.

• Register of DMA Controller:-

* It consists of 3 type of registers:-

Starting address register:- It is used to store the starting address of the memory block.

word-count register:- The format of word count is used to store the no of words to be transferred from main memory to External devices and vice-versa.

Status and controller register:- • Status register is a hardware register in microcontrollers or CPUs.
• controller register used to configure and control specific aspects of the processor. or peripherals.

DMA controller :- It connects two External device namely disk1 and disk2 to system bus.

-DMA controller also interconnects high speed network devices to system bus.

(2). What is Bus arbitration? Explain different types of bus arbitration.

→ Any device which initiates data-transfer operation on bus at any instant of time is called as Bus-master.

→ When the bus mastership is transferred from one device to another device, the next device is ready to obtain the bus mastership.

Bus arbitration is a mechanism used in computer system to manage access to a shared bus by multiple devices.

Since multiple devices may require simultaneous access to the bus, arbitration ensures that only one devices uses the bus at a time, avoiding conflicts.

Centralized Arbitration:- A single arbiter (controller) manages access to the bus.

- Devices are assigned fixed priorities; higher-priority devices get access first.
- Polling :- The arbiter sequentially checks each device to grant access.

- Devices are connected in a chain.

Distributed Arbitration:

- All devices participate in the arbitration process without a central controller.
- Devices communicate directly to decide which gets access.
- Common in systems with high scalability requirements, like in some network protocols.

(3) What is cache Memory? Explain the different mapping functions used in cache-memory.

→ Cache memory is a small, high-speed ~~stroo~~ storage located close to the CPU, used to temporarily store frequently accessed data and instruction.

It acts as a buffer between the CPU and main memory, reducing access time and improving system performance.

Mapping functions in Cache Memory.

1. Direct-Mapping: Each block of main memory maps to Exactly one cache line.

A specific memory block can only occupy a specific location in the cache.

Advantages:- Simple and inexpensive to implement

disadvantages:- may lead to frequent cache misses multiple memory blocks map to the same cache line.

2 Fully Associative Mapping:

- A memory block can be placed in any cache line. The cache controller searches all lines to find a match.

Best for small caches requiring high hit rates. Reduces cache misses by providing flexibility in placing block.

3 Set -Associative Mapping.

→ combination of direct and fully associative mapping. The cache is divided into sets, and each memory block maps to a specific set but can be placed in any line within that set.

4 Explain the Effect of size, cost and speed in memory Hierarchy

→ The memory hierarchy in a computer system is designed to balance three key factors: size, cost and speed.

Memory Size:-

Small size:- memories like registers and cache are small in size because they are expensive and have high access speeds.

Large size:- main memory (RAM) and secondary storage (HDD/SSD) are larger because they are cheaper per unit of storage.

2. Memory Cost :-

- High cost memory :- Fast memory is built with advance, high-speed technologies like SRAM
- These are Expensive, so their size is kept limited

lower cost memory :-

- Slower memory uses cheaper technologies like DRAM or magnetic storage.
- This allows for larger storage at an affordable cost.

3. Memory Speed :- High-speed memory :-

Registers are the fastest memory located inside the CPU.

Cache memory slightly slower than register but faster than RAM, used to bridge the speed gap b/w the CPU and main memory.

Low-Speed memory :-

- RAM :- Slower than cache, used for active data and program storage.
- Secondary storage :- the slowest memory, used for long-term data storage.