JAIN COLLEGE OF ENGINEERING & RESEARCH, BELAGAVI
Programme: Computer Science and Engineering (AIML)

CONTINUOUS INTERNAL EVALUATION-I

Semester:3rd **Date: 19/10/2024**
Course:Digital Design and Computer Organization Code:BCS302 **Max. Marks: 50**
Course Coordinator: Dr. Prakash K Sonwalkar **Duration:1 Hour 30 Min**
Note: Answer any one full question choosing from each part.

Q. No.	Question	Marks	CO	R.B.T. Level
	Part -A			
1 a)	Simplify the Boolean function F (A, B, C, D) =A′B+A′C+BD using Boolean algebra.	7	1	L3
1 b)	Using a 4-variable Karnaugh map, simplify the following function: F(A,B,C,D)=∑m(0,1,2,5,8,9,10,14)	8	1	L4
1 c)	Explain the working of NAND and NOR gates. Design a circuit for a Boolean function using only NAND gates.	10	1	L4
	OR			
2 a)	What are don't-care conditions? How do they help in simplifying Boolean functions? Use an example to explain.	9	1	L2
2 b)	Implement the Boolean function F (A, B, C) =AB+BC+AC using NOR gates only.	9	1	L3
2 c)	Write a Verilog model for a simple 2-input AND gate.	7	1	L6
	Part -B			
3 a)	Explain the design procedure of a 4-bit binary adder-subtractor circuit.	7	2	L2
3 b)	Design a 3-to-8-line decoder and explain its working principle. .	8	2	L3
3 c)	What is a multiplexer? Design a 4-to-1 multiplexer and explain how it works with an example.	10	2	L4
	OR			
4 a)	What is a priority encoder? Design afour-input priority encoder and explain its operation.	7	2	L2
4 b)	Explain the concept of combinational logic circuits and provide an example of a full-adder design.	8	2	L4
4 c)	Design a Octal to Binary encoder and explain its working principle.	10	2	L6

COURSE OUTCOMES (COs)	
1	Apply the K–Map techniques to simplify various Boolean expressions.
2	Design different types of combinational and sequential circuits along with Verilog programs.
3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.
4	Explain the approaches involved in achieving communication between processor and I/O devices.
5	Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance

REVISED BLOOMS TAXONOMY LEARNING LEVEL (RBT)					
L1: Remember	L2: Understand	L3: Apply	L4: Analyze	L5: Evaluate	L6: Create

PROGRAM OUTCOMES (POs)					
1	Engineering Knowledge	5	Modern tool usage	9	Individual and Team-Work
2	Problem Analy is	6	Engineer and Society	10	Communication
3	Design / Development Solutions	7	Environment and Sustainability	11	Project Management and Finance
4	Conduct Investigations of Complex problems	8	Ethics	12	Life-long Learning

JAIN COLLEGE OF ENGINEERING & RESEARCH, BELAGAVI
Programme: Computer Science and Engineering (AIML)

CONTINUOUS INTERNAL EVALUATION-II

Semester:3rd **Date:23/12/2024**
Course:Digital Design and Computer Organization **Code:BCS302** **Max. Marks: 50**
Course Coordinator: Dr. Prakash K Sonwalkar **Duration:1 Hour 30 Min**

Note: Answer any one full question choosing from each part.

Q. No.	Question	Marks	CO	R.B.T. Level
	Part -A			
1 a)	Differentiate between a latch and a flip-flop. Explain the working of an SR latch with a neat diagram.	8	2	L2
1 b)	Explain the functional units of a computer with a block diagram.	8	3	L2
1 c)	Describe the bus structure in computer systems and its role in data transfer.	9	3	L2
	OR			
2 a)	Describe the types of flip-flops and explain the working of a JK flip-flop with a timing diagram.	8	2	L2
2 b)	Discuss the basic performance equation. How does clock rate affect system performance?	8	3	L2
2 c)	Explain the concept of memory locations and addresses. How are instructions sequenced in a program?	9	3	L2
	Part -B			
3 a)	Illustrate different addressing modes with suitable examples.	8	3	L3
3 b)	Describe the process of handling multiple devices using interrupts.	8	4	L2
3 c)	Discuss the trade-offs between speed, size, and cost in memory systems.	9	4	L2
	OR			
4 a)	Explain the role of interrupts in I/O devices. Discuss the hardware needed to handle interrupts.	8	4	L2
4 b)	What is Direct Memory Access (DMA)? Explain the bus arbitration mechanism used in DMA.	8	2	L1
4 c)	Explain the concept of cache memory. Discuss the different mapping functions used in cache design.	9	2	L2

COURSE OUTCOMES (COs)	
1	Apply the K–Map techniques to simplify various Boolean expressions.
2	Design different types of combinational and sequential circuits along with Verilog programs.
3	Describe the fundamentals of machine instructions, addressing modes and Processor performance.
4	Explain the approaches involved in achieving communication between processor and I/O devices.
5	Analyze internal Organization of Memory and Impact of cache/Pipelining on Processor Performance

REVISED BLOOMS TAXONOMY LEARNING LEVEL (RBT)					
L1: Remember	L2: Understand	L3: Apply	L4: Analyze	L5: Evaluate	L6: Create

PROGRAM OUTCOMES (POs)					
1	Engineering Knowledge	5	Modern tool usage	9	Individual and Team-Work
2	Problem Analysis	6	Engineer and Society	10	Communication
3	Design / Development Solutions	7	Environment and Sustainability	11	Project Management and Finance
4	Conduct Investigations of Complex problems	8	Ethics	12	Life-long Learning

CBCS SCHEME

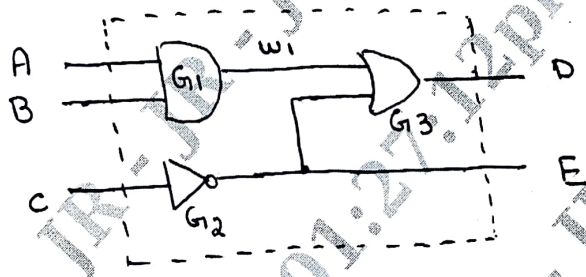
USN | 2 | J | R | 2 | 3 | C | I | 0 | 3 | 2 |

BCS302

Third Semester B.E./B.Tech. Degree Examination, Dec.2024/Jan.2025
Digital Design and Computer Organization

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Determine the complement of the following function: (i) F = xy′+ x′y (ii) F = x′yz′ + x′y′z	06	L3	CO1
	b.	Describe map method for three variables.	04	L2	CO1
	c.	Apply K map technique to simplify the following function: (i) F(x, y, z) = Σ(0, 2, 4, 5, 6) (ii) F(x, y, z) = x′y + yz′ + y′z′	10	L3	CO1
		OR			
Q.2	a.	Apply K map technique to simplify the function : F(w, x, y, z) = Σ(1, 3, 7, 11, 15) and d(w, x, y, z) = Σ(0, 2, 5)	06	L3	CO1
	b.	Determine all the prime implicants for the Boolean function F and also determine which are essential F(w, x, y, z) = Σ(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)	10	L3	CO1
	c.	Develop a verilog gate-level description of the circuit shown in Fig.Q2(c).  Fig.Q2(c)	04	L3	CO1
		Module – 2			
Q.3	a.	Explain the combinational circuit design procedure with code conversion example.	10	L2	CO2
	b.	Design a full adder circuit. Also develop data flow verilog model for full adder.	10	L3	CO2
		OR			
Q.4	a.	Describe 4 × 1 MUX with block diagram and truth table. Also develop a behavioral model verilog code for 4 × 1 MUX.	10	L2	CO2
	b.	What are storage elements? Explain the working of SR and D latch along with logic diagram and function table.	10	L2	CO2
		Module – 3			
Q.5	a.	Explain the basic operational concepts between the processor and memory.	10	L2	CO3
	b.	Describe the following: (i) Processor clock (ii) Basic performance equation (iii) Clock rate (iv) SPEC rating	10	L2	CO3
		OR			
Q.6	a.	Define addressing mode. Explain any four types of addressing mode with example.	10	L2	CO3

	b.	Mention four types of operations to be performed by instructions in a computer. Explain the basic types of instruction formats to carry out. $C \leftarrow [A] + [B]$	10	L2	CO3
		Module – 4			
Q.7	a.	With a neat diagram, explain the concept of accessing I/O devices.	10	L2	CO4
	b.	What is bus arbitration? Explain centralized and distributed arbitration method with a neat diagram.	10	L2	CO4
		OR			
Q.8	a.	With neat sketches, explain various methods for handling multiple interrupts requests raised by multiple devices.	10	L2	CO4
	b.	What is cache memory? Explain any two mapping function of cache memory.	10	L2	CO4
		Module – 5			
Q.9	a.	Draw the single bus architecture and write the control sequence for execution of instruction ADD (R_3), R_1.	10	L3	CO5
	b.	With suitable diagram, explain the concept of register transfer and fetching of word from memory.	10	L2	CO5
		OR			
Q.10	a.	With a neat diagram, explain the flow of 4-stage pipeline operation.	10	L2	CO5
	b.	Explain the role of cache memory and pipeline performance.	10	L2	CO5

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