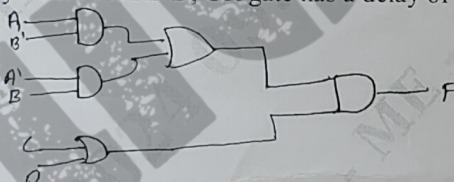


Third Semester B.E./B.Tech. Degree Examination, Dec.2023/Jan.2024  
**Digital Design and Computer Organization**

Time: 3 hrs.

Max. Marks: 100

*Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.  
2. M : Marks , L: Bloom's level , C: Course outcomes.*

Module – 1			M	L	C
Q.1	a.	Obtain a minimum product of sums with a Karnaugh map. $F(w, x, y, z) = x' z' + wyz + w' y' z' + x' y$ .	10	L3	CO1
	b.	Find the minimum sum of products for each function using a Karnaugh map i) $F_1(a, b, c) = M_0 + M_2 + M_5 + M_6$ ii) $F_2(d, e, f) = \sum m(0, 1, 2, 4)$ iii) $F_3(r, s, t) = r t' + r' s' + r' s$	10	L3	CO1
OR					
Q.2	a.	Identify the prime implicants and essential prime implicants of the following functions: i) $f(A, B, C, D) = \sum (1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$ ii) $f(W, X, Y, Z) = \sum(0, 1, 2, 5, 7, 8, 10, 15)$ .	10	L3	CO1
	b.	Write the verilog code for the given expression using dataflow and behavioral model where $Y = (AB' + A'B) (CB + AD) (AB'C + AC)$ .	5	L2	CO1
	c.	Write the verilog code and time diagram for the given circuit with propagation delay where the AND, OR gate has a delay of 30ns and 10ns. 	5	L2	CO1
Module – 2					
Q.3	a.	What is Latch? With neat diagram, explain S-R latch using NOR gate. Derive characteristics equation.	10	L3	CO2
	b.	What is priority encoder? Design 4:2 priority encoder with necessary diagrams.	10	L3	CO2
OR					
Q.4	a.	Design and explain four bit adder with carry look ahead.	10	L3	CO2
	b.	What is multiplexer? Design 9:1 mux using 2:1 mux.	10	L3	CO2

1 of 2



## Module – 3

Q.5	a.	Explain four types of operation performed by computer with an example.	10	L2	CO3
	b.	Show how below expression will be executed in one address, two address zero address and three address processor in an accumulator organization $X = (A * B) + (C * D)$ .	10	L1	CO3

## OR

Q.6	a.	What is addressing mode? Explain different types of addressing mode with an examples.	10	L2	CO3
	b.	With a neat diagram, explain basic operational concepts of a computer.	10	L2	CO3

## Module – 4

Q.7	a.	Explain the following with respect to interrupts with diagram. i) Vector interrupt ii) Interrupt nesting iii) Simultaneous request.	10	L2	CO3
	b.	Explain Direct Memory Access with a neat diagram.	10	L2	CO3

## OR

Q.8	a.	What is Bus arbitration? Explain different types of bus arbitration.	10	L2	CO3
	b.	Discuss different types of mapping functions of caches.	10	L2	CO3

## Module – 5

Q.9	a.	Draw and explain the single-bus organization of the data path inside a processor.	10	L2	CO4
	b.	List out the actions needed to execute the instruction ADD (R3), R1 write and explain the sequence of control steps for the execution of the same.	10	L2	CO4

## OR

Q.10	a.	Analyze how does execution of a complete instruction carry out.	10	L4	CO4
	b.	What is pipeline? Explain the performance of pipeline with an example.	10	L4	CO4

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