Model Question Paper- II with effect from 2022

CBCS SCHEME

Third Semester B.E Degree Examination_____

Digital Design and Computer Organization (BCS302)

TIME: 03 Hours   **Max.Marks:100**

1. Note: *Answer any **FIVE** full questions, choosing at least **ONE** question from each **MODULE***
2. *M: Marks, L: Bloom's level, C: Course outcomes.*

		Module - 1	**M**	**L**	**C**
Q.1	**a**	Demonstrate the working of NAND & XOR gate.	6	L1	CO1
	b	Explain the working of Test Bench in Verilog.	6	L2	CO1
	c	Simplify the following Boolean function into (i) sum-of-products form and (ii) product-of-sums form: $F(A, B, C, D) = \Sigma(0, 6, 8, 13, 14)$ $d(A, B, C, D) = \Sigma(2, 4, 10)$	8	L3	CO1
		OR			
Q.2	**a**	Write a program in Verilog to demonstrate the working of User-Defined primitive table.	6	L3	CO1
	b	Realize F = AB + CD using NAND gate only.	6	L1	CO1
	c	Simplify the following Boolean Expression using kmap: $F(A, B, C, D) = \Sigma(0, 1, 3, 7, 8, 9, 10, 13, 15)$ $F(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 7, 10, 15)$	8	L3	CO1
		Module - 2			
Q.3	**a**	Explain Dataflow Modeling in Verilog with an example program.	6	L2	CO2
	b	Design a Full Adder and Subtractor Circuit.	6	L3	CO2
	c	Design an Octal-to-Binary Encoder.	8	L3	CO2
		OR			
Q.4	**a**	Explain the working of Four-bit adders using 4-Full Adders.	6	L3	CO2
	b	Design a BCD-to-excess-3 code converter.	6	L3	CO2
	c	Demonstrate the working of SR Latch and Edge-Triggered D Flip-Flop.	8	L2	CO2
		Module - 3			
Q.5	**a**	Describe the Big-endian and little-endian address assignment.	5	L2	CO3

	b	Demonstrate the Instruction Execution and Sequencing for C ← [A] + [B] with block diagram.	8	L4	CO3
	c	With a block diagram, explain the basic functional units of a computer.	7	L2	CO3
		OR			

Q.6	a	With relevant example, Explain the following modes of Addressing:
		   i) Direct
		   ii) Register
		   iii) Index
		   iv) Base with index and offset
		   v) Autoincrement
			10	L2	CO3

	b	A program with 7000 machine instructions needs an average of 3 basic steps to execute one instruction. Find the performance of the computer having a clock speed of 700 KHz.	5	L3	CO3
	c	What are Condition Code Flags? Mention the significance of the flags N, Z, V and C.	5	L1	CO3
		Module - 4			
Q.7	a	Describe DMA with its registers and controllers.	10	L2	CO4
	b	Explain the effect of size, cost and speed in Memory Hierarchy.	10	L3	CO4
		OR			
Q.8	a	Explain Hardware Interrupt, enabling/disabling of Interrupts and sequence of events in handling interrupt request from a single device.	10	L2	CO4
	b	Describe the different memory mapping functions.	10	L2	CO4
		Module - 5			
Q.9	a	Describe how an ALU performs an Arithmetic and Logic Operations along with input gating diagrams.	10	L3	CO5
	b	Explain 4-stage pipeline with diagrams.	10	L2	CO5
		OR			
Q.10	a	Explain the complete set of operations involved in executing the instruction Add (R3), R1 along with control sequence.	10	L4	CO5
	b	What are Hazards? Explain Data Hazard, Control Hazard and Structural Hazard.	10	L2	CO5