

Fig: Structure of nMOS.

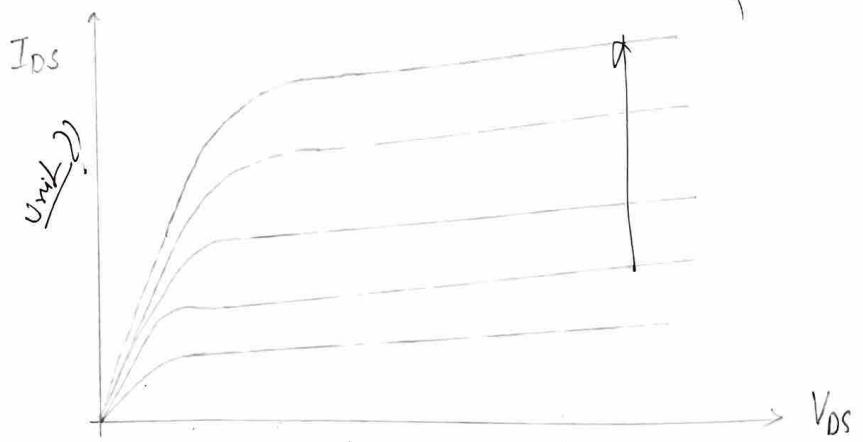


Fig: nmos output characteristics

## # Experiment 1: MOSFET and OP-AMP Characteristics

**Objective :** To study the drain and transfer characteristics and effect of body bias in transistor using LTSpice

**Components & Equipment :** Computer, LTSPICE

**Theory :** An nMOS transistor is a 4 terminal device containing source, drain and a substrate. Two n layers are diffused into a P substrate. And the space between is overlapped by poly silicon. The source is connected to ground and so is the substrate. We increase the gate voltage until  $V_{TH}$  after which a channel is formed below the gate. The channel becomes stronger as we increase  $V_{GS}$  from here and is determined by the overdrive voltage given by  $V_{ov} = V_{GS} - V_{TH}$ . At a constant  $V_{DS}$ , the transconductance characteristics is shown below.

Here, the MOSFET operates in linear region and acts as a resistor. If we increase  $V_{DS}$ , at  $V_{DS} = V_{GS} - V_{TH}$ . The voltage then pinch-off occurs at the drain and the current remains for any further increase in the  $V_{DS}$  voltage.

The output current  $I_{DS}$  is given by the equation:

$$I_{DS} = 0 ; V_{GS} = 0$$

$$I_{DS} = \beta \{ (V_{GS} - V_{TH}) V_{DS} - V_{DS}^2 \} ; V_{DS} < V_{GS} - V_{TH}$$

$$I_{DS} = (\beta/2) (V_{GS} - V_{TH})^2 ; V_{DS} > V_{GS} - V_{TH}$$

## Introduction to LTSPICE tool:

SPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open-source analog electronic simulator. It is a program used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behaviour.

LTSpice is a high-performance SPICE simulator, schematic capture and wave-form viewer with enhancement and models for easing the simulation of switching regulators. The enhancements to SPICE have made simulating switching regulators extremely fast compared to normal SPICE simulators, allowing the user to view waveforms for most switching regulators in just a few minutes.

Included in this download are LTSpice, Macro models for majority of Linear Technology's switching regulators, over 200 op-amp models, as well as resistors, transistors & MOSFET models.

LTSPICE can run simulations on either schematic files or coded netlist files. Both methods are quite similar, and only simulations with schematic files are introduced in detail here.

## OP-AMP Characteristics

It is a 3-terminal device consisting of 2 high impedance input terminals, one called the inverting input denoted by a minus sign  $-$ . The other is non-inverting input. The 3rd terminal is the output.

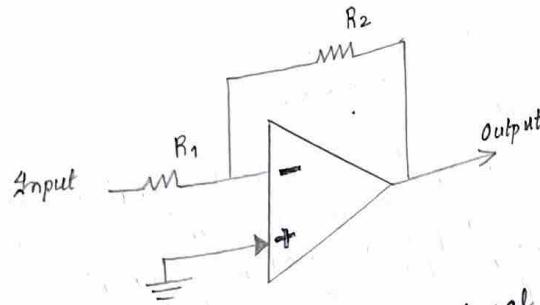


Fig: Inverting Operational Amplifier

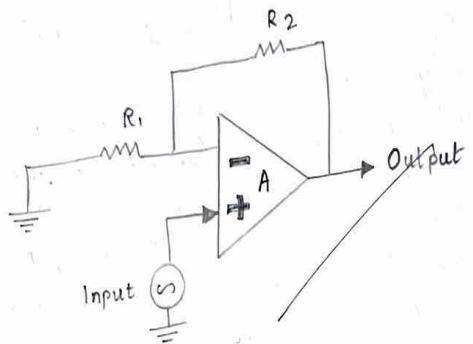


Fig: Non-Inverting Operational Amplifier

Inverting Operational Amplifier:

In the inverting operational amplifier circuit, the signal is applied at the inverting input and the non-inverting input is connected to the ground. In this type of Amplifier, the output is  $180^\circ$  out of phase to the input, i.e. when positive signal is applied to the circuit, the output of the circuit will be negative. By assuming the Op-Amp to be ideal, then the concept of virtual short can be applied at the input terminals of the Op-Amp. So that voltage at the inverting terminal is equal to the voltage at non-inverting terminal.

Non-Inverting operational Amplifier:

When the signal is applied at the non-inverting input, the resulting circuit is known as Non-Inverting Op-Amp. In this Amplifier the output is exactly in phase with the input i.e. when a positive voltage is applied to the circuit, the output will also be positive. By assuming the Op-Amp is ideal, then concept of virtual short can be applied i.e. the voltage at the inverting and non-inverting terminal is equal.

EXERCISE PROBLEMS:

- 1) a)  $I_D$  vs  $V_{GS}$  curve, by keeping  $V_{DS}$  constant. (for PMOS)

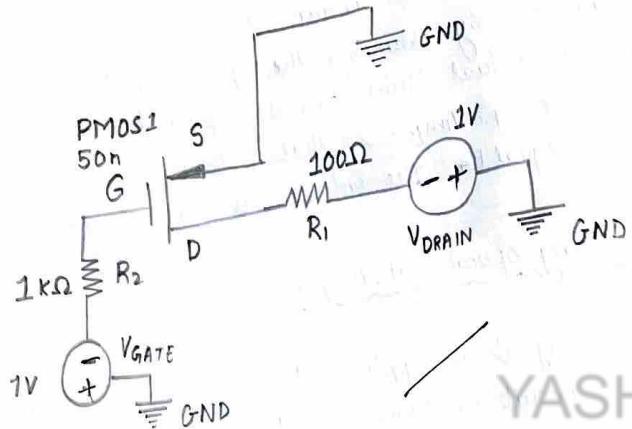
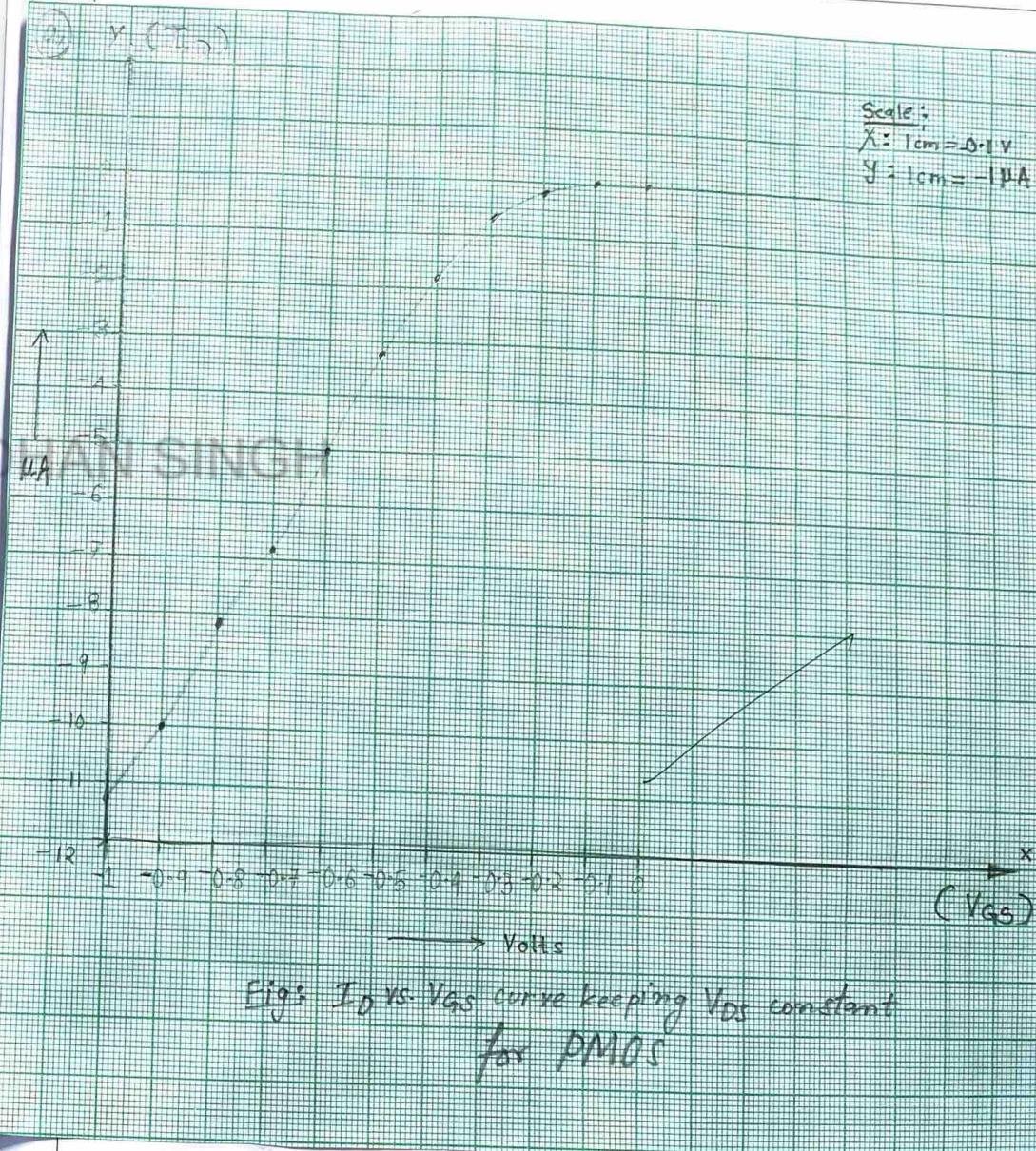


Fig: PMOS Schematic



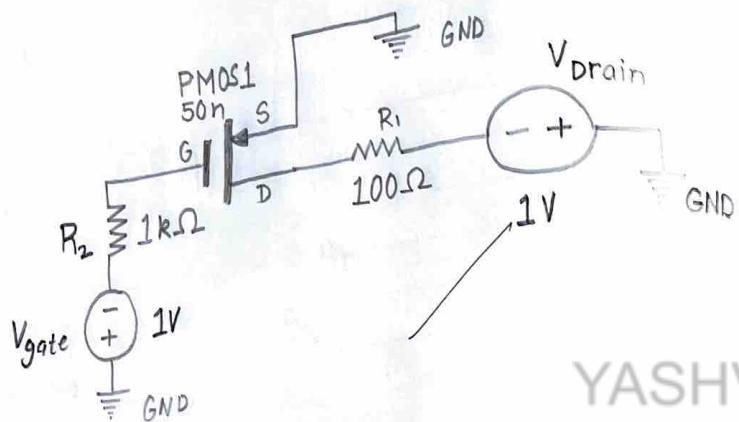
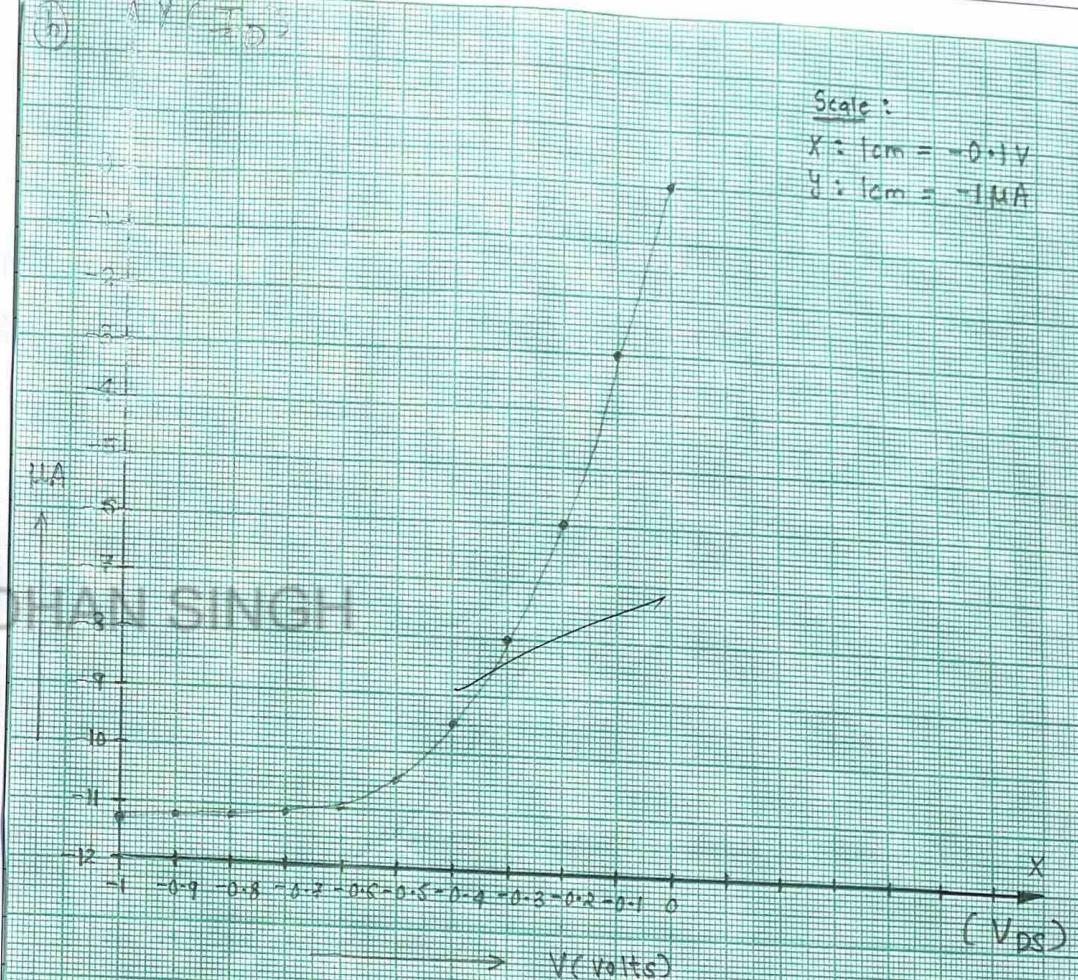


Fig: 1(b) - PMOS Schematic

Q1.B)  $I_D$  vs.  $V_{DS}$  by keeping  $V_{GS}$  constant.(b)  $I_D$  vs.  $V_{DS}$ Fig:  $I_D$  vs.  $V_{DS}$  curve keeping  
 $V_{GS}$  constant  
for PMOS

Q1.C)  $I_D$  vs.  $V_{GS}$  curve, by varying the values of  $V_{DS}$ .

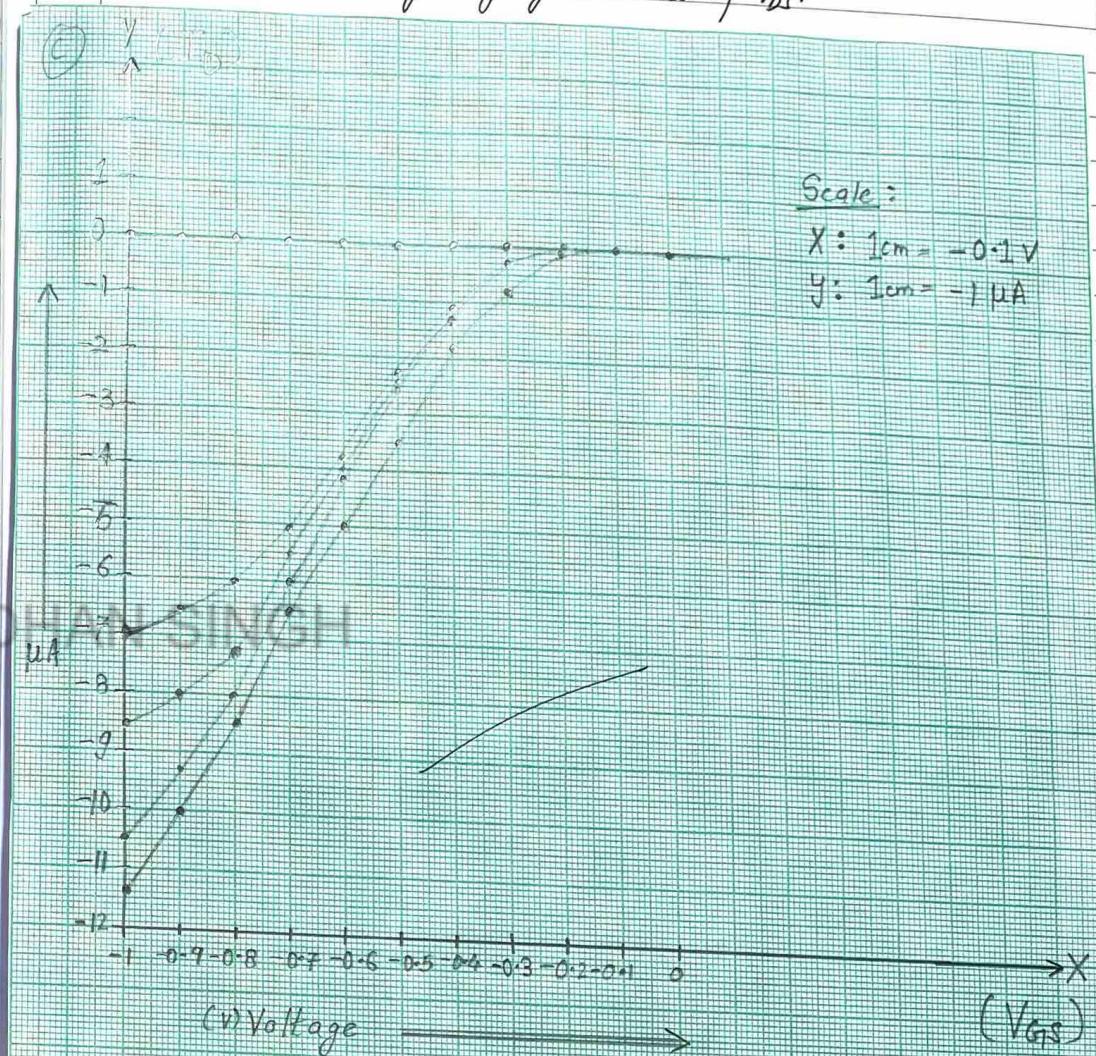
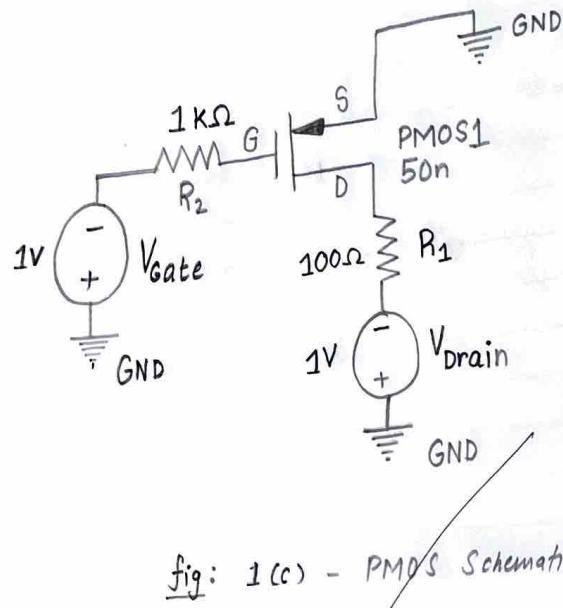


Fig:  $I_D$  vs.  $V_{GS}$  curve  
by varying  $V_{DS}$   
for PMOS

Q1.D)  $I_{DS}$  vs.  $V_{DS}$  curve, by varying the values of  $V_{GS}$

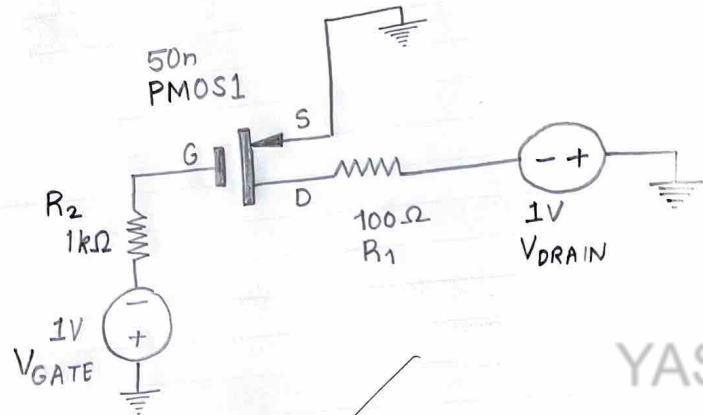
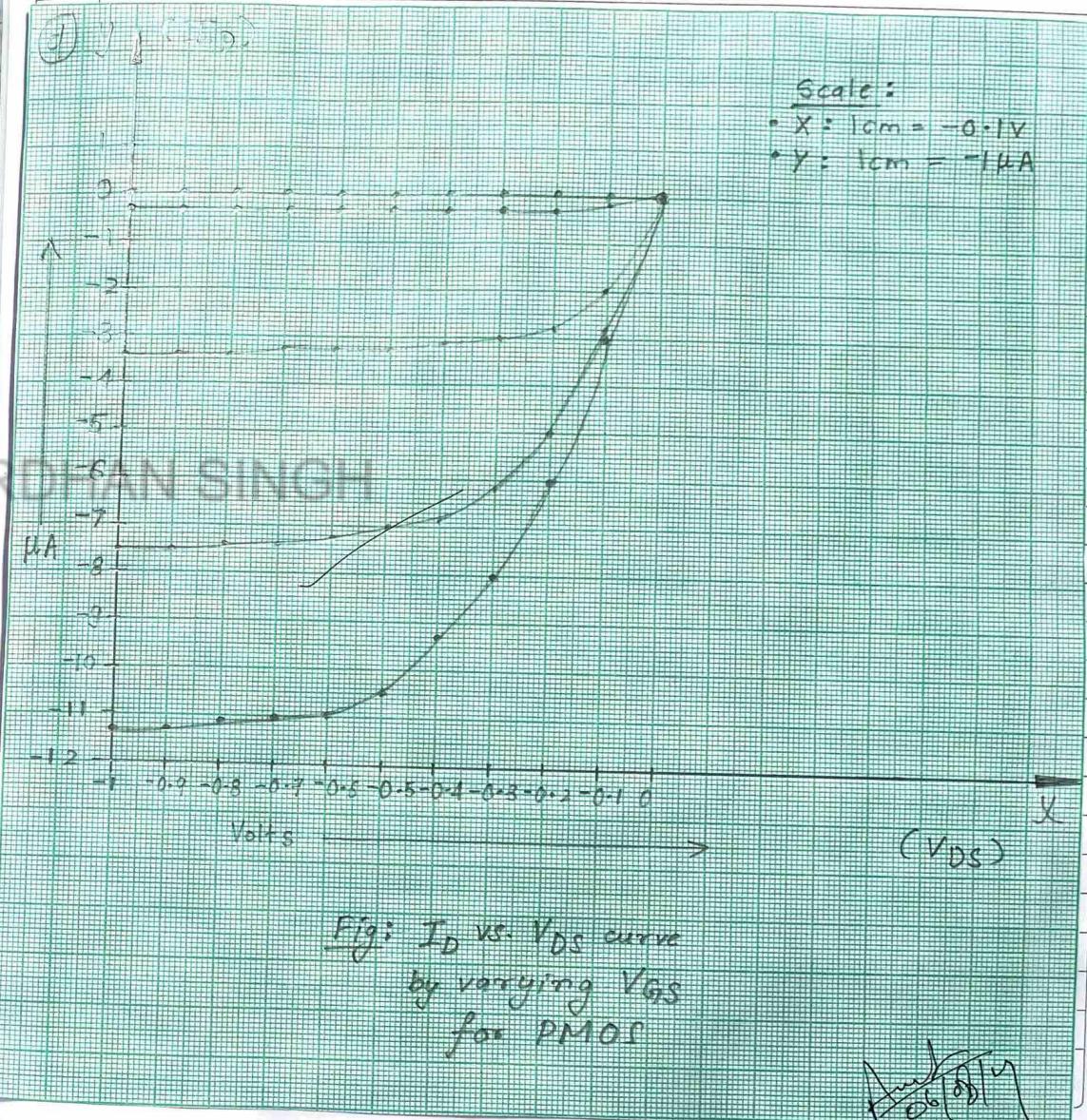


fig: 1(d) - PMOS schematic



## EXPERIMENT 2: MOSFET Amplifiers

### # Objective:

To design common source, common drain, and common gate MOSFET amplifiers and analyze the performance using LTSpice.

### # Components & Equipment:

Computer, LT Spice software

### # Theory:

#### → COMMON SOURCE AMPLIFIER:

It uses the gate as its input terminal and the drain as its output. The source terminal is common to both the input and output in terms of the AC signals, hence the name common-source.

It is designed for providing very high input impedance.

An ideal CS amplifier has infinite input impedance (draws no current at DC) and a moderately high output resistance (easier to match for maximum power transfer) and a high voltage gain (a desirable property).

#### → COMMON DRAIN AMPLIFIER:

The input is applied between the gate and drain terminals, while the output is measured between the source and drain terminal. Since the drain terminal is common between the input and output side, it is known as common Drain amplifier. Since the output at the source terminal is following the input signals, it is also known as Source Follower.

It is a unit gain amplifier with a very large input impedance but a smaller output impedance.

Therefore, it is good for matching a high impedance circuit to a low-impedance circuit or to a circuit that needs a larger supply of current.

→ COMMON GATE AMPLIFIER:

Here, input is applied between source and gate and output is taken between drain and gate. Gate potential is at constant potential. So, increase in input voltage in positive direction cause increase in the negative gate source voltage.

The reduction in drain current results in an increase in output voltage. As the input impedance is low, it is good for matching sources with a low input impedance due to the maximum power theorem, but it draws more current, implying high power consumption from the signal source.

YASHVARDHAN SINGH

Please Turn Over For Exercise  
Questions →

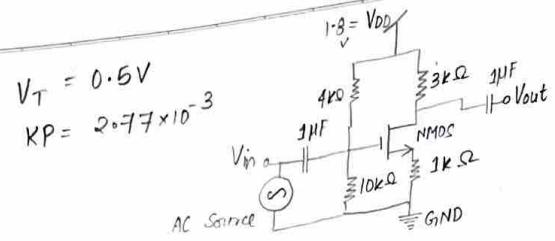
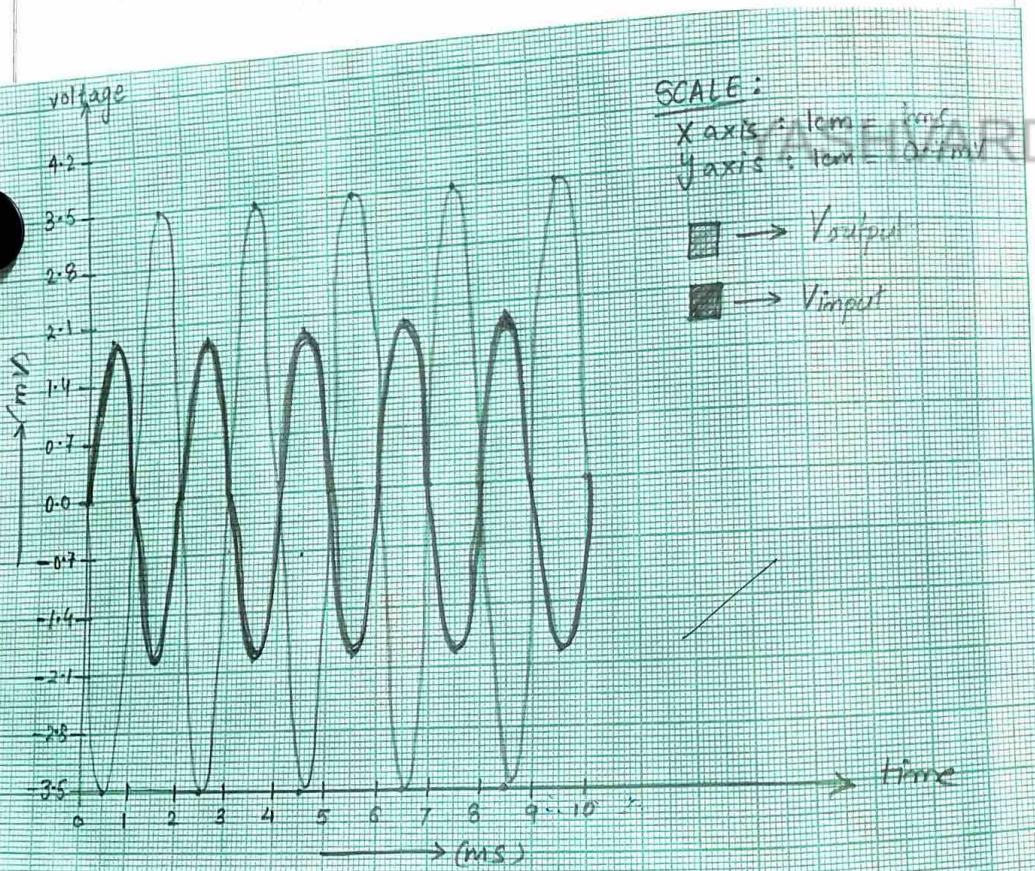


Fig: Circuit for Q1.

# corresponding circuit for Question 1

# Corresponding V-T curve for Question 1 :



## # EXP. 2 : EXERCISE PROBLEMS

Q1) Determine the gain of the circuit diagram in Fig 2.1, if the capacitor  $C_1$  is removed.

Q2) Determine the gain of the circuit diagram in Fig 2.1, if  $C_1 = 100 \mu F$  and  $\lambda = 0.1 V^{-1}$ .

⇒ Figure 2.1:

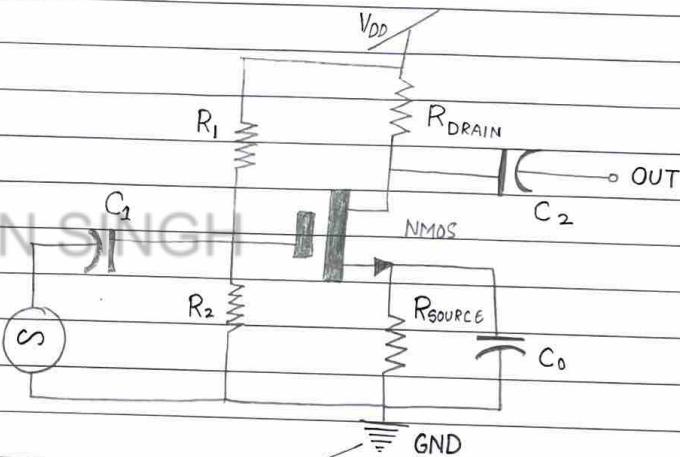


Fig: CS Amplifier

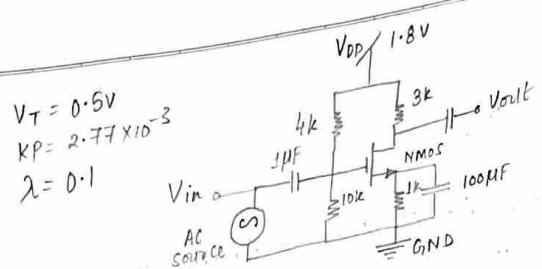
### # Relevant Calculations for Exercise Questions:

Q1) when capacitor  $C_1$  removed

$$\frac{1}{2} M_n C_{ox} \frac{W}{L} = 1.388 \times 10^{-3} \leftarrow \text{value of constants}$$

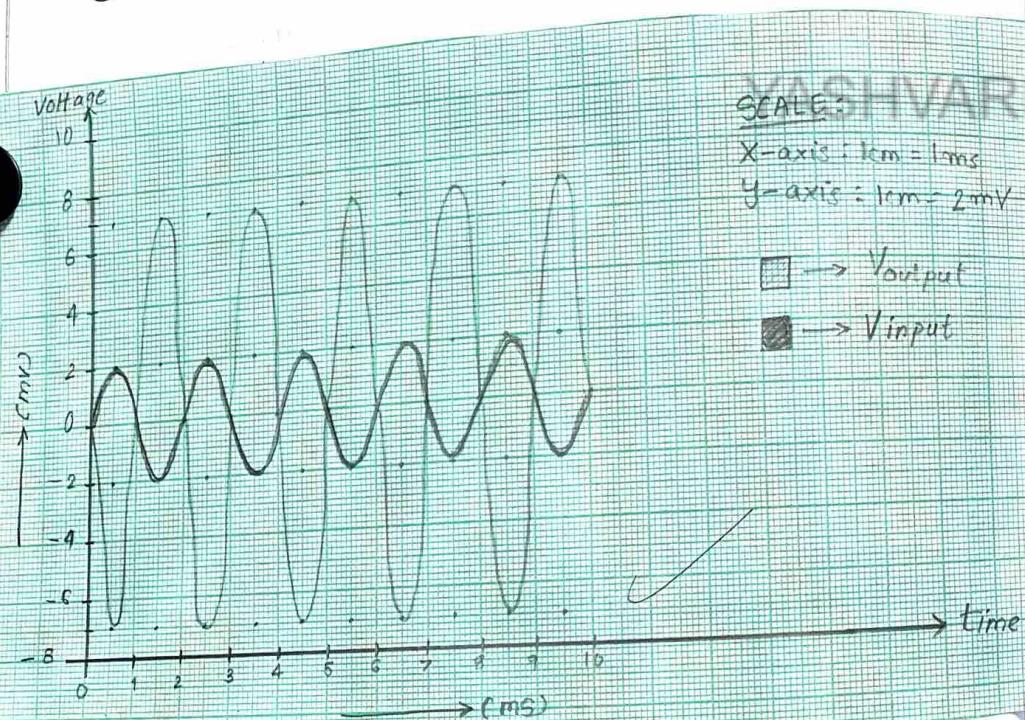
$$V_G = \frac{1.8 \times 10}{10 + 4} = \frac{18}{14} = 1.28V$$

$$I_D = 1.388 \times (V_{GS} - V_{TH})^2 \rightarrow ①$$

Fig: circuit for  
Q2:

# Corresponding circuit for Q2

# Corresponding V-T curve for Question - 2:



g1]  $V_{GS} = V_G - V_S$

contd:  $V_G = 1.28V$  and  $V_S = I_D R_S \rightarrow R_S = 1k\Omega$   
 $\therefore V_{GS} = 1.28 - I_D(1000) \rightarrow (2)$

Substituting (1) in (2):

$$V_{GS} = 1.28 - 1.388 \{ V_{GS}^2 + 0.25 - V_{GS} \}$$

$$V_{GS} = 0.971V$$

$$I_D = 1.388 \times (0.971 - 0.5)^2 = 0.03 \mu A$$

∴  $V_{Gate-Source} = 0.971V$

$I_{Drain} = 0.03 \mu A$

⇒ Transconductance  $\Rightarrow g_m = \mu_m C_{ox} W (V_{GS} - V_{TH})$

$$g_m = 1.308 \times 10^{-3}$$

⇒ Voltage gain :

$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$

$$= - \frac{(1.308 \times 10^{-3} \times 3 \times 10^3)}{(1 + 1.308 \times 10^{-3} \times 10^3)} = -1.700173$$

∴  $A_V = -1.7001$

Q2]  $\lambda = 0.1 \leftarrow$  given

$$V_{DS} = V_D - V_S = 1.8V - I_{DSCLM}(1000)$$

$$I_{PSCLM} = \frac{1}{2} \mu_m C_{ox} W (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

$$V_{GS} = V_G - V_S = 1.28 \leftarrow I_{DSCLM}(1000)$$

$$I_{DS} = 1.388 \times 10^{-3} (0.78 - I_{DSCLM} \times 10^3)^2 (1 + 0.18 \times 100 I_{DS}) \\ = (1.6042 \times 10^{-3} - 0.139 I_D) (0.68084 - 1560 I_D + 10^6 I_{DS}^2)$$

∴  $I_D = 3.1881 \times 10^{-4} A$

Expt. No. 2

$$Q_2] V_{GS} = 0.9612 \text{ V}$$

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})$$

$$\text{Voltage gain} = A_v = -g_m R_D$$

$$g_m = 2.776 \times 10^{-3} (0.9612 - 0.5)$$

$$g_m = 1.28 \times 10^{-3}$$

$$\therefore A_v = -1.28 \times 10^{-3} \times 3 \times 10^3$$

$$A_v = -3.84$$

## # Conclusion :

① The voltage gain ( $A_v$ ) for the Fig 2.1 when  $C_1$  removed is : -1.7

② The voltage gain ( $A_v$ ) for the Fig 2.1 when  $C_1 = 100 \text{ pF}$  and  $\lambda$  is non-zero, i.e.  $\lambda = 0.1 \text{ V}^{-1}$  is : -3.84.

This case will experience Channel length modulation effect.

(END)

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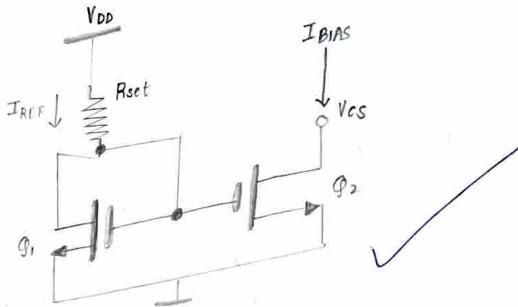


Fig: Current Mirror circuit

EXPERIMENT 3 : MOSFET Current Mirror

## # Objective:

To design basic current mirror (with resistive load, nmos load and pmos load) and analyze the performance using LTSpice.

## # Components &amp; Equipment:

Computer, LTSpice Software

## # Theory:

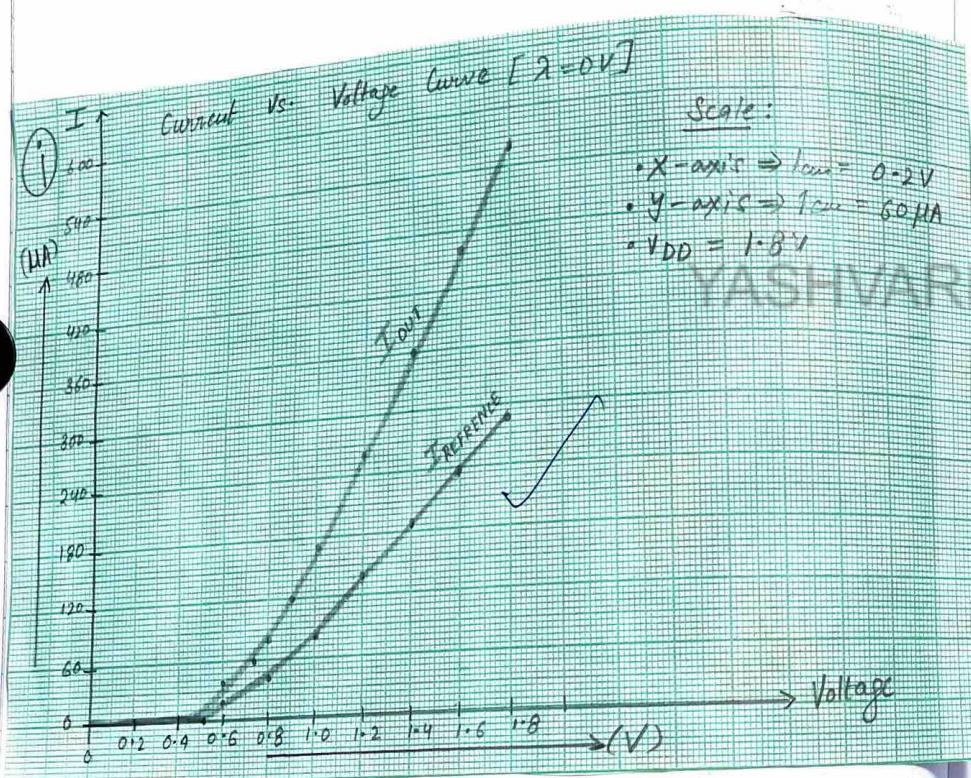
Current mirror is an analog circuit that senses the reference current and generates the copy or number of copies of the reference current, with the same characteristics. The replicated current is as stable as the reference current source. The replicated current could be the same as the reference current, or it could be either multiple or fraction of the reference current.

Current mirrors are particularly useful in the integrated circuit, for biasing the amplifiers. The advantage of biasing the amplifiers with the current source is that it provides a high voltage gain and good biasing ability.

## # Observations - from Exercise Problems

<u>I</u>	<u>V<sub>DD</sub></u>	<u>I<sub>REF</sub></u>	<u>I<sub>OUT</sub></u>	<u>THEORY <math>I_{D2}/I_{D1}</math></u>	<u>LTSPICE <math>I_{D2}/I_{D1}</math></u>
0	2V	$3.77 \times 10^{-4}$	$1.885 \times 10^{-3}$	4.99964	4.99964
0	3V	$6.69 \times 10^{-4}$	$3.334 \times 10^{-3}$	4.99964	4.9964
0	4V	$9.697 \times 10^{-4}$	$4.84 \times 10^{-3}$	4.99964	4.99964
0.01	2V	$3.776 \times 10^{-4}$	$1.909 \times 10^{-3}$	5.0609	5.05579
0.01	3V	$6.703 \times 10^{-4}$	$3.418 \times 10^{-3}$	5.1061	5.09921
0.01	4V	$9.706 \times 10^{-4}$	$4.992 \times 10^{-3}$	5.1521	5.14367

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## # EXERCISE - PROBLEMS :

Q1. Repeat the circuit in Figure 3.1 when :

- $\lambda = 0$
- $\lambda = 0.01 \text{ V}^{-1}$

and,

$$\rightarrow \mu n C_{ox} = 100 \mu A/V^2$$

$$\rightarrow (W/L)_1 = 10/0.18$$

$$\rightarrow V_T = 0.6V$$

$$\rightarrow (W/L)_2 = 50/0.18$$

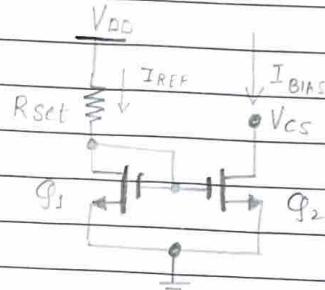


Figure 3.1

## # CALCULATIONS — FOR THEORY VALUE :

Q1) i)  $\lambda = 0 \rightarrow$  no channel length modulation

$\Rightarrow K_{N1} \rightarrow$  for mosfet  $Q_1$ :

$$K_{N1} = \mu n C_{ox} \left( \frac{W}{L} \right)_1 = \frac{100 \times 10^{-6}}{0.18} \times 10 = 5.556 \times 10^{-3}$$

$$K_{N2} = \mu n C_{ox} \left( \frac{W}{L} \right)_2 = \frac{100 \times 10^{-6}}{0.18} \times 50 = 27.778 \times 10^{-3}$$

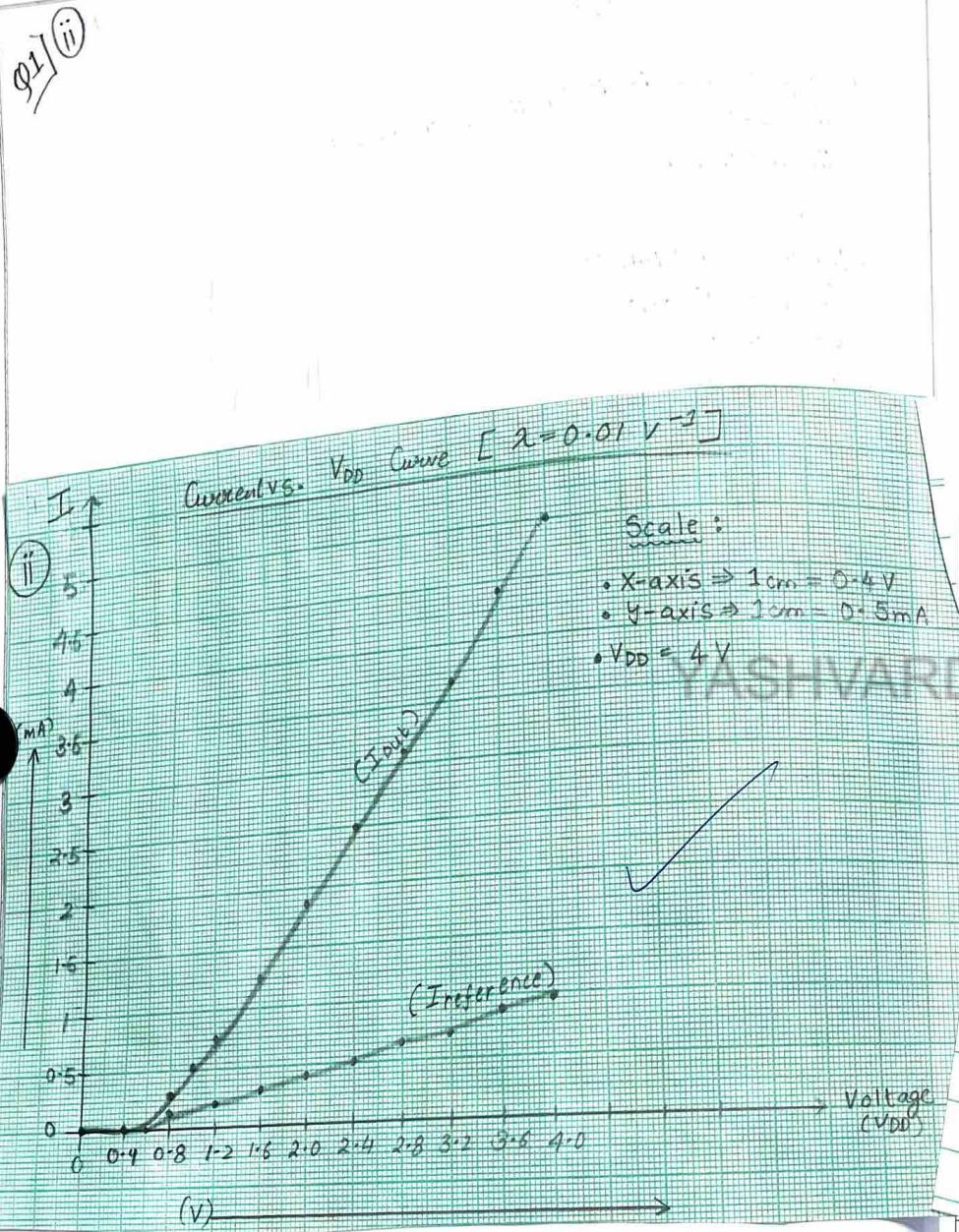
$\Rightarrow$  Theoretical Ratio:

$$\frac{I_{D2}}{I_{D1}} = \frac{\frac{K_{N2}}{2} (V_{GS2} - 0.5)^2}{\frac{K_{N1}}{2} (V_{GS1} - 0.5)^2} \rightarrow ①$$

$$\frac{I_{D2}}{I_{D1}} = \frac{27.778 \times 10^{-3}}{2} [V_{GS2} - 0.5]^2 \rightarrow ①$$

$$\frac{5.556 \times 10^{-3}}{2} [V_{GS1} - 0.5]^2$$

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$\Rightarrow$  Gate Voltage Calculations:

$$V_{GS1} = V_{GS2}, \text{ assuming } V_{DD} = 2 \text{ V}$$

$$= K_n (V_{GS} - V_{TH})^2 = \frac{(V_{DD} - V_{GS})}{R_D}$$

$$= 5.556 \times 10^{-3} [V_{GS} - 0.5]^2 = 2 - V_{GS} / 3000$$

$$= 16.668 V_{GS}^2 + 4.167 - 16.668 V_{GS} = 2 - V_{GS}$$

$$= 16.668 V_{GS}^2 + 2.167 - 15.668 V_{GS} = 0$$

$\hookrightarrow$  solving quadratic equation, we get:

$$V_{GS} = 0.771 \text{ V} \quad \text{and} \quad V_{GS} = 0.1685 \text{ V}$$

$$\therefore V_{GS} = 0.771 \text{ V}$$

invalid as  $V_{GS} \neq V_{TH}$

$\Rightarrow$  plug these values of the gate voltage in equation (1):

$$\frac{I_{D2}}{I_{D1}} = \frac{27.778 (0.771 - 0.5)^2}{5.556 (0.771 - 0.5)^2} = \frac{27.778}{5.556} = 4.99964$$

$$\therefore \text{Theoretical Value} = 4.99964$$

$\Rightarrow$  as this equation is independent of  $V_{DD}$  variable, the ratio theoretically will be the same for varying  $V_{DD}$  values.

(Q1) (ii)  $\lambda = 0.01 \text{ V}^{-1} \rightarrow$  channel length modulation occurs  
the equation will now become:

$$\frac{I_{D2}}{I_{D1}} = \frac{(W/L)_2}{(W/L)_1} \times \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})}$$

Expt. No. 3

here,

$$V_{DS2} = V_{DD}$$

$$V_{DS1} = V_{GS}$$

$$\lambda = 0.01 \text{ V}^{-1}$$

→ plug in the values:

$$\begin{aligned} \frac{I_{D2}}{I_{D1}} &= \frac{(50/0.18) \times (1 + (0.01) V_{DS2})}{(10/0.18) \times (1 + (0.01) V_{DS1})} \\ &= \frac{5 + 0.05 V_{DS2}}{1 + 0.01 V_{DS1}} \end{aligned}$$

①  $V_{DD} = 2V \rightarrow \text{case } ①$

$$\therefore V_{DS2} = 2V$$

to determine  $V_{GS}$ :

$$K_n (V_{GS} - V_{TH})^2 = (V_{DD} - V_{GS}) / R_D$$

$$\begin{aligned} \curvearrowleft 16.668 V_{GS}^2 + 4.167 - 15.668 V_{GS} &= V_{DD} \xrightarrow{2V} \textcircled{2} \\ = 16.668 V_{GS}^2 + 2.167 - 15.668 V_{GS} &= 0 \end{aligned}$$

$$V_{GS} \Rightarrow 0.7714V$$

$$\left[ \frac{I_{D2}}{I_{D1}} \right]_{\text{case 1}} = \frac{5 + 0.05 (2)}{1 + 0.01 (0.7714)} = \boxed{\underline{\underline{5.0609}}}$$

②  $V_{DD} = 3V \rightarrow \text{case } ②$

$$= 16.668 V_{GS}^2 + 4.167 + (-15.668 V_{GS}) = 3V$$

$$= 16.668 V_{GS}^2 + 1.167 - 15.668 V_{GS} = 0 \rightarrow V_{GS} = V_{DS1} = 0.858V$$

$$\left[ \frac{I_{D2}}{I_{D1}} \right]_{\text{case 2}} = \frac{5 + 0.05 (3)}{1 + 0.01 (0.858)} = \boxed{\underline{\underline{5.1061}}}$$

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Expt. No. 3

$$V_{DD} = 4V \rightarrow \text{case (3)}$$

$$\therefore 16 \cdot 668 V_{GS}^2 + 0 \cdot 167 - 15 \cdot 668 V_{GS} = 0$$

$$\Rightarrow V_{GS} = 0.9292 V$$

$$\left[ \frac{I_{D2}}{I_{D1}} \right]_{\text{case 3}} = \frac{5 + 0.05(4)}{1 + 0.01(0.9292)} = \boxed{5:15.21}$$

## # Conclusion :

1)  $\lambda = 0$

the  $I_{D2}/I_{D1}$  current ratio for simulation and theoretical values is the same, i.e. = 4.99964.

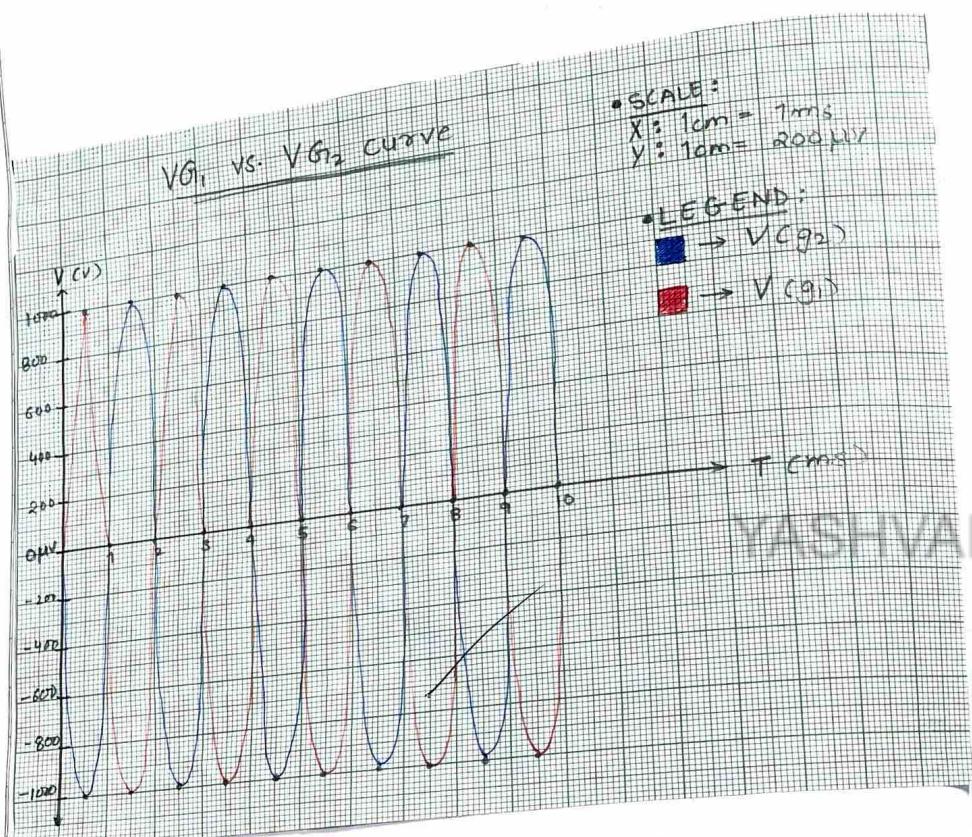
2)  $\lambda = 0.01 V^{-1}$

the  $I_{D2}/I_{D1}$  current ratio for simulation and theoretical values is similar, i.e.  $\approx 5.06, 5.10, 5.15$  for 2V, 3V, 4V in theory and 5.05, 5.09, 5.14 for 2V, 3V, 4V in LTSpice Simulation.

(END)

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Graph 4.1: V<sub>G1</sub> vs V<sub>G2</sub> Curve

### EXPERIMENT 4: MOSFET Differential Amplifier

#### # Objective :

To design a MOSFET differential amplifier with resistive load and analyze performance using LTSpice.

#### # Component & Equipment :

Computer, LTSpice software

#### # Theory :

Differential amplifiers provide a high input impedance for the input terminals. A properly designed differential amplifier with its current-mirror biasing stages is made from matched-pair devices to minimize imbalances from one side of the differential amplifier to the other. 2 active devices are connected to a positive voltage supply via passive series elements. The transistors must be a matched pair (i.e. two matched MOSFETs). The "pull up" loads are similarly matched to each other. The lower terminals of the active devices are connected together, and a dc current source pulls current down toward the negative voltage bus to effect the bias. The controlling input ports of the devices are connected to input signals.

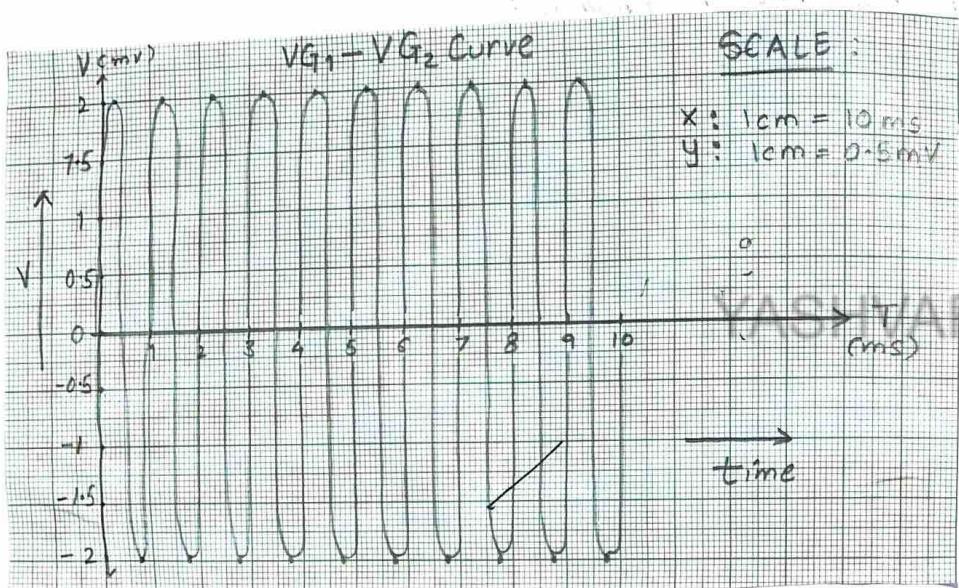
Differential amplifiers apply gain not to one input signal but to the difference between two input signals. This means that a differential amplifier naturally eliminates noise or interference that is present in both input signals.

Differential amplification also suppresses common-mode signals, i.e., a DC offset that is present in both input signals will be removed,

and the gain will be applied only to the signal of interest, eliminating the need for bulky DC-blocking capacitors. The subtraction occurs in a differential pair makes it easy to incorporate the circuit into negative feedback amplifier.

### # Exercise Problems :

- Q. Repeat the circuit in Fig 4.1 with  $V_{TH} = 0.5V$ ,  $\mu nCox = 100 \mu A V^{-2}$   $w_L = 869$  and  $g = 0.01 V^{-1}$ .



Graph (Fig) 4.2: Input Voltage

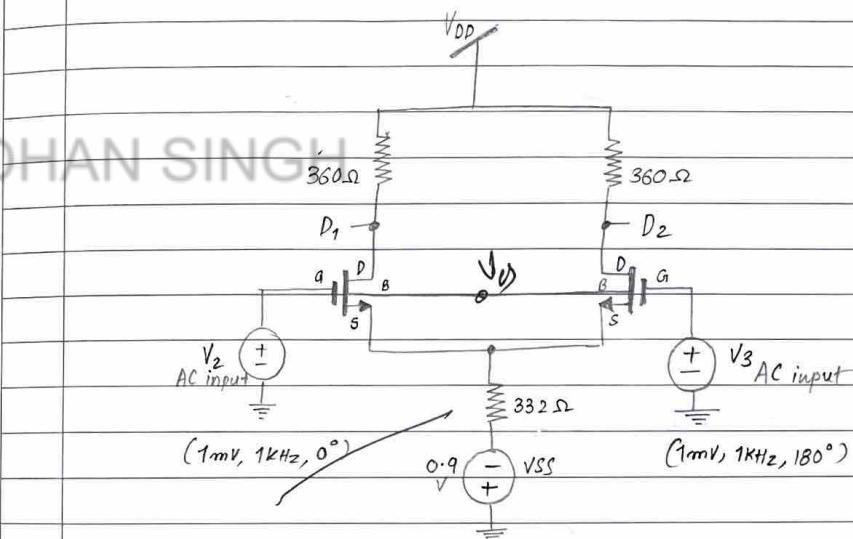
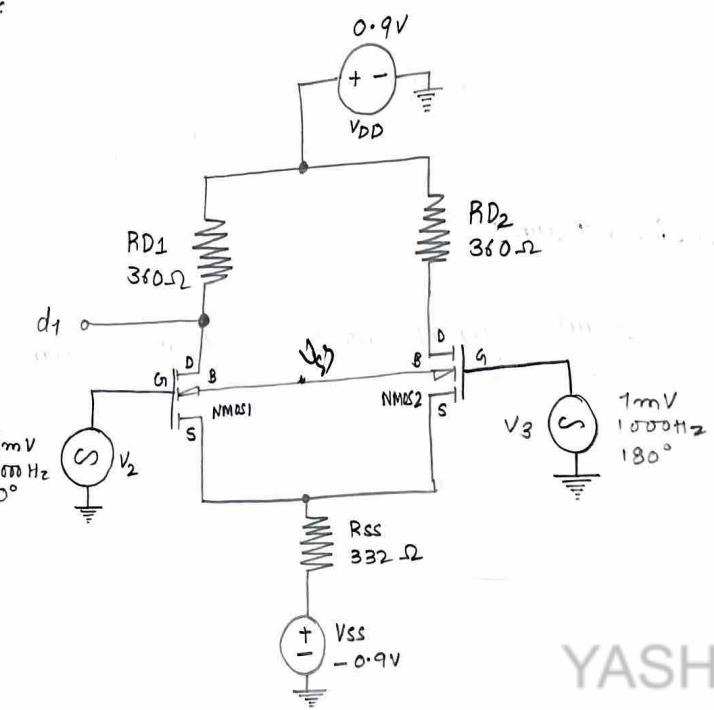


Figure 4.1

fig: differential amplifier

- $V_T = 0.5$  Volts
- $(\frac{W}{L}) \mu n C_{ox} = 0.9869$
- $\lambda = 0.01 V^{-1}$

→ Answer to Exercise Problem: { THEORETICAL }

$$K_n = \frac{1}{2} \mu n C_{ox} \frac{W}{L} = 0.04345$$

$$I_D = 0.04345 (V_{GS} - 0.5)^2 (1 + 0.01 V_{DS}) \rightarrow ①$$

$$V_{GDS} = 0.9 - 66.4 I_D \rightarrow ②$$

$$\begin{aligned} V_{DS} &= V_D - V_S \\ &= (V_{DD} - I_D R_D) - (V_{SS} + 2 I_D R_S) \end{aligned}$$

$$= 1.8 - I_D (R_D + 2 R_S)$$

$$= 1.8 - 1024 I_D \rightarrow ③$$

Substitute eq<sup>n</sup> ② and ③ in equation ①.

# equation ①:

$$I_D = 0.04345 (V_{GS} - 0.5)^2 (1 + 0.01 V_{DS})$$

# equation ②:

$$V_{GDS} = 0.9 - 66.4 I_D$$

# equation ③:

$$V_{DS} = 1.8 - 1024 I_D$$

$$\bullet I_D = 0.00045 A = 4.5 \times 10^{-4} \text{ Amperes}$$

$$\bullet V_D = 1.3392 \text{ Volts}$$

$$\bullet V_{GDS} = 0.6012 \text{ Volts} = 6.012 \times 10^{-2} \text{ V}$$

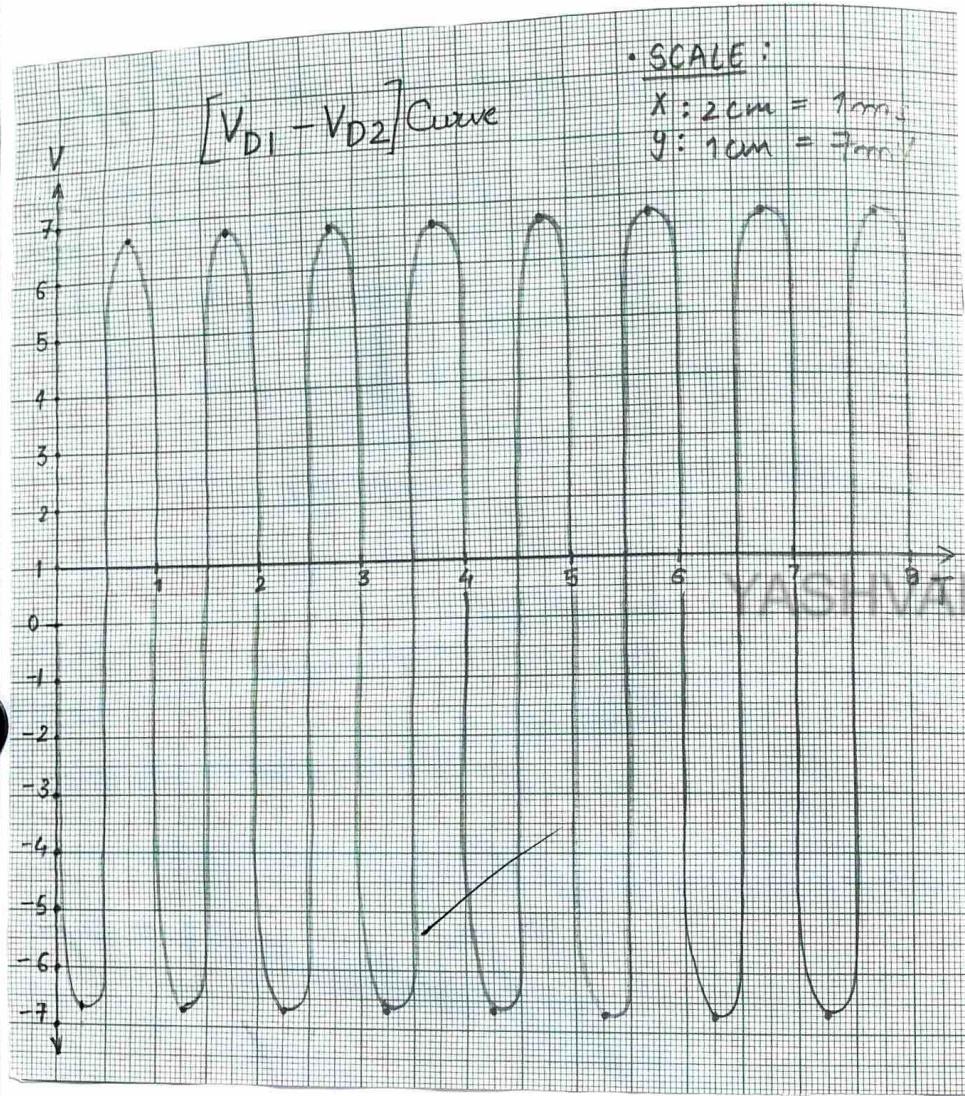
$$\bullet g_m = 2 K_n (V_{GDS} - V_{TH}) (1 + \lambda V_{DS})$$

$$= 0.00891$$

$$= 8.91 \times 10^{-3}$$

$$\bullet A_v = \text{Voltage Gain} = g_m (r_o \parallel R_D)$$

$$= \underline{\underline{3.202}}$$



Graph 4.3 : Output Voltage

# Simulation results for Exercise problems :

$$\textcircled{1} \quad I_D = 4.5 \times 10^{-4} \text{ Amps}$$

$$\textcircled{2} \quad r_0 = \frac{1}{2I_{DS}} = \frac{1}{0.01 \times 4.5 \times 10^{-4}} = \underline{\underline{222.22 \text{ k}\Omega}}$$

$$\textcircled{3} \quad V_{DS} = 1.34 \text{ V}$$

$$\textcircled{4} \quad V_{GS} = 6.01 \times 10^{-1} \text{ Volts}$$

$$\textcircled{5} \quad g_m = 8.9 \times 10^{-3}$$

$$\textcircled{6} \quad \text{Voltage Gain} \Rightarrow A_v = g_m \{ r_0 || R_D \} = 3.1988$$

graphically :  $\frac{V_{out \text{ P2P}}}{V_{in \text{ P2P}}} = \frac{6.5 \times 2}{2 \times 2} \approx \underline{\underline{3.25}}$

# Conclusion :

→ The theoretical and simulation results are same to a great extent and thus, which helps us aptly analyse the differential amplifier.

END

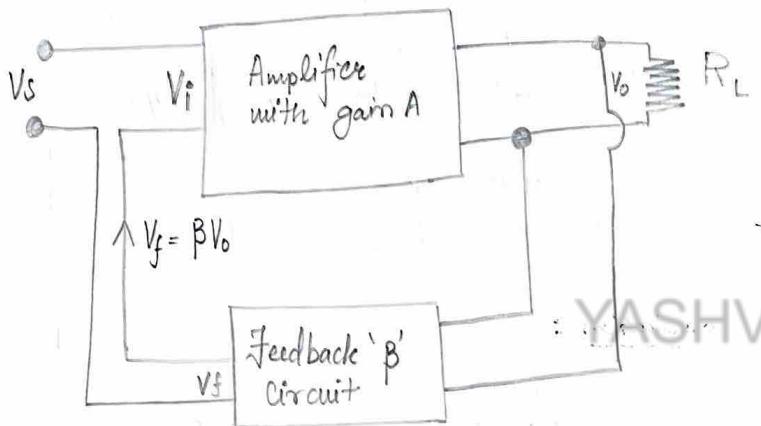


Fig 5.1 : Block diagram of Voltage Series feedback amplifier

### EXPERIMENT 5: MOSFET Feedback Amplifier

#### # Objective:

To design MOSFET feedback amplifier and analyze the performance using LT Spice.

#### # Components & Equipment :

Computer, LTSpice Software

#### # Theory :

The concept of feeding the output signal back to its input circuit is known as feedback and hence the name feedback amplifier. It is dependent between the output and input with effective control. Figure 5.1 (on the left blank page) shows voltage series feedback amplifiers, where feedback circuit is connected in shunt with the output in shunt with the output but in series with respect to the input signal.

Feedback Amplifiers are divided into two types: positive and negative feedback. In the positive feedback amplifier, the input voltage or the current is in phase with the input signals. Both the input signal and feedback introduce a phase shift of  $180^\circ$  and makes a  $360^\circ$  resultant phase shift to be in phase with the input signal. It increases the gain of the amplifier but also increases distortion / instability. Normally, positive feedback is not used for amplifiers. For example, the feedback is used to provide hysteresis for oscillators and comparators.

When any increase in the output signal results into the way to cause the decrease in the output

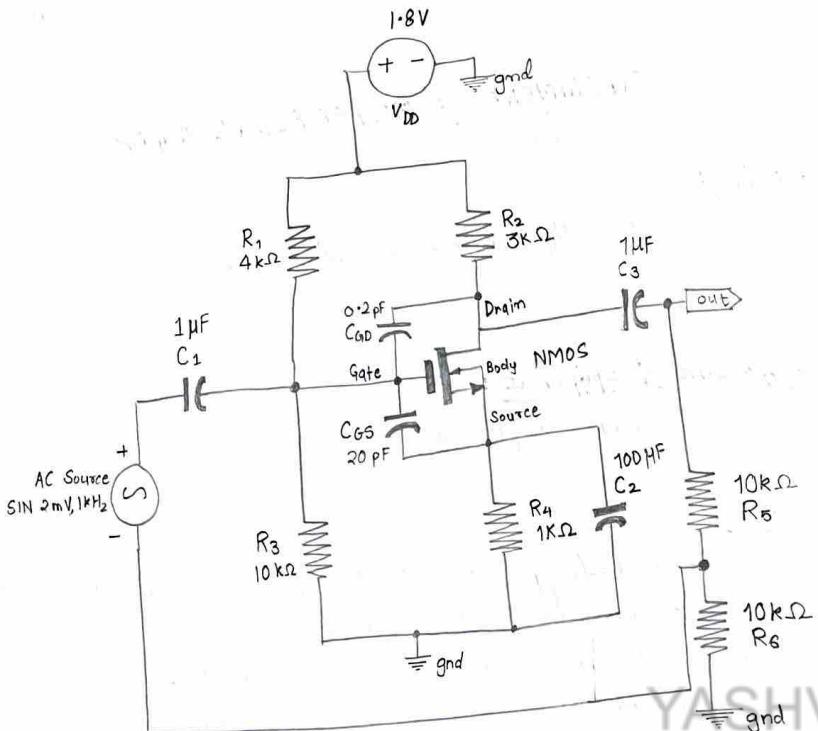


Fig 5.1: CS Amplifier with Feedback

- C<sub>GD</sub>, C<sub>GS</sub> → internal capacitances of the MOSFET. needed to obtain high frequency response of the amplifier.

- B calculations →  $B = \frac{R_6}{R_5 + R_6} = \frac{10k}{20k} = 0.5$

$$\boxed{B=0.5}$$

Signal, the amplifier is said to have negative feedback. The advantages of providing negative feedback are that the transfer gain of the amplifier with feedback can be stabilized against variations in the hybrid parameters of the transistor or the parameters of the other active devices used in the circuit. The most advantage of the negative feedback is that there is significant improvement in the frequency response and in the linearity of the operation of the amplifier. In the voltage - series feedback, the input impedance of the amplifier is increased and the output impedance is decreased. Noise and distortions are reduced considerably.

#### # Exercise Problems :

- g. Design a common source feedback amplifier and analyze its transient and frequency response using LT Spice. Use CS Amplifier from experiment 2 and example 1 as the base amplifier.

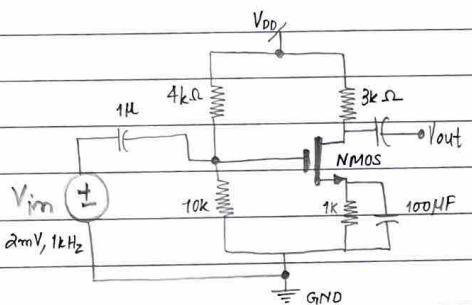
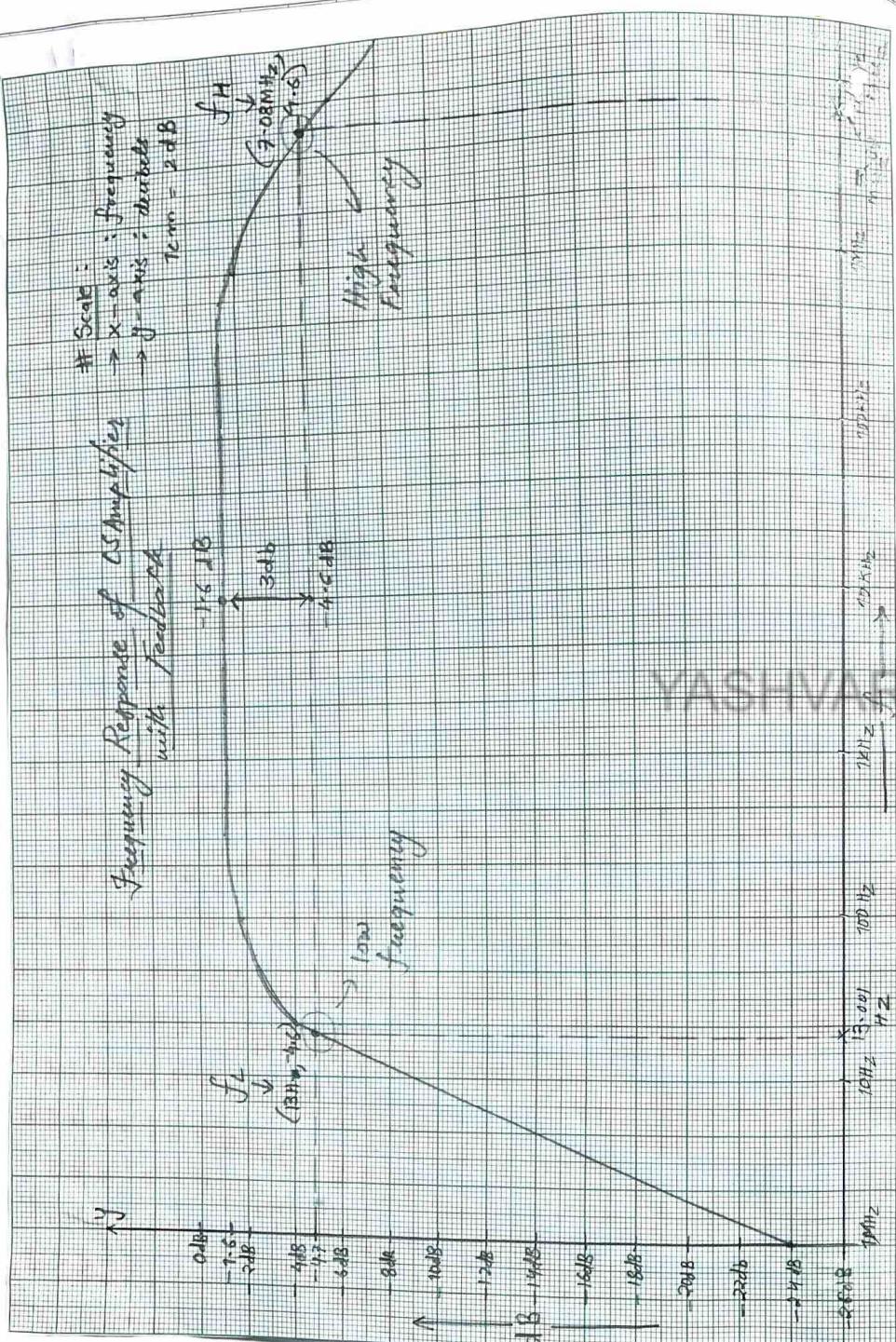


Fig 12.1  
Common Source Amplifier (Nmos)

Expt. No. 5



## # Observations :

→ From observing transient analysis, we know that the gain after adding feedback to the CS Amplifier is -1.66.

## → Bandwidth Calculations:

: From frequency plot:

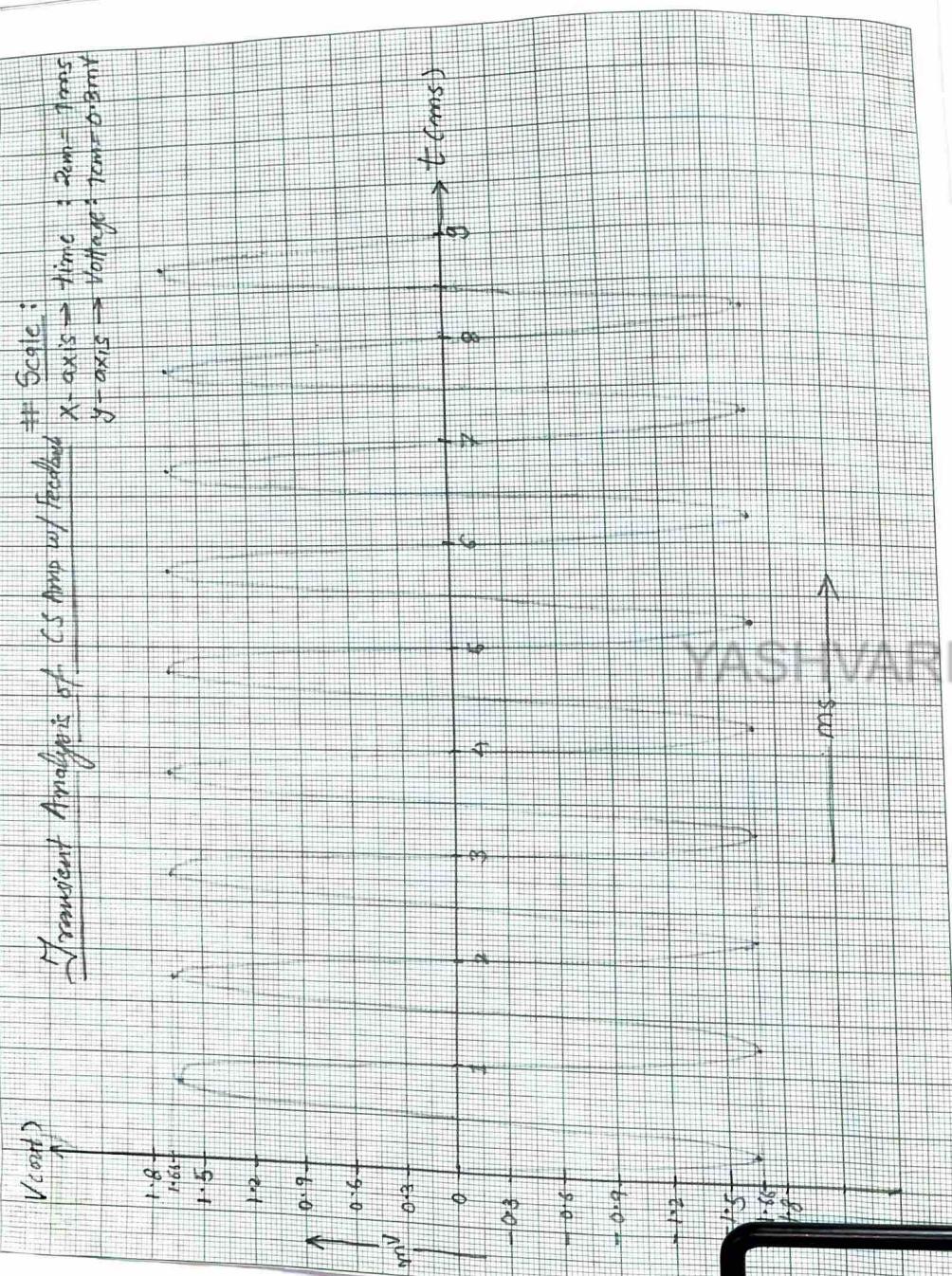
$$-1.6 \text{ dB} - 3 \text{ dB} = -4.6 \text{ dB}$$

$$f_L @ -4.6 \text{ dB} = 13.001 \text{ Hz}$$

$$f_H @ -4.6 \text{ dB} = 7.08 \text{ MHz}$$

$$\text{Bandwidth} = f_H - f_L = 7.08 - 13.001 = 7.079 \times 10^6 \text{ Hz}$$

$$\therefore \text{Bandwidth} : \underline{\underline{7.079 \text{ MHz}}}$$



# conclusion :

after adding feedback to the Common Source MOSFET amplifier,  
the new parameters are:

$$\begin{aligned} \textcircled{1} \text{ gain in Voltage } (CAv) &= -1.66 \\ \textcircled{2} \text{ Bandwidth } &= f_H - f_L = 7.079 \times 10^6 \text{ Hz} \\ &= 7.07 \text{ MHz} \end{aligned}$$

END of Lab 5

EXPERIMENT 6 : MOSFET Oscillators# Objective:

To design MOSFET oscillators and analyze the performance using LTSpice.

# Components & Equipments:

- Computer
- LTSpice

# Theory:

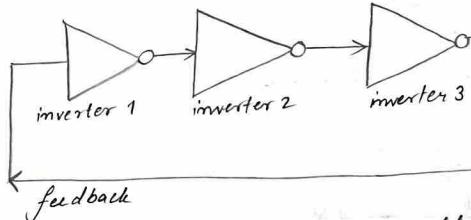
An oscillator is used to generate a signal which has a specific frequency, and these are useful for synchronizing the computation process in digital systems. It is an electronic circuit that produces continuous waveforms without any input signal. The oscillator converts a DC signal into an alternating signal form at the desired frequency. There are various types of oscillators depending on the components which are using in the electronic circuit.

• LC Oscillator :

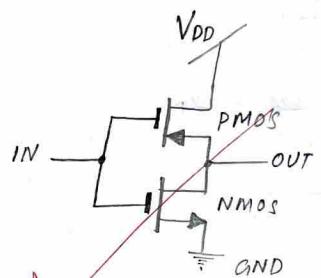
The LC Oscillator is a type of tuned oscillator that uses a combination of inductor (L) and capacitor (C) to provide the required positive feedback, which is essential to produce sustained oscillations ensure periodic oscillations at a specific frequency. LC Oscillators reverse the voltage polarity using an inductor (L) and a capacitor (C) to create the oscillating effect.

• RC Oscillator :

A linear oscillator circuit which uses an RC network,



(6.1) Fig: 3 stage ring oscillator

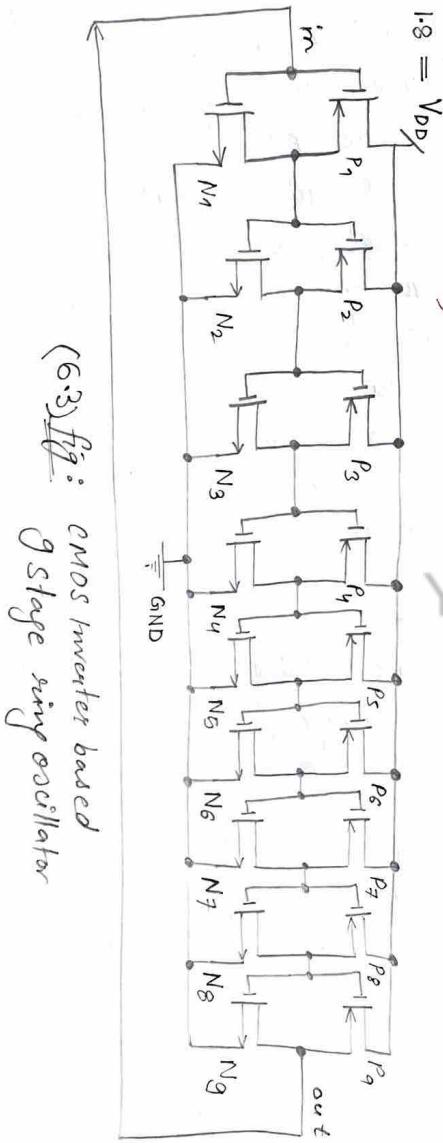


(6.2) Fig: CMOS inverter

a combination of resistors and capacitors, for its frequency selective part is called ~~is~~ an RC oscillator. In RC oscillator circuits which use a single inverting amplifying device, the amplifier provide  $180^\circ$  of the phase shift, so the RBC network must provide the other  $180^\circ$ . Since each capacitor can provide a maximum of  $90^\circ$  of phase shift, RC oscillators require at least 2 frequency-determining capacitors in the circuit (two poles), and most have 3 or more, with a comparable number of resistors. RC oscillators are used to produce lower frequencies, mostly audio frequencies, in such applications as audio-signal generators and electronic musical instruments.

#### Schmitt Trigger:

Schmitt triggers are bistable networks that are widely used to enhance the immunity of circuits to noise and disturbances. The main difference between Schmitt triggers and comparators lies in DC transfer characteristics. The comparators show only one switching threshold, while Schmitt trigger shows different switching thresholds for positive-going and negative-going input signals. This characteristic is called hysteresis. If the node magnitude of the input signal is less than the switching threshold difference, Schmitt trigger will not respond, thus making Schmitt trigger immune to the undesired noise. The Schmitt trigger is a circuit that converts a varying voltage into a stable logical signal (one or zero). The DC transfer characteristic of a Schmitt trigger has hysteresis to reduce the sensitivity to noise and disturbances. The hysteresis in a Schmitt trigger



(6.3) Fig: CMOS inverter based 9 stage ring oscillator

offers better noise margin and noise stable operation.

- Ring Oscillator:

Ring oscillator is described as an odd number of inverters are connected in a series form with positive feedback and output oscillates between 2 voltage levels  $\rightarrow$  either 1 or zero, to measure the speed of the process. These oscillators have an 'n' odd number of inverters. The number of inverter stages in this oscillator mainly depends on the frequency that we want to generate from this oscillators.

# Exercise Problems:

g. Design and simulate a ring oscillator (with CMOS inverters) circuit using LTSpice.

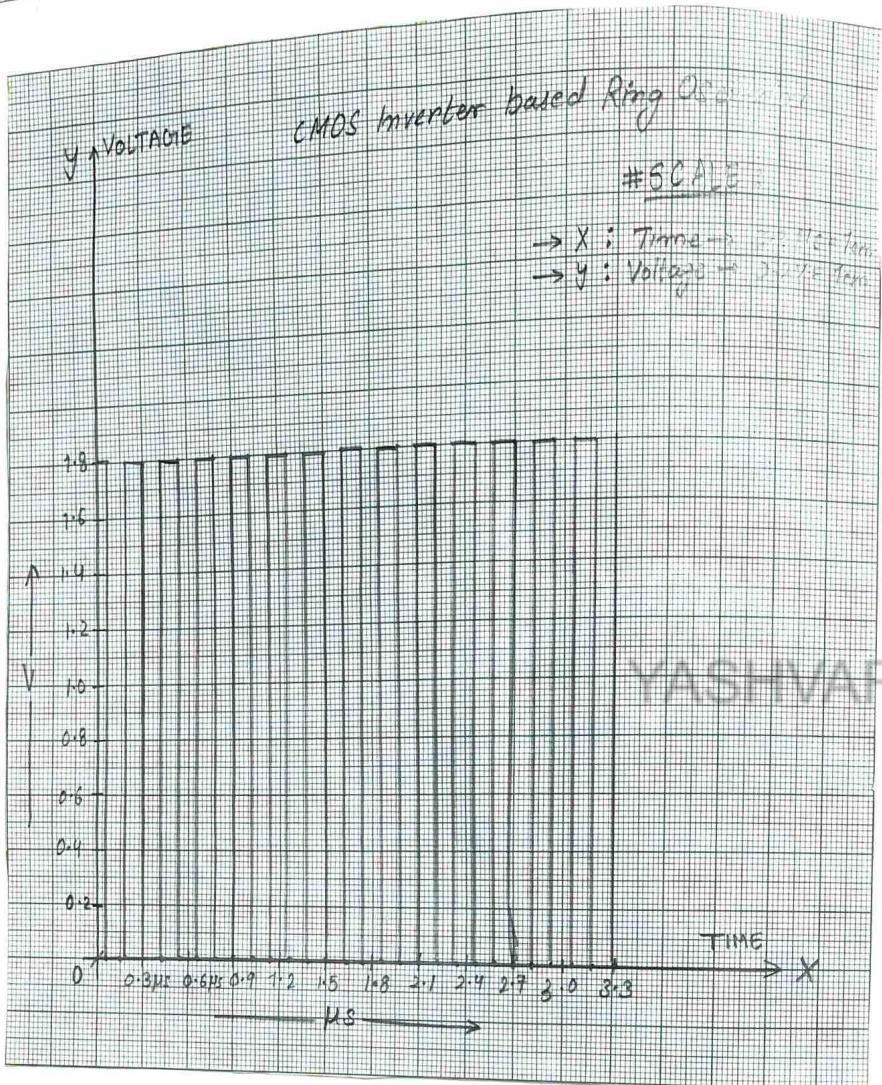
Sol<sup>n</sup>: Design: refer to image 6.3 on page 56.  
 ↳ (on the left side)

Analysis: refer to the plot on next page. (Graph 6.1 – 58 page)

# Conclusion:

The MOSFET oscillators were simulated and analyzed in LT-Simulation Program with Integrated Circuit Emulator.

Expt. No. 7



Graph 6.1

Experiment (6)

[END of Exp - (6)]

EXPERIMENT 7: Linear application of OP-AMPS

## # Objective:

To design and test inverting amplifier, summing amplifiers and integrator using OP-AMPS.

## # Components &amp; Equipment:

Dual source DC power supply, Cathode Ray Oscilloscope, μA741 Op-amp and discrete components.

## # Theory:

(a) INVERTING AMPLIFIER:

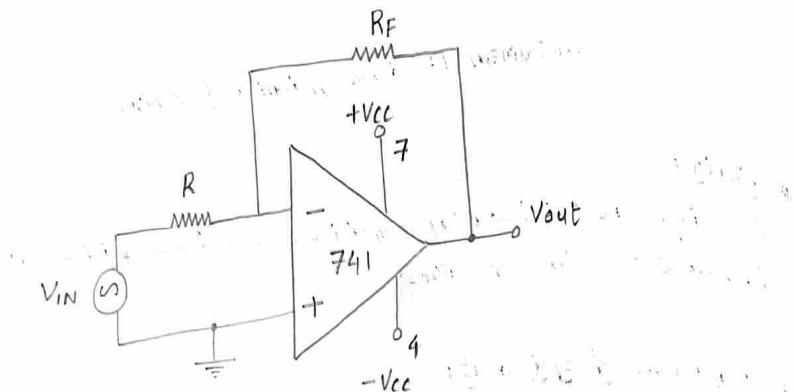
design:  $A_v = 10$ ,  $R = 1\text{ k}\Omega$  and  $R_f = 10\text{ k}\Omega$

diagram and graphs are on the following page.

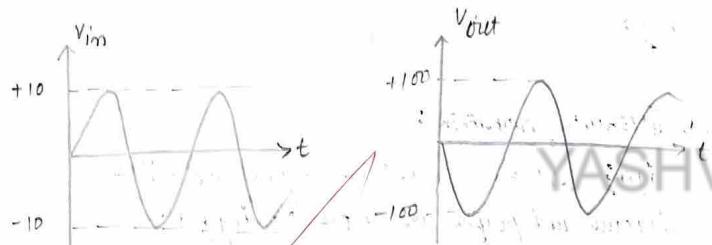
Procedure:

- rig up the circuit as shown in Figure.
- apply  $V_{cc} = \pm 12$  Volts
- Apply 2 Volts peak to peak sinusoidal input signal of 1kHz from AFO.
- Observe the output waveform on the CRO and measure the voltage gain.
- Vary the input frequency from 100 Hz to 1MHz and note down the corresponding output voltage. Also measure the 3dB frequency.
- increase the frequency in multiples of 10 and measure the ~~3dB frequency~~ roll-off rate in dB per decade
- Check what happens if input voltage is increased to 5 V p2p.

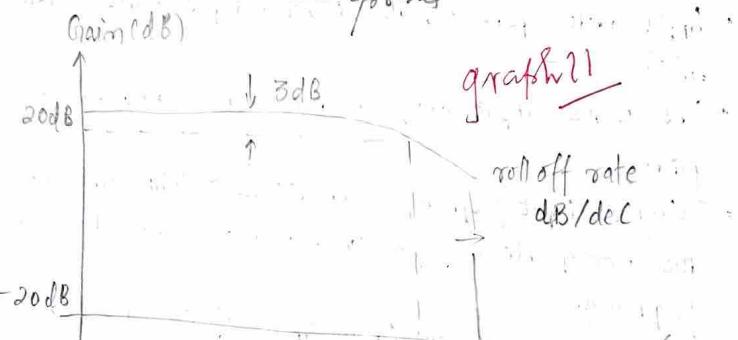
Teacher's Signature \_\_\_\_\_



(7.1)(a) Fig: Inverting Amplifier circuit.



(7.1)(b) Fig: Inverting Amplifier Input &amp; Output Waveforms.



(7.2) Fig: Frequency Response

(b) Summing Amplifier

Design:  $V_{out}$  should be  $= - \frac{(V_1 + V_2)}{R_f}$   
 inversion  $\downarrow$  summation

$$\text{Let } R_f = 1\text{k}\Omega,$$

$$R_1 = R_2 = 1\text{k}\Omega,$$

$$R_3 = R_4 = 1\text{k}\Omega$$

Procedure:

- Construct the circuit as shown in fig 7.3 (next page). Give  $V_1$  and  $V_2$  from 2 different input sources (2 different DC power supplies) and measure the output.
- Repeat for three to four sets of positive / negative values and measure the output.

## # Observations for example (a) Inverting Amplifier

- decibel gain becomes -ve around 140 KHz.

Frequency (Hz)	O/p Voltage (V)	Gain ( $\frac{V}{V_i}$ )	20 Log (Gain) dB
100	19.6 V	-10	20
1K	19.6 V	-10	20
10K	19.6 V	-10	20
15 <del>10</del> K	16.8 V	-8.57	18.659
30K	9.2 V	-4.69	13.423
50K	5.2 V	-2.65	8.464
100K	2.8 V	-1.42	3.045
140K	2.8 V 1.6 V	-1.42 0.8	3.045 -1.938

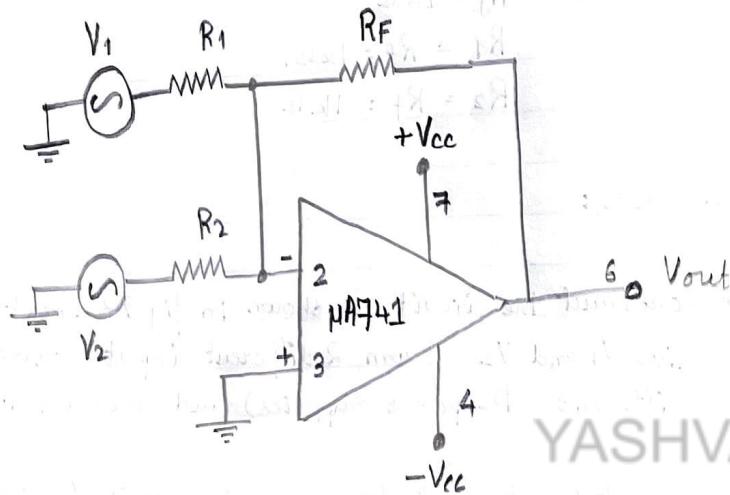
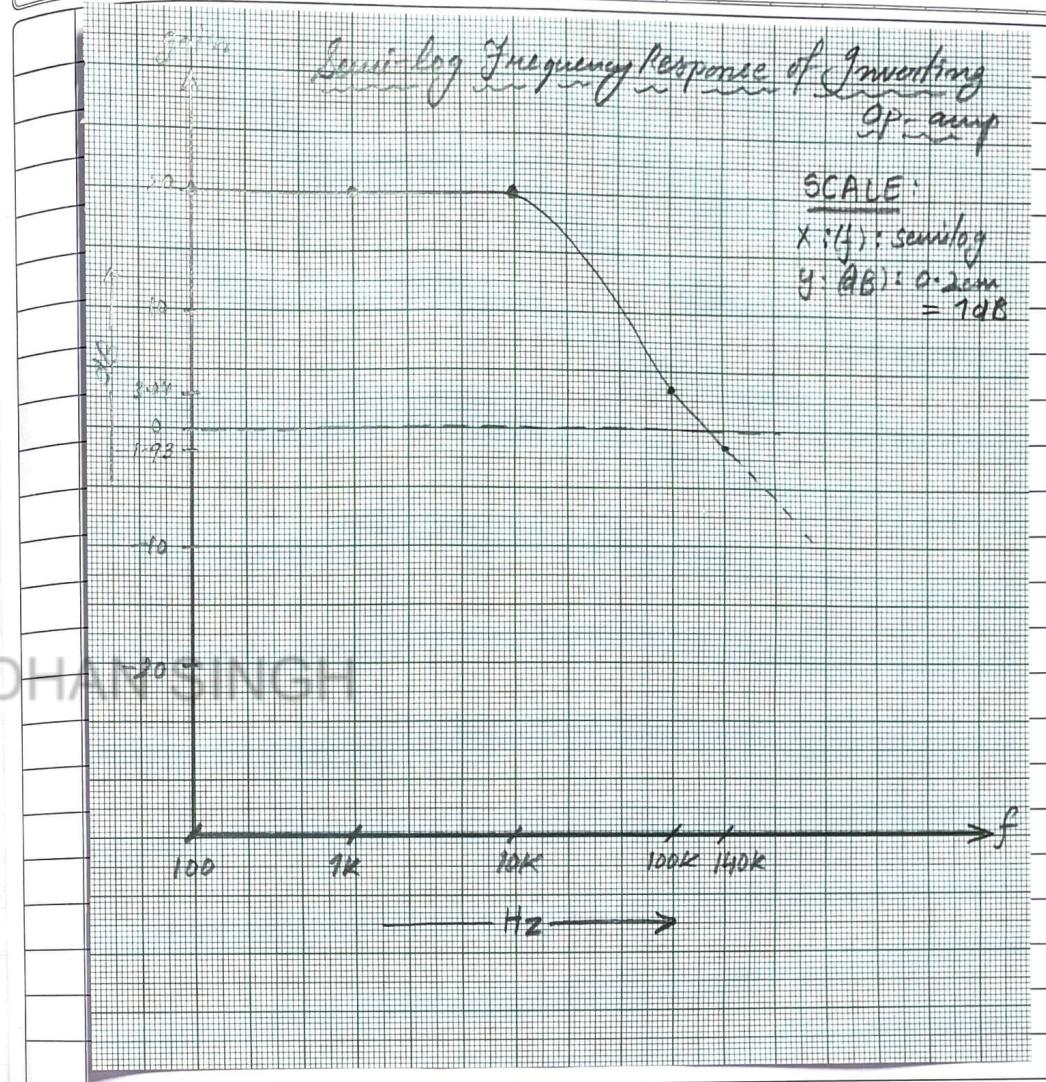


fig 7.3 : Summing  
Op-Amp  
Circuit

Draw the frequency response curve



Experiment 8: Active Filters using OP-AMP# Objective:

To design and implement low pass and high pass active filters  
and to observe frequency responses

# Components & Equipment:

- Dual source DC power supply
- Cathode ray oscillator
- function generator
- OPAMP  $\mu$ A 741
- discrete components

# Theory:# LOW PASS FILTER (LPF): { figure 8-17}design:

$f_c = 1 \text{ kHz}$ , with pass band gain = 2

Assume  $C_1 = C_2 = 0.1 \mu\text{F}$

Let  $R_1 = 10 \text{ k}\Omega$ . Therefore,  $A_v = 1 + \frac{R_f}{R_1} = 2$ ,  $R_2 = 10 \text{ k}\Omega$

procedure:

- 1) Rig up the circuit as shown in figure
- 2) using AFO, apply 1kHz sinusoidal input with p2p amplitude of 1V, positive peak = 0.5V. Observe input & output using CRO.
- 3) Keeping input voltage constant, vary the input frequency from 10 Hertz. to 1 kHz and note down the amplitude change

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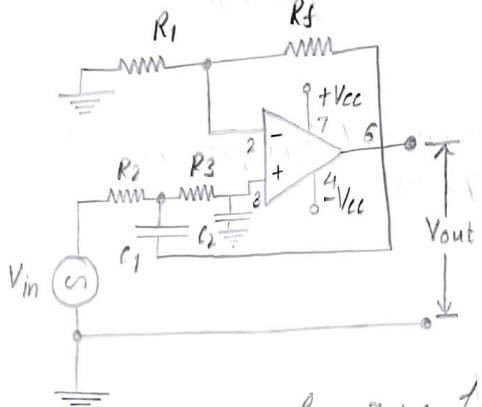


fig 8.1 : Low Pass Filter  
(second order)

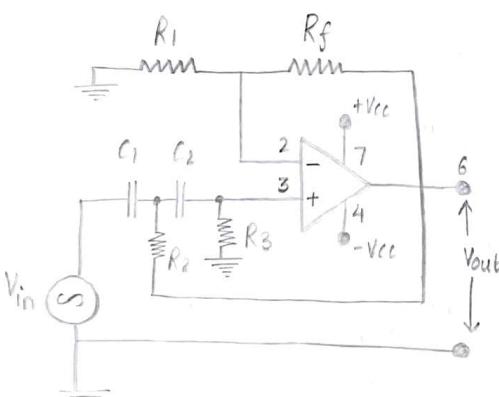
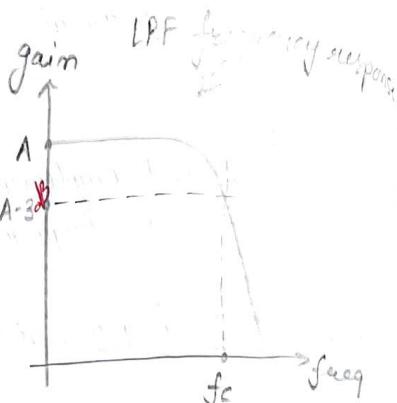
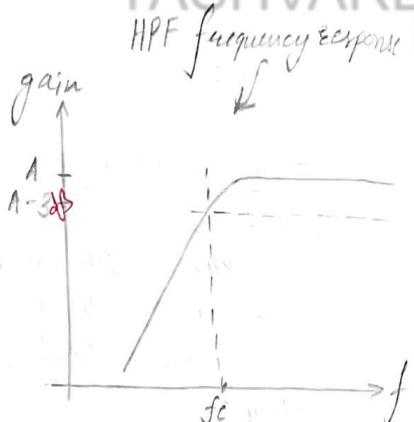


fig 8.2 : High-Pass Filter  
(second order)

YASHVARDHAN SINGH



in output voltage waveform.

HIGH-PASS FILTER : & figure 8.23

design :

$f_c = 100 \text{ Hz}$ , with pass band gain = 2.

Assume  $C_1 = C_2 = 0.1 \text{ mF}$

Let  $R_1 = 10 \text{ k}\Omega$ . Therefore,  $A_v = 1 + \frac{R_f}{R_1} = 2$ , then  $R_2 = 10 \text{ k}\Omega$ .

### # Excuse questions :

find

q1. Frequency response of Notch Band pass filter.

Solution:

frequency (Hz)	$V_{out}^{(V)}$	Gain (dB)
10	2.6 V	-17.97
100	3	-16.73
1K	3.4	-15.64
10K	4.8	-12.65
100K	9.2	-7
1M	7.2	-9.10

constant  $V_{in} = 20.6 \text{ V}$

graph of frequency response & circuit on  
next page.

→ Please Turn Over

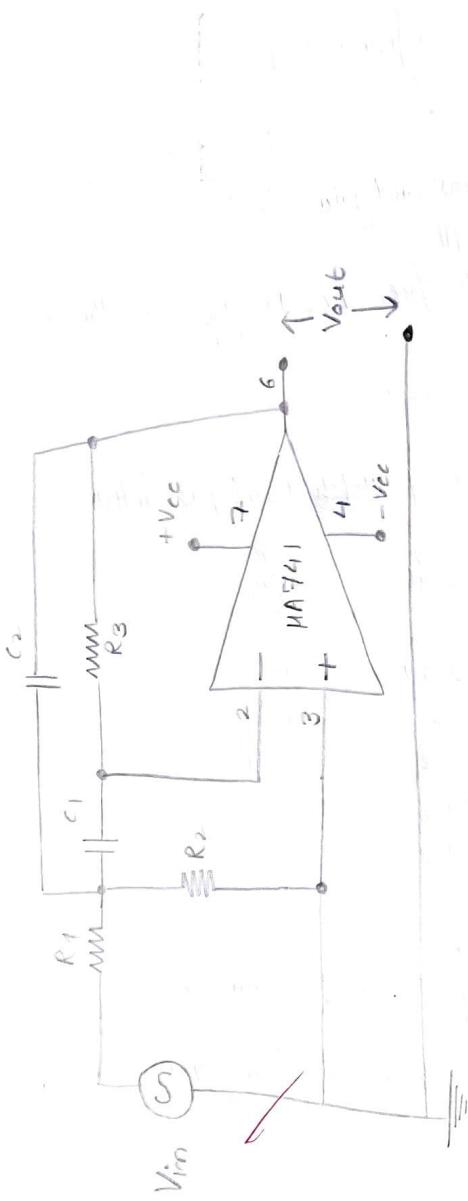
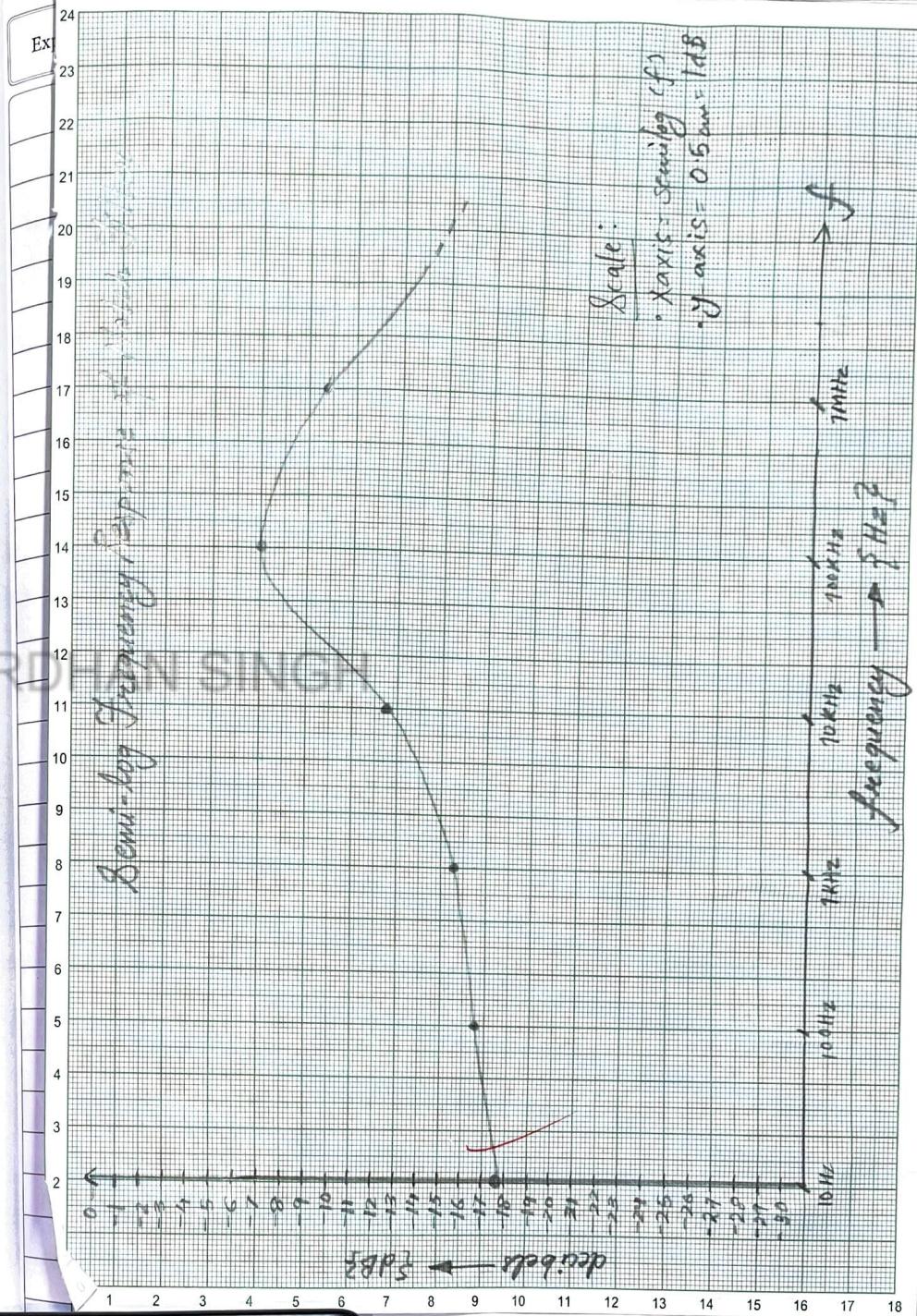


Fig 8.3 : Notch Band Pass Filter



Q2. Find PHASE Frequency Response for All-pass filter.

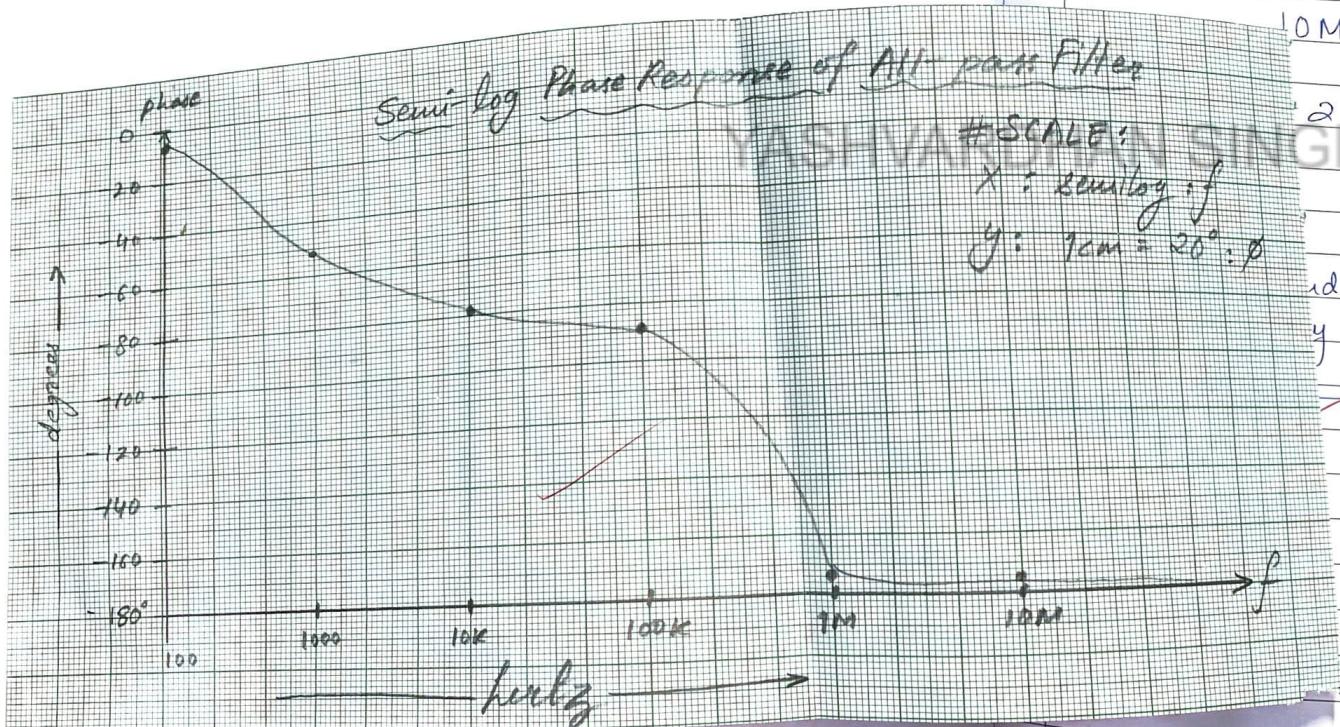
Solution :

$$R_f = R_1 = R = 10k\Omega$$

Frequency (Hz)	Phase Shift (degrees)
100	-7.16°
1K	-53.13°
10K	-79.65°
100K	-89.98°
1M	-179.99°
10M	-179.99°

$$2 \tan^{-1} (2 \pi f RC)$$

# SCALE:  
 $X : \text{Semilog of } f$   
 $y : 1cm = 20^\circ : \phi$



nd practical observation of OP-AMP based active  
y similar trends.

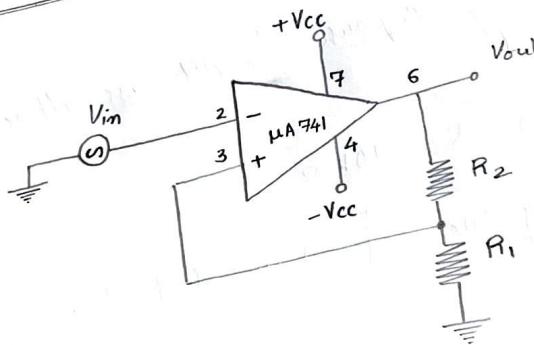


Fig 9.1: (a) Inverting Schmitt Trigger Circuit

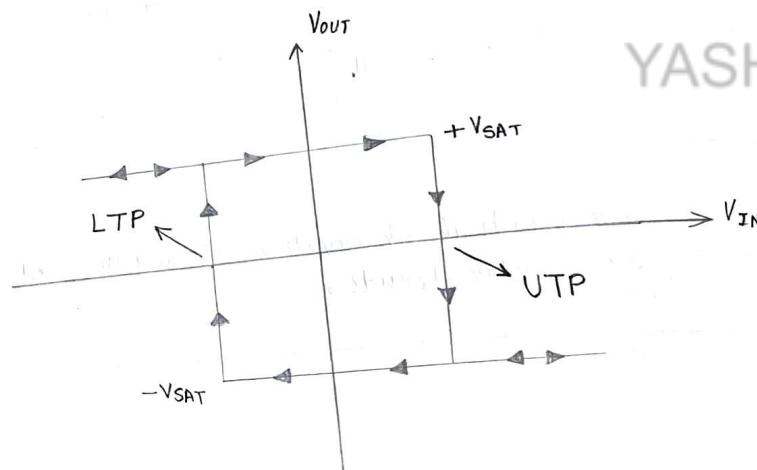


Fig 9.1: (b) Hysteresis Curve

Expt. No. 9

Date Feb  
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### Experiment 09: Schmitt Trigger using OP-AMP

#### # Objective:

To design and test Schmitt Trigger using OP-AMP.

#### # Components & Equipment:

- Dual mode DC power supply
- Cathode Ray oscilloscope
- UA 741
- discrete components

#### # Procedure:

- Rig up the circuit as shown in fig. 9.1 (a)
- Apply 1 kHz sinusoidal signal of 1V peak to peak.
- Observe and note the input and output waveforms using Oscilloscope.

#### # DESIGN:

- $V_{UTP} = 7.5 \text{ volts}$
- $V_{LTP} = -7.5 \text{ volts}$
- $V_{OUT} = \pm 15 \text{ volt}$

$$V_{UTP} = \frac{R_1}{R_1 + R_2} V_{sat}$$

$$R_1 = R_2 = 1 \text{ k}\Omega$$

$$V_{LTP} = \frac{-R_1}{R_1 + R_2} V_{sat}$$

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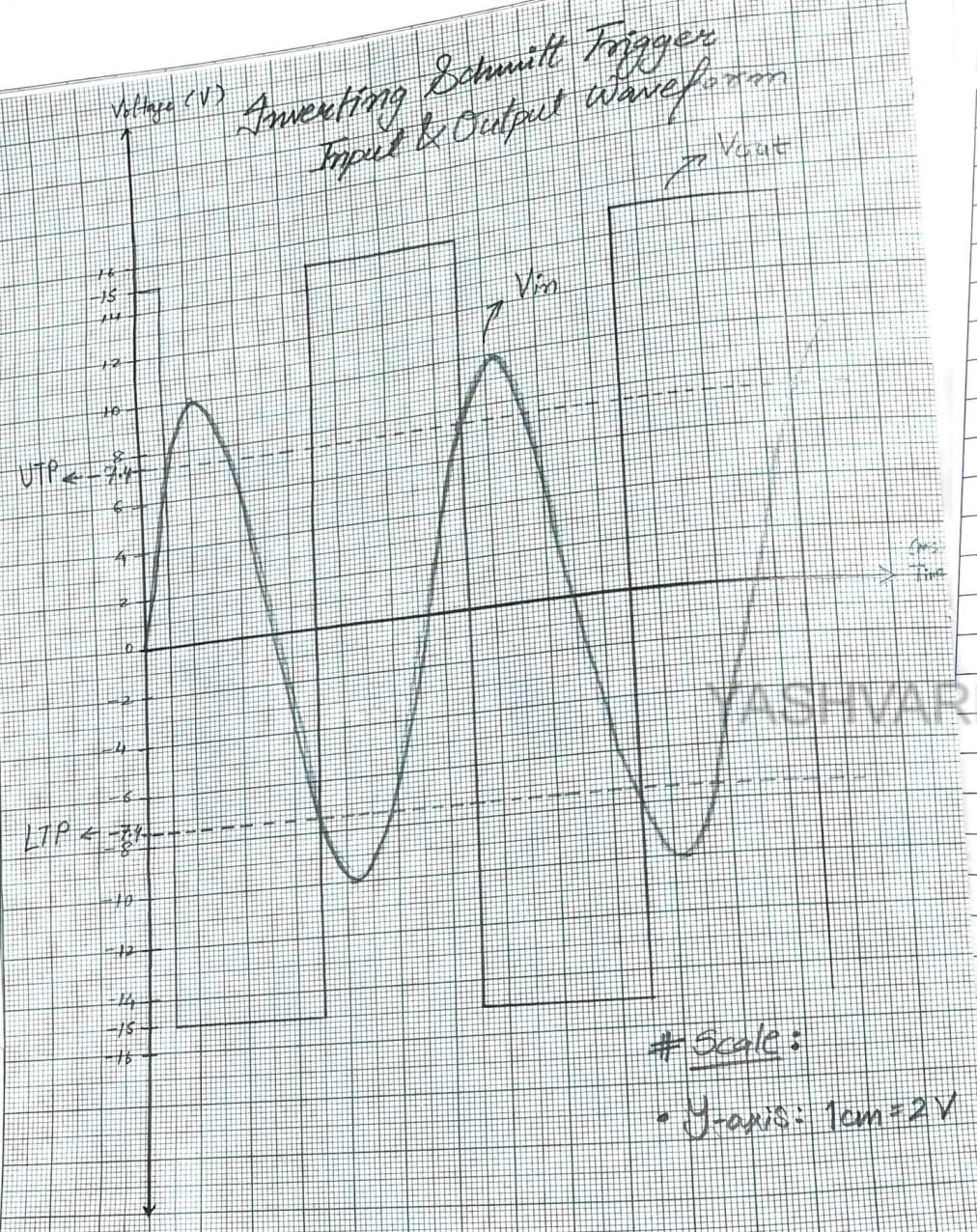


fig 9.1(c): Schmitt Trigger I/O waveform

Expt. No. 9

Date \_\_\_\_\_  
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$$V_{UTP} \text{ (Theoretical)} = \frac{R_1 (+V_{sat})}{R_1 + R_2} = \frac{1}{2} (15) = 7.5 \text{ V}$$

$$V_{LTP} \text{ (Theoretical)} = R_1 (-V_{sat}) = \frac{1}{2} (-15) = -7.5 \text{ V}$$

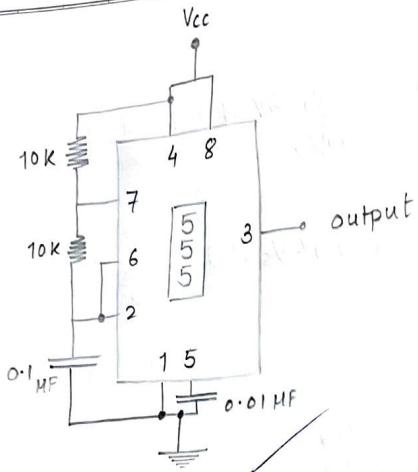
# Results :

- $V_{UTP}$  (practical) = 7.4 V
- $V_{LTP}$  (practical) = -7.4 V

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27/10/2021*

example ①



example ②

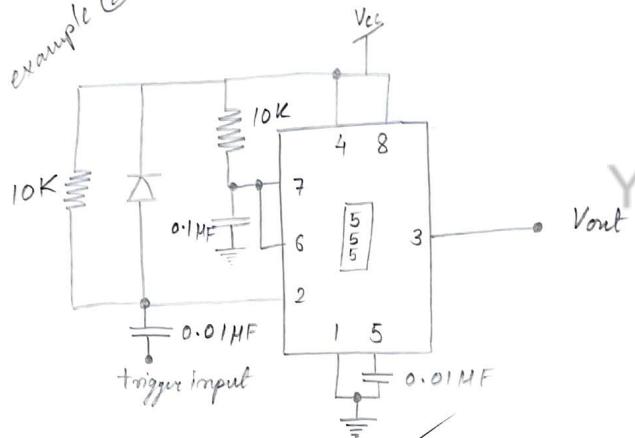


Fig 10.2: Monostable multivibrator

Expt. No. 10

Experiment 10:

## 555 Timer Applications

# OBJECTIVE:

To design Astable and Monostable multivibrators using IC 555.

# COMPONENTS:

- IC 555
- DC Power Supply
- C.R.O
- IN4001
- discrete components

# Astable Multivibrator:

circuit: fig 10.1 → page 76

plot: graph 10.1 → page 80

Observations:

- V<sub>pp</sub> of Square Wave : 4.56V
- V<sub>pp</sub> of Capacitor voltage : 1.75V
- T<sub>ON</sub> : 0.88 ms
- T<sub>OFF</sub> : 0.486 ms

Result:

output	Theoretical	Practical
Frequency	500 Hz	727 Hz
Amplitude	5V	4.56V

Nuty cycle = 64.42%

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Expt. No. 10

## # Monostable multivibrator:

## • Observations:

circuit : fig 10.2 → page 76

plot : graph 10.2 → page 82

- ① V<sub>PP</sub> of Pulse Wave : 4.32 Volts
- ② V<sub>PP</sub> of Capacitor Voltage : 4.6 Volts
- ③ T<sub>ON</sub> : 780 μs
- ④ T<sub>OFF</sub> : 860 μs
- ⑤ Duty Cycle : 0.4756 or 47.56%

## # EXERCISES:

Q1. 555 Timer IC Circuit to generate 3 kHz, 75% duty cycle square wave.

circuit : fig 10.3 (page 78) plot : graph 10.3 (page 84)

Solution :

$$T = 1/f = 1/3 \times 10^3 = 3.333 \times 10^{-4} \text{ s}$$

$$(R_A + R_B) C \times 0.69 = 2.5 \times 10^{-4} \rightarrow ①$$

$$R_B C \times 0.69 = 8.3 \times 10^{-5} \rightarrow ②$$

$$\frac{t_{on}}{t_{on} + t_{off}} = 0.75 \rightarrow ③$$

$$t_{on} = 2.5 \times 10^{-4} \text{ s} \quad t_{off} = 8.3 \times 10^{-5} \text{ s}$$

let's assume,

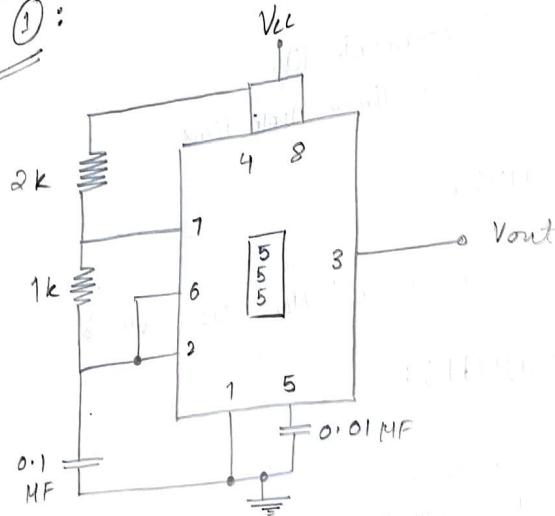
$$R_A C = X$$

$$R_B C = Y$$

$$Y = \frac{8.3 \times 10^{-5}}{0.69} = 1.202 \times 10^{-4}$$

$$(X+Y) 0.69 = 2.5 \times 10^{-4}$$

exercise ① :

Fig 10.3 : 75% duty cycle at 3 kHz  
astable multivibrator

exercise ② :

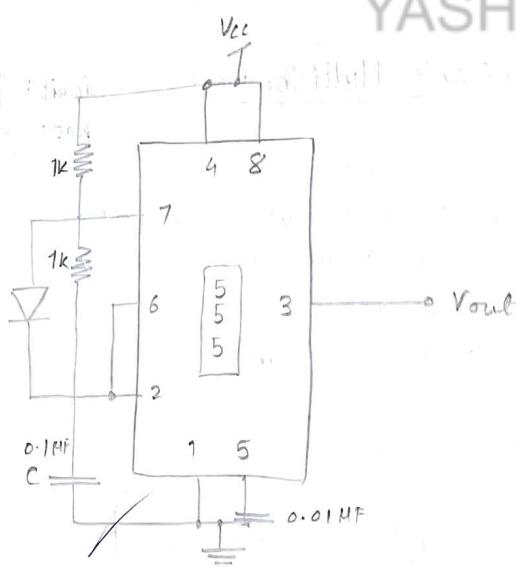
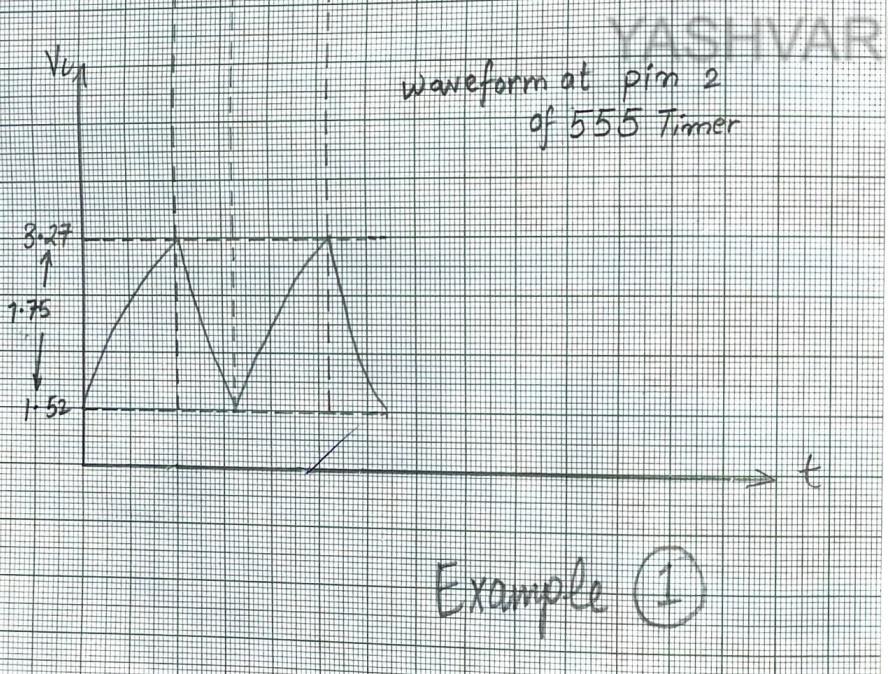
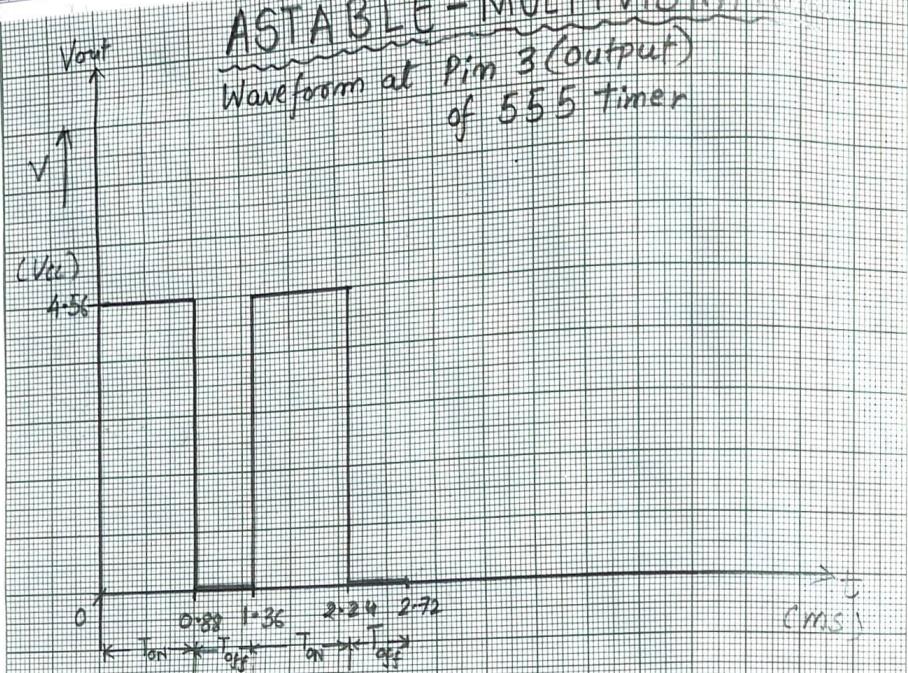


fig 10.4 : Symmetric astable multivibrator

Expt. No. 10



graph 10-1

$$\therefore X = RAC = 2.420 \times 10^{-4}$$

$$Y = RBC = 1.202 \times 10^{-4}$$

$$\frac{X}{Y} = \frac{RAC}{RBC} = \frac{RA}{RB} = \frac{2.420}{1.202}$$

$$RA = 2.013 RB$$

$$RA \approx 2 RB$$

$$\frac{t_{on}}{t_{on} + t_{off}} = 0.75 \rightarrow ③$$

substitute ① and ② in ③:

$$\frac{(X+Y) 0.69}{[R+Y] 0.69 + [Y - X] 0.69} = 0.75$$

$$\frac{0.69 (X+Y)}{0.69 (X+Y+Y)} = 0.75$$

$$\frac{X+Y}{X+2Y} = 0.75 ; X = RAC, Y = RBC$$

$$\frac{RA\ell + RBL}{RA\ell + 2RBC} = 0.75 \quad ; \quad \frac{3RB}{4RB} = 0.75$$

$$\frac{2RB + RB}{2RB + 2RB} = 0.75$$

$$RB = 1k\Omega$$

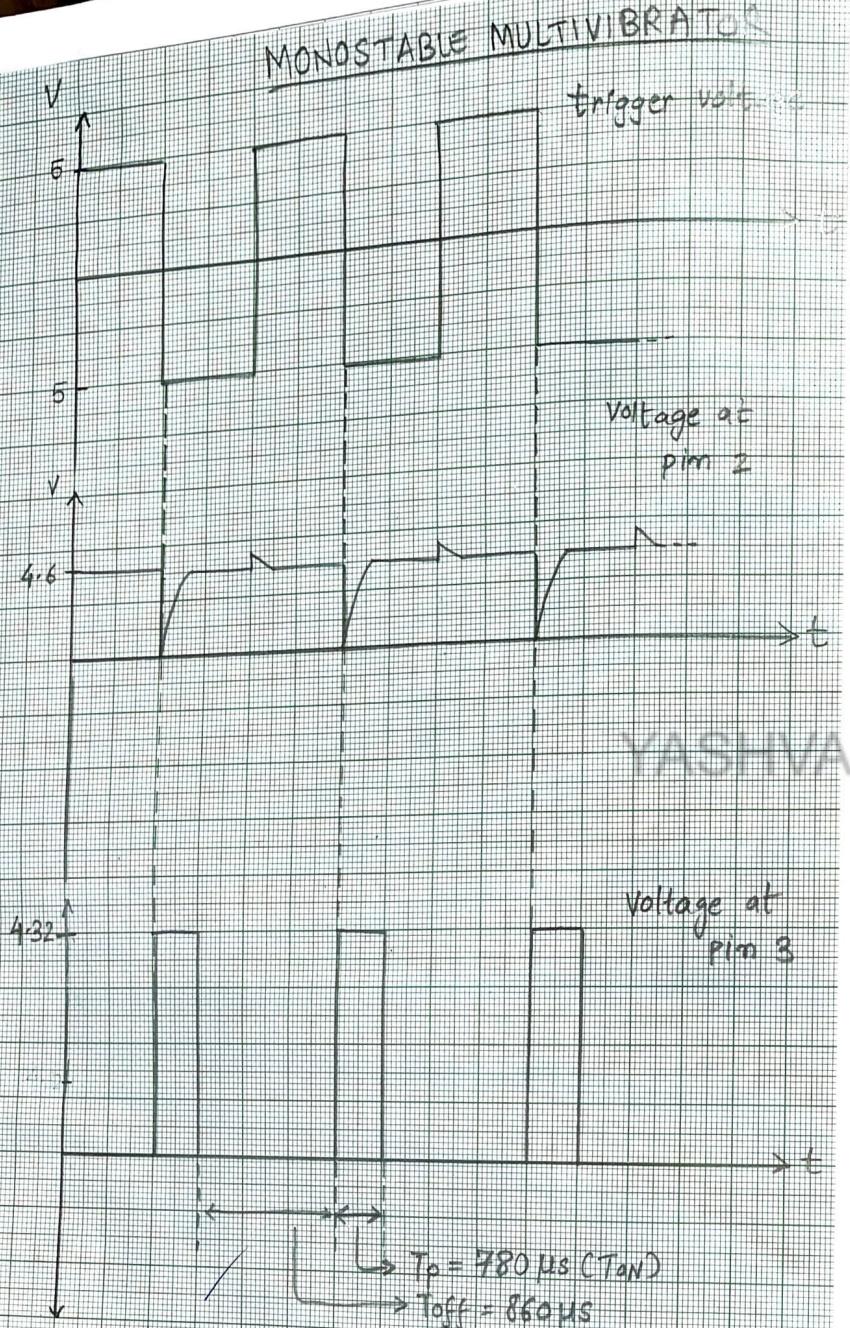
$$RA = 2k\Omega$$

$$C = 0.1\mu F$$

$$690 L \cdot 8.3 \times 10^{-5} \Rightarrow C = 0.1202 \mu F$$

Teacher's Signature \_\_\_\_\_

Expt. No. 10



Graph 10.2 - Example

component parts: (values)

$R_A = 2 k\Omega$
$R_B = 1 k\Omega$
$C = 0.1 \mu F$

• OBSERVATIONS:

- ①  $t_{on} : 136 \mu s$
- ②  $t_{off} : 46 \mu s$
- ③ total :  $182 \mu s$
- ④ Duty cycle :  $74.725\%$ .

Q2. Design symmetric astable multivibrator parameters and values given.

• OBSERVATIONS:

- ①  $t_{on} : 54 \mu s$
- ②  $t_{off} : 50 \mu s$
- ③ total :  $104 \mu s$
- ④ Duty Cycle :  $51.92\% \rightarrow 50\% \text{ (symmetric)}$

• circuit : fig 10.4 (page 78)  
 • plot : Graph 10.4 (page 85)

