Digital Electronics - Internal Assessment - (4)

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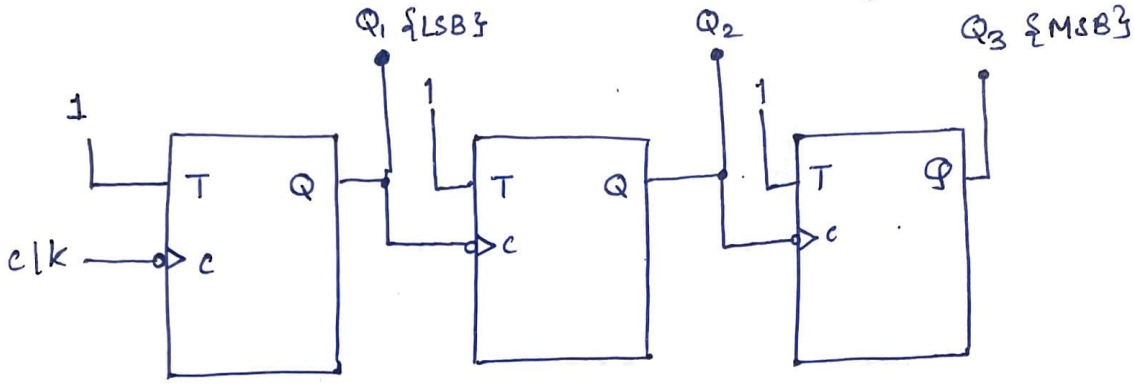
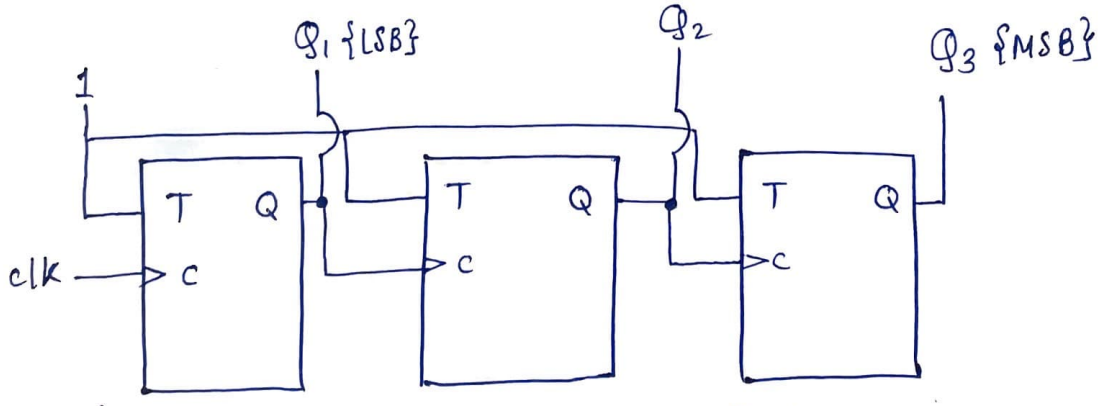
SIGN : yve

Q1] (i) 3 bit asynchronous up counter using T-ff



(ii) 3 bit asynchronous down counter using T-ff



↳ uses positive edge triggered clock instead of the negative edge triggered clock being used by up-counter (asynchronous).

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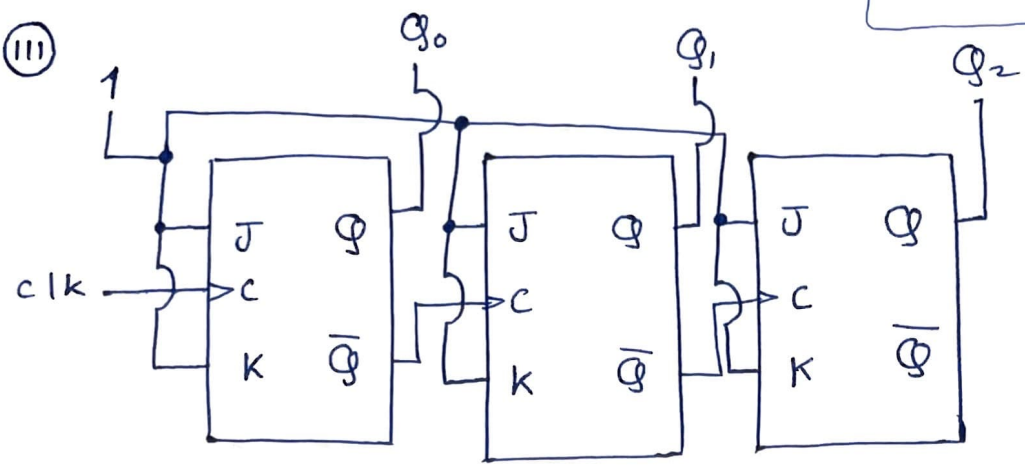
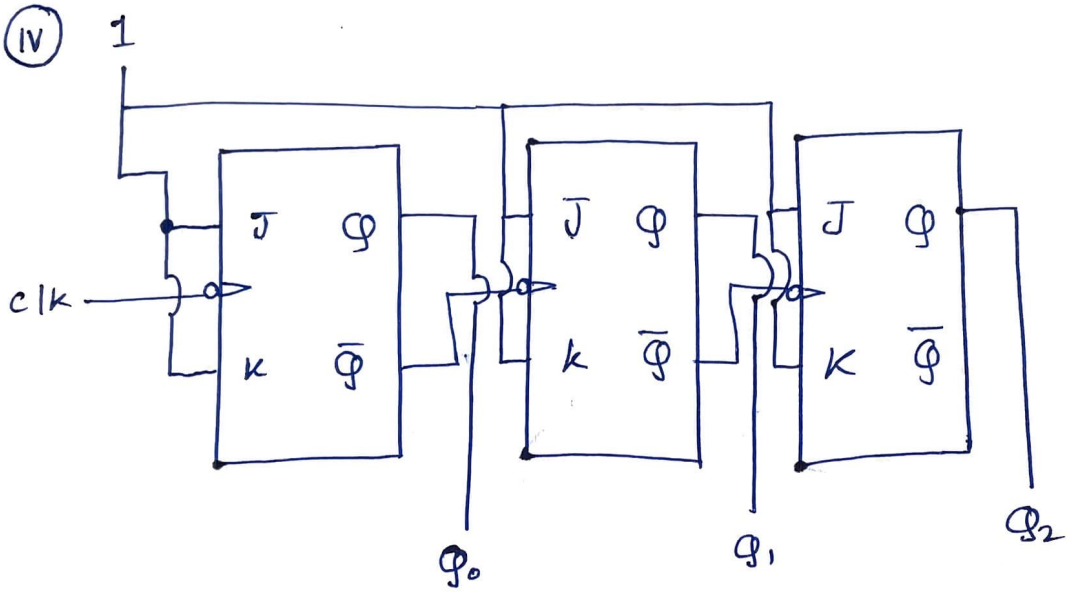
Q1] (III)



3-bit asynchronous up counter

(IV)



3 - bit asynchronous down counter

Q1] (V) 3 bit synchronous up counter using JK-FF.

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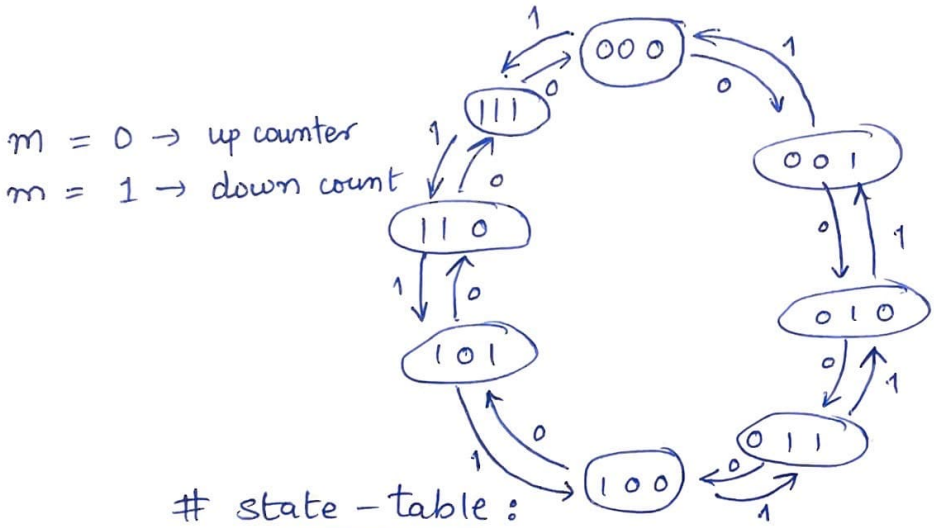
Excitation table of JK:

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

state-diagram:



state-table:

	m	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	J_2	K_2	J_1	K_1	J_0	K_0
UP	0	0	0	0	0	0	1	0	x	0	x	1	x
	0	0	0	1	0	1	0	0	x	1	x	x	1
	0	0	1	0	0	1	1	0	x	x	0	1	x
	0	0	1	1	1	0	0	1	x	x	1	x	1
	0	1	0	0	1	0	1	x	0	0	x	1	x
	0	1	0	1	1	1	0	x	0	1	x	x	1
	0	1	1	0	1	1	1	x	0	x	0	1	x
	0	1	1	1	0	0	0	x	1	x	1	x	1
DOWN	1	0	0	0	1	1	1	1	x	1	x	1	x
	1	0	0	1	0	0	0	0	x	0	x	x	1
	1	0	1	0	0	0	1	0	x	x	1	1	x
	1	0	1	1	0	1	0	0	x	x	0	x	1
	1	1	0	0	0	1	1	x	1	1	x	1	x
	1	1	0	1	1	0	0	x	0	0	x	x	1
	1	1	1	0	1	0	1	x	0	x	1	1	x
	1	1	1	1	1	1	0	x	0	x	0	x	1

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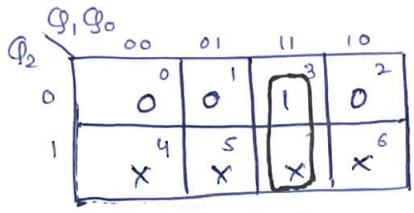
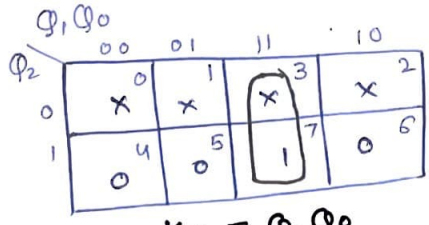
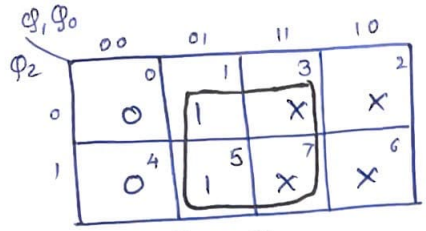
(v) # Solving k-maps : for (m = 0)



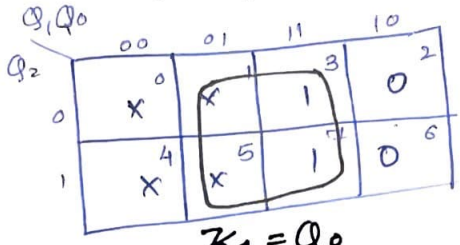
$J_2 = Q_1 Q_0$



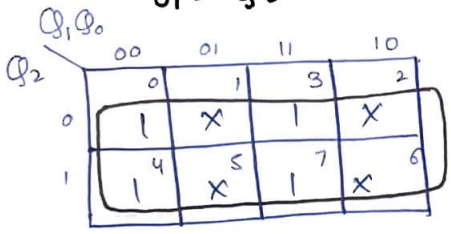
$K_2 = Q_1 Q_0$



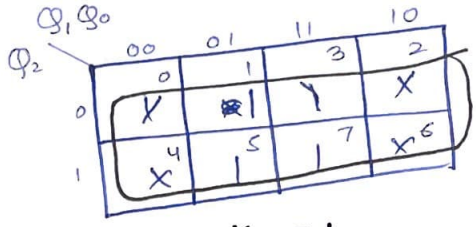
$J_1 = Q_0$



$K_1 = Q_0$



$J_0 = 1$

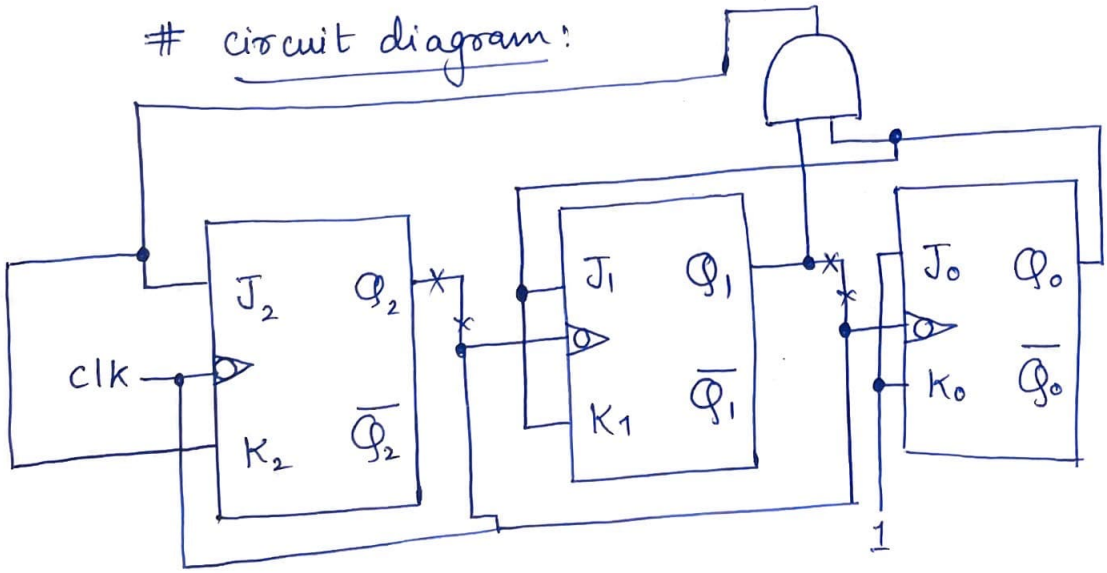


$K_1 = 1$

clock and state table:

	$Q^{\oplus}$	$\overline{Q}^{\ominus}$
▷ +ve edge	down	up
○▷ -ve edge	up	down

circuit diagram:



Q1] (VI) 3 bit synchronous down counter

→ borrowing the state table / diagram and excitation table from Q1. (V), for $m = 1$.

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solving k-maps for $m = 1$:

J_1

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	x	x
1	1	0	x	x

$J_1 = \overline{Q_0}$

K_1

Q_2 \ Q_1Q_0	00	01	11	10
0	x	x	0	1
1	x	x	0	1

$K_1 = \overline{Q_0}$

J_2

Q_2 \ Q_1Q_0	00	01	11	10
0	1	0	0	0
1	x	x	x	x

$J_2 = \overline{Q_1 Q_0}$

K_2

Q_2 \ Q_1Q_0	00	01	11	10
0	x	x	x	x
1	1	0	0	0

$K_2 = \overline{Q_1 Q_0}$

$J_0, K_0 = 1 = \text{High}$

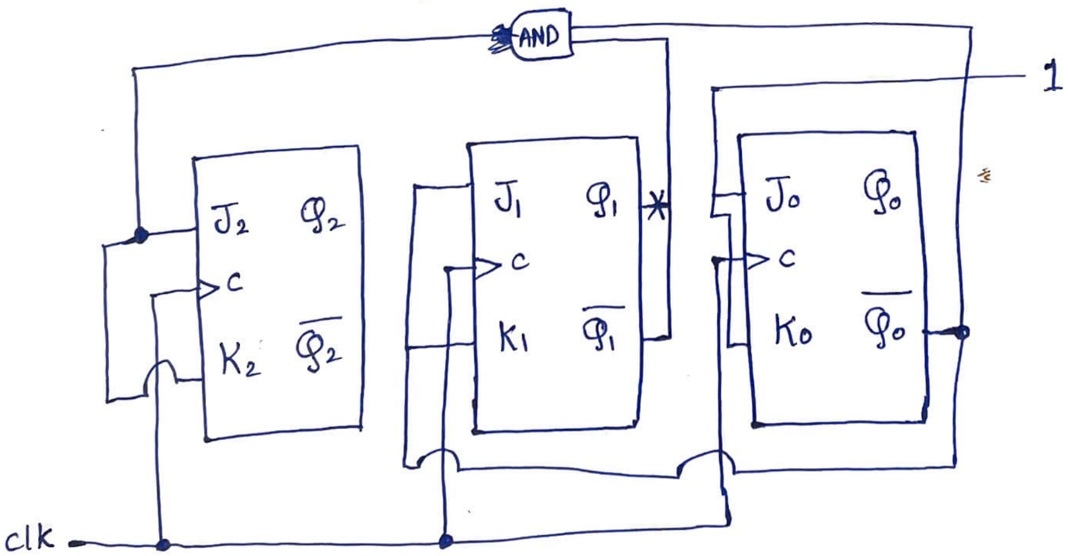

fig: 3 bit synchronous down counter

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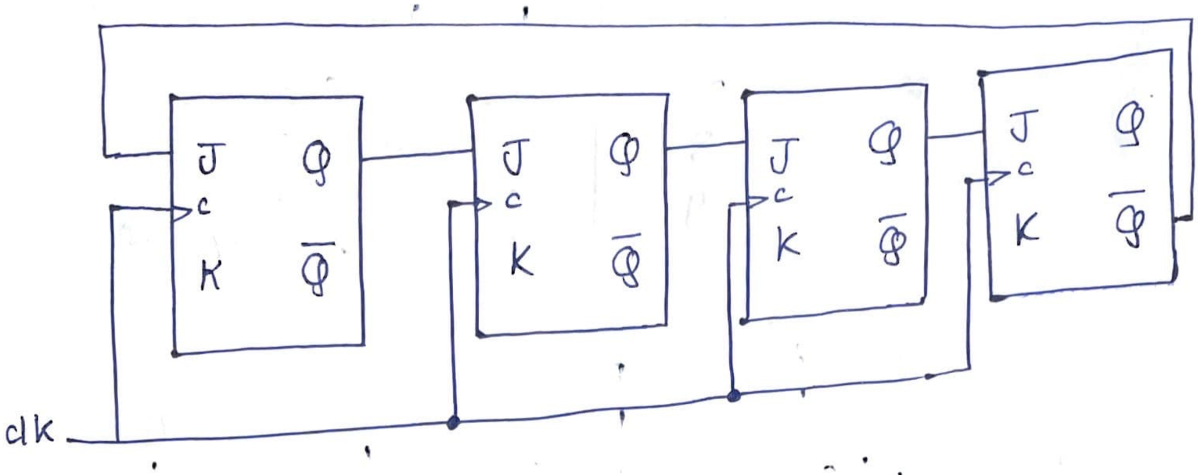
Q1] VII) 4 bit Johnson Counter :

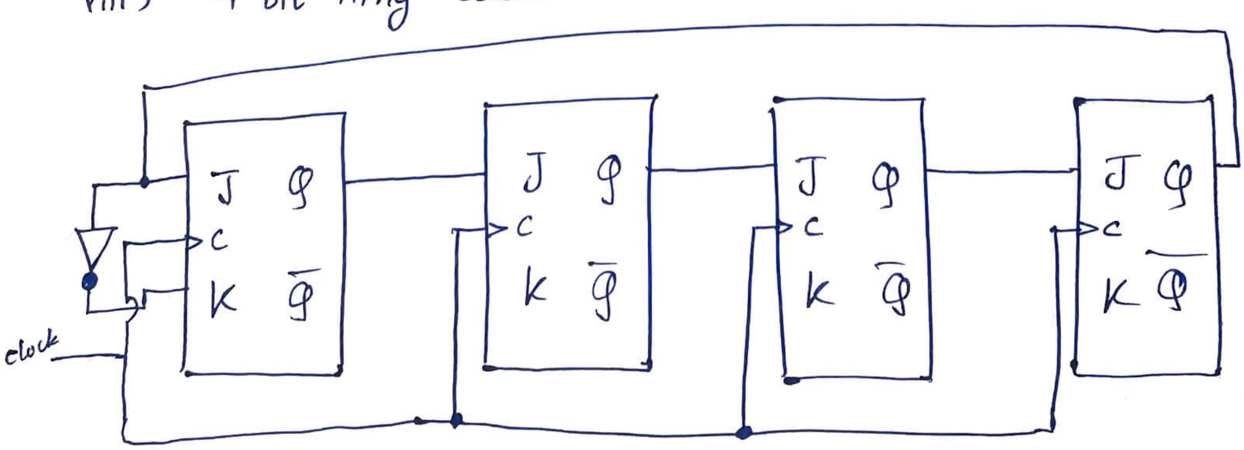


TRUTH-TABLE :

clock	A	B	C	D
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1
8	0	0	0	1

after this cycle repeats...

VIII) 4 bit Ring Counter :



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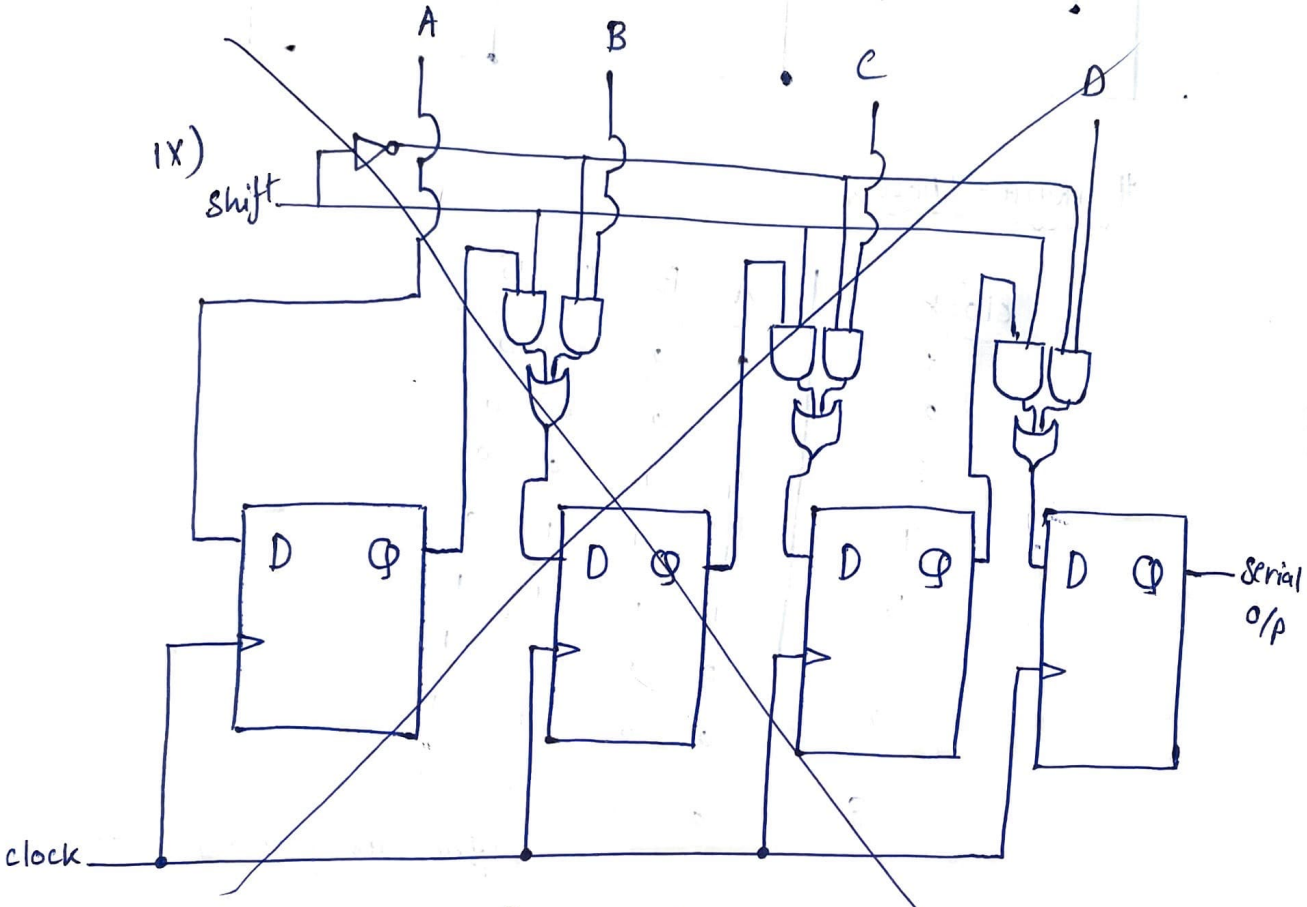
Q1] VIII) # Truth - Table :

clock	A	B	C	D
1	1	0	0	0
2	0	1	0	0
3	0	0	1	0
4	0	0	0	1

.... repeats

IX)



→ please turn over...

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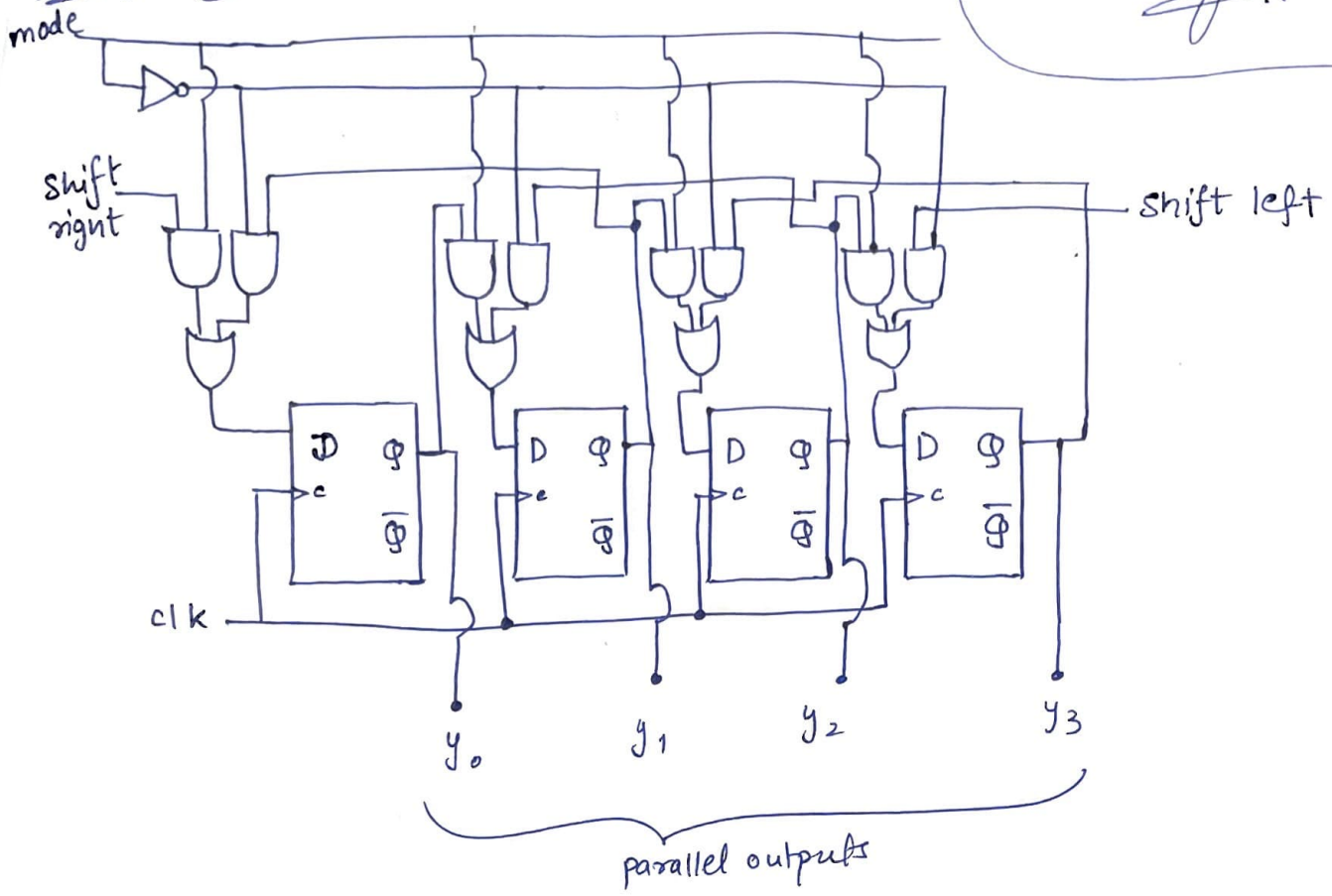
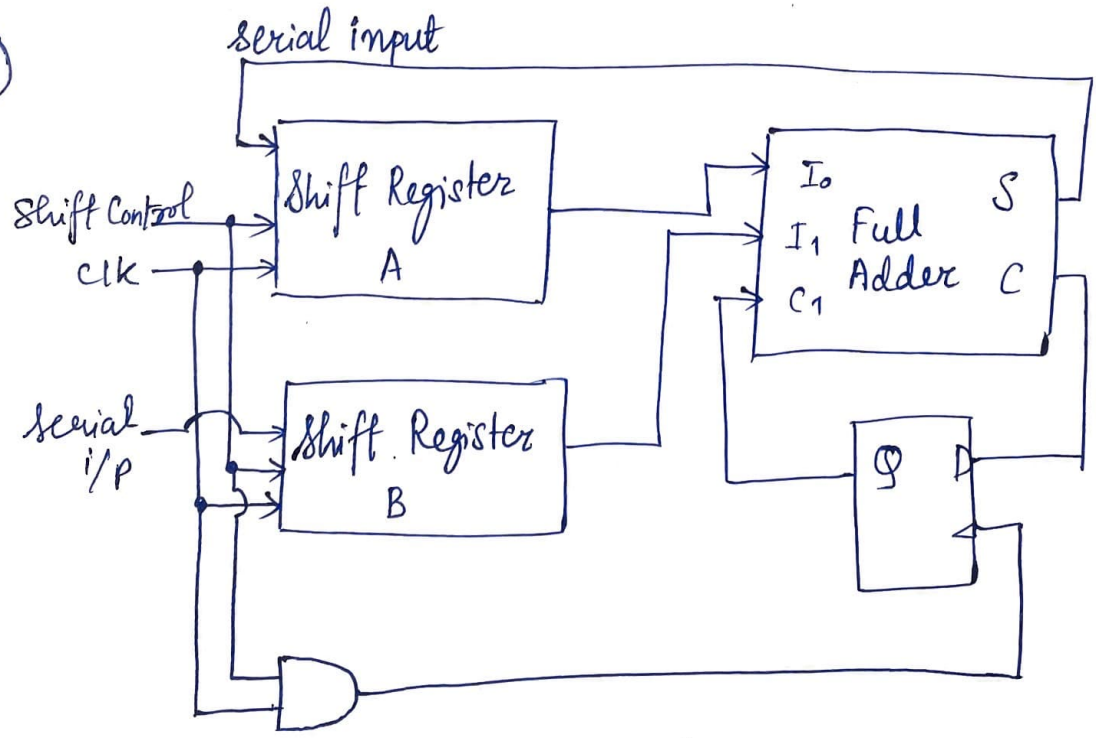
Q1 (IX)



Bi-directional Shift Register

(X)



Serial Adder