

GRAPHIC ERA HILL UNIVERSITY

DEHRADUN

Name- Rahul Singh Ramat

Roll No- 21561011

Enrolment No. PV-21010158

Course- MCA Sem- I

Section- A

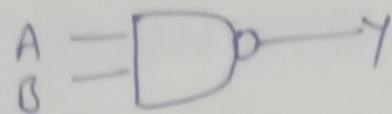
Subject- Computer organisation and
Architecture Mid sem
Practical Exam.

Rahul

Pabul Singh Rawat 21561011

① NAND gate

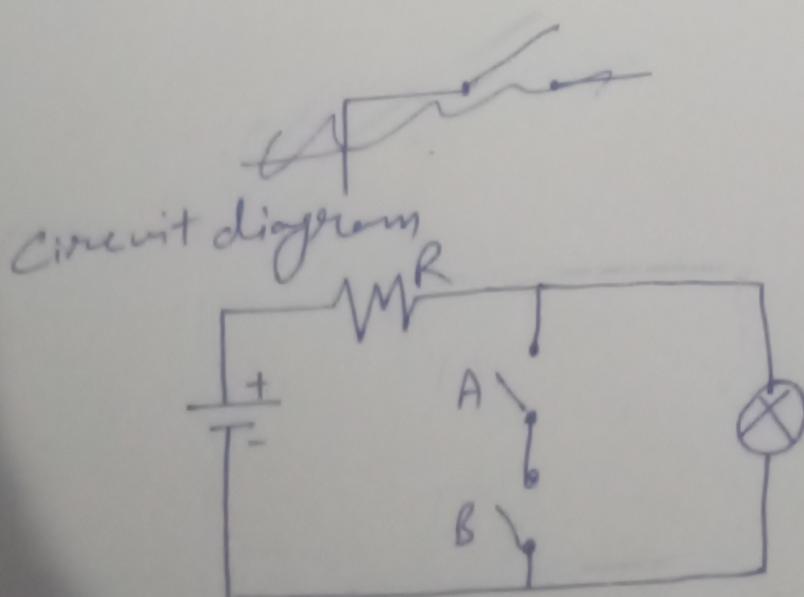
The NAND gate is the combination of two basic logic gates, the AND gate and the NOT gate connected in series.



$$Y = \overline{A \cdot B}$$

Truth table.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



Rohit