VLSI MINI PROJECT EC383

RTL to GDSII ASIC Flow 32-bits MIPS Pipelined Processor.

Submitted in partial fulfillment of the requirements for the degree of
BACHELOR OF TECHNOLOGY in
ELECTRONICS AND COMMUNICATION ENGINEERING

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OBJECTIVE :

Objective: Develop a high-performance MIPS 32-bit pipelined design from RTL to GDSII utilizing ASIC flow. Optimize for speed, area, and power efficiency while ensuring design correctness and adherence to specifications. Employ advanced techniques in synthesis, timing closure, physical design, and verification to achieve a robust and manufacturable ASIC implementation..

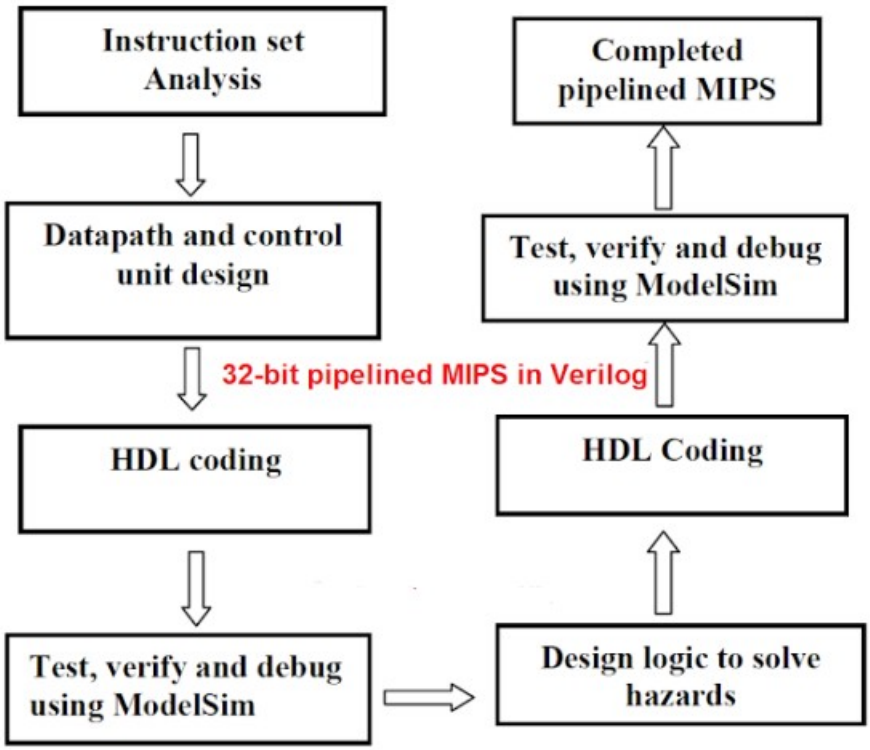
TOOLS USED :

1.OPENLane

1. Synthesis
    1. yosys/abc - Perform RTL synthesis and technology mapping.
    2. OpenSTA - Performs static timing analysis on the resulting netlist to generate timing reports
2. Floorplanning
    1. init_fp - Defines the core area for the macro as well as the rows (used for placement) and the tracks (used for routing)
    2. ioplacer - Places the macro input and output ports
    3. pdngen - Generates the power distribution network
    4. tapcell - Inserts welltap and decap cells in the floorplan
3. Placement
    1. RePLace - Performs global placement
    2. Resizer - Performs optional optimizations on the design
    3. OpenDP - Performs detailed placement to legalize the globally placed components
4. CTS
    1. TritonCTS - Synthesizes the clock distribution network (the clock tree)
5. Routing
    1. FastRoute - Performs global routing to generate a guide file for the detailed router
    2. TritonRoute - Performs detailed routing
    3. OpenRCX - Performs SPEF extraction
6. Tapeout
    1. Magic - Streams out the final GDSII layout file from the routed def
    2. KLayout - Streams out the final GDSII layout file from the routed def as a back-up
7. Signoff
    1. Magic - Performs DRC Checks & Antenna Checks
    2. KLayout - Performs DRC Checks
    3. Netgen - Performs LVS Checks
    4. CVC - Performs Circuit Validity Checks

2. OPENRoad
3. YOSYS
4. Klayout

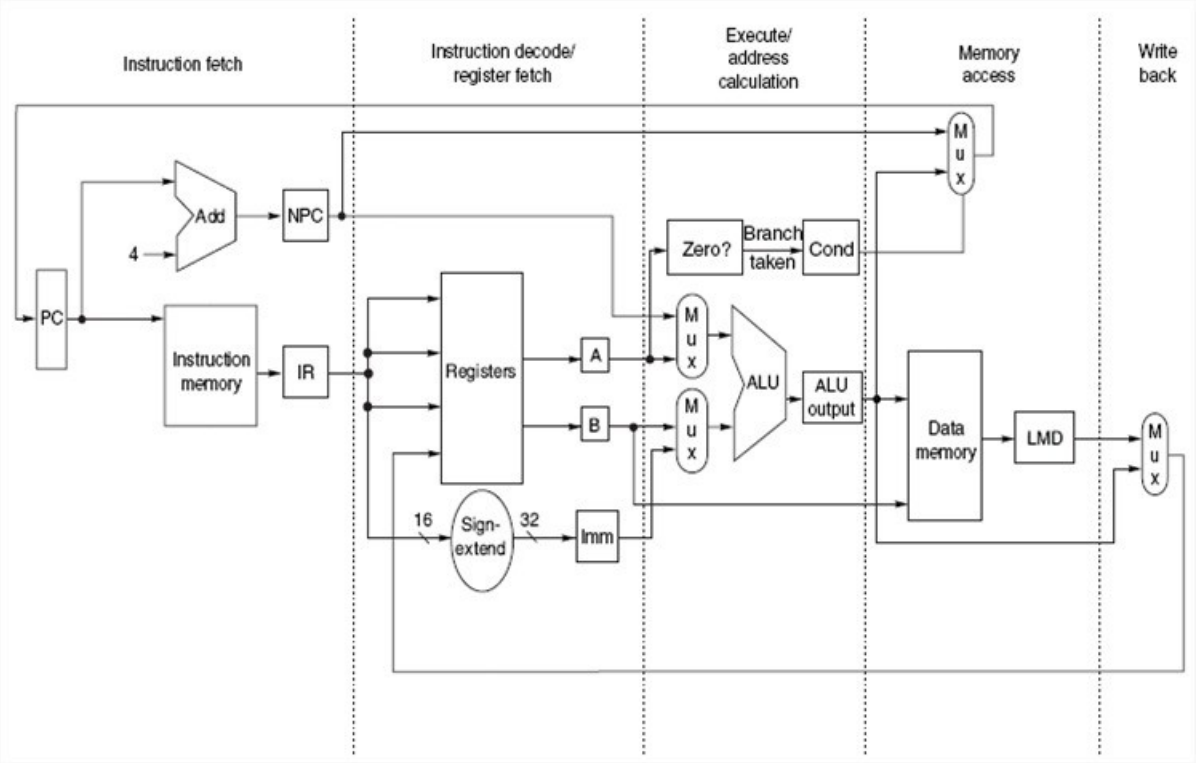
INTRODUCTION:



This is the Flow Chart of the 32- bitt pipe-lined MIPS verilog process from instructions set to pipelined output. Hazards solving contains forwarding, control unit.

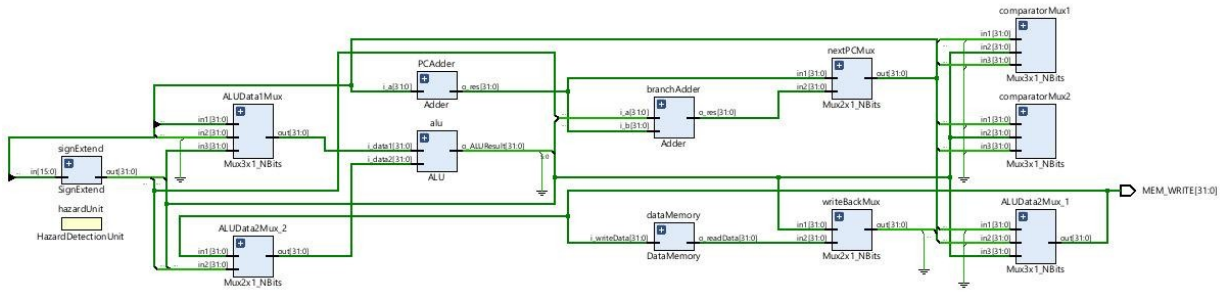
1. Instruction Memory for 32 32-bit MIPS instructions.
2. 32 32-bit Data Memory locations.
3. Instruction Memory consisting of arithmetic, logical, branch, jump, and memory-access instructions. Immediate arguments and argument registers are hard-coded.
4. TRAP destination is generally OS-specific, and has been left to zero here.
5. 5-stage pipelining; stages are:
   a) Instruction Fetch (IF)
   b) Instruction Decode (ID)
   c) Execute (EX)
   d) Memory Access (MEM)
   e) Writeback (WB)
6. Data Forwarding Unit to partially resolve hazards in R-type instructions.
7. Hazard Detection Unit to insert stalls (nop cycles) wherever required.

IMPLEMENTATION DETAILS :



Processor design of the 32-bit pipelined MIPS processor

Elaborated design



Elaborated design obtained using Vivado

Config.json file :

- Design files and clock declaration :

```
"DESIGN_NAME": "cpu",
"VERILOG_FILES": "dir::src/*.v",
"CLOCK_PORT": "clk",
"CLOCK_PERIOD": 10.0,
"PNR_SDC_FILE": "/home/yash/OpenLane/scripts/base.sdc",
"SIGNOFF_SDC_FILE": "/home/yash/OpenLane/scripts/base.sdc",
"//": "PDN",
"FP_PDN_VOFFSET": 5,
"FP_PDN_HOFFSET": 5,
"FP_PDN_VWIDTH": 2,
"FP_PDN_HWIDTH": 2,
"FP_PDN_VPITCH": 30,
"FP_PDN_HPITCH": 30,
"FP_PDN_SKIPTRIM": true,
"FP_PDN_CORE_RING":1,
"LEC_ENABLE":1,
"FP_SIZING":"absolute",
"CORE_AREA": "5 5 90 90",
"DIE_AREA": "0.0 0.0 100 100",
"FP_PDN_MULTILAYER": true,
"ROUTING_CORES":4,
"RUN_TAP_DECAP_INSERTION":true,
"//": "Technology-Specific Configs",
"pdk::sky130*": {
    "FP_CORE_UTIL": 45,
    "CLOCK_PERIOD": 10,
    "scl::sky130_fd_sc_hd": {
        "CLOCK_PERIOD": 8
    },
    "scl::sky130_fd_sc_ls": {
        "MAX_FANOUT_CONSTRAINT": 5
    }
}
```

- Floorplan sizing - This determines the specific die area and core area to be used in floorplanning when FP_SIZING is set to absolute.
- Diode Padding- It is used to specify the amount of extra space to be added around diode components during the layout phase of integrated circuit development.
- LEC check at every stage - This command performs logical verification at every stage using YOSYS. This results in an increase in runtime but helps in minute analysis.
- "PL_RANDOM_INITIAL_PLACEMENT" signals the use of randomized initial placement.
- "FP_PDN_VOFFSET" and "FP_PDN_HOFFSET" The offset of the vertical and horizontal power stripes on the metal layer 5 in the power distribution network "FP_PDN_VWIDTH" and "FP_PDN_HWIDTH" define the strap width for the vertical and horizantal layers used in PDN. .
- "FP_PDN_VPITCH" and "FP_PDN_HPITCH" The pitch of the vertical and horizantal power stripes on the metal layer 4 in the power distribution network.

These commands ensure efficient power distribution and optimal component placement.

- Core Utilization - This sets the core utilization to avoid routing congestion.
- Tap cells and Decap cells insertion - Tap cells serve as connection points for power and ground distribution in integrated circuits, ensuring stable voltage across the chip and reducing voltage drop. Decap cells, or decoupling capacitors, are strategically placed capacitors that reduce noise and voltage fluctuations by providing local charge reservoirs, improving signal integrity and preventing power supply droop during transient events.
- Core ring Insertion - Enables adding a core ring around the design. More details on the control variables in the pdk configurations documentation
- Technology specifications define a target core utilization of 45%. Additionally, it provides overrides for clock period constraints for specific libraries within the sky130 PDK, setting it to 8 time units for the high-speed (hs) library and specifying a maximum fanout constraint of 5 for the low-power (ls) library.
- SDC file :

```
if {[info exists ::env(CLOCK_PORT)] && $::env(CLOCK_PORT) != ""} {
    create_clock [get_ports $::env(CLOCK_PORT)]  -name $::env(CLOCK_PORT)  -period $::env(CLOCK_PERIOD)
} else {
    create_clock -name __VIRTUAL_CLK__ -period $::env(CLOCK_PERIOD)
    set ::env(CLOCK_PORT) __VIRTUAL_CLK__
}

set input_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
set output_delay_value [expr $::env(CLOCK_PERIOD) * $::env(IO_PCT)]
puts "\[INFO\]: Setting output delay to: $output_delay_value"
puts "\[INFO\]: Setting input delay to: $input_delay_value"

set_max_fanout $::env(MAX_FANOUT_CONSTRAINT) [current_design]
if { [info exists ::env(MAX_TRANSITION_CONSTRAINT)] } {
    set_max_transition $::env(MAX_TRANSITION_CONSTRAINT) [current_design]
}

set clk_input [get_port $::env(CLOCK_PORT)]
set clk_indx [lsearch [all_inputs] $clk_input]
set all_inputs_wo_clk [lreplace [all_inputs] $clk_indx $clk_indx ""]

#set rst_input [get_port resetn]
#set rst_indx [lsearch [all_inputs] $rst_input]
#set all_inputs_wo_clk_rst [lreplace $all_inputs_wo_clk $rst_indx $rst_indx ""]
set all_inputs_wo_clk_rst $all_inputs_wo_clk

# correct resetn
set_input_delay $input_delay_value  -clock [get_clocks $::env(CLOCK_PORT)] $all_inputs_wo_clk_rst
#set_input_delay 0.0 -clock [get_clocks $::env(CLOCK_PORT)] {resetn}
set_output_delay $output_delay_value  -clock [get_clocks $::env(CLOCK_PORT)] [all_outputs]

if { ![info exists ::env(SYNTH_CLK_DRIVING_CELL)] } {
    set ::env(SYNTH_CLK_DRIVING_CELL) $::env(SYNTH_DRIVING_CELL)
}

if { ![info exists ::env(SYNTH_CLK_DRIVING_CELL_PIN)] } {
    set ::env(SYNTH_CLK_DRIVING_CELL_PIN) $::env(SYNTH_DRIVING_CELL_PIN)
}

set_driving_cell -lib_cell $::env(SYNTH_DRIVING_CELL) -pin $::env(SYNTH_DRIVING_CELL_PIN) $all_inputs_wo_clk_rst
set_driving_cell -lib_cell $::env(SYNTH_CLK_DRIVING_CELL) -pin $::env(SYNTH_CLK_DRIVING_CELL_PIN) $clk_input

# fF -> pF
set cap_load [expr $::env(OUTPUT_CAP_LOAD) / 1000.0]
puts "\[INFO\]: Setting load to: $cap_load"
set_load  $cap_load [all_outputs]
```

RESULTS AND DISCUSSION :

```
53. Printing statistics.

=== cpu ===

   Number of wires:                201
   Number of wire bits:            418
   Number of public wires:           9
   Number of public wire bits:     226
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                416
     $_MUX_                         32
     $_NOT_                        160
     sky130_fd_sc_hd__dfxtp_2      224
```

```
61. Printing statistics.

=== cpu ===

   Number of wires:                440
   Number of wire bits:            471
   Number of public wires:         195
   Number of public wire bits:     226
   Number of memories:               0
   Number of memory bits:            0
   Number of processes:              0
   Number of cells:                469
     sky130_fd_sc_hd__and2b_2       32
     sky130_fd_sc_hd__buf_1         53
     sky130_fd_sc_hd__dfxtp_2      224
     sky130_fd_sc_hd__inv_2        160

   Chip area for module '\cpu': 5844.355200
S
```

Power consumption summary post synthesis :

```
 report_power
======================== Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.92e-09   1.12e-03  64.0%
Combinational          1.96e-06   9.81e-07   2.34e-10   2.94e-06   0.2%
Clock                  1.87e-04   4.38e-04   7.01e-10   6.24e-04  35.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------
Total                  1.30e-03   4.38e-04   2.85e-09   1.74e-03 100.0%
                          74.8%      25.2%       0.0%
```

Post-synthesis sta :

```
report_tns
tns 0.00

report_wns
wns 0.00

report_worst_slack -max (Setup)
worst slack 1.51

report_worst_slack -min (Hold)
worst slack 0.08
```

Area utilization post floorplanning :

Die area : 16,965 sq um

3-initial_fp_die_area.rpt

```
0.0 0.0 125.0 135.72
```

Core area : 12,670.92 sq um

3-initial_fp_core_area.rpt

```
5.52 10.88 119.14 122.4
```

Area utilized : 74.68 %

Post global placement sta :

13-gpl_sta.summary.rpt

```
****************************************
report_tns
****************************************
tns 0.00

****************************************
report_wns
****************************************
wns 0.00

****************************************
report_worst_slack -max (Setup)
****************************************
worst slack 1.40

****************************************
report_worst_slack -min (Hold)
****************************************
worst slack 0.08
```

Post detailed placement sta :

18-dpl_sta.summary.rpt

```
****************************************
report_tns
****************************************
tns 0.00

****************************************
report_wns
****************************************
wns 0.00

****************************************
report_worst_slack -max (Setup)
****************************************
worst slack 1.35

****************************************
report_worst_slack -min (Hold)
****************************************
worst slack 0.08
```

Post global placement power consumption :

13-gpl_sta.power.rpt

```
****************************************
 report_power
****************************************
====================== Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.92e-09   1.12e-03  64.0%
Combinational          1.96e-06   1.36e-06   2.34e-10   3.32e-06   0.2%
Clock                  1.87e-04   4.38e-04   9.67e-10   6.24e-04  35.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------
Total                  1.30e-03   4.39e-04   3.12e-09   1.74e-03 100.0%
                          74.8%      25.2%       0.0%
```

Post detailed placement power consumption :

18-dpl_sta.power.rpt

```
====================================================================================
 report_power
====================================================================================
======================== Typical Corner ===========================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.80e-09   1.12e-03  64.0%
Combinational          2.50e-06   1.74e-06   4.47e-10   4.25e-06   0.2%
Clock                  1.87e-04   4.38e-04   9.67e-10   6.24e-04  35.7%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------------------
Total                  1.31e-03   4.39e-04   3.22e-09   1.75e-03 100.0%
                          74.8%      25.2%       0.0%
```

Post clock tree synthesis sta :

20-cts_sta.summary.rpt

```
====================================================================================
report_tns
====================================================================================
tns 0.00

====================================================================================
report_wns
====================================================================================
wns 0.00

====================================================================================
report_worst_slack -max (Setup)
====================================================================================
worst slack 1.35

====================================================================================
report_worst_slack -min (Hold)
====================================================================================
worst slack 0.08
```

Post clock tree synthesis power consumption :

20-cts_sta.power.rpt

```
====================================================================================
 report_power
====================================================================================
======================== Typical Corner ===========================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.80e-09   1.12e-03  33.6%
Combinational          2.50e-06   1.79e-06   4.47e-10   4.29e-06   0.1%
Clock                  1.52e-03   6.85e-04   1.74e-09   2.21e-03  66.3%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------------------------
Total                  2.64e-03   6.87e-04   3.99e-09   3.33e-03 100.0%
                          79.4%      20.6%       0.0%
```

Post global routing sta :

32-grt_sta.summary.rpt

```
================================================================================
report_tns
================================================================================
tns 0.00

================================================================================
report_wns
================================================================================
wns 0.00

================================================================================
report_worst_slack -max (Setup)
================================================================================
worst slack 0.93

================================================================================
report_worst_slack -min (Hold)
================================================================================
worst slack 0.08
```

Post global routing power consumption :

32-grt_sta.power.rpt

```
================================================================================
 report_power
================================================================================
======================== Typical Corner ===================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power (Watts)
----------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.81e-09   1.12e-03  33.6%
Combinational          2.51e-06   1.16e-06   1.19e-09   3.67e-06   0.1%
Clock                  1.52e-03   6.85e-04   1.74e-09   2.21e-03  66.3%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  2.64e-03   6.86e-04   4.74e-09   3.33e-03 100.0%
                          79.4%      20.6%       0.0%
```

Multi-corner sta report :

```
================================================================================
report_tns
================================================================================
tns -9.25

================================================================================
report_wns
================================================================================
wns -0.94

================================================================================
report_worst_slack -max (Setup)
================================================================================
worst slack -0.94

================================================================================
report_worst_slack -min (Hold)
================================================================================
worst slack -0.03
```

Overall power consumption for multi-corners:

```
================================================================================
 report_power
================================================================================
======================== Fastest Corner ========================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power  (Watts)
----------------------------------------------------------------
Sequential             1.31e-03   0.00e+00   3.30e-09   1.31e-03  28.9%
Combinational          2.96e-06   3.23e-06   4.09e-09   6.20e-06   0.1%
Clock                  1.83e-03   1.39e-03   5.61e-09   3.22e-03  70.9%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  3.15e-03   1.39e-03   1.30e-08   4.54e-03 100.0%
                          69.3%      30.7%       0.0%
======================== Slowest Corner ========================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power  (Watts)
----------------------------------------------------------------
Sequential             8.60e-04   0.00e+00   3.05e-06   8.63e-04  28.2%
Combinational          2.02e-06   2.07e-06   1.39e-06   5.47e-06   0.2%
Clock                  1.27e-03   9.16e-04   2.01e-06   2.19e-03  71.6%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  2.13e-03   9.18e-04   6.45e-06   3.06e-03 100.0%
                          69.7%      30.0%       0.2%
======================== Typical Corner ========================================

Group                  Internal  Switching    Leakage      Total
                          Power      Power      Power      Power  (Watts)
----------------------------------------------------------------
Sequential             1.12e-03   0.00e+00   1.81e-09   1.12e-03  29.1%
Combinational          2.54e-06   2.68e-06   1.19e-09   5.22e-06   0.1%
Clock                  1.54e-03   1.18e-03   2.07e-09   2.72e-03  70.8%
Macro                  0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
Pad                    0.00e+00   0.00e+00   0.00e+00   0.00e+00   0.0%
----------------------------------------------------------------
Total                  2.66e-03   1.18e-03   5.06e-09   3.84e-03 100.0%
                          69.3%      30.7%       0.0%
```

Here, "fastest," "slowest," and "typical" corners refer to specific combinations of process, voltage, and temperature variations that represent extreme and typical operating conditions for integrated circuits.

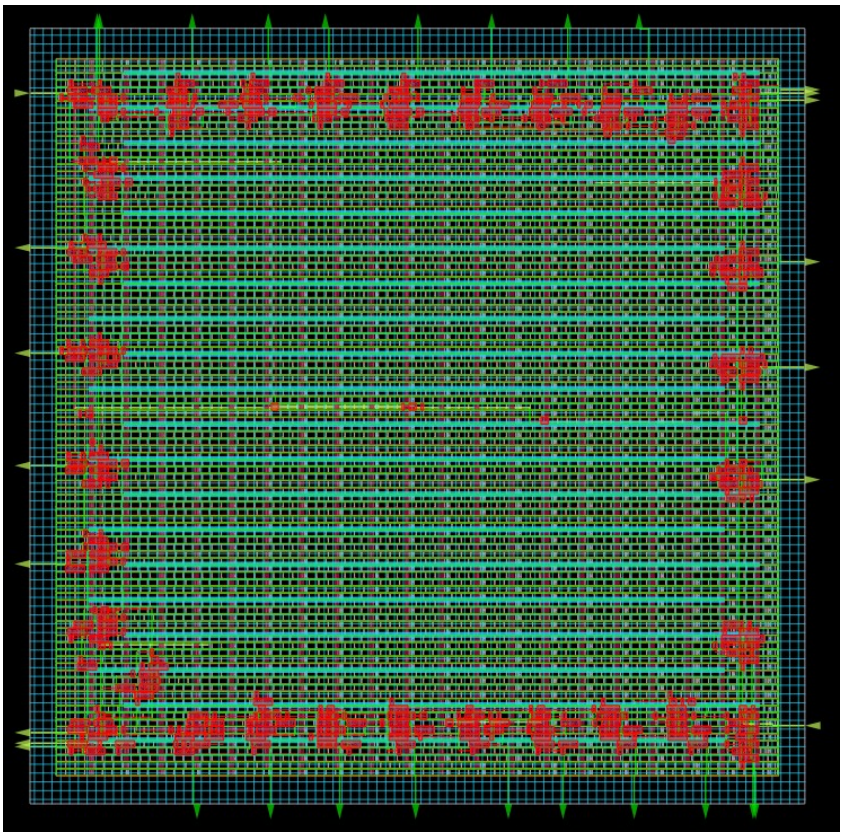
LVS report :

```
LVS reports no net, device, pin, or property mismatches.

Total errors = 0
```

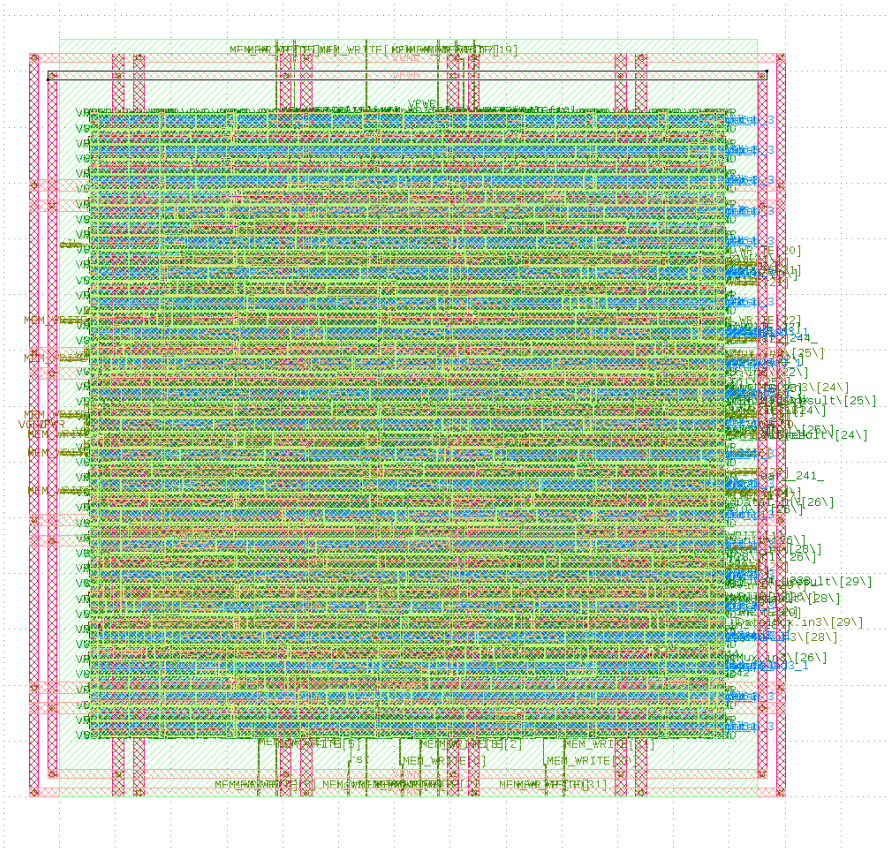
Openroad gcd_sky130hd.tcl file:

```
# gcd flow pipe cleaner
source "helpers.tcl"
source "flow_helpers.tcl"
source "sky130hd/sky130hd.vars"

set synth_verilog "synth_cpu_1.v"
set design "cpu"
set top_module "cpu"
set sdc_file "gcd_sky130hd.sdc"
set die_area {0 0 299.96 300.128}
set core_area {9.996 10.08 289.964 290.048}

source -echo "flow.tcl"
```

Layout using openroad viewer:



GDSII file using Klayout :



CONCLUSION :

The area required to make a chip is 5845 units. There are no setup or hold time violations for this chip. The power consumption is between 3mW an 4.55mW.

REFERENCES :

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[4] https://www.fpga4student.com/2017/06/32-bit-pipelined-mips-processor-in-verilog-1.html
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[7] G. K. Dewangan, G. Prasad and B. C. Mandi, "Design and Implementation of 32 bit MIPS based RISC Processor", 2021 8th International Conference on Signal Processing and Integrated Networks (SPIN), pp. 998-1002, 2021.