**5E5101** 

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Total No of Pages:

5E5101

B. Tech V Sem. (Main/Back) Exam. Nov-Dec. 2015
Computer Science & Engineering
5CS1A Computer Architecture
Common with IT

Time: 3 Hours

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Maximum Marks: 80

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

## Instructions to Candidates:

Roll No.

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. NIL

2. <u>NIL</u>

## <u>UNIT-I</u>

Q.1 (a) Explain Flynn's classification with suitable examples.

[8]

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(b) Explain direct and indirect register addressing modes with suitable examples. [8]

**OR** http://www.rtuonline.com

Q.1 (a) Explain basic design of a simple computer system.

[8]

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(b) Is there any difference among software, hardware & firmware? Explain.

[8]

## <u>UNIT-II</u>

1.2 (a) Is there any difference between RISC & CISC computers? Explain.

[8]

(b) What is the advantage of pipelining? Explain instruction pipeline in detail.

[8]

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_			<u>OR</u>		
	Q.2	(a) What do you understand by speedup and efficiency? What are bottlenecks?			
La Partie			Explain.	[8]	
r		(b)	Explain arithmetic pipeline with a suitable example. Draw diagram also.	[8]	
		_	<u>UNIT-III</u>		
http://www.rtuonline.com	Q.3	(a)	Explain array multiplier with a suitable example.	[8]	http:/
		<b>(b)</b>	Explain stack organization of Central Processing Unit.	[8]	
			<u>OR</u>		www.rtuonlin
	Q.3	Multiply and steps of $(-37) \times (21)$ multiplication are to be shown using			v.rtu
		mul	tiplier algorithm.	[16]	onli
					ne.com
	Q.4	Des	ign 4×3 RAM. Also explain basic cell.	[16]	m
			<u>OR</u>		
	Q.4	Wha	at are the 3 different cache memory schemes? Explain in detail with su	itable	
		examples.		[16]	
ww.rtuonline.		<u>UNIT-V</u>			
	Q.5	Write short notes on -			http://www.rtuon
		(a)	IOP	[8]	ww.
		(b)	DMA	[8]	rtuo
	<u>OR</u>				=
	Q.5	Write short notes on			ne.com
		(a)	Priority interrupts	[8]	3
		(b)	I/O Interface.	[8]	
A. A.					

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