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B.TECH. VI SEM MAIN/BACK EXAM AUGUST 2023

COMPUTER SCIENCE AND ENGINEERING

(6CS4-04) - COMPUTER ARCHITECTURE AND ORGANIZATION

COMMON WITH CSE & IT, CSE(AI&ML),CSE(DS)

Time : 3 Hours]

[Max. Marks : 120

[Min. Passing Marks :

Instructions to Candidates : Part – A : Short answer type questions (up to 25 words) 10 × 2 marks = 20 marks. All ten questions are compulsory.

Part – B: Analytical/Problem Solving questions 5 × 8 marks = 40 marks. Candidates have to answer 5 questions out of 7.

Part – C: Descriptive/Analytical/Problem Solving questions 4 × 15 marks = 60 marks. Candidates have to answer 4 questions out of 5.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting materials is permitted during examination. (Mentioned in form No. 205)

1_____ 2_____

PART A

Q. 1. Describe the purpose of the buffer gate in the clock input of a register. [2]

Q. 2. Differentiate computer organization and computer architecture. [2]

Q. 3. Describe the purpose of buffer gate. [2]

Q. 4. Differentiate instruction code and operation code. [2]

Q. 5. Differentiate memory reference and register reference computer instructions. [2]

Q. 6. What is the difference between a direct and an indirect address instruction ? [2]

Q. 7. What are the two instructions needed in the basic computer in order to set the E flip-flop to 1 ? [2]

Q. 8. Differentiate between assembly language and machine language. [2]

Q. 9. Show how the MRI and non-MRI tables can be stored in memory. [2]

Q. 10. Explain the difference between hardwired control and microprogrammed control. [2]

PART B

Q. 1. Draw the block diagram of a dual 4-to-1-line multiplexers and explain its operation by means of a function table. [8]

Q. 2. Represent the following conditional control statement by two register transfer statements with control functions. [8]

If (P = 1) then (RI ← R2) else If (Q= 1) then (RI ← R3)

Q. 3. Draw a timing diagram assuming that SC is cleared to 0 at time T3 if control signal C_7 is active. [8]

C_7T_3 : SC → 0

C_7 is activated with the positive clock transition associated with T_7.

Q. 4. An output program resides in memory starting from address 230. It is executed after the computer recognizes an interrupt when FGO becomes a 1 (while IEN = 1). [8]

(a) What instruction must be placed at address 1 ?

(b) What must be the last two instructions of the output program ?

Q. 5. The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields: an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of 60 processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the in instruction is in one memory word. [8]

Q. 6. How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is (a) a computational type requiring an operand from memory; (b) a branch type. Explain with the help of an example. [8]

Q. 7. Write the RISC I instruction in assembly language that will cause a jump to address 3200 if the Z (zero) status bit is equal to 1. [8]

(a) Using immediate mode

(b) Using a relative address mode (assume that PC = 3400)

PART C

Q. 1. An instruction at address 021 in the basic computer has I = 0, an operation code of the AND instruction, and an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand B8F2 and the content of AC is A937. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR. Repeat the problem three more times starting with an operation code of another memory-reference instruction. [15]

Q. 2. Write a program to evaluate the arithmetic statement : [15]

$$X = \frac{A - B + C * (D * E - F)}{G + H * K}$$

(a) Using a general register computer with three address instructions.

(b) Using a general register computer with two address instructions.

(c) Using an accumulator type computer with one address instructions.

(d) Using a stack organized computer with zero-address operation instructions.

Q. 3. Give an example of a RISC I instructions that will perform the following operations : [15]

(a) Decrement a register

(b) Complement a register

(c) Negate a register

(d) Clear a register to 0

(e) Divide a signed number by 4

(f) No operation.

Q. 4. Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment. [15]

Q. 5. How many characters per second can be transmitted over a 1200-baud line in each of the following modes ? (Assume a character code of eight bits.) [15]

(a) Synchronous serial transmission.

(b) Asynchronous serial transmission with two stop bits.

(c) Asynchronous serial transmission with one stop bit.

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