5E5101

Roll No. _____ Total No of Pages: 3

5E5101

B. Tech. V Sem. (Main / Back) Exam., Dec. 2014

Computer Science & Engineering

5CS1A Computer Architecture

Common with CS IT

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q. 1 (a) Explain Flynn classification of computer architecture based on streams. [8]

(b) Write 3 different types of shift micro-operations in Register Transfer Language.[8]

OR

(a) Explain bus transfer micro operation. Write it in Register Transfer Language. [8]

(b) Explain the concept of Von-Neuman Architecture. [8]

UNIT – II

Q. 2 (a) Design a 4 bit ALU. [8]

(b) Draw reservation table for 10 instructions. Also explain the instruction pipeline stages. [8]

OR

(a) Explain speedup, efficiency and throughput in pipelining. [8]

(b) Is there any difference in RISC & CISC architectures? Explain. [8]

UNIT – III

Q. 3 (a) Multiply 10101 & 11011 using Booth multiplier algorithm. Show the steps. [8]

(b) Describe the working of Carry Save Adder. rtuonline.com [8]

OR

(a) Divide 0100100001 by 11001 using restoring division algorithms. Show the steps. [8]

(b) How will you subtract 2 floating point numbers? Explain with an example. [8]

UNIT – IV

Q. 4 (a) Design a 16 by 4 RAM. Explain binary cell also. [16]

OR

Write short notes on any two: [8x2=16]

(a) Associative memory

(b) Segmentation

(c) LRU page replacement policy.

UNIT – V

Q. 5 (a) What are the various modes of data transfer to and from the computers system? Explain. [8]

(b) Explain the I/O interface for a pen drive. [8]

OR

Write short notes on any two: [8x2=16]

(a) Input Output Processor

(b) DMA

(c) Priority Intercept.
