5E5101

Roll No. _____ Total No of Pages: 3

5E5101

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Computer Science & Engineering
5CS1A Computer Architecture
Common with CS, IT

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Write down the Flynn's classification of computer? [8]

(b) What does pipeline, vector and array processor mean in parallel processing? [8]

OR

Q.1 (a) Describe the Von – Neumann model and explain the functioning of its components. [8]

(b) Explain and draw a diagram of a bus system that use multiplex k, register of n bits each to produce an n – line common bus. [8]

UNIT – II

Q.2 (a) Explain the following in detail: [8]

(i) Address Sequencing

(ii) Hardwired control unit

(b) Draw and explain the organization of a CPU showing the connections between the Register to a common bus. [8]

OR

Q.2 (a) Discuss all factor which affect the performance of pipelining processor based systems. [8]

(b) A non- pipeline system takes 100 ns to process a task. The same task can be processed in a six- segment pipeline with a clack cycle of 20ns. Determine the speedup ratio of the pipeline for 200 tasks. What is maximum speedup that can be achieved? [8]

UNIT – III

Q.3 (a) Describe the procedure for addition and subtraction for fixed point number. Explain by use of Flowchart? [8]

(b) Explain Booth multiplication algorithm and its hardware. [8]

OR

Q.3 (a) Draw and explain flowchart for additional and subtraction of floating points number. [8]

(b) Represent the number (+46.5) 10 as a floating point binary number with 24 bits. The normalized fraction Mantissa has 16 bits and be exponent has 8 bits. [8]

UNIT – IV

Q.4 (a) What is cache coherency why is it necessary? Explain different approaches for cache coherency. [8]

(b) Explain associative memory with its hardware organization. Discuss the procedure for reading and writing data in associative memory. [8]

OR

Q.4 (a) Explain the role of virtual Memory. [8]

(b) Draw and explain the memory hierarchy in a digital computer. What are the advantages of cache memory over main memory? [8]

UNIT – V

Q.5 (a) List various commands that an interface may receive from control line of the Bus. Explain the process of handling an interrupt that occurs during the execution of a program, with the help of an example. [8]

(b) A DMA controller transfer 16- bits words to memory using cycle stealing. The words are assembled from a device that transmits character at a rate of 2400 characters per second. The CPU be is fetching and executing instruction at an average rate of 1 million instructions per second. By how much the CPU be slowed down because of the DMA transfer? [8]

OR

Q.5 (a) What is an interrupt service subroutine? How can the interrupt priority be resolved?

(b) Explain in short programmed I/O and interrupt initiated I/O.

(c) What do you mean by synchronous and asynchronous data transfer? Explain hand shaking method asynchronous data transfer? [16]
