5E5101

Roll No.

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B. Tech. (Sem. V) (Mercy Back) Examination, November 2012
Computer Sc. & Engineering
5CS1A Computer Architecture (CS, IT)

Time : 3 Hours

Maximum Marks : 70
Min. Passing Marks : 24

*Attempt any **five** questions, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) If a computer has 128 operation codes and 512 K addresses, how many bits would be required for

(i) Single address instruction

(ii) Two address instruction

6

(b) What is instruction ? What are different parts of instruction ? Explain the significance of each part of instruction with an example.

6

(c) What do you mean by instruction set completeness ?

4

OR

1

1 (a) Explain the following terms with reference to Von-neumann machines :

(i) SISD

(ii) SIMO

(iii) MISD

(iv) MIMO 8

(b) A digital computer has a common bus system for 16 registors of 32 bit each. The bus is constructed with multiplexers.

(i) How many selection input are there in each multiplexers ?

(ii) What size of multiplexer are needed ?

(iii) How many multiplexers are there in the bus ? 8

UNIT - II

2 (a) Explain the following in detail :

(i) Address sequencing

(ii) Hardwired control unit 8

(b) Draw and explain the organization of CPU showing the connections between the register to a common bus. 8

OR

2 (a) Explain speed up, efficiency and throughout in pipelining. 8

(b) Is there any different in RISC and CISC architecture ? Explain. 8

UNIT - III

3 (a) Explain Array Mutiplier with a suitable example. 8

(b) Explain stack organization of central processing unit. 8

OR

3 Multiply and steps of (–37) × (21) multiplication are to be shown using Booth multiplier algorithm. 16

UNIT - IV

4 (a) Construct a memory system having static 1k ×4 RAM. How many such RAMs will be required to

(i) Construct 1k ×8 RAM bank ?

(ii) 4k×4 RAM memory bank ? Show the block diagram and the address decoding circuit. 10

(b) Write short note on : Virtual memory. 6

OR

4 (a) What is cache coherency ? Why it is necessary ? Explain different approaches for coche coherency. 8

(b) Explain Associative memory with its hardware organization. Discuss the procedure for reading and writing data in associative memory. 8

UNIT - V

5 (a) Design a parallel priority interrup hardware for a aystem with eight interval sources.

8

(b) Why does DMA have priority over the CPU when both request a memory transfer ?

8

OR

5 Write short note on :

(a) Priority Interrupts

(b) I/O Interface.

2×8=16