

## 16x16 Booth Encoded Wallace Tree Multiplier

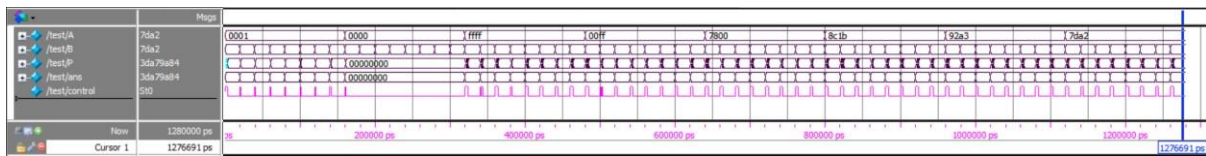
The unit gate delays and areas are given in Table 1. Depending on these unit magnitudes the delay and area of the designed multiplier are given in the table also.

The transient simulation results are given in Figure 1. “control” signal is defined to see any differences between expected and measured product values.

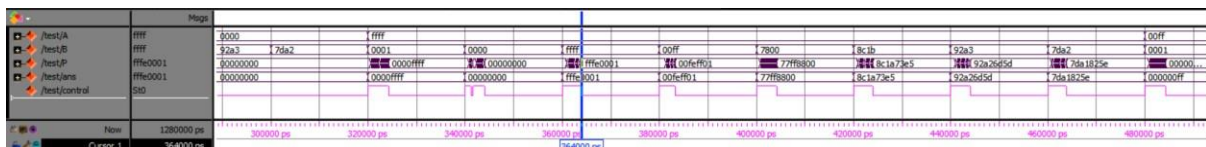
In the appendix the multiplier scheme is given. In the first stage partial products are generated and regulated in a triangular shape. In the next stages the tree is reduced using half and full adders and in the last stage the remaining two rows are added using Kogge Stone adder.

**Table 1.** The area and delay assumptions and measurements

Type	Area	Delay
AND	1	0.1ns
OR	1	0.1ns
XOR	1	0.2ns
Depending on the assumptions above		
32bit Booth-Wallace Multiplier	2181	4ns (40 unit delay)



a)



b)

**Figure 1.** Transient simulation results of the Booth encoded Wallace tree multiplier b) zoomed.

## APPENDIX: Booth Wallace Tree Operations

Height increase due to carry from previous stage												Half adder								Full Adder								Unchanged						
W0	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
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W1	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
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