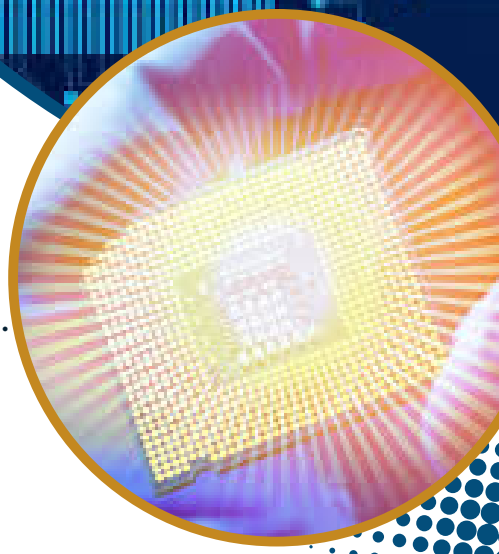
EE-926
SYSTEM VALIDATION COURSE
@ NUST COLLEGE OF EME

KICKSTART YOUR CAREER IN DESIGN VERIFICATION



Pakistan's booming semiconductor industry highly demands skilled verification engineers. EE-926 System Validation course can be your launchpad to a successful career in this field at time when Asia and MENA regions are investing highly into this field.

1 IN-DEMAND CONTENT

Key Topics:
regression analysis, code coverage, constraint-based verification, formal methods, assertion-based verification, and transaction-level modeling.

2 HANDS-ON TRAINING

Develop testbenches using the industry-standard Universal Verification Methodology (UVM). Write resuable testbenches using UVM facatory and config DB.

3 REAL WORLD APPLICATION

Tackle complex and real-world design challenges with practical insights.

About the Instructor:
Dr. Muhammad Yasin
Assistant Professor, DCSE Deptt.
NUST College of EME
PhD Electrical Engg., NYU
MS Microsystems Engg., Masdar Institute
Research Focus: Hardware Security

Students who can benefit the most:
EE, CE, and CS students who have good familiarity with digital logic design and object oriented programming.
Venue: CRC-16, DC&SE Deptt, NUST College of EME
Timing: Fridays, 1800-2100 hrs

Course outline link: https://github.com/yasinnyu/systemvalidation

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