National University of Sciences & Technology (NUST)
College of Electrical and Mechanical Engineering (CEME)
Department of Computer & Software Engineering (DC&SE)

System Validation

Course Code:	EE926	**Semester:**	Fall 2024
Credit Hours:	3	**Prerequisite Codes:**	Digital Logic Design, Object Oriented Programming
Instructor:	Dr. Muhammad Yasin	**Class:**	MS/PhD
Office:	DCE-21 (First Floor)	**Telephone:**	03049111410
Lecture Days:	Friday (6-9 PM)	**E-mail:**	m.yasin@ceme.nust.edu.pk
Class Room:	**CRC-XYZ**	**Consulting Hours:**	Friday Before the Class or Email

Course Objectives:

Pakistan's semiconductor industry is steadily growing, creating increasing demand for skilled verification engineers. Ensuring the accuracy of chip designs before production is crucial to prevent costly mistakes. This course provides a solid foundation in verification and validation. Students will learn essential techniques like stimulus generation, testbench development, and regression analysis. To address complex design challenges, the course covers advanced topics such as constraint-based verification, formal methods, assertion-based verification, and transaction-level modeling. Hands-on training on developing testbenches according to the industry standard Universal Verification Methodology (UVM) is a core component of the course; this skill is in high demand in Pakistan's semiconductor industry.

Grading	Distribution
Mid Term	30%
Final	30%
Assignments (4-6)	10%
Quizzes (4-6)	10%
Project	20%
Total	100%

Books:

Text Book:

1. SystemVerilog For Verification: A Guide to Learning the Testbench Language Features By CHRIS SPEAR Synopsys, Inc.
2. ASIC/SoC Functional Design Verification, A Comprehensive Guide to Technologies and Methodologies. By Ashok B. Mehta

Reference Books:

1. UVM Cookbook, Verification Methodology Online Cookbook By Siemens Verificaiton Academy (formerly Mentor Graphics Verification Academy)

Topics to be Covered:

Background Knowledge (Chip design and manufacturing ecosystem)

Verification basics:

- Verification Plan
- Verification Strategies and Environments
- Stimuli Generation, Test Bench Structures

- Regression Analysis
- Simulation Based Verification
- Constraint Based Verification, Code Coverage

Verification methods:

- Formal Methods
- Assertion Based Verification
- Model Checking
- Equivalence Checking
- Embedded Software Verification

Deploying Industry-standard Verification:

- Introduction to System Verilog
- Use of Object-Oriented Programming in Verification
- Introduction UVM
- UVM Testbench Architecture
- UVM Phases and UVM Config DB
- UVM Driver, Monitor, Scoreboard, Agent, Sequencer, Sequences
- Case studies on developing Verification IP

Lecture Breakdown:

Week No.	Topics	Assessments
	Part 1 Fundamentals	
1	Introduction to Semiconductor Ecosystem	
	Need for Verification, Verification and Validation	
2	Stimulus Generation	
	Regression Analysis	
3	Introduction to System Verilog	
4	Constraint based Verification	
5	Code Coverage	
	Part 2 Methods	
6	Assertion based Verification (in System Verilog)	
7	Formal Methods, Model Checking	
8	Equivalence Checking	
	Mid Term Exam	
	Part 3 Deployment	
9	Introduction to UVM	
10	UVM Test Bench Hierarchy	

11	UVM Test Bench Components	
12	UVM Phases	
13	UVM Factory and Config DB	
14	Virtual Interfaces and Ports	
15	Transaction Level Modelling	
16	UVM IP Case Study 1	
17	UVM IP Case Study 2	
	End Semester Exam (ESE)	

Assignments

Assign 01:	.....
Assign 02:	.....
Assign 03:	.....
Assign 04:	.....

Grading Policy:

Quiz Policy:	The quizzes will be unannounced and normally last for five-ten minutes. The question framed is to test the concepts involved in last few lectures. Number of quizzes that will be used for evaluation is at the instructor's discretion. Grading for quizzes will be on a fixed scale of 0 to . A score of 5 indicates an exceptional attempt towards the answer and a score of 1 indicates your answer is entirely wrong but you made a reasonable effort towards the solution. Scores in between indicate very good (4), good (3), satisfactory (2), and poor (1) attempt. Failure to make a reasonable effort to answer a question scores a 0.
Assignment Policy:	In order to develop a comprehensive understanding of the subject, assignments will be given. Late assignments will not be accepted / graded. All assignments will count towards the total (No 'best-of' policy). The students are advised to do the assignment themselves. Copying assignments is highly discouraged and violations will be dealt with severely by referring any occurrences to the disciplinary committee. The questions in the assignment are meant to be challenging to give students confidence and extensive knowledge about the subject matter and enable them to prepare for the exams.
Plagiarism:	NUST CEME maintains a zero-tolerance policy towards plagiarism. While collaboration in this course is highly encouraged, you must ensure that you do not claim other people's work/ ideas as your own. Plagiarism occurs when the words, ideas, assertions, theories, figures, images, programming codes of others are presented as your own work. You must cite and acknowledge all sources of information in your assignments. Failing to comply with the NUST CEME plagiarism policy will lead to strict penalties including zero marks in assignments and referral to the academic coordination office for disciplinary action.

Tools / Languages/Software Requirement:

- EDA Playground
- Modelsim (optional)
- SystemVerilog
- MiniSAT /PycoSAT solver
- EMBC Model Checker