Modified Simple As Possible Computer Design

Block Diagram Control Signal Description:-

SL no	Control Signal	Description
1	Cp	Count Enable for Program Counter
2	Ep	Output Enable for Program Counter
3	Lp	Load Enable for Program Counter
4	Jp	Conditional Jump Enable for Program Counter
5	Lm	Load MAR
6	RE	Read from RAM
7	WE	Write into RAM
8	Sn	Input from Hex Keypad Enable
9	Ein	Output Enable for Hex-Keypad
10	Li	Load Instruction Register
11	INC	Increment Stack Pointer
12	DEC	Decrement Stack Pointer
13	Es	Output Enable for Stack Pointer
14,15	T1, T0	Temporary Register Operation Control
16	ST	BUS and Temporary Register Buffer Control
17,18,19	A0, A1, A2	ALU Operation Control
20	La	Load Enable for A Register
21	Ea	Output Enable for A Register
22	Lb	Load Enable for B Register
23	Eb	Output Enable for B Register
24	Lo	Load Enable for Output Register

Temporary Register Control Operation:-

T1	T0	Description
0	0	Load Enable for Upper Byte
0	1	Load Enable for Lower Byte
1	0	Output Enable to Upper Byte
1	1	Output Enable to Lower Byte