Modified Simple As Possible Computer (MSAP-2015) Design

1. I have written my control word in order that can do execution cycle first and then fetch cycle for next instruction. There is a boot cycle for the fetch of first instruction. I have used this method to avoid extra NOP state after each instruction or other complex circuity. Whenever any of instruction is executed successfully then controller/sequencer do the fetch cycle for the next instruction and then do the next execution cycle.
2. Here I have used 16 bit up counter for the 64 Kbytes of main memory (RAM) support. I used cascaded four 4-bit up counter. Moreover, I have started my STACK POINTER from the address FF00h. So, there is a logic circuit for reset synchronization if my program counter exceeds this address.
3. Here I have used 128 Kbytes RAM. As PROTEUS does not have any 64 Kbytes RAM which I have required. So, I used 128 Kbytes RAM and the MSM is grounded to use it as 64 Kbytes memory support. Here I have used different counter and ROM for the auto loading of the program into RAM.
4. I have used my STACK POINTER from the address FF00h. So, my upper two bytes for the STACK POINTER is fixed. I have reduced two up-down counter ICs here. My stack memory is 256 bytes.
5. I have used both the clock edge in this design. Negative edge is used for the control word and positive edge is used for the loading in the register. So, each clock pulse synchronization is done correctly.
6. In schematics there are three options for simulation. Full run, single instruction and single T state run can be possible by selecting proper switch in control panel (see user manual).
7. There are two different clocks for program loading and main program running. To change the program loading frequency you have to go the child sheet of the RAM and for changing simulation frequency you have to go to the child sheet of clock sub-circuit.
8. Each blocks output are shown in BCD display in the schematics. You can easily see the accuracy of running program step by step by seeing this values.
9. There are some sample codes and outputs snapshots in Test Code and Output folder.
10. Each .bin file and control word excel file and ICs excel file is provided with the main folder.