

Solving combinational design problems

- **Step 1: Understand the problem**
 - Identify the inputs and outputs
 - Draw a truth table
- **Step 2: Simplify the logic**
 - Draw a K-map
 - Write a simplified
 - Boolean expression SOP or POS
 - Use don't cares
- **Step 3: Implement the design**
 - Logic gates and/or Verilog
 - Run on FPGA board

To Do in these lab hour:

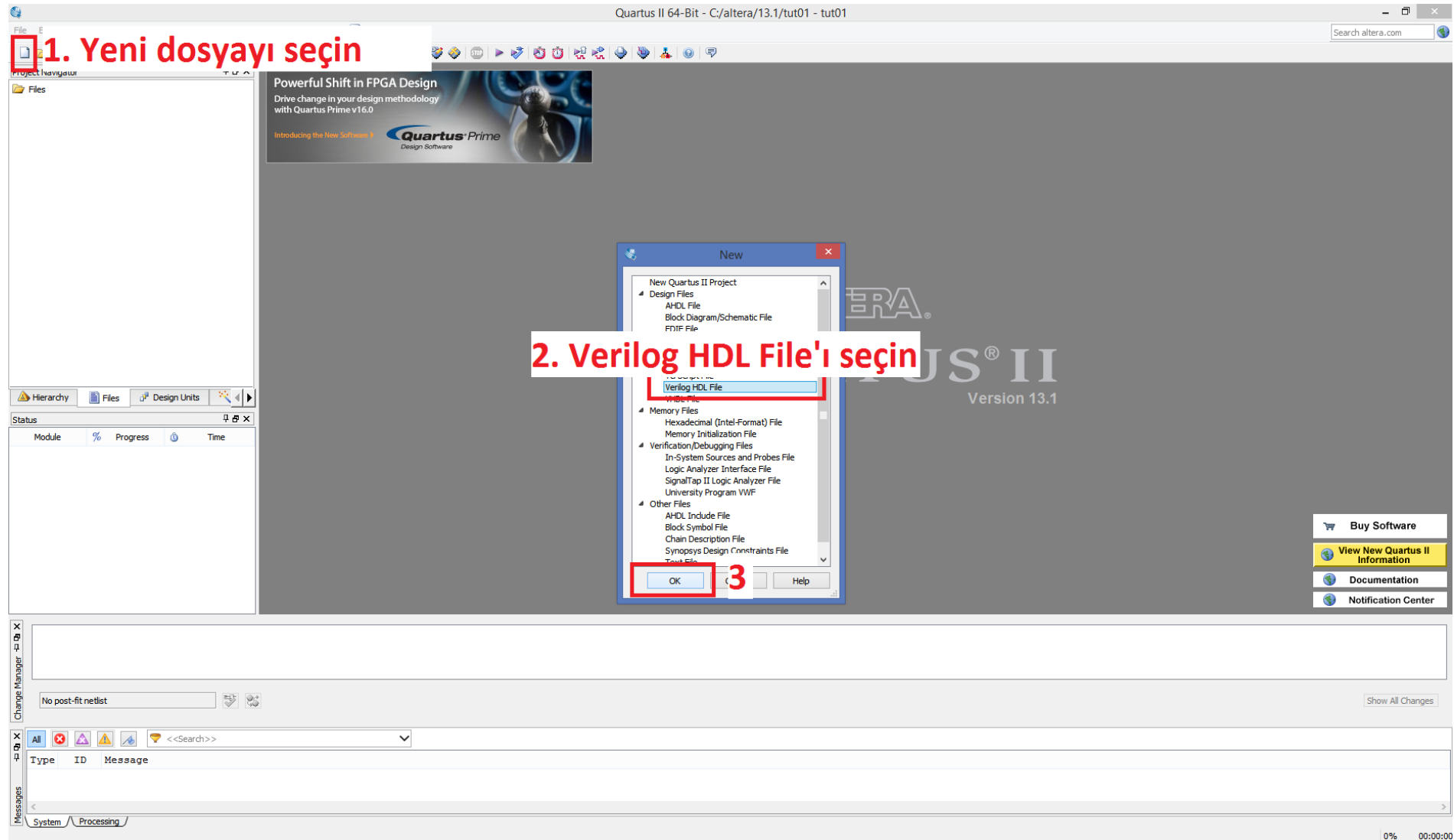
Part1: (on paper)

- Understand the given problem
- Draw truth table & write logic equation
- Simplify the equation with K-map

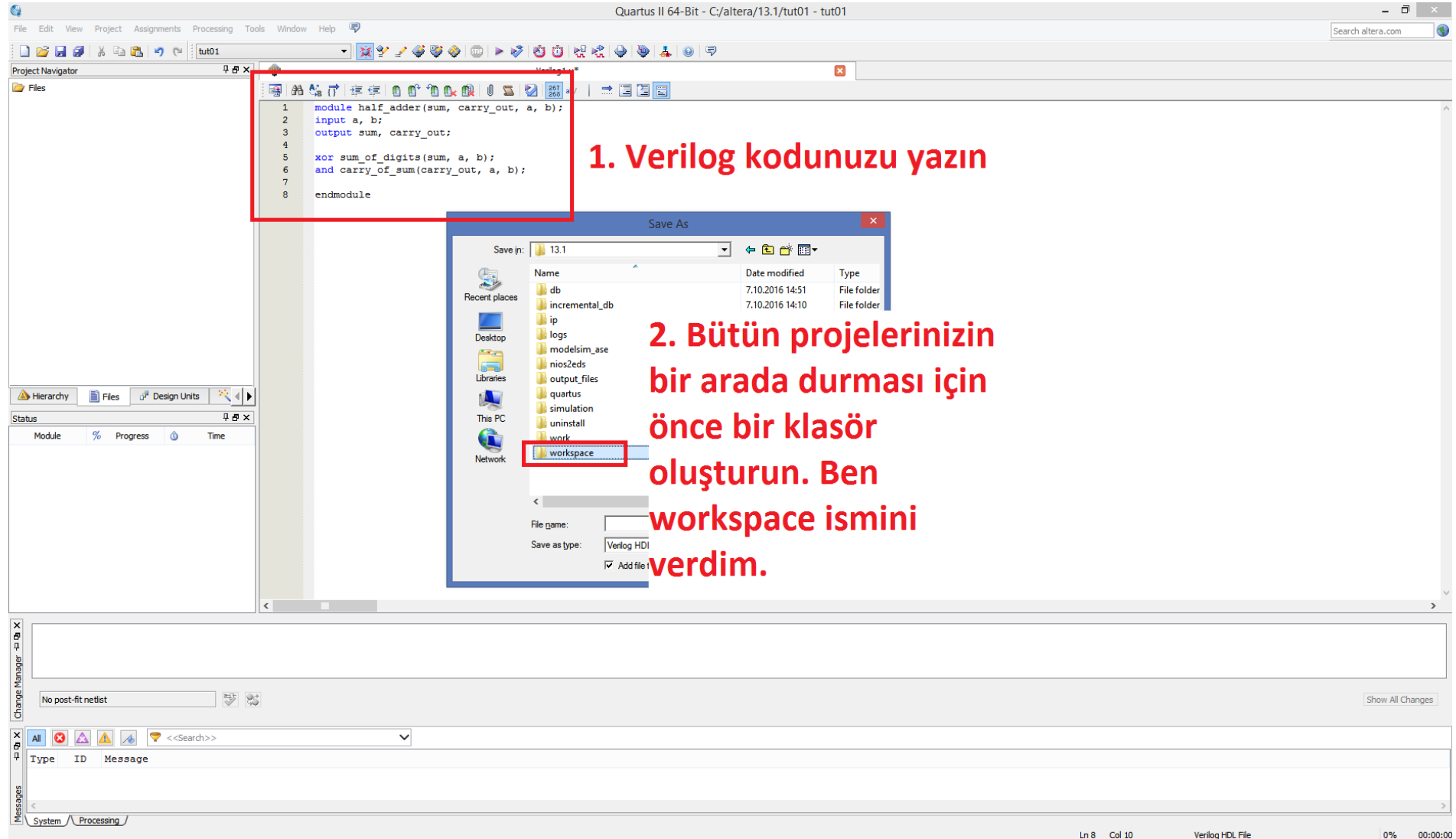
Part2:

- Implement the design with structural verilog
- Implement the design with data flow Verilog
- Running these designs on the FPGA board, separately.

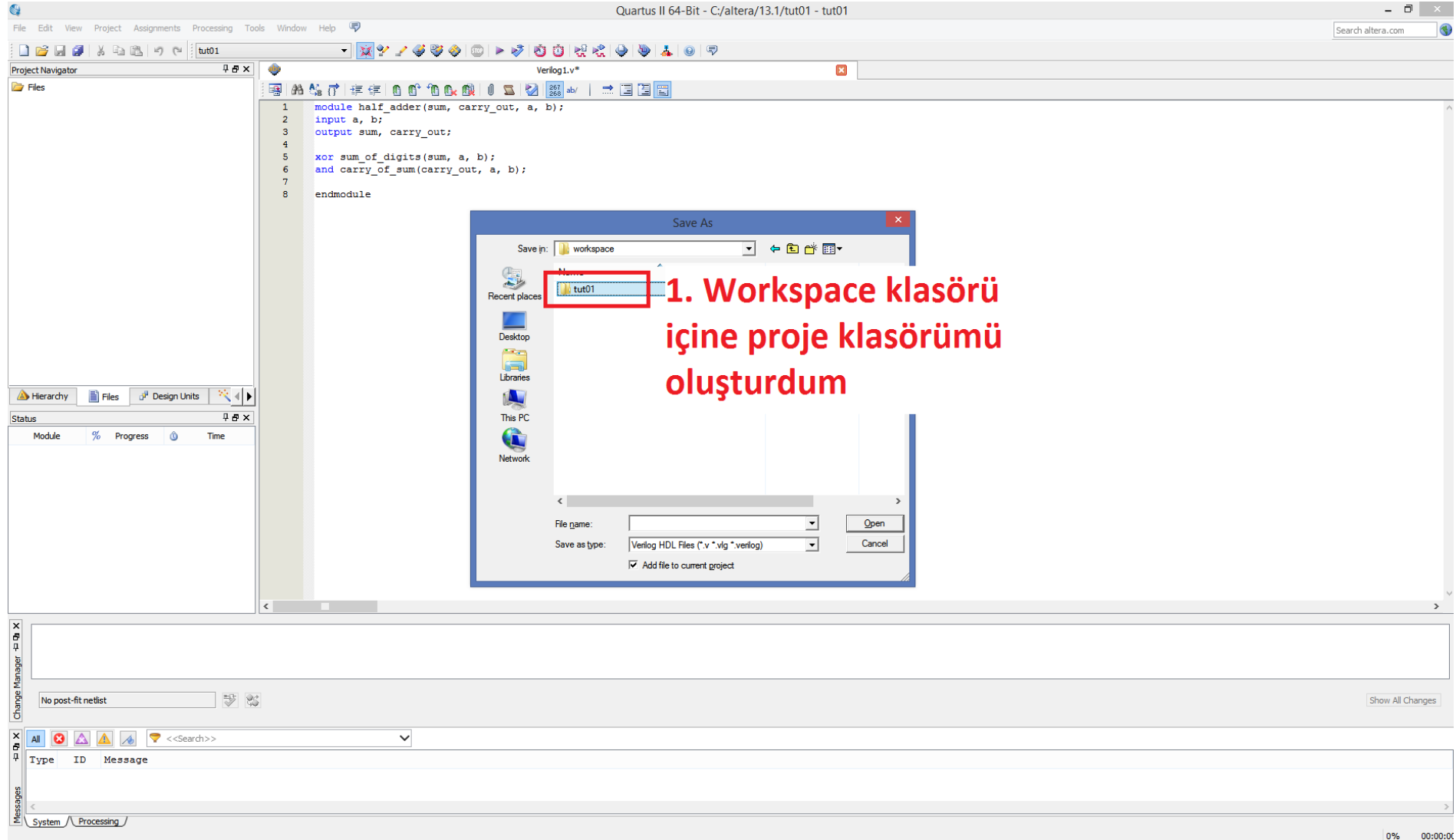
Most Common Mistakes on Previous Lab



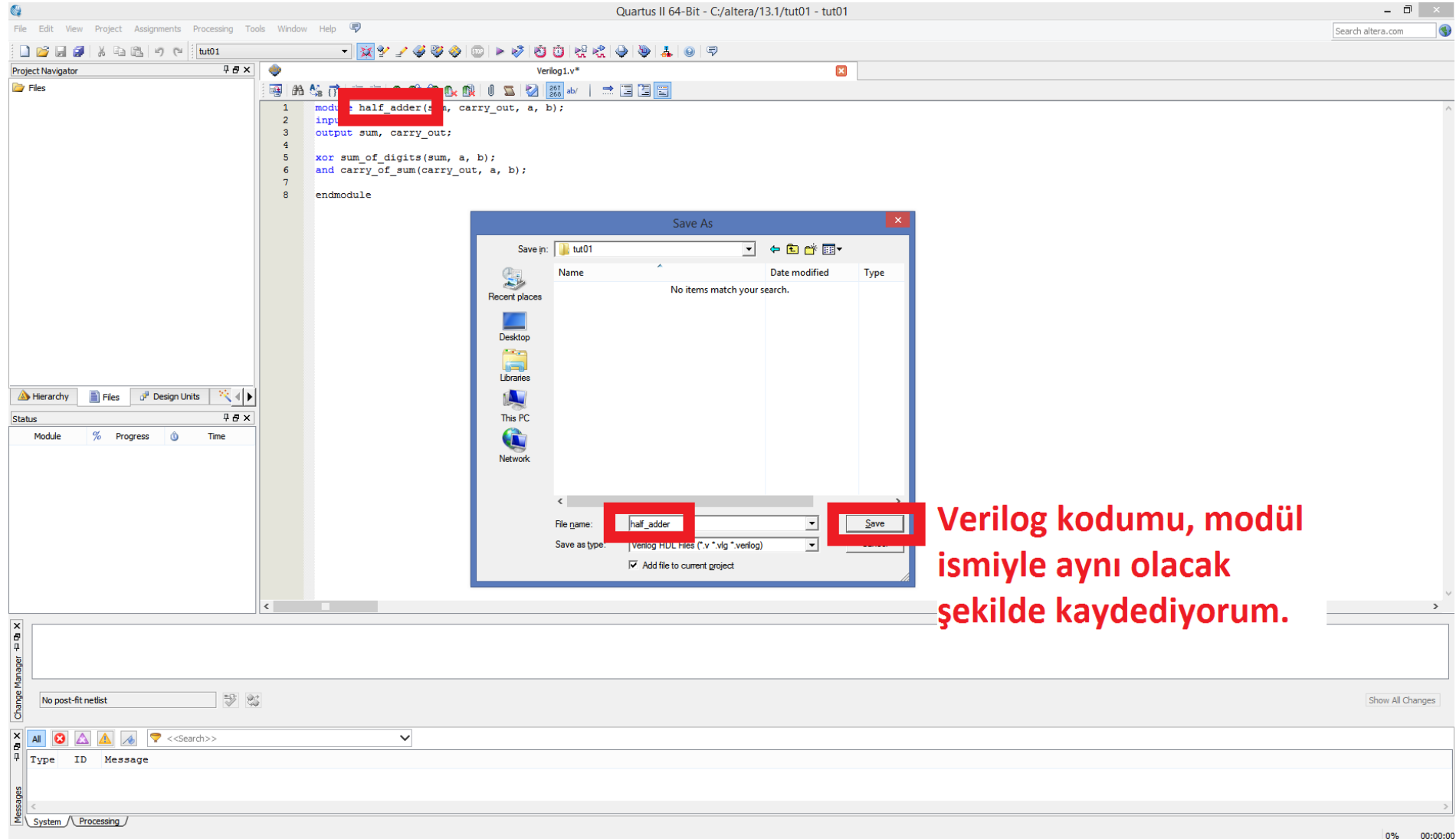
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The screenshot shows the Quartus II 64-Bit software interface with several annotations highlighting common mistakes:

- 3. Tekrar analiz ve sentez işlemini yapıyorum.** (I am repeating the analysis and synthesis process.) - Points to the 'Run' button in the top toolbar.
- 2. Ana modülümü belirtiyorum** (I am specifying my main module) - Points to the 'Set as Top-Level Entity' option in the context menu.
- Not: İlk analiz & sentez işleminden önce bunu yapabilirdim.** (Note: I could have done this before the first analysis & synthesis process.) - Points to the 'Flow Summary' window.
- 1. Top level design entity 'i yani ana modülü bulamadı.** (Top level design entity 'i, i.e. main module not found.) - Points to the error message in the Messages window: "12007 Top-level design entity 'tut01' is undefined".

The Messages window also displays the following error: "Quartus II 64-Bit Analysis & Synthesis was unsuccessful. 1 error, 0 warnings".