Solving combinational design problems

- **Step 1: Understand the problem**
  - Identify the inputs and outputs
  - Draw a truth table
- **Step 2: Simplify the logic**
  - Draw a K-map
  - Write a simplified
  - Boolean expression SOP or POS
  - Use don’t cares
- **Step 3: Implement the design**
  - Logic gates and/or Verilog
  - Run on FPGA board

To Do in these lab hour:

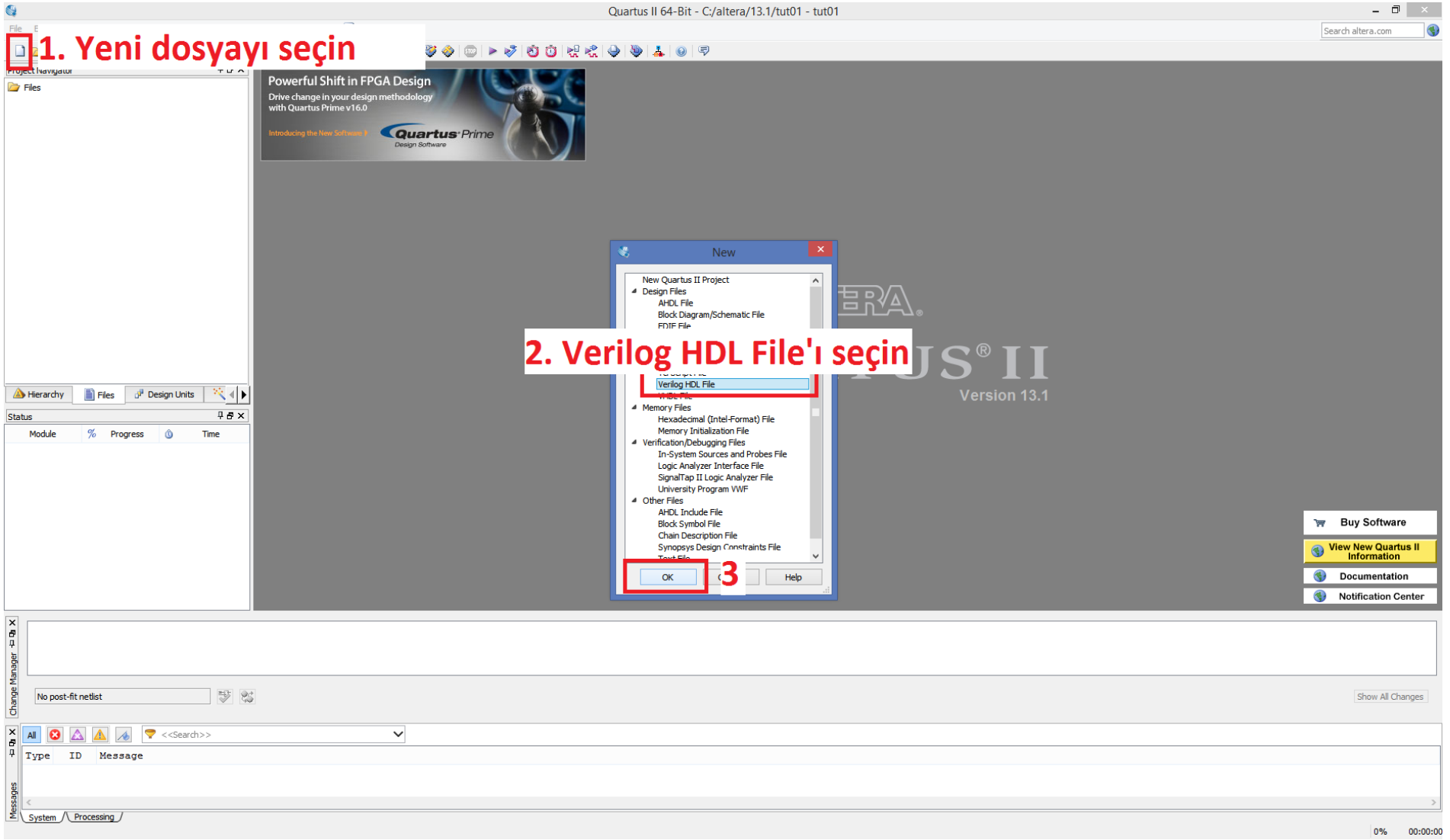
Part1: (on paper)

- Understand the given problem
- Draw truth table & write logic equation
- Simplify the equation with K-map

Part2:

- Implement the design with structural verilog
- Implement the design with data flow Verilog
- Running these designs on the FPGA board, separately.

Most Common Mistakes on Previous Lab



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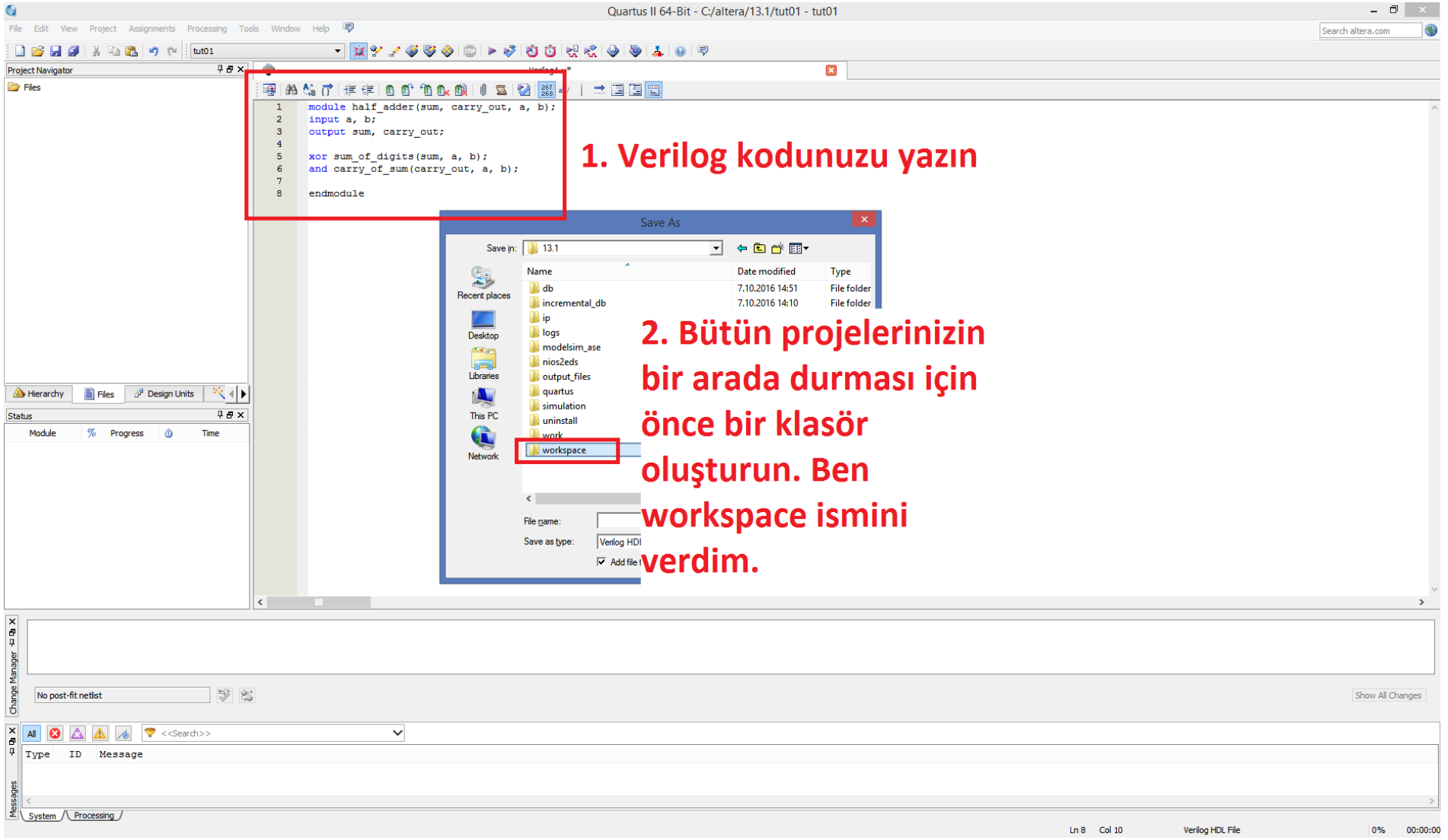

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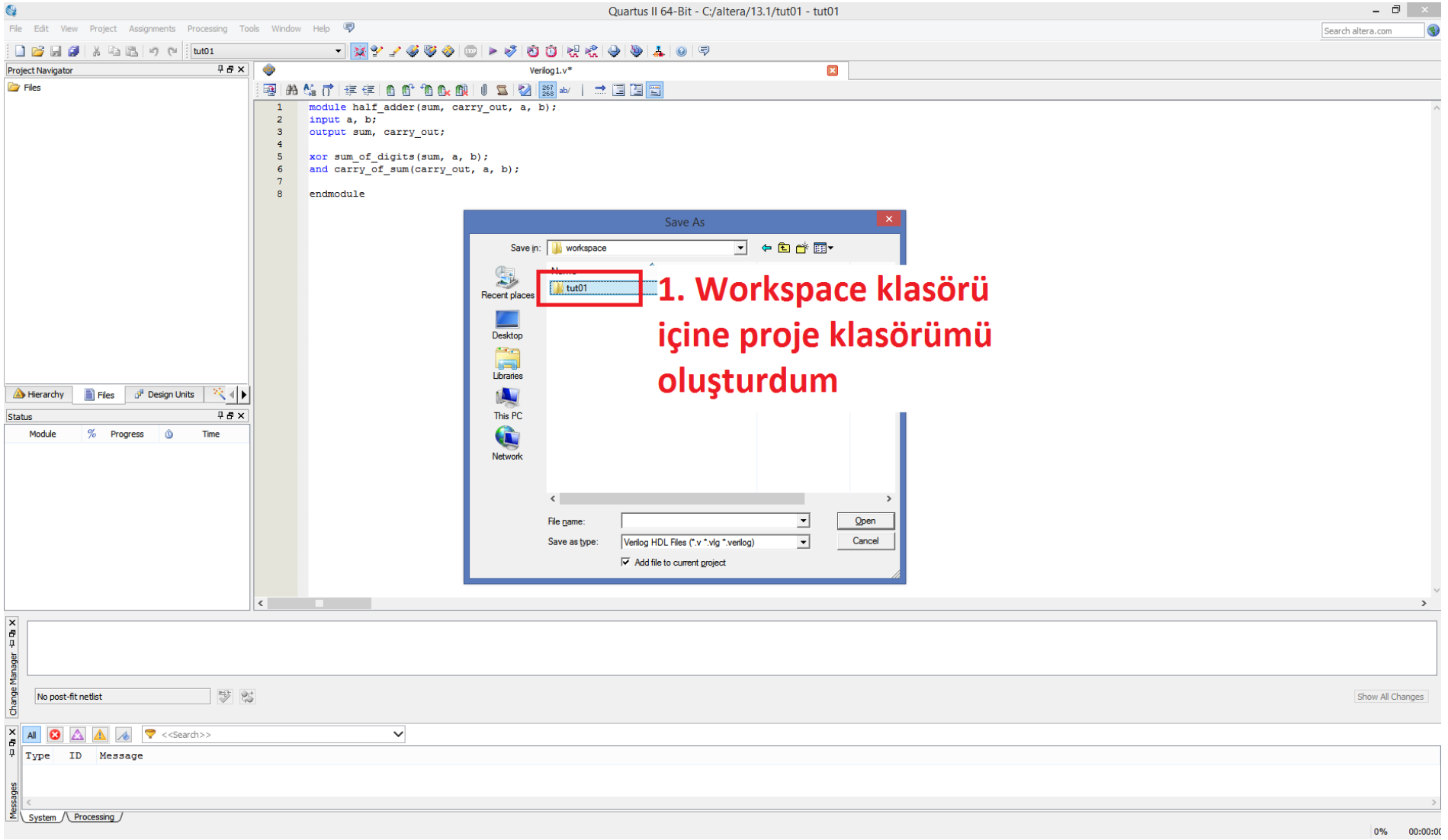

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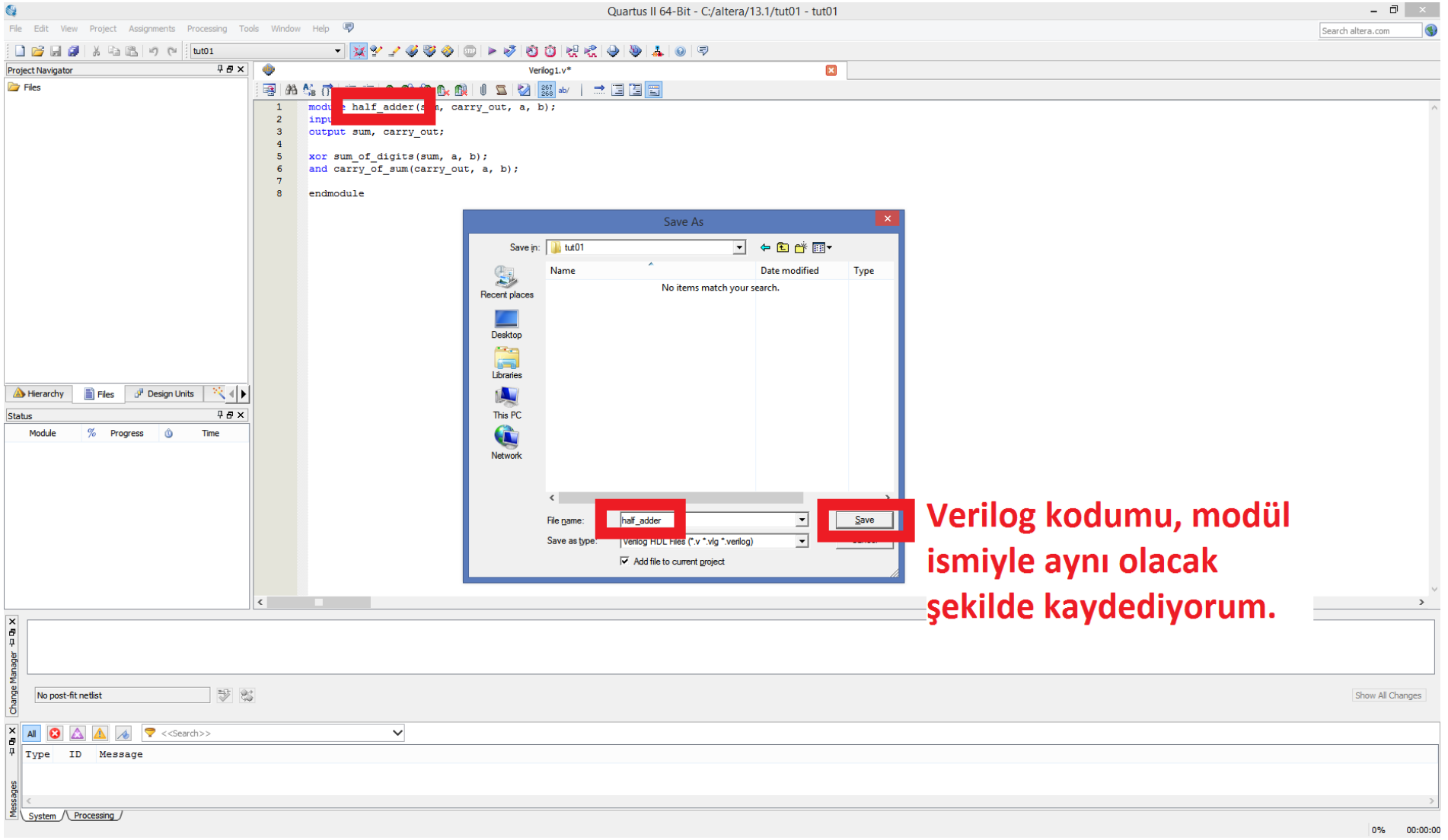

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