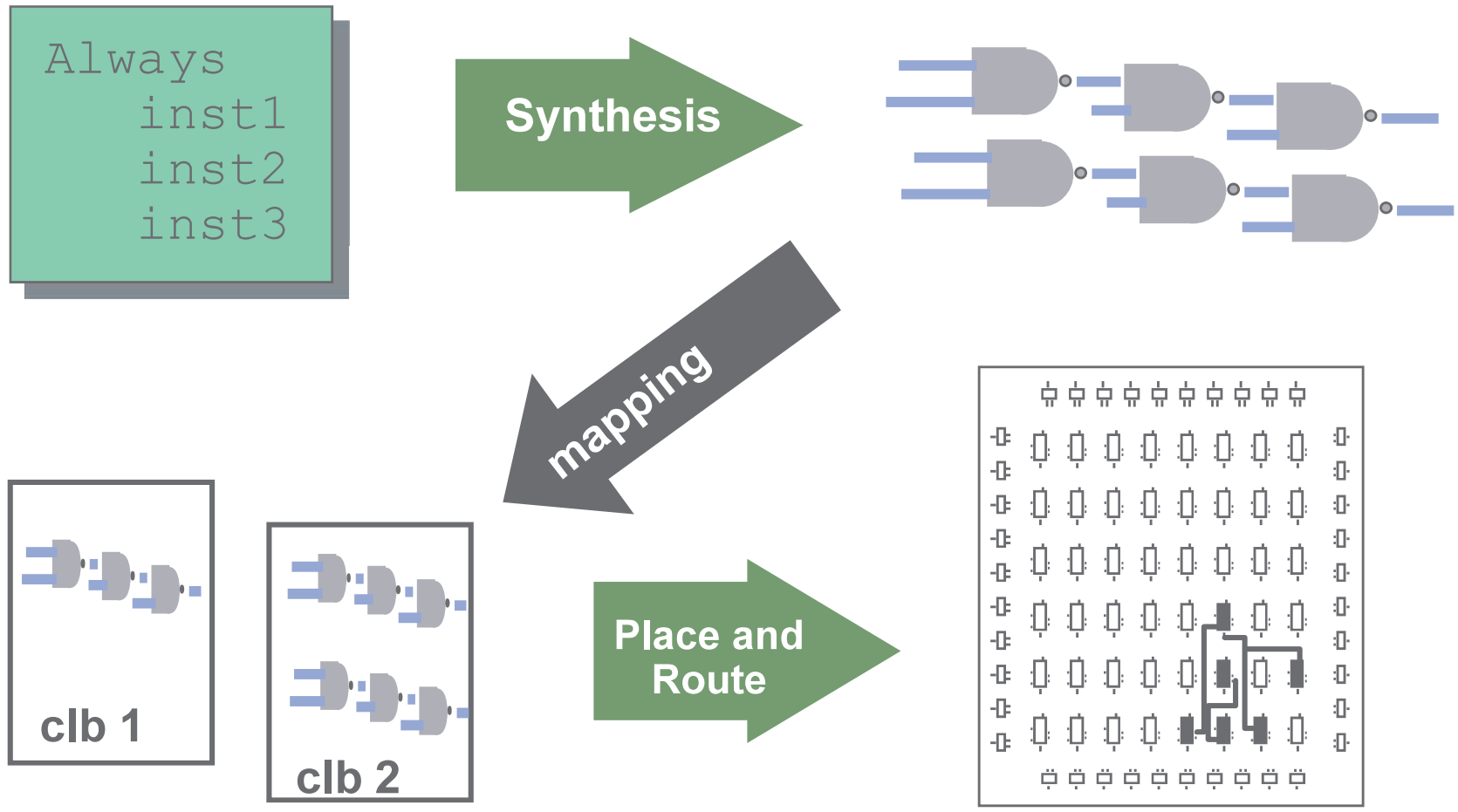
Modern Project Methodology



Module

General definition

```
module module_name ( port_list );
    port declarations;
    …
    variable declaration;
    …
    description of behavior
endmodule
```

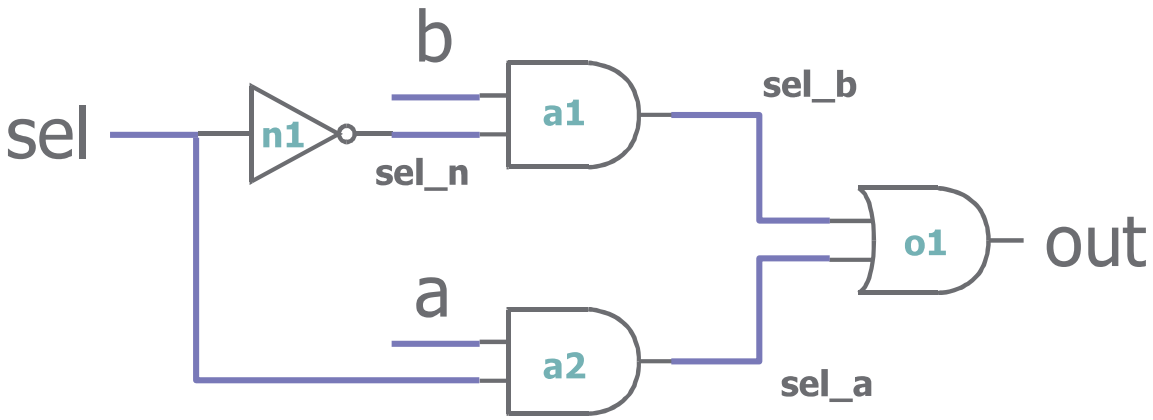
Example

```
module HalfAdder (A, B, Sum Carry);
input A, B;
output Sum, Carry;
assign Sum = A ^ B;
//^ denotes XOR
assign Carry = A & B;
// & denotes AND
endmodule
```

2. Verilog modeling Styles

- **Structural**: Logic is described in terms of Verilog gate primitives
- Example:

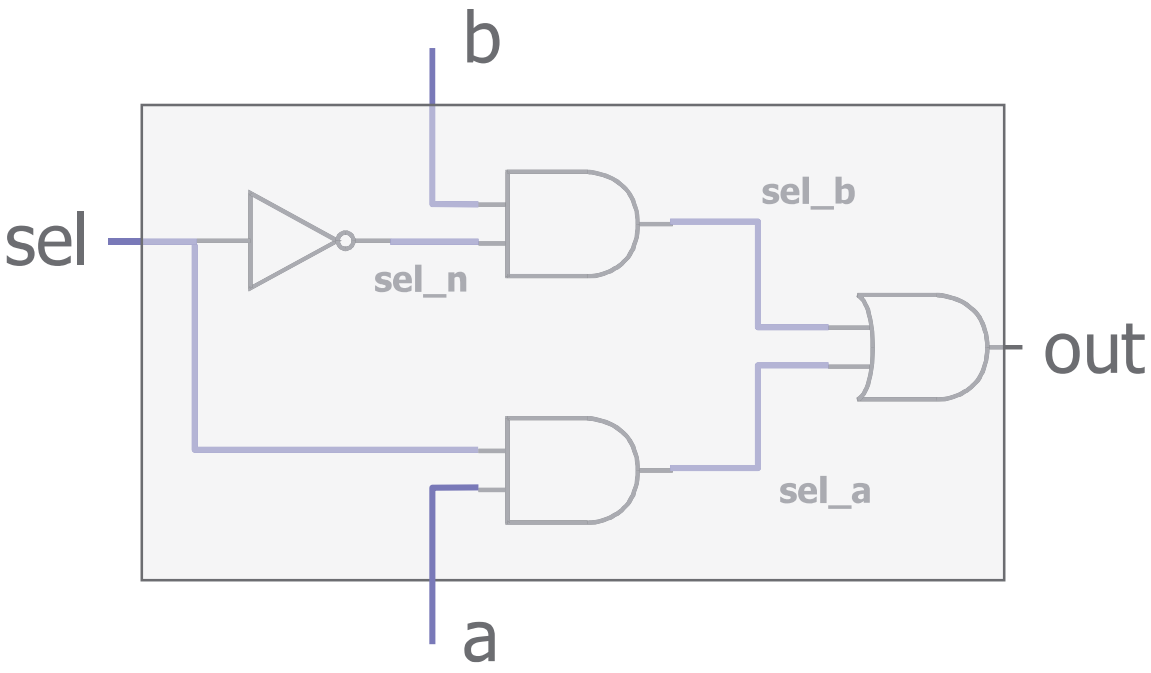
```
not  n1(sel_n, sel);
and a1(sel_b, b, sel_b);
and a2(sel_a, a, sel);
or    o1(out, sel_b, sel_a);
```



Description Styles (cont.)

- **Dataflow**: Specify output signals in terms of input signals
- Example:

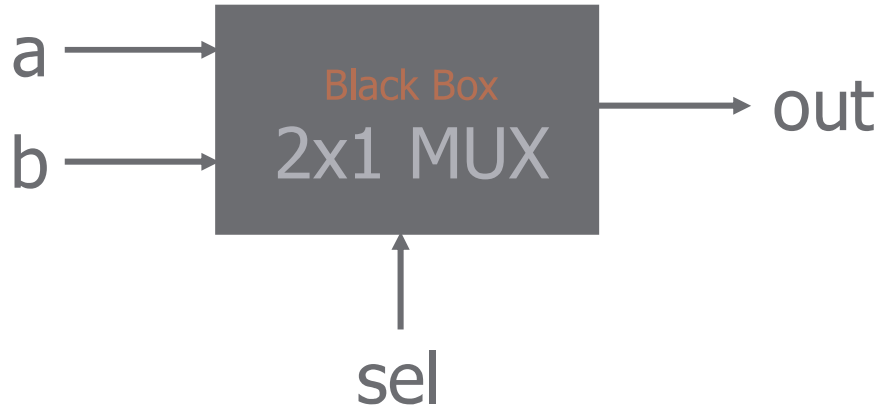
```
assign out = (sel & a) | (~sel & b);
```



Description Styles (cont.)

- **Behavioral**: Algorithmically specify the behavior of the design
- Example:

```
if (select == 0) begin
        out = b;
end
else if (select == 1) begin
        out = a;
end
```



Dataflow Modeling

- Uses continuous assignment statement
  - Format: assign [delay] net = expression;
  - Example: assign sum = a ^ b;
- **Delay**: Time duration between assignment from RHS to LHS
- All continuous assignment statements execute concurrently
- Order of the statement does not impact the design

Dataflow Modeling (cont.)

- Delay can be introduced
  - Example: assign #2 sum = a ^ b;
  - "#2" indicates 2 time-units
  - No delay specified : 0 (default)
- Associate time-unit with physical time
  - `timescale time-unit/time-precision
  - Example: `timescale 1ns/100 ps
- Timescale

  `timescale 1ns/100ps
  - 1 Time unit = 1 ns
  - Time precision is 100ps (0.1 ns)
  - 10.512ns is interpreted as 10.5ns

Dataflow Modeling (cont.)

- Example:

```
`timescale 1ns/100ps
module HalfAdder (A, B, Sum, Carry);
  input A, B;
  output Sum, Carry;
  assign #3 Sum = A ^ B;
  assign #6 Carry = A & B;
endmodule
```

Dataflow Modeling (cont.)