EN3021 Group Project - Progress as of OCT03

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October 3, 2024

Current status: 20% Complete

Completed Parts

Following parts of the project have been completed as of October 03:

- The paper design of the single-cycle micro-architecture
- Control signals for each class of instruction
- Planning of hardware implementation of the following components
  - Instruction and data memories
  - Registry file
  - ALU

Paper Design of the Single-cycle Micro-architecture

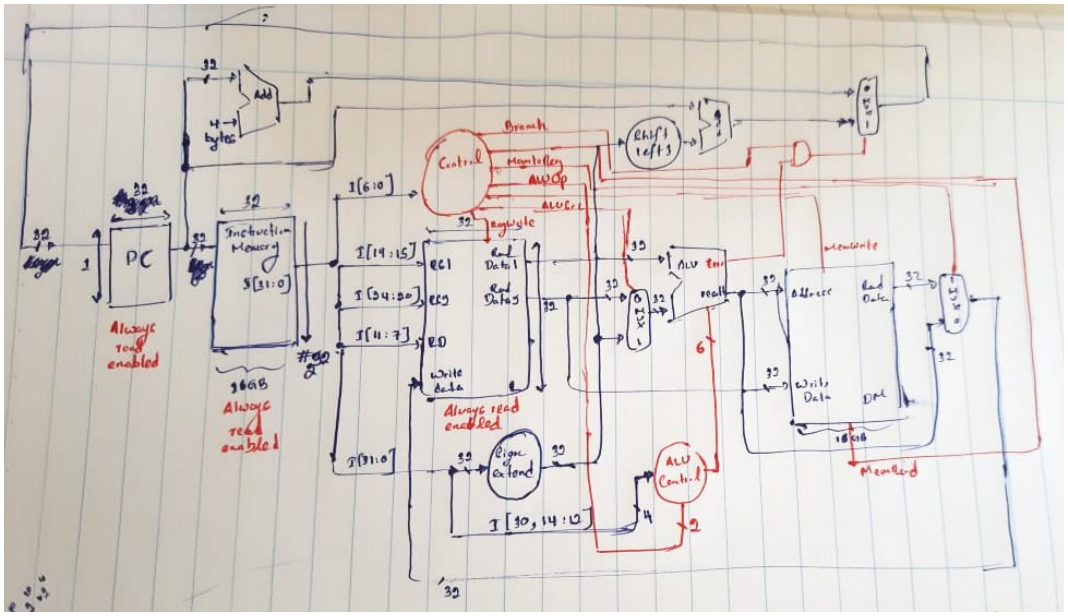

Figure 1: Paper design

Control Signals

Here there's the following set of control signals:

- `Branch`
- `MemRead`
- `MemtoReg`
- `ALUOp[1:0]`
- `MemWrite`
- `ALUSrc`
- `RegWrite`

.

And these signals change according to each instruction class as below:

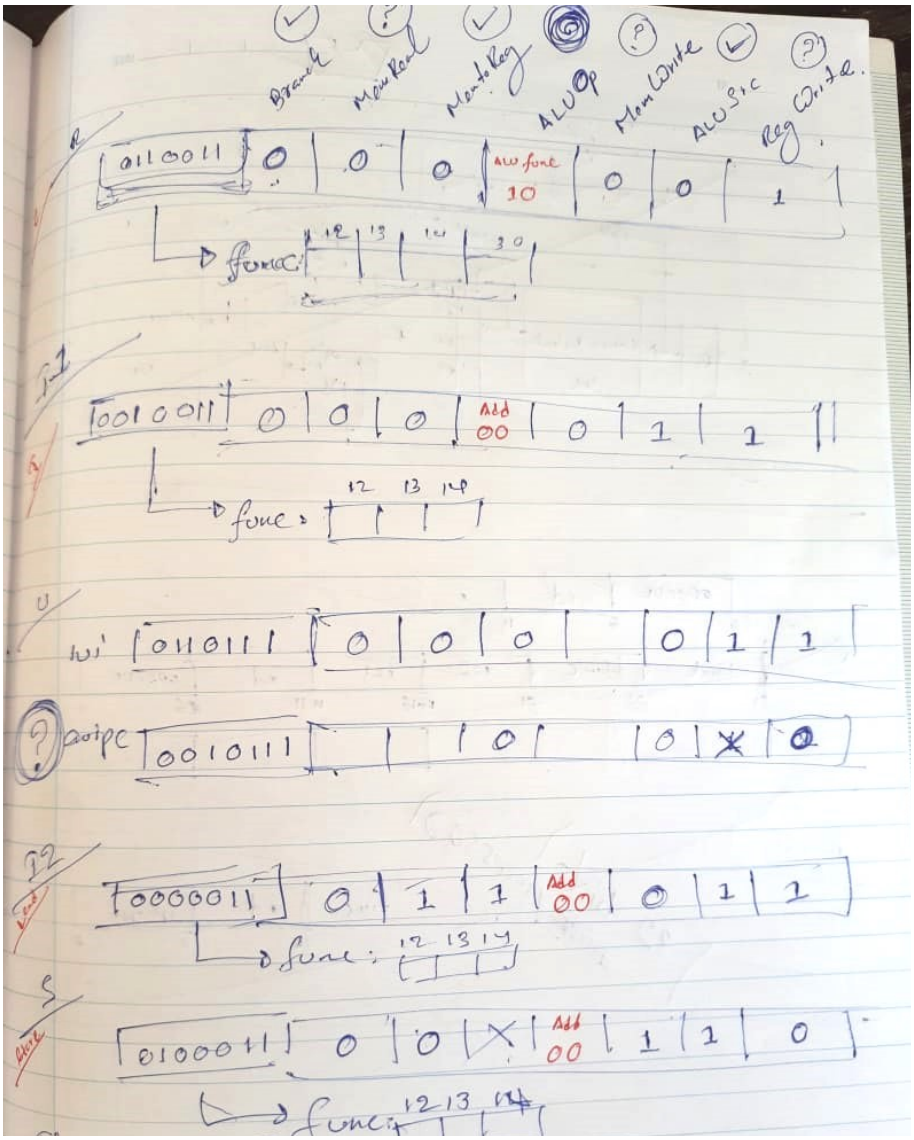

Figure 2: Control signals

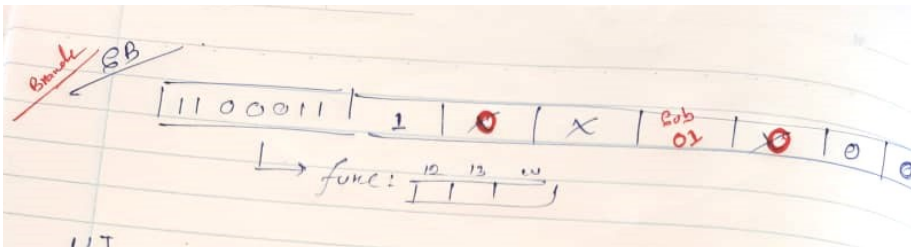

Figure 3: Control signals

Hardware Implementation

The rough architecture of some components were done as below:

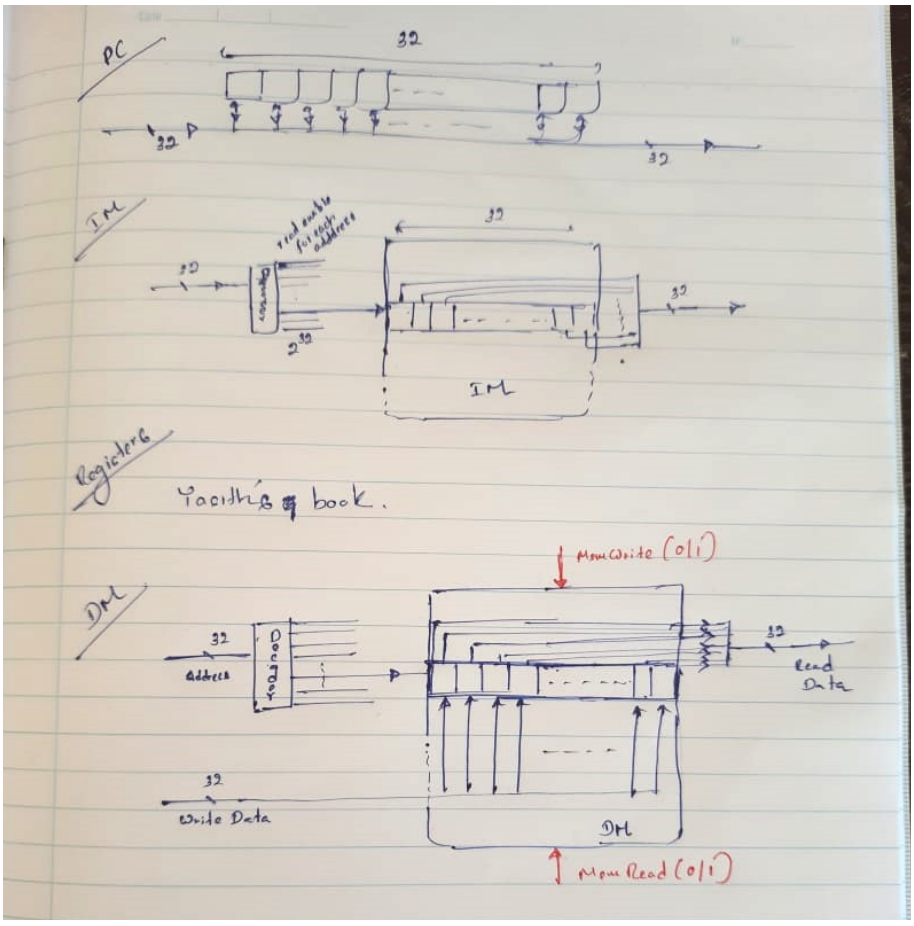

Figure 4: Implementation of PC, IM and DM

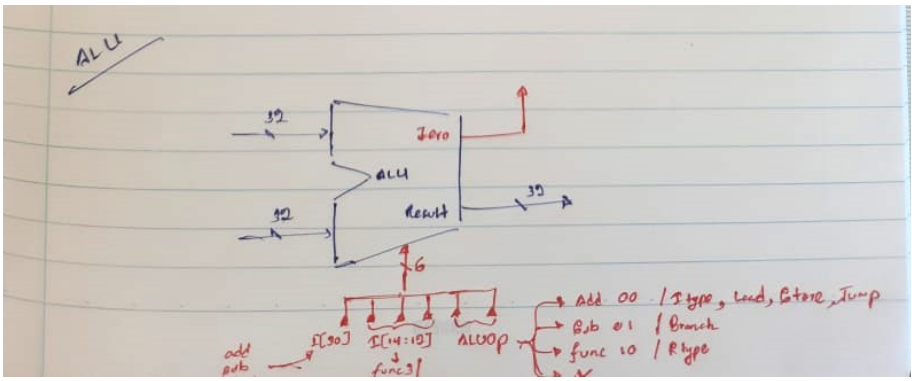

Figure 5: Implementation of the ALU

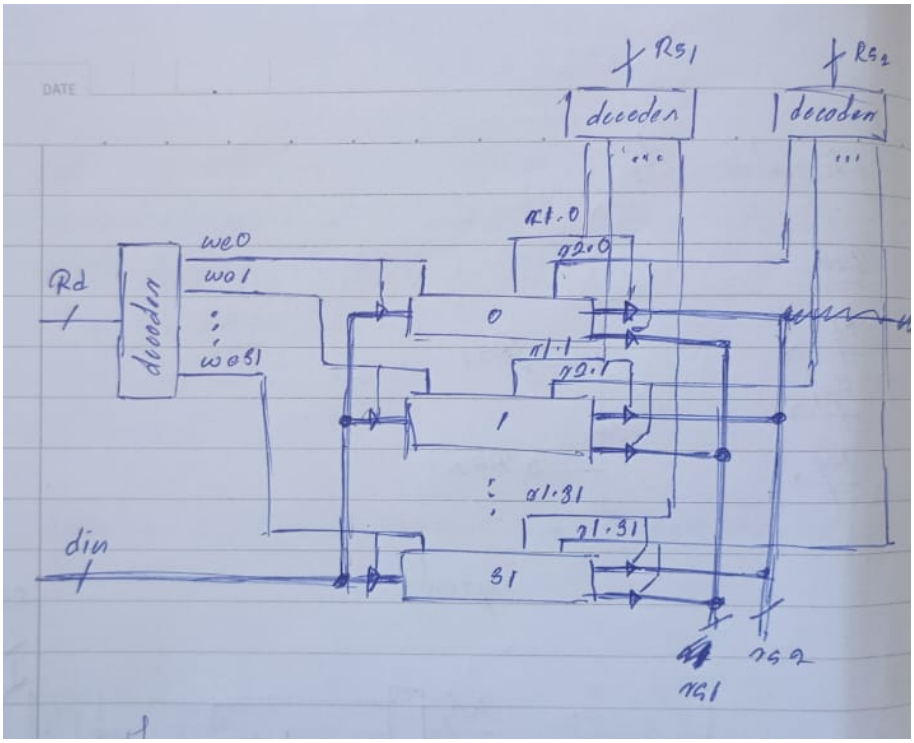

Figure 6: Implementation of the Registry File

Members' Contribution

The paper design part was done together by all team members.