1. Describe the steps that transform a program written in a high-level language such as C into a representation that is directly executed by a computer processor.
2. Assume a color display using 8 bits for each of the primary colors (red, green, blue) per pixel and a frame size of 1280 × 1024.
   a. What is the minimum size in bytes of the frame buff er to store a frame?
   b. How long would it take, at a minimum, for the frame to be sent over a 100 Mbit/s network?
3. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
   a. Which processor has the highest performance expressed in instructions per second?
   b. If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.
   c. We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?
4. Consider two different implementations of the same instruction set architecture. The instructions can be divided into four classes according to their CPI (class A, B, C, and D). P1 with a clock rate of 2.5 GHz and CPIs of 1, 2, 3, and 3, and P2 with a clock rate of 3 GHz and CPIs of 2, 2, 2, and 2. Given a program with a dynamic instruction count of 1.0E6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?
   a. What is the global CPI for each implementation?
   b. Find the clock cycles required in both cases.
5. The Pentium 4 Prescott processor, released in 2004, had a clock rate of 3.6 GHz and voltage of 1.25 V. Assume that, on average, it consumed 10 W of static power and 90 W of dynamic power. The Core i5 Ivy Bridge, released in 2012, had a clock rate of 3.4 GHz and voltage of 0.9 V. Assume that, on average, it consumed 30 W of static power and 40 W of dynamic power.
   a. For each processor fi nd the average capacitive loads.
   b. Find the percentage of the total dissipated power comprised by static power and the ratio of static power to dynamic power for each technology.
   c. If the total dissipated power is to be reduced by 10%, how much should the voltage be reduced to maintain the same leakage current?
6. Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm2.
   a. Find the yield for both wafers.
   b. Find the cost per die for both wafers.
   c. If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, fi nd the die area and yield.

d. Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm2.

7. State Moore's law and use the web to find new technologies that may allow it to continue to the future.
8. Find out the speed of the fastest computer in existence today.