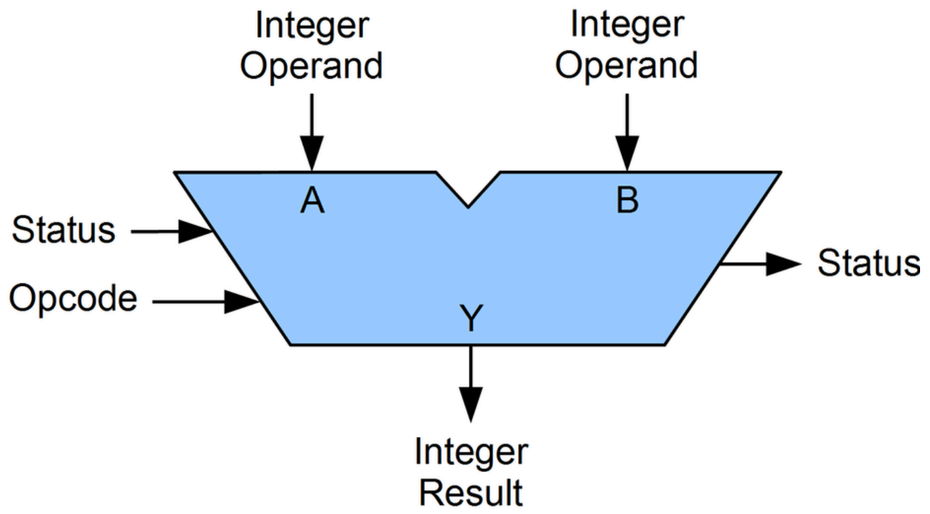
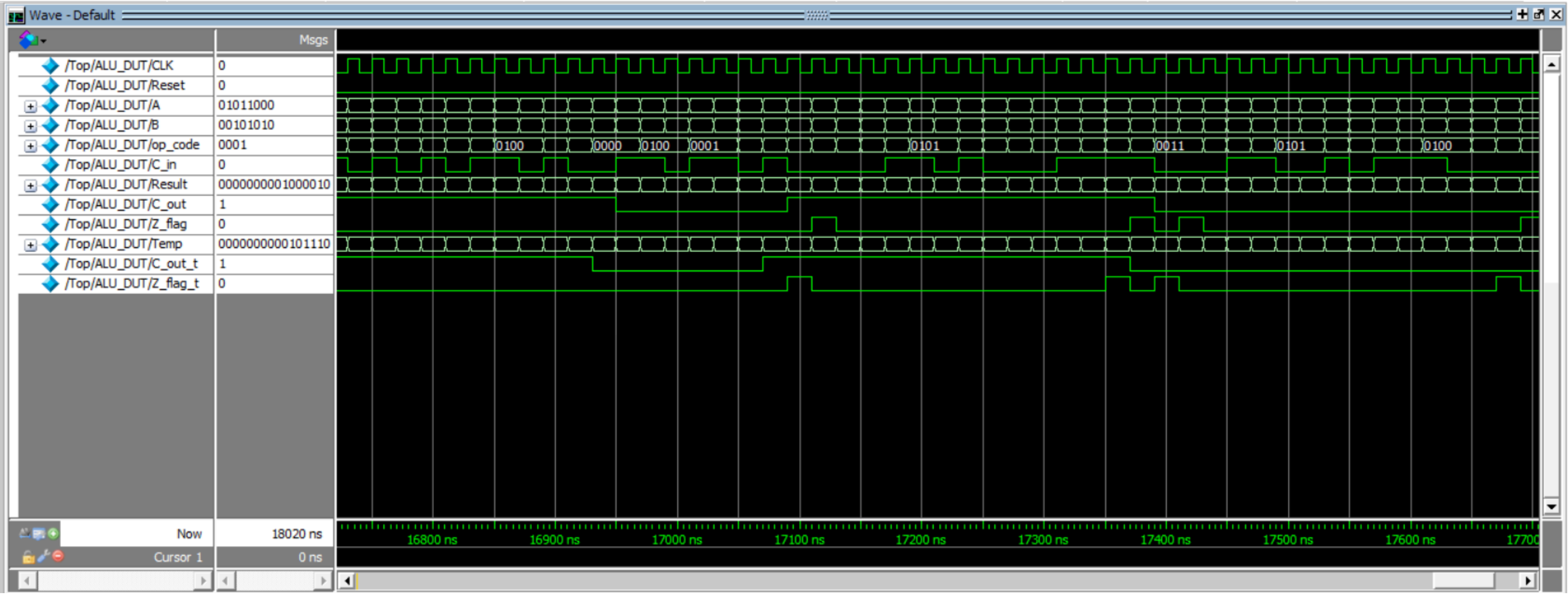
ALU TEST
USING
UVM



Presented By
Yasser Mohamed

wave


Wave - Default
Msgs
/Top/ALU_DUT/CLK
/Top/ALU_DUT/Reset
/Top/ALU_DUT/A
/Top/ALU_DUT/B
/Top/ALU_DUT/op_code
/Top/ALU_DUT/C_in
/Top/ALU_DUT/Result
/Top/ALU_DUT/C_out
/Top/ALU_DUT/Z_flag
/Top/ALU_DUT/Temp
/Top/ALU_DUT/C_out_t
/Top/ALU_DUT/Z_flag_t
0
0
01011000
00101010
0001
0
0000000010000010
1
0
0000000000101110
1
0
0100
0000
0100
0001
0101
0011
0101
0100
Now
18020 ns
Cursor 1
0 ns
16800 ns
16900 ns
17000 ns
17100 ns
17200 ns
17300 ns
17400 ns
17500 ns
17600 ns

QUESTA COVERAGE REPORT

Number of tests run:	1
Passed:	1
Warning:	0
Error:	0
Fatal:	0

List of tests included in report...

Coverage Summary by Structure:

Design Scope	Coverage (%)
uvm_pkg	100.00%
uvm_callbacks	100.00%
uvm_phase	100.00%
uvm_component	100.00%
ALU_pkg	100.00%
Coverage_Collector	100.00%

Coverage Summary by Type:

Weighted Average:				100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Coverage (%)**
Covergroup	13	13	0	100.00%
Assertion Attempted	22	22	0	100.00%
Assertion Failures	22	0	-	0.00%
Assertion Successes	22	22	0	100.00%

COVERAGE SUMMARY BY INSTANCE

ALU_PKG

Scope: /ALU_pkg

Coverage Summary By Instance:

Scope	TOTAL	Cvg	Cover	Statement	Branch	UDP Expression	UDP Condition	FEC Expression	FEC Condition	Toggle	FSM State	FSM Trans
TOTAL	100.00%	100.00%	--	--	--	--	--	--	--	--	--	--
Coverage_Collector	100.00%	100.00%	--	--	--	--	--	--	--	--	--	--

Questa Covergroup Coverage Report

Covergroups / Instances	Total Bins	Covered Bins	Coverage
Covergroup ALU_signals	13	13	**100.00%**
Instance \/ALU_pkg::Coverage_Collector::ALU_signals per_instance true	13	13	**100.00%**

Covergroup type:ALU_signals				**100.00%**
Coverpoints / Bins	**At Least**	**Hits**	**Goal**	**Coverage**
Coverpoint: reset_case			100.00%	**100.00%**
Coverpoint: carry_input_case			100.00%	**100.00%**
Coverpoint: op_code_case			100.00%	**100.00%**
Coverpoint: input_A_case			100.00%	**100.00%**
Coverpoint: input_B_case			100.00%	**100.00%**

Details

reset case

Covergroup instance:\/ALU_pkg::Coverage_Collector::ALU_signals				100.00%
Coverpoints / Bins	**At Least**	**Hits**	**Goal**	**Coverage**
Coverpoint: reset_case (covered 2 of 2 bins) (missing 0 of 2 bins)			100.00%	**100.00%**
bin auto['b0]	1	449		**Covered**
bin auto['b1]	1	1		**Covered**

carry input case

Coverpoint: carry_input_case (covered 2 of 2 bins) (missing 0 of 2 bins)			100.00%	**100.00%**
bin auto[0]	1	247		**Covered**
bin auto[1]	1	203		**Covered**

opcode case

Coverpoint: op_code_case (covered 5 of 5 bins) (missing 0 of 5 bins)			100.00%	**100.00%**
bin ADD	1	71		**Covered**
bin SUB	1	72		**Covered**
bin MULT	1	65		**Covered**
bin DIV	1	74		**Covered**
bin XOR	1	83		**Covered**

two inputs case

Coverpoint: input_A_case (covered 2 of 2 bins) (missing 0 of 2 bins)			100.00%	**100.00%**
bin all_ones	1	4		**Covered**
bin all_zeros	1	5		**Covered**
default bin random_data	1	441		**Occurred**
Coverpoint: input_B_case (covered 2 of 2 bins) (missing 0 of 2 bins)			100.00%	**100.00%**
bin all_ones	1	2		**Covered**
bin all_zeros	1	1		**Covered**

Coverage Summary By Instance

UVM_pkg

Scope	TOTAL	Cvg	Cover	Statement	Branch	UDP Expression	UDP Condition	FEC Expression	FEC Condition	Toggle	FSM State	FSM Trans	Assertion Attempted	Assertion Passes	Assertion Failures	Assertion Successes
TOTAL	100.00%	--	--	--	--	--	--	--	--	--	--	--	100.00%	--	0.00%	100.00%
uvm_callbacks	100.00%	--	--	--	--	--	--	--	--	--	--	--	100.00%	--	0.00%	100.00%
uvm_phase	100.00%	--	--	--	--	--	--	--	--	--	--	--	100.00%	--	0.00%	100.00%
uvm_component	100.00%	--	--	--	--	--	--	--	--	--	--	--	100.00%	--	0.00%	100.00%

Recursive Hierarchical Coverage Details

Weighted Average:				100.00%
Coverage Type	**Bins**	**Hits**	**Misses**	**Coverage (%)**
Assertion Attempted	22	22	0	100.00%
Assertion Failures	22	0	-	0.00%
Assertion Successes	22	22	0	100.00%

THANK YOU

If you are interested in anything about UVM, don’t hesitate to contact me.